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SELECTIVE METALLIZATION AND PASSIVATION OF DRY-TRANSFERRED CARBON NANOTUBES IN FIELD-EFFECT TRANSISTORS

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ABSTRACT

The use of selective atomic layer deposition (ALD) of platinum and alumina was investigated for top-clamping and passivation of contacts of suspended pristine single-walled carbon nanotubes (SWNTs). This wet-chemical-free process offers an interesting alternative to lithography-based methods as it avoids degradation of the transfer characteristics by resist residues or amorphous carbon deposition on the carbon nanotubes (CNTs) in field-effect transistor (FET) configuration. It was observed that the annealing and clamping effect can be used not only to obtain lower contact resistances and higher signal to noise ratio (SNR), but also to induce, what appears to be, band gap opening in metallic nanotubes. On average, a current increase of more than one order of magnitude and SNRs as high as 200 could be observed for metallized and passivated small-gap semiconducting CNTs.

INTRODUCTION

The performance of CNFETs is strongly affected by any wet chemical processing [1]. Ultra-clean CNT dry-transfer methods [2, 3] offer an interesting alternative to on-chip growth, in particular as they also allow for CNT pre-characterization and a fair degree of position control during the placement process. These non-top-clamped CNTs can suffer from strong contact resistance fluctuations and relatively low current levels (nA range). Wet chemical and resist free methods for top-contacting include shadow masking [4], electron beam welding [5] and mask free processes such as selective atomic layer deposition (ALD) [6, 7]. Passivation prevents the long-term degradation of contacts in ambient atmosphere [8].

EXPERIMENTAL

To investigate the effect of annealing and of top-clamping two different types of devices were used – single and fourfold receiving pair devices with different channel lengths (see Figure 1). Multiple devices from a single CNT are in particular interesting to investigate the variation in contact resistance and current fluctuation.

The devices were assembled by using dedicated growth substrates and a micromanipulator (with 3 orthogonally placed piezoelectric actuators) to transfer CNTs onto the receiving substrates [3] (see Figures 2,3). The CNTs were grown on an oxidized silicon substrate in a chemical vapor deposition (CVD) process using iron nanoparticles as catalysts [9]. The hereby produced CNTs typically range between 1.5 and 2.5 nm in diameter. The receiving substrates were fabricated on silicon wafers (see Figure 2). First, an insulating silicon nitride layer was deposited by plasma enhance chemical vapor deposition

Figure 1: The employed device architectures consisted of single as well as multiple CNFETs per tube.

Figure 2: The receiving substrates were fabricated using multiple e-beam lithography (EBL) and UV-lithography (UVL) steps. 2x2 cm chips with gold EBL markers were used. To pattern L1 AR-N 7520.17 was employed as a resist. For L2 either XR1541.006 was used for ion milling or AR-P 617.06 + AR-P 672.02 for lift-off. L3 was fabricated with AZ 6612 as the mask.

(PECVD) and patterned by reactive ion etching (RIE). Onto this structured layer, electrodes were deposited either by a conventional lift-off process (for electrodes larger than 250 nm) or by a top-down ion milling approach (electrodes smaller than 250 nm, down to 100 nm) [10]. In order to be compatible with the dry-transfer, the nitride and silicon layer were simultaneously patterned in a Bosch process by inductively-coupled plasma reactive ion etching (ICP-RIE).

Figure 3: To assemble the CNFET devices a manually controlled micromanipulator set-up was used. The growth substrate was hereby fixed to the movable arm and the electric current was constantly monitored until a CNT was successfully dry-transferred.

To be able to differentiate the annealing effect, the metallization effect and the passivation effect, they were executed successively with electrical characterization in between (see Figure 4). The selective platinum deposition was performed at 300°C with alternating pulses of MeCpPtMe_3 and oxygen. The oxygen pressure hereby determines the nucleation delay on non-catalyzing surfaces [11]. Thus, growth is expected only on the palladium electrodes. Catalytic dissociation of the platinum precursor on palladium surfaces was observed from 275°C upwards. To deposit 10 nm of platinum (≈ 250 cycles, Pt pulse: 1s, O_2 pulse: 5s) the pressure was 15 mTorr. For 20 nm (≈ 500 cycles) it was reduced to 7.5 mTorr to prevent short-circuiting. All annealing and metallization steps were executed at the same temperature (300°C). Subsequently the devices were passivated by depositing a 25 nm alumina ALD layer (TMA + H_2O) at 200°C. The alumina selectively deposits everywhere, except on the CNT, due to its chemical inertness. Only if defects are present on a CNT, alumina beads can nucleate in that area. Previous work reported no significant growth delay of alumina deposition on platinum [12].

The electrical characterization was performed in a synthetic dry air atmosphere and while continuously pulsing and sweeping the gate (standard = ± 2 V, see Figure 5). This approach has been demonstrated to reduce the baseline drift [13]. Measurements were performed for one hour each (720 sweeps). For the analysis the mean and the standard deviation of the source-drain current (I_{sd}) over 50 min were used.

Figure 4: After the dry-transfer the devices, inside the ceramic package, were annealed, metallized, and finally, passivated.

Figure 5: Electrical characterization was performed by continuously sweeping and pulsing the gate voltage. For the data analysis the time range indicated in brackets was used as to avoid the regime where current annealing can appear and to evade data glitches at the end.

RESULTS & DISCUSSION

As seen in Figure 6, post-transfer annealing at 300°C leads to an average 18-fold increase in current, whereas metallization resulted in a further 9-fold enhancement.

For fourfold receiving pair devices (Figure 7) directly after transfer, typically only the current of one or two segments was indistinguishable from noise. While the current level can be the limiting factor in some electronic applications, for most sensing applications the SNR (here defined as the mean current value divided by the current fluctuation) is decisive. The annealing gave rise to a linear increase in SNR in the initially low current segments (see Figure 8).

Figure 9 shows that after 3 h annealing the SNR converges to a steady value. The metallization leads to a further increase of the SNR, whereas the passivation resulted in an initial drop. This is mostly likely associated with the introduction of an oxide near the contact region. Subsequent annealing results in an increase in SNR, which may be due to either rearrangement at the CNT-Pt- Al_2O_3 interface or because of a diffusion or reduction of the residual carbon and oxygen content in the Pt ALD layer. These residues are a result of incompletely oxidized ligands during the deposition. Detailed structural and

elemental analysis of the interface would be necessary to determine the exact cause. Overall, the annealing and metallization can greatly improve the SNR ($\sim 15\times$). For most initially metallic CNTs (Figure 10,11) the heat treatment resulted in a gradual increase in gate modulation. This could be associated with the progressive opening of a bandgap due to residual strain after non-reversible rearrangement of the CNT-electrode interface at 300°C .

Figure 6: For all samples (circle = semiconducting, rhombus = metallic) annealing resulted in approximately an order of magnitude increase in current.

Figure 7: For multiple segments of a CNT an exponential increase in the current level was observed, except for the one that was already in good contact.

Figure 8: For these multiple CNT segments the annealing gradually reduced the scatter in SNR.

For semiconducting CNTs (Figure 12) annealing lead to a shift in the current level, but the subthreshold slope stayed the same. In addition, metallization resulted in a small positive threshold voltage shift, which cannot be explained by the change in work function alone.

Figure 9: Metallization and the annealing of the ALD deposited layer led to a further significant increase in current. While current levels already started converging to a value after annealing of 0.5 to 1 h, the SNR converged on a slower timescale.

Figure 10: The annealing of metallic tubes resulted in residual strain in the CNTs and band gap opening could be observed.

Figure 11: This residual strain was preserved to a slightly higher extent during metallization.

Figure 12: In semiconducting CNTs the annealing did not affect the sub-threshold slope only the saturation current level. Metallization resulted in a threshold voltage shift of approximately 0.19 V.

For both deposition of 10 and 20 nm of platinum, no short-circuiting and no platinum bead formation on CNTs was observed. The yield of the Pt ALD process was close to 100%, whereas the yield of the alumina ALD at 200°C was lower at 75%. For higher alumina ALD deposition temperatures, the yield dropped (50% at 250°C).

CONCLUSIONS

We have shown that ALD based selective metallization and passivation can be used to reliably increase the signal to noise ratio and to produce low resistance contacts while maintaining the pristine nature of carbon nanotubes.

This technique is highly scalable and also compatible with fully bonded and packaged CNTs. As the processing selectivity relies mostly on the pre-fabricated substrate, it is not limited to CNTs and could also be used with various other 1-D and 2-D materials.

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