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Hybrid Lithography based Fabrication of 3D Patterns by Deep Reactive Ion Etching

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Abstract

Electron-beam lithography (EBL) possesses tremendous capabilities in terms of patterning ultra-small features, with very low line edge roughness and high overlay accuracy. In order to reduce write times and processing steps, hybrid lithography is an interesting alternative. Here, an approach combining EBL and ultraviolet lithography (UVL) was pursued in order to pattern multi-level 3D-structures by inductively coupled plasma deep reactive ion etching (ICP-DRIE). The substrate etched hereby consisted of a silicon nitride thin film and the underlying silicon. The correlation of UVL under- and overexposures with the resist layer height and sidewall taper after development, in combination with the optimization of the ICP-DRIE selectivity in dependence of the biasing conditions and the aspect ratio dependent etch lag for small features, allowed for the accurate prediction and therefore programming of the desired structures. Further, the selectivity was tailored by introducing an oxygen pulse after the breakthrough step. This facilitated the simultaneous etching of structures with an in-plane resolution of down to 250 nm (aspect ratio 1:22) and trench depths ranging from 200 nm to 25 μm .

Graphical Abstract

Highlights

- A 2D lithography approach to etch 3D structures in a single step was developed and characterized.
- The combination of hybrid lithography and deep reactive ion etching enables the simultaneous structuring of features, in- and out-of-plane, spanning three orders of magnitude in size.
- Pattern transfer rate and taper control of a Novolac based resist were obtained by introducing an additional oxygen pulse after the breakthrough step.

Keywords

Hybrid lithography; deep reactive ion etching; pattern transfer; 3D profile etching; taper control

1. Introduction

For various nano- and microelectromechanical systems (NEMS and MEMS) based devices, complex substrate topographies with feature sizes ranging from tens of nanometers to hundreds of micrometers are required.

For the fabrication of silicon based 3D-structures, such as diffraction gratings, photonic band gap crystals, lenses, microactuators, one-step 3D patterning of a resist layer in combination with a suitable pattern transfer method can reduce process complexity. The optimization of micromachining techniques, such as deep reactive ion etching (DRIE), is mainly driven by the need for high aspect ratio features, and the desire to reduce the footprint of devices.

In order to fabricate complex resist topographies with multiple levels and various feature sizes, gray-scale direct-write laser (DWL) and nanoimprint lithography (NIL) have been widely explored. Two

photon polymerization (2PP or TPP) DWL [1], inclined X-ray lithography (XRL) [2] and multi-directional ultra violet lithography (UVL) [3], can be used to fabricate free-standing structures. In terms of resolution, UVL is limited to approximately 750 nm. For feature sizes below 250 nm 2PP-DWL is also approaching its limits [1,4]. In addition, most 2PP-DWL set-ups rely on transparent substrates. NIL can be used to pattern very small, as well as very large features, and overlay accuracy on the order of 20 nm has been demonstrated by using Moiré fringes [5]. It's only drawback is the prior need for master fabrication and limitations in terms of resist choice [6]. EBL on the other hand, offers both high resolution [7] and high overlay accuracy [8]. E-beam gray scale lithography has been demonstrated [9], also in combination with DRIE [10], but is very time intensive.

The use of sequential resist patterning processes, also referred to as hybrid lithography, can significantly reduce the pattern fabrication time, and reduces the introduction of artefacts.

Fig. 1. **a)** CNTFETs, consisting of a source, drain and gate electrode, were fabricated in a dry-transfer process. The two scanning electron microscopy (SEM) images show the two commonly used architectures. The fabrication of multiple FETs from a single CNT is in particular interesting for the investigation of fundamental properties and to obtain statistical data about the contact quality. **b)** SEM images of an integrated thermal actuator (TA) for the on-chip straining of SWCNTs. To fabricate these structures, a silicon-on-insulator (SOI) wafer with a 5 μm device layer thickness was used. Hereby a narrow gate electrode spacing was critical in order to keep the channel distance low, as SWCNTs with a finite length (typically 10 μm) were used for the dry-transfer. For electrical characterization see [11].

Common combinations include nano-imprint lithography (NIL) and ultra violet lithography (UVL) [12,13] or electron beam lithography (EBL) and UVL, deep-UV lithography (DUVL) [14–16] or XRL [17].

The combination of hybrid or gray-scale lithography and DRIE to create 3D structures has been explored for example to facilitate capacitive read-out of closely spaced electrodes [18] (EBL + UVL), to fabricate micro-compressors [19] (UVL gray-scale) and phase Fresnel lenses [20] (UVL gray-scale).

Here, a combination of EBL and UVL was chosen to pattern a substrate consisting of an insulating silicon nitride layer on a silicon structural layer by DRIE. The aim was to pattern features with an in- and out-of-plane resolution of less than 250 nm, and trench aspect ratios of more than 20:1. This substrate was

later used as the basis to fabricate self-aligned electrodes [21] and in combination with a dry-transfer process [22], single-walled carbon nanotube (SWCNT) field-effect transistors (FETs) were assembled (see Figure 1.a). This is also the reason for the presence of the protruding mesa-structure. The same approach also allows for the fabrication of strainable SWCNT-FETs (see Figure 1.b) [11].

In particular, the assembly of multiple CNTFETs from a single SWNT is of interest for the investigation of fundamental properties. Similarly, the fabrication of multi-FETs with varying gate-CNT distances enables the study of the CNT-gate coupling effect on resonant or gas sensing behaviour. Tapered profiles allow for the patterning of a common electrode for all FETs (see Figure 2).

Fig. 2. Very small (~250 nm) as well as very large (~1 mm) structures, and also tapered profiles are preferentially etched simultaneously. In terms of depth, structures ranging from 200 nm to 25 µm were patterned.

2. Materials and methods

Multi-FET devices (Figure 1,3) were fabricated on a (100) Si wafer coated with a silicon nitride layer. For the strainable devices (Figure 2) the silicon nitride was deposited on a silicon-on-insulator wafer (SOI, 5 µm device layer, 1 µm oxide, 300 µm handle layer). The 550 nm low stress silicon nitride layer was grown by plasma enhanced chemical vapor deposition (PECVD). To pattern this layer, AR-N 7520.17, which is a Novolac based resist. It acts negative both as an e-beam as well as a UV resist, was spun onto 2x2 cm chips. Resist spinning at 4k rpm resulted in a film of 430 nm thickness, while spinning at 2k rpm produced a 650 nm thick film. The samples were then baked at 85°C for 1 minute. The

resist was first exposed by UV (MA6, g and i-line), this was directly followed by an exposure by e-beam (EBPG5200). Development was performed using AR 300-47 (8:1 diluted) followed by a short rinse in DI-H₂O. The UV exposure dose was varied between 5.2 and 39 mJ/cm² and the structures were investigated by profilometer line scans and scanning electron microscopy (SEM) (see Figure 3). The resist is only sensitive to the 365 nm wavelength. The minimum feature size for the e-beam structures was 250 nm, all features larger and requiring an overlay accuracy of less than 500 nm were exposed by UV-lithography. For a complete process overview for all the structures shown here, please refer to the supporting information.

Fig. 3. Full exposure was observed at ~ 25 mJ/cm². For resist spinning at 2000, as well as 4000 rpm, full exposure was observed at this dose. For this work, if the UVL was performed directly after spin-coating, all exposure times resulted in positively tapered profiles.

To transfer the resist pattern into the nitride and the underlying silicon, layer inductively coupled plasma deep reactive ion etching (ICP-DRIE, Oxford PlasmaPro 100 Estrelas) was used (see Figure 4). In comparison to conventional RIE, DRIE is able to produce much higher aspect ratio structures and offers a better selectivity of silicon over photoresist etch rate, which is crucial for high aspect ratio features.

The devices with the actuator structures were mainly used to investigate the necessary alignment accuracy and the ability to etch high aspect ratio trenches. Whereas the multi-FET devices were used to test the ability to etch trenches with different depths simultaneously and to transfer tapered profiles into the silicon nitride.

Fig. 4. A close coupled mass flow controller (MFC) ICP-DRIE machine was used to perform a Bosch™ process, which consisted of alternating etching and passivation cycles. In addition, an oxygen pulse was included after the breakthrough step for optional etch rate tailoring.

Fig. 5. SEM images of the alignment accuracies. An overlap of exposure areas of ~ 0.5 μm proved to be sufficient to fabricate movable electrodes with a gap of 250 nm.

3. Results and Discussion

As can be seen in Figure 6, feature sizes spanning multiple orders of magnitude, were successfully co-integrated by allowing for an alignment accuracy of 500 nm. The investigation of the aspect ratio dependent etching (ARDE) lag showed that effect becomes noticeable in trenches below 1 μm (see Figure 6). For the etched structures (Figure 5, right) no notching was noticeable even after strong overetching. This demonstrates the ability of even very short low frequency pulses (LF, 990 Hz pulse frequency, 350 kHz generator frequency) to depolarize the substrate. If overetching can be tolerated this further expands the variety of structures, which can be etched simultaneously.

Fig. 6. For the etching of silicon by LF based DRIE, only for trenches below 1 μm ARDE lag became apparent. For 250 nm trenches the etch rate is reduced to 75%.

Fig. 7. In order to fabricate tapered profiles, the UV exposure was performed before the e-beam exposure. Hereby an overexposure at 39 mJ/cm^2 was employed. The ICP-RIE etch resulted in a taper of 40° in the nitride layer.

As shown previously (see Figure 3), the UV exposure of the resist resulted in an exposure dose independent taper of the resist sidewalls. This is most likely a result of the presence of an edge bead, since the chip size was fairly small – 2 by 2 cm, and scattering at the glass/air, air/resist interface may have occurred. This effect was observed to be strongly time dependent, which is consistent with the decrease of sensitivity of the resist over time. As a result, tapered UV exposures should be performed directly after the resist softbake. When using the standard recipe, without any oxygen present, this resulted in a taper angle of 40° in the silicon nitride

layer. Whereas this is convenient for the structures at hand here, as it allows for the patterning of continuous electrodes over the profile, a different method needs to be employed in order to vary the taper. This is the reason for the introduction of an oxygen pulse (see Figure 4) after the break-through step and the investigation of the influence of both LF and high frequency (HF, 13.56 MHz) biasing. Interestingly, when applying a HF bias, a close to linear decrease in the selectivity was observed, whereas a LF bias resulted in a close to linear increase of the selectivity.

Fig. 8. The dependence of the photoresist (PR) and silicon etch rate (ER) on the oxygen flow were tested in a Bosch process (top and bottom left graph) and a continuous etching mode (bottom right). It displayed that the photoresist etch rate linearly scales with the oxygen flow, whereas the silicon nitride etch rate changed relatively little. The selectivity of the nitride etch rate over the photoresist etch rate was directly proportional for LF based etching and inversely proportional for HF etching. This means shallower (LF) or steeper (HF) profiles result from an increased oxygen flow during the process. For all etch rate numbers and selectivities, please refer to the supporting information

The HF bias is typically correlated with a chemical etching component rather than sputtering, as it tends to accelerate the heavier ions less strongly towards the substrate than LF based processes [23]. In addition, a higher oxygen content resulted in a heightened bias voltage at a given power. The gradual shift of LF based etching towards higher selectivities is therefore explained by the increasing kinetic energy of SF₆ ion derivatives impacting with the resist, which results in more pronounced resist hardening at higher biases. For HF based continuous etching, an increase of the oxygen flow by 15 sccm resulted in angle change of 5°. The oxygen flow can be further increased as the observed selectivity was still significantly higher than one and no increase in the non-homogeneity of the etched surface or burning of the resist was observed. For LF based etching a factor 1.5 higher selectivity (43:1) of Si/PR was observed in comparison to HF based etching (28:1). In order to be able to pattern high aspect ratio features, it is favourable to employ a high selectivity process. As

a result also processes combining first a LF (575 ms), followed by a HF bias step (350 ms) were investigated. It could be shown that depending on the oxygen concentration, both a SiN/PR selectivity increase or decrease can be obtained while still maintaining a 30% higher Si/PR etch rate ratio (36:1) in comparison to the HF process, and suppressing notching. While the previous two sections were concerned with the individual pattern transfer of in-plane and out-of-plane structures respectively, they can also be actively combined. As mentioned earlier in order to obtain consistent results, the UV exposures should precede the e-beam exposure. By exposing the areas, where later the gate electrodes were patterned (see Figure 9, UVL 1-2), by 16.9 and 20.8 mJ/cm² respectively an effective trench depth difference of 75 nm was obtained. If a tapered profile is not desired, then the UV exposure can also be performed at a fixed time after the softbake. This requires the re-evaluation of the exposure dose – resist height curve in order to predict the correct profile after etching.

Fig. 9. In order to simultaneously etch structures with different trench depths, multiple UV exposures are necessary. To integrate 2 trench levels in the silicon nitride, and also a mesa structure in the silicon, in total 3 UV exposures are necessary. The doses were as follows – UVL 1: 16.9 mJ/cm², UVL 2: 20.8 mJ/cm², UVL 3: 39 mJ/cm².

4. Conclusions

We demonstrated that it is possible to use a 2D approach to fabricate complex 3D substrates by combining a hybrid lithography approach with deep reactive ion etching. The combination of UV lithography and e-beam lithography allows for a process time reduction while still retaining high resolution in critical areas. In addition, underexposed and tapered resist profiles can be used to fabricate multi-level structures. Performing the breakthrough step with a low-frequency bias and introducing an oxygen pulse with a high-frequency pulse can be used to optimally tailor the etch rates, while maintaining a high silicon to photoresist selectivity and still preventing notching when terminating on oxide surfaces. Since the here used resist is a Novolac based resist, the presented findings should be applicable for similar resist systems, also when different photosensitizers or cross-linkers are employed.

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