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Analysis of Parameters Determining Nominal Dynamic Performance of 1.2 kV SiC Power MOSFETs

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Abstract—A good understanding of internal MOSFET capacitances is required in order to accurately model the dynamic characteristics of SiC MOSFETs. MOSFET compact models used to simulate and optimize power converter systems have to take into account the effects of non-linear voltage-dependent internal MOSFET capacitances correctly. In this paper, the individual influence of the voltage-dependent drain-source capacitance C_{ds} and the drain-gate capacitance C_{dg} on the MOSFET dynamics is investigated in detail. A comprehensive analysis of the switching performance of 1.2 kV SiC power MOSFETs with respect to C_{ds} and C_{dg} by means of a physics-based compact model, TCAD modeling, and the switching measurements of a 1.2 kV 80 mΩ SiC power MOSFET is presented. It is demonstrated that the non-linearity of C_{gd} impacts the turn-off delay time $t_{d,OFF}$, while the non-linearity of C_{ds} does not have a significant impact on the switching transients.

I. INTRODUCTION

Virtual prototyping based on electromagnetic circuit coupling can be used as a tool to provide a deep insight into the fast switching behavior of SiC power MOSFETs as shown in [1]. Development of accurate compact models suitable for virtual prototyping requires the knowledge of the MOSFET design and fabrication parameters and their impact on the fast switching capabilities. Nowadays, a great effort is being made in the direction of developing compact models for SiC MOSFETs, which are able to take into account temperature, non-linear behavior of capacitances [2]–[5] and voltage-dependent mobility [6]. However, the previous publications do not clarify which effects are dominant and to which extent each parameter influences the dynamic characteristics of SiC MOSFETs. This paper presents a comprehensive analysis of the switching performance of 1.2 kV SiC power MOSFETs with respect to different MOSFET design parameters by means of a physics-based compact model, TCAD modeling, and the switching measurements of a 1.2 kV 80 mΩ SiC power MOSFET. Identifying the dominant effects based on the semiconductor physics will allow the optimization of SiC MOSFET models for computationally extensive multi-physics simulations.

II. LITERATURE SURVEY

The MOSFET switching transients have been analyzed extensively in literature, observing the impact of the stray inductances seen from the drain, source and gate terminals [7], the threshold voltage, and the MOSFET transconductance [8]. However, the individual influence of the non-linear voltage-dependent drain-source capacitances C_{ds} and drain-gate capacitance C_{dg} is still unclear. In [9], a MOSFET analytical model assuming simplified piece-wise constant voltage-dependency of MOSFET internal capacitances was used to show the influence of parasitic effects on the MOSFET switching performance. However, such a simplified model does not include the non-linear voltage dependence of MOSFET capacitances, and hence, does not represent the effect of this non-linearity on the switching waveforms. Recent publications [4], [10]–[12] clearly demonstrate the importance of modeling the non-linear behavior of MOSFET capacitances, especially the drain-gate capacitance. In [4], [10], [11], behavioral MOSFET models were developed, and the corresponding analytical models describing C_{dg} and C_{ds} as the functions of the MOSFET terminal voltages were parametrized based on either S-parameter measurements of MOSFET capacitances or using the slow switching measured current and voltage waveforms. These modelling approaches do not provide any physical understanding of the MOSFET capacitances. On the other hand, in [12] a physics-based model of C_{dg} was developed based on the surface-potential approach. This model, however, does not address the modelling of the so called kink point in the non-linear C_{dg} - V_{ds} curve as described in [5] and also observed in the C_{dg} measurements of the modelled 1.2 kV 80 mΩ SiC power MOSFET. Therefore, in this paper we analyze the importance of modelling C_{dg} with two different decay rates for the increase of the drain voltage around a kink in the measured C_{dg} - V_{ds} curve. Additionally, this paper presents also an analysis of switching waveforms with respect to C_{ds} .

III. PROPOSED MODELLING APPROACH

As the numerical modeling of semiconductor physics in TCAD tools is computationally expensive, behavioral and/or physics-based compact models are typically used for the device and system analysis. In this paper, a physics-based compact model for vertical SiC MOSFETs is used for a parametric study on dynamic behavior of a 1.2 kV 80 mΩ SiC MOSFET (C2M0080120D) from Cree. This model accurately simulates the device characteristics by iteratively calculating the surface potential and considering important material and geometry effects. The physical background and consideration of mobility degradation effects due to interface traps and surface roughness distinguishes this model from other physics-based compact models of SiC power MOSFETs proposed in literature [6]. The model is established using the Spectre circuit simulator from Cadence. It allows evaluating and visualizing the switching waveforms with much less computational resources compared to TCAD mixed-mode simulations while still providing the link between semiconductor device physics and MOSFET dynamics. As a result, it enables an efficient evaluation of the impact of different MOSFET design parameters on both static and dynamic MOSFET behaviors. TCAD modeling is used to derive the physics-based models of MOSFET parameters, e.g. channel mobility as function of V_{gs} , $C_{ds}(V_{ds})$ and $C_{gd}(V_{gd}, V_{ds})$.

IV. DYNAMIC PERFORMANCE ANALYSIS

The unknown parameters of the compact model were extracted from the I-V and C-V measurements of a C2M0080120D sample as described in [13]. The developed compact model was validated by the double-pulse test (DPT) measurements using a C2M0080120D MOSFET as the low-side switch and a Cree C4D10120D SiC diode as the free-wheeling diode (see Fig. 1), while considering the parasitics of the measurement setup [1]. The verification of the compact model in the switching transient simulation is shown in Fig. 2. The difference between the measured and simulated switching energy losses calculated from $I_S(t)$ and $V_{DS}(t)$ is $\approx 5\%$, which indicates that the model can be used to predict accurately the switching losses. In comparison to the behavioral compact model for C2M0080120D MOSFET provided by the device manufacturer, the developed compact model provides a physical insight into the dynamic MOSFET characteristics, however, by its nature it is more sensitive to convergence problems. As a result, the oscillations observed in the simulated $V_{DS}(t)$ at turn on (Fig. 2b) are more damped in the measurements, which will be further investigated in the course of future research.

In the next step, the analysis of switching waveforms is performed to identify the impact of MOSFET capacitances on its dynamic performance under nominal operation. TCAD modeling based on Synopsys Sentaurus is used to better understand the physics of the nonlinear voltage dependency of the capacitance.

Fig. 1. Simplified equivalent circuits of: a) the DPT measurement setup, and b) the implemented compact model of the 1.2 kV SiC MOSFET.

Fig. 2. Comparison between the measured and simulated switching waveforms: a) turn on ($t_{start,on} = 11.541 \mu s$), and b) turn off ($t_{start,off} = 0.841 \mu s$).

A. Effect of C_{gd}

Using the Sentaurus device simulator, a half pitch cell of the 1.2 kV Cree SiC MOSFET is designed with two different configurations having the same threshold voltage of $V_{th} = 3.0V$. The first MOSFET configuration (DUT0) is designed in TCAD with constant doping of the JFET and the drift region (10^{16} cm^{-3}) over a total epi-layer thickness of $L_{gd,max} = 10 \mu m$. In the second configuration (DUT1), the JFET doping was increased up to $3 \cdot 10^{16} \text{ cm}^{-3}$ in the top $0.6 \mu m$ of the drain region under the gate oxide, which resulted in a non-linear

C_{gd} - V_{ds} curve with a kink point around $V_{DS1} = 10$ V and the same voltage-dependency as DUT0 for $V_{ds} > 20$ V, see Fig. 3. In comparison to DUT0, the on-state performance of DUT1 is improved in terms of on-state resistance, i.e. $R_{ds,on,DUT1} \approx 0.71 \cdot R_{ds,on,DUT0}$, determined at $V_{ds} = 20$ V and $I_d = 20$ A as shown in Fig. 4. A higher C_{gd} of DUT1 is due to the larger doping concentration, whereas the decay of C_{gd} around the kick-point $V_{ds} = 10$ V can be explained by a combination of two effects: an extension of the depletion in the JFET region in the vertical direction from the oxide surface with an increase of V_{gd} , and an extension of the depletion in lateral direction from the base-drain p-n junction with an increase of V_{ds} leading to the pinch-off of the JFET region, see also Fig. 1b.

Fig. 3. C_{gd} characteristics of the two MOSFET designs DUT0 and DUT1 at 1 MHz.

Fig. 4. Transfer characteristics of the two MOSFET designs DUT0 and DUT1 at 300 K. DUT1 has a smaller on-state resistance than DUT0 while having the same threshold voltage $V_{th} = 3.0$ V.

A TCAD simulation was used to extract the non-linear C_{gd} as a function of both the gate-source, V_{GS} , and drain-source, V_{DS} , voltages. A TCAD small-signal simulation of $C_{gd,DUT1}$ at 1 MHz during the switch off transient is shown

in Fig. 6 together with the $C_{gd,DUT1}(V_{DS}, V_{GS})$ under a quasi-stationary variation of V_{DS} for different gate-source voltages $V_{GS} = 0 - 20$ V. For $V_{GS} < V_{th}$, the C_{GD} dependence on V_{GS} mostly leads to a parallel shift of $C_{gd}(V_{DS})$ in comparison to $C_{gd}(V_{DS})$ at $V_{GS} = 0$ V. For $V_{GS} > V_{th}$, increasing V_{GS} leads to a smaller channel resistance, and lower C_{gd} magnitude. Additionally, the voltage drop across the drain resistance (R_{JFET}) increases with the drain current $I_D(V_{GS})$, which leads to a $C_{gd}(V_{DS})$ dependency different than $C_{gd}(V_{DS})$ at $V_{GS} = 0$ V. Analyzing the dynamic response of two designs DUT0 and DUT1, we observed that the non-linear C_{gd} of DUT1 influences only the turn-off transient introducing a time delay, Δt_{shift} , of the current and voltage waveforms as shown in Fig. 5. This impact increases if the kick-point V_{DS1} is at higher V_{DS} . Accordingly, the non-linearity of C_{gd} does not affect the turn-on transient significantly, and introduces a time-delay of current and voltage curves at turn-off.

Fig. 5. Comparison between turn off switching waveforms for the two MOSFET designs, DUT0 and DUT1.

B. Effect of C_{ds}

The effect of the non-linear drain-source capacitance C_{ds} is investigated for three different C_{ds} models: a p-n junction capacitance model fitted to match the measured $C_{ds}(V_{DS})$, a $C_{ds}(V_{DS,approx1})$ model approximated with values $C_{ds,high}$ and $C_{ds,low}$ at low and high V_{DS} voltages respectively, and for $C_{ds}(V_{DS,approx2}) = \text{const.}$, equal to the measured C_{ds} at high V_{DS} voltages, as shown in Fig. 7.

The simulations of the turn-on and turn-off transients, including the parasitics of measurement setup and the device packages, are shown in Fig. 8a) and b) for three different C_{DS} models. The comparison of the I_S and V_{DS} curves in Fig. 8a) and b) points out that an assumption of $C_{DS} = \text{const.}$ can be used to model the MOSFET dynamic performance with an acceptable accuracy. Similarly, the constant value of $C_{GS} = \text{const.}$ can be adopted to accurately reproduce the switching transients.

Fig. 6. TCAD small-signal simulation of $C_{gd,DUT1}$ at 1 MHz during switch off (black curve, V_{GS} changing from 20 V to -5 V), and for the quasi-stationary dc variation of V_{DS} for different $V_{GS} = 0 - 20$ V.

Fig. 7. Three models of C_{ds} : $C_{ds}(V_{DS})$ dependency.

V. CONCLUSION

This paper presents a detailed analysis of dynamic performance of a 1.2 kV SiC MOSFET with respect to non-linear drain-source C_{ds} and gate-drain C_{gd} semiconductor capacitances. It is demonstrated that the non-linearity of C_{gd} impacts the turn-off delay time $t_{d,OFF}$, while the non-linearity of C_{ds} does not have a significant impact on the switching transients. These results can help to develop a simplified MOSFET model, which can be used for electromagnetic-circuit coupled, i.e. multiphysics, simulations.

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Fig. 8. Three models of C_{ds} : a) turn-on and b) turn-off switching transients.

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