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Journal Article

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Publication date:

2018-12

Permanent link:

<https://doi.org/10.3929/ethz-b-000461392>

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Originally published in:

IEEE Transactions on Circuits and Systems I: Regular Papers 68(12), <https://doi.org/10.1109/TCSI.2018.2875741>

Efficient Soft-Output Gauss-Seidel Data Detector for Massive MIMO Systems

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Abstract—For massive multiple-input multiple-output (MIMO) systems, linear minimum mean-square error (MMSE) detection has been shown to achieve near-optimal performance but suffers from excessively high complexity due to the large-scale matrix inversion. Being matrix inversion free, detection algorithms based on the *Gauss-Seidel* (GS) method have been proved more efficient than conventional *Neumann* series expansion (NSE) based ones. In this paper, an efficient GS-based soft-output data detector for massive MIMO and a corresponding VLSI architecture are proposed. To accelerate the convergence of the GS method, a new initial solution is proposed. Several optimizations on the VLSI architecture level are proposed to further reduce the processing latency and area. Our reference implementation results on a Xilinx Virtex-7 XC7VX690T FPGA for a 128 base-station antenna and 8 user massive MIMO system show that our GS-based data detector achieves a throughput of 732 Mb/s with close-to-MMSE error-rate performance. Our implementation results demonstrate that the proposed solution has advantages over existing designs in terms of complexity and efficiency, especially under challenging propagation conditions.

Index Terms—Massive MIMO, minimum-mean square error (MMSE), *Gauss-Seidel* method, soft-output data detection, VLSI.

I. INTRODUCTION

THE transmission of multiple data streams concurrently and in the same frequency band, which is known as multiple-input multiple-output (MIMO) technology, enables higher data rates compared to traditional single-input single-output (SISO) wireless communication systems [2]. Due to the combined effect of the ever-growing mobile data traffic and the scarcity of favorable radio spectrum in the low-loss frequency range, massive MIMO is widely believed to be a core technology for upcoming fifth generation (5G) wireless communication systems [3]. Massive MIMO promises higher data rates, improved spectral efficiency, better link reliability, and coverage over small-scale MIMO systems [4–9]. Compared to SISO systems, multiple interfering messages/symbols are transmitted concurrently in MIMO systems and expected to be separated at the receiver side with the contamination of noise or interference [10]. In the case of massive MIMO, however, this data detection operation entails excessively high computational

complexity with optimal methods as the number of base-station and user antennas increases significantly.

A. Detection in Massive MIMO Systems

The optimal data detection problem in MIMO systems is non-deterministic polynomial-time hard (NP-hard) [11–13]. Hence, existing algorithms that aim at solving this problem optimally, e.g., algorithms based on the optimal maximum-likelihood (ML) criterion [14] or the maximum *a posteriori* (MAP) criterion [15], inevitably require excessively high complexity as the number of decision variables increases with the number of transmitted data streams. Though the hardware computing capability has evolved significantly over recent decades, efficient hardware implementations for optimal data detection remains challenging. On the other hand, the new emerged application scenarios such as massive machine type communications (mMTC) and ultra-reliable low latency communications (URLLC) are expecting massive MIMO detectors of low complexity, latency, and area, which implies that even data detectors that have modest-complexity would be unacceptable due to the stringent power and area constraints [10]. Therefore, near-optimal, low-complexity, and high-speed massive MIMO detectors are highly desired to bridge the gap between algorithms and hardware implementations.

One possible solution to perform optimal data detection are non-linear data detection algorithms with reduced complexity, such as the sphere decoder (SD) [16–18] and tabu search (TS)-based data detectors [19, 20]. Admittedly, such solvers worked perfectly well for traditional, small-scale MIMO systems. However, for massive MIMO systems with tens to hundreds of antennas and higher-order modulation schemes [21, 22], such methods result in prohibitively high computation and implementation complexity [12].

Alternatively, one can resort to linear data detection algorithms, such as zero-forcing (ZF) or minimum mean-square error (MMSE)-based equalization, to tradeoff performance versus complexity [3]. Unfortunately, both of these methods require a large-dimensional matrix inversion. Exact inversion algorithms of an $N \times N$ matrix, using, for example, QR-*Gram* Schmidt [23], *Gauss-Jordan* [24], or *Cholesky* decomposition [25], entail high complexity of $\mathcal{O}(N^3)$. By exploiting the channel hardening property of wireless channels in massive MIMO systems, reference [26] proposed a *Neumann* series expansion (NSE) that reduces the complexity of matrix inversion. However, this algorithm still suffers from a complexity of $\mathcal{O}(N^3)$ when the NSE length $K \geq 2$ (even higher than the exact inverse

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This paper was presented in part at IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada, 2016 [1]. Chuan Zhang and Zhizhen Wu have the same contribution to this work. (*Corresponding author: Chuan Zhang.*)

when $K \geq 4$) [26]. To achieve a lower complexity of $\mathcal{O}(N^2)$, a soft-output detection based on *Gauss-Seidel* (GS) method was proposed in [27] recently. But the existing GS-based detectors still exhibit slow convergence rates and relatively high hardware efficiency.

B. Contributions

In this paper, an efficient GS-based soft-output data detection algorithm and a corresponding VLSI architecture are proposed. Based on the fact that the MMSE filtering matrix is diagonally dominant for massive MIMO systems, a 2-term NSE is employed to generate the initial solution of the GS method, which effectively accelerates the convergence, especially under challenging propagation environments, such as MIMO systems with a large system loading factor or correlated channels. We provide a VLSI architecture along with numerous architecture- and hardware-level optimizations. Our implementation results demonstrate that the proposed detector achieves a throughput of 732 Mb/s with close-to-MMSE error-rate performance, outperforming state-of-the-art designs in terms of complexity and efficiency. With the aid of the proposed efficient architecture, the GS-based detector is flexible and suitable to meet various system requirements.

C. Outline of the Paper

The reminder of the paper is organized as follows. Section II reviews the prerequisites. Section III proposes the GS-based soft-output data detection algorithm for massive MIMO systems and provides a complexity analysis and error-rate performance comparison. Section IV details the VLSI architecture with several optimizations. Section V provides reference FPGA implementation results and a comparison with existing designs. Section VI concludes the paper.

D. Notation

Lower- and upper-case boldface letters stand for column vectors and matrices, respectively. The entry in the i th row and j th column of a matrix $\mathbf{A}$ is represented by A_{ij} ; the k th entry of a vector $\mathbf{a}$ is represented by a_k . The operations $(\cdot)^H$, $(\cdot)^T$, $(\cdot)^{-1}$ denote conjugate transpose, transpose and inverse respectively; $|\cdot|$ and $\|\cdot\|$ denote the absolute value operator and the Euclidean norm respectively. $\mathbb{E}\{\cdot\}$ stands for expectation. $\mathbf{I}_K$ denotes the $K \times K$ identity matrix. The superscript $(\cdot)^{(k)}$ indicates the k th iteration of iterative methods.

II. PREREQUISITES

A. System Model

We consider a multi-user MIMO uplink system with N_t users and N_r receive antennas at the base station (BS). In the case of massive MIMO, we assume that $N_r \gg N_t$. Spatial multiplexing is employed and each user is equipped with a single antenna¹. For each user, the information bits $\mathbf{b}$ are encoded into the coded bit-stream $\mathbf{x}$ and then mapped to the transmit vector $\mathbf{s} = [s_1, \dots, s_{N_t}] \in \Omega^{N_t}$, where Ω corresponds to the 2^B -QAM

constellation using Gray labelling. Therefore, each transmit vector is associated with $N_t B$ information bits and x_{ib} denotes the b th bit of the i th entry of $\mathbf{s}$. The transmit vector $\mathbf{s}$ is transmitted over a wireless MIMO channel modeled as

$$\mathbf{y} = \mathbf{H}\mathbf{s} + \mathbf{n}, \quad (1)$$

where $\mathbf{y} = [y_1, \dots, y_{N_r}]^T \in \mathbb{C}^{N_r}$ corresponds to the received vector at the BS, $\mathbf{H} \in \mathbb{C}^{N_r \times N_t}$ is the channel matrix, and $\mathbf{n} \in \mathbb{C}^{N_r}$ stands for independent identically distributed (i.i.d.) Gaussian noise with mean zero and variance N_0 per entry. In the following, the channel matrix $\mathbf{H}$ and the noise variance N_0 are assumed to be perfectly known at the receiver. The transmit symbol variance is normalized as $E_s = \mathbb{E}[|s_i|^2] = 1$. In what follows, we employ the average SNR per receive antenna defined as $\text{SNR} = N_t E_s / N_0$.

B. Soft-Output MMSE Data Detection

The task of the BS is to compute log-likelihood ratio (LLR) values for the coded bits given $\mathbf{H}$ and $\mathbf{y}$ with a soft-output data detection algorithm. Since MMSE algorithms have been proven to be near-optimal for massive MIMO uplink with low complexity [26], we consider the typical linear MMSE detection, which can be written as

$$\hat{\mathbf{s}} = \mathbf{W}^{-1} \mathbf{y}^{\text{MF}}, \quad (2)$$

where $\mathbf{y}^{\text{MF}} = \mathbf{H}^H \mathbf{y}$ is the matched-filter output and $\mathbf{W} = \mathbf{G} + N_0 \mathbf{I}_{N_t}$ is the regularized Gram matrix with the Gram matrix $\mathbf{G} = \mathbf{H}^H \mathbf{H}$. In order to obtain the LLR values, (2) can be rewritten as

$$\hat{\mathbf{s}} = \mathbf{U}\mathbf{s} + \mathbf{W}^{-1} \mathbf{H}^H \mathbf{n}, \quad (3)$$

where $\mathbf{U} = \mathbf{W}^{-1} \mathbf{G}$ is the equivalent channel matrix. Then the equalized symbol of the i th user can be written as $\hat{s}_i = \mu_i s_i + t_i$, where $\mu_i = \mathbf{U}_{ii}$ denotes the effective channel gain and t_i denotes noise-plus-interference (NPI). The *a posteriori* LLRs for each bit of $\mathbf{x}$ can be computed by

$$L_{ib} = \ln \left(\frac{\Pr[x_{ib} = 1 | \mathbf{y}]}{\Pr[x_{ib} = 0 | \mathbf{y}]} \right), \quad i = 1, \dots, N_t, b = 1, \dots, B. \quad (4)$$

Entailing only a small loss for high-order modulation schemes, the approximation of LLR computation proposed in [28] is hardware-friendly for Gray mappings. Therefore, an efficient approach to compute the extrinsic LLRs of the detector is given by

$$\hat{L}_{ib} = \rho_i \left(\min_{a \in \Omega_b^0} |z_i - a|^2 - \min_{a' \in \Omega_b^1} |z_i - a'|^2 \right) = \rho_i \lambda_b(z_i), \quad (5)$$

where $z_i = \hat{s}_i / \mu_i$ and $\rho_i = \mu_i^2 / \nu_i^2 = \mu_i / (1 - \mu_i)$ represents post-equalization signal-to-interference-and-noise-ratio (SINR), Ω_b^0 and Ω_b^1 denote subsets of Ω for which the b -th bit is 0 and 1, respectively. As summarized in [28], the function $\lambda_b(z_i)$ can be computed efficiently for Gray mappings. Note that the computation of the LLRs is the same for both real parts and imaginary parts.

¹The model can be extended to the case of multiple spatial streams per user.

III. LOW-COMPLEXITY SIGNAL DETECTION ALGORITHM

In this section, a low-complexity soft-output detection algorithm named improved GS detection (IGS) is proposed for massive MIMO uplink. Algorithm 1 provides a summary of the method.

A. Signal Detection with Gauss-Seidel Method

Computing the inverse of the regularized Gram matrix $\mathbf{W}^{-1}$ requires a computational complexity of $\mathcal{O}(N_t^3)$ using hardware-friendly matrix inverse approaches, which is prohibitive for massive MIMO. Therefore, iterative methods with low complexity have been exploited in massive MIMO detection. The GS method is used to solve the N -dimension linear equation $\mathbf{A}\mathbf{x} = \mathbf{b}$, where $\mathbf{A}$ is the $N \times N$ coefficient matrix, $\mathbf{x}$ is the solution vector, and $\mathbf{b}$ is the measurement vector. In what follows, the reason why the GS method can be utilized to solve massive MIMO detection problem is explained.

Lemma 1. *For massive MIMO systems, the columns of channel matrix $\mathbf{H}$ are asymptotically orthogonal, and the regularized Gram matrix $\mathbf{W}$ is Hermitian positive definite with probability one.*

Proof: Please refer to [3] and [29] for the proof. ■

Theorem 1. *The GS method converges for any initial solution if $\mathbf{A}$ is Hermitian positive definite.*

Proof: Refer to [30, Chapter 4] for a proof. ■

Specifically, signal detection in massive MIMO systems using the GS method is carried out by the following steps:

Step 1: Decompose the regularized Gram matrix $\mathbf{W}$ as

$$\mathbf{W} = \mathbf{D} + \mathbf{L} + \mathbf{L}^H, \quad (6)$$

where $\mathbf{D}$, $\mathbf{L}$, and $\mathbf{L}^H$ are the diagonal, strictly lower triangular, and strictly upper triangular components of $\mathbf{W}$, respectively.

Step 2: Compute initial solution $\mathbf{s}^{(0)}$ of the GS method. Usually, $\mathbf{s}^{(0)}$ is set as a zero vector if no *prior* information of the final solution is available.

Step 3: The transmitted signal vector $\mathbf{s}$ is then estimated iteratively as follows:

$$\mathbf{s}^{(k)} = (\mathbf{D} + \mathbf{L})^{-1}(\mathbf{y}^{\text{MF}} - \mathbf{L}^H \mathbf{s}^{(k-1)}), \quad k = 1, 2, \dots, K, \quad (7)$$

where K is the maximum number of iterations.

B. Fast-Converging Initial Solution

As discussed in Section III-A, since no *a priori* information of the final solution is available, the initial solution $\mathbf{s}^{(0)}$ in (7) is often set as an all-zero vector. Such a choice is simple but requires a large number of iterations. In general, the initial solution plays an important role for the convergence of the GS method and affects both complexity and accuracy when the number of iterations is finite (and small).

The exact solution of GS method is given in Eq. (2). Note that the inverse of the regularized Gram matrix $\mathbf{W}^{-1}$ here can also be computed by the following NSE:

$$\mathbf{W}^{-1} = \sum_{k=0}^{\infty} (\mathbf{I}_{N_t} - \mathbf{X}^{-1} \mathbf{W})^k \mathbf{X}^{-1}, \quad (8)$$

Algorithm 1 Improved GS detection for massive MIMO (IGS)

```

1: Input:  $\mathbf{y}$ ,  $\mathbf{H}$ ,  $N_0$  and  $K$ 
2: (Preprocessing)
3:  $\mathbf{W} = \mathbf{H}^H \mathbf{H} + N_0 \mathbf{I}_{N_t}$  and  $\mathbf{y}^{\text{MF}} = \mathbf{H}^H \mathbf{y}$ 
4:  $\mathbf{W} = \mathbf{D} + \mathbf{E}$  and  $\mathbf{E} = \mathbf{L} + \mathbf{L}^H$ 
5: (Initialization)
6:  $\mathbf{W}_2^{-1} = \mathbf{D}^{-1} - \mathbf{D}^{-1} \mathbf{E} \mathbf{D}^{-1}$ 
7:  $\mathbf{s}^{(0)} = \mathbf{W}_2^{-1} \mathbf{y}^{\text{MF}}$ 
8: (GS iteration)
9: for  $k = 1, 2, \dots, K$  do
10:    $\mathbf{s}^{(k)} = (\mathbf{D} + \mathbf{L})^{-1}(\mathbf{y}^{\text{MF}} - \mathbf{L}^H \mathbf{s}^{(k-1)})$ 
11: end for
12: (LLR computation)
13:  $\tilde{\mathbf{U}} = \mathbf{I}_{N_t} - N_0 \mathbf{W}_2^{-1}$ 
14: for  $i = 1, 2, \dots, N_t$  do
15:   for  $b = 1, 2, \dots, B$  do
16:      $\hat{L}_{ib} = \rho_i \lambda_b(z_i)$  (See Eq. (5) for details.)
17:   end for
18: end for
19: Output:  $\hat{L}_{ib}$ 

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where $\mathbf{X}^{-1}$ is an arbitrary matrix satisfying the condition

$$\lim_{k \rightarrow \infty} (\mathbf{I}_{N_t} - \mathbf{X}^{-1} \mathbf{W})^k = \mathbf{0}_{N_t}. \quad (9)$$

Letting $\mathbf{X} = \mathbf{D}$ for the sake of low complexity and keeping only the first 2 terms of NSE, we arrive at the following 2-term approximation of $\mathbf{W}^{-1}$ [31]

$$\mathbf{W}_2^{-1} = \mathbf{D}^{-1} - \mathbf{D}^{-1} \mathbf{E} \mathbf{D}^{-1}, \quad (10)$$

where $\mathbf{E}$ is the off diagonal part of $\mathbf{W}$. Exploiting such an efficient approximation, we have the new initial solution $\mathbf{s}^{(0)}$ as follows:

$$\mathbf{s}^{(0)} = \mathbf{W}_2^{-1} \mathbf{y}^{\text{MF}}. \quad (11)$$

Remark 1. *The NSE-based approximation is only efficient with the number of terms less than three, otherwise it will still suffer from high complexity.*

C. Efficient LLR Computation

Although the computational complexity of LLR computation has been reduced significantly in (5), it requires the inverse matrix $\mathbf{W}^{-1}$ to compute the effective channel gains μ_i . For the purpose of computing LLRs more efficiently, we propose an approximated method to obtain the effective channel gains with a negligible performance loss. Firstly, the equivalent channel matrix can be rewritten as

$$\mathbf{U} = \mathbf{W}^{-1} \mathbf{G} = \mathbf{I}_{N_t} - N_0 \mathbf{W}^{-1}. \quad (12)$$

Inspired by the proposed initial solution in Section III-B, we also exploit the 2-term NSE $\mathbf{W}_2^{-1}$ to approximate $\mathbf{W}^{-1}$ here:

$$\tilde{\mathbf{U}} = \mathbf{I}_{N_t} - N_0 \mathbf{W}_2^{-1}. \quad (13)$$

Therefore, the effective channel gain can be computed by

$$\tilde{\mu}_i = 1 - N_0 W'_{ii}, \quad (14)$$

where W'_{ii} denotes the i th diagonal entry of $\mathbf{W}_2^{-1}$. Then, the approximated LLRs can be efficiently computed by (5).

Fig. 1. BER Performance comparison for different methods with $N_r = 128$ and $N_t = 16$.

Fig. 2. BER Performance comparison for different methods with $N_r = 64$ and $N_t = 16$.

D. Computational Complexity Analysis

Since most of the linear MMSE algorithms of massive MIMO detection require to pre-compute the regularized Gram matrix $\mathbf{W}$ and the matched-filter output $\mathbf{y}^{\text{MF}}$, we focus mainly on the complexity of the other parts. Therefore, we have:

Lemma 2. *The computational complexity of the proposed IGS algorithm scales as $\mathcal{O}((K+2)N_t^2)$.*

Proof: In what follows, we estimate the computation complexity of reciprocal operations in term of complex-valued multiplications.

Computing $\mathbf{W}_2^{-1}$: As the multiplication of a $N_t \times N_t$ diagonal matrix and a $N_t \times N_t$ matrix requires N_t^2 complex-valued multiplications, the number of complex-valued multiplications for calculating $\mathbf{W}_2^{-1}$ is $(2N_t^2 - N_t)$ according to (10). Since $\mathbf{D}^{-1}\mathbf{E}\mathbf{D}^{-1}$ is Hermitian, only the lower-triangle component or the upper-triangle component needs to be computed. Hence, the total number of complex-valued multiplications is N_t^2 .

Computing $\mathbf{s}^{(0)}$: As the matched-filter output $\mathbf{y}^{\text{MF}}$ is a $N_t \times 1$ vector, it requires N_t^2 complex-valued multiplications to obtain the proposed initial solution $\mathbf{s}^{(0)}$ according to (11).

Solving (7): Considering $(\mathbf{D} + \mathbf{L})$ is a lower-triangular matrix, the computation of (7) after K iterations requires KN_t^2

Fig. 3. BER performance comparison for different initial solutions with $N_r = 64$ and $N_t = 8$.

Fig. 4. BER performance comparison for different correlation factors ζ_t with $N_r = 128$, $N_t = 16$ and $\zeta_r = 0.4$.

complex-valued multiplications. Note that since the proposed initial solution is relatively close to the exact solution in favourable propagation environments, K could be quite small.

Computing μ_i : Since $\mathbf{W}_2^{-1}$ has been computed, the required number of complex-valued multiplications of computing μ_i (for $i = 1, \dots, N_t$) is simply N_t according to (14).

To sum up, the overall required number of complex-valued multiplications of proposed IGS algorithm is $(K+2)N_t^2$. For massive MIMO detection, the computational complexity of IGS reduces to $\mathcal{O}((K+2)N_t^2)$. ■

E. Simulation Results

Numerical results of BER performance against SNR are shown in Figs. 2–4 to compare the proposed IGS algorithm with the *Cholesky* decomposition, the NSE-based method, and conventional GS-based algorithms. We consider massive MIMO systems with different parameters, where a standard rate-1/2 convolutional channel code and 64 quadrature amplitude modulation (QAM) scheme are employed. All the compared methods compute soft-outputs. At the receiver, LLRs are extracted from the detected signal for soft-input *Viterbi* decoding.

Fig. 5. High-level architecture of IGS detector.

Remark 2. We let the number of iterations of the NSE-based approach greater than that of IGS ($K_{\text{NSE}} = K_{\text{GS}} + 2$) in order to enable a fair comparison, since the 2-term NSE is employed to obtain the initial solution of IGS.

In Fig. 1 and 2, we compare the BER performance of IGS with the other conventional approaches under different antenna configurations. It is shown that IGS outperforms the NSE-based algorithm under both antenna configurations of 64×16 and 128×16 . According to Fig. 1, IGS with $K = 1$ achieves similar performance as the NSE-based algorithm with $K = 4$. Noting that with the greater system loading factor N_t/N_r (shown in Fig. 2), the NSE-based algorithm converges much slower than IGS. Therefore, the proposed IGS algorithm has advantage of convergence rate over the NSE-based one.

In Fig. 3, we compare the performance of the GS-based algorithms with different initial solutions. Compared to existing choices, the proposed initial solution successfully accelerates the convergence. It is shown that the GS method with the proposed initial solution for $K = 1$ almost achieves the same performance of that with the zero-vector initial for $K = 2$. Moreover, IGS also outperforms the one with initial solution $\mathbf{s}^{(0)} = \mathbf{D}^{-1}\mathbf{y}^{\text{MF}}$ proposed in [27] in terms of error-rate performance for given K .

In Fig. 4, we study the BER performance of IGS and other conventional approaches considering the spatial correlation of realistic MIMO systems. Here we adopt the *Kronecker* model proposed in [32], where ζ_r and ζ_t ($0 \leq \zeta \leq 1$) denote the correlated factor at the BS and the user sides respectively. We can see that all these approaches degrade to various extents as the channel correlation becomes serious. For both $\zeta_t = 0.2$ and $\zeta_t = 0.5$, the conventional NSE-based algorithm is hardly able to converge. However, IGS still converges with relatively small number of iterations.

IV. VLSI ARCHITECTURE

In this section, we describe a low-complexity VLSI architecture for the proposed IGS algorithm and provide several solutions to reduce hardware overhead and processing latency.

Fig. 6. Array structure of matched filter (e.g., $N_t = 3$). Fig. 7. Array structure of regularized Gram matrix computation unit (e.g., $N_t = 3$).

A. Architecture Overview

The VLSI architecture is depicted in Fig. 5. The proposed architecture consists of five units: 1) preprocessing unit (PU), 2) initial solution computation unit (ISCU), 3) GS method unit (GSMU), 4) SINR computation unit (SCU), and 5) LLR computation unit (LCU). Fed by $\mathbf{y}$, $\mathbf{H}^H$ and N_0 , PU performs matched filtering $\mathbf{y}^{\text{MF}} = \mathbf{H}^H \mathbf{y}$ and computes the regularized Gram matrix $\mathbf{W}$. Note that both operations can be performed by systolic arrays to achieve high-throughput. The outputs of PU are then passed to ISCU for computing the 2-term NSE

Fig. 8. Distribution of the value in regularized Gram matrix $\mathbf{W}$ with $N_r = 128$ and $N_t = 8$.

$\mathbf{W}_2^{-1}$ and the initial solution of GS method $\mathbf{s}^{(0)}$. While GSMU is iteratively computing $\hat{\mathbf{s}}$, SCU is computing the equivalent channel gain μ_i and the post-equalization SINR ρ_i . Finally, LCU performs the computation of LLRs according to Eq. (5).

B. Preprocessing Unit (PU)

The preprocessing unit is employed to compute the matched filter output $\mathbf{y}^{\text{MF}}$ and the regularized Gram matrix $\mathbf{W}$, which will be further passed to other units. Note that this unit is able to perform the operations above in parallel, since there is no data dependence between them.

1) *Matched Filtering*: The matched filter (MF) consists of a linear array of N_t PEs and performs the operation of $\mathbf{y}^{\text{MF}} = \mathbf{H}^H \mathbf{y}$. Fig. 6 shows the systolic array structure of MF. In each clock cycle, MF reads a new entry of $\mathbf{y}$ and the corresponding entries of $\mathbf{H}^H$, and the multiply-accumulate (MAC) operation is performed in each PE.

Remark 3. The total processing latency of MF is $(N_t + N_r - 1)$, and it utilizes N_t complex-valued multipliers.

2) *Regularized Gram Matrix Computation*: In massive MIMO systems, the dimension of the Gram matrix $\mathbf{G}$ tends to be very large. Therefore, the conventional systolic array for matrix-matrix multiplication which consists of $N_t \times N_t$ PEs is not scalable for large N_t . As discussed in Section III-A, the Gram matrix in massive MIMO uplink is Hermitian positive

Fig. 9. Architecture for proposed hardware-efficient quantizer.

Fig. 10. Architecture for data decompression.

definite. Hence, either upper triangular part or lower triangular of $\mathbf{G}$ is required to be calculated. Fig. 7 depicts the systolic array structure for computing the regularized Gram matrix (RGM). In this array, only $N_t(N_t + 1)/2$ PEs are employed to compute the lower triangular part of the Gram matrix $\mathbf{G}$. Each PE in the array contains a MAC unit. There are two types of PEs in the array, denoted by PE-A and PE-B, respectively. The transposed channel matrix $\mathbf{H}^H$ is shifted one column at a time into the systolic array. PE-As have the same structure as PEs of MF. Once an input value reaches a PE-B, the value is conjugated and passed to the lower part of the systolic array. Then, PE-Bs add the noise variance N_0 to the diagonal entries of $\mathbf{G}$. Finally, the lower triangular part of the regularized Gram matrix $\mathbf{L}$, the upper triangular part $\mathbf{L}^H$ and the diagonal part $\mathbf{D}$ are stored in the register files.

Remark 4. Total processing latency of RGM is $(2N_t + N_r - 1)$, and it uses $N_t(N_t - 1)/2$ complex-valued multipliers and N_t real-valued multipliers since the diagonal entries of $\mathbf{W}$ are real-valued.

3) *Data Compression Scheme*: Note that the regularized Gram matrix $\mathbf{W}$ is diagonally dominant in the case of massive MIMO with i.i.d. assumption, meaning that the diagonal entries of $\mathbf{W}$ are much greater than the off-diagonal ones. Hence, conventional uniform quantization schemes that cover the entire dynamic range of entries of $\mathbf{W}$ will cost a mass of hardware resources. Fig. 8 shows the distribution of entries of $\mathbf{W}$ in form of histogram. Obviously, values of $\mathbf{W}$ can be separated into two groups, one is around zero and the other is around N_t . By exploiting this property, the hardware overhead for storing and processing $\mathbf{W}$ can be saved significantly. The hardware-efficient quantization scheme with data compression for $\mathbf{W}$ can be denoted as follows (see Fig. 9 for architecture details)

Step 1: Compare W_{mn} with $N_t/2$. If the former is bigger

Fig. 11. Data flow graph of initial solution computation.

(a) Basic architecture for 2-term NSE.

(b) Proposed architecture for 2-term NSE with low latency.

Fig. 12. Two architectures for 2-term NSE computation.

than the latter, set the first bit of the fixed-point output (offset flag) as 1, otherwise set it as 0.

Step 2: If $W_{mn} > N_t/2$, subtract W_{mn} with N_t and then obtain the remaining bits of fixed-point output.

The compressed bits of W_{mn} will be sent to other units in detector, e.g. ISCU and GSMU. Before these units start to compute, the corresponding operation of data decompression is required. As shown in Fig. 10, the procedure of data decompression is simple and straightforward.

C. Initial Solution Computation Unit (ISCU)

As shown in Fig. 11, ISCU first performs the approximate matrix inversion $\mathbf{W}_2^{-1}$ and then computes the initial solution $\mathbf{s}^{(0)}$ of GS method. Since the computation of $\mathbf{s}^{(0)}$ is a typical matrix-vector multiplication, which can be performed by an array of MACs similar to MF, we focus mainly on the architecture design of the 2-term NSE approximation $\mathbf{D}^{-1} - \mathbf{D}^{-1}\mathbf{E}\mathbf{D}^{-1}$. A straightforward method to obtain $\mathbf{W}_2^{-1}$ is shown in Fig. 12(a), where d_i is the i th diagonal entry of $\mathbf{D}$, $\mathbf{e}_i^H$ and $\mathbf{w}_i^H$ denote the i th row of $\mathbf{E}$ and $\mathbf{W}_2^{-1}$, respectively. To compute $\mathbf{D}^{-1}$, a reciprocal module based on look-up table (LUT), which is suitable for FPGA implementation, is employed. The diagonal matrix $\mathbf{D}^{-1}$ is stored as a vector $\mathbf{d}^{-1}$ for the sake of saving storage space. The function of mul-A is to multiply a vector by a scalar.

Remark 5. For the architecture in Fig. 12(a), either one row or column is computed in mul-A per clock cycle, therefore four buffers are used to obtain a row of $\mathbf{W}_2^{-1}$ per clock cycle.

The major drawback of the architecture in Fig. 12(a) is the high processing latency. Considering the regularized Gram matrix $\mathbf{W}$ of order N_t , an undesirable latency of $2N_t$ clock cycles are required to obtain $\mathbf{w}_i^H$. Since $\mathbf{W} = \mathbf{D} + \mathbf{E}$ and $\mathbf{W}$ is Hermitian, the off-diagonal matrix $\mathbf{E}$ is therefore Hermitian.

(a) Basic architecture of GS iteration.

(b) Hardware-efficient architecture of GS iteration.

Fig. 13. Two architectures for GS iterative method.

Then, a low-latency version of this architecture is provided in Fig. 12(b). Instead of computing the reciprocal of d_i per clock, the proposed structure in Fig. 12(b) computes all entries of $\mathbf{D}$ during one clock cycle. Note that the mul-B is employed here to perform element-wise multiplication of $\mathbf{m}_i^H$ and $\mathbf{d}^{-1}$.

Remark 6. By exploiting the Hermitian characteristic, the proposed structure in Fig. 12(b) is able to obtain $\mathbf{W}$ in N_t clock cycles, and extra buffers are no longer needed.

After obtaining the 2-term NSE $\mathbf{W}_2^{-1}$, the initial solution of the GS method is computed according to Eq. 11, which can be performed by the systolic array in Fig. 6. It requires $(2N_t - 1)$ clock cycles to perform this operation.

D. GS Method Unit (GSMU)

Fig. 13(a) shows the basic architecture of GS method unit, where $\mathbf{M} = -\mathbf{L}^H$ and $\mathbf{N} = (\mathbf{D} + \mathbf{L})^{-1}$. Since $(\mathbf{D} + \mathbf{L})$ is a lower triangular matrix, a specific systolic array that performs forward substitution (FS) [33] is employed here to compute $\mathbf{N}'$. According to Eq. (7), each iteration of GS method can be divided into three phases. In the first phase, a systolic array for matrix-vector multiplication (denoted as mul-C) is employed to perform $-\mathbf{L}^H \mathbf{s}^{(k-1)}$. In the second phase, the operation $\mathbf{b} = \mathbf{y}^{\text{MF}} - \mathbf{L}^H \mathbf{s}^{(k-1)}$ is performed by N_t complex-valued adders. In the third phase, another systolic array denoted as mul-D is used to compute the matrix-vector multiplication of $\mathbf{N}'$ and $\mathbf{b}$. These phases can be repeated for a configurable number of iteration until the error rate performance meets the requirement. Since $\mathbf{s}$ is updated from the previous iteration, only a few registers are required to store the latest $\mathbf{s}^{(k-1)}$.

Remark 7. Both mul-C and mul-D in Fig. 13 consist of N_t MACs.

1) Hardware-Efficient Architecture: Fig. 13(b) depicts the proposed hardware-efficient architecture of GS method, derived

Fig. 14. Timing schedule of mul-C.

Fig. 15. Timing schedule of mul-D.

from the basic architecture in Fig. 13(a). In order to reduce the dynamic range of the values in GS method unit, we firstly normalize the input $\mathbf{y}^{\text{MF}}$ and $\mathbf{N}$ into $\mathbf{y}' = \mathbf{N}_r^{-1} \mathbf{y}^{\text{MF}}$ and $\mathbf{N}' = \mathbf{N}_r \mathbf{N}$. Such a trick is commonly used in fixed-point arithmetic. Therefore, $\mathbf{M}\mathbf{s}^{(k-1)}$ is scaled by $1/\mathbf{N}_r$ correspondingly, ensuring that the final result is equivalent. Note that $\mathbf{N}_r$ is usually a power of 2, therefore these scaling operations can be performed easily by shifting. After scaling, word-length of the data in GSMU can be significantly shortened and therefore the hardware overhead is reduced. Since the inputs $\mathbf{L}$, $\mathbf{D}$ and $\mathbf{L}^H$ are compressed according to Section IV-B3, they should be converted into conventional fixed-point numbers before computing. Also, the proposed architecture is irrelevant of the number of iterations, and therefore suitable for various applications.

2) *Timing Schedule for Lower Latency*: Usually, for a systolic array which performs matrix-vector multiplication of dimension N_t , it requires $(2N_t - 1)$ clock cycles to obtain the result (see the left parts of Fig. 14 and Fig. 15). It is worth noting that the GS iteration could have certain disadvantages because the variables that depend on each other can only be updated sequentially. Thus, it is important to reduce the overall latency of GS iterations so as to meet the throughput requirement. To this end, we propose a fast-converging initial solution in Section III-B, which is able to significantly reduce the number of iterations. Here, we introduce an efficient timing schedule scheme to further reduce the latency within each GS iteration.

As shown in Fig. 14, since $\mathbf{M} = -\mathbf{L}^H$ is an upper-triangular matrix, we reverse the input sequence of $\mathbf{d}$ and each row of $\mathbf{M}$. As a result, the total latency of mul-C is reduced from $(2N_t - 1)$ clock cycles to only N_t clock cycles. Likewise, since $\mathbf{N}' = \mathbf{N}_r(\mathbf{D} + \mathbf{L})^{-1}$ is a lower-triangular matrix, we simply

Fig. 16. Timing diagram for parallel implementation of IGS detector.

reverse the input sequence of $\mathbf{N}'$ (see Fig. 15) and therefore reduce the total latency of mul-D into N_t clock cycles.

Remark 8. By exploiting the rescheduling schemes in Fig. 14 and 15, latency of each GS iteration can be significantly reduced to half its original time.

E. SCU and LCU

The design of SCU is simple and efficient. According to Section III-C, the equivalent channel matrix $\mathbf{U}$ can be easily approximated by adders and scalar multipliers. Then the SINR computation is simply carried out by multipliers and reciprocal modules as described in Section II-B. Given the effective channel gains μ_i and the post-equalization SINR values ρ_i , the computation of the max-log LLRs can be simplified with Gray mappings according to Section II-B. Hence, the LCU focuses mainly on evaluating the linear function $\lambda_b(z_i)$. The readers can refer to [34] for more details of LCU architectures.

F. Timing Schedule of IGS Detector

As discussed before, because the GS method is inherently sequential, it is difficult to be performed in parallel. However, the proposed IGS detector consists of several units and some of them exist no data dependency. Therefore, some operations can be performed concurrently. After careful analysis and arrangement, the overall timing schedule of IGS detector is shown in Fig. 16.

V. IMPLEMENTATION RESULTS

In this section, the proposed IGS detector has been implemented with Xilinx Virtex-7 XC7VX690T FPGA. The corresponding fixed-point parameters, FPGA implementation results, and comparison to other designs are provided here.

A. Fixed-Point Error-Rate Performance

In order to achieve near-optimal error-rate performance with lower hardware complexity, fixed-point arithmetic is used in this

TABLE I
FPGA IMPLEMENTATION RESULTS AND COMPARISON FOR 128×8 MIMO SYSTEM.

Detector	This work	M. Wu [26] [JSTSP'Nov. 14]	B. Yin [35] [ISCAS'15]	O. Castañeda [36] [ISCAS'16]	M. Wu [37] [TCAS-I'Dec. 16]
Method	IGS	NSE	CGLS	TASER	OCD
Performance	near-MMSE	near-MMSE	near-MMSE	near-ML	near-MMSE
Iteration #	1	3	3	3	3
Modulation	64-QAM	64-QAM	64-QAM	QPSK	64-QAM
Instance or subcarrier #	10	8	1	N.A.	24
Slices	35,721	48,244	1,094	4,350	11,094
LUTs	105,135	148,797	3,324	13,779	23,914
FFs	73,130	161,934	3,878	6,857	43,008
DSP48s	1,850	1,016	33	168	774
Block RAMs	20	16	1	0	2
Latency [clks]	202	196	951	225	795
Maximum clock freq. [MHz]	308	317	412	72	258
Throughput [Mb/s]	732	621	20	50	376
Throughput/LUTs	6,943	4,173	6,017	3,629	15,597
Throughput/FFs	9,982	3,835	5,157	7,292	8,743

(a) $N_r = 128$ and $N_t = 8$.

(b) $N_r = 64$ and $N_t = 8$.

Fig. 17. Fixed-point simulation result for proposed quantization scheme.

implementation. The associated word-lengths for the proposed architecture have been determined via numerical simulations. The parameters provided in the following refer to the real or imaginary part.

For PU, the channel matrix $\mathbf{H}$, the receive vector $\mathbf{y}$, and the noise variance N_0 are represented with 15 bit; the output of RGM is also quantized to 15 bit and it is then compressed to 9 bit with the proposed data compression scheme; the output of MF is set to 15 bit. For ISCU and GSMU, the input $\mathbf{D}$ and $\mathbf{E}$ are decompressed to 15 bit at beginning. For SCU, the input and the output are set to 15 bit and 12 bit, respectively. For LCU, its input is represented with 12 bit and its output is quantized to 10 bit. Here all multiplications are mapped onto DSP48 slices. The MAC registers are set to 22 bit. Each LUT in the reciprocal module has 1024 addresses and 15 bit outputs, implemented by a single B-RAM.

Fig. 17 compares BER performance of the proposed fixed-point scheme and the floating-point algorithms for 128×8 and 64×8 systems. One can observe that the degradation introduced by the fixed-point scheme is negligible, compared

to the floating-point result. Specifically, the implementation loss is less than 0.05 dB SNR at 0.1% BER.

B. FPGA Implementation Results and Comparison

Table I provides the key implementation results of our GS-based soft-output massive MIMO detector and compares it with the post-place-and-route results of other state-of-the-art massive MIMO detectors [26, 35–37]. In addition, Fig. 18 compares these detectors in terms of throughput and hardware overhead.

As discussed in Section III-E, the proposed IGS algorithm for massive MIMO uplink should be compared to other NSE-based algorithms with less number of iterations for the sake of fairness. Since the detectors presented in [26, 35, 37] are with $K = 3$ iterations and a 2-term NSE is used in our algorithm, the proposed IGS detector is implemented with only $K = 1$ iteration. As shown in Table I, our IGS detector has a much higher throughput (732 Mb/s) than the other detectors. One can also achieve a higher clock frequencies via increasing the number of pipeline stages, if the hardware complexity is

Fig. 18. Implementation comparison of state-of-the-art massive MIMO detectors.

affordable. Here we introduce the ratios of throughput/LUTs and throughput/FFs to measure the hardware efficiency of detectors. It is clear that our IGS detector achieves the highest hardware efficiency in terms of throughput/FFs, and the second highest hardware efficiency in terms of throughput/LUTs.

Furthermore, Fig. 1, 2, and 17 show that IGS with $K = 1$ iteration outperforms the NSE-based one with $K = 3$ in the case of different antenna configurations. In addition, for large system loading factors N_t/N_r (e.g., 16/64 and 8/64), the conventional NSE-based detection algorithm performs much worse than the proposed GS-based one, even results in convergence issues.

Table II reports the throughput of IGS detector with different number of iterations. It indicates that the proposed IGS detector with $K = 2, 3$ can still achieve higher throughputs than the other aforementioned detectors.

TABLE II
THROUGHPUT FOR K ITERATIONS WITH 64-QAM, 128 BS ANTENNAS,
AND 8 USERS.

	$K = 1$	$K = 2$	$K = 3$
LUTs	105, 135	105, 135	105, 135
FFs	73, 130	73, 130	73, 130
Latency [cls]	202	219	236
Maximum clock freq. [MHz]	308	308	308
Throughput [Mb/s]	732	675	626

VI. CONCLUSION

In this paper, we have proposed an efficient hardware architecture of the GS-based soft-output detection algorithm for massive MIMO systems. The proposed iterative algorithm employs a novel initial solution based on NSE to accelerate convergence. The proposed detection algorithm has shown its advantage of both convergence rate and BER performance in various antenna configurations and propagation environments. The corresponding VLSI architecture has been also provided with low hardware complexity. To further reduce the word-length of the regularized Gram matrix, a hardware-efficient

data compression/decompression scheme is proposed in this paper. Exploiting the Hermitian property of the 2-term NSE, the proposed architecture for NSE computation has a much lower processing latency. The optimized architecture for the GS method reduces the latency of each iterative by half. The provided reference FPGA implementation results have shown that our GS-based massive MIMO detector achieves a medium throughput with a much lower hardware complexity and a better error-rate performance, compared to the conventional ones. Future work focuses on iterative data detection and decoding in massive MIMO systems based on this work.

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