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Short Circuit Robustness and Carrier Lifetime in Silicon Carbide MOSFETs

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Abstract—Short circuit (SC) operation can lead to thermal runaway failures of SiC MOSFETs associated with leakage current uncommon to unipolar power devices. This paper presents the physical models required to simulate the leakage current in SiC power MOSFETs during SC accurately. It is shown that the SRH-generation carrier lifetime significantly affects the SC performance of SiC MOSFET, depending on defects in the epitaxial layer and processing induced damage. The temperature and field dependence of carrier lifetime as well as the surface recombination velocity are investigated and their influence on the SC current of a 1.2 kV SiC power MOSFET are presented.

Keywords—short-circuit robustness; SiC MOSFET; lifetime; SRH generation-recombination; leakage current

I. INTRODUCTION

The short-circuit (SC) experiments of SiC power MOSFETs at higher DC-link voltages (>50% of the rated voltage) point towards a thermal runaway failure mechanism [1,2,3]. The thermal runaway is associated with a leakage current causing parasitic BJT turn-on [2]. The channel current is ensured to be turned off with a sufficient negative gate bias [4]. However, under the SC operation, SiC MOSFETs may exhibit a leakage current that remains after the turn-off of SC operation, which is common for bipolar Si-IGBTs (the so-called tail current) but unexpected for unipolar power devices such as power MOSFETs. Accordingly, the physical mechanisms responsible for the leakage current limiting the SC capability of SiC power MOSFETs should be well understood in order to improve their SC ruggedness.

The leakage current has so far been explained from qualitative analysis based on simplified 1-D electro-thermal simulations [2] or with 2D TCAD electro-thermal simulations without emphasis on defects and carrier lifetime [1]. The aim of this paper is to analyze the nature of the leakage current present inside of SiC power MOSFETs during the SC operation in a comprehensive way. Particularly, the role of carrier lifetime on the generation of the leakage current is investigated taking into account the temperature-dependent SiC material parameters. The investigation is performed based on actual SC measurements and a calibrated 2D TCAD electro-thermal model developed in the Sentaurus TCAD for a commercial

planar gate 1.2 kV 80m Ω SiC power MOSFET from Wolfspeed (C2M0080120D) [5].

II. MODELING OF LEAKAGE CURRENT

Fig. 1 shows the measured drain current during SC tests performed on the MOSFET under test (C2M0080120D) at a DC-link voltage of $V_{DC} = 600$ V. A positive slope of the drain current before the SC operation turn-off can be observed for the SC duration t_{sc} above 8 μ s. Additionally, a non-zero drain current (i.e. tail current) increasing with the duration t_{sc} is present at the SC turn-off. The positive slope of the drain current is an indication for the on-set of leakage current in the device [1, 2]. Due to the high channel current and high voltage across the p-base/n-drift junction blocking V_{DC} , the device experiences a high power dissipation. The temperature distribution inside of the SiC power MOSFET during the SC operation is non-homogenous, the hotspot is located in the depleted JFET region, with the highest temperature, T_{max} , in the device reaching above 1500 K at failure[5].

Fig. 1: Drain current measured for C2M0080120D with increasing the SC pulse duration up to $t_{sc} = 10$ μ s with an initial temperature $T = 298$ K, $V_{DS} = 600$ V, $V_{GS} = 20$ V/-5 V.

In the developed TCAD model, the n+ source region and p-base have separate contacts in order to distinguish the current flowing through the channel (I_{source}) and the p-base (I_{base}). A large DC-link voltage, leads to an extension of the

depletion region around the p-base/n-drift junction towards (till) the heavily doped buffer layer below the drift region. Then the SC leakage current is first comprised of I_{base} , the p-n junction leakage current, which originates from the carrier generation current of the depletion region. The main thermal carrier generation-recombination (G-R) mechanism in SiC is Shockley-Read-Hall (SRH) [6].

A. SRH Generation-Recombination Process

The intrinsic carrier concentration, n_i , increases with temperature, which is modeled by $n_i(T)$ based on the temperature dependent bandgap narrowing effect [7]. Since in the depletion region $n \cdot p \ll n_{i,eff}^2$ from the standard SRH G-R rate formula [6], at high temperatures (i.e. above 1000 K) and the mid-gap position of the recombination center ($E_{trap} = E_i$), I_{base} is determined by:

$$I_{base} \approx 2q \int_{depletion} G(\vec{r}) dV \quad (1)$$

$$G(r) \approx \frac{n_i(T)}{\tau_n(T, r) + \tau_p(T, r)} \quad (2)$$

Thus, carrier generation G in the depletion region increases proportional to $n_i(T)$ and depends on electron and hole generation lifetimes, τ_n and τ_p , respectively that vary with temperature (T) and position (r). Due to different mechanisms and conditions involved, the generation lifetimes can differ from the recombination ones [12,15]. The ratio of electron and hole lifetimes τ_n/τ_p is assumed to be five [8] in all the simulations shown in this paper. The simulated 2D current density in a half-pitch MOSFET cell during the SC turn off with $V_{DS} = 600$ V, at $t_{sc} = 9$ μ s, is shown in Fig. 2 (right). As seen from Fig. 2 (left), the increase of the drain current, I_{drain} , and the excess base current, I_{base} , is comparable. The total I_{drain} of the device is the sum of I_{base} , and the source current, I_{source} .

Fig. 2: (left) SC current obtained from TCAD simulation for $t_{sc} = 10$ μ s with $V_{DS} = 600$ V; (right) Total current density in the half-pitch MOSFET cell at $t_{sc} = 9$ μ s showing the current through the base I_{base} . BJT onset occurs after $t_{sc} = 9$ μ s and hence I_{source} starts to increase rapidly.

Reducing the lifetimes (τ_p, τ_n) enhances the SRH generation in the depletion region of the p-base/n-drift junction of the MOSFET. With a larger SRH generation the total I_{drain} increases as the generated holes flow through the p-base to the base-contact. The influence of SRH generation lifetime is

shown in Fig. 3. Due to the increase of I_{base} , depending on the design of p-base/n+source doping and geometry [9], the parasitic BJT is triggered once the voltage drop at this junction reaches ~ 2.5 V, leading to the injection of carriers from n+source through the p-base and further increase in the leakage current by the gain factor β of the BJT. When the SC condition persists further, the thermal runaway occurs due to the positive temperature coefficient of the BJT current. In order to simulate the effect of SRH carrier generation on the SC current, standard doping, temperature, and the electric field dependence of the carrier lifetime is included in the SRH model, following Sentaurus TCAD Advanced Calibration.

Fig. 3: Comparison of simulated SC current at $V_{DS} = 600$ V with varying SRH generation lifetime $\tau_{max,n} = 2.5$ μ s (low SRH generation) and $\tau_{max,n} = 25$ ns (large SRH generation) with the defect level in the mid-gap ($E_{trap} = E_i$).

B. Carrier Lifetime – Doping Dependence

The doping dependence of lifetime is modeled based on the Scharfetter relation,

$$\tau_{dop} = \frac{\tau_{max,n,p}}{1 + \left(\frac{N_A + N_D}{N_{ref}} \right)^\gamma} \quad (3)$$

where the reference doping is considered as $N_{ref} = 3 \times 10^{17}$ cm^{-3} and $\gamma = 0.3$ [8]. Here, it should be noted that the value of γ is likely to be underestimated [10].

C. Carrier Lifetime – Temperature Dependence

The temperature dependence of carrier lifetime in 4H-SiC is commonly modeled in literature as $\tau_g \sim \tau_{max} \cdot (T/300)^\alpha$, where $\alpha = +1.72$ and $\tau_{max} = 1$ μ s were obtained from the recombination lifetime τ_r measurements presented in [11], i.e. τ_{max} is τ at the temperature of $T = 300$ K at low doping concentration. On the other hand, the experiments on bulk generation lifetimes from [12] suggest $\tau_g \approx 1$ -1000 ns in epitaxial 4H-SiC, however, the exact temperature dependence of τ_g was not revealed in [12]. With a lack of experimental results for temperature-dependent carrier lifetimes in 4H-SiC at high temperature levels as those

encountered during SC condition, a negative temperature dependence of lifetime with $\alpha = -1.5$ is considered in the proposed TCAD simulations based on [13]. Fig. 4 demonstrates the drain current modeling results in comparison to the measured drain current for the two values of α with $\tau_{\max,n} = 25$ ns (i.e. in the range of 1-1000ns). The simulated drain current at the failure matches to the measured current waveform with $\alpha = -1.5$.

Fig. 4: Influence of temperature dependence parameter of SRH lifetime on the SC current for $V_{DS} = 600$ V $t_{sc} = 10$ μ s.

D. Carrier Lifetime – Electric Field Dependence

The electric field dependence of carrier lifetime is incorporated in the TCAD simulation using phonon-assisted tunnel emission model [13]. Here, it is essential to choose appropriate parameters for 4H-SiC. As there is limited data for 4H-SiC published, the electron-phonon coupling strength S , i.e. Huang-Rhys factor, is considered to be $S = 10$ following [14]. The tunneling electron mass of $0.1m_0$ is adopted with the trap level in the mid-gap. Fig. 5 shows that light phonons ($\hbar\omega < 60$ meV) reduce the SC withstand time. For $\hbar\omega > 60$ meV, the field effect on lifetime reduction is minimal for $V_{DC} = 600$ V. SRH field enhancement can be used for fitting of the dependence of SC leakage current on the DC-link voltage.

Fig. 5: Simulated SC drain current with electric field dependence of carrier lifetime to show the influence of effective phonon energy ($\hbar\omega$). Huang-Rhys factor $S = 10$, $\tau_{\max,n} = 25$ ns, $V_{DS} = 600$ V.

III. PROCESSING DEFECTS

The SRH G-R is governed by the concentration of defects and their location in the bandgap. The carrier generation lifetime in 4H-SiC epitaxial wafers measured by Chung et al. [15] shows that the dominant defect affecting the generation lifetime is probably EH6/7 (attributed to $V_{C(0/+)}$) with energy level close to mid-gap ($E_c - 1.55$ eV) [16]. The proposed TCAD simulation of the SC current with $\tau_n = 25$ ns and defect energy levels corresponding to mid-gap (E_i), Z1/2 ($E_c - 0.63$ eV) and EH6/7 is shown in Fig. 6. It can be seen that deep levels such as EH6/7 accelerates the device failure during SC by early onset of the leakage current.

Fig. 6: Simulated SC drain current with the trap energy levels at mid-gap, $E_c - 0.63$ eV (for Z1/2), $E_c - 1.55$ eV (EH6/7) and measured SC current of C2M0080120D at $V_{DS} = 600$ V. The effect of EH6/7 is slightly larger than mid-gap as $\tau_n \neq \tau_p$ in the simulation ($\tau_n/\tau_p = 5$) in comparison to $\tau_n = \tau_p = 25$ ns, shown by the green dashed line.

In addition to the defect density inherent to the epitaxial layer, the processing of a SiC MOSFET (such as ion implantation for p-base and JFET region doping and annealing) can induce intrinsic point defects as well. The actual distribution of those defects is hardly known as they are mobile and can interact with each other causing recombination or creation of complex defects. The carrier lifetime has been varied locally in the p-base and JFET regions in the TCAD simulations in order to demonstrate the effect of reduced carrier lifetime in a certain area of the cell due to process damage schematically. Fig. 7 shows that a lower lifetime in the p-base and/or JFET region reduces the SC robustness by increasing the SRH generation current. Since the depletion region can expand over the whole n-drift epi-layer, a special care must be taken to control the damage induced by processing. In addition, non-homogeneous distribution of defects over the MOSFET area can increase the SRH generation and leakage in weak cells, which in turn can cause hot spot formation and subsequent failure during the SC. The SRH generation of carriers also occurs at the SiC surface, due to defects at the SiC/SiO₂ interface. The

surface carrier generation is considered in the TCAD simulation by the surface G-R velocity [17]. Fig. 8 demonstrates that even very large values of surface recombination velocity ($S0$) do not cause earlier onset of leakage current with a low $\tau_{\max,n}$ in the bulk. However, in devices with larger bulk $\tau_{\max,n}$, surface defects start to dominate. In this case, an increase in $S0$ from $1e3$ cm/s to $1e6$ cm/s reduces the SC withstand time by $\sim 20\%$.

Fig. 7: (top) Lifetime profiles in the half-pitch MOSFET cell; (bottom) Impact of low lifetime ($\tau_{\max,n} = 2$ ns) in the specific regions of the cell (bulk lifetime, $\tau_{\max,n} = 200$ ns) on the SC current.

Fig. 8: Influence of surface defects on the SC current at $V_{DC} = 600$ V, modeled based on the surface velocity $S0$ in comparison to the bulk defects modeled based on the generation lifetime $\tau_{\max,n} = 25$ ns, and $\tau_{\max,n} = 2.5$ μs.

IV. CONCLUSION

The device parameters influencing the leakage current during a SC condition in a SiC MOSFET with planar gate are demonstrated with an emphasis on the SRH generation carrier lifetime. The comprehensive TCAD simulation results correlated with the measured SC current point out that the defects leading to SRH generation current cause a leakage current during SC. Increasing carrier generation lifetimes by minimization of the deep level defect concentration can substantially decrease the leakage current during SC operation of SiC power MOSFETs and thus, increase their SC robustness.

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