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Scaled, Ferroelectric Memristive Synapse for Back-End-of-Line Integration with Neuromorphic Hardware

Laura Bégon-Lours, Mattia Halter, Francesco Maria Puglisi, Lorenzo Benatti, Donato Francesco Falcone, Youri Popoff, Diana Dávila Pineda, Marilyne Sousa, and Bert Jan Offrein*

Ohmic, memristive synaptic weights are fabricated with a back-end-of-line compatible process, based on a 3.5 nm $HfZrO_4$ thin film crystallized in the ferroelectric phase at only 400 °C. The current density is increased by three orders of magnitude compared to the state-of-the-art. The use of a metallic oxide interlayer, WO_x, allows excellent retention (only 6% decay after 10^6 s) and endurance (10^{10} full switching cycles). The On/Off of 7 and the small device-to-device variability (<5%) make them promising candidates for neural networks inference. The synaptic functionality for online learning is also demonstrated: using pulses of increasing (resp. constant) amplitude and constant (resp. increasing) duration, emulating spike-timing (resp. spike-rate) dependent plasticity. Writing with 20 ns pulses only dissipate femtojoules. The cycle-to-cycle variation is below 2%. The training accuracy (MNIST) of a neural network is estimated to reach 92% after 36 epochs. Temperature-dependent experiments reveal the presence of allowed states for charge carriers within the bandgap of hafnium zirconate. Upon polarization switching, the screening of the polarization by mobile charges (that can be associated with oxygen vacancies and/or ions) within the ferroelectric layer modifies the energy profile of the conduction band and the bulk transport properties.

1. Introduction

Artificial neural networks, by analogy with the brain, consist of collections of interconnected neurons. The information flows from a layer of neurons to another, through vector-matrix multiplications (VMM). Tasks such as classification are possible by training the network, i.e., adjusting the matrix elements or "synaptic weights." Analog,[1] in-memory[2,3] as well as neuromorphic[4,5] computers aim at implementing the VMM in the analog domain:[6,7] the "multiply" (through Ohm's law) and "accumulate" (through Kirchhoff's law) operation is performed by a parallel voltage drop through a cross-bar array of nonvolatile, programmable resistances. Different technologies exist for memristive devices: phase-change memory,[8] filamentary-based resistive random access memory,[9] and electrochemical memory[10] rely on ion motion, with intrinsic limitations. In contrast, ferroelectric synaptic weights rely on electrostatic effects: for example, Schottky barrier height[11] or width[12] modulation, or electrostatically induced metal–insulator transitions.[13] The neuromorphic computers' learning paradigms (unsupervised[14,15] or supervised[16,17]) require the ferroelectric memristive devices to show synaptic behavior, i.e., the ability to gradually decrease (depression) or increase (potentiation) their conductance upon voltage pulses emulating the effect on biological synapses of the pre- and postsynaptic spikes emitted by the neurons. Cointegrating ferroelectric materials with CMOS neurons became possible with the discovery of ferroelectricity in hafnia compounds.[18] In the race to miniaturization of front-end-of-line (FEOL) devices, logic functions and discrete multilevel memories are demonstrated at the 28 and even 22 nm node.[19]

Fabrication in the back-end-of-line (BEOL) relaxes the constraint on the device size, which can exceed micrometric dimensions: large numbers of nanometric ferroelectric domains can be contained in the active device area, allowing multilevel and/or analog conductance level updates, as demonstrated, for example, in field-effect transistors[20] and in metal–ferroelectric–insulator–metal (MFIM) devices. Based on thick HfO_2 layer, the band diagram of these two-terminal devices is engineered such that the electrons tunnel through the insulator, and partially through the ferroelectric.[21,22] These devices have a large dynamic range (>10), but suffer from a small current density (10^{-8} A cm^{-2} at 2 V), operate at voltages larger than 5 V (but ±8 V); and their large nonlinearity (which can be circumvented by

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the use of a logarithmic driver[3]) limit their usage for VMM. Furthermore, the dielectric interlayer is responsible for moderate retention[23] and endurance[24] performances. In contrast, in metal–ferroelectric–semiconductor (MFS) devices, the electrons see the full thickness of the ferroelectric. In the back-end, the process temperature cannot exceed 400 °C. 5–15 nm thick Hafnia films grown by atomic layer deposition can be crystallized in the ferroelectric phase with a moderate thermal budget by rapid thermal annealing,[25] laser annealing,[26] or millisecond-flash lamp annealing[27–29] but they result in low current densities. By decreasing the thickness, the current density increases, but at the cost of a higher thermal budget required for crystallizing the film, as shown in ref. [30] where 4 nm thick HZO requires 500 °C. As in ref. [31], where 600 °C are required to crystallize 5 nm of $HfZrO_4$ (HZO), ferroelectricity was demonstrated but not resistive switching. Ali et al.[32] reported synaptic functionality in HZO/Al_2O_3 bilayers with HZO thickness of 6 nm, but found that the On/Off ratio vanishes from 4 to 1 for 4 nm thick films, both crystallized at 800 °C.

In this work, ferroelectricity was obtained in a TiN/WO_x/HZO/TiN structure with an HZO film as thin as 3.5 nm crystallized at 400 °C, a thermal budget compatible with back-end-of-line. Compared to synaptic weights based on a 5 nm thick HZO layer fabricated in the same conditions[29] and to state-of-the-art MFIS HfO_2(10 nm)/Al_2O_3 bilayers,[21,22] the current density is three and six orders of magnitude higher respectively, drastically reducing their footprint. Their synaptic functionality, endurance, and retention properties were characterized. By thinning the HZO from 5[29] to 3.5 nm, the On/Off at 100 mV was reduced from 10 to 7, but the maximum voltage for linear read-out was increased from 30 to 70 mV. In addition, the cycle-to-cycle variation was improved from 10% to 2%. The synaptic weights were further integrated in a passive cross-bar array configuration. The performance of a neural network based on this technology was estimated. The conduction mechanisms across the device, as well as the mechanisms governing the resistive switching, were explored using structural and ferroelectric characterization, as well as temperature dependent electrical measurements.

2. Ferroelectricity in Ultrathin, Back-End Compatible Bilayer

TiN, WO_3, $HfZrO_4$ (HZO), and TiN layers were deposited by plasma-enhanced atomic layer deposition (PE-ALD) on an SiO_2 buffered Si substrate. The role of the WO_x interlayer, as discussed in ref. [33], is to induce an asymmetry in the energy profile of the memristor, leading to a resistive switching effect driven by the ferroelectric domain switching. TiN was chosen as a capping layer to promote the crystallization of HZO in the ferroelectric phase by a mechanical constraint during the annealing.[34] HZO was preheated to 400 °C, then a 20 ms long energy pulse of 90 J cm^{-2} was applied to crystallize it in the orthorhombic/tetragonal phase, without any fraction of the monoclinic phase, as is confirmed by the grazing incidence X-rays diffraction scan in **Figure 1**. For comparison, the green

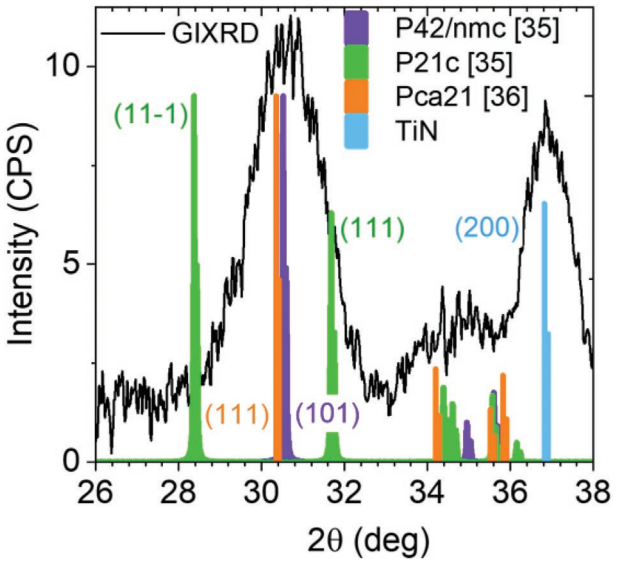

Figure 1. GIXRD scan of the device stack after crystallization (black curve). The green lines (resp. purple) correspond to the monoclinic HZO (resp. tetragonal ZrO_2) in Materlik et al.,[35] the orange lines to the orthorhombic HZO in Müller et al.,[36] the blue lines to TiN (CIF 1011102). X-ray reflectivity (Figure S1a, Supporting Information) confirms sharp interfaces and an ultralow HZO thickness of 3.5 nm. To confirm the back-end-of-line compatibility of the crystallization process, the same annealing was performed on MOSFETs (130 nm). The drain current as a function of the gate voltage characteristics of the annealed transistors fell within the spread of the characteristics of the pristine transistors. During the whole process, tools and temperatures compatible with back-end-of-line conditions were used: the devices were defined by optical lithography and reactive ion etching. The HZO, WO_x, and bottom TiN layer were etched using inductive coupled plasma with a CF_4 chemistry. The sputtered W metal lines were isolated by a SiO_2 spacer, deposited by plasma-enhanced chemical vapor deposition at 300 °C, as sketched in Figure S2 (Supporting Information). Devices with top electrode diameters comprised between 10 and 30 µm are fabricated. In the following sections, devices of 22 µm are chosen: their resistance around 10 MΩ is easily measurable with standard source measurement units.

lines (resp. purple) correspond to the monoclinic HZO (resp. tetragonal ZrO_2) in Materlik et al.,[35] and the orange lines to the orthorhombic HZO in Müller et al.[36] The peak at $2\theta = 37°$ is attributed to TiN (CIF 1011102). Fitting the peak at $2\theta = 30.2°$ by a Gaussian with a width at half maximum of $w = 1.7°$, using a k factor in the range 0.7–0.94, would lead to an in-plane crystallite size of $d = 3.8$–5.0 nm (Scherrer equation:[37] $d = k\lambda^{Cu}_{k\alpha 1}/(w\cos\theta)$). To get more insight on the microstructure of the film, high-resolution bright field scanning transmission electron microscopy (BF-STEM) image was acquired around the HZO/WO_x region of a cross section of the device and is presented in Figure S1b (Supporting Information). It reveals that the HZO grains have a typical in-plane dimension above 10 nm, indicating that the broadening of the GIXRD peak at $2\theta = 30.2°$ could be due to the presence of the tetragonal phase of HZO. The STEM analysis confirms the polycrystalline nature of the top and bottom TiN electrodes and of the HZO layer. It also reveals a columnar growth of the bottom TiN layer which translates into a slight WO_x and HZO roughness.

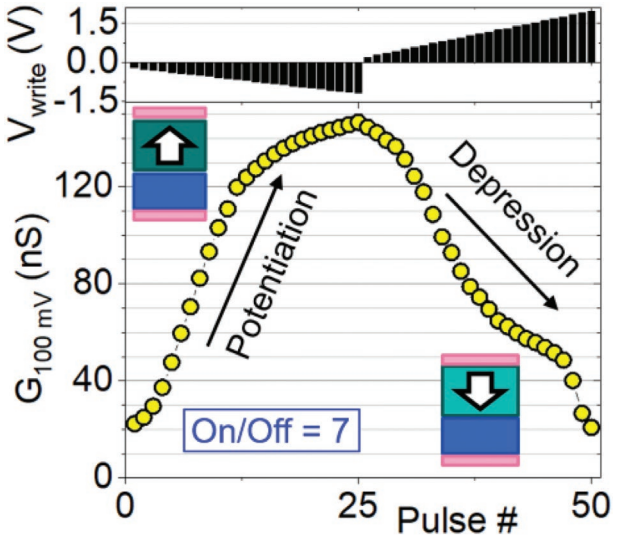

Figure 2. Potentiation and depression of the device upon DC pulses (the duration of the bias depends on the amplitude) of increasing amplitude V_{write}. The On/Off ratio is the maximal conductance divided by the minimal conductance.

3. A Ferroelectric Synaptic Weight

3.1. DC Resistive Switching

Potentiation (depression) of the two-terminal device was first obtained by applying a negative (positive) DC "pulses" of decreasing (increasing) amplitude with respect to the grounded TiN/WO_x electrode. In this DC configuration, the duration of the bias is not parametrized and decreases as the current flowing through the device, thus the amplitude, increases. After the application of each pulse of amplitude V_{write} (that varies in the –1.4 to 1.6 V range) the bias was set back to zero, then the conductance was measured at 100 mV, as shown in **Figure 2** (yellow data points). In the high resistive state (HRS), the HZO polarization points toward the WO_x layer (blue layer in the sketch in Figure 2). Upon the application of an increasing positive bias, the fraction of domains whose polarization points away from the WO_x layer gradually increases. The On/Off ratio, defined as the ratio of the device conductance in the low resistive state (LRS) and in the HRS is 7. More than 25 levels can be clearly distinguished. The nonlinearity of the long-term potentiation and depression was quantified by fitting the normalized data represented in Figure 2, by a function of the normalized pulse number $y : x \rightarrow \frac{1-e^{\left(-\frac{x}{A}\right)}}{1-e^{\left(-\frac{1}{A}\right)}}$, as proposed in ref. [38]. The parameter A was chosen by minimizing the root mean square error of the fitting. Values of $A_{LTP} = 0.5$ for the long-term potentiation and $A_{LTD} = -1$ for the long-term depression, respectively, were found. For a device area of 314 μm^2, the resistance in the LRS, R_{on}, is 7 MΩ. The device-to-device variation, measured at 0.1 V as shown in Figure S3 (Supporting Information), is 5%.

In **Figure 3**a, the *I*–*V* characteristics of a device in a 3 × 3 crossbar are presented. Below the voltage of 70 mV the characteristics are linear, and quasi linear at 100 mV which is ideal for

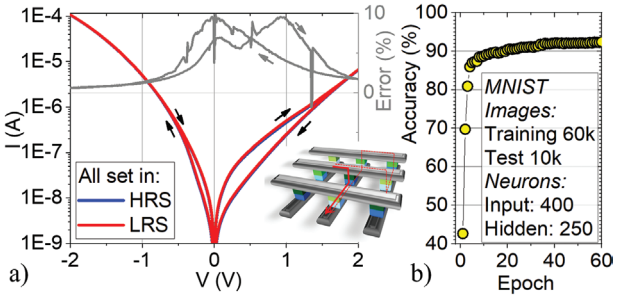

Figure 3. a) *I*–*V* of a device in a 3 × 3 array when the eight other elements are in HRS (blue line) or in LRS (red line). Gray line: relative error. b) Simulated accuracy of a 1R array of 400 input, 250 hidden and 10 output neurons (MNIST database).

vector-matrix multiplication when the input is mapped on this range. Above, the nonlinearity, quantified by the $I(V)/I(V/2)$ ratio, gradually increases from 3 at 0.6 V to 18 at 2.0 V, as represented in Figure S4 (Supporting Information). In a neural network, the use of a selector or a selector diode is required to suppress the sneak paths. To assess their effect, the current-voltage characteristic of the same device in the center of the array was measured in the worst-case scenario (all the other devices in the crossbar array were set to the LRS) and in the best-case scenario (all the other devices in the HRS). The unaddressed word and bit lines were floating during the measurement. The data, shown in Figure 3a, differ by maximum 10% (gray curve). With the parameters listed earlier, the online learning accuracy of a selector-less array of 400 input, 250 hidden, and 10 output neurons trained on the MNIST database was simulated using the "MLP+NeuroSimV3.0" framework.[39] It is a circuit level macro model designed for benchmarking neuromorphic architectures. The weight update characteristics and device parameters listed above are mapped to a list of parameters used for the simulation, and are provided in the Supporting Information. As shown in Figure 3b, the accuracy reaches 92% after 36 training epochs.

3.2. Pulsed Weight Update

The conductance was then modulated using an arbitrary waveform generator and trapezoidal pulses of constant rising and dropping time of 20 ns. **Figure 4** shows the conductance at $V_{read} = 100\ mV_{DC}$, measured after each write pulse of increasing amplitude (V_{write}) and of constant duration $t_{write} = 20$ ns. In the inset, the same data are represented as a function of the pulse number within the cycle: the conductance varies by less than 2% from cycle to cycle. The energy dissipated during the writing is minimal for $V_{write} = 0.2$ V ($E^{0.2\ V} \approx 10^{-15}$ J) and maximal for $V_{write} = -2$ V ($E^{-2\ V} \approx 10^{-12}$ J).

In **Figure 5**, the amplitude is kept constant (–1.4 V for potentiation, 2.0 V for depression) and the pulse width (t_{write}) is increased. With this scheme, 20% of the dynamic range is traversed after the first pulse (20 ns, lower limit of the generator). The circuitry required for the on-chip implementation of this scheme is more accessible than the one required by the scheme with increasing amplitude. Moreover, it emulates spike trains and shows that the proposed devices have potential

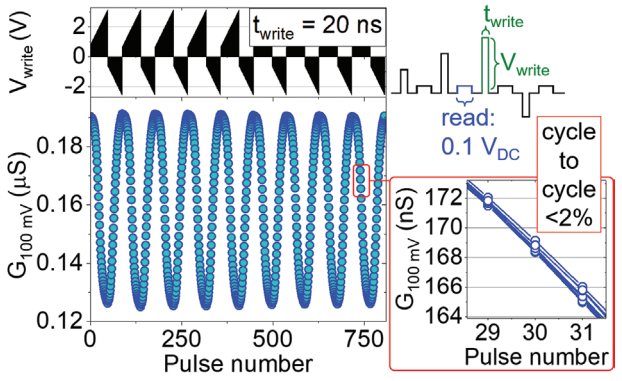

Figure 4. Synaptic potentiation and depression with pulses of increasing amplitude. The pulse amplitude V_{write} and the pulse duration t_{write} are defined as in the measurement scheme (top right). The inset shows the cycle-to-cycle variation.

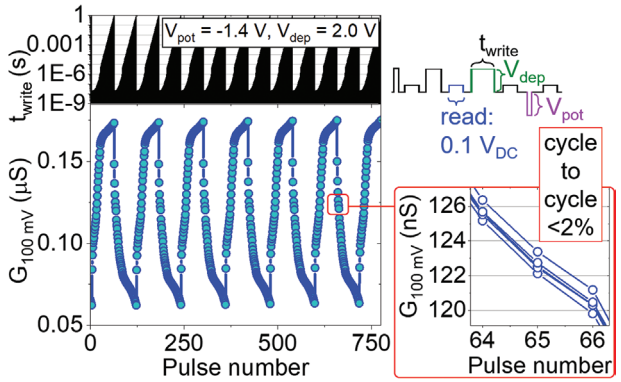

Figure 5. Long-term potentiation and depression for pulses with constant amplitudes V_{pot} and V_{dep} (as defined in the measurement scheme) and increasing duration t_{width}. The inset shows the cycle-to-cycle variation.

applications in neuromorphic systems implementing a spike-rate-dependent-plasticity learning rule.[40,41] The cycle-to-cycle variation for both schemes is <2%. Cumulative switching (upon applying pulses of constant width and amplitude) was not observed. Because of the dual dependence on the pulse amplitude and duration for ferroelectric synaptic weights, implementing spike-timing-dependent-plasticity (STDP) rules with such devices requires tailored spike shapes as described by Boyn et al. in ferroelectric perovskites[42] and Max et al. in ferroelectric hafnia.[21]

Retention properties were measured for over ten days: the worst-case scenario corresponds to a 6% decay at 300 h (10^6 s) in the case where the polarization points toward the oxide interlayer (pink triangles in Figure S5, Supporting Information). This confirms that the devices based on a metal oxide/ferroelectric bilayer showed limited back-switching compared to devices based on a dielectric interlayer: for comparison, optimized junctions based on a SiO_2/Si:HfO_2 bilayer showed a 30% decay.[43] This observation is consistent with a better screening of the polarization charges by the metallic WO_x, which implies a reduction of the depolarization field across the HZO ferroelectric layer that leads to improved retention characteristics. Finally, the devices showed strong robustness against fatigue, with no dielectric breakdown after more than 10^{10} full switching cycles (±2 V at 100 kHz). Dynamic hysteresis measurements performed during the endurance experiment can be found in Figure S6 (Supporting Information).

4. Investigation of the Resistive Switching Mechanism

Both tungsten oxides[44] and hafnium oxides[45] were used as memristors operating with the displacement of oxygen vacancies and ions. In this work, the current density (see Figure S7a, Supporting Information) is constant in the range (–2 V; 2 V) for circular devices with diameters in the 10–30 µm range: Figure S7b (Supporting Information) shows the resistances measured at 0.1 V in the HRS and LRS in logarithmic scale, showing a constant On/Off ratio of 7. The homogeneous conduction across the device indicates there is no filament or conduction at the edges. In addition, for a given polarity, resistive switching was only observed for pulses of increasing amplitude or time. Electroresistance loops (Figure S8, Supporting Information) revealed hysteretic behavior: the resistance increases (resp. decreases) while the amplitude increases from 0 to 2 V (resp. decreases from 0 to –2 V), then remains constant as the amplitude decreases from 2 to 0 V (resp. increases from –2 to 0 V). Moreover, a saturation is observed above 1.8 V and below –1.5 V. This discards current-driven resistive switching mechanisms (governing, e.g., filamentary resistive memories for which the weight update is performed by successive identical pulses).

Positive-up-negative-down (PUND) experiments were performed to measure the ferroelectric properties of the devices. The waveform is schematized in Figure S9a, Supporting Information). The polarization for a 60 µm capacitor measured at 50 kHz is represented in Figure S9b (Supporting Information). As for the current density, the polarization (per unit area) is independent on the device area (circular devices of diameter 40, 50, and 60 µm), and confirms the ferroelectric properties of the devices ($2P_r \approx 4.5$ µC cm^{-2}). This value is low compared to 10 nm films (≈20 µC cm^{-2}) due to the reduced thickness. For a constant voltage range (–1 to 1 V), the polarization decreases with the frequency of the measurement, as represented in **Figure 6**: this effect reflects the dependence of the resistive

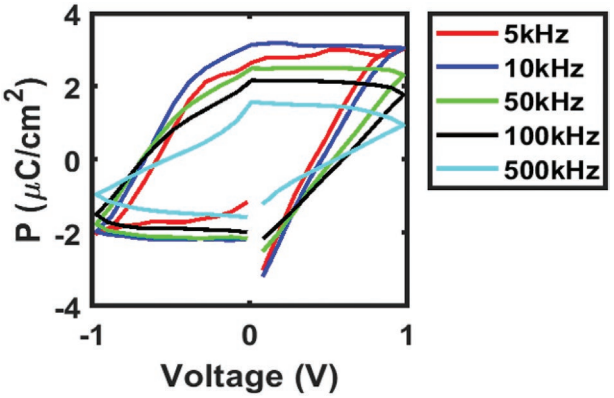

Figure 6. Polarization measured by the PUND method for a 60 µm capacitor, for various frequencies.

switching on the pulse duration observed in Figure 5. The polarization switching occurs over a broad range of coercive fields (from ±0.2 to above ±1 V), matching the voltage range where the resistive switching is observed (see Figure 2. Such broad distribution is explained by the polycrystalline nature of the HZO film, determined by the X-ray analysis in Figure 1. Finally, we observed that the resistive switching saturates upon increasing field amplitude for both polarities (see the electroresistance loops in Figure S8, Supporting Information). These observations are consistent with the resistive switching originating from ferroelectric domains switching: it saturates when all the domains are aligned in the same direction. The multiple intermediate configurations are allowed by the polycrystalline nature of HZO: because of their different orientations and environment, some grains require a smaller electric fields to switch than others. By applying pulses of intermediate amplitude or duration, a fraction of the domains can be switched.

The role of the WO_x interlayer between the bottom TiN electrode and the HZO layer is to create an asymmetry in the energy profile of the device. By reversing the polarization from outward to toward this interlayer, the energy barrier seen by an electron is modified. A test structure was fabricated without the WO_x interlayer. The surface of the bottom TiN electrode is expected to be oxidized by the oxygen plasma applied during the HZO deposition. Despite this small asymmetry and consistently with the mechanism proposed above, no resistive switching was observed (see Figure S10, Supporting Information). In this paragraph, the relative contribution of WO_x to the overall resistance is discussed. WO_3 is an insulator with a bandgap of 3.40 eV; oxygen vacancies create donor states that push the Fermi level close to the conduction band, conferring n-type semiconducting properties to WO_x.[46] For $x < 2.9$, WO_x shows metallic behavior.[47] The situation where WO_x is most likely to contribute to the resistance of the device is when the polarization points away from the WO_x layer, after applying a negative bias on the top (TiN) electrode, causing an electrostatic depletion of electrons in the WO_x. From the resistive switching experiments (e.g., in Figure 2), this corresponds to the LRS of the synaptic weight. This shows that the resistance change in the WO_x layer is small compared to the resistance change in the HZO layer. In addition, a chip with identical HZO thickness but with a WO_x layer thickness of only 1 nm (compared to 2 nm for the reference stack) was fabricated. Two devices of the same diameter (80 µm) but different WO_x thicknesses shared the same LRS of $R_{On} = 1.13$ MΩ, showing that the resistance of the WO_x layer was small compared to the resistance of the HZO layer. In the following paragraph, we assume that the electric field drop in the WO_x is small compared to that in the HZO layer.

The conduction mechanisms across the devices were then analyzed with current–voltage (I–V) sweeps between 25 and 55 °C, back and forth with no degradation observed upon heating. Although the On/Off ratio remains constant, the resistance decreases with increasing temperature, as shown in **Figure 7** and Figure S8 (Supporting Information). For this

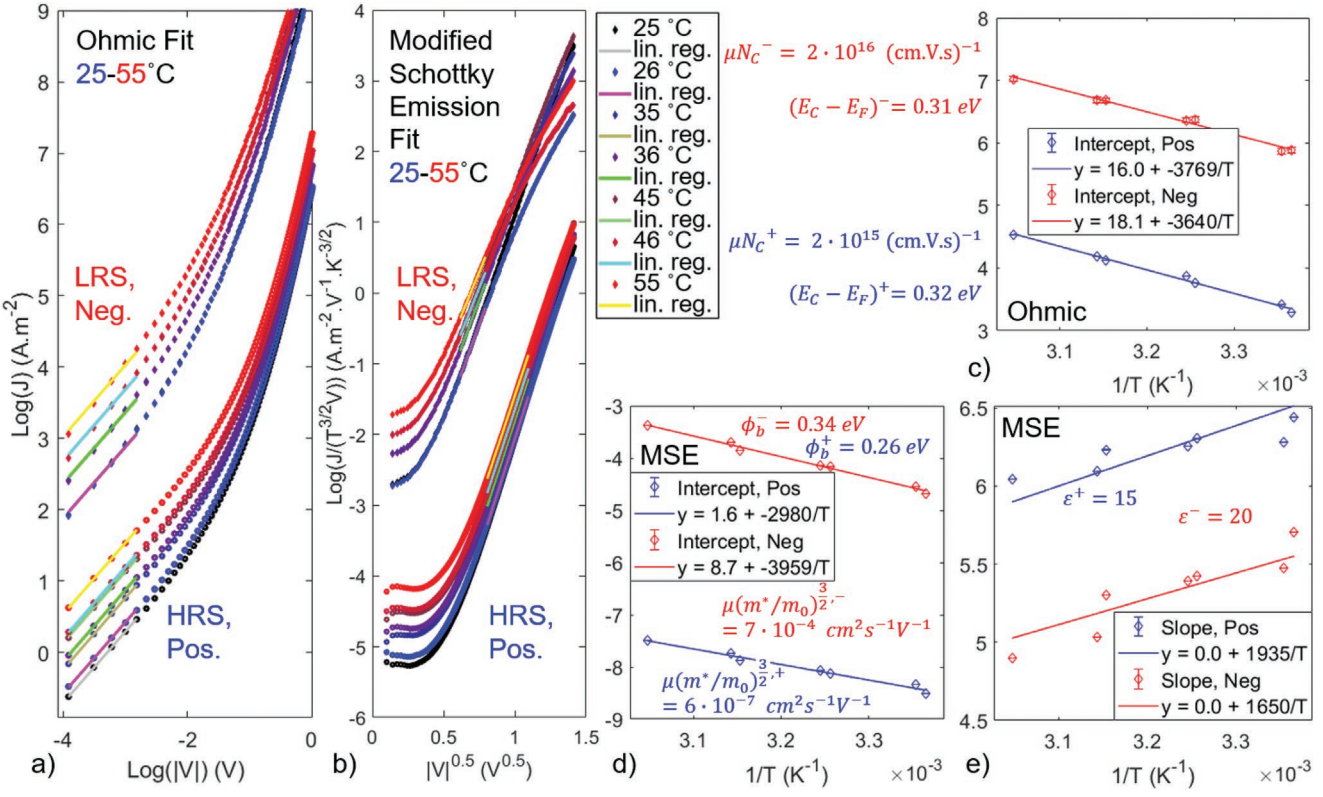

Figure 7. Current–voltage characteristics in the a) Ohmic and b) modified Schottky emission (MSE) representations. At each temperature, a linear regression is performed on the negative, increasing branch (LRS, nonswitching) and on the positive, decreasing branch (HRS, nonswitching). c) Arrhenius plots allow the calculation of the μN_C and E_C–E_F parameters from the intercepts of the linear regressions in the Ohmic regime, d) the $\mu(m^*/m_0)^{3/2}$ parameter is calculated from the intercepts of the linear regression in the MSE regime, and e) the parameters Φ_B, ε from the slopes of the latter.

reason, direct tunneling[48] and Fowler Nordheim tunneling[49] (respectively proposed in refs. [50] and [51]) were discarded as being the dominant transport mechanism. At low bias, below 70 mV and where the On/Off ratio is maximal, Ohmic conduction is observed, due to the drift of a small number of mobile electrons in the material's conduction band.[52] It is described by

$$J = \sigma E = \mu q N_C \exp\left[\frac{-(E_C - E_F)}{kT}\right] E \quad (1)$$

equivalent to

$$Log\left(J\right) = Log\left(\mu q N_C / t\right) + \frac{-(E_C - E_F)}{k} \times \frac{1}{T} + Log\left(V\right) \quad (2)$$

where J is the current density, σ the electrical conductivity, μ the electron mobility, q the electronic charge, N_C the carrier concentration at equilibrium, t the sample thickness, $E_C - E_F$ the energy difference between the conduction band and the Fermi level, k the Boltzmann constant, T the absolute temperature, and E the electric field across the ferroelectric layer. As discussed in the previous paragraph, the electric field was assumed to drop mainly across the ferroelectric layer resulting in $E = V/t$ where the thickness t is equal to 3.5 nm. Only the nonswitching branches of the IV sweeps were analyzed. The product μN_C is assumed independent of the temperature.[52] At each temperature, a linear regression was performed in the Log(V) ↦ Log(J) representation, shown in Figure 7a. Figure 7c shows the Arrhenius plot of the intercepts of the linear regression in the Ohmic regime: the presence of the conduction band at only 0.3 eV above the Fermi level, deducted using Equation (2), indicates the presence of donor states in the bandgap of HZO (≈5.4 eV[53]). Such states could originate from the presence of oxygen vacancies, but also from hydrogen trapped in the lattice during the atomic layer deposition.[54] From Figure 7c and Equation (2), we found that the resistive switching originates from an increase by one order of magnitude in the μN_C product in the LRS compared to the HRS.

At large fields (below –600 mV and above 1.5 V) the I–V characteristics keep the same diode-like polarity regardless of the polarization direction, showing that the energy band diagram of the TiN/HZO/WO_x junction is not structurally modified upon polarization reversal as, for example, in refs. [55–57].

At intermediate bias (from –400 to –640 mV and 640 to 1200 mV) we first considered electrode-limited mechanisms: the thermionic emission model[58] (proposed in ref. [59]) fitted reasonably well the data, however the Richardson constant obtained was of the order of 0.1 A m^{-2} K^{-2} in the HRS and 100 A m^{-2} K^{-2} in the LRS, which is orders of magnitude smaller than the universal Richardson constant[60] (≈10^6 A m^{-2} K^{-2}). Bulk-limited conduction mechanisms were also studied: similarly, it was possible to fit the experimental data with a Poole–Frenkel conduction model (proposed in ref. [61]), but the dielectric constant obtained with this model was unrealistically as high as 60. Thermionic-field emission,[62] hopping,[63] and space-charge-limited[63] fittings were not satisfying. Phonon-mediated trap-assisted-tunneling[64] and simplified trap-assisted-tunneling[65] models, in a single branch approach, were not fitting the data on a sufficient range. Regardless of the conduction mechanisms explored, the corresponding barrier height seen by the electrons on the negative branch (TiN to HZO injection, Φ_b^-) is higher than in the other polarity (Φ_b^+), although the current flowing is larger. It supports the description of the transport by a "modified Schottky emission" (MSE) mechanism,[66] which confers both electrode and bulk limited characters to the conduction. The MSE model was previously observed in ZrO_2 thin films[67] and describes the experimental data well. It is governed by the equation

$$J = \alpha T^{\frac{3}{2}} E \mu \left(\frac{m^*}{m_0}\right)^{\frac{3}{2}} \exp\left[\frac{-q\left(\phi_B - \sqrt{qE / 4\pi\varepsilon_r\varepsilon_0}\right)}{kT}\right] \quad (3)$$

equivalent to

$$\log\left(\frac{J}{T^{\frac{3}{2}}V}\right) = \frac{\alpha}{t}\mu\left(\frac{m^*}{m_0}\right)^{\frac{3}{2}} + \frac{-q\phi_B}{k} \times \frac{1}{T} + \frac{-q\left(\sqrt{q / t4\pi\varepsilon_r\varepsilon_0}\right)}{k} \times \frac{1}{T} \times \sqrt{V} \quad (4)$$

where $\alpha = 3 \times 10^{-4}$ A s cm^{-3} $K^{-3/2}$ is a constant, m_0 the free electron mass, m^* the effective electron mass in HZO, $q\phi s$ the Schottky barrier height, ε_0 the permittivity in vacuum, and ε_r the dynamic dielectric constant. Linear regressions in the representations of Log($J/(T^{3/2}V)$) as a function of $|V|^{0.5}$ were performed (Figure 7b).

For this mechanism, the barrier heights measured from Figure 7d and Equation (4) are $\phi_b^- = 0.34$ eV and $\phi_b^+ = 0.26$ eV. Consistently with the increase of μN_C measured at low bias, the average product $\mu(m^*/m_0)^{3/2}$ calculated from Figure 7d and Equation (4) increases by several orders of magnitude from the HRS to the LRS. On average, the dynamic dielectric constant ε, calculated from Figure 7e and Equation (4) also increases.

The models describe HZO as a semiconductor and show that the resistive switching originates from the modification of bulk transport properties upon polarization reversal. Such modification can be explained by the displacement of charged defects within the semiconducting ferroelectric layer upon polarization switching in the vicinities of the interfaces. The displacement of charged defects is driven by the screening of the polarization charges as observed recently in substoichiometric $BaTiO_{3-x}$ tunnel junctions,[68] but also in a polymer ferroelectric.[69] The simplified analytical models presented above do not capture eventual gradients within the HZO layer: further analysis using compact models simulations[70] may further improve the understanding of the resistive switching in the HZO/WO_x bilayers.

5. Conclusion

In this work, ferroelectricity was obtained in TiN/WO_x/ HZO/ TiN structure with an HZO film as thin as 3.5 nm crystallized at 400 °C, a thermal budget compatible with back-end-of-line. Thanks to the reduced thickness, the current density

was increased by three orders of magnitude compared to the state-of-the-art[33] and the devices operate in the Ohmic regime for read-out, which makes them ideal memristors for analog vector-matrix multiplication. The use of a metallic oxide electrode, WO_x, enables good retention properties: the conductance in the less stable state varies by only 6% after 10^6 s. In comparison, optimized MFIM devices show a 30% decay for the most stable state.[43] The On/Off of 7 and the small device-to-device variability (<5%) make them promising candidates for neural networks inference.

In addition, the synaptic functionality was demonstrated using pulses of increasing amplitude and constant duration, emulating spike-timing dependent plasticity. Using pulses as short as 20 ns, the writing energy was in the femtojoule range. Spike-rate dependent plasticity was also emulated, using pulses of constant amplitude (of only 2 V) and increasing duration. For both schemes the cycle-to-cycle variation was below 2%. The current–voltage nonlinearity in the range of 3–18, allowing limited effects of the sneak paths on addressing a device in passive cross-bar arrays, which was verified on a 3×3 cross-bar. Using the weight update nonlinearity parameters of 0.5 and –1, the training accuracy of a neural network based on the proposed synapse on the MNIST data set was estimated to reach 92% after 36 epochs. In addition, the endurance of the devices exceeds 10^{10} full switching cycles.

The conduction mechanisms across the device, as well as the mechanisms governing the resistive switching, were explored using temperature-dependent experiments: the results indicate the presence of allowed states for charge carriers within the bandgap of HZO, originating from defects such as oxygen vacancies. Upon polarization switching, the screening of the polarization by mobile charges (that could be associated with oxygen vacancies and/or ions) within the ferroelectric layer modifies the energy profile of the conduction band and the bulk transport properties.

6. Experimental Section

Device Preparation: A 200 nm thick SiO_2 oxide was grown on Si by thermal oxidation. The active stack was then deposited by PE-ALD: 20 nm of TiN was deposited at 300 °C with tetrakis(dimethylamino) titanium and N_2 as precursors. 2 nm of WO_x was deposited at 375 °C with $(BuN)_2W(NMe_2)_2$ and O_2, then 3.5 nm of HZO was deposited at 300 °C alternating one cycle with tetrakis(ethylmethylamino) hafnium(IV) and O_2, and two cycles with bis(methylcyclopentadienyl) (methyl)(methoxy)zirconium(IV) and O_2. Ten additional nanometers of TiN were deposited. The crystallization was performed with the millisecond flash lamp annealing technique:[27] the sample was preheated to 400 °C, then a 20 ms long energy pulse of 90 J cm^{-2} was applied. A 100 nm thick W metal electrode was then deposited by sputtering. The top electrode, defining the area of the junction, was defined by optical lithography and reactive ion etching (RIE) of the W and top TiN layers. Using this method, the HZO layer acted as an etch stop. The bottom electrode was then defined by optical lithography and inductive coupled plasma reactive ion etching (ICP) of the HZO, WO_x, and TiN layers. A 100 nm thick SiO_2 passivation layer was deposited at 300 °C by plasma-enhanced chemical vapor deposition (PECVD). Vias to the top and the bottom electrode were defined by optical lithography. The SiO_2 layer was etched by RIE, then the HZO and the WO_x were etched by ICP, exposing the TiN layer to air. The etch was immediately followed by the sputtering of 100 nm of W. The first metal lines were then defined by optical lithography and etching by RIE. A 100 nm thick SiO_2 passivation layer was deposited at 300 °C by PECVD. Vias to the bottom electrode contacts were defined by optical lithography. The SiO_2 layer was etched by RIE. 100 nm of W was sputtered. The second metal lines were then defined by optical lithography and RIE.

Structural Characterization: Grazing-incidence X-ray diffraction (GIXRD) and X-ray reflectivity (XRR) measurements were performed on a Bruker D8 Discover diffractometer equipped with a rotating anode generator. The lamella for STEM analysis was prepared by focused ion beam (FIB) using an FEI Helios NanoLab 450S. STEM analysis was carried out on a double spherical aberration-corrected JEOL JEM-ARM200F microscope. BF-STEM images were acquired at 200 kV.

Electrical Characterization: Electrical measurements were performed on an Agilent B1500A semiconductor analyzer with a B1530A waveform generator/fast measurement unit (WGFMU). Write pulses were generated by a remote-sense and switch unit (RSU) module close to the probe and applied to the top electrode while the bottom electrode is grounded. The device resistance was measured at $V = \pm 100$ mV with a high-resolution source-measurement unit (SMU) at the top electrode while the bottom electrode was grounded.

PUND experiments were performed to measure the ferroelectric properties of the devices. The waveform is schematized in Figure S9a (Supporting Information): during each of the P (positive, switching), U (positive, nonswitching), N (negative, switching), and D (negative, nonswitching) pulses of period T, the current I was measured during a time t_{READ} (that depends on the voltage range spanned and on the frequency) at a voltage V, then the voltage was increased by 0.1 V during a 20 ns long ramp. The polarization was calculated from the measured I–V curves.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

back-end-of-line, ferroelectrics, resistive switching, synaptic weight, transport

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