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## Journal Article

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**Publication date:**

2013-07

**Permanent link:**

<https://doi.org/10.3929/ethz-b-000068506>

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**Originally published in:**

IEEE Transactions on Power Delivery 28(3), <https://doi.org/10.1109/TPWRD.2013.2260359>

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Digital Object Identifier: [10.1109/TPWRD.2013.2260359](https://doi.org/10.1109/TPWRD.2013.2260359)

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# Contribution of Fault Current Sources in Multi-Terminal HVDC Cable Networks

Matthias K. Bucher, *Student Member, IEEE*, and Christian M. Franck, *Senior Member, IEEE*

**Abstract**—The scope of this paper is the investigation of the development of fault currents in a circuit breaker during a pole-to-ground fault in a generic multi-terminal HVDC cable system based on Voltage Source Converters. It aims to contribute to the current discussion of which requirements on breaking time and peak current HVDC circuit breakers need to fulfill in such networks. Therefore, the fault current is broken down into the individual contributions from the different network components and the influence of the key parameters on the development of the fault current in the circuit breaker of the faulted cable is illustrated.

**Index Terms**—HVDC transmission, Power system faults, Power system simulation, PSCAD.

## I. INTRODUCTION

OFFSHORE wind farms are widely recognized as a key component of the roadmap towards a low carbon electricity supply. The installed capacity of fully commissioned offshore wind turbines in Europe reached more than 3200 MW, with another 3850 MW presently under construction and significantly more installations planned [1]. Up to now, the power transmission from offshore wind farms has been exclusively based on point-to-point connections either using HVAC or HVDC submarine cables. However, academics, industry consortiums, and environmental NGOs have envisioned the creation of an interconnected HVDC offshore power network [2]–[6]. Visions for an offshore network on the US east coast are similarly ambitious [7]. Expected benefits from an interconnected HVDC network include increased system redundancy, higher flexibility for power trading, and reduced investment and operational costs.

As HVAC cables are not technically viable for long transmission distances, such an offshore network has to be based on HVDC interconnections. The latest developments in HVDC technology such as higher ratings of the semiconductor devices and the introduction of Voltage Source Converters (VSC) make the Multi-Terminal HVDC (MTDC) network a viable option.

Grid protection is currently one of the main drawbacks for MTDC networks. While AC side circuit breakers (CBs) can adequately protect point-to-point HVDC connections, the same protection concept would not be viable for HVDC grids, as it requires the de-energization of the entire system [8], [9]. DC CBs are needed to selectively isolate a faulty cable by quickly and reliably breaking DC fault currents. There are

several concepts for DC CBs [10], [11], [3], which still have significant drawbacks in terms of on-state losses or speed. Other concepts to address fault clearance have to be chosen as long as no fully satisfying DC CB concept is developed [12].

This paper aims to contribute to the better understanding of the transient development of the fault current through a DC CB during a pole-to-ground fault in an MTDC cable network. Therefore, the fault current is broken down into the individual contributions from the different network components, such as DC capacitors, cables, and the adjacent AC network. A breakdown of the fault current allows for a detailed analysis of the influence of the component parameters and fault condition on the total fault current in the DC CB. It enables the specification of DC CB requirements and fault detection mechanisms, as well as the identification of measures to reduce the transient overcurrent in the CB without additional Fault Current Limiters (FCLs). The paper illustrates the sensitivities of the key parameters in different scenarios, which consider the converter technology including the required filters and the fault condition, i.e. the fault impedance.

To do so, this paper analyzes pole-to-ground faults in a simple, radial, bipolar three-terminal HVDC cable system with two cable branches only. This is the simplest possible layout including all available components, which are able to contribute to the fault current in the CB. While cable faults occur less frequently than overhead line faults, but are typically permanent, it is still a condition that a future DC network has to cope with. The emphasis in this paper is on pole-to-ground faults, since they are regarded as significantly more frequent compared to pole-to-pole faults [13], although the latter fault would lead to more severe conditions [14].

The paper is structured as follows: Section II explains the transients in an HVDC system during a pole-to-ground fault and Section III describes the methodology of transient simulation, cable modeling, and the network model implemented in PSCAD. Section IV presents and discusses the results of the simulations followed by the conclusions in Section V.

## II. TRANSIENTS IN HVDC NETWORKS

Potential sources of transients in an HVDC network include surges due to pole-to-ground faults, pole-to-pole faults, the operation of switching devices, and the sudden loss of a terminal and the subsequent change in the DC voltage. In the following, only pole-to-ground faults in bipolar underground cable systems with two-level VSC terminals are considered.

Aging of the cable's main insulation or external damages due to digging or anchoring in case of sea cables [15] may lead to a breakdown of the cable insulation. First, an arc

Manuscript received October 30, 2012; revised March 01, 2013; accepted April 19, 2013. This work was financially supported by ABB Switzerland Ltd, Siemens AG, Alstom Grid, and the Swiss Federal Office of Energy (BfE).

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burns between the pole and the sheath of the cable and a ground loop through the sheath and the next grounding point is established. The current through the arc increases rapidly, which likely leads to explosion and destruction of the cable at the ground fault location. Subsequently, the arc burns between the pole and the ground, and a low-ohmic path is established in between. After the ground fault occurs, the voltage at the fault location decreases within a few microseconds to a level given by the fault resistance. Its value depends on the magnitude of the fault current and the characteristics of the soil, e.g. the ionization and de-ionization time constants, and the soil resistivity, as described in [16]. The voltage drop at the fault location occurs very quickly, but not instantaneously due to the voltage supporting, distributed cable capacitance and the inductance in the fault path. The severity of the pole-to-ground fault depends on the value of the fault resistance and thus on the characteristics of the discharge path. In general, the higher the fault resistance, the lower the voltage drop along the line. Right after the fault occurrence, negative voltage surges start to travel from the fault location into both directions towards the terminals. Along its way, the distributed cable capacitance is discharged gradually into the ground fault. Upon the arrival at the terminals after the traveling time  $\tau$ , the negative voltage surge is reflected back as a positive surge due to the capacitive termination of the cable given by the DC capacitors [17], [18]. DC capacitors include the VSC capacitors and possible tuned filter capacitors, which are usually installed at the DC side of a VSC in order to reduce the voltage ripple injected by the converter. The converter technology determines the size of the DC capacitor. In general, multi-level converter topologies require less filtering, but larger converter capacitors due to the lower valve switching frequency. A 3-level neutral point clamped VSC requires an about three times higher capacitor volume than a 2-level topology for the same target value of less than 5% voltage ripple on the DC line [19]. Other topologies such as the Modular Multi-level Converter (MMC) [20] with a sufficiently large number of submodules do not need any filter capacitances and the blocked converter valves prevent a discharge of the storage capacitors during DC faults [21]. In bipolar HVDC schemes, the midpoint of the DC capacitors is usually grounded to provide a reference voltage to the pole voltages [22], [19]. The midpoint is grounded either via a low-ohmic connection or through a reactor depending on the requirement, whether the bipole has to be able to be operated in monopolar mode or not. The grounded capacitor midpoint and the ground fault form a loop that provokes a discharge of the capacitors. This discharge current is superposed on the reflected, backward traveling surge, which can be approximated by the convolution of the incident wave form and the impulse response of the DC capacitor [23] (assuming a purely capacitive cable termination):

$$v_{\text{reflected}}(t) = \left[ -\delta(t) + \frac{2}{R_c C} e^{-\frac{t}{R_c C}} u(t) \right] * v_{\text{incident}}(t) \quad , \quad (1)$$

where  $R_c$  is the approximated, concentrated cable resistance,  $C$  the DC capacitance,  $\delta(t)$  a Dirac pulse, and  $u(t)$  a step function.

As the surge arrives again at the fault location, one part is reflected and the other part transmitted through the fault into the opposite section of the cable according to the reflection coefficient  $\Gamma$  and transmission coefficient  $T$  as depicted in Fig. 1. The forward and backward traveling waves result in multiple peaks in the current wave form. The reflection coefficient is given by:

$$\Gamma = -\frac{1}{1 + 2\frac{R_f}{Z_c}} \quad , \quad (2)$$

where  $R_f$  is the fault resistance and the surge impedance of the cable is

$$Z_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad . \quad (3)$$

Fig. 2 illustrates the dependence of the reflection coefficient on the magnitude of the fault resistance. The transmission coefficient is related to the reflection coefficient as follows:

$$T = 1 + \Gamma \quad . \quad (4)$$

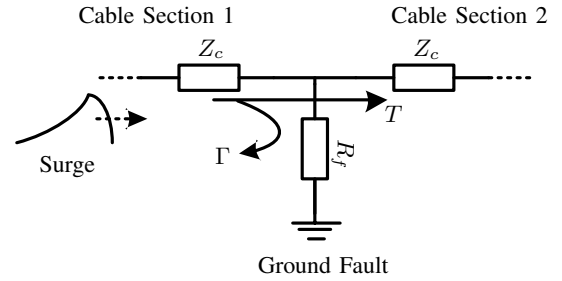


Fig. 1. Reflection and transmission of surges at fault location

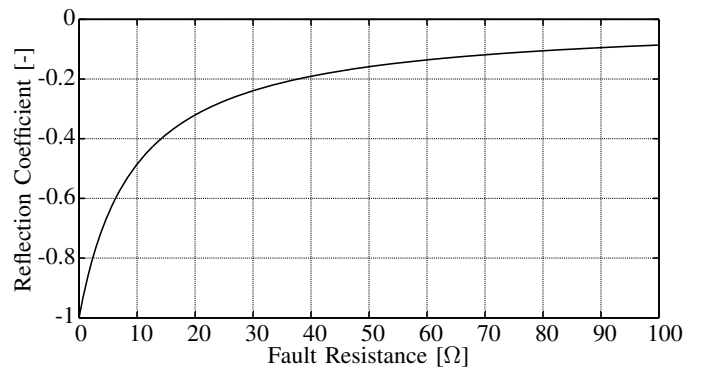


Fig. 2. Reflection coefficient at fault location as a function of fault resistance

### III. METHODOLOGY

A general description of time domain solution approaches that are evaluated for the simulation of transients, as well as the cable, converter, and network models are given in this section.

### A. Solution Approach

A widely used time domain method for the simulation of transients in power systems is the Electromagnetic Transient Program (EMTP) [24]. It allows an accurate simulation of transients in networks modeled by distributed as well as lumped elements and permits the inclusion of the frequency dependence of the line parameters. All EMTP based time domain solutions are based on the decoupling of the sending and receiving end of the transmission line given by the traveling time of the wave. Fig. 3 depicts an EMTP two-port model of the transmission line.

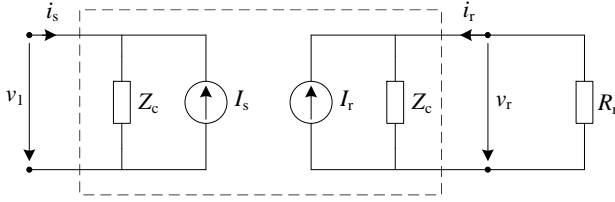


Fig. 3. EMTP line model for time domain solution based on [25]

From Fig. 3 follow the equations for the sending end and receiving end currents using a simulation time step of  $\Delta t$ :

$$i_s(t) = \frac{1}{Z_c} v_1(t) - I_s(t - \Delta t) \quad (5)$$

$$i_r(t) = \frac{1}{Z_c} v_r(t) - I_r(t - \Delta t) \quad , \quad (6)$$

with the past values of the equivalent current sources

$$I_s(t - \Delta t) = \frac{1}{Z_c} v_1(t - \Delta t) - i_s(t - \Delta t) \quad (7)$$

$$I_r(t - \Delta t) = \frac{1}{Z_c} v_r(t - \Delta t) - i_r(t - \Delta t) \quad . \quad (8)$$

The disadvantage of this method is the discrete integration algorithm, which requires the past history of the network [26]. Moreover, the choice of the discrete simulation time step is crucial in order to get accurate results. The EMTP method gives only the sending end and receiving end values for the line current and voltage and intermediate points cannot be obtained unless the line is split appropriately [25].

Another time domain method, which mitigates the aforementioned problem, is the state-space transient analysis. It consists of the derivation of partial differential equations (PDEs) from the distributed line parameters and the conversion of these equations into a set of coupled ordinary differential equations (ODEs) by spatial discretization of the line [26]. Thus, all states of the system are accessible and a high spatial resolution can be achieved. The disadvantage of the state-space approach is the computationally expensive repeated inversion of the coefficient matrix.

The evaluation of the simulation approaches showed that the EMTP approach is the best choice for models consisting of transmission lines with distributed, frequency-dependent parameters and in which only the sending end and receiving end quantities are of interest. The state-space approach performs better than the EMTP approach in case of single frequency

TABLE I  
PROPERTIES OF THE ASSUMED 320 kV XLPE CABLE

Layer	Material	Outer Radius (mm)	Resistivity ( $\Omega\text{m}$ )	Rel. per-mittivity	Rel. per-meability
Core	Copper	21.4	$1.72 \cdot 10^{-8}$	1	1
Insulation	XLPE	45.9 <sup>1</sup>	-	2.3	1
Sheath	Lead	49.4	$2.2 \cdot 10^{-7}$	1	1
Insulation	XLPE	52.4	-	2.3	1
Aarmor	Steel	57.9	$1.8 \cdot 10^{-7}$	1	10
Insulation	PP	61.0	-	2.1	1

<sup>1</sup> Including inner and outer semi-conductor layer of 1.2 and 1.3 mm thickness, respectively

line models with cascaded Pi-sections, where the voltage and current distribution along the line is of interest and its values have to be accessible. The EMTP based frequency-dependent cable model has been selected for this study due to the best performance, most accurate results, and the fact that only the receiving end and sending end currents are required.

### B. Cable Model

The system is modeled in PSCAD-EMTDC and makes use of a detailed frequency-dependent, distributed-parameter cable model. The general design of the cable cross-section is derived from a real 150 kV XLPE VSC-HVDC submarine cable [27], [15]. The cross-section was scaled up to a 320 kV cable respecting the diameter of the copper conductor [28], while keeping the electric field stress (cold condition) similar. The material properties are based on values given in [29]. Table I summarizes the material properties and Fig. 4 illustrates the cable cross-section dimensions of all cable layers. The cable sheath is assumed to be grounded at each cable joint every approximately 900 m as in [30]. Simulations have shown that the sheath impedance in the aforementioned grounding scheme contributes only a negligibly small portion to the conductor current damping and the sheath is, therefore, mathematically eliminated in the simulations, i.e. assumed to have ground potential over the whole cable length.

The frequency-dependent cable model is the most accurate model that also accounts for the frequency dependence of the cable parameters, it is, however, computationally expensive and has no straightforward solution in the time domain. It is widely used in EMTP type simulations when accurate transient waveforms have to be computed. In this model, the cable is represented by the propagation function matrix  $\mathbf{H}$

$$\mathbf{H} = e^{-\sqrt{\mathbf{Z} \cdot \mathbf{Y}} \cdot l} \quad (9)$$

and the characteristic admittance matrix  $\mathbf{Y}_c$

$$\mathbf{Y}_c = \mathbf{Z}^{-1} \cdot \sqrt{\mathbf{Z} \cdot \mathbf{Y}} \quad (10)$$

that are calculated at discrete points in the frequency domain. These matrices are then approximated and replaced by low order rational functions through curve fitting methods [31].

### C. Converter and Network Model

The 3 terminal radial HVDC network shown in Fig. 5 is modeled in PSCAD using the EMTP approach. A pole-to-ground fault with a fault resistance  $R_f$  is applied at 100 km

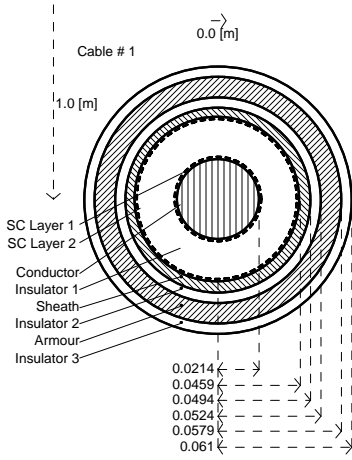


Fig. 4. Cable layers

TABLE II  
SYSTEM PARAMETERS

Parameter	Value
Rated Converter Power (Bipole)	800 MW
DC Voltage	$\pm 320$ kV
AC Voltage (L-L, RMS)	400 kV
X/R of AC Network	10
Transformer Leakage Reactance	0.1 p.u.
Converter Phase Reactor	0.05 p.u.
Total Resistance of Converter Diodes	0.1691 $\Omega$

away from terminal 1. The converters are modeled as a  $\pm 320$  kV bipolar two-level VSC topology with concentrated midpoint-grounded DC capacitors at each terminal as depicted in Fig. 6. However, the analysis of pole-to-ground faults presented in this paper would be equally valid for a system based on asymmetrical monopoles. The converter control protects the Insulated Gate Bipolar Transistor (IGBT) modules from overcurrents through blocking of the valves within a few  $\mu$ s making the half-bridge based VSC an uncontrolled rectifier [32]. Therefore, the converter model to be implemented for the transient study can be simplified.

The AC network adjacent to the converter terminal is modeled by its equivalent short-circuit impedance consisting of  $R_{AC}$  and  $L_{AC}$ , and a voltage source  $V_{AC}$ . The windings of the converter transformer have star configuration with grounded neutral on the high voltage side and delta configuration on the converter side. An additional phase reactor  $L_s$  is installed between converter bridge and transformer for harmonic filtering of the AC currents. The values of system parameters are summarized in Table II. The value for the converter losses during the AC infeed are determined by the on-state resistance  $R_D$  of the freewheeling diodes. The value for  $R_D$  is based on a series connection of 89 4500 kV/2000 A press-pack IGBTs [33]. Terminal 1 is operated in rectifier mode with a secondary winding voltage of the converter transformer of 237 kV and terminals 2 and 3 are operated as inverters with 213 kV at the AC side of the converter.

#### IV. RESULTS AND DISCUSSION

The simulations are performed in PSCAD using a time step of  $10 \mu$ s. The following paragraphs describe and discuss the

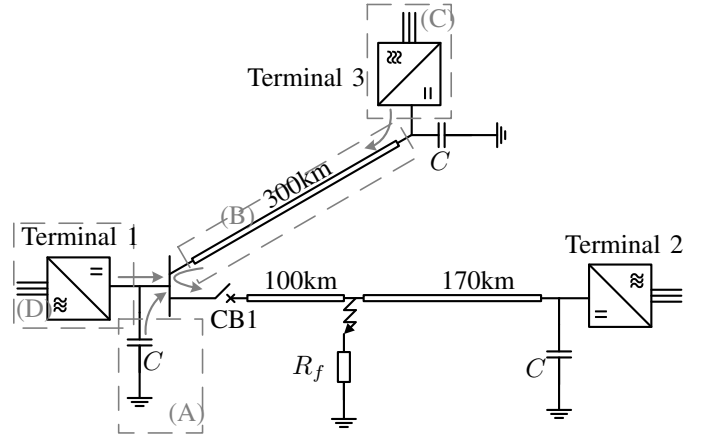
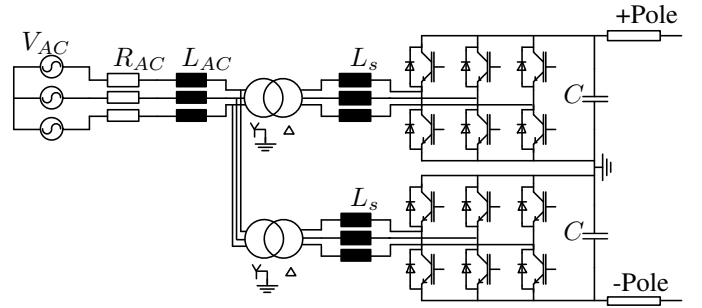


Fig. 5. Network layout with different fault feeding sources: (A) DC capacitor, (B) adjacent feeder cable, (C) AC infeed at terminal 3, (D) AC infeed at terminal 1

Fig. 6. Scheme of the converter model ( $V_{AC}$ : AC voltage,  $R_{AC}$ : AC resistance,  $L_{AC}$ : AC inductance,  $L_s$ : phase reactor,  $C$ : DC capacitor)

results of the simulation. First, the base case is presented and then the key parameters are varied to explain their influence on the fault current in the CB.

##### A. Base Case

The base case assumes a constant fault resistance  $R_f$  of  $7 \Omega$ , which corresponds to the ground resistance of a sparking ground connection in wet loamy sand at the current peak of 19.35 kA [16]. The dependence of the fault current on the fault resistance is neglected in all the simulations, as well as the sheath impedance, which might be present after the fault occurrence for a very short time. The default value of the DC capacitor is  $100 \mu$ F and the DC pole reactor is neglected in the base case. The Short Circuit Ratio (SCR) of the adjacent AC networks at the Point of Common Coupling (PCC) is assumed to be 10 for each terminal. The SCR is defined by the ratio of the short circuit capacity of the AC network at the PCC and the rated power of the converter as follows:

$$SCR = S_{PCC}^{sc} / S_{converter}^{rated} \quad (11)$$

The cables are initially at rest at 320 kV and no current is flowing. This simplification is justified by the negligible influence of the initial steady-state current on the transient peak current. Figures 7 and 8 illustrate the development of the fault current in the CB (solid line) and distinguish the different fault current contributors as labeled in Fig. 5: A) DC

capacitor, B) adjacent feeder cable, C) AC infeed at terminal 3, and D) AC infeed at terminal 1. As shown in Fig. 7, the fault appears at terminal 1 after a short delay (about 0.5 ms) given by the line length of 100 km between fault and terminal 1. The first peak corresponds to the discharge of the DC capacitor at the arrival of the negative voltage surge generated at the fault location. The subsequent peaks originate from the forward and backward traveling initial surge. After the second peak at around 2.5 ms, a sudden decrease of the CB current can be observed, which arises from a positive surge from terminal 2 transmitted through the fault.

The first 5 ms are dominated by the capacitive discharge current contributions as depicted in Fig. 8 (areas A) and B)), which gives an overview of the first 100 ms after fault occurrence. The surge propagates through the busbar into the neighboring feeder and its cable capacitance is discharged through the busbar into the faulted cable. Due to the distributed nature of the neighboring feeder capacitance, the cable is discharged gradually as the negative voltage surge propagates through the cable towards terminal 3. Note that the adjacent feeder contribution (area B in Figures 7 and 8) includes the contribution of the concentrated DC capacitor at terminal 3. The DC capacitor and the adjacent feeder cable capacitance are discharged simultaneously. The lumped DC capacitance is the dominant contributor during the first few milliseconds, whereas the cable capacitance contribution is larger afterwards due to its distributed nature.

After 10 ms, the capacitive discharge contributions fade out and a steady-state period dominated by the AC infeed at terminals 1 and 3 begins (c.f. areas C) and D)). The AC infeed starts as soon as the DC voltage drops below the voltage of the AC side of the converter and the freewheeling diodes become conducting. Current from the AC side is injected into the DC network through one or two diodes (depending on the phase of the AC voltages and the magnitude of the DC voltage) in the upper half and a return path is set up through the grounded filter midpoint and one or two diodes in the lower half of the 6-pulse bridge. This results in a phase-to-phase fault or two simultaneous phase-to-phase faults as seen from the AC side. The current contribution from the AC side rises slower compared to the capacitor discharge contributions as it is limited by the AC impedance.

All terminals connected to the busbar with the faulted feeder also contribute to the fault current in CB1. DC capacitor discharge and AC current feeding start once the voltage surge arrives at terminal 3. The reflected surge plus the discharge current and the AC current travel to terminal 1 and superpose the current in CB1 as depicted in Fig. 7 (area C). A higher delay for the AC infeed at terminal 3 as compared to terminal 1 can be observed due to the travel time of the initial negative voltage surge on the line between terminals 1 and 3 after having passed through the busbar, and the travel time back to terminal 1. Over the whole simulation period, the contribution from terminal 3 is smaller than the contribution from terminal 1, because of the long cable of 300 km and, consequently, higher attenuation.

After 30 ms, a 300 Hz ripple from the converter 6-pulse bridge is visible (c.f. Fig. 8). During this period, the cable

and filter capacitances are periodically charged and discharged. The charging of the capacitances (negative currents) is truncated in Figures 7 and 8, since it does not contribute to the CB current.

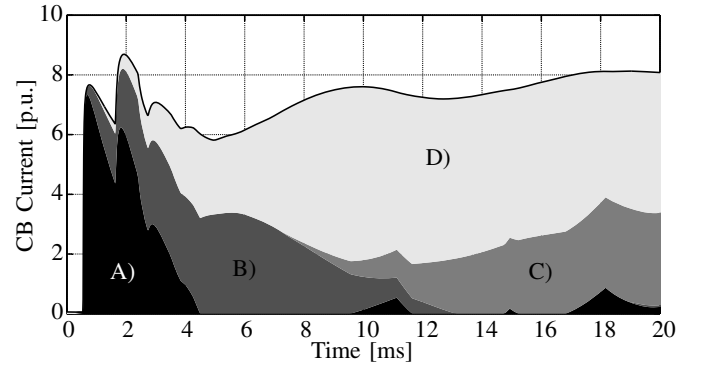


Fig. 7. Breaker current contributions, zoomed - A): DC capacitor, B): adjacent feeder cable, C): AC infeed at terminal 3, D): AC infeed at terminal 1, solid line: total CB current

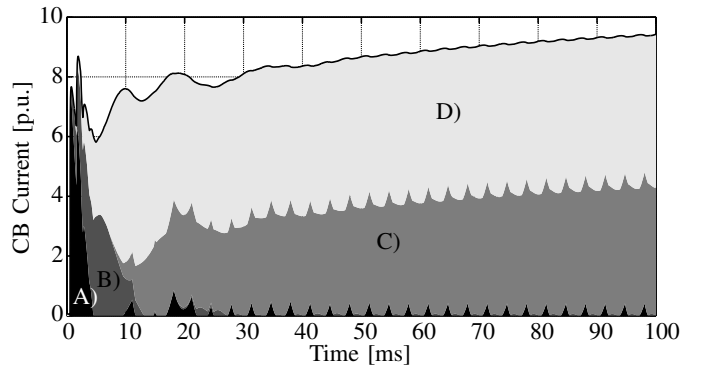


Fig. 8. Breaker current contributions - A): DC capacitor, B): adjacent feeder cable, C): AC infeed at terminal 3, D): AC infeed at terminal 1, solid line: total CB current

### B. Dependence of Fault Current on Fault Resistance

Fig. 9 illustrates the dependence of the maximum fault current in CB1 on the fault resistance. The maximum values within 5 ms of the CB current and its contributions from the individual components are given for certain values of the fault resistance. The other system parameters are kept equal to the base case. The short simulation period is chosen in order to account only for the initial discharge peaks with the highest  $di/dt$ . Depending on the SCR of the AC network, the CB current may increase up to much higher values at a later point in time. As can be seen in Fig. 9, low values for the fault resistance result in high peak currents during the first 5 ms after fault occurrence. This is due to the larger voltage drop initiated at the fault location given the lower fault resistance. The DC capacitor has the highest contribution amongst all fault current contributors for the whole range of fault resistance as the capacitor discharging is the dominant process during the first few milliseconds. Note that the adjacent feeder contribution in Fig. 9 includes the AC infeed at terminal 3,

which has a marginal share in this simulation. At very high values of fault resistance ( $> 50 \Omega$ ), the DC capacitor is the only contributor to the fault current in the CB (neglecting a minor contribution from the adjacent feeder) and the AC infeed contribution decreases to zero. To explain this fact, the time-to-peak-current has to be considered, i.e. which surge of the forward and backward traveling wave leads to the maximum current. As the DC capacitor discharge current after the first surge decreases rather slowly given the high DC capacitance in this simulation, the subsequent discharge current is superposed on the first one and depending on the magnitude of the second negative voltage surge, i.e. the fault resistance, the second discharge current peak might be higher than the first one. The magnitude of the second surge at terminal 1 depends on the reflection coefficient at the fault location and thus, on the fault resistance. For zero fault resistance, the reflection coefficient is  $-1$  (c.f. Equation (2) and Fig. 2) and, hence, the entire wave is reflected back to terminal 1, but with opposite sign. For very high fault resistances, the reflection coefficient tends to 0 and the surge is entirely transmitted through the fault towards terminal 2. Low fault impedances up to  $50 \Omega$  result in a high reflection coefficient and, thus, the second surge is responsible for the maximum current in the CB as indicated in Fig. 9. At this time, the current from the AC side has already increased and contributes a small share to the total CB current. During high impedance fault conditions ( $> 50 \Omega$ ), however, the first surge leads already to the maximum current in the CB. The AC infeed current has not increased yet due to the high AC inductance and the DC capacitor current is the only contributor to the CB current. Fig. 10 depicts the CB current waveforms for fault resistances of  $0.5$ ,  $20$ , and  $100 \Omega$  and illustrates the above stated.

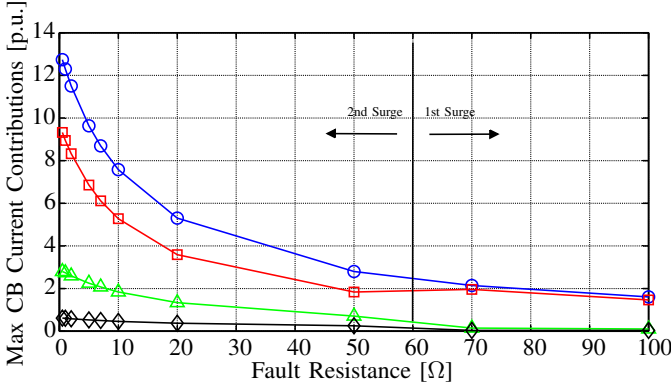


Fig. 9. Contributions from fault current sources to the maximum CB current within 5 ms;  $\circ$ : maximum CB current,  $\square$ : DC capacitor,  $\triangle$ : adjacent feeder,  $\diamond$ : AC infeed at terminal 1

### C. Influence of DC Capacitor on Fault Current

The maximum fault current in the CB increases almost linearly with the value of the DC capacitance as depicted in Fig. 11. For very low filter capacitances, such as in MMC topologies, only the AC infeed and the adjacent feeder contribute to the initial fault current in the CB. Note that the adjacent feeder contribution in Fig. 11 includes the AC infeed at terminal 3. As indicated in Figures 11 and 12 (left),

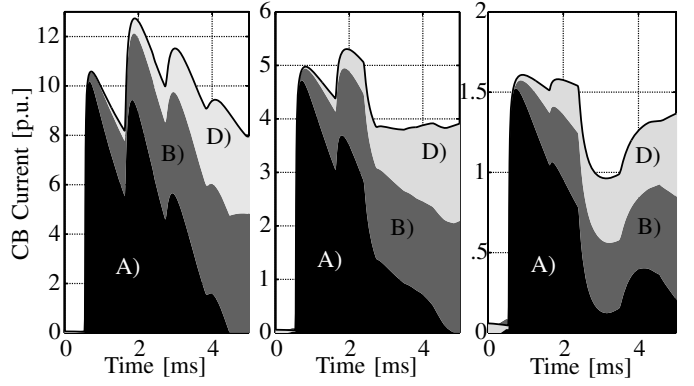


Fig. 10. Breaker current contributions for  $R_f = 0.5 \Omega$  (left),  $R_f = 20 \Omega$  (center),  $R_f = 100 \Omega$  (right) - A): DC capacitor, B): adjacent feeder cable, C): AC infeed at terminal 3, D): AC infeed at terminal 1; Note the different current scales on the y-axis

the time-to-peak-current is higher than in converter topologies with large DC capacitors and corresponds approximately to the fourth surge at  $t = 7\tau$ , where  $\tau$  corresponds to the travel time on the cable from the fault to terminal 1. For DC capacitances above  $7 \mu\text{F}$ , the first surge leads to the maximum current in the CB and, hence, the capacitor has the largest share on the total current as shown in Fig. 12 (center). For even higher values above  $50 \mu\text{F}$ , the second negative voltage surge at  $t = 3\tau$  produces the maximum current and, consequently, the contribution from the AC infeed is higher compared to DC capacitors with  $10 - 20 \mu\text{F}$ . In general, the second negative voltage surge is responsible for the maximum current in case of high values of the DC capacitance, because the second capacitor discharge peak is superposed on the still high first discharge current given the increased capacitor time constant (c.f. Fig. 12, right).

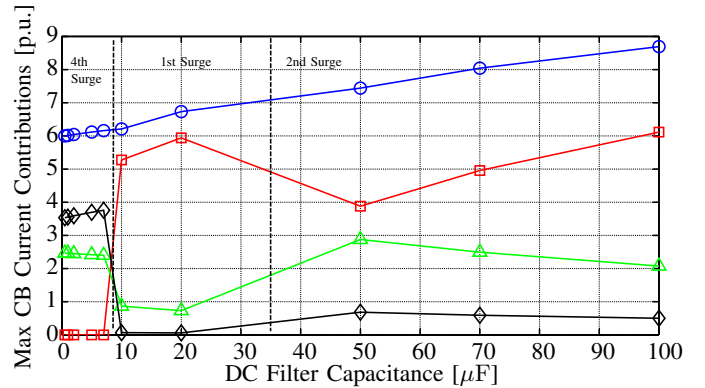


Fig. 11. Contributions from fault current sources to the maximum CB current within 5 ms;  $\circ$ : maximum CB current,  $\square$ : DC capacitor,  $\triangle$ : adjacent feeder,  $\diamond$ : AC infeed at terminal 1

### D. Influence of AC Short Circuit Capacity

As shown in Fig. 13, a variation of the SCR at the PCC has no influence on the first peaks within 5 ms, as they are exclusively originated in the discharge of the DC capacitor and cable capacitance. A higher SCR, however, results in a higher steady-state fault current of up to 12 p.u. in case of a strong AC network with a SCR of 20.

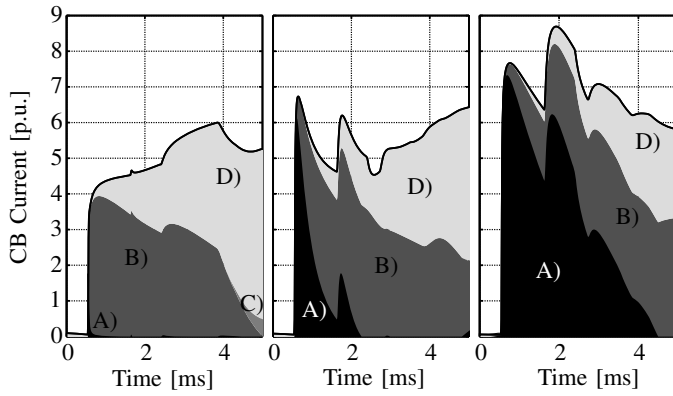


Fig. 12. Breaker current contributions for  $C_{\text{filter}} = 0.5 \mu\text{F}$  (left),  $C_{\text{filter}} = 20 \mu\text{F}$  (center),  $C_{\text{filter}} = 100 \mu\text{F}$  (right) - A): DC capacitor, B): adjacent feeder cable, C): AC infeed at terminal 3, D): AC infeed at terminal 1

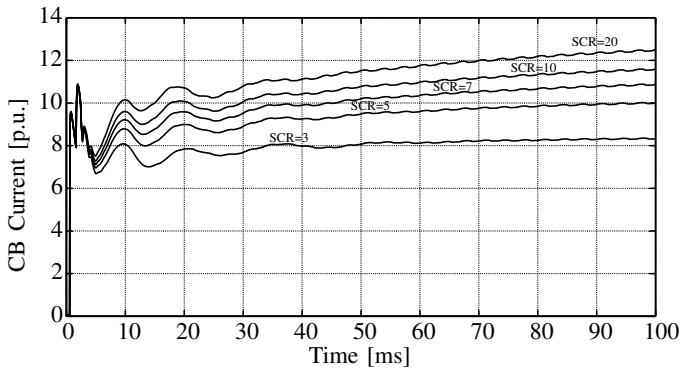


Fig. 13. Influence of the SCR at the PCC on the development of the fault current in the DC CB

#### E. Influence of Neighboring Feeder Length

The length of the neighboring feeder at the busbar of terminal 1 determines the delay of the contribution of terminal 3 to the CB current. It also has an impact on the duration of the cable capacitance discharge. The longer the cable is, the later the contribution from terminal 3 appears and the longer the cable capacitance discharge into the fault lasts, which depends on the travel time of the surge. The cable discharge starts as the forward traveling negative voltage surge penetrates into the feeder via busbar and ceases after twice the travel time on the cable between terminals 1 and 3, when the positive backward traveling voltage surge arrives again at terminal 1.

#### F. Influence of DC Pole Reactor

DC pole reactors serve multiple purposes such as DC current filter or Fault Current Limiter (FCL) in series with the CB. The latter is needed to limit the rate of rise of the fault current in hybrid HVDC CBs, such that the current does not exceed the CB's maximum breaking current capability within the breaking time. For a maximum rise of the fault current of  $3.5 \text{ kA/ms}$  in a  $320 \text{ kV}$  MTDC with 10% overvoltage, a  $100 \text{ mH}$  DC pole reactor is required [34]. Fig. 14 illustrates the influence of the pole reactor  $L_r$  on the CB current development within the first 10 ms after fault occurrence for various reactor sizes. A higher inductance reduces considerably the rate of

rise of the current during the capacitive discharge dominated period. The peak of the prospective CB current within the considered time frame is reduced and delayed. A larger DC reactor also reduces the steady-state fault current level, increases, however, the systems time constant and deteriorates the performance of the converter control.

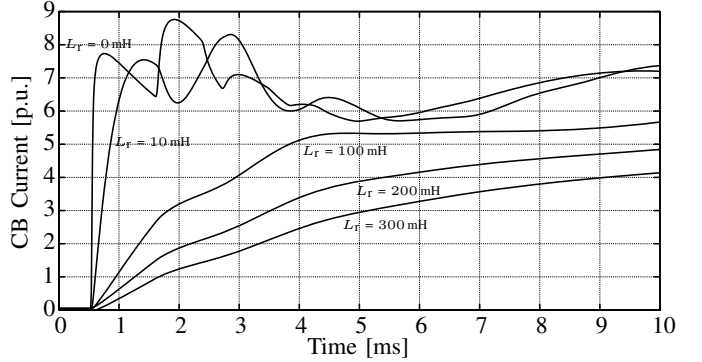


Fig. 14. Influence of the DC pole reactor  $L_r$  on the development of the fault current in the DC CB

### V. CONCLUSIONS

This paper has illustrated the contribution from each network component to the fault current in a DC CB and has explained their dependencies on the network parameters. Simulations have been performed in a simple, radial HVDC network using PSCAD. The results have shown that filter and cable capacitance discharges are dominant during the first 10 ms, whereas the AC infeed contributions from terminal 1 and 3 are exclusively present after 10 ms. Measures to reduce the first peaks from capacitive discharges are: the reduction of the DC capacitors' size (including filter capacitors), i.e. change of the converter topology, the limitation of the number of feeders per busbar to reduce the cable contributions to the CB fault current, and the increase of the pole reactor size to limit the rate of rise of the discharge current. In order to reduce the maximum CB current during the later AC infeed dominated period, the converter topology has to be changed to a full-bridge configuration that allows the control of the AC infeed, but does not isolate the faulty cable branch in a MTDC network. Alternatively, the phase reactor between the converter and the transformer has to be increased to reduce the rate of rise of the AC infeed and the number of DC feeders per busbar has to be limited to reduce the contributions from the AC side at remote terminals.

Converter topologies with low DC capacitor requirements are favorably in terms of maximum CB current and time-to-peak within 5 ms, but still have the disadvantage of high contributions from the AC infeed after several tens of milliseconds and, thus, high CB currents that have to be interrupted. The rate of rise of the CB current is comparable to converter topologies with large DC capacitors due to the similar behavior of the distributed cable capacitance. This capacitance of neighboring feeder cables is crucial. The higher the number of feeders at the same bus, the higher the capacitance discharge contribution during the first period.

Foreseeable DC CBs will require additional fault clearance support, such as FCLs, e.g. inductance in series with the CB.

To estimate the minimum CB requirements ( $di/dt$  and peak current), zero DC capacitance has to be assumed and the initial discharge current from adjacent feeders has to be calculated.

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