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Fabrication of High-Resolution, Self-Aligned Palladium Electrodes

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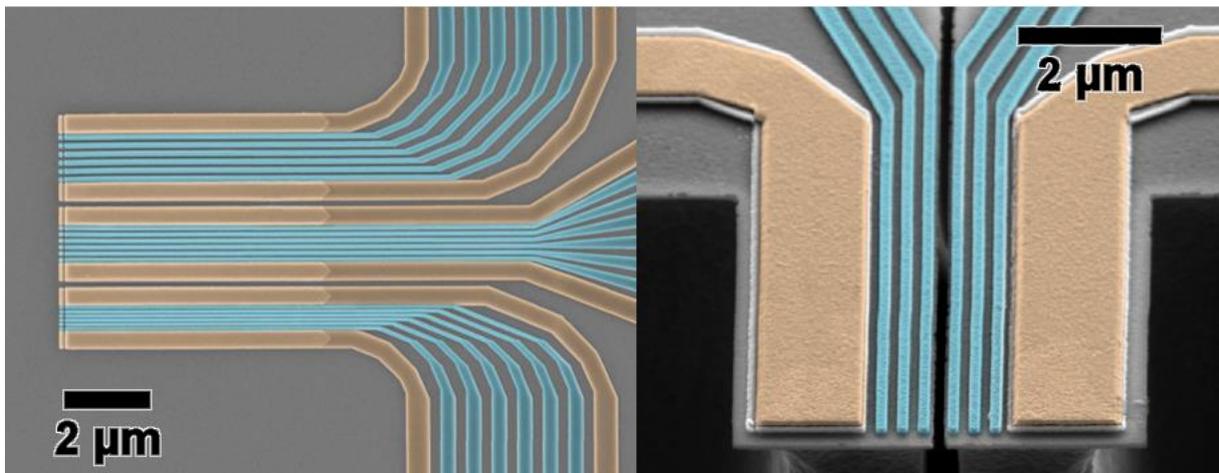
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Abstract

Here, a fabrication approach is presented, which allows for the patterning of vertically displaced, high density and high resolution palladium electrodes in a single processing step. A top down method, namely ion milling, was used to transfer the e-beam lithography pattern into the palladium. Hereby hydrogen silsesquioxane (HSQ) was used as a hard mask. Other than the conventionally used lift-off based approach, this method does not restrict the line height to spacing ratio and therefore permits the fabrication of very densely spaced electrodes. Specifically, electrodes with as little as 25 nm spacing were obtained, although only lines with spacings of 80 nm or more were electrically isolated without any further processing. By adjusting the tilting angle and the HSQ to Pd thickness the cross-sectional profile can be controlled and varied from triangular (30° side-wall slope at 10° tilt) to rectangular (30° tilt). This can be used to its advantage in order to reduce the parasitic capacitance of adjacent lines for a given pitch. Additionally, a proximity effect was observed as the decrease of spacing of electrodes was correlated with an increase in side-wall verticality. In summary, we have demonstrated a robust process to pattern perfectly aligned electrodes on complex topographical substrates. The here presented method is characterized by a high degree of scalability and also high flexibility in terms of materials selection.

Graphical Abstract



Highlights

- Fabrication of high density, vertically displaced electrodes with no misalignment due to simultaneous etching on a pre-patterned substrate
- The cross-sectional profile of the electrodes can be varied from triangular all the way to rectangular by adjusting the HSQ to palladium height ratio, the sample tilt and the over-etching degree.
- The observed proximity effect allows for patterning of very closely spaced electrodes at low tilting angles during ion milling

Keywords

self-aligned; palladium; ion milling; multi-gate

1. Introduction

Palladium (Pd) is known to form excellent contacts with low-dimensional carbon materials, in particular with single-walled carbon nanotubes (SWNTs). Specifically, favorable wetting properties and a high on-off current ratio have previously been observed [1]. Simultaneously palladium is difficult to chemically dry etch [2,3], therefore the choice of fabrication methods for nanostructures is primarily limited to lift-off and physical etching.

Here, we present an ion milling based approach to pattern densely spaced high-resolution source, drain and gate electrodes in a single step on a pre-patterned substrate. Unlike lift-off based processes this approach does not limit the spacing between adjacent electrodes with respect to the desired line height.

These vertically displaced electrodes can then later be used to transfer a carbon nanotube (CNT) from

a separate growth substrate on top, in order to create functional devices [4–6].

For suspended CNT devices in field-effect-transistor (FET) architecture (see Figure 1.a) scaling down the gate dimensions and electrode spacings allows for the fabrication of ultra-short channel devices, but also enables the packing of multiple gate electrodes between the source and drain (see Figure 1.b). These structures can be used for local actuation and sensing [5]. Hereby quantum-effects can be studied [5,7,8] and also, in case of resonant devices, mode coupling [9,10] can be investigated. Using a one-step process in comparison to a conventional 2-step process means that the exact relative location of the electrodes is well defined (see Figure 1.c). This permits a further decrease in spacing between adjacent electrodes.

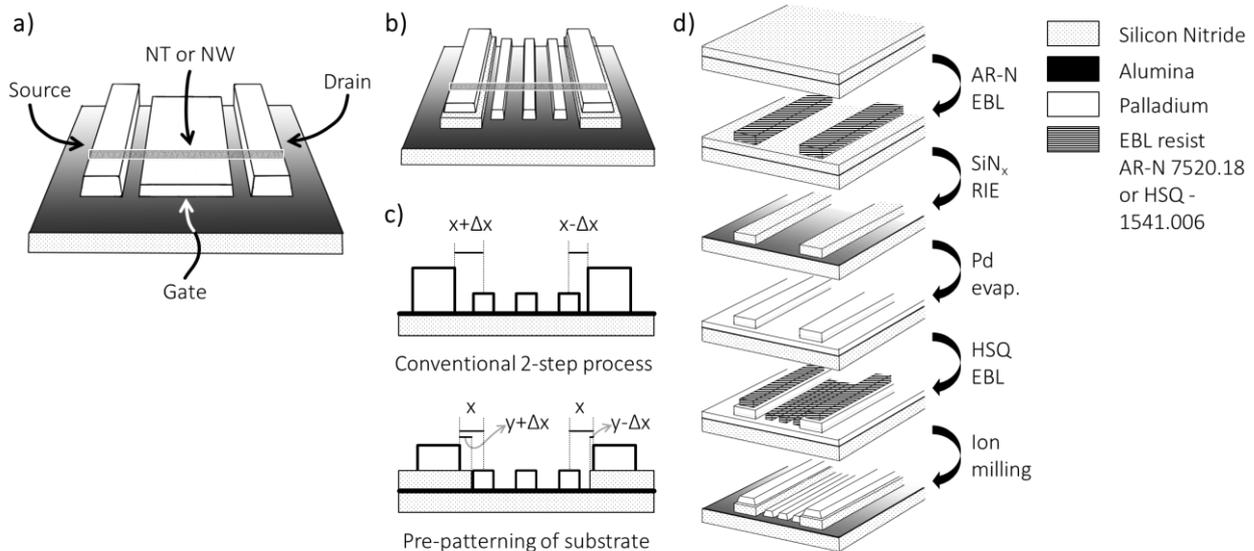


Fig. 1. a) A typical nanoresonator design. b) CNT on a multi-gate structure. c) By choosing to pattern electrodes on a pre-patterned substrate rather than using a conventional two-step process the misalignment is shifted to between the electrodes and substrate rather than the electrodes themselves. d) Fabrication steps for the here demonstrated structures.

2. Materials and methods

A layer stack of 200 nm plasma-enhanced chemical vapor deposited SiN_x (PECVD, at 300°C , 120 sccm SiH_4 + 1000 sccm N_2), 2 nm atomic layer deposited Al_2O_3 (ALD, at 250°C), 100 nm PECVD SiN_x was precipitated onto a Si (100) wafer and annealed in a rapid thermal annealing system (AS One 150) at 850°C . This results in an increased

wet-etch resistance of the nitride layers [11] and the recrystallization of the alumina layer. For ALD alumina the transition to α -alumina has been observed at temperatures as low as 750°C [12]. In comparison to amorphous alumina, α -alumina is compatible to hydrofluoric acid (HF) as well as vapor HF [3,13]. This is required here for a release step of suspended Si-structures at a later stage. This layer stack was patterned (see Figure 1.d)

using a negative e-beam resist (AR-N 7520.18, 400 nm, e-beam tool: Vistec EBPG 5200+ at 100 kV). A CHF_3 based RIE process was used to pattern the SiN_x layer with the alumina as an etch stop.

Onto this pre-patterned substrate 2 nm chromium and 73 nm palladium were evaporated. Next, a 20 nm layer of SiO_2 was deposited using a PECVD process (300°C, 150 sccm SiH_4 + 710 sccm N_2O) to improve the surface adhesion of hydrogen silsesquioxane (HSQ, XR-1541.006), which was used as the high-resolution e-beam resist. After e-beam writing and development (with AZ351B) the layer was ion milled (Oxford Ionfab 300, ion currents of 250 to 500 mA, acceleration voltage of 350-500 V, at a processing pressure of $7 \cdot 10^{-5}$ Torr and a platen temperature of 5°C), while using secondary ion mass spectroscopy (SIMS) to detect when the end of the process was reached. Palladium is highly chemically stable. In particular in fluorine based plasmas a Pd-F film evolves, which is even more chemically stable than bulk Pd [2]. Chemical etching of palladium in chlorine plasmas is as of yet unreported. As a result it can only be effectively etched by sputtering [3]. HSQ was chosen for ion milling due to its low etch rate in comparison to Pd, its high resolution and low line roughness [3,14].

The structures were analyzed electrically (resistance and leakage current measurements) and by scanning electron microscopy (SEM).

3. Results and Discussion

The primary focus here was on the quality of the pattern transfer, the limitations in terms of half-pitch relative to the electrode height and width and the overall constraints put on the process by the overlay mismatch of the e-beam writing.

For the pre-patterning of the insulating layer precise control of the step height between the gate electrode and the source/drain electrode level was essential. Therefore a 2 nm Al_2O_3 etch stop was employed. 2 nm of alumina proved to be enough to withstand over-etching (etch rate of alumina 0.95 nm/min, silicon nitride: 30.5 nm/min). Slight over-etching was necessary in order to compensate for micro- or macro-loading effects [15].

After palladium deposition a smooth step coverage was observed within the transition region, which is

of importance in order to be able to spin the HSQ uniformly for the following processing steps.

For the pattern transfer of the HSQ lines into the palladium layer, it was observed that a high degree of profile control could be obtained by adjusting the ratio of palladium to HSQ thickness and choosing the tilting angle accordingly. The theoretical etch rate of palladium to HSQ is around 1:1 (Pd etch rate ~ 20 nm/min at 250 mA, 10° tilt β , see Figure 2) [3]. In reality, an etch rate much closer to 1:2 was observed, which is due to the faster propagation of the etch-front in the facets that develop rather than in perpendicular direction to the surface.

The etching of the HSQ hard mask and the palladium follow different trends primarily because their etch products display significantly different levels of redeposition. HSQ is chemically identical to polycrystalline SiO_2 , with some structural defects and residual Si-H bonds. For most materials the sputter yield, whilst neglecting any redeposition, follows a similar trend with a maximum sputter yield at approximately 75° (relative to the vertical) [16]. This is a result of only the re-sputtered atoms close to the surface in the interaction volume being able to escape. Therefore at high tilting angles (β) the highest degree of material removal is observed [17]. As the interaction volume mainly depends on the kinetic energy of the ions and the density of the target material, the acceleration voltage is the most important parameter. With decreasing voltage the maximum sputter yield shifts to lower tilting angles, although a significant change can only be observed at very low energies. [16–18]

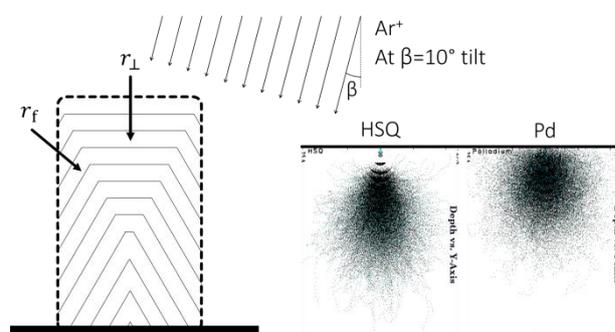


Fig. 2. Facet development due to angle dependent sputter yield ($r_f > r_{\perp}$) during etching of HSQ and TRIM simulations of the interaction volume of 500eV Ar ions with HSQ and Pd.

Therefore, when a HSQ line is being ion etched and the corners are not perfectly rectangular, which is in effect always the case, a facet develops very quickly. This facet is therefore finally dominating the resist edge shape (see Figure 2). For amorphous SiO₂ layers a maximum sputter yield at tilting angles between 50°-60° has been previously reported [19].

At a 10° substrate tilt (β) during ion milling, a dominant facet with a 29.5° angle was observed for HSQ and the calculated etch rate ratio normal to the corresponding surface was 0.36 (r_{\perp}): 0.64 (r_{\parallel}).

Depending on the Pd:HSQ height ratio and the degree of over-etching the HSQ facet can be either completely or not at all transferred into the Pd layer [18]. For a full transfer perfectly triangular electrodes could be observed (see Figure 3). If the facet was not transferred, depending on the tilting angle, trapezoidal to rectangular cross-sections were obtained. All other conditions resulted in polygonal cross-sections.

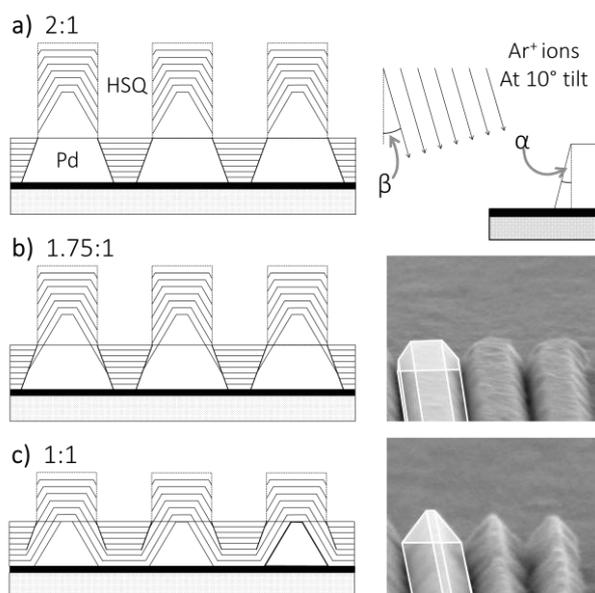


Fig. 3. Different cross-sectional profiles resulting from Pd: HSQ thickness ratio ranging from 2:1 to 1:1.

When no transfer takes place, the sidewall angle (α) of the palladium electrodes can be adjusted between 0° to 30° (see Figure 4), as this angle corresponds to the tilt with the maximum sputter yield. A slight broadening of the lines occurs due to an initial crown formation [18]. If the etching is terminated exactly when the facet reaches the Pd interface no residual crowns are observed after

stripping the HSQ. Above 30° (β), with a thick HSQ layer, the bottoms of the trenches cannot be efficiently sputtered anymore due to excessive shadowing.

Whilst side wall angles (α) of up to 30° could be observed, further flexibility can be obtained by significantly reducing the acceleration voltage. For lower ion energies, the maximum sputter yield is observed at lower angles (β) and also more isotropic sputtering is expected, which indicates that the evolving facets in the HSQ layer should propagate much slower [16].

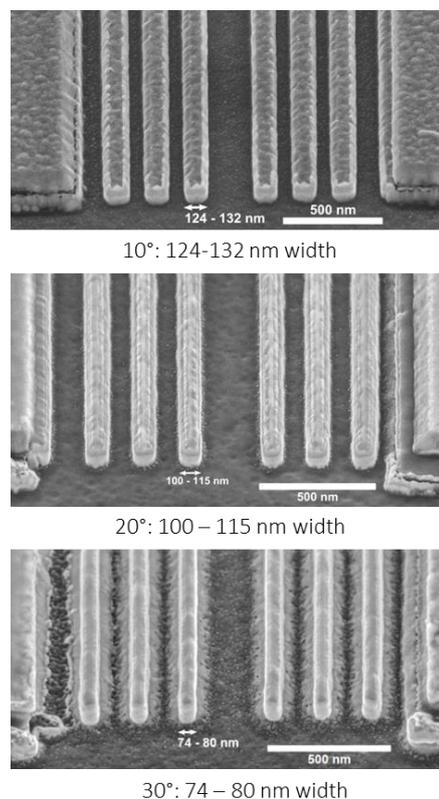


Fig. 4. The result of changing the tilting degree (β) from 10° to 30°. The initial line width was 50 nm, the spacing 150 nm.

Interestingly, for very narrowly spaced electrodes a proximity effect was observed at etching with a 10° tilt (β , see Figure 5). For those lines the side-wall verticality increased with decreasing line spacing. This, most likely, is a result of the locally reduced generation of re-sputtered moieties. A fit with the exposed volume normalized by the total volume between the HSQ lines yields a satisfactory correlation of 0.88 given the small sample size. In other words, electrodes can be spaced much closer than initially anticipated, while still remaining

spatially separated. At such small distances electrical insulation is not necessarily guaranteed, as very small Pd islands may nucleate in areas with low sputter yields. To circumvent this problem, the use of a thicker chromium adhesion layer is suggested. This layer can subsequently be wet etched in order to remove any residual Cr islands. Above a line spacing of 80 nm no leakage currents were observed. In this case this corresponds to a line width : line height : half-pitch ratio of 1 : 0.6 : 1.2 (e.g. line width of 120 nm with a half-pitch of 100 nm in a 75 nm palladium layer).

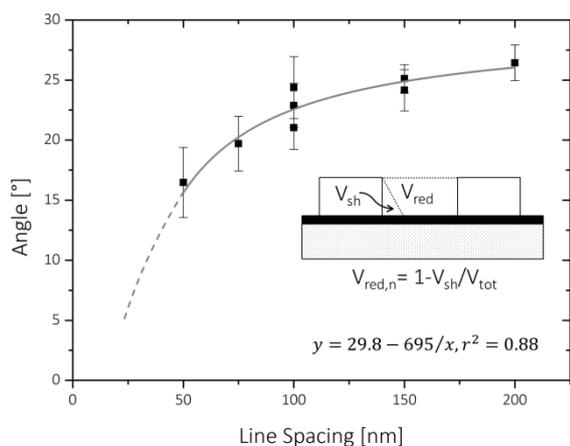


Fig. 5. For smaller spacings, much steeper side-wall angles (α) were observed under identical etching conditions at 10° tilt (β). V_{sh} is the shadowed volume, V_{tot} the total and V_{red} the reduced volume. $V_{red,n}$ is the normalized V_{red} .

At a given pitch and set footprint, the fabrication of electrodes with a specific side-wall angle (α) can be used to its advantage in order to reduce the parasitic capacitance between adjacent lines as long as the volume reduction is insignificant for the desired application.

When looking at the combination of these two process steps (see Figure 6) it becomes apparent that the process is ultimately not limited by the resolution of the e-beam resists, but rather by the overlay mismatch between the two writing steps. With an e-beam exposure overlay mismatch of less than 15 nm (as specified by the manufacturer) line spacings of 30 nm should be feasible without inducing any misalignment.

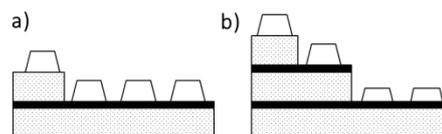
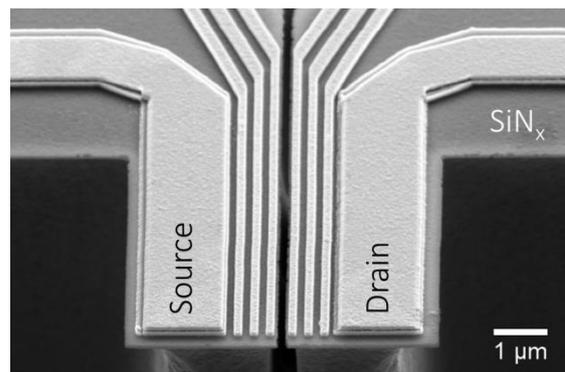


Fig. 6. The end result of the combined process with the cross-section as shown in a). Also more complex profiles with different layer heights such as in b) can be fabricated.

While very thin lines with low line edge roughness can also be fabricated using lift-off, limitations apply in terms of line height and line spacing. By choosing a top-down process in particular, the line spacing can be greatly reduced. Additionally, this process is not only compatible with line-of-sight deposition methods but also with conformal chemical vapor deposition (CVD) methods. One such process of interest here is ALD, as it can yield palladium layers with a very well defined height and low roughness. ALD Pd layers are characterized by a very low percolation threshold of less than 4 nm [20]. As the minimum pitch to width ratio is expected to scale proportionally with the reduced height, very small features can potentially be fabricated, down to the resolution limit of the e-beam resist. For HSQ it has been demonstrated that lines of 10 nm can be resolved [21].

Here, a relatively simple topographical structure was desired, but this process is compatible with pre-patterned substrates with a much more complex topography, including multiple levels and materials, as long as the height profile is within the depth of field of the e-beam tool (see Figure 6.b). Direct e-beam writers are characterized by a very high depth of focus of multiple micrometers. Theoretically, layers of different heights can also be patterned simultaneously, while still not inducing any mismatch between the electrodes. Here the alumina layer, which etches much slower than

palladium (2.5 nm/min vs. 20 nm/min etch rate) can be used to compensate for over-etching.

4. Conclusions

We have shown a robust process to fabricate self-aligned electrodes by combining ion milling of palladium with a pre-patterned substrate. Electrodes with a half-pitch of 100 nm and a height of 75 nm were successfully fabricated. It was observed that for small resist height the obtained electrode profile is strongly determined by faceting effects, while for thicker resists, the sidewall angle can be adjusted within 0°-30°. Additionally, the observed proximity effects should allow patterning of very closely spaced lines, if the other etching parameters are chosen correctly. Under standard e-beam operation, lines with separation as low as 30 nm can potentially be fabricated without inducing any mismatch.

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