Optimizations of epilayer structure design and fabrication process on INP/GAASSB double heterojunction bipolar transistors

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OPTIMIZATIONS OF EPI LAYER STRUCTURE DESIGN AND FABRICATION PROCESS ON INP/GAASSB DOUBLE HETEROJUNCTION BIPOLAR TRANSISTORS

A dissertation submitted to
ETH ZURICH

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2011
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Abstract

InP/GaAsSb double heterojunction bipolar transistors (DHBTs) have been first developed for long-talk time wireless applications. Rapidly the development of these devices shifted to the realization of ultrahigh-speed devices intended for digital circuits in optical fiber communication and test equipment applications. Compared to other material systems used for HBTs, the type-II band alignment between the GaAsSb base and InP collector offers an energy launcher for the electrons and avoids the current blocking effect. Moreover, the large valence band offset between the ternary alloy GaAsSb and the InP emitter provides an efficient confinement for the base holes preventing the hole back injection into the emitter.

This thesis focuses on the development of the epilayer structure and the fabrication process in order to improve the DC and RF performances in InP/GaAsSb DHBTs. The impact of the collector, base and emitter layer compositions and doping concentrations on the DC and RF device characteristics has been studied in detail.

In different epilayers composing the DHBT, a grading in composition and doping has been introduced to further improve the device performance. The compositional and doping graded base introduces a quasi-electric field which accelerates the electrons, reducing the base transit time. The GaInP/InP compositional grading in the emitter has been chosen to avoid the energy barrier for the electrons at the emitter/base junction, while an GaInAs compositional grading in the emitter cap layer should provide a lower contact resistivity. The epilayer thickness of the collector has been chosen to reduce both the electron transit time and the base/collector capacitance.

The fabrication process optimization has been carried out by means of the emitter undercut reduction, the base undercut maximization and a minimization of the contact resistivity. The surface treatment applied before the contact metal deposition is of pivotal importance in order to minimize the contact resistivity. The emitter undercut has been realized with a combination of chemical wet- and dry-etching. The base undercut has been performed by an aggressive base undercut etching in order to reduce the extrinsic base/collector capacitance.
The optimized epilayer structure and fabrication process allows achieving a current-gain cutoff frequency \( (f_T) \) of 475 GHz with the emitter area of \( 0.4 \times 8.4 \, \mu \text{m}^2 \). A balanced \( f_T \) and maximum oscillation frequency \( (f_{\text{MAX}}) \) of 388 and 351 GHz have been simultaneously achieved from DHBTs with an emitter area of \( 0.6 \times 11.5 \, \mu \text{m}^2 \) and a collector thickness of 125 nm. DHBTs with an emitter area of \( 0.3 \times 3.4 \, \mu \text{m}^2 \) exhibit simultaneously an \( f_T \) and \( f_{\text{MAX}} \) of 400 and 322 GHz, and a minimum noise figure of 1.2 dB at 20 GHz, which is the best noise performance ever reported for III-V HBTs.
Zusammenfassung

InP/GaAsSb Doppelheteroübergang bipolaren Transistoren (DHBTs) wurden ursprünglich für drahtlose Funkanwendungen mit langer Sprechzeit entwickelt. Schnell verschob sich der Entwicklungsschwerpunkt dieser Bauelemente, hin zur Realisierung von Ultrahochgeschwindigkeitsbaulemenenten für digitale Schaltungen für Anwendungen in faseroptischer Kommunikation und Testgeräten. Im Vergleich zu anderen Materialsystemen für HBTs bietet die Typ-II Bandausrichtung zwischen der GaAsSb Basis und dem InP Kollektor eine Energiestartrampe für Elektronen und vermeidet den Stromblockadenefekt. Ausserdem bietet der grosse Valenzbandversatz der ternären GaAsSb Legierung und des InP Emitters eine effiziente Konfination für die Löcher der Basis und verhindert damit die Rückinjektion der Löcher in den Emitter.

Diese Arbeit fokussiert sich auf die Entwicklung der epitaktischen Strukturen und des Fabrikationsprozesses um die DC und HF Leistungsfähigkeit von InP/GaAsSb DHBTs zu verbessern. Der Einfluss der Kollektor, Basis und Emitterzusammensetzung und der Dotierkonzentrationen auf die DC und HF Bauteilcharakteristik wurden im Detail untersucht.

In den verschiedenen Epitaxieschichten der HBTs wurde ausserdem ein Gradient der Zusammensetzung und der Dotierung eingeführt um die Bauteilleistungsfähigkeit weiter zu verbessern. Der Gradient der Zusammensetzung und Dotierung in der Basis führt zu einem quasi elektrischen Feld, welches die Elektronen beschleunigt und damit die Basistransitzeit verringert. Der Emitter mit dem GaInP/InP Gradientenprofil der Zusammensetzung wurde gewählt um die Energiebarriere beim Emitter-Basis Übergang für Elektronen zu vermeiden, während eine in der GaInAs Zusammensetzung varierende Emitter Deckschicht für einen geringen Kontaktwiderstand sorgt. Die epitaktische Schichtdicke des Kollektors wurde so gewählt, dass sowohl die Elektronentransitzeit als auch die Basis/Kollektor Kapazität verringert wurde.

Die optimierte epitaktische Schicht und der optimierte Fabrikationsprozess ermöglichen es eine Stromverstärkungsgrenzfrequenz \( (f_T) \) von 475 GHz mit einer Emitterfläche von \( 0.4 \times 8.4 \, \mu m^2 \) zu erreichen. Eine ausgewogene Stromverstärkungsgrenzfrequenz und maximale Oszillationsfrequenz \( (f_{MAX}) \) von 388 und 351 GHz wurden simultan für einen DHBT mit einer Emitterfläche von \( 0.6 \times 11.5 \, \mu m^2 \) und einer Kollektordicke von 125 nm erreicht. DHBTs mit einer Emitterfläche von \( 0.3 \times 3.4 \, \mu m^2 \) weisen ein simultanes \( f_T \) und \( f_{MAX} \) von 400 und 322 GHz und eine minimale Rauschzahl von 1.2 dB bei 20 GHz auf, welches die beste jemals veröffentlichte minimale Rauschzahl für III-V HBTs darstellt.
In this Chapter, the fundamental operating principle of bipolar junction transistors is described. The performances of InP/GaAsSb double heterojunction bipolar transistors (DHBTs) are compared with those of other HBTs, and their advantages and disadvantages are discussed. The state-of-the-art for $f_T$, $f_{MAX}$, breakdown voltage, minimum noise figure for InP HBTs is summarized. Finally, the motivations for this work and the approaches chosen are presented.
1.1 Basic Operation Principle

A bipolar junction transistor (BJT) is a three-terminal electronic device conceptually consisting of three main layers: the emitter, the base and the collector. For an npn transistor, electrons are injected from the emitter through the base, to the collector. The emitter and collector layers are doped n-type, whereas the base layer is doped p-type.

In a typical operation condition, the base/emitter junction is forward biased while the base/collector junction is reverse-biased. When the base/emitter junction is forward biased, the thermal equilibrium is broken, allowing the electron injection from the emitter/base interface into the base region. According to the junction law, the electron density at the base side of the emitter/base junction increases exponentially with the applied base/emitter bias. A major part of the electrons diffuses through the base in the presence of the reverse bias at the base/collector junction. In a well designed transistor, a small fraction of the injected electrons recombines with the holes which are the majority carriers in the p-type base material.

![Band diagram of transistors with emitter/base homojunction and heterojunction (simulated with Simwindows) at thermal equilibrium condition.](image)

Figure 1.1 Band diagram of transistors with emitter/base homojunction and heterojunction (simulated with Simwindows) at thermal equilibrium condition.
Figure 1.1 depicts the energy band diagram of transistors with emitter/base homo-
junction and hetero-junction based on GaAs material system simulated with
Simwindows program. AlGaAs is used as the emitter material to realize the
emitter/base heterojunction. Transistors with an AlGaAs emitter exhibit a higher
energy barrier for holes and will thus show an improved DC current gain.

1.2 Brief Review of HBTs

One goal of $npn$ transistor design is to maximize the electron current while
simultaneously minimizing the hole current, and thus increasing the current gain. For
bipolar junction transistors, this can be achieved by providing a much higher doping
level in the emitter than in the base. This however, increases base resistance and thus
degrades the transistor maximum oscillation frequency $f_{\text{MAX}}$. H. Kroemer [1]
proposed a wide band-gap emitter material to increase the emitter injection efficiency
and thus the current-gain by exploiting the valence band discontinuity which provides
an efficient confinement for holes in the base. This exemplifies one of the main
advantages of heterojunction bipolar transistors over BJTs.

Some material systems used for heterojunction bipolar transistors are AlGaAs/GaAs,
GaInP/GaAs, InP/GaInAs, InP/GaAsSb, Si/SiGe. The AlGaAs/GaAs material system
for HBTs requires a compositional grading at the emitter/base interface in order to
eliminate the large conduction band discontinuity $\Delta E_C$ of 0.3 eV between the
$\text{Al}_{0.28}\text{Ga}_{0.72}\text{As}$ emitter and the GaAs base [2]. The low valence band discontinuity $\Delta E_V$
of 0.053 eV between the GaAs base and the AlGaAs emitter is not sufficient to build
an efficient hole confinement [2]. In addition, there is no etching solution that
removes the AlGaAs emitter without attacking the underlying GaAs base; Aluminum
is extremely reactive and background impurities are likely to be incorporated into the
AlGaAs layers during growth, thereby leading to a high density of traps.

As an alternative material, lattice-matched Ga$_{0.5}$In$_{0.5}$P material offers a lower $\Delta E_C$
(0.16 eV) [2], a higher $\Delta E_V$ (0.29 eV) [2] as well as an improved device reliability
compared to AlGaAs [3]. The lower $\Delta E_C$ between the Ga$_{0.5}$In$_{0.5}$P emitter and the
GaAs base avoids the ballistic launching ramp when the electrons travel from the
emitter into the base; Ga$_{0.5}$In$_{0.5}$P/GaAs HBTs also feature a higher valence band
discontinuity $\Delta E_V$ which confines holes in the base material [2]. Additionally, the etching solutions for the GaInP emitter are selective and do not attack the GaAs base.

Table 1.1 lists selected physical properties (such as the band gap, electron mobility, electron peak velocity, breakdown field) of some selected semiconductor materials. Despite the maturity of the silicon process technology and its low cost, III-V compound semiconductors show higher electron mobility and electron peak velocities. InP exhibits the highest breakdown field and is thus usually used as the collector to improve the transistor breakdown property.

It was concluded in Reference [4] that SiGe-based HBTs are promising for low noise applications due to their lower noise figures, while they suffer from high speed and high breakdown operations due to their low bandgap; GaAs-based HBTs are suitable for high power applications due to their high-breakdown voltages, while they suffer from heat dissipation due to their poor thermal conductivity; and InP-based HBTs will be the choice for mm-wave frequency operation for high-data rates applications. The breakdown and thermal conduction properties of InP make InP-based HBTs attractive in various circuit application areas, such as frequency dividers with high $f_{\text{MAX}}$ InP HBTs [5], fast baseband amplifiers and multiplexers [6], as well as in high-performance analog-to-digital converters [7]. These applications are some of the driving forces that motivate this work.
Table 1.1 Selected material properties of Si, GaAs, InP, GaInAs.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap (eV)</td>
<td>1.12</td>
<td>1.42</td>
<td>1.35</td>
<td>0.75</td>
</tr>
<tr>
<td>Electron Mobility (cm$^2$/V·s)</td>
<td>1400</td>
<td>8500</td>
<td>4600</td>
<td>12000</td>
</tr>
<tr>
<td>Electron Peak Velocity ($\times 10^7$ cm/s)</td>
<td>1</td>
<td>2</td>
<td>2.5</td>
<td>3</td>
</tr>
<tr>
<td>Electron Saturation Velocity ($\times 10^7$ cm/s) [13]</td>
<td>0.8</td>
<td>0.8</td>
<td>1.5</td>
<td>0.7</td>
</tr>
<tr>
<td>Breakdown Field ($\times 10^5$ V/cm)</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>2</td>
</tr>
</tbody>
</table>
1.3 The State-of-the-Art for InP-Based HBTs

The use of GaAsSb instead of GaInAs as the base material in InP based HBTs shows different advantages. The conduction band offset of the type-II band alignment between the GaAsSb base and the InP collector provides an energy launcher for electrons. This eliminates the complex growth procedure to smooth out the electron barrier between the GaInAs base and InP collector for the InP/GaInAs DHBTs. The higher valence band discontinuity of InP/GaAsSb (~0.53 eV) compared to InP/GaInAs (~0.36 eV), provides an efficient barrier for the hole confinement, which leads to an improved DC current gain. One of the disadvantages of type-II InP/GaAsSb DHBTs is the conduction band discontinuity between the InP emitter and GaAsSb base, acting as an energy barrier that prevents electrons transferring from the emitter to the base. A part of our work focuses on the elimination of this barrier.

![Graph](image)

*Figure 1.2 State-of-the-art of $f_{\text{MAX}}$ versus $f_T$ for InP based HBT technology.*

$f_{\text{MAX}}$ is a good figure of merit for analog circuits, while $f_T$ is a good indicator for the switching speed of logic circuits. A trade-off challenge is usually faced when seeking simultaneously improved $f_T$, $f_{\text{MAX}}$ and breakdown voltage in HBTs. Transistors
exhibiting a high $f_T$ often incur a degraded $f_{MAX}$ and breakdown voltage. For instance, a thinner collector was adopted to reduce the collector transit time and therefore to increase $f_T$. The reduced collector thickness however results in a reduced breakdown voltage and an increased base/collector capacitance and therefore a reduced $f_{MAX}$. Figures 1.2 and 1.3 illustrate the state-of-the art of $f_{MAX}$ (maximum oscillation frequency) versus the current-gain cut-off frequency $f_T$ and the emitter-collector junction breakdown voltage $BV_{CEO}$ versus the collector thickness for various InP HBT technologies [14]-[40]. InP/GaInAs pseudomorphic HBTs (PHBTs) utilize pseudomorphic graded GaInAs base and collector. The pseudomorphic collector grading allows many benefits, such as an increased mobility in the indium-rich material, as well as a higher $Γ$-$L$ separation, allowing velocity overshoot to occur over a larger portion of the collector region to effectively reduce the collector transit time. They feature the highest $f_T$ due to the high electron mobility of GaInAs used as the base and collector layers. However, the lowest breakdown voltage is also obtained in PHBTs due to a narrow bandgap of the GaInAs collector. InP/GaAsSb DHBTs maintain the highest breakdown voltage for all collector thicknesses and the highest $f_T \times BV_{CEO}$ product. The highest $f_{MAX}$ has been achieved with InP/GaInAs DHBTs, but they exhibit poorer breakdown properties. Special epilayer structure design and fabrication processes need to be considered to achieve improved transistor high speed performances.
1.4 Base Grading to Improve Device DC and RF Performances

H. Kroemer stated [41] that although no internal electric field exists in material with a uniform doping concentration and composition, a change in composition can introduce a quasi-electric field, which helps to reduce the electron transit time.

Both the compositional grading and doping grading can be applied to aid the electron transport. For PHBTs [29], the electric field was introduced by an Indium compositional grading. For InP-based DHBTs containing antimony (Sb) in the base, a quasi-electric field can be induced by either increasing the Indium concentration in
1.5 Motivation for Low Noise Transistors

High-frequency noise in HBTs is the limiting factor in the performance of integrated circuits working in GHz range for wireless and wired communications. A poor noise performance translates into a large power consumption and a low battery lifetime of handheld devices. In addition, noisy transistors degrade the performance of fiber-optic receivers and prevent achieving the stringent requirements imposed on transimpedance amplifiers and oscillators working at 10 GHz or 40 GHz [42]. Receivers need to be able to detect and amplify incoming low-power signals without adding much noise.

Si/SiGe HBTs have shown significant advantages over III-V HBTs in terms of cost and noise performance. A minimum noise figure lower than 0.5 dB was shown in SiGe HBTs [43]. III-V HBTs are however competitive counterparts due to their outstanding transport properties.

Shot noise and thermal noise are two types of high-frequency noise relevant in semiconductor devices. Thermal noise exists in thermal equilibrium while shot noise exists in non-equilibrium and is proportional to current. Si CMOS and GaAs FETs have negligible shot noise due to the absence of pn junctions, making gate resistance thermal noise more of a contributor to the noise figure. In contrast, SiGe and InP HBTs have higher shot noise but lower base resistance and thermal noise. InP HBTs have an optimal bias current for noise figure that is considerably lower than the maximum gain bias, leading to a significant trade-off between noise and gain. Since our transistors feature a high current gain, the shot noise in the collector current becomes dominating. A low collector current level is thus preferable to achieve an
improved device noise performance. However, transistors are usually operated at high collector current levels to achieve high cut-off frequencies. In this work, device parasitics have been reduced to an extent enabling good cutoff frequencies to be achieved at low current levels which have enabled low noise device operation.

### 1.6 Scope of Dissertation

The group lead by Prof. C.R. Bolognesi set a new benchmark for high-speed HBTs with simultaneous $f_T$ and $f_{MAX}$ cut-off frequencies at 300 GHz with InP/GaAsSb DHBTs in 2001 at Simon Fraser University. In 2006, a new record $f_T$ of 384 GHz was set, and the group moved to the Swiss Federal Institute of Technology (ETH) and continued this project. The present work describes the continued development of InP/GaAsSb DHBTs within the FIRST lab at ETH.

Chapter 2 describes the fabrication process for devices with emitter areas of $20 \times 30$, $40 \times 40$, $80 \times 80 \ \mu \text{m}^2$, as well as for devices with submicron emitter widths between 0.2 and 0.5 $\mu \text{m}$. Processes relying on optical and electron beam lithography are presented in detail.

In Chapter 3, we present epilayer structure and fabrication process optimization studies aiming to improve device DC and RF performances. Epilayer optimization schemes for the emitter, base and collector are investigated. Furthermore, surface treatments are studied for lower emitter and base Ohmic contact resistivity.

In Chapter 4, the microwave noise characterization of AlInAs/GaAsSb/InP DHBTs and GaInP/GaAsSb/InP DHBTs is discussed. The development of a ledge process on AlInAs/GaAsSb/InP DHBTs is presented and the minimum noise figure results for both DHBT types are discussed. The impact of the base resistance on the minimum noise figure of AlInAs/GaAsSb/InP DHBT is studied.

Chapter 5 summarizes the results of this work and outlines future work areas for the extension of InP/GaAsSb DHBT technology.
Overview of Wafer Characterization and Device Fabrication Processes

This Chapter reviews in detail the epitaxial material preparation, the fabrication of large area transistors with emitter areas of 20 × 30, 40 × 40 and 80 × 80 μm², and the fabrication of submicron transistors with designed emitter widths of 0.2, 0.3, 0.4 and 0.5 μm. The fabrication process for the sub-micron DHBTs is based on a standard self-aligned triple mesa technology, using optical and electron beam lithography.
2.1 Epitaxial Layer Growth

2.1.1 Growth System and Configuration

Metal-organic vapor phase epitaxy (MOVPE) was used for the growth of the DHBT epitaxial layers used in this work.

Growths were performed in an Aixtron AIX 200/4 (Fig. 2.1) horizontal reactor heated by halogen lamps under palladium-diffused hydrogen atmosphere. The precursor sources were trimethylgallium (TMGa) and trimethylindium (TMIn) for the group III elements, and trimethylantimony (TMSb), arsine (AsH$_3$) and phosphine (PH$_3$) for the group-V elements. The precursors for the $p$- and $n$- type doping are carbon tetrabromide (CBr$_4$) and silane (SiH$_4$), respectively.

![Figure 2.1 Front view of the MOVPE growth system in FIRST lab.](image)

The DHBT structure was deposited on 2-inch (100) semi-insulating (Fe-doped) InP substrates. The reactor temperature was set to 610°C for the growth of the InP sub-collector, collector, emitter cap and the InGaAs contact layers. The InP emitter and the GaAsSb:C base layers were deposited at 550°C. A lower growth temperature was selected for GaAsSb because thus a higher free hole concentration could be achieved [44]. The reactor pressure was set to 160 mBar and the carrier gas flow ranges
between 10.5 to 21.5 l/min. We have taken advantage of the mass flow controllers to grow compositionally graded bases and emitter layers in the DHBT structures.

An *in-situ* optical monitoring system (EpiRAS) installed on the growth tool enables different measurements during the growth on the wafer surface, such as growth rate, rotation speed, reflectance, reflectance anisotropy spectroscopy (RAS) signal and surface temperature.

### 2.1.2 Epilayer Characterization and Calibration

The composition of the ternary alloys as well as the layer thickness was determined by high-resolution X-ray diffraction measurements from calibration wafers. Carrier concentrations and mobilities of the semiconductor materials were obtained from Hall effect and capacitance-voltage measurements. Multiple calibration growths allowed by trial-and-error to find the appropriate growth conditions for the deposition of the designed DHBT structure.

### 2.1.3 Transistor Structure

Table 2.1 shows a typical epilayer structure for an optimized InP/GaAsSb DHBT. The epitaxial growth of the DHBT structure begins with a 300 nm thick InP:Si sub-collector layer with an \( n \)-type doping concentration of \( 3 \times 10^{19} \text{ cm}^{-3} \) and a 20 nm thick \( \text{Ga}_{0.37}\text{In}_{0.63}\text{As}:\text{Si} \) etch stop layer doped at \( 3 \times 10^{19} \text{ cm}^{-3} \). A 50 nm thick InP:Si collector pedestal doped at \( 1 \times 10^{19} \text{ cm}^{-3} \) is used to reduce the extrinsic collector capacitance. The 75 nm thick InP collector layer is nominally doped with silicon at \( 3 \times 10^{16} \text{ cm}^{-3} \). The 20 nm thick base is formed by a carbon (C) \( p \)-doped \( \text{GaAs}_{x}\text{Sb}_{1-x} \) layer with an average doping level of \( 8 \times 10^{19} \text{ cm}^{-3} \). For graded-base layers, the As concentration increases from \( x = 0.4 \) on the collector side to \( x = 0.6 \) at the emitter side. The \( n \)-doped composite emitter consists of 15 nm thick \( \text{Ga}_{y}\text{In}_{1-y}\text{P}:\text{Si} \) doped at \( 1.5 \times 10^{17} \text{ cm}^{-3} \), 10 nm thick graded \( \text{Ga}_{y}\text{In}_{1-y}\text{P} \) and 15 nm thick InP doped at \( 7.8 \times 10^{17} \text{ cm}^{-3} \). The ternary alloy is linearly graded with the Ga concentration varying from \( y = 0.22 \) next to the base, to \( y = 0 \) on the emitter surface side. A 10 nm thick InP:Si layer doped at \( 1 \times 10^{18} \text{ cm}^{-3} \) is inserted as a doping transition layer, and followed by a 100 nm thick InP:Si emitter layer doped with silicon at \( 3 \times 10^{19} \text{ cm}^{-3} \). The 35 nm composite emitter contact layer consists of 20 nm of \( \text{Ga}_{0.47}\text{In}_{0.53}\text{As}:\text{Si} \) with
a doping level of $3 \times 10^{19}$ cm$^{-3}$, 10 nm of Ga$_{0.47}$In$_{0.53}$As graded to Ga$_{0.22}$In$_{0.78}$As, and 5 nm of Ga$_{0.22}$In$_{0.78}$As:Si doped at $3 \times 10^{19}$ cm$^{-3}$.

Table 2.1 A typical InP/GaAsSb DHBT epilayer structure used in the present work.

<table>
<thead>
<tr>
<th>Bol286</th>
<th>Thickness</th>
<th>Doping (cm$^{-3}$)</th>
<th>Composition</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>In$<em>{z}$Ga$</em>{1-z}$As</td>
<td>50 Å</td>
<td>Si: $&gt; 3 \times 10^{19}$</td>
<td>$z = 0.78$</td>
<td>Emitter cap</td>
</tr>
<tr>
<td>In$<em>{z}$Ga$</em>{1-z}$As</td>
<td>100 Å</td>
<td>Si: $&gt; 3 \times 10^{19}$</td>
<td>$z = 0.53 \rightarrow 0.78$</td>
<td>Emitter cap</td>
</tr>
<tr>
<td>In$<em>{z}$Ga$</em>{1-z}$As</td>
<td>200 Å</td>
<td>Si: $&gt; 3 \times 10^{19}$</td>
<td>$z = 0.53$</td>
<td>Emitter cap</td>
</tr>
<tr>
<td>InP</td>
<td>1000 Å</td>
<td>Si: $3 \times 10^{19}$</td>
<td>Emitter</td>
<td></td>
</tr>
<tr>
<td>InP</td>
<td>100 Å</td>
<td>Si: $1 \times 10^{18}$</td>
<td>Emitter</td>
<td></td>
</tr>
<tr>
<td>InP</td>
<td>150 Å</td>
<td>Si: $7.8 \times 10^{17}$</td>
<td>Emitter</td>
<td></td>
</tr>
<tr>
<td>InP</td>
<td>100 Å</td>
<td>Si: $1.5 \times 10^{17} \rightarrow 7.8 \times 10^{17}$</td>
<td>Emitter</td>
<td></td>
</tr>
<tr>
<td>In$<em>{1-y}$Ga$</em>{y}$P</td>
<td>100 Å</td>
<td>Si: $1.5 \times 10^{17}$</td>
<td>$y = 0.22 \rightarrow 0$</td>
<td>Emitter</td>
</tr>
<tr>
<td>In$<em>{1-y}$Ga$</em>{y}$P</td>
<td>50 Å</td>
<td>Si: $1.5 \times 10^{17}$</td>
<td>$y = 0.22$</td>
<td>Emitter</td>
</tr>
<tr>
<td>GaAs$<em>{x}$Sb$</em>{1-x}$</td>
<td>200 Å</td>
<td>C: $1 \times 10^{19} \rightarrow 6 \times 10^{19}$</td>
<td>$x = 0.6 \rightarrow 0.4$</td>
<td>Base</td>
</tr>
<tr>
<td>InP</td>
<td>750 Å</td>
<td>Si: $3 \times 10^{16}$</td>
<td>Collector</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>45 min Pause</td>
<td></td>
</tr>
<tr>
<td>InP</td>
<td>500 Å</td>
<td>Si: $1 \times 10^{19}$</td>
<td>Sub-Collector</td>
<td></td>
</tr>
<tr>
<td>In$<em>{z}$Ga$</em>{1-z}$As</td>
<td>200 Å</td>
<td>Si: $&gt; 3 \times 10^{19}$</td>
<td>$z = 0.498$</td>
<td>Sub-Collector</td>
</tr>
<tr>
<td>InP</td>
<td>3000 Å</td>
<td>Si: $3 \times 10^{19}$</td>
<td>Sub-Collector</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S.I. InP Substrate</td>
<td></td>
</tr>
</tbody>
</table>
2.2 Quick HBT Fabrication Process and DC Characterization of InP/GaAsSb DHBTs

We have routinely used a three-step process, called quick HBT (QHBT) process to fabricate a DHBT with the emitter sizes of 20 × 30, 40 × 40, and 80 × 80 μm² in order to perform a rapid characterization of the epilayer quality.

A schematic QHBT process flow is shown in Fig. 2.2(a) – (d). This process consists of emitter and base mesa etching steps (b) – (c) and a common final metallization step (d). The etching solution H₃PO₄:H₂O₂:H₂O (6:2:80) was used for removing the InGaAs emitter cap and the GaAsSb base. For the InP emitter and collector etching we used the solution HCl:H₂O (30:20). The etching time and type of the solution during the emitter and base mesas etching were not optimized at this stage since the undercut for transistors with a large emitter area is not critical for the device performance. A metal stack of Pt/Ti/Pt/Au (2/15/15/300 nm) was deposited to form the emitter, base and collector contacts. The final devices are shown in Fig. 2.3 with the emitter, base and collector contacts, labeled with (E), (B), (C), respectively. Particular care was taken to keep the fabrication process simple and reproducible for all the DHBTs structures. This enables a meaningful comparison of electrical properties between devices of different structures, excluding effects which might otherwise result from non-standard processing steps.

A Karl Süss PM8 wafer prober was used to measure the QHBTs. Sharp probe tips with 12 μm radius were contacting the devices. A Keithley SCS 4200 parameter analyzer was used to measure the device DC performances such as the BE junction curve $I_B - V_{BE}$, the BC junction curve $I_B - V_{BC}$, the Gummel characteristics $I_B, I_C - V_{BE}$, the common-emitter $I_C - V_{CE}$ characteristics, and emitter-collector junction breakdown properties $I_{CEO} - BV_{CEO}$. The dependence of DC gain on the base sheet resistance was also examined in these devices.
Figure 2.2  Schematic process flow for the preparation of a QHBT. (a) Epilayers after growth; (b) Emitter mesa formation; (c) Base mesa formation; (d) Final metallization.
Figure 2.3  Optical microscope pictures of the processed QHBT with emitter areas of $20 \times 30$, $40 \times 40$ and $80 \times 80 \, \mu m^2$. Emitter, base and collector contacts are labeled as $E$, $B$ and $C$, respectively.
2.3 High-Speed DHBT Fabrication Process

2.3.1 Overview of High-Speed DHBT Fabrication Process Flow

Devices with submicron feature sizes are required for reducing the junction capacitances, leading thus to improved RF device characteristics. Emitter widths of $\sim 0.5 \, \mu\text{m}$ can be fabricated with optical contact lithography. Further downscaling of the device dimensions requires the utilization of high resolution lithography systems, such as electron beam lithography.

An overview of the high-speed DHBTs fabrication process by optical contact or electron beam lithography is schematically depicted in Fig. 2.4. The fabrication process includes the following steps: emitter metallization (a) – (b), emitter mesa etching (c) – (e), base metallization (f) – (h), base mesa etching (i) – (j), collector metallization (k), isolation mesa etching (l) – (m), air bridge patterning (n) – (p) and final pad metallization (q).
2.3 High-Speed DHBT Fabrication Process

(a) E-Cap
Emitter
Base
Collector
Sub-Collector
Buffer
Substrate

(b) E-Cap
Emitter
Base
Collector
Sub-Collector
Buffer
Substrate

(c) E-Cap
Emitter
Base
Collector
Sub-Collector
Buffer
Substrate

(d) E-Cap
Emitter
Base
Collector
Sub-Collector
Buffer
Substrate

(e) E-Cap
Emitter
Base
Collector
Sub-Collector
Buffer
Substrate

(f) E-Cap
Emitter
Base
Collector
Sub-Collector
Buffer
Substrate

(g) E-Cap
Emitter
Base
Collector
Sub-Collector
Buffer
Substrate

(h) E-Cap
Emitter
Base
Collector
Sub-Collector
Buffer
Substrate
2.3 High-Speed DHBT Fabrication Process

Figure 2.4  Schematic process flow of high-speed DHBT. (a) As-grown epilayers; (b) Emitter metallization; (c) Emitter mesa formation; (d) Emitter mesa protection; (e) Interface removal; (f) Protection resist removal; (g) Base metal lithography; (h) Base metallization; (i) Base mesa lithography; (j) Base mesa formation; (k) Collector contact metallization; (l) Isolation lithography; (m) Isolation mesa formation; (n) PMMA lithography; (o) PMMA reflow; (p) AZ lithography; (q) Pad metallization.

In the next sections, the details of some process steps are presented and representative in-process scanning electron microscopy (SEM) images are shown.
2.3.2 DHBT Process Flow by Optical Contact Lithography

Emitter Metallization

Optical contact lithography is carried out with a Karl Süss MA6 mask aligner. The smallest emitter size designed on the optical mask is 0.5 \( \mu \text{m} \). For the metallization step, a 1.1 \( \mu \text{m} \) thick AZ5214E resist is applied by spin-coating the resist at 6000 rpm during 40 seconds. The metal contact is defined by patterning this 1.1 \( \mu \text{m} \) thick resist and developing the resist in the AZ developer after exposure. A metal stack of Ti/Pt/Au (5/20/350 nm) is then deposited, and the emitter contact is finally obtained after a lift-off process. For the smallest emitter size on the mask of 0.5 \( \mu \text{m} \), an emitter metal width of 0.78 ~ 0.80 \( \mu \text{m} \) can be achieved, as shown in Fig. 2.5.

![Emitter Metal](image)

*Figure 2.5*  SEM picture showing the emitter contact after lift-off.

Emitter Mesa

During this step, the emitter metal in the device active region acts as a hard mask to define the semiconductor emitter-base junction. In order to reduce the emitter undercut, which plays an important role for the extrinsic base resistance, an experiment to characterize the InGaAs etch rate was carried out. A calibration wafer with the epilayer structure shown in Table 2.2 was used in this experiment. Two solutions CH\(_3\)COOH:H\(_2\)O\(_2\):H\(_2\)O (30:6:60) and H\(_3\)PO\(_4\):H\(_2\)O\(_2\):H\(_2\)O (6:2:80) were respectively used to etch two samples for 15 seconds. The etch rates were
210 nm/minute for CH$_3$COOH:H$_2$O$_2$:H$_2$O (30:6:60) and 246 nm/minute for H$_3$PO$_4$:H$_2$O$_2$:H$_2$O (6:2:80). The CH$_3$COOH:H$_2$O$_2$:H$_2$O (30:6:60) solution was chosen to etch the emitter cap layer, since its lower etch rate ensures a precise control of the InGaAs undercut etching. Besides the vertical selective etching of the 35 nm thick emitter cap layer, an approximate 50 nm undercut was formed after etching for 15 seconds.

*Table 2.2 Calibration wafer structure used for wet etching test.*

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Concentration</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 nm In$<em>{0.75}$Ga$</em>{0.25}$As:Si</td>
<td>3.5×10$^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>10 nm grading In$<em>{0.49}$Ga$</em>{0.51}$As to In$<em>{0.75}$Ga$</em>{0.25}$As:Si</td>
<td>3.5×10$^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>~100 nm In$<em>{0.49}$Ga$</em>{0.51}$As:Si</td>
<td>3.5×10$^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>50 nm InP:Si</td>
<td>1.3×10$^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>S.I. InP Substrate</td>
<td></td>
</tr>
</tbody>
</table>

The remaining part of the emitter, which consists of InP, was etched in HCl:H$_3$PO$_4$ (12:72) for 10 seconds at 45°C. This etch produces an undercut of ~60 nm, leading to a total emitter mesa undercut of ~110 nm with respect to the emitter metal. With this undercut, the emitter-base junction width ranges between 0.55 and 0.60 μm wide. An SEM image showing the emitter undercut cross-section is depicted in Fig. 2.6.

*Figure 2.6* SEM picture showing the emitter cross-section after the emitter mesa etching. A 115.6 nm wide undercut is shown.
Base Metallization

MIBK developer is used in this process step, because the TMAH in the AZ developer etches the base surface. Consequently, PMMA and the co-PMMA resists were used since they can be developed by the MIBK developer. Sample alignment with respect to the mask and exposure were performed with an ABM Deep-UV mask aligner, since both PMMA and co-PMMA can be exposed by deep ultra-violet (DUV) light. A negative resist profile is formed after developing PMMA spun on top of co-PMMA, because the MIBK developer dissolves co-PMMA faster than PMMA (see Fig. 2.7).

The base contact was self-aligned to the emitter, which reduces the distance between the emitter mesa edge and the base contact edge, decreasing thus the extrinsic base resistance. A base metal width of 1.25 μm was designed to provide enough margin for manual contact lithography, because the optical alignment cannot be performed accurately on contact widths below ~1 μm. Pt/Ti/Pt/Au with the thickness of 2/10/10/80 nm metal stack was evaporated to form the base contact metal. The deposition of Pt on the p-type doped GaAsSb base surface produces a lower contact resistivity compared to other metals like Ti with a lower work function energy (Ti:4.33 eV; Pt:5.12 ~ 5.93 eV [45]). Moreover, Pt is known to be very reactive with the surface and at the same time, depending on the Pt layer thickness, it does not diffuse much into the semiconductor [46] [47]. These features of Pt, make this metal suitable as the first layer deposited on the base surface. The Pt deposited on top of Ti serves as a diffusion barrier preventing the Au diffusion into the semiconductor.

![Figure 2.7](image-url)  
*Figure 2.7  Resists profile before the base metallization.*
2.3 High-Speed DHBT Fabrication Process

Base Mesa

A combination of dry and wet etching was performed for the base mesa formation. Dry etching is first applied to the base layer and a part of the collector. To achieve the designed collector size, a precise base undercut etching with the solution H₃PO₄:H₂O₂:H₂O (6:1:80) is necessary. The remaining part of the collector and the InP pedestal are etched by the solution HCl:H₃PO₄ (12:72) at 45°C. To prevent the emitter from being also etched in these last two wet etching steps, the whole emitter was protected by Shipley 1818 resist as shown in Fig. 2.8 which is the dark area in the center of the image.

![SEM picture of a transistor configuration after the base mesa etching. The dark areas in the center of the image are Shipley1818 photoresist.](image)

Collector Metallization

A thin InGaAs contact layer was grown above the heavily doped InP sub-collector. This contact layer provides a low collector contact resistance and serves as an etching stop layer to protect the sub-collector during the base mesa wet-etching. The low InGaAs thermal conductivity of 0.05 Wcm⁻¹K⁻¹ does not allow efficient heat dissipation from the operating device into the sub-collector and the substrate [48]. An excessive thermal resist can be avoided by reducing the InGaAs layer thickness. On the other hand, an improved contact layer sheet resistance results directly from increasing its thickness and the doping concentration. Consequently, the thickness of
the InGaAs layer has to be carefully adjusted. In the course of this work, an InGaAs layer thickness of 20 nm and a doping concentration higher than $3 \times 10^{19}$ cm$^{-3}$ have been chosen. The sheet resistance of InGaAs contact layer together with the InP sub-collector layer is 12 Ohm/$\square$. Fig. 2.9 shows an SEM picture of several transistors after the collector contact metallization.

![SEM picture of DHBTs after collector contact metallization.](image)

**Figure 2.9 SEM picture of DHBTs after collector contact metallization.**

**Isolation Mesa Etching**

The isolation step adopted in this work involves a micro air bridge process, consisting of a metal bridge that connects the base contact to the base pad metal.

Fig. 2.10(a) and (b) show SEM images of the base air bridge respectively with and without underlying conductive material. The base air bridge metal width (see Figs. 2.10) was 2 $\mu$m. In this step, the active region of the transistors is protected by Shipley 1818 photoresist. On the exposed areas, a ~ 500 to 600 nm isolation mesa height is produced and ensures that all the devices are isolated from each other. The base layer, collector, sub-collector and part of the substrate underneath the air bridge metal were etched. The chemical wet etching for InGaAs in the solution $\text{H}_3\text{PO}_4$:$\text{H}_2\text{O}_2$:$\text{H}_2\text{O}$ and for InP in $\text{HCl}$:$\text{H}_3\text{PO}_4$ is performed two times to guarantee a complete removal of the base/collector material underneath the metal air bridge.
2.3 High-Speed DHBT Fabrication Process

Figure 2.10  Base air bridge (a) with some material underneath and (b) without any material underneath the metal air bridge.

If the material underneath the base air bridge is not completely etched away, larger BC junction capacitances and lower maximum oscillation frequencies $f_{\text{MAX}}$ [49] are to be expected. The $I_B - V_{BC}$ base/collector diode characteristics measured from the devices with and without residual material below the air bridge metal are shown in Fig. 2.11. The device with no semiconductor material under the air bridge metal shows more ideal BC junction characteristics and a lower BC current at low biases.

![Base Air Bridge](image)

Figure 2.11  Effect of the residual semiconductor material under the base air bridge on the $I_B-V_{BC}$ B/C diode characteristics.
Air Bridge and Pad Metallization

After the isolation step, the active device fabrication is finished. Air bridges enable the connection between the emitter and the final pad.

A scheme of the air bridge formation is shown in Fig. 2.12. Three PMMA resist layers with a total thickness of 1.5 μm were spun on top of the devices with a height of 1.2 μm as depicted in (a). The resist was patterned by DUV optical contact lithography. The PMMA resist was reflowed at 180°C for 10 minutes (b). The AZ resist was patterned to define the pad and air bridge, while the reflowed PMMA serves as a support for the deposited metal (c). The PMGI polymer was inserted between the PMMA resists and the substrate, which forms an improved undercut due to its higher development rate in the AZ developer.

![Figure 2.12 Air bridge formation scheme. (a) PMMA lithography; (b) PMMA reflow; (c) AZ lithography; (d) lift-off.](image)

Consequently, the final pad lift-off is facilitated. Since PMMA is not sensitive to near-UV light, but only to DUV light, the exposure of the top AZ resists does not affect the PMMA resist at all. Finally, the devices were dipped in NMP during 30 minutes for lift-off (d).
2.3 High-Speed DHBT Fabrication Process

An SEM picture of the whole device after PMMA and final pad lift-off is shown in Fig. 2.13(a) and (b), respectively. PMMA covers the device active region and the region where the emitter air bridge spans over the collector contact metal.

Figure 2.13  (a) A transistor covered by patterned PMMA layers; (b) A final transistor profile rotated by 180° with respect to the one in (a).
2.3.3 Process Flow for DHBTs Scaled for Narrow Emitter Widths

Further DHBT down-scaling is necessary to improve the transistor high-frequency performances. For this purpose, electron beam lithography (EBL) was used in the fabrication process. Because structures of less than 500 nm cannot be patterned by optical contact lithography and because an excellent alignment between the emitter and base contacts is required when base contact widths are of $\leq 0.5 \, \mu m$, the emitter and base contact metallization process steps were realized by EBL. EBL provides excellent level-to-level alignment tolerances and small feature resolution. All the other process steps were carried out by optical contact lithography as described above. However, an additional PMMA etch-back process step was introduced before the final pad metallization. The etch-back process was applied to expose the emitter contact, as well as the base and collector plugs, which are deposited for the emitter, base and collector contacts planarization. After the etch-back process, the emitter contact, the base and collector plugs are connected to the final metal pads through air bridges.

The emitter and base metallization steps achieved by means of electron beam lithography as well as the emitter and base mesa etching, the PMMA etch-back process followed by the final metallization step are presented in detail.

Emitter Metallization

The emitter metal size is one of the factors that influence the radio-frequency (RF) performance of DHBTs. Increasing the emitter size increases the intrinsic BE and BC junction capacitances, which results in a drop of the cutoff frequency $f_T$. On the other hand, a reduction of the emitter size increases both the emitter contact and the semiconductor resistances.

For the photolithography step, PMMA and co-PMMA resists were used. The emitter sizes were designed to be 0.2 $\mu m$, 0.3 $\mu m$ and 0.4 $\mu m$. A 1 $\mu m$ thick resist layer was spun on top of the emitter cap layer. Firstly, the resist was patterned by electron beam lithography. After developing the resist in MIBK developer, a Ti/Pt/Au metal stack was deposited. Finally, the emitter contact was obtained after lift-off. The real emitter size was approximately 100 nm larger than the designed size (see Fig. 2.14), which is
the consequence of the electron scattering effect in the resist occurring during the electron beam lithography exposure.

![Graph showing real emitter metal size versus design size after emitter metallization step.](image)

*Figure 2.14  Real emitter metal size versus design size after emitter metallization step.*

**Emitter Mesa Etching**

The formation of an undercut during the emitter mesa etching is of pivotal importance to prevent a short circuit between base and emitter when the self-aligned base contacts are deposited. On the other hand, an excessive undercut which reduces the emitter area at the base/emitter junction results in an increased base extrinsic resistance, and in a thus lower maximum oscillation frequency. For these reasons, the undercut etching has to be carefully adjusted.

A combination of ICP-RIE dry and wet etching is employed to define the undercut. The parameters for the dry etching, the vertical etch rates and the SEM images of the emitters are shown in Table 2.3.
Four etching conditions were tested, labeled as Test 1, 2, 3 and 4, respectively. Test 3 exhibited the lowest etch rate. Test 1, 2, and 4 exhibited similar profile results. The etching conditions for Test 1 led to the highest etch rate and were applied to the emitter removal. As can be seen in Table 2.3, the dry etching does not result in any undercut with respect to the emitter metal.

Wet etching is applied directly after dry etching to remove the remaining part of the exposed emitter layer. During the wet chemical etching, the exposed InP emitter layer is etched vertically as well as laterally underneath the emitter contact. The emitter
width at the base/emitter junction could be defined by setting the appropriate layer thickness removed by dry etching, before applying wet etching.

![SEM picture after emitter mesa formed by a combination of dry and wet etching. The undercut on each side of the emitter mesa is 60 to 70 nm.](image)

**Figure 2.15**  *SEM picture after emitter mesa formed by a combination of dry and wet etching. The undercut on each side of the emitter mesa is 60 to 70 nm.*

A complete emitter removal via ICP-RIE dry etching is not possible, because it is not selective for the base material, it produces surface defects and no emitter metal undercut is formed. The combination of 85 nm dry and 100 nm wet etching led to a total undercut of 60-70 nm as shown in Fig. 2.15. This undercut is to be compared to a value of 110 ~ 120 nm when the emitter mesa is completely wet etched.
Base Metallization

The base contacts are self-aligned to the emitter metal. PMMA and co-PMMA were spun on the whole wafer surface, with a total thickness of 1.4 μm. EBL was used to pattern 1.0 μm, 1.1 μm, 1.2 μm wide structures centered on the emitter mesas with 0.2 μm, 0.3 μm and 0.4 μm wide, respectively. After developing the resist in MIBK developer, the total structure width of the window opening in the resist was approximately 150 nm larger than the designed sizes, owing to the electron scattering mechanism during EBL exposure (see Fig. 2.16). A 200 × 200 μm² rather than 800 × 800 μm² write field improved the precision in the alignment of the base contact with respect to the emitter contact.

Figure 2.16  Real total base metal width versus design size.
In the worst case, the lack of alignment accuracy will make the base contact appear only on one side of the emitter. As a result, the total base resistance doubles, which reduces the base and collector current [50]. Fig. 2.17 shows an SEM picture after base contact metallization. The base pad is evaporated simultaneously with the base contact allowing a connection to the probing pads at a later stage.

**SiN\textsubscript{x} Deposition and Base Mesa Etching**

After the self-aligned base contact metallization, a 220 nm thick SiN\textsubscript{x} layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at a temperature of 120°C. The low temperature for this deposition was chosen in order to prevent base contact resistivity degradation. Reactive ion etching (RIE) was employed to etch SiN\textsubscript{x} and re-expose the emitter and base metal contacts. The ellipsometer was used to measure the SiN\textsubscript{x} thickness before and after etching to calibrate the SiN\textsubscript{x} growth and etch rates. SiN\textsubscript{x} is left on the extrinsic base mesa, between the base contact and the emitter mesa, as well as on the emitter mesa sidewalls, and should act as a passivation layer.
An etch rate of ~50 nm/min was determined. After SiNx etching, 150 - 200 nm of the emitter metal have to be exposed (see Fig. 2.18) to ensure good conduction between the emitter metal and the emitter pad. If the exposed emitter metal height exceeds 200 nm, the base layer in the extrinsic region is also etched (see Fig. 2.19, with the emitter-base barely becoming an open circuit), leading to an emitter-base open circuit. On the other hand, if SiNx is not sufficiently etched to expose the emitter contact, the emitter metal resistance rapidly increases. The emitter and base metals as well as SiNx on the emitter sidewalls and on the extrinsic base region create a protection mask for the base mesa etching.
During the base mesa etching, the base and part of the collector were first etched by the ICP-RIE dry etching process. The mesa height obtained after the dry etching was \( \sim 40 \text{ nm} \). The base undercut was carefully adjusted by the etch time of the sample in the solution \( \text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} \) (6:1:80). The width of the base metal contact on the base material should not be smaller than the transfer length. If it is smaller, it reduces the base collector current, which further degrades the high frequency performances.

The remaining part of the base mesa, which consists of an InP collector and the InP:Si pedestal layers, was etched in \( \text{HCl}:\text{H}_3\text{PO}_4 \) (12:72) at 45\(^\circ\)C. The collector width is typically the same as the base width.

The descriptions of the collector metallization and the isolation etching steps are identical to those of the optical contact lithography process.

**Metal Plugs Deposition, PMMA Etch-Back and Final Pad Metallization**

![A schematic diagram for the base and collector plugs.](image)

*Figure 2.20  A schematic diagram for the base and collector plugs.*

After the isolation mesa etch step, the base and collector contacts are approximately at the same height whereas the emitter contact is higher. To bring the collector and base contacts up to the height of the emitter contact, 640 nm metal plugs were deposited as shown in Fig. 2.20. To realize the air-bridge contacts, PMMA was spun to cover completely all the device structures on the wafer. An etch-back process of the PMMA was performed by an \( \text{O}_2 \) plasma to expose the emitter contact metal, and the base and
collector plugs. The emitter metal and the plugs have to be exposed 200-300 nm to guarantee a proper electrical connection to the air-bridge contacts. Exceeding a PMMA resist etching of 300 nm causes a short circuit between the emitter air-bridge and the collector metal. After etching, the PMMA resist is reflowed to improve the step coverage.

An SEM picture of a transistor after etch-back and reflow is shown in Fig. 2.21(a). A metal stack of Ti/Pt/Au (10/30/900 nm) was deposited to form the final pad and the air bridge metals. The emitter pad metal deposition was integrated in the air bridge contact metallization step. The latter serves as a connection layer between the emitter metal and the final pad metal. An SEM picture after the final pad liftoff is shown in Fig. 2.21(b).

Figure 2.21 SEM picture (a) after PMMA etch-back and (b) after final pad lift-off.
Optimization of DHBT Structure Design and Fabrication Process

The transistor DC and RF performances directly depend on the epilayer structure design, the growth and the fabrication process. This Chapter presents the optimization of the DHBT epilayer stack and the fabrication process aiming for improved DC and RF device performances. Surface treatments during device fabrication were studied to reduce the contact resistivity. Respective emitter and base contact resistivity as low as \(5 \times 10^{-9} \ \Omega \cdot \text{cm}^2\) and \(4 \times 10^{-8} \ \Omega \cdot \text{cm}^2\) could be achieved. A DC gain of 220 was obtained on InP/GaAsSb QHBTS with an emitter area of \(20 \times 30 \ \mu\text{m}^2\). Devices with an emitter area of \(0.6 \times 11.5 \ \mu\text{m}^2\) fabricated by optical contact lithography exhibited cut-off and maximum oscillation frequencies \(f_T\), \(f_{\text{MAX}} > 350 \ \text{GHz}\) simultaneously. A peak current-gain cut-off frequency \(f_T\) of 475 GHz was achieved by electron beam lithography on devices with an emitter area of \(0.4 \times 8.4 \ \mu\text{m}^2\) and a 50 nm thick collector.
Chapter 3: Optimization of DHBT Structure Design and Fabrication Process

The GaAs\textsubscript{0.51}Sb\textsubscript{0.49} mixed-group V ternary alloy is an interesting alternative base material for InP-based N-p-N DHBTs by virtue of a staggered “type-II” band alignment with InP that prevents the collector electron blocking effect at the B/C heterojunction. The type-II B/C conduction band offset functions as an electron launcher, which accelerates electrons as they are injected from the GaAsSb base into a full InP collector. Additionally, the large valence band discontinuity $\Delta E_V$ at emitter/base (E/B) junction suppresses the back-injection of holes into the emitter. A key advantage of the InP/GaAsSb material system is that high-performance DHBTs can be implemented \textit{without any} grading layers at both the E/B and B/C heterojunctions. The principal challenge is of course that GaAsSb technology currently is less mature than its GaInAs electronics/optoelectronics counterparts.

### 3.1 Emitter Optimizations

#### 3.1.1 Emitter Contact Resistivity Optimization

Because the emitter resistance plays an important role in the total charging time, an emitter contact resistivity of $\leq 1 \times 10^{-8} \ \Omega \cdot \text{cm}^2$ is required for the DHBT fabrication with improved high-speed performances [51]. Consequently, the high emitter contact resistivity of $1.62 \times 10^{-7} \ \Omega \cdot \text{cm}^2$ we measured at the early stage of our project had to be decreased.

In order to reduce the emitter contact resistivity, both the Indium (In) concentration and the doping level in the InGaAs emitter cap layers were increased. Furthermore, an optimized surface treatment was applied before the emitter contact metallization.

#### 3.1.1.1 Emitter Contact Resistivity Improvement by Epilayer Optimization

A contact for a heavily $n$-doped InGaAs layer is formed by depositing a layer stack of Ti/Pt/Au. Ti is the metal layer in contact with the semiconductor surface and has an electron work function of 4.33 eV. On the other hand, InGaAs lattice to InP shows an electron affinity of 4.5 eV. Assuming that the Fermi level of InGaAs does not pin at the semiconductor/metal interface, no barrier is present for electrons (see Fig. 3.1). Compared to Pt, Ni and Au, Ti is the metal with the lowest work function, and thus
the most appropriate material to form a low resistive contact with the InGaAs:Si contact layer.

![Figure 3.1](image1.png)

**Figure 3.1** Theoretical band diagram of Ti/InGaAs interface for a heavily doped n-type InGaAs in the absence of surface states (a) before and (b) after equilibrium.

In reality, however, defects at the metal/semiconductor interface produce a bending of the InGaAs bands, as qualitatively depicted in Fig. 3.2.

![Figure 3.2](image2.png)

**Figure 3.2** Band bending in the presence of surface states.

A barrier for the electrons is formed for Ti and In$_{0.53}$GaAs, which leads to an increased contact resistivity. The contact resistivity depends on the doping concentration $N_d$ and the total barrier height $\phi_{bn}$ according to Eqn. (3.1) [52]:

$$\rho_c \propto \exp\left(\frac{2\sqrt{e_m}}{h} \cdot \frac{\phi_{bn}}{\sqrt{N_d}}\right)$$  \hspace{1cm} (3.1)
where $\phi_{Bn}$ is the effective barrier height, $m_n^*$ is the electron effective mass and $N_d$ is the carrier concentration.

A higher doping level results in a lower contact resistivity (Eqn. 3.1), since the decreased depletion width increases the tunneling probability of electrons through the barrier. The contact resistivity can be further reduced by increasing the In content in InGaAs. In fact, as shown in Ref. [53], the In-rich ternary alloy shows a higher electron affinity and the Fermi-level pinning at the metal/InGaAs interface occurs closer to or even in the conduction band, reducing $\phi_{Bn}$. Therefore, an InGaAs layer with increased doping level and indium content is preferred for the improvement of emitter contact resistivity.

We have investigated the indium concentration effect on the emitter contact resistivity with InGaAs:Si doped at $4 \times 10^{19}$ cm$^{-3}$.

Table 3.1 shows the details of four emitter cap layer structures with In concentrations of 0.498, 0.782, 0.826, 0.87 in the top 5 nm InGaAs. The linear transmission line method (L-TLM) was applied to characterize the emitter contact resistivity. After the contact metallization step, the TLM structures were formed by wet etching of the InGaAs and InP. The mesas were etched down to isolate the TLM structures from each other.

**Table 3.1 DHBT emitter cap layer structures used for the investigation of the contact resistivity.**

<table>
<thead>
<tr>
<th>In$<em>x$Ga$</em>{1-x}$As</th>
<th>Bol183</th>
<th>Bol187</th>
<th>Bol186</th>
<th>Bol185</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 nm</td>
<td>0 nm</td>
<td>5 nm, $x = 0.782$</td>
<td>5 nm, $x = 0.826$</td>
<td>5 nm, $x = 0.87$</td>
</tr>
<tr>
<td>Graded In$<em>x$Ga$</em>{1-x}$As</td>
<td>0 nm</td>
<td>10 nm, $x$ from 0.498 to 0.782</td>
<td>10 nm, $x$ from 0.498 to 0.826</td>
<td>10 nm, $x$ from 0.498 to 0.87</td>
</tr>
<tr>
<td>In$<em>{0.498}$Ga$</em>{0.502}$As</td>
<td>325 nm</td>
<td>325 nm</td>
<td>325 nm</td>
<td>325 nm</td>
</tr>
<tr>
<td>$4 \times 10^{19}$ cm$^{-3}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>InP Substrate</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Because the surface of sample Bol185 ([In] = 0.87) after MOVPE growth was rough due to the high indium content, only the emitter contact resistivity achieved from samples Bol183, Bol186 and Bol187 was investigated. The surface was treated in the solutions HCl:H$_2$O (1:9) and NH$_3$H$_2$O:H$_2$O (1:5) before the emitter contact
metallization. The emitter contact resistivity versus indium concentration for different surface treatment conditions is shown in Fig. 3.3.

Sample Bol183 ([In] = 0.498) treated with the HCl solution exhibits an average contact resistivity of \(3.1 \times 10^{-8} \Omega \cdot \text{cm}^2\), which is \(\sim 5 \times\) lower than that of an emitter cap layer structure with the same In concentration and a doping level of \(1 \times 10^{19} \text{cm}^{-3}\). The samples with an In concentration of \([\text{In}] = 0.498\) show a higher contact resistivity than those with a compressive strained InGaAs layer. As extensively discussed above, for higher doping and In concentrations, a lower contact resistivity is expected. Sample Bol183 and Bol187 were chosen for the collector and the emitter contact, respectively.

![Figure 3.3](image.png)

*Figure 3.3  Contact resistivity as a function of In content with two different surface treatments, HCl:H\(_2\)O (1:9), and NH\(_3\).H\(_2\)O:H\(_2\)O (1:5), respectively.*

### 3.1.1.2 Emitter Contact Resistivity Improvement by Surface Treatment

Surface treatment is of pivotal importance for the fabrication of reliable Ohmic contacts. In order to find the surface treatment leading to the lowest emitter and collector contact resistivity, we cleaved four pieces from a wafer containing a DHBT structure with an emitter cap layer which is the same as that of sample Bol187.
Before the contact metallization step, each of the four samples was subjected to different surface treatments, as listed in Table 3.2. Either the ultraviolet ozone cleaning system (UVOCS) or the oxygen plasma asher system has to be used to remove the resist residuals from the surface after the lithography step. The maximum applied RF power during the plasma ashing was 150 W because a power larger than 200 W results in surface damage [54]. The mesas for the TLM structures were formed by etching the emitter down to the base.

The total resistance plotted versus the contact separation in the transmission line-pattern is shown in Fig. 3.4 for each sample. The slope of the linear extrapolation is nearly the same for all samples, indicating they all have the same sheet resistances.

Table 3.2 Surface treatment conditions before contact metallization.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Surface Treatment Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample #1</td>
<td>UVOCS 1 minute + HCl:H₂O (9:81) 30 s + rinse 1 minute</td>
</tr>
<tr>
<td>Sample #2</td>
<td>UVOCS 1 minute + NH₃.H₂O:H₂O (1:10)10 s + no rinse</td>
</tr>
<tr>
<td>Sample #3</td>
<td>Asher (73 sccm 150 W 30 s + 100 W 30 s) + HCl:H₂O (9:81) 30 s + rinse 1 minute</td>
</tr>
<tr>
<td>Sample #4</td>
<td>Asher (73 sccm 150 W 30 s + 100 W 30 s) + NH₃.H₂O:H₂O (1:10) 10 s + no rinse</td>
</tr>
</tbody>
</table>

The vertical intercept obtained from an extrapolation of the curves to zero spacing then corresponds to twice the total contact resistances ($2R_C$). Samples #3 and #1 respectively show the lowest and highest contact resistivity. The contact resistivity of the four samples is summarized in Fig. 3.5. The UVOCS treated samples (samples #1 and #2) exhibit a higher contact resistivity than those treated with oxygen plasma (samples #3 and #4). UV-ozone has been reported to enhance the effective Schottky barrier height [55], [56]. Sample #3 exhibits a lower contact resistivity than sample #4, because the HCl used for sample #3 removes the non-stoichiometric native oxides or contained OH groups more efficiently. Samples #1 and #2 were both exposed to UV-ozone for one minute, and stoichiometric oxides were formed on the surfaces. Diluted ammonium hydroxide is probably more efficient to remove this oxide than diluted HCl, since sample #2 shows a higher contact resistivity as compared to sample #1.
3.1 Emitter Optimizations

Other researchers achieved contact resistivity in the order of $10^{-9} \, \Omega \cdot \text{cm}^2$ on $n$-type lattice-matched InGaAs with similar surface treatment consisting of UV-ozone followed by a dip in ammonium hydroxide [57]. Further examinations on the interface (e.g. Auger electron spectroscopy, X-ray photon spectroscopy) need to be done to correlate the surface composition resulting from the treatments with the contact resistivity. These analytical techniques for sub-monolayer detection are usually limited due to the surface contamination occurring before or during the analysis. Despite the potential usefulness of these techniques, the surface characterization remained beyond the scope of our work. The surface treatment applied to sample #3 was chosen for the real transistor fabrication process.

![Figure 3.4](image)

*Figure 3.4*  Total resistance as a function of space width (2, 4, 6, 10, 100 µm, respectively) between the transmission lines for different surface preparation conditions.
3.1.1.3 Annealing of the Emitter Contacts

The above mentioned emitter contacts were not subject to any thermal annealing. Rapid thermal annealing (RTA) is utilized to further improve the Ohmic contacts. In a standard triple-mesa process, the emitter, base and collector contacts are deposited in sequence in different steps. In order to achieve a low contact resistivity on InGaAs, both the emitter and collector contacts have to be annealed at temperatures above 250 °C. However, if this is feasible for the first deposited emitter contact, the annealing procedure applied to anneal the collector metal implies automatically an additional annealing of the base and emitter contacts. An annealing temperature above 180 °C produces metal diffusion through the GaAsSb base layer (see page 77). As a consequence, the collector and base contacts were not annealed, and the PMMA resist in the air-bridge process was baked at 180 °C to protect the base material.

In order to find out the optimal annealing temperature for the emitter contact resistivity, sample #4 was further cleaved into four pieces and annealed at several conditions in the RTA system. Each sample was respectively annealed at 250 °C, 270 °C, 300 °C, 350 °C, respectively, for one minute in a N₂ atmosphere. Contact
resistivity of sample #4 was plotted versus annealing temperature in Fig. 3.6. It was found that the contact resistivity decreases with increasing temperature in the range between 20 °C and 270 °C. Above 270 °C, the contact resistivity increases by raising the temperature. 270 °C was thus chosen as the annealing temperature for the emitter contact.

The emitter contact resistivity before and after the annealing at 270 °C is shown in Fig. 3.7. Sample #3 still exhibits a contact resistivity of $5 \times 10^{-9} \, \Omega \cdot \text{cm}^2$ which is the lowest.

![Figure 3.6](image)

Figure 3.6  Emitter specific contact resistivity versus annealing temperature.
In summary, the experiments show that the doping concentration strongly influences the contact resistivity. The increasing of the doping level from $1 \times 10^{19}$ cm$^{-3}$ to $4 \times 10^{19}$ cm$^{-3}$ results in a contact resistivity decrease from $\sim 10^{-7}$ $\Omega$·cm$^2$ to $\sim 10^{-8}$ $\Omega$·cm$^2$. The surface treatment conditions also control the contact resistivity. The surface treatment consisting of oxygen plasma and a dip in diluted HCl lowers the contact resistivity down to $\sim 5 \times 10^{-9}$ $\Omega$·cm$^2$. Finally, a temperature of 270 °C was found to lead to the lowest emitter contact resistivity.

### 3.1.2 Optimization of the Emitter Epilayer Structure

#### 3.1.2.1 Choice of the Emitter Material: GaInP Emitter

A wide band gap emitter material with a low conduction band and a high valence band offset is required to achieve a favorable gain in DHBTs and reduce the hole back injection at the Emitter/Base (E/B) interface. For DHBTs with GaAsSb bases, AlInAs, GaInP and InP are three potential candidates for the emitter material. Up to the present, little work has been published reporting on the suitability of an emitter material.
material in type-II DHBTs. Some experimental details concerning this topic are discussed in this section.

DHBT epilayers with the InP and GaInP emitters were grown by a MOVPE system in the ETH FIRST laboratory while the structures with an AlInAs emitter were grown by molecular beam epitaxy (MBE) system at Agilent.

DHBTs with these three emitters have similar epilayer structures. Transistors with the emitter areas of $20 \times 30 \ \mu m^2$, $40 \times 40 \ \mu m^2$ and $80 \times 80 \ \mu m^2$ were fabricated by the QHBT process described in Chapter 2. The base sheet resistances vary from 1100 to $3300 \ \Omega/\square$ for the DHBTs with InP, GaInP emitters while the base sheet resistances for the DHBTs with AlInAs emitter vary from 890 to $1500 \ \Omega/\square$. 

![Diagram](image-url)
Figure 3.8  Representative Gummel plots of the devices with the emitter area of 20 × 30 µm² and with (a) an AlInAs and (b) a GaInP emitter.

Figure 3.8(a) and (b) show the Gummel characteristics of the DHBTs with an AlInAs and a GaInP emitter, respectively and with emitter areas of 20 × 30 µm². The ideality factors for the base and collector currents of DHBTs with AlInAs emitter are $n_B = 1.35$ and $n_C = 1.02$, respectively, whereas for DHBTs with GaInP emitter, the base and collector ideality factors are $n_B = 1.66$ and $n_C = 1.01$, respectively.

Figure 3.9  Band alignments of the materials (a) AlInAs, InP and GaAsSb and (b) GaInP, InP and GaAsSb.
Figure 3.10 Gain versus collector current from devices with the emitter area of 20 × 30 µm² and with (a) an AlInAs and (b) a GaInP emitter.

The conduction band edge of Al₀.₄₈In₀.₅₂As is 0.14 eV higher than that of GaAs₀.₅₁Sb₀.₄₉, as shown in Fig. 3.9 [58]. On the other hand, the Ga₀.₂₄In₀.₇₆P conduction band lies 0.05 eV below that of GaAs₀.₅₁Sb₀.₄₉ [59]. A lower current gain is thus expected in DHBTs with a GaInP emitter, because the emitter/base junction incorporates a blocking barrier for electrons.

Fig. 3.10 shows the gain as a function of the collector current for DHBTs with GaInP, AllInAs emitters and with the emitter area of 20 × 30 µm². The gain of DHBTs containing an AllInAs emitter is lower over the entire collector current region. This result is however contrary to expectations mentioned above.

The gain measured at the collector current of 85 mA as a function of base sheet resistance for various DHBTs with the emitter area of 20 × 30 µm² is shown in Fig. 3.11. The DHBTs with GaInP and InP emitters exhibit the highest and lowest gain, respectively.
Figure 3.11 Gain plotted versus the base sheet resistance for DHBTs with InP, AlInAs and GaInP emitters. The DHBT base layers have a uniform doping and composition. Dashed lines are trend lines to guide the eye.

For a better understanding of how the gain depends on the emitter material, the surface recombination current was studied. The total base current can be expressed by

$$\frac{J_C}{\beta} = \frac{I_{B\text{I}}}{A_E} + \frac{I_{\text{SURF}}}{A_E} = (J_{BQN} + J_{B\text{SCR}} + J_{Bp}) + K_{\text{SURF}} \frac{P_E}{A_E} \quad [60] \quad (3.2)$$

where $\beta$ is the DC common-emitter current gain ($I_C/I_B$ at $V_{CB} = 0$ V), $J_C$ is the collector current density, $I_{B\text{I}}$ and $I_{\text{SURF}}$ are the intrinsic and the extrinsic base recombination current components, respectively. $K_{\text{SURF}}$ thus represents the surface recombination rate (surface recombination current divided by emitter periphery). $J_{BQN}$, $J_{B\text{SCR}}$ and $J_{Bp}$ respectively are the base bulk quasi-neutral, space charge and back-injection recombination base current contributions. Because of the very large $\Delta E_V$, we assume $J_{Bp} = 0$. $A_E$ and $P_E$ represent the emitter area and periphery.
Figure 3.12  Emitter size dependence of $J_C/\beta$ for DHBTs with GaInP emitter and AlInAs emitter.

By plotting the measured $J_C/\beta$ characteristics of large area devices (with the emitter sizes of $20 \times 30 \, \mu m^2$, $40 \times 40 \, \mu m^2$, $80 \times 80 \, \mu m^2$) as a function of the emitter periphery-to-area ratio $P_E/A_E$ (see Fig. 3.12), the surface recombination rate $K_{\text{SURF}}$ is obtained from the slope of a linear fit through the data, and the intrinsic recombination current density $J_{\text{BI}}$ corresponds to the extrapolated ordinate at $P_E/A_E = 0$ (under the reasonable assumption that as $A_E \to \infty$ periphery effects become negligible).

Fig. 3.13 shows a plot of the normalized emitter periphery surface recombination rate $K_{\text{SURF}}$ versus the base sheet resistance at the collector current of 1 kA/cm² for the DHBTs with InP, GaInP and AlInAs emitters. DHBTs with AlInAs emitter showed a lower surface recombination rate than DHBT with InP emitter, but a higher $K_{\text{SURF}}$ than devices with GaInP emitter.

The normalized emitter periphery surface current $K_{\text{SURF}}$ and the intrinsic $J_{\text{BI}}$ (the $y$-intercept at $P_E/A_E=0$) of the DHBTs with both AlInAs and GaInP emitters were investigated. $K_{\text{SURF}}$ and $J_{\text{BI}}$ are higher for DHBTs with an AlInAs emitter as compared to DHBTs with a GaInP emitter. In order to exclude the surface recombination current effect, we have calculated the expected gain from an infinitively large device.
Figure 3.13 Surface recombination rate as a function of base sheet resistance at the collector current density of 1 kA/cm$^2$ for all the devices with the three different emitters: InP, AlInAs and GaInP. The base layer of all the DHBT structures has uniform doping levels and As concentrations. Dashed lines are trend lines to guide the eye.

(P$_E$/A$_E=0$) at a collector current of 6 mA. The two data points are also shown in Fig. 3.10 for each transistor. The gain of the DHBT with an AlInAs emitter is still lower than that with a GaInP emitter, even for P$_E$/A$_E=0$. In order to understand this result, the current components leading to the intrinsic current density must be considered. Since the bases are the same for both transistors, the quasi-neutral current is the same. The difference in the intrinsic current between the two devices arises thus from the space charge and back inject current densities.

The electron mobility of AlInAs ($\mu_n = 700$ cm$^2$/V·s) is much lower than that of GaInP ($\mu_n > 1000$ cm$^2$/V·s). As a consequence, the electrons are expected to have a higher recombination rate in the AlInAs emitter space charge region. Moreover, the lower valence band discontinuity between AlInAs and GaAsSb (Fig. 3.9) might eventually produce a higher $J_{BP}$, and thus a lower gain for transistors provided with an AlInAs emitter.
In conclusion, we ascribe the lower gain of DHBTs with an AllInAs emitter to the increase of the surface recombination current, the space charge recombination current and the back injection current. GaInP was chosen as a part of the emitter material, since transistors with a GaInP emitter exhibit the highest current gain. Since the composition and doping level of the ternary emitter material affects the band alignment at the emitter-base junction, optimization of the emitter Ga concentration and doping level is discussed in the following paragraphs.

### 3.1.2.2 Choice of the Emitter Doping Level

In order to increase the current gain cut-off frequency \( f_T \) in aggressively-scaled DHBTs with already low base and collector delay times \( \tau_B \) and \( \tau_C \), the emitter doping level should be chosen to minimize the emitter charging time and the emitter resistance without unduly increasing the emitter capacitance. The pertinent trade-offs are summarized by the usual expression for the current gain cut-off frequency of a bipolar transistor where \( \tau_B \) and \( \tau_C \) are the base and collector delay times, \( I_C \) is the collector current, \( C_{BE} \) is the base-emitter capacitance, \( C_{CB} \) is the collector-base capacitance, and \( R_{EX} \) and \( R_C \) are the emitter and collector resistances, respectively. With short delay times \( \tau_B \) and \( \tau_C \), the impact of the various \( RC \) terms in Eqn. (3.3) becomes increasingly important to eventually dominate as device dimensions reach into the deep sub-micrometer regime. Clearly, \( R_{EX} \), \( C_{BE} \) and \( I_C \) all depend on the emitter doping. Increasing the emitter doping level decreases \( R_{EX} \), and helps to achieve higher \( I_C \) [61], but it also increases the emitter/base junction capacitance \( C_{BE} \).

\[
f_T = \frac{1}{2\pi} \left( \frac{1}{\tau_B + \tau_C} + \frac{kT}{qI_C} \left( C_{BE} + C_{CB} \right) + \left( R_{EX} + R_C \right) C_{CB} \right)
\]

(3.3)

The emitter optimization therefore involves design trade-offs which may conceivably be specific to the material system under consideration. The effect of emitter doping level in HBTs has been extensively studied for (Al,Ga)As/GaAs HBTs which showed improved current gains under low injection conditions for higher emitter doping levels [13]. The conclusions reached with (Al,Ga)As/GaAs HBTs however do not necessarily apply to other material systems: for instance, the gain characteristics of InP/GaInAs HBTs were reported to be independent of the emitter doping level [62].
The InP/GaAsSb material system is sufficiently different from AlGaAs/GaAs and InP/GaInAs to warrant an investigation of the impact of emitter doping levels on the DC and RF performances of InP/GaAsSb–based DHBTs. We show that InP/GaAsSb emitters do in fact behave differently from their AlGaAs/GaAs or InP/GaInAs counterparts.

Transistors were implemented from wafers differing only in their emitter doping levels of $3 \times 10^{17}$ cm$^{-3}$ (sample A) and $6 \times 10^{16}$ cm$^{-3}$ (sample B) by optical contact lithography. The measured base sheet resistances for both samples were practically identical (A: 1000 Ω/sq; B: 1030 Ω/sq). Fig. 3.14 shows room temperature Gummel characteristics for the DHBTs of samples A and B with a $0.4 \times 5.5$ µm$^2$ emitter area.

The collector current is nearly identical for both emitter doping levels, and both show a collector current ideality factor $n_C = 1.04$. The collector currents differ only under very high-injection conditions, where the higher emitter doping (sample A) supports higher current densities, as is to be expected [61]. The collector current overlap at lower and medium currents is of course to be expected, because electrons are

![Gummel plot for DHBTs with the emitter area of $0.4 \times 5.5$ µm$^2$ from samples A and B, with respective emitter doping levels of $3 \times 10^{17}$ cm$^{-3}$ and $6 \times 10^{16}$ cm$^{-3}$.](image-url)
thermally injected from the composite InP/(Ga,In)P emitter into the GaAsSb base: under low-injection, the collector current should be entirely determined by the quantity $n_{Bi}^2/N_{BA}$, where $n_{Bi}$ is the intrinsic carrier concentration in the GaAsSb base, and $N_{BA}$ is the base acceptor concentration. The $J_C$ overlap in Fig. 3.14 provides another indication (beyond the identical base sheet resistance values) that both base layers are effectively identical.

Because the base layers in samples A and B are nominally identical, the Auger, Shockley-Read-Hall (SRH) and band-to-band recombination rates in the GaAsSb base layer are expected to be the same for both samples. A priori, one would expect identical base currents in both devices, but Fig. 3.14 shows that a higher emitter doping results in a higher base current at low $V_{BE}$ biases, while the base currents nearly merge for high-injection conditions ($V_{BE} > 0.75$ V). Fig. 3.14 shows that the emitter doping level affects the base current ideality factor, with $n_{B(A)} = 1.54$ and $n_{B(B)} = 1.23$. The increased emitter doping enhances the recombination processes involving the emitter region. The higher emitter doping results in a lower current gain at low currents, but the situation is reversed for higher injection levels $J_C > 1.7$ mA/µm$^2$, as shown in Fig. 3.15. The current gain does not scale proportionally with the emitter doping level (i.e. by a factor of 5) as a simple bipolar transistor theory would suggest. This reflects that recombination mechanisms are dependent on the emitter doping. Fig. 3.16 contrasts the emitter/base diode characteristics of 40 × 40 µm$^2$ emitter DHBTs (used to minimize low-current fluctuations and potential edge effects): the higher emitter doping level (sample A) results in an excess current at low forward biases, as well as in an excessive reverse diode leakage. similar features in the I-V characteristics of silicon bipolar transistors are associated with emitter/base tunneling [63] [64]. Next, we examine the nature of recombination mechanisms in the context of the emitter doping by experimentally separating recombination in the intrinsic emitter and at its periphery.

In order to understand how the differences in recombination arise as a function of emitter doping, we have studied the base current makeup by resolving the recombination current components arising at the emitter periphery and in the intrinsic region of the transistor (that is, directly under the emitter) as discussed in Section 3.1.2.1, by characterizing the emitter-size dependence of the current gain (i.e. emitter-size effects, ESEs) as a function of the collector current density $J_C$. Fig. 3.17 show
that the higher emitter doping level leads to higher recombination currents, both at the emitter periphery \( (K_{\text{SURF}}) \) and in the intrinsic region under the emitter contact \( (J_{\text{BI}} = I_{\text{BI}}/A_{E}) \).

![Graph showing Gain as a function of collector current density for devices with the emitter area of 0.4 × 5.5 μm² from samples A and B, with respective emitter doping levels of 3 × 10^{17} \text{cm}^{-3} \text{ and } 6 \times 10^{16} \text{cm}^{-3}.]

**Figure 3.15** Gain as a function of collector current density for devices with the emitter area of 0.4 × 5.5 μm² from samples A and B, with respective emitter doping levels of 3 × 10^{17} \text{cm}^{-3} \text{ and } 6 \times 10^{16} \text{cm}^{-3}.
Figure 3.16  Emitter-base diode I-V characteristics of devices with the emitter area of 40 × 40 µm². The higher emitter doping results in excess forward bias currents as well as a higher reverse bias diode leakage.
Figure 3.17  (a) Intrinsic recombination and (b) surface (periphery) recombination current densities as a function of collector current density for samples A and B, with respective emitter doping levels of $3 \times 10^{17}$ cm$^{-3}$ and $6 \times 10^{16}$ cm$^{-3}$. The 1:1 lines indicate increases proportional to $J_C$. Surface recombination (intrinsic) increases faster (slower) than $J_C$.

As the collector current density increases, the difference between the recombination properties with the two emitter doping levels is reduced. This is consistent with the Gummel characteristics of Fig. 3.14 which show nearly identical base currents under high-injection conditions (high $V_{BE}$). It is interesting to note in Fig. 3.17 that both $J_{BI}$ and $K_{SURF}$ increase (nearly) exponentially with $J_C$, albeit at different rates: for low current densities, the intrinsic base recombination current $J_{BI}$ increases more slowly than $J_C$, while recombination at the periphery $K_{SURF}$ rises faster than $J_C$ (the 1:1 lines in Fig. 3.17 correspond to recombination current increases in proportion to $J_C$). The collector current ideality factor is practically equal to unity, as shown in Fig. 3.14. Fig. 3.17(a) reveals that the intrinsic recombination current $J_{BI}$ ideality factor depends on the emitter doping level, with $n_{BI} \approx 1.58$ for $N_E = 3 \times 10^{17}$ cm$^{-3}$ while $n_{BI} \approx 1.32$ for $N_E = 6 \times 10^{16}$ cm$^{-3}$. These values are in good general agreement with the base current ideality factors as shown in Fig. 3.14: it will be shown later (Fig. 3.19) that $J_{BI}$ is the dominant recombination current for $0.4 \times 5.5 \, \mu m^2$ devices when $J_C < 10^{-3}$ mA/µm$^2$, and the agreement reflects this fact. Small discrepancies arise because of two reasons:
i) $J_{BI}$ (and $K_{SURF}$) are derived from measurements involving many large area devices, and ii) the base current ideality factors in Fig. 3.14 were obtained by fits including higher current densities, and thus reflect “more ideal” currents at higher $V_{BE}$ values.

Fig. 3.17 reveals much about the internal operation of the transistor, and deserves further consideration. We first focus on the difference in intrinsic recombination density between samples A and B as a function of $J_C$. In Fig. 3.18, we plot the relative variation of intrinsic recombination current density $[J_{BI(A)} - J_{BI(B)}]/J_{BI(A)}$ as a function of $J_C$ to find that the difference is greatest under low injection conditions (i.e. at low $V_{BE}$), and that the intrinsic recombination becomes identical in both samples at high current levels. Because the base layers are nominally identical in composition, doping and thickness (as confirmed by sheet resistance and Gummel characteristic measurements), the increased recombination in the highly-doped emitter (sample A) must arise either from the emitter-base junction proper, or from its immediate vicinity. In the framework of Eqn. (3.2), the intrinsic recombination current must therefore correspond to the $J_{BSCR}$ component. We consider potential mechanisms for intrinsic recombination current below, after considering the relative roles of intrinsic and periphery recombination as a function of $J_C$ next.

Fig. 3.17 can be used to determine the relative importance of the intrinsic and surface recombination currents as a function of injection conditions. Fig. 3.19 shows the ratio of surface recombination current ($K_{SURF}P_E/A_E$) to $J_{BI}$ again plotted as a function of $J_C$ for $0.4 \times 5.5 \, \mu m^2$ emitter devices. The plot shows that intrinsic recombination clearly dominates under low injection conditions, but that under the high-injection conditions associated with high-speed operation, surface recombination at the emitter periphery largely dominates. The crossover in the dominant recombination mechanism is a consequence of the steeper rise of periphery recombination compared to intrinsic recombination with increasing $J_C$ (or $V_{BE}$) seen in Fig. 3.17. To the best of our knowledge, the bias dependence of the recombination mechanisms and the associated shift from intrinsic recombination dominated performance to surface recombination dominated performance with increasing $J_C$ has not been reported before. We note that the dominance of periphery recombination at high current levels was simulated by Tiwari and Frank in their detailed numerical study of AlGaAs/GaAs HBTs [61]. This feature is a natural consequence of the saddle-point potential arising at the intersection of the emitter mesa and the extrinsic base surface. As such, periphery
surface recombination can be expected to dominate the high current performance of all mesa type HBTs, regardless of surface passivation. It was pointed out by Tiwari and Frank [61], but it is still not widely appreciated, that a consequence of the two-dimensional nature of electron transport in the saddle-point potential (and the resulting direct injection of electrons onto the extrinsic base surface), is an emitter size dependence of the current gain even when the surface recombination velocity is set to $S = 0$ cm/s (i.e. with a perfectly passivated surface, electrons injected onto the extrinsic base surface recombine at the base Ohmic contact).
Figure 3.18  Relative difference in intrinsic recombination currents for samples A and B. As the current density increases, intrinsic recombination levels become identical in both samples.

Figure 3.19  Surface (periphery) to intrinsic recombination current ratio as a function of collector current density for 0.4 × 5.5 µm² emitter devices.
Band diagrams for our InP-GaInP/GaAsSb DHBTs were simulated under equilibrium and operating conditions using the *Synopsis* TCAD numerical tool. The equilibrium band diagram for the emitter-base junction in Fig. 3.20(a) indicates that quantum-mechanical tunneling of electrons from the InP emitter toward the GaAsSb valence band is likely at low applied $V_{BE}$ since the energy gap at the E/B junction is approximately equal to that of the GaAsSb base ($\sim 0.72$ eV). The role of E/B tunneling in silicon bipolar transistors has been studied in depth: tunneling-related non-idealities become important when the equilibrium depletion layer width becomes narrower than 40 nm, increasing by roughly 2.5 orders of magnitude for each 5 nm reduction in depletion layer width [64]. Noting that the direct tunneling distance indicated in Fig. 3.20(a) is of the order of 30-35 nm, and that the electron effective mass in InP is significantly lower than that in silicon ($m_{\text{InP}}^* = 0.077m_0$ vs. $m_{\text{Si}}^* = 0.19m_0$), suggests that emitter-base tunneling, either direct or defect-assisted, plays a role in the junction non-idealities observed at low injection levels. A higher emitter doping level results in a higher zero-bias electric field in the emitter, and a $\sim 5$ nm shorter direct tunneling distance in the present case, as indicated in Fig. 3.20(a).

Figure 3.16 shows measured emitter/base diode characteristics for samples A and B: the excess forward current and the softer reverse leakage characteristics shown by sample A are reminiscent of those observed in silicon diodes in the presence of tunneling, be it direct or defect-assisted [64]. Similar results have also been previously reported for Si/SiGe/Si HBTs [65], where at low current levels the tunneling current showed an increase with doping concentration in the lightly-doped side of the junction. We are at this time unable to resolve whether the intrinsic recombination current mechanism occurs through pure tunneling, or whether it involves defect-assisted tunneling. One possibility could be that the doping of the InP-GaInP emitter introduces some defects near the emitter-base junction, because undoped InP-(Al)GaAsSb heterojunctions grown in the same MOVPE reactor show long recombination lifetimes, as determined by time-resolved pump-probe measurements [66]. Regardless of their exact origin, the low-level reverse leakage shown in Fig. 3.16, and the intrinsic recombination current $J_{\text{RI}}$ have little impact on the high-speed operation of transistors in comparison to the much stronger periphery recombination at high biases. From now on, we therefore focus on the high-level operation.
Fig. 3.20(b) shows the band diagram for samples A and B at a collector-emitter bias of $V_{CE} = 1$ V and at a current density of $J_C = 5.8$ mA/µm$^2$. With a high $V_{BE}$, direct emitter-base tunneling no longer plays a role because the emitter conduction band is raised far above the base valence band: no available final GaAsSb valence band states are available for electrons tunneling from the InP/GaInP emitter conduction band, although tunneling to the base can still be mediated by defects in the vicinity of the heterojunction. Fig. 3.20(b) also shows that the emitter conduction band energy for the emitter doped at $3 \times 10^{17}$ cm$^{-3}$ (sample A) shows less of an upward bulge than that of sample B due to its higher emitter doping level. The bulge in the emitter band diagrams is due to the traveling electron space charge, and was coined “alloy potential” by Tiwari and Frank in their numerical analysis of the operation of AlGaAs/GaAs HBTs. The difference between the heavily and lightly-doped band diagrams is of the order of $kT$ due to the increased electron traveling space charge effects in the lightly-doped emitter (i.e. $n > N_D$). Consequently, the lightly-doped emitter supports a reduced maximum collector current density in comparison to the heavily-doped emitter, and it shows a lower DC current gain than that of sample A for a given base current in the higher current density region. The lightly-doped emitter also clearly features a higher emitter dynamic resistance $r_e = \partial V_{BE}/\partial I_C$, as shown in Fig. 3.14.

The microwave performance of our DHBTs as a function of emitter doping has been assessed over the 45 MHz to 40 GHz frequency band using an HP8510C vector network analyzer and an off-wafer line-reflect-reflect-match (LRRM) calibration substrate. Fig. 3.21(a) shows the short-circuit current gain $|h_{21}|^2$ as a function of frequency for both samples biased at $V_{CE} = 1$ V and $J_C = 10$ mA/µm$^2$ (with a measured $V_{BE} = 0.871$ V for sample A, and 0.883 V for sample B) for devices with a $0.4 \times 5.5$ µm$^2$ emitter area. The current gain cutoff frequency $f_T$ was determined by a $–20$ dB/dec extrapolation of $|h_{21}|^2$, yielding peak values $f_{TA} = 355$ GHz and $f_{TB} = 324$ GHz for samples A and B, respectively.
Figure 3.20  (a) Equilibrium band diagram at the emitter-base junction of our composite-emitter InP-GaInP/GaAsSb DHBTs. The higher emitter doping level results in a higher electric field in the emitter. The diagram suggests that emitter-base tunneling is a possible mechanism for the excess currents arising at low base-emitter biases. (b) Band diagram under high-current operation with $V_{CE} = 1 \, \text{V}$ and $J_C = 5.8 \, \text{mA/µm}^2$. 
The evolution of $f_T$ versus the collector current density $J_C$ is shown in Fig. 3.21(b). For both samples, $f_T$ increases with increasing the collector current density $J_C$, and exhibits a maximum before rolling off at collector current densities $J_C > 10$ mA/µm² due to the onset of the Kirk effect in the collector [67]. At low currents, both devices offer similar performances because of the dominant influence of the $kT/I_C$ term in Eqn. (3.1). The emitter doping level, as expected, does not significantly affect the Kirk current density (which is primarily determined by the collector doping and thickness). Over the whole current density range, sample A shows higher cut-off frequencies as compared to sample B, and the performance difference grows at higher current densities, nearing 100 GHz at $J_C = 20$ mA/µm².

Deeper insight into the device microwave performance can be gained by considering the behavior of $R_E$, $C_{BE}$, and $C_{BC}$ extracted from the measured S-parameters according to the approach of [68]. A higher emitter resistance is expected for sample B in light of the lower doping level compared to sample A. Fig. 3.22 shows the total emitter resistance for both samples, as well as the room temperature dynamic emitter resistance $r_e = nkT/I_C$ included (with $n = 1$) as a comparison of the relative contributions. The higher emitter doping shows a resistance that is on average 0.76 Ω (1.67 Ω·µm²) lower. The emitter resistance reduction with higher emitter doping is 4-5× smaller than what one might expect based on straightforward resistivity calculations, indicating that carrier transport near the emitter-base heterojunction under high-injection conditions is far from Ohmic in nature, and that the emitter doping near the base in fact has a relatively weak impact on the emitter resistance. This view is supported by numerical simulations: under the bias conditions corresponding to Fig. 3.20(b), the free electron density in the graded GaInP emitter already significantly exceeds the emitter doping level in both samples A and B at $J_C = 5.8$ mA/µm² and therefore perturbs the band diagram as shown in the figure because $n > N_E$. 
Figure 3.21  (a) $|h_{21}|^2$ as a function of frequency for 0.4 × 5.5 μm$^2$ devices. (b) Current gain cutoff frequency extracted from S-parameter measurements between 45 MHz and 40 GHz plotted against collector current density $J_C$. 
3.1 Emitter Optimizations

Figure 3.22 Total RF emitter resistance extracted from S-parameters. For reference, the room temperature emitter dynamic resistance $kT/qIC$ is also shown.

Figure 3.23 Extracted emitter-base and base collector capacitances as a function of collector current density $J_C$. 
Fig. 3.23 shows the extracted values of $C_{BE}$ and $C_{BC}$ as a function of $J_C$. Also as expected, the more highly-doped emitter shows a higher base-emitter capacitance $C_{BE}$, until the values eventually merge for current densities far exceeding the peak $f_T$ limit of 10 mA/µm². Both samples show comparable values of $C_{BC}$ over most biases, but it is interesting to note that $C_{BC}$ rises much faster for the lightly-doped emitter (sample B) for $J_C > 15$ mA/µm². We tentatively ascribe this behavior to the higher base-emitter bias $V_{BE}$ required for the lightly-doped emitter to source a given current density under high drive conditions. Because our RF measurements are carried out with a fixed $V_{CE} = 1$ V, a higher $V_{BE}$ for sample B leaves a weaker collector-base reverse bias, thereby enhancing collector charge storage effects under very high drive levels.

In conclusion, it was shown that a higher emitter doping decreases the low current gain, but that the current gain under high-injection conditions is higher. The effect of emitter doping was further characterized through measurements of the emitter-size effect, which showed that under low drive levels, the device current gain is dominated by recombination occurring directly under the emitter contact. The intrinsic recombination is in fact largely responsible for the non-ideality of the base current in our sub-micrometer devices. At high drive levels, the dominant recombination mechanism is surface injection at the emitter periphery. To the author’s knowledge, the bias dependence of the location of recombination in a DHBT was never reported before. It was also shown that both intrinsic and periphery recombination increase with emitter doping level.

In terms of microwave performance, the higher emitter doping results in a peak $f_T = 355$ GHz that is to be compared to 324 GHz for the lightly-doped emitter, as well as a growing performance advantage at higher current densities. The lightly-doped emitter shows a reduced emitter capacitance but a slightly higher emitter resistance, indicating that transport near the emitter-base junction under high-level injection is not Ohmic in nature, and that the emitter doping near the base in fact has relatively weak impact on the emitter resistance.

The dependence of device performance upon the emitter doping level is therefore quite different from those observed in AlGaAs/GaAs and InP/GaInAs HBTs,
indicating that no universal emitter design strategy exists, *i.e.* the emitter design must be optimized for each different material system.

### 3.1.2.3 Choice of the GaInP Emitter Ga Concentration

As previously described, an increased emitter doping level leads to a decreased current gain when the transistors operate in the low bias region. In order to further improve the device current gain, transistors were fabricated from three wafers with structures differing only in the emitter Ga contents of 0 (sample A), 0.15 (sample B) and 0.24 (sample C). The emitter doping level is $6 \times 10^{16}$ cm$^{-3}$. The average doping of the 20 nm thick $p$-doped GaAsSb base layer is $8 \times 10^{19}$ cm$^{-3}$ with As concentration graded from 0.6 at the emitter side to 0.4 at the collector side. The 75 nm thick InP collector is nominally doped with silicon at $3 \times 10^{16}$ cm$^{-3}$. The effect of the emitter Ga concentration on the DC characteristics of large emitter area devices ($20 \times 30$ µm$^2$, $40 \times 40$ µm$^2$ and $80 \times 80$ µm$^2$), and on the RF characteristics of small emitter area devices ($0.45 \times 9.5$ µm$^2$) was investigated. The base width of the small emitter area devices ($0.45 \times 9.5$ µm$^2$) was designed to be 0.5 µm.

Figure 3.24 shows the equilibrium band diagram for Ga$_x$In$_{1-x}$P emitter compositions of $x = 0$, 0.15, and 0.24. The effect of an increased Ga mole fraction is to fill in the “Type-II” $\Delta E_C$, gradually eliminating the conduction band notch at the E/B junction. Electrons are injected more easily from the emitter to the base with the elimination of the conduction band discontinuity. Figure 3.25 shows the typical gain as a function of collector current from Gummel measurement on devices with the emitter area of $20 \times 30$ µm$^2$ for the three samples. As the current increases, the gain of the transistors increases for all the three samples. As expected, sample C shows the highest current gain through the whole current range.

In order to further understand how the differences in recombination arise as a function of Ga concentration, we studied the base current by resolving the recombination current components arising at the emitter periphery and in the intrinsic region of the transistor (that is directly under the emitter), by characterizing the emitter-size dependence of the current gain (i.e. emitter-size effects, ESEs) as a function of the collector current density $J_C$. By plotting the measured $J_C/\beta$ characteristics of large emitter area devices ($20 \times 30$ µm$^2$, $40 \times 40$ µm$^2$, $80 \times 80$ µm$^2$) as a function of the
Figure 3.24 Equilibrium band diagram around the E/B junction of GaInP/GaAsSb/InP DHBTs. The addition of Ga to the InP emitter gradually fills in the “type-II” band discontinuity, achieving a nearly smooth conduction band profile for \( x = 0.24 \).

Figure 3.25 Measured gain characteristics for various Ga emitter concentrations on 20 × 30 µm² DHBTs.
emitter periphery-to-area ratio $P_E/A_E$ (not shown), the surface recombination factor $K_{BSurf}$ is obtained from the slope of a linear fit through the data, and the intrinsic recombination current density $J_{Bl}$ corresponds to the extrapolated ordinate at $P_E/A_E = 0$ (under the reasonable assumption that as $A_E \rightarrow \infty$ periphery effects become negligible).

Fig. 3.26 represents the periphery surface recombination rate $K_{BSurf}$ as a function of Ga content. $K_{BSurf}$ is exponentially reduced with an increasing Ga mole fraction $x$. Fig. 3.27 shows the intrinsic current density as a function of Ga content. While the Ga content increases, the intrinsic current density decreases. This again is a reminiscence of the two-dimensional nature of electron transport in the saddle-point potential [61], which leads to the current gain dependence on the conduction band discontinuity.

![Figure 3.26](image)

**Figure 3.26** Emitter periphery surface recombination current component $K_{BSurf}$ extracted from emitter-size effect (ESE) measurements on multiple transistor sizes. The periphery recombination is exponentially decreased with increased emitter Ga content.
Chapter 3: Optimization of DHBT Structure Design and Fabrication Process

The microwave performance of our DHBTs as a function of Ga contents was assessed over the 45 MHz to 40 GHz frequency band using an HP8510C vector network analyzer and an off-wafer line-reflect-reflect-match (LRRM) calibration substrate.

Figure 3.28 shows the short circuit current gain $|h_{21}|^2$ and unilateral gain as a function of frequency for the three samples biased at $V_{CE} = 1$ V for devices with a $0.45 \times 9.5 \mu m^2$ emitter area. The current gain cutoff frequency $f_T$ was determined by a $-20$ dB/dec extrapolation of $|h_{21}|^2$, yielding peak values $f_{TA} = 318$ GHz, $f_{TB} = 348$ GHz and $f_{TC} = 387$ GHz for samples A, B and C, respectively. For the three samples, $f_T$ increases with increasing collector current density $J_C$, and exhibits a maximum before rolling off at collector current densities due to the onset of the Kirk effect in the collector [67]. Transistors with the emitter area of $0.45 \times 9.5 \mu m^2$ on sample C show lower Kirk current densities (8.0 mA/$\mu m^2$) than those transistors with the emitter area of $0.3 \times 11.5 \mu m^2$ on our standard in-house grown wafers (9.27 mA/$\mu m^2$). This is due to the collector current spreading [69]. With a smaller emitter width, the collector current spreading becomes more severe, and therefore the effective area of the
collector increases. It was also observed that transistors on sample C with the emitter area of $0.45 \times 9.5 \, \mu m^2$ exhibit $J_C = 8 \, mA/\mu m^2$ while those with the same emitter area on sample A and sample B exhibit lower Kirk current densities. With a lower Ga content, electrons encounter a higher energy barrier to be injected into the base at the E/B interface which increases recombination at the emitter periphery potential saddle point. It appears a larger amount of electrons are lost at the edge of the emitter for those transistors with lower Ga contents. The effective emitter area thus becomes smaller, and the collector current decreases. The maximum oscillation frequency $f_{MAX}$ for samples A, B and C are 186 GHz, 200 GHz and 209 GHz, respectively. Since the process is the same for all the three samples, the same base resistance and BC junction capacitance are to be expected. The variation of $f_{MAX}$ follows from the $f_T$ variation associated with the different emitter Ga content.

![Figure 3.28 Determination of $f_T$ and $f_{MAX}$ from 40 GHz VNA S-parameter measurements on $0.45 \times 9.5 \, \mu m^2$ devices with various emitter Ga contents.](image)

To summarize, the effect of the emitter Ga content on the DC current gain and the cut-off frequency of InP/GaAsSb DHBTs with a $0.45 \times 9.5 \, \mu m^2$ emitter area was investigated. It was shown that the DC current gain increases as the Ga content increases. Significant reductions in both the emitter surface periphery recombination
rate and the intrinsic recombination current were observed as the Ga content increases. At higher current densities, the current-gain cut-off frequency increases as the Ga increases. The elimination of the conduction band discontinuity helps to improve transistor performances.

Transistors with an emitter area of $0.45 \times 9.5 \, \mu m^2$ were fabricated by optical contact lithography. The GaInP in the composite emitter has a composition of $x = 0.24$ and a doping level of $3 \times 10^{17} \, cm^{-3}$. The base contact width was also designed to be 0.5 µm to reduce the base/collector capacitance. A cut-off frequency $f_T$ of 401 GHz was obtained as shown in Fig. 3.29. This is the highest $f_T$ among devices fabricated by optical contact lithography within this work. The above mentioned Ga concentration and doping level were thus chosen for GaInP emitter in InP/GaAsSb DHBTs.

![Figure 3.29](image)

Figure 3.29 |$h_{21}$|$^2$ as a function of frequency for devices with the emitter area of $0.45 \times 9.5 \, \mu m^2$. 
3.2 Base Optimizations

3.2.1 Base Contact Resistivity Optimization

3.2.1.1 Annealing Effect

In order to improve the maximum oscillation frequency $f_{\text{MAX}}$ of DHBTs, we have to reduce the total base resistance, which is the sum of the base spreading resistance, the extrinsic base resistance and the base contact resistance. A decrease of both the intrinsic and extrinsic base resistances can be realized by reducing the emitter size and the emitter mesa undercut, respectively.

![Graph showing base contact resistivity before and after annealing](image)

*Figure 3.30 Base contact resistivity increase after annealing at 250 °C for 30 minutes.*

One approach to reduce contact resistivity, and thus contact resistance, is thermal annealing. However, not all contacts improve after annealing. In the particular case of contacts deposited on GaAsSb:C, annealing leads to an even higher contact resistivity. Fig. 3.30 shows the degradation of the contact deposited on a base material with the doping level of $8 \times 10^{19}$ cm$^{-3}$ after 30 minutes of rapid thermal annealing at 250 °C. The base contact resistivity increases by $\sim 45\%$ from an average value of $8.7 \times 10^{-5}$
7 Ω·cm² to 1.27 × 10⁻⁶ Ω·cm². Consequently, for the DHBT base contact step, we did not apply any thermal annealing.

### 3.2.1.2 Base Contact Resistivity Dependence on Doping level

According to Eqn. 3.1, a reduction of contact resistivity can be achieved by increasing the base doping concentration, since this decreases the depletion width at the semiconductor/metal interface. Fig. 3.31 experimentally confirms the lower base contact resistivity for increasing base doping levels in DHBTs grown with an InP emitter. An increase of the base doping level from 3.4 × 10¹⁹ cm⁻³ to 6.4 × 10¹⁹ cm⁻³ results in a base contact resistivity reduction by more than two orders of magnitude.

![Figure 3.31](image)

*Figure 3.31  Base contact resistivity as a function of the base doping level for the structures with InP emitter. The dashed trend line is to guide the eye.*
3.2 Base Optimizations

3.2.1.3 Base Contact Resistivity Comparison of DHBTs with GaInP and InP Emitters

![Graph showing base contact resistivity comparison between InP and GaInP emitters.]

**Figure 3.32** Base contact resistivity from DHBTs with InP and GaInP emitters versus the base doping level.

We increased the base doping level in DHBTs with GaInP emitters to further decrease the base resistance. The base contact resistivity versus the doping level of the DHBTs with both emitters is shown in Fig. 3.32. The base contact resistivity of GaInP/GaAsSb/InP DHBTs however is largely independent of the base doping level. This suggests that some material that was not completely etched during the emitter mesa etching is left on the base surface and introduces a higher base contact resistivity.

3.2.1.4 Base Contact Resistivity Improvement by Removing the Residual Material on Top of the Base Surface

To check whether any material might be left on top of the base is present, the following experiment was carried out on a sample with the epilayer structure shown in Table 3.3. The cap layer GaInP was removed by HCl:H₃PO₄ (12:72) solution. The sample was then split into two pieces, one of which was treated with concentrated HCl for 10 seconds (sample A).
Table 3.3 Epilayer structure of calibration (Bol280) used in this experiment.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness</th>
<th>Impurity</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 nm GaInP</td>
<td></td>
<td></td>
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<tr>
<td>GaAs&lt;sub&gt;0.63&lt;/sub&gt;Sb</td>
<td>30 nm</td>
<td>8 × 10&lt;sup&gt;19&lt;/sup&gt; cm&lt;sup&gt;-3&lt;/sup&gt;</td>
</tr>
<tr>
<td>80–85 nm UID InP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>InP SI Substrate</td>
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</table>

After the metal contact deposition, the TLM structures were isolated from each other by etching the entire epilayer structure down to the substrate, thus creating a mesa height of 500 nm. The base contact resistivity of the HCl treated and not treated samples were 3.7 × 10<sup>-9</sup> and 4.0 × 10<sup>-7</sup> Ω·cm<sup>2</sup>, respectively, as shown in Fig. 3.33. We showed that removing the residual material on the base treated with concentrated HCl led to a significant reduction of contact resistivity. This residual material probably consists of GaInP contaminated with Sb and As. This kind of contamination is related to growth and can not be avoided. Consequently, the resulting alloy can not be etched by the HCl:H<sub>3</sub>PO<sub>4</sub> solution used for the (Ga,In)P emitter etching. Only concentrated HCl enabled the etching of this undesired material, leading to an improved base contact resistivity.

Figure 3.33 Comparison of the base contact resistivity with and without concentrated HCl surface treatment.
3.2 Base Optimizations

The thickness of the residual material was investigated by means of an etching test performed on a DHBT structure. After the emitter mesa etching step, half of the sample (surface B) was protected by Shipley photoresist S1818 while the other half of the sample (surface A) was exposed to the air. The entire sample was dipped into concentrated HCl (see Fig. 3.34). After the photoresist removal, atomic force microscopy (AFM) was carried out to characterize the surface morphology of the surfaces A and B. The result is as shown in Fig. 3.35. Table 3.4 shows that the thickness of the residual material is 3.3 ± 0.3 nm and the root mean square roughness of surface A and B are 0.55 nm and 0.85 nm, respectively.

Figure 3.34 The base surface step formed after the etching with concentrated HCl. Surfaces A and B are treated with and without concentrated HCl, respectively.

![Figure 3.34](image)

Table 3.4 Surface roughness of both surfaces on a DHBT.

<table>
<thead>
<tr>
<th>Wafer No.</th>
<th>Interface Thickness</th>
<th>RMS of Surface B</th>
<th>RMS of Surface A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bol286F</td>
<td>3.3±0.3 nm</td>
<td>0.85 nm</td>
<td>0.55 nm</td>
</tr>
</tbody>
</table>

Figure 3.35 AFM images showing the step after removing the residual material on top of the base surface on half of the sample. (a) 1.8 × 1.8 µm² scan surface; (b) 6.4 × 6.4 µm² scan surface.
3.2.1.5 Base Surface Oxidation Effect on the Base Contact Resistivity

It is crucial to avoid contact surface oxidation that can degrade Ohmic performance [70]. In order to study the effect of the surface degradation induced by the base layer oxidation, the base contacts were deposited under two different conditions. The base layer of the first sample was exposed to air for one hour before the base metal deposition. For the second sample, the base metal was deposited immediately after the de-oxidation step. Fig. 3.36 shows the base contact resistivity obtained from both samples. The first sample exhibits a base contact resistivity of $2.5 \times 10^{-7} \, \Omega \cdot \text{cm}^2$, which is much higher than $7.8 \times 10^{-8} \, \Omega \cdot \text{cm}^2$ obtained from the second sample. This shows that it is of pivotal importance to reduce the time of the base layer exposure to air to a minimum, in order to avoid the contact resistivity degradation.

![Graph showing base contact resistivity degradation after one hour exposure to air.](image)

*Figure 3.36 Base contact resistivity degradation after one hour exposure to air.*
3.2.1.6 Base Contact Resistivity Improvement by Surface Treatment

![Diagram showing base contact resistivity in DHBT fabrication process with different surface treatment conditions.]

**Figure 3.37** Base contact resistivity in DHBT fabrication process with different surface treatment conditions.

During the optical contact lithography process of submicron DHBTs, PMMA associated resists and MIBK developer were used instead of the AZ developer. Before the base contact deposition, two different surface treatment solutions, (NH₄)₂S:H₂O (2:18) and HCl:H₂O (9:81) were respectively applied on the base layer of sample C and sample D. Commercially available (NH₄)₂S with the concentration of 21% and HCl with the concentration of 32% were diluted with DI water to form the solutions for both samples. As shown in Fig. 3.37, samples C and D exhibited an average base contact resistivity of $6.15 \times 10^{-8}$ and $3.84 \times 10^{-7} \, \Omega \cdot \text{cm}^2$, respectively.

A similar effect was also reported in Ref. [71] for GaAs, where the specific contact resistivity was reduced from $1.07 \times 10^{-3} \, \Omega \cdot \text{cm}^2$ to $2.49 \times 10^{-4} \, \Omega \cdot \text{cm}^2$ after sulfur treatment. This indicates that the sulfur treatment applied to the GaAs surface removes the native oxide and decreases the contact resistivity. Our results show that ammonium sulfide is more efficient than hydrochloric acid in removing the native oxides present on GaAsSb base layers, and that with this surface treatment, a lower specific contact resistivity was achieved.
3.2.2 $f_{\text{MAX}}$ Improvement due to Base Resistance Reduction

As discussed in Chapter 2, high frequency performance $f_{\text{MAX}}$ can be increased by reducing the emitter mesa undercut width and the base contact resistivity. Samples E, F and G with the emitter area of 0.6 $\times$ 11.5 $\mu$m$^2$ were fabricated by means of the optical contact lithography process discussed in Chapter 2. The DHBT structure was characterized by a 150 nm thick collector and a base sheet resistance of $\sim$ 1200 $\Omega$/$\square$.

The emitter layers of sample E were etched with a combination of dry and wet etching, creating an emitter mesa undercut of $\sim$ 60 - 70 nm. A concentrated HCl treatment for the residual material at the emitter/base interface was then applied. Fig. 3.38(a) and (b) show SEM images of sample E before and after applying the HCl treatment, respectively. Fig. 3.38(a) shows a much rougher semiconductor surface than (b), which shows an excellent smoothness.

![Figure 3.38 SEM pictures during the process: (a) sample E after InP wet etching; (b) sample E after HCl treatment; (c) sample F after the standard emitter wet etching; (d) sample G after HCl treatment.](image)

The emitters of the samples F and G were etched with the standard wet etching process (see Fig. 3.38(c)). The concentrated HCl treatment for removing the residual
material was additionally applied on sample G (see Fig. 3.38(d)). Thus, samples F and G differed only in that sample F consisted of the residual semiconductor material on which the base contact was deposited. Sample F exhibits a contact resistivity of $\sim 3 \times 10^{-6} \, \Omega \cdot \text{cm}^2$, owing to the residual material left on top of the base surface. Sample E and G both exhibit a lower base contact resistivity of $\sim 4 \times 10^{-7} \, \Omega \cdot \text{cm}^2$ proving that the residual material is responsible for the unexpected high contact resistivity.

### 3.2.2.1 Emitter Mesa Undercut Width Influence on $f_{\text{MAX}}$

Fig. 3.39 depicts the Gummel plots of DHBTs from samples E and G with the emitter area of $0.6 \times 11.5 \, \mu\text{m}^2$. Both samples show nearly overlapping base and collector currents. The reduced emitter mesa undercut width of sample E does not affect DC performances.

![Gummel plots of transistors with emitter area of 0.6 × 11.5 µm² from sample E and G. The emitter of sample E was etched with a combination of dry and wet etching. Sample G was processed with a standard wet etching.](image)

*Figure 3.39* Gummel plots of transistors with emitter area of $0.6 \times 11.5 \, \mu\text{m}^2$ from sample E and G. The emitter of sample E was etched with a combination of dry and wet etching. Sample G was processed with a standard wet etching.
In order to study the effect of the emitter mesa undercut width on $f_{\text{MAX}}$, the microwave performance of DHBTs was characterized over the 45 MHz to 40 GHz frequency band with an HP8510C vector network analyzer. A line-reflect-reflect-match (LRRM) calibration and an off-wafer impedance standard were used. Pads were de-embedded with on-wafer open/short calibration structures. The LRRM calibration method was chosen since it provides a good accuracy and requires a less critical placement of the probing tips.

![Image of a graph showing $|h_{21}|^2$ and Mason's unilateral gain $U$ as a function of frequency for devices biased at $V_{\text{CE}} = 1.6$ V and $I_{\text{C}} = 25$ mA.]

Figure 3.40  $|h_{21}|^2$ and Mason’s unilateral gain $U$ as a function of frequency of sample E and G.

Fig. 3.40 shows the short-circuit current gain $|h_{21}|^2$ and the Mason’s unilateral gain $U$ as a function of frequency for devices biased at $V_{\text{CE}} = 1.6$ V and $I_{\text{C}} = 25$ mA. The current gain cutoff frequency $f_T$ was determined by a $-20$ dB/dec extrapolation of $|h_{21}|^2$. A peak $f_T(\text{E}) = 317$ GHz and $f_T(\text{G}) = 322$ GHz was respectively obtained for samples E and G. As expected, the emitter mesa undercut width neither affects the current gain nor causes any difference in the current-gain cut-off frequency. The Mason’s unilateral gain $U$ with $-20$ dB/dec roll-off yields cutoff frequencies $f_{\text{MAX}(\text{E})} = 314$ GHz and $f_{\text{MAX}(\text{G})} = 320$ GHz, respectively for sample E and G. A higher $f_{\text{MAX}}$ from sample E could be expected, since its emitter mesa undercut width is smaller compared to that of sample G. The peaks of $U$ at $\sim 20$ GHz are due to the
resonance of the emitter pads connecting all the devices. The extracted total base resistance according to Ref. [72] yields nearly identical values of 21.97 Ω and 21.67 Ω for samples E and G, respectively. This indicates that the reduced emitter mesa undercut width in sample E does not induce a significant reduction of the total base resistance for transistors with an emitter area of 0.6 × 11.5 µm². The emitter undercut width reducing from 120 nm to 70 nm introduces only a slight difference of 2.6 Ω (the total base resistance reduces from 21.1 Ω to 18.5 Ω) in extrinsic base resistance, as calculated according to the device geometry. Consequently, $f_{\text{MAX}}$ does not increase. Transistors with an emitter width of 0.6 µm are characterized by a total base resistance dominated by the base contact resistance, and not by the extrinsic base resistance. This is verified by the calculated base resistance components, which are 5.26 Ω and 9.55 Ω for the intrinsic base resistance (base spreading resistance) and base contact resistance, respectively, according to the transistor geometry.

3.2.2.2 $f_{\text{MAX}}$ Improvement by Removing the Residual Material on Top of the Base Layer

![Figure 3.41 Gummel plots of 0.6 × 11.5 µm² transistors of samples F and G. The emitters of samples F and G were etched with standard wet etching, while sample G was additionally treated with concentrated HCl.](image-url)
The Gummel plots of DHBTs with an emitter area of $0.6 \times 11.5 \, \mu m^2$ for samples F and G are shown in Fig. 3.41. At low biases, both transistors exhibit nearly identical base and collector currents. However, sample F shows lower base and collector currents than sample G at high biases. The higher base contact resistance of sample F due to the residual GaInP(SbAs) material on top of the base layer results in a lower base current and therefore a lower collector current at a given high base voltage.

![Figure 3.42](image)

*Figure 3.42*  Gain as a function of the collector current for sample F and G. The emitters of sample F and G were etched by the standard wet etching while sample G was additionally treated with concentrated HCl.

The corresponding gain as a function of the collector current is plotted in Fig. 3.42. The voltage drop across the base and collector in sample F is larger than in sample G, due to the higher contact resistance caused by the residual material on the base layer. As a consequence, the Kirk current for sample F is expected at a higher applied base-collector voltage, as shown in Fig. 3.42. Moreover, after the base mesa etching step, the total collector size of sample F was measured (by Focus Ion Beam) to be $2.58 \, \mu m$, $\sim 250 \, nm$ larger than that of sample G due to the lower base undercut etching rate of sample F in the presence of the residual material which is difficult to
be etched away. This is also considered as one of the factors that lead to the higher Kirk current of sample F.

The current gain cutoff frequency $f_T$ was determined by a $-20$ dB/dec extrapolation of $|h_{21}|^2$, as shown in Fig. 3.43. A peak values $f_{T(F)} = 315$ GHz and $f_{T(G)} = 322$ GHz were extrapolated for samples F and G, respectively. However, Mason’s unilateral gain $U$ with $-20$ dB/dec roll-off yields remarkably different cutoff frequencies $f_{\text{MAX}(F)} = 211$ GHz and $f_{\text{MAX}(G)} = 320$ GHz, respectively for sample F and G. The extracted total base resistance, according to Ref. [72], yields values of 35 $\Omega$ and 21.67 $\Omega$ for sample F and G, respectively. Since the emitter and base geometric sizes of both transistors are the same, the extrinsic and intrinsic base resistances should also be the same. Therefore, the significant increase of $f_{\text{MAX}}$ in sample G can only be correlated to the base contact resistance reduction. Table 3.5 summarizes the RF performances and compares the extracted total base resistances of sample E, F and G. The $f_{\text{MAX}}$ improvement of sample G is attributed to the reduction of the base contact resistance.

![Figure 3.43](image-url)  

Figure 3.43 $|h_{21}|^2$ and Mason’s unilateral gain $U$ as a function of frequency of sample F and G.
Table 3.5 Summary of the RF performances and extracted base resistances in samples E, F and G.

<table>
<thead>
<tr>
<th>Sample ID</th>
<th>Process of the emitter mesa</th>
<th>Device No.</th>
<th>( f_T ) (GHz)</th>
<th>( f_{\text{MAX}} ) (GHz)</th>
<th>( R_b ) (( \Omega ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>Dry + Wet Etching + HCl</td>
<td>73B2</td>
<td>317</td>
<td>314</td>
<td>22.0</td>
</tr>
<tr>
<td>F</td>
<td>Standard Wet Etching</td>
<td>55B3</td>
<td>315</td>
<td>211</td>
<td>35.0</td>
</tr>
<tr>
<td>G</td>
<td>Standard Wet Etching + HCl</td>
<td>54B2</td>
<td>322</td>
<td>320</td>
<td>21.7</td>
</tr>
</tbody>
</table>

3.2.2.3 (NH\(_4\)\)\(_2\)S Surface Treatment Effect on \( f_{\text{MAX}} \)

DHBT samples H and K with an InP collector thickness of 125 nm were prepared to study the influence of the ammonium sulfide (NH\(_4\)\)\(_2\)S base surface treatment on the maximum oscillation frequency \( f_{\text{MAX}} \). The base sheet resistance was 1200 \( \Omega /\square \). Transistors with an emitter size of 0.6 \( \times \) 11.5 \( \mu \)m\(^2\) were fabricated with a standard triple mesa process by optical contact lithography.

![Gummel plots of DHBTs with emitter area of 0.6 \( \times \) 11.5 \( \mu \)m\(^2\) for samples with HCl and (NH\(_4\)\)\(_2\)S base surface treatments.](image)

Before base metallization, sample H was dipped into HCl:H\(_2\)O (1:9) solution during 30 seconds for deoxidation and rinsed in DI water for 1 minute. Sample K was dipped into (NH\(_4\)\)\(_2\)S:H\(_2\)O (1:9) solution for deoxidation and the purpose of the base surface
passivation during 30 seconds before being rinsed in DI water for 1 minute. The base contact resistivity of sample H and K was discussed in Subchapter 3.2.1.6. An aggressive base/collector undercut etching of 0.75 µm was applied for both samples to reduce the extrinsic base collector capacitance. Fig. 3.44 shows the Gummel plots of the transistors for both samples. The collector currents of both samples overlap. However, sample K showed a higher base current than sample H over the entire applied bias range. The corresponding plot of gain versus collector current is shown in Fig. 3.45. As expected, the gain of sample H is higher than that of sample K in the entire collector current region.

Jin [73] et al., have shown that (NH₄)₂S treated DHBT is Surface-Recombination-Free. The DHBTs of [73] were subjected to the surface treatment for 2 minutes. Tan et al. [71] showed that DHBTs with a GaAs base surface treated in (NH₄)₂S for two and 15 minutes exhibited lower and higher gains as compared to a DHBT with a GaInP ledge structure. Consequently, an optimal surface treatment time and a proper S weight concentration are necessary to increase the gain. In our experiments, the time of both the sulfide and HCl treatments was 30 seconds. In Fig. 3.46(a) and (b), the material in

![Figure 3.45](image)

*Figure 3.45  Corresponding gain versus collector current of DHBTs from sample H and K with emitter area of 0.6 × 11.5 µm².*
black located in the extrinsic area on top of the base surface represents the residual material. This layer formed during growth does not react with the two surface treatment solutions. Since sample K was treated with the (NH₄)₂S solution before the base contact evaporation, the surface of the InP emitter sidewall was also exposed to sulfide solution.

Surface recombination currents occur because electrons are injected directly from the emitter into the extrinsic base surface region through a saddle point in the conduction band potential at the emitter mesa sidewall intersection with the exposed base surface [61] [74]. This saddle point is formed by the surface Fermi level pinning at the emitter mesa sidewalls and the extrinsic base surfaces. The conduction band edge of the emitter treated with ammonium sulfide (sample K) moves closer to the Fermi level as compared to that treated with HCl (sample H) [75]. This results in a lower conduction band discontinuity between the GaAsSb and the GaInP emitter for sample K.

Figure 3.46 Schematic cross-section of the fabricated DHBTs with (a) HCl and (b) (NH₄)₂S surface treatments before base contact evaporation. The orange area shows the region which was in contact with (NH₄)₂S.
At the InP/air interface, the Fermi level pins at an energy level of 0.45 eV [74] below the conduction band forming a depletion region. The InP surface treatment with (NH₄)₂S moves the Fermi level pinning energy closer to the conduction band [76] reducing the upward conduction band bending as well as the depletion width. Consequently, the emitter sidewalls of sample K treated with (NH₄)₂S assist the transfer of electrons from the emitter to the extrinsic base region through the saddle point [77]. This mechanism is responsible for a surface recombination rate in sample K of $3.66 \times 10^{-4}$ mA/µm, which is higher as compared to $2.673 \times 10^{-4}$ mA/µm measured in sample H. The gain is therefore lower in sample K.

The short-circuit current gain $|h_{21}|^2$ and Mason’s unilateral gain $U$ as a function of frequency for both devices with emitter area of $0.6 \times 11.5 \mu m^2$ are shown in Fig. 3.47(a) and (b). The devices on both samples show the same short-circuit current gain $|h_{21}|^2$ and therefore yield the same peak current-gain cut-off frequency $f_T$ of 388 GHz (Fig. 3.47(a)). The total emitter resistances extracted from the S parameters are $R_E = 3.295 \Omega$ and $3.147 \Omega$ for sample H and K, respectively. The lower $R_E$ supports the idea that the effective emitter/base junction area of sample K is larger than that of sample H due to the reduced depletion width of the emitter sidewall for sample K caused by the (NH₄)₂S treatment.
Figure 3.47  (a) $|h_{21}|^2$ and (b) Mason’s unilateral gain $U$ as a function of frequency on $0.6 \times 11.5 \ \mu m^2$ DHBTs for both transistors.

Sample K exhibits a higher Mason’s unilateral gain $U$ and $f_{\text{MAX}}$ over the entire frequency range as shown in Fig. 3.47(b). Figure 3.48 details the evolution of the current-gain cut-off frequency and the maximum oscillation frequency as a function of the collector current for devices from both samples at a bias of $V_{\text{CE}} = 1.4 \ \text{V}$. 
3.2 Base Optimizations

Figure 3.48  Evolution of $f_T$ and $f_{\text{MAX}}$ with the collector current for DHBTs with the emitter area of $0.6 \times 11.5 \, \mu m^2$ for sample H and K.

Sample K shows similar $f_T$ values as sample H over the entire collector current range. At each collector current level, sample K shows a higher $f_{\text{MAX}}$ than sample H. The peak $f_{\text{MAX}}$ is 319 GHz and 351 GHz for sample H and K, respectively. At the peak $f_T$ bias point, the base resistances for both samples extracted from the S-parameters according to Ref. [72] are $R_B (H) = 22.38 \, \Omega$ and $R_B (K) = 13.89 \, \Omega$, respectively. This is also consistent with the base resistance values calculated according to the device geometry and contact/sheet resistances which are $R_B (H) = 20.1 \, \Omega$ and $R_B (K) = 14.3 \, \Omega$ for sample H and K, respectively. Since the devices of both samples have the same physical geometry, the lower total base resistance of sample K is only due to the reduced base contact resistivity. Therefore, the $f_{\text{MAX}}$ improvement of sample K is attributed to the reduced base contact resistivity and thus the decreased base contact resistance.

In summary, DC and RF performances of $0.6 \times 11.5 \, \mu m^2$ devices with two base surface treatments were studied. The sample is dipped into diluted HCl and (NH$_4$)$_2$S, respectively, for 30 seconds followed by rinsing in DI water for 30 seconds before the base metal deposition. It was found that the transistor with the (NH$_4$)$_2$S treated base
shows a lower gain due to the moving up of the surface Fermi pinning level of the emitter sidewall. However, it exhibits a lower base contact resistivity and thus a higher maximum oscillation frequency $f_{\text{MAX}}$. DHBTs with simultaneous $f_T = 388 \text{ GHz}$ and $f_{\text{MAX}} = 351 \text{ GHz}$ were obtained with a 125 nm thick collector by optical contact lithography for a 20 nm thick base characterized by a sheet resistance $R_{\text{SH}}$ of 1200 $\Omega/\square$.

### 3.2.3 Graded Base and Uniform Base

As mentioned in Chapter 1, when the As content and the doping level of the base layer are uniform, the electrons injected from the emitter travel through the base layer only by diffusion. To further accelerate the electrons, an electric field can be introduced by a compositional grading or doping grading. When the conduction band energy in the base material decreases from the emitter/base interface towards the base/collector interface, an internal quasi-electric field is created. Consequently, electrons are driven by this quasi-electric field through the base. A conduction band energy decreasing from the emitter to the collector is obtained by decreasing the Arsenic concentration in GaAsSb, and by decreasing the $p$-type doping concentration.

Samples Bol150 and Bol153 were grown with a uniform base layer, while samples Bol157 and Bol163 were grown with graded composition and doping in the base. The base As concentration of the samples Bol157 and Bol163 increases respectively from 0.5 and 0.4 at the base/collector interface to 0.6 at the base/emitter interface. (Ga,In)P/GaAsSb DHBTs with an emitter area of $20 \times 30 \mu\text{m}^2$ were fabricated with QHBT process.

The corresponding band gap difference for the graded bases and its induced base electric field factor $K$ ($K = \frac{\Delta E}{KT}$) are calculated according to Ref.[59]. The calculated $K$ factor for Bol157 and Bol163 are respectively 0.6 and 1.2, if we consider only the effect of the base electric field induced by the compositional grading. The ratio between the gain of DHBTs with uniform and graded base layer $\frac{\beta(\text{uniform base})}{\beta(\text{graded base})}$ is

$$f(K) = \frac{2}{K} \left( 1 - \frac{1}{K} + \frac{1}{K} e^{-K} \right)$$

(3.4)
3.2 Base Optimizations

\( f \) is plotted versus \( K \) in Fig. 3.49. For Bol157 and Bol163, Eqn. 3.4 yields \( f(0.6) = 0.83 \) and \( f(1.2) = 0.7 \), respectively (see Table 3.6).

**Table 3.6 Sheet resistances and doping levels of the base layers under investigation and the corresponding calculated \( K \) factor for the graded bases if the compositional grading is considered only.**

<table>
<thead>
<tr>
<th>Wafer No.</th>
<th>Base Sheet Resistance ( R_s ) (Ω/□)</th>
<th>Average Doping Level (cm(^{-3}))</th>
<th>As Concentration from E/B to B/C</th>
<th>Energy Band Gap Difference (eV)</th>
<th>Base Electric Field Factor ( K )</th>
<th>( f(K) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bol150</td>
<td>1786</td>
<td>4.9 \times 10^{19}</td>
<td>uniform</td>
<td>0</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Bol157</td>
<td>1494</td>
<td>6 \times 10^{19}</td>
<td>graded (0.6 to 0.5)</td>
<td>0.015</td>
<td>0.6</td>
<td>0.83</td>
</tr>
<tr>
<td>Bol153</td>
<td>1161</td>
<td>8 \times 10^{19}</td>
<td>uniform</td>
<td>0</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Bol163</td>
<td>1084</td>
<td>8 \times 10^{19}</td>
<td>graded (0.6 to 0.4)</td>
<td>0.03</td>
<td>1.2</td>
<td>0.7</td>
</tr>
</tbody>
</table>
Figure 3.49  Gain ratio $f$ between DHBTs with uniform and graded base versus the base electric field factor $K$.

Figure 3.50  Gain at the collector current of 60 mA versus base sheet resistance from transistors with the emitter area of $20 \times 30 \mu m^2$ and with both uniform and graded base layers.
Fig. 3.50 shows the gain obtained at the collector current of 60 mA versus the base sheet resistance for transistors with the emitter area of $20 \times 30 \, \mu m^2$ and for both uniform and graded base layers. Bol153 and Bol163 feature similar average doping levels and therefore similar base sheet resistances. The gain ratio between Bol153 and Bol163 is 0.69, and agrees well with the calculated value $f(K) = 0.7$. Despite the lower base sheet resistance of Bol157 as compared to Bol150, Bol157 features a higher DC gain.

In conclusion, the experiments clearly show a higher DC gain in the graded base layers at a given sheet resistance. This is due to the electric field which reduces the electron transit time in base and thus the electron-hole recombination.

### 3.2.4 Base Thickness Optimization

![Graph showing base sheet resistance versus base thickness](image)

*Figure 3.51 Base sheet resistance versus the base thickness determined by linear TLM measurement on the base layers.*

Both the introduction of an internal electric field in the base and a decrease of the base layer thickness, could lead to lower electron base transit time. DHBTs with epilayer structures containing a base layer thickness of 15 nm, 20 nm and 25 nm were fabricated by means of the QHBT process (described in Chapter 2) with an emitter...
area of $20 \times 30 \mu m^2$. All the transistor structures are provided by a base layer with a
doping level of $8.4 \times 10^{19} cm^{-3}$ and a uniform As content of 0.536. Fig. 3.51 depicts
the measured base sheet resistance versus base thickness. The base sheet resistance is
reduced as the base thickness increases, as expected, although the relation appears to
be non-linear.

Fig. 3.52 shows the Gummel plots of the transistors with the three different base
thicknesses. At low biases, both the base and collector currents for all three transistors
slightly differ from each other. The lowest base and collector currents were found for
the transistor with 15 nm base thickness.

A thinner base leads to a higher intrinsic base resistance for the holes and thus higher
total base resistance. The corresponding gain versus the collector current for all three
transistors is shown in Fig. 3.53. The reduction of the base layer thickness leads to a
significant gain increase since the lower electron transit time and lower recombination
probability produces the lower recombination current.

A 20 nm thick base with the doping level of $8.4 \times 10^{19} cm^{-3}$ was chosen as a
compromise in order to target a high $f_t$ without overly sacrificing $f_{MAX}$. 

Figure 3.52  Gummel plots of transistors with the emitter area of $20 \times 30 \mu m^2$ for
different base thicknesses.
3.2 Base Optimizations

3.2.5 Effect of Base Arsenic Concentration

Despite the above-listed advantages in terms of band structure and layer simplicity, InP/GaAsSb DHBTs often feature relatively low common-emitter current gain values $\beta = I_C/I_B$. One possible reason is that the type-II conduction band edge discontinuity $\Delta E_C$ at E/B interface presents a small barrier for the electrons, thus reducing the DC current gain. In type-II DHBTs, gain could therefore in principle be increased by reducing or eliminating the type-II conduction band offset $\Delta E_C$ to reduce recombination at the E/B interface. This line of reasoning received experimental support by replacing the InP emitter with an AlInP layer [78] or by inserting a 15 nm InAlAs layer between the base and the emitter layers [79] in order to achieve a type-I E/B interface transition with the GaAsSb base layer. Gain improvements were indeed achieved experimentally, but no previous work has been done to determine the current gain dependence of InP/GaAs$_{1-x}$/Sb$_{x}$/InP DHBTs on the base As mole fraction $x$, as well as to clarify which recombination mechanism(s) dominate(s) transistor performance. The present work thus addresses these questions.
We experimentally study the gain characteristics of InP/GaAs$_{x}$Sb$_{1-x}$/InP DHBTs with different As base contents ranging from $x = 0.485$ to $x = 0.645$. Large area devices with emitter contact sizes of $20 \times 30 \ \mu m^2$, $40 \times 40 \ \mu m^2$, $80 \times 80 \ \mu m^2$ were fabricated, and both the periphery and the intrinsic surface recombination characteristics were determined from the emitter size dependence of the current gain $\beta$ (i.e. emitter size effects). We observed that both the emitter periphery and intrinsic recombination currents decrease as the base arsenic mole fraction $x$ increases and as the type-II $\Delta E_C$ at the E/B heterojunction decreases. The Gummel characteristics were also examined to determine the effect of $\Delta E_C$ on the current transport mechanism through InP/GaAsSb DHBTs, and showed that the base As mole fraction $x$ does not modify the carrier injection mechanism over the entire composition range considered here. However, the Gummel characteristics revealed that the gain improvement accrued with increasing As mole fractions $x$ follows uniquely from a base current reduction.

High-resolution x-ray diffraction (HRXRD) profiles were measured on 100 nm bulk GaAs$_x$Sb$_{1-x}$ calibration samples grown on InP (Fig. 3.54): these calibrations were used to determine the alloy compositions, growth rates, and doping levels. The base As concentrations used in the actual transistor structures were varied between $x = 0.485$ and 0.645. The 100 nm bulk calibration run corresponding $x = 0.645$ showed cross-hatch strain relaxation features because of the large strain for the thick GaAs$_{0.645}$Sb$_{0.355}$ layer grown on InP substrate, but this did not play a role in the growth of the corresponding transistor structure because the GaAsSb base thickness is only 20 nm. As shown in Fig. 3.54, the GaAs$_x$Sb$_{1-x}$ diffraction peak moves further away from InP substrate peak with increasing arsenic mole fraction $x$, indicating that tensile strain increases.

The epitaxial device structure consists of a 300 nm $n = 3 \times 10^{19} \ \text{cm}^{-3}$ InP sub-collector, a heavily doped $n = 7.5 \times 10^{18} \ \text{cm}^{-3}$ 50 nm Ga$_{0.47}$In$_{0.53}$As etch-stop layer, a 200 nm $n = 3 \times 10^{16} \ \text{cm}^{-3}$ collector, a 20 nm base, a 70 nm $n = 3 \times 10^{17} \ \text{cm}^{-3}$ emitter, a 50 nm $n = 3 \times 10^{19} \ \text{cm}^{-3}$ emitter cap and a 100 nm $n = 1.5 \times 10^{19} \ \text{cm}^{-3}$ emitter contact layer. Five samples with different base As concentrations and acceptor doping levels (i.e. more precisely hole concentrations) were grown at $5.89 \times 10^{19}$, $3.9 \times 10^{19}$, $3.56 \times 10^{19}$, $3.57 \times 10^{19}$, $3.11 \times 10^{19} \ \text{cm}^{-3}$ and $x = 0.485$, 0.538, 0.574, 0.615, 0.645, respectively,
as summarized in Table 3.7. These five DHBT structures are labeled as sample U, V, W, X and Y, respectively. It was not possible to grow all samples with exactly the same free hole concentrations because the C-doping level and the mole fraction $x$ are coupled parameters in MOVPE-grown GaAs$_x$Sb$_{1-x}$ [80] [81]. The 20 nm GaAsSb base thickness in samples U to Y was subsequently confirmed by cross-sectional electron microscopy. All DHBTs under study have the same emitter and collector areas. The emitter contact sizes are $20 \times 30 \ \mu m^2$, $40 \times 40 \ \mu m^2$ and $80 \times 80 \ \mu m^2$, respectively. The devices were fabricated by conventional wet etching with two mesa steps and a single common metal evaporation step. The devices were not subjected to any passivation treatment. The DC characteristics were measured with a Keithley S4200 semiconductor parameter analyzer.
Table 3.7 Layer structures used in this study

<table>
<thead>
<tr>
<th>Material</th>
<th>( x(\text{As}) )</th>
<th>Doping Level (cm(^{-3}))</th>
<th>Thickness (nm)</th>
<th>Base ( R_{\text{SH}}(\text{Ohm/sq.}) / \mu_p(\text{cm}^2/\text{Vs}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaInAs:Si</td>
<td></td>
<td>1.5 \times 10^{19}</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>InP:Si</td>
<td></td>
<td>3 \times 10^{19}</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>InP:Si</td>
<td></td>
<td>3 \times 10^{17}</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td><strong>GaAs(<em>x)Sb(</em>{1-x}) C-doped</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sample U</td>
<td>0.485</td>
<td>5.89 \times 10^{19}</td>
<td></td>
<td>1370 / 38.7</td>
</tr>
<tr>
<td>Sample V</td>
<td>0.538</td>
<td>3.90 \times 10^{19}</td>
<td></td>
<td>1866 / 42.9</td>
</tr>
<tr>
<td>Sample W</td>
<td>0.574</td>
<td>3.56 \times 10^{19}</td>
<td>20</td>
<td>2095 / 41.8</td>
</tr>
<tr>
<td>Sample X</td>
<td>0.615</td>
<td>3.57 \times 10^{19}</td>
<td></td>
<td>2315 / 37.8</td>
</tr>
<tr>
<td>Sample Y</td>
<td>0.645</td>
<td>3.11 \times 10^{19}</td>
<td></td>
<td>3350 / 30.0</td>
</tr>
<tr>
<td>InP:Si</td>
<td></td>
<td>3 \times 10^{16}</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>GaInAs:Si</td>
<td></td>
<td>7.5 \times 10^{18}</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>InP:Si</td>
<td></td>
<td>3 \times 10^{19}</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td><strong>Semi-Insulating InP</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The corresponding equilibrium band diagrams for structures U to Y are shown in Fig. 3.55. It can be seen that the type-II conduction band discontinuity \( \Delta E_C \) is reduced as the base arsenic mole fraction \( x \) increases. Therefore, the possibility of electron piling up at the interface decreases [31, 82], thus in principle easing electron injection from the InP emitter into the GaAsSb base as \( \Delta E_C \) decreases. According to Peter et al. [59], the maximum As concentration considered here (\( x = 0.645 \)) still results in a type-II alignment between the InP emitter and the tensile-strained GaAsSb base: this means that \( \Delta E_C \) remains negative for samples U to Y, as illustrated in Fig. 3.56 (i.e. the GaAsSb conduction band edge remains above that of InP throughout the present work). \(|\Delta E_C|\) decreases as \( x \) increases, which means electrons meet the smallest energy barrier height in sample Y. It should be noted that according to [59], \(|\Delta E_C|\) between InP and GaAs\(_x\)Sb\(_{1-x}\) only goes to zero when \( x = 0.73 \), but GaAs\(_{0.73}\)Sb\(_{0.27}\) base layers could not be grown in this work because of pseudomorphic growth limitations.
3.2 Base Optimizations

Figure 3.55 Equilibrium band diagram for the two end points of base arsenic concentrations considered here. $\Delta E_C$ decreases as the arsenic content increases, but the band alignment remains type-II.

The dependence of current gain $\beta = I_C/I_B$ on the GaAs$_x$Sb$_{1-x}$ base As mole fraction $x$ was measured from Gummel characteristics by sweeping the emitter-base bias with a fixed $V_{BC} = 0$ V. Figure 3.57(a) shows gain measured at $I_C = 50$ mA as a function of arsenic content as measured on 80 $\times$ 80 $\mu$m$^2$ emitter devices. The current gain $\beta$ clearly increases as the GaAsSb base arsenic mole fraction $x$ increases. The gain plotted as a function of the base sheet resistance $R_{SH}$ for samples U to Y together with a series of lattice-matched reference transistor samples in Fig. 3.57(b). It is easily confirmed that As-rich samples exhibit higher gain levels than those of lattice-matched samples at a given base sheet resistance $R_{SH}$. The gain therefore clearly improves with increasing base arsenic mole fraction $x$ in InP/GaAsSb DHBTs. We now proceed with the clarification of the mechanism(s) behind this gain improvement.
Figure 3.56 Energy gap and conduction, valence band discontinuity from samples U to Y with base As concentrations of 0.485, 0.538, 0.574, 0.615, 0.645, respectively. All show type-II alignment (i.e. $\Delta E_C < 0$).
Figure 3.57  (a) Gain as a function of arsenic concentration for 80 × 80 µm² devices at a collector current of $I_C = 50 \text{ mA}$. (b) Gain as a function of sheet resistance on 80 × 80 µm² devices at $I_C = 50 \text{ mA}$. Gain as a function of sheet resistance for several lattice-matched samples with different C- doping levels is given for comparison.

Table 3.8 Details of the lattice-matched samples in Fig. 3.57(b)

<table>
<thead>
<tr>
<th>Base Sheet Resistance $R_{SH}$ ($\Omega/\square$)</th>
<th>Doping Level ($\text{cm}^{-3}$)</th>
<th>Hole Mobility $\mu_p$ ($\text{cm}^2/\text{Vs}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1450</td>
<td>$6.1 \times 10^{19}$</td>
<td>39.1</td>
</tr>
<tr>
<td>1410</td>
<td>$6.1 \times 10^{19}$</td>
<td>39.1</td>
</tr>
<tr>
<td>1370</td>
<td>$5.9 \times 10^{19}$</td>
<td>35.2</td>
</tr>
<tr>
<td>2302</td>
<td>$3.9 \times 10^{19}$</td>
<td>40.1</td>
</tr>
<tr>
<td>3653</td>
<td>$2.4 \times 10^{19}$</td>
<td>35.7</td>
</tr>
<tr>
<td>3322</td>
<td>$3.1 \times 10^{19}$</td>
<td>35.1</td>
</tr>
<tr>
<td>1015</td>
<td>$8.4 \times 10^{19}$</td>
<td>33.5</td>
</tr>
<tr>
<td>2109</td>
<td>$3.9 \times 10^{19}$</td>
<td>39.2</td>
</tr>
</tbody>
</table>
Chapter 3: Optimization of DHBT Structure Design and Fabrication Process

### (a)

![Graph](image)

- \( [As] = 0.485 \quad K_{surf} = 4.06 \times 10^{-3} \text{ mA/\mu m} \)
- \( [As] = 0.538 \quad K_{surf} = 4.97 \times 10^{-4} \text{ mA/\mu m} \)
- \( [As] = 0.574 \quad K_{surf} = 4.32 \times 10^{-4} \text{ mA/\mu m} \)
- \( [As] = 0.615 \quad K_{surf} = 3.06 \times 10^{-4} \text{ mA/\mu m} \)
- \( [As] = 0.645 \quad K_{surf} = 1.36 \times 10^{-4} \text{ mA/\mu m} \)

**Emitter Periphery-to-Area Ratio, \( \frac{P_E}{A_E} \) (\( \mu \text{m}^{-1} \))**

### (b)

![Graph](image)

- Normalized Periphery Current (mA/\mu m)
- Collector Current Density (A/cm\(^2\))

- \( [As] = 0.485 \)
- \( [As] = 0.538 \)
- \( [As] = 0.574 \)
- \( [As] = 0.615 \)
- \( [As] = 0.645 \)
3.2 Base Optimizations

Figure 3.58  (a) Surface recombination rate extraction at $J_C = 10^3$ A/cm² from sample U to sample Y with arsenic concentration $x = 0.485, 0.538, 0.574, 0.615, 0.645$, respectively. The slope of each line corresponds to the factor $K_{Bsurf}$ in Eqn. 3.2. (b) Surface recombination factor $K_{Bsurf}$ as a function of collector current density $J_C$. (c) Intrinsic base recombination current density $J_{BI}$ as a function of $J_C$.

In order to shed some light on the gain improvement mechanism associated with higher arsenic base mole fractions, we studied the emitter-size dependence of the current gain $\beta$ in order to distinguish between surface (i.e. periphery) and intrinsic (i.e. directly under the emitter contact) recombination effects in our InP/GaAsSb DHBTs. The impact of emitter size effects on the DC current gain can be quantified by writing the equivalent total base current density as shown in Eqn. 3.2, where $J_C$ is the collector current density, $J_{QBN}$, $J_{BSCR}$ and $J_{BP}$ are the base bulk quasi-neutral, space charge and back-injection recombination current densities (all taking place under the emitter contact), and $\beta$ is the common-emitter current gain evaluated at $J_C$. As previously mentioned, it is probably a good assumption to take $J_{BP} = 0$ because of the very large $\Delta E_V$ in InP/GaAsSb DHBTs. The quantity $K_{Bsurf}P_E$ in Eqn. 3.2 represents the total emitter periphery surface recombination current, and $P_E$ and $P_E$ are the emitter area and periphery. By measuring and plotting $J_C/\beta$ as a function of the
emitter periphery-to-area ratio \( P_E/A_E \), the surface recombination factor \( K_{Bsurf} \) is obtained as the slope from a linear fit through the data. \( K_{Bsurf} \) was found to decrease as the arsenic mole fraction \( x \) increases as shown in Fig. 3.58(a). Between samples U and Y, corresponding to a 16% increase in \( x \), the surface periphery recombination decreased nearly by a factor of 30\( \times \), from \( 4.06 \times 10^{-3} \) to \( 1.36 \times 10^{-4} \) mA/\( \mu \)m at a collector current density of \( J_C = 10^3 \) A/cm\(^2\). Based on previous analysis [74], periphery surface recombination occurs through the direct injection of electrons from the emitter mesa onto the extrinsic base surface through a saddle point potential. The present results show that a larger type-II \( \Delta E_C \) at the E/B favors the injection of electrons from the emitter to the extrinsic base surface by presumably capturing electrons in the type-II notch present at forward biased E/B junctions [74]. In the present case, the decreased \( \Delta E_C \) with increasing As content weakens the saddle point potential that causes surface emitter periphery recombination. Extrapolating the plots of Fig. 3.58(a) back to \( P_E/A_E = 0 \) also allows one to determine the non-periphery related (i.e. intrinsic) base current component \( J_{BI} = (J_{QBN} + J_{BSCR}) \approx (J_{QBN} + J_{BSCR}) \) in Eqn. (3.2) to find that intrinsic recombination is also reduced by a factor of 13.5\( \times \) (at \( J_C = 10^3 \) A/cm\(^2\)) by increasing the base arsenic content.

\( K_{Bsurf} \) was found to rise as collector current density increases for all the samples as shown in Fig. 3.58(b), which reproduces the trend seen in [74]. Sample U (\( x = 0.485 \)) showed the highest surface recombination rate at all current densities, followed by a continuous reduction of \( K_{Bsurf} \) from sample V (\( x = 0.538 \)) to sample Y (\( x = 0.645 \)). Fig. 3.58(c) shows that the intrinsic base recombination current (i.e. directly under the emitter contact, and either in the space charge region or in the quasi-neutral undepleted base region) also increase with \( J_C \) with the lowest values always achieved for the highest base As mole fractions (sample Y). Clearly, the reduction or elimination of \( \Delta E_C \) is of primary importance to the optimization of InP/GaAsSb DHBT performance. The data of Fig. 3.58 therefore unambiguously demonstrate that the emitter type-II conduction band discontinuity between the InP emitter and the GaAs\(_x\)Sb\(_{1-x}\) base enhances the undesirable emitter-size effects (ESEs) due to periphery surface recombination currents \( K_{Bsurf}P_E \), and increases intrinsic recombination currents \( J_{BI} \) directly under the emitter contact. The \( J_{BI} \) reduction with higher base As mole fractions \( x \) can arise from two distinct mechanisms: i) the lower \( \Delta E_C \) at the E/B
interface results in a lower electron density in the E/B space charge region and minimizes type-II recombination across the InP-GaAsSb interface and/or defect mediated recombination; and ii) tensile strain in the GaAsSb base favorably alters the quasi-neutral base recombination parameters (such as the Auger coefficients) because of modifications to the GaAsSb base valence band structure. Some reduction in $J_{BI}$ may be attributed to the increased base sheet resistance accompanying higher As mole fractions (see Table 3.7). The base sheet resistance increases by a factor of $\sim 2.4 \times$ between samples U and Y, and one could thus expect a 2.4-6.0× reduction in $J_{BI}$ from this effect, depending on whether the recombination in the quasi-neutral base is dominated by band-to-band ($\beta \sim R_{SH}$) or Auger ($\beta \sim R_{SH}^2$) processes [83] [84]. This suggests the reduced $\Delta E_C$ also helps minimize recombination in the E/B space charge region since intrinsic recombination drops by a factor of at least 13.5×. It is not possible to electrically distinguish between the two effects without independently determining carrier lifetimes in heavily-doped GaAsSb strained layers: this task lies beyond the scope of the present work.

The Gummel characteristics for sample U to Y reveal collector current ideality factors $n_C = 1.02-1.05$, indicating that the electrons are thermally injected from the InP emitter into the GaAs$_x$Sb$_{1-x}$ base layers, regardless of the As mole fraction $x$. The base current ideality factor $n_B \sim 1.45$ also does not appreciably depend on the base composition for the range investigated here. Fig. 3.59 shows representative Gummel characteristics for $40 \times 40 \mu m^2$ devices processed on samples V and Y (chosen since V and Y have comparable base doping levels, as seen in Table 3.7). It is interesting to note that when superposed, the Gummel characteristics result in almost exactly overlapping $I_C$ plots but decreasing $I_B$ plots with increasing As mole fraction. The observation indicates that the current gain improvement follows directly from a reduction of both the periphery and intrinsic base recombination current components achieved by increasing the GaAsSb base As mole fraction $x$. Whereas lattice-matched bases show recombination characteristics that are very similar to those of InP/GaInAs HBTs [74] and enable the realization of 300-400 GHz transistors [82] [31], further improvements can be achieved by reducing or eliminating the emitter-base band discontinuity $\Delta E_C$. We have recently provided independent evidence for this by reducing the type-II $\Delta E_C$ through the use of a GaInP strained emitter [34]. The
present work therefore provides the first physical clarification for the improvements accrued with wider-gap emitters such as [34] [78] [79].

![Gummel characteristics for 40 x 40 µm² devices fabricated on samples V and Y. The collector and base current ideality factors n_C and n_B are indicated in the plot. The data indicate that the current gain enhancement associated with higher As concentrations occurs principally through a reduction of the base current.](image)

In conclusion, the performance of type-II InP/GaAs<sub>x</sub>Sb<sub>1-x</sub>/InP DHBTs was studied as a function of the base arsenic mole x. The static DC gain $\beta = I_C/I_B$ was improved with arsenic concentration increases due to significant reductions in both the surface emitter periphery recombination rate and the intrinsic recombination taking place immediately under the emitter contact. The type-II $\Delta E_C$ was reduced by adjusting the base As concentration, in agreement with the work on emitters.

### 3.2.6 Base Undercut Effects

It is highly desirable to engineer devices with balanced values for the current-gain cut-off frequency $f_T$ and the maximum oscillation frequency $f_{MAX}$ with more relaxed critical dimensions. Base/collector junction capacitance ($C_{CB}$) is an important factor for the improvement of $f_{MAX}$ as well as $f_T$, as indicated in Eqn. 3.3. Reducing $C_{CB}$ can
be realized by increasing the collector thickness and the base mesa undercut. In this work we demonstrate by optical contact lithography type-II InP/GaAsSb DHBTs which achieve simultaneous $f_T$ and $f_{MAX} > 340 \text{ GHz}$ and maintain a breakdown voltage $BV_{CEO} = 5.85 \text{ V}$. The effects of base metal undercut etch and of the base metallization contact width on the RF performances of our InP/GaAsSb DHBTs are also discussed.

Two typical DHBT wafers with InP collector thicknesses of 125 and 150 nm were grown by MOVPE. The measured base sheet resistances for both samples were practically identical (1200 $\Omega/\square$). Transistors were fabricated with the standard triple-mesa etching process. The base mesa was formed by a combination of dry and wet etching. A ~ 80 nm GaAsSb/InP mesa was first formed by dry etching after the base contact step. Undercuts of 0.45 and 0.75 $\mu$m were then implemented by an aggressive wet etching of the GaAsSb base in order to reduce the extrinsic base collector capacitance $C_{CBX}$.

We describe the development of the processing steps to achieve the designed base undercut width. The base contact metal was deposited on some test samples and ICP dry etching was used to form a base mesa height of ~ 80 nm. A test sample was first dipped in the solution $\text{H}_3\text{PO}_4$:$\text{H}_2\text{O}_2$:$\text{H}_2\text{O}$ (6:1:80) in order to etch GaAsSb. A second etching was applied to this test sample in $\text{HCl}$:$\text{H}_3\text{PO}_4$ (12:72) for etching both the collector and InP pedestal layers. In order to achieve the designed undercut widths of 0.45 and 0.75 $\mu$m, the etching time had to be adjusted. The experiments showed that the lateral etching of InP is not possible underneath the GaAsSb layer (See Fig. 3.60). As a consequence, the undercut width is controlled directly by the lateral etch of the GaAsSb layer (timed etch). A time of 60 s (80 s) and 20 s (40 s) for the etching of GaAsSb and InP enabled an undercut of 0.45 $\mu$m (0.75 $\mu$m) respectively (See Figs. 3.61 and 3.62).
Figure 3.60  SEM image of a base mesa with a 211 nm undercut. The sample was first etched in \( H_3PO_4:H_2O_2:H_2O \) (6:1:80) for 20 s to remove GaAsSb. A second etch in \( HCl:H_3PO_4 \) (12:72) for 140 s was applied to remove InP. It is not possible to etch laterally the InP below the GaAsSb layer.

Fig. 3.62 shows the cross-section of a device with the B/E junction protected by a positive photoresist mask after the base mesa etching. It shows that a good alignment by optical contact lithography is necessary in order to permit an aggressive base mesa etching.

Fig. 3.63 shows Gummel characteristics from \( 0.6 \times 11.5 \mu m^2 \) devices for both collector thicknesses. Both feature identical base and collector currents before the Kirk effect sets in. This indicates that the epitaxial layers are practically identical with the exception of the collector thickness, and it demonstrates excellent growth and processing reproducibility.
3.2 Base Optimizations

Figure 3.61 SEM image of a base mesa with a 463 nm undercut after etching GaAsSb and InP in $\text{H}_3\text{PO}_4$:$\text{H}_2\text{O}_2$:$\text{H}_2\text{O}$ (6:1:80) for 60 s and InP HCl:$\text{H}_3\text{PO}_4$ (12:72) for 20 s, respectively.

Figure 3.62 SEM image of a base mesa with a 750 nm undercut after etching GaAsSb and InP in $\text{H}_3\text{PO}_4$:$\text{H}_2\text{O}_2$:$\text{H}_2\text{O}$ (6:1:80) for 80 s and HCl:$\text{H}_3\text{PO}_4$ (12:72) for 40 s, respectively.

The peak current gain exceeds $\beta > 60$ for both wafers, suggesting that gain is available to be traded off to further lower the base sheet resistance. As expected, the device with 125 nm collector shows a slightly higher Kirk current than the device with
150 nm collector. This is also verified by the plots of gain as a function of $V_{BE}$ also shown in the same plot.

![Gummel plot](image)

**Figure 3.63** Typical Gummel plot of $0.6 \times 11.5 \mu m^2$ devices with the collector thickness of 125 and 150 nm, respectively. The base and collector currents overlap well at low biases. At the higher biases, the device with the thinner collector shows a slightly higher collector current due to its higher Kirk current.

Fig. 3.64 shows $f_T$ and $f_{MAX}$ as a function of collector current for $0.6 \times 11.5 \mu m^2$ devices built with a 125 nm InP collector at the bias of $V_{CE} = 1.4V$. The cut-off frequencies $f_T$ and $f_{MAX}$ roll-off as the Kirk effect occurs. The devices with a 125 nm InP collector exhibit a peak $f_{MAX}$ at the bias of $V_{CE} = 1.4V$ whereas devices with a 150 nm InP collector show a peak $f_{MAX}$ at the bias of $V_{CE} = 1.6V$.

Fig. 3.65 shows $f_T$ and $f_{MAX}$ as a function of collector current for $0.6 \times 11.5 \mu m^2$ devices from each wafer at the collector emitter bias of $V_{CE} = 1.6 V$. Under this bias, the InP collector is depleted in both devices. Fundamental differences in device performance are highlighted at high current densities, when the Kirk limit is exceeded in the thicker collector device, bringing about a precipitous roll-off of $f_T$ and $f_{MAX}$ with increasing current levels. On the contrary, the 125 nm collector transistor shows
$f_{\text{MAX}} < f_T$ due to the higher base-collector capacitance but maintains a better performance at high current densities.

![Graph showing cutoff frequency as a function of collector current](image)

**Figure 3.64** Current gain cut-off frequency maximum oscillation frequency as a function of collector current for $0.6 \times 11.5 \mu m^2$ devices with the collector thickness of 125 nm. $V_{CE}$ was set to 1.4 V.

Similar devices with different base undercut etching and with various base metallization contact widths were also fabricated on the wafer with a 125 nm InP collector. Table 3.9 summarizes the RF performance of these devices. Devices with $W_B = 2 \mu m$ base metallization contact show lower $f_T$ and $f_{\text{MAX}}$ values than those with 1.25 $\mu m$ base metallization contact. The devices with undercut of $\sim 0.75 \mu m$ by aggressive base over-etching show higher $f_T$ values than those with $\sim 0.45 \mu m$ base undercut over-etching. The measured base contact resistivity determined from linear TLM patterns is $\sim 4 \times 10^{-7} \Omega \cdot \text{cm}^2$, corresponding to a calculated total base resistance of $R_B \sim 19.4 \Omega$, according to the device geometry shared by all transistors. The $R_B$ value extracted from RF measurements is in good agreement, showing a value of $R_B = 20 \Omega$.

In the simplest approximation, the maximum oscillation frequency $f_{\text{MAX}}$ is related to $f_T$ by
\[ f_{\text{MAX}} = \sqrt{f_T / (8\pi R_B C_{\text{CB}})} \] \hspace{1cm} (3.5)

![Graph showing frequency vs collector current for different collector thicknesses.](image)

**Figure 3.65** Current gain cut-off frequency and maximum oscillation frequency as a function of collector current for 0.6 × 11.5 µm² devices with collector thickness of 125 and 150 nm, respectively. \( V_{CE} \) was set to 1.6 V.

Table 3.9 shows the effective \( R_B C_{\text{CB}} \) products determined from the measured \( f_T \) and \( f_{\text{MAX}} \) values, as well as the corresponding \( C_{\text{CB}} \). It is found that all the devices show very similar base-collector capacitances \( \sim 7 - 8 \) fF, regardless of very different amounts of base contact undercut etching. In other words, the extrinsic base capacitance \( C_{\text{CBX}} \) only plays a secondary role in determining \( f_{\text{MAX}} \), and the intrinsic capacitance \( C_{\text{CBI}} \) dominates. This observation is in good agreement with the analysis of Kurishima [85].

Although an aggressive base over-etching to reduce the total base-collector junction area does not directly reduce the effective \( R_B C_{\text{BC}} \) value which determines \( f_{\text{MAX}} \), Table 3.9 shows that it is beneficial to increase \( f_T \): for the 125 nm collector, reducing \( W_B \) and \( W_S \) can result in substantial improvements of \( f_T \), leading to an increase of 60 GHz/µm of extrinsic base/collector width reduction.
Table 3.9 Undercut effects on $f_T$ and $f_{MAX}$ of the devices with 125 nm collector.

<table>
<thead>
<tr>
<th>Undercut (µm)</th>
<th>$W_B$ (µm)</th>
<th>$W_S$ (µm)</th>
<th>$f_T$ (GHz)</th>
<th>$f_{MAX}$ (GHz)</th>
<th>$f_T/(8\pi f_{MAX}^2)$ (fs)</th>
<th>$C_{CB}$ (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.45</td>
<td>1.25</td>
<td>0.8</td>
<td>360</td>
<td>313</td>
<td>146.283</td>
<td>7.3</td>
</tr>
<tr>
<td>0.45</td>
<td>2</td>
<td>1.55</td>
<td>313</td>
<td>278</td>
<td>161.226</td>
<td>8.06</td>
</tr>
<tr>
<td>0.75</td>
<td>1.25</td>
<td>0.5</td>
<td>377</td>
<td>318</td>
<td>149.592</td>
<td>7.48</td>
</tr>
<tr>
<td>0.75</td>
<td>2</td>
<td>1.25</td>
<td>325</td>
<td>288</td>
<td>155.984</td>
<td>7.8</td>
</tr>
</tbody>
</table>

In conclusion, the developments presented here show, for the first time since the demonstration of 300 GHz transistors by Dvorak et al. [31], that a balanced performance can be achieved in InP/GaAsSb DHBTs even without aggressive lithographic scaling. The extent of the progress can be better assessed by noting that Chu-Kung et al. reported $0.38 \times 8$ µm² devices with $f_T = 358$ GHz and $f_{MAX} = 194$ GHz with $BV_{CEO} = 4.2$ V and a current gain of $\beta = 19$ in an electron beam lithography process [39].

The present results suggest that transistors with $f_T$ and $f_{MAX}$ approaching 400 GHz should be possible in an all-optical process if the total base resistance can be further reduced. In this context, optical lithography has already permitted the demonstration of devices with $f_T = 384$ GHz [32]. From the base resistance point of view, assuming base recombination is dominated by Auger processes would suggest a doubling of the base doping level would be accompanied by a 4-fold gain reduction [86], leading to an expected $\beta = 15$ for a 600 Ω/□ base sheet resistance. There are however some indications that Auger might not be dominant in GaAsSb materials grown by different methods or with alternate precursors as in [83], permitting one to anticipate even more favorable potential outcomes. In any case, the present current gain levels should comfortably allow for a reduction of the base sheet resistance to values 700-800 Ω/□.
3.3 Collector Optimizations

3.3.1 Collector Doping Spike

For the conventional design of bipolar junction transistors, a doping spike is usually introduced in the collector layer to suppress Kirk effect, which causes the base push-out and the roll-off of $f_T$. InP/GaAsSb DHBTs feature a high current $f_T$ roll-off due to a completely different physical mechanism. No classical base push-out as in homojunction collectors can take place in InP/GaAsSb DHBTs because of the large valence band discontinuity $\Delta E_V \approx 0.78 \text{ eV}$ \cite{59, 87} between the GaAsSb base and the InP collector. The “Kirk-like” $f_T$ roll-off at high current densities in InP/GaAsSb DHBTs was clarified to take place when base/collector electric field collapses due to the traveling electron space charge in the collector \cite{88}. When a higher collector current density is forced through the transistor, the electric field reverses at the base/collector heterojunction, resulting in an induced electrostatic barrier which slows down the flow of electrons from the GaAsSb base to the InP collector.

In this section, we study the doping spike effect on the DC and RF performances as well as the Kirk current of the DHBTs. The epilayers used here consist of a 70 nm $n$-type InP emitter doped at $3 \times 10^{17} \text{ cm}^{-3}$, a 20 nm uniform C-doped Ga$_{0.56}$As$_{0.44}$Sb base layer at $8 \times 10^{19} \text{ cm}^{-3}$, and a 200 nm $n$-type InP collector at $2 \times 10^{16} \text{ cm}^{-3}$ (Bol89). Two additional wafers (Bol91 and Bol92) were used with the only difference in structure having the doping spike layers inserted in the collector. The doping spike layers consist of 20 nm thick InP:Si doped at $5.5 \times 10^{17} \text{ cm}^{-3}$, which are located at a distance of 140 nm and 40 nm from the base/collector interface, for sample Bol91 and Bol92, respectively. DHBTs with the emitter area of $80 \times 80 \text{ µm}^2$ were fabricated from these three wafers using the QHBT process as presented in Chapter 2. The doping profile in the collector has been verified by capacitance-voltage measurements applied at the base/collector junction of DHBTs with the emitter area of $80 \times 80 \text{ µm}^2$.

The gain versus the collector current from DHBT with the emitter area of $80 \times 80 \text{ µm}^2$ on these wafers is shown in Fig. 3.66. An identical current gain was observed for all these structures. Because the gain is determined by the electron lifetime and transit time in the base (when the collector current density is far below the Kirk current...
density), and because in our case the emitter and base layers are the same for the three wafers, the presence of the doping spike in the collector layer does not affect the DC gain of devices with the emitter area of $80 \times 80 \, \mu m^2$. The overlapping curves again demonstrate the excellent reproducibility of the wafer growth and the device fabrication process.

*Figure 3.66  Gain versus the collector current on transistors with an emitter area of $80 \times 80 \, \mu m^2$ calculated from Gummel measurements.*

In order to see how the doping spike layer affects the device Kirk current and high frequency performances, DHBTs with emitter areas of $0.6 \times 11.5 \, \mu m^2$ and $1 \times 23.5 \, \mu m^2$ were fabricated using the standard triple mesa wet etching process and optical contact lithography. Fig. 3.67 depicts the Gummel plots of DHBTs with an emitter area of $1 \times 23.5 \, \mu m^2$ for the three wafer structures. The collector currents overlap for the three transistors while the base current of Bol89 in the high bias region is higher than that of the other two samples. This behavior is attributed to the Kirk effect which occurs at lower collector currents in Bol89. The gain versus the collector current for the three transistors is shown in Fig. 3.68. The two DHBTs with the doping spike layer in the collector (Bol91, Bol92) show a much higher Kirk current than the devices with a uniform collector (Bol89). The DHBTs with the doping spike...
Figure 3.67  Gummel plots of transistors with the emitter area of $1 \times 23.5 \, \mu m^2$.

Figure 3.68  Gain versus the collector current on transistors with the emitter area of $1 \times 23.5 \, \mu m^2$ calculated from the Gummel measurements.
layer inserted at the distance of 40 nm (Bol92) from the base/collector interface shows a larger Kirk current as compared to the DHBTs with the doping spike layer placed at 140 nm from the base/collector interface (Bol91).

The short-circuit current gain $|h_{21}|^2$ and Mason’s unilateral gain $U$ as a function of frequency is respectively shown in Fig. 3.70(a) and (b), for devices with $0.6 \times 11.5 \, \mu\text{m}^2$ emitter area biased at $V_{CE} = 1.6 \, \text{V}$. The Kirk current for Bol89, Bol91 and Bol92 is 17.6, 23.6 and 28.6 mA, respectively, corresponding to a Kirk current density of 2.55, 3.42 and 4.14 mA/$\mu\text{m}^2$, respectively. Sample Bol89 features a Kirk current density 1.6× higher than Bol92. This is due to the 40 nm distance of the doping spike layer from the base/collector interface in Bol92. According to Ref. [89], the collector current density at the onset of Kirk effect is:

$$J_K = qv_{sat} [N_C + \frac{2(V_{CB} + \phi_{bi})E}{qW_c^2}]$$  \hspace{1cm} (3.6)

where $v_{sat}$ is the electron velocity (which is often assumed to be constant and equal to the electron saturation velocity $v_{sat}$ for analytical expressions, due to the high electric fields in the collector), $V_{CB}$ is the applied reverse bias to BC junction, $W_c$ is the collector thickness, and $\phi_{bi}$ is the built-in voltage of the BC junction, $N_C$ is the collector doping concentration assuming the donors are fully ionized and that hole concentration in the collector is neglected. According to this equation, Kirk current density is calculated to be 2.6 mA/$\mu\text{m}^2$ for Bol89 with $v_{sat}$ assumed to be $4 \times 10^7 \, \text{cm/s}$. This Kirk current is in good agreement with the experimental results. For Bol91 and Bol92, Kirk current density is derived from Poisson’s equation in the following paragraph.

Fig. 3.69 shows the doping profiles of Bol91 and Bol92. Here $w_1$ and $w_2$ represent the starting and end positions of the doping spike layer doped at $5 \times 10^{17} \, \text{cm}^{-3}$ ($N_s$). The doping level elsewhere in the collector is $N_0 = 2 \times 10^{16} \, \text{cm}^{-3}$. Since in type II InP/GaAsSb DHBTs, the electric field inversion related to the Kirk effect occurs at a distance of $x_0 = 20 \, \text{nm}$ from the B/C interface. This implies that $E(x_0) = 0$ according to [90]. The region between this zero-electric field point and the B/C interface acts as a barrier for the electrons. The collector region is divided into three regions: $0 < x < w_0$ (Region I), $w_1 < x < w_2$ (Region II) and $w_2 < x < W_c$ (Region III).
According to Poisson’s equation and $\int_0^{w_C} Edx = -(V + \phi_b)$, we obtain

$$
\begin{align*}
\phi_x &= \frac{N_s[(w_1 - \xi)^2/2 - \xi^2/2] + N_0(w_1^2/w_0^2/2 + (N_0 - N_0)(w_1 - w_0) - N_0\xi_0(w_1 - w_0) + N_0(w_1^2/w_0^2)/2 + (N_0 - N_0)(w_1 - w_0) - N_0\xi_0(w_1 - w_0) + d\phi_d + d\phi_b)/q}{(w_1^2/2 - \xi_0^2)} \\
\end{align*}
$$

Replacing $w_1$ with 140 nm and 40 nm, the electron densities for Bol91 and Bol92 calculated with Eqn. 3.7 are $7.9 \times 10^{16}$ and $1.45 \times 10^{17}$ cm$^{-3}$, respectively, corresponding to current densities of 5.0 and 9.3 mA/µm$^2$ for Bol91 and Bol92, respectively. These values are higher than the values obtained from the experiment.
Figure 3.70 (a) $|h_{21}|^2$ and (b) Mason’s unilateral gain $U$ as a function of frequency on DHBTs with the emitter area of $0.6 \times 11.5 \, \mu m^2$ for the three wafer structures.

The disagreement between the calculated and the experimental results may be due to the fact that the electron saturation velocity was assumed to be constant in this
calculation. The electron velocity in the collector depends on the electron position, as discussed in Ref. [91] and should thus be considered in the calculation of the Kirk current.

The current-gain cut-off frequency $f_T$ is nearly the same for all three transistor structures. On the other hand, the maximum oscillation frequency $f_{\text{MAX}}$ of Bol89 is higher than that of the other two samples as shown in Fig. 3.70. The lower expected charging time due to the higher Kirk current density in Bol91 and Bol92 should increase the current-gain cutoff frequency $f_T$. Unfortunately, the experiments did not reveal an improved $f_T$. Due to the doping spike layer in the collector, a higher base/collector capacitance is expected, as well as a higher Kirk current density. According to Eqn. 3.3, the total emitter to collector transit time in samples Bol91 and Bol92 might not vary much due to the simultaneous increase of the BC capacitance, the collector transit time and the Kirk current in the structures. The increased BC capacitance is also indicated by the decrease of $f_{\text{MAX}}$ for Bol91 and Bol92. The doping spikes effect on the transistor performances is summarized in Table 3.10.

<table>
<thead>
<tr>
<th>Wafer No.</th>
<th>Dev. No.</th>
<th>$f_T$ (GHz)</th>
<th>$f_{\text{MAX}}$ (GHz)</th>
<th>$I_C$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bol89</td>
<td>66B1</td>
<td>193</td>
<td>227</td>
<td>17.6</td>
</tr>
<tr>
<td>Bol91</td>
<td>66B1</td>
<td>183</td>
<td>162</td>
<td>23.6</td>
</tr>
<tr>
<td>Bol92</td>
<td>66B1</td>
<td>192</td>
<td>176</td>
<td>28.6</td>
</tr>
</tbody>
</table>

The measured $BV_{CEO}$ breakdown characteristics for the various collector doping profile designs are shown in Fig. 3.71. Clearly, such doping spikes have a minimal impact on the breakdown voltage $BV_{CEO}$. This is to be contrasted with the behavior of type-I DHBTs which require heavy doping near the collector grading region.
3.3 Collector Optimizations

3.3.2 Collector Thickness Effect

Increasing of HBT bandwidth can be realized by reducing the RC charging time and the electron transit time according to Eqn. 3.3. The electron transit time is primarily determined by the base and collector layer thicknesses. A reduction of the collector layer thickness however leads to an increase of the base/collector capacitance and therefore of the RC charging time. Furthermore, a decrease of the lateral device dimensions also decreases the base/collector and base/emitter capacitances, but increases the emitter resistance and thus the RC charging time. Hence, a trade-off between the vertical and lateral scaling has to be considered in order to improve the device high-frequency performances.

Type II GaAsSb DHBTs with \( f_T > 670 \) GHz has been demonstrated by Snodgrass et al. [38] on a DHBT structure with a 20 nm thick base and a 60 nm thick collector. In this section, we investigate the RF performance of DHBTs with a 20 nm thick base layer and collector thicknesses of 75, 125 and 150 nm. Transistors with a base and collector thickness of 15 nm and 50 nm, respectively, were fabricated. Device manufacturing techniques relied on e-beam lithography to define the emitter widths of 0.2, 0.3 and
0.4 µm and the base widths of 0.3 and 0.4 µm. The details for the transistor fabrication process were discussed in Chapter 2.

The short-circuit current gain $|h_{21}|^2$ at peak $f_T$ bias as a function of frequency is shown in Fig. 3.72 for DHBTs with the emitter area of $0.4 \times 8.4 \, \mu m^2$ devices and collector thicknesses of 75, 125 and 150 nm. Current-gain cut-off frequency $f_T$ enhancement from 340 GHz to 432 GHz is observed when the collector thickness is reduced from 150 nm to 75 nm.

Table 3.11 shows the collector transit time, the total emitter charging time and the respective charging time components, extracted from the measured S-parameters. The total electron transit time in the collector is reduced from 263 to 171 fs when the collector thickness decreases from 150 to 75 nm. For transistors with a collector thickness of 75 nm, the total charging time (120.3 fs) is far less than the collector transit time (170.81 fs). This suggests that an additional vertical scaling down of transistors with emitter area of $0.4 \times 8.4 \, \mu m^2$ can further reduce the collector transit time. RF performance of DHBT with an emitter size of $0.4 \times 8.4 \, \mu m^2$, a 15 nm base and a 50 nm thick collector is shown in Fig. 3.73. The peak $f_T$ of 475 GHz was the highest current-gain cut-off frequency measured in this work. This result is not in agreement with that reported in Ref. [92], wherein $f_T$ increase was obtained by decreasing the collector thickness from 300 nm to 75 nm, but dropped abruptly when the collector thickness was further decreased to 50 nm due to impact ionization.

To investigate the vertical scaling limit of the devices fabricated in this work, the cut-off frequencies, the collector transit times and the total charging times with their respective components were plotted versus the collector thickness in Fig. 3.74.
3.3 Collector Optimizations

(a) $V_{CE} = 1 \text{ V} \quad I_B = 0.7 \text{ mA} \quad K8$

$0.4 \times 8.4 \mu \text{m}^2$

$X_C = 75 \text{ nm}$

Bol286 $|h_{21}|^2 \quad f_T = 432 \text{ GHz}$

(b) $V_{CE} = 1.4 \text{ V} \quad I_B = 0.4 \text{ mA} \quad K8$

$0.4 \times 8.4 \mu \text{m}^2$

$X_C = 125 \text{ nm}$

Bol333 $|h_{21}|^2 \quad f_T = 367 \text{ GHz}$
Figure 3.72 $|h_{21}|^2$ as a function of frequency for DHBTs with emitter area of $0.4 \times 8.4 \, \mu m^2$ and with collector thicknesses of (a) 75 nm (b) 125 nm and (c) 150 nm.

Table 3.11 Collector transit time, total charging time with its respective charging time components calculated with the extracted physical parameters from measured S parameters of $0.4 \times 8.4 \, \mu m^2$ transistors with a 20 nm base and collector thicknesses of 75, 125 and 150 nm. The corresponding values for devices with an emitter area of $0.4 \times 8.4 \, \mu m^2$, and a base and collector thickness of 15 and 50 nm are used for comparison.

<table>
<thead>
<tr>
<th>Collector Thickness (nm)</th>
<th>Device No.</th>
<th>$I_C$ (mA)</th>
<th>$f_T$ (GHz)</th>
<th>$\frac{kT}{qI_C}C_{BE}$ (fs)</th>
<th>$\frac{kT}{qI_C}C_{BC}$ (fs)</th>
<th>$R_{E-C_{BE}}$ (fs)</th>
<th>$R_{C-C_{BC}}$ (fs)</th>
<th>Total Charging Time (fs)</th>
<th>Collector Transit Time (fs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>75</td>
<td>Bol286</td>
<td>35.43</td>
<td>432</td>
<td>51.8</td>
<td>11.5</td>
<td>38.2</td>
<td>17.8</td>
<td>120.3</td>
<td>170.8</td>
</tr>
<tr>
<td>125</td>
<td>Bol333</td>
<td>24.28</td>
<td>368</td>
<td>77.7</td>
<td>8.7</td>
<td>23.7</td>
<td>9.19</td>
<td>119.7</td>
<td>235.5</td>
</tr>
<tr>
<td>150</td>
<td>Bol332</td>
<td>18.51</td>
<td>340</td>
<td>89.8</td>
<td>9.1</td>
<td>21.2</td>
<td>7.75</td>
<td>127.9</td>
<td>263</td>
</tr>
<tr>
<td>50</td>
<td>Bol206</td>
<td>28.1</td>
<td>475</td>
<td>62.9</td>
<td>19.8</td>
<td>41.8</td>
<td>25.6</td>
<td>150.1</td>
<td>145.1</td>
</tr>
</tbody>
</table>
3.3 Collector Optimizations

**Figure 3.73** $|h_{21}|^2$ versus frequency on DHBTs with an emitter area of $0.4 \times 0.3 \mu m^2$ and base and collector thickness of 15 nm and 50 nm, respectively.

**Figure 3.74** Collector transit time, total charging time and the respective components of the charging time plotted versus the collector thickness for DHBTs with a 20 nm thick base. Values for devices with a 15 nm thick base and a 50 nm thick collector were also plotted for comparison.
The collector transit time is higher than the total emitter charging time for DHBTs with 75, 125 and 150 nm collector thicknesses. The collector transit time decreases as the collector thickness is reduced from 150 nm to 50 nm. The total charging time increases when the collector thickness is reduced from 75 nm to 50 nm while it is nearly constant for collector thicknesses between 75 nm and 150 nm. At a collector thickness of 50 nm, the total charging time becomes larger than the collector transit time. This implies that a lateral scaling down is required to further increase the current gain cut-off frequency $f_T$.

The component $kTC_{BE}/qI_C$ of the total charging time is dominant and decreases with decreasing collector thickness, because of the Kirk current increase. Consequently, both an increase of the Kirk current and a decrease of the emitter/base capacitance can contribute to enhance $f_T$. The unexpected lower Kirk current for the transistor with 50 nm collector is probably due to the 150 nm thick pedestal InP layer and the 10 nm InGaAs which features a lower thermal conductivity [93].
Figure 3.75 $|h_{21}|^2$ and $U$ as a function of frequency for devices with a collector thickness of 75 nm, with base widths of 0.3 and 0.4 µm, and with emitter areas of (a) $0.3 \times 8.4 \text{ µm}^2$, (b) $0.4 \times 8.4 \text{ µm}^2$ and (c) $0.5 \times 8.4 \text{ µm}^2$. 
Fig. 3.75 shows the RF performances of the devices with a collector thickness of 75 nm and with base widths of 0.3 and 0.4 µm and the emitter sizes of (a) $0.3 \times 8.4 \, \mu m^2$, (b) $0.4 \times 8.4 \, \mu m^2$ and (c) $0.5 \times 8.4 \, \mu m^2$.

The maximum oscillation frequency $f_{\text{MAX}}$ can be expressed as: $f_{\text{MAX}}^2 = f_t / 8 \pi R_b C_{\text{BC,I}}$, where $C_{\text{BC,I}}$ stands for the intrinsic base/collector capacitance. Table 3.12 shows the ratio $f_{\text{MAX}}^2/f_t = F$ for various emitter and base sizes. This ratio depends primarily on the emitter width and increases when the emitter width reduces, which indicates that further lateral scaling improves $f_{\text{MAX}}$. The ratio is almost independent on the base metal width: in other words, there is almost no dependence on the extrinsic base/collector capacitance $C_{\text{CB,x}}$. This agrees well with the analysis of Kurishima [85], which claims that the external collector capacitance has only a small impact on $f_{\text{MAX}}$.

The base contact width has a decreasing effect on the total transistor delay time as the emitter width is enlarged, as seen by the numbers of the total delay time difference as listed in the last column of Table 3.12. This seems to come about because the $RC$ delay contributions to $\tau_T$ are:

$$r_E(C_{\text{BE}} + C_{\text{CB,I}} + C_{\text{CB,x}}) + (R_C + R_E)(C_{\text{CB,I}} + C_{\text{CB,x}}).$$

The emitter (forward-bias) capacitance $C_{\text{BE}}$ and its value per unit area is much higher than $C_{\text{CB,I}}$ or $C_{\text{CB,x}}$, and it appears to dominate the $RC$ contributions in wider emitters. In the narrower emitters, $(r_E + R_E)C_{\text{CB,x}}$ becomes relatively more important and it is helpful to maintain a low $C_{\text{CB,x}}$ and maximize $f_t$.

<table>
<thead>
<tr>
<th>$W_E$ (µm)</th>
<th>$W_B = 0.3$ µm (GHz)</th>
<th>$W_B = 0.4$ µm (GHz)</th>
<th>Total Delay Time Difference (fs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3</td>
<td>215.0</td>
<td>214.7</td>
<td>24</td>
</tr>
<tr>
<td>0.4</td>
<td>152.8</td>
<td>158.6</td>
<td>17</td>
</tr>
<tr>
<td>0.5</td>
<td>126.9</td>
<td>129.1</td>
<td>9.5</td>
</tr>
</tbody>
</table>

The extracted total base resistances are plotted versus the emitter/base junction width in Fig. 3.76. The total base resistance increases as the emitter size increases from 0.3 µm to 0.5 µm due to the associated increase of the base spreading resistance. The
transistors with 0.3 µm base contacts width feature a higher total base resistance, because the narrower base contact metal introduces a higher base metal resistance. The total base resistance increases from 16.3 Ω to 19 Ω by decreasing the base width from 0.4 µm to 0.3 µm for an emitter width of 0.4 µm. On the other hand, the total base resistance increases from 16.3 Ω to 17.3 Ω when the emitter width is increased from 0.4 µm to 0.5 µm at a base width of 0.4 µm. This implies that the total base resistance can be effectively reduced by increasing the base contact metal width. It provides a way for further $f_{\text{MAX}}$ improvement: decreasing the base contact metal resistance for DHBTs fabricated by electron beam lithography in this work.

Figure 3.76  Extracted base resistance versus emitter size for devices with base widths of 0.3 and 0.4 µm.
Noise Figure

Characterization of InP/GaAsSb DHBTs

We characterize the minimum noise figure of InP/GaAsSb DHBTs with AlInAs and GaInP emitters. AllInAs/GaAsSb/InP devices fabricated by optical contact lithography feature cutoff frequencies $f_T = 210 \text{ GHz}$ and $f_{\text{MAX}} = 127 \text{ GHz}$, and achieve a minimum noise figure $NF_{\text{min}} < 3 \text{ dB}$ with an associated gain $G_A = 12 \text{ dB}$ at 10 GHz. The (Ga,In)P/GaAsSb/InP DHBTs with 0.3 µm wide emitter feature common emitter current gain of 46 and cutoff frequencies $f_T = 400 \text{ GHz}$ and $f_{\text{MAX}} = 322 \text{ GHz}$ for devices implemented with a 20 nm base and a 75 nm InP collector. The DHBTs feature attractive noise properties with an unprecedented minimum noise figure $NF_{\text{min}} = 1.2 \text{ dB}$ at 20 GHz which is nearly independent of frequency over the 2-20 GHz band. The AlInAs/GaAsSb/InP DHBTs fabricated by electron beam lithography features a minimum noise figure of 2.34 dB and a peak cutoff frequency $f_T$ of 270 GHz. The minimum noise figure was found to be strongly dependent on the base contact resistance. The latter is mostly controlled by the surface treatment prior to the base contact deposition.
4.1 Noise Figure of DHBTs with AlInAs Emitter

InP-based heterojunction bipolar transistors (HBTs) have been widely investigated for high-speed electronic applications. InP/GaAsSb based DHBTs emerged as a viable alternative to InP/GaInAs DHBTs by exploiting the type-II band alignment between GaAsSb and InP, which allows the direct injection of electrons from the GaAsSb base layer into the InP collector without requiring grading at the base/collector heterojunction [31].

To date, InP/GaAsSb DHBTs provide the highest $f_T \times B V_{CEO}$ product of any bipolar transistor technology with a value of 2.5 THz-V at 300 K [35]. Although such devices were principally intended for application in high-speed digital circuits [91], lower frequency devices could also prove interesting in long talk-time, battery-driven, telecom applications owing to their low turn-on voltages: GaAsSb based transistors require a base-emitter voltage that is ~0.7 V (~0.1 V) lower than required in a GaAs (SiGe)-based HBT to establish a given collector current density.

In contrast to other transistor technologies, relatively little is known to date about the microwave noise properties of GaAsSb–based DHBTs [94] [95]. The noise properties of “type-II” emitter of InP/GaAsSb/InP DHBTs (i.e. with an InP emitter) were first characterized by Ehrich et al., and showed minimum noise figures of ~7.5 dB between 2-18 GHz for devices operating at $J_C = 1$ mA/µm$^2$ (and 4-6 dB at 0.1 mA/µm$^2$) [94]; while Chuang et al. later reported a minimum noise figure $NF_{\text{min}} = 5$ dB at 18 GHz in 0.3 × 3 µm$^2$ devices operating at with a peak $f_T = 370$ GHz bias at 4 mA/µm$^2$ [95]. The frequency dependence of noise characteristics was not reported in [95], but the authors identified their low current gain ($\beta < 20$) as a main noise performance limiter [95]. The noise properties of AlInAs/GaAsSb/InP DHBTs with a “type-I” AlInAs emitter have no yet been reported and are the focus of this work. The study is of interest because the higher current gain achieved with an AlInAs emitter should lead to improved noise characteristics.

The epitaxial layers were grown at Agilent Technology (Santa Rosa, California) by molecular beam epitaxy (MBE) on a 3-inch semi-insulating InP substrate. Silicon and carbon were the donor and acceptor species. The C-doped 15 nm GaAs$_{0.51}$Sb$_{0.49}$ base
layer is doped at $8 \times 10^{19} \text{cm}^{-3}$. The base sheet resistance is $\sim 1470 \ \Omega/\square$. 0.9 × 11.5 µm² emitter devices were fabricated by optical lithography in a triple-mesa HBT process where the emitter/base junction mesa sidewall is passivated by a PECVD SiN film.

The DC characteristics were measured with an HP4156B semiconductor parameter analyzer. Fig. 4.1 shows the Gummel and current gain characteristics, and indicates that a low $V_{BE} = 0.45 \text{V}$ leads to a current density of $J_C = 10^{-5} \text{mA/µm}^2$ (while GaAs HBTs require $V_{BE} = 1.1 \text{V}$ to achieve the same $J_C$). The peak current is $\beta = J_C/J_B = 60$, and the $BV_{CEO}$ is $\sim 4.5 \text{V}$.

![Figure 4.1](image)

**Figure 4.1** Gummel and gain characteristics for 0.9 × 11.5 µm² SiN passivated DHBT. The plot of current gain versus collector current density is also shown.

The transistor microwave performance was characterized up to 40 GHz with an HP8510C vector network analyzer using an off-wafer LRRM calibration. The peak current gain cutoff and the maximum oscillation frequencies are $f_T = 210 \text{GHz}$ and $f_{MAX} = 127 \text{GHz}$ at a bias of $V_{CE} = 1 \text{V}$ and $J_C = 3 \text{mA/µm}^2$, as determined by -20 dB/dec extrapolations of the common-emitter current gain $|h_{21}|^2$ and of Mason’s unilateral power gain $U$. The noise performance was characterized at $V_{CE} = 1 \text{V}$ from 2 to 20 GHz with a cascade NPT26 noise parameter test system including an
HP8970B noise figure meter and an HP8971C frequency converter. Fig. 4.2 shows the frequency dependence of the minimum noise figure $NF_{\text{min}}$ and associated gain $G_A$ with the collector current density as a parameter. The corresponding $f_T$ is shown in the Figure for each bias condition. $NF_{\text{min}}$ is largely independent of frequency because, in all cases, the measurement range is much lower than the device $f_T$. At low bias, an $NF_{\text{min}} < 3$ dB is achieved at 10 GHz with $G_A = 12$ dB.

![Figure 4.2](image)

**Figure 4.2** Minimum noise figure and associated gain against frequency measured at collector current densities of $J_C = 0.32$, 0.51, 1.37 and 2.24 mA/µm². The corresponding $f_T$ values were 102, 130, 182, 210 GHz.
Fig. 4.3 shows that the noise resistance $R_n$ is almost independent of $J_C$ and remains $< 50 \, \Omega$ over the measurement range. At peak $f_T$ bias, the device $S$-parameter data revealed that $R_E = 6.6 \, \Omega$, while the total base resistance amounts to $R_B = 9.8 \, \Omega$.

It is not straightforward to adequately compare the noise performance of bipolar transistors across different technologies because noise parameters depend on device gain, bandwidth, as well as on geometry. In comparison to InP/GaInAs SHBTs, the present devices offer nearly a 2 dB advantage at a current density of 0.5 mA/µm$^2$ for similar $G_A$ at 10 GHz [96], but they show a 1.0–1.5 dB higher low current noise at 1 GHz. InP/GaInAs DHBTs were reported with $NF_{\text{min}} = 2.2$ dB at 18 GHz [95]. The present devices achieve much improvement over [94] and a similar $NF$ to the smaller and faster InP/GaAsSb DHBTs of [95] despite the larger emitter widths used here (0.9 compared to a 0.3 µm emitter width in [95], thanks to the improved current gain achieved with the AlInAs type-I emitter chosen for this work. This noise performance still does not approach the best SiGe HBT results, which show $NF_{\text{min}} < 1$ dB at 10 GHz owing to aggressive device scaling and higher current gains with $\beta \sim 200$ [97]. SiGe HBTs however do suffer from a rapid increase of $NF_{\text{min}}$ owing to impact
ionization noise as $V_{CE}$ exceeds the $BV_{CEO}$ [7]. In this context, high-speed high-$BV_{CEO}$ GaAsSb DHBTs with AlInAs or InP emitters could become an interesting alternative to SiGe HBTs in higher frequency bands where the reduced $BV_{CEO}$ of high-speed SiGe HBTs can be expected to result in excessive noise levels.

To summarize, the first characterization of microwave noise in AlInAs/GaAsSb/InP DHBTs with a $0.9 \times 11.5 \mu m^2$ ‘type-I’ AlInAs emitter is reported. Our DHBTs feature a peak current gain of $\beta \sim 60$, peak cutoff frequencies $f_t/f_{MAX} = 210/127$ GHz, and are characterized by an $NF_{\min} < 3$ dB with $G_A = 12$ dB at 10 GHz for low bias operation, thanks to the improved current gain associated with the use of an AlInAs ‘type-I’ emitter. The measured $NF_{\min}$ values exceed those predicted from first-order transistor noise models, and future work should involve the decomposition of the noise components in order to clearly identify the different contributions.

### 4.2 Noise Figure of Transistors with (Ga,In)P Emitter

The development of InP/GaAsSb/InP-based double heterojunction bipolar transistors (DHBTs) was initiated for long-talk time wireless applications [98], but its focus rapidly shifted to the realization of ultrahigh-speed devices intended for digital circuits for optical fiber communication [91] and test equipment [99] applications. This focus shift followed naturally from the simplified collector implementation associated with the formation of abrupt grading-free heterojunctions between GaAsSb bases and InP wide-bandgap collectors. As a result, relatively little attention has been given to the analog properties of InP/GaAsSb DHBTs in general. In particular, few works so far have focused on the microwave noise properties of InP/GaAsSb DHBTs [95] [100] [101]. Although InP/GaAsSb DHBTs can exhibit attractive cutoff frequencies, their reported minimum noise figures have been high (e.g., $NF_{\min} = 3.5 \sim 4.5$ dB at 10 GHz) and were attributed to high base current levels. Such a performance is not competitive with $NF_{\min}$ values available in III–V HEMTs, high-performance SiGe-based HBTs, or even modern RF CMOS [102].

Achieving good $NF_{\min}$ values in HBTs proves challenging because bipolar transistors inherently are high-current drive devices whose performance peaks at high current
densities. Consequently, they are subject to high shot noise levels when operated near their peak $f_T$ bias [43]. In order to achieve good microwave noise characteristics, bipolar transistors must therefore be downscaled while maintaining a high current gain, in order to minimize both the collector current and base current levels. Device parasitics must also be minimized to preserve acceptable gain and bandwidth under low current operation. SiGe-based HBTs have managed this evolution exceedingly well by exploiting the aggressively scaled device geometries and the high current gain levels afforded by silicon process technology [43].

In this section, we describe 400 GHz InP/GaAsSb DHBTs featuring minimum noise figures $NF_{\text{min}} = 1.2$ dB with an associated gain of 10 dB at 20 GHz. This is an improvement of at least 2.3 dB with respect to previously reported values for GaAsSb based DHBTs [95], [100]. This unprecedented performance was enabled by the introduction of an InP/GaInP composite emitter which enables small-area devices to maintain usable gain and a good RF performance under low current operating conditions necessary to achieve low-noise figures [34], [77].

The epitaxial layer structure employed in this work and the details of the fabrication process are described in Chapter 2. Transistors were fabricated in a standard triple-mesa process. The emitter and base metal contacts were defined by electron-beam lithography. An emitter junction width of $\sim 0.3 \, \mu m$ was formed by a combination of dry and wet etching. The 0.3 \, \mu m wide base electrodes were self-aligned to the emitter contact. The transistor emitter-base mesa was passivated with SiN deposited by low-temperature PECVD. The GaAsSb base mesa was formed by a combination of dry and wet etching cycles which led to a 0.1 \, \mu m base metal undercut in order to reduce the extrinsic capacitance between the base and the collector. Micro-airbridges for the emitter and base contacts were used to minimize parasitic capacitances. A PMMA-based etch-back process was utilized to expose the emitter contact and the base and collector posts for the final metal interconnect. TLM measurements reveal an extrinsic base sheet resistance $R_{SH} \sim 1070 \, \Omega/\square$ and $\rho_C = 3 \times 10^{-7} \, \Omega \cdot \text{cm}^2$ base contact.
Fig. 4.4 shows representative Gummel characteristics for a device with a 0.3 × 3.4 μm² emitter area. The inset shows the corresponding common-emitter $I_C - V_{CE}$ characteristics. A SEM inspection confirmed the emitter mesa dimension of 0.3 μm and the base contact width of ~0.3 μm. The maximum DC current gain $\beta = I_C/I_B$ is 46 with $V_{CB} = 0$ V, due to the (Ga,In)P composite emitter [34], [77]. The collector and base current ideality factors are $n_C = 1.0$ and $n_B = 1.58$, respectively. All further data presented below come from the same transistor.

The DHBT microwave performance was characterized over the 45 MHz – 40 GHz frequency band with an HP8510C vector network analyzer using a line-reflect-reflect-match calibration and an off-wafer impedance standard. Pads were de-embedded with on-wafer open/short calibration structures.

Fig. 4.5 shows the short-circuit current gain $|h_{21}|^2$ and Mason’s unilateral gain $U$ as a function of frequency for the device in Fig. 4.4 that is biased at $V_{CE} = 1$ V and
$I_C = 8.74$ mA. Extrapolation of $|h_{21}|^2$ and $U$ with a $-20$ dB/dec roll-off yields cutoff frequencies $f_T = 400$ GHz and $f_{\text{MAX}}(U) = 322$ GHz. The total base and emitter resistances extracted from RF data are $R_B = 48 \Omega$ (consistent with the 46 $\Omega$ value calculated from the device geometry and the measured $R_{SH}$ and $\rho_C$) and $R_E = 62 \Omega$ (at $I_C = 0.48$ mA low-noise bias).

![Figure 4.5](image)

**Figure 4.5** $|h_{21}|^2$ and Mason’s unilateral gain $U$ as a function of frequency. (Inset) Scanning electron micrograph (SEM) showing the emitter and base contacts before base mesa etching.

The current gain cutoff frequency $f_T$ and maximum oscillation frequency $f_{\text{MAX}}$ as a function of collector current are shown in Fig. 4.6 for $V_{CE} = 1$ V. Even at a collector current density of 18.2 mA/$\mu$m$^2$, the transistor maintains cutoff frequencies of $f_T = 292$ GHz and $f_{\text{MAX}}(U) = 223$ GHz.
Figure 4.6  Evolution of $f_T$, $f_{\text{MAX}}$, and $N_{\text{Fmin}}$ and $G_A/5$ at 10 GHz with collector current for DHBT with the emitter area of $0.3 \times 3.4 \, \mu m^2$ biased at $V_{CE} = 1 \, V$.

The microwave noise performance was characterized from 2 to 20 GHz with a Cascade NPT26 noise parameter test system. Fig. 4.6 also shows the variation of $N_{\text{Fmin}}$ and $G_A$ with collector current at $V_{CE} = 1 \, V$ at 10 GHz. As expected, $N_{\text{Fmin}}$ increases with $I_C$, starting from low values at low current levels. Near peak $f_T$ bias conditions, the minimum noise figure and associated gain rise to $N_{\text{Fmin}} = 4.25 \, \text{dB}$ and $G_A = 26 \, \text{dB}$ at 10 GHz.

Fig. 4.7 details the frequency dependence of the minimum noise figure $N_{\text{Fmin}}$ and associated gain $G_A$ under low-noise bias conditions $I_C = 0.48 \, \text{mA}$ and $V_{CE} = 1 \, \text{V}$ ($I_B = 0.011 \, \text{mA}$). Because of the high $f_T$, $N_{\text{Fmin}}$ is nearly independent of frequency and exhibits an average value of $1.2(\pm 0.2) \, \text{dB}$ over the $10–20 \, \text{GHz}$ range. The associated gain is $G_A > 10 \, \text{dB}$ at 20 GHz. Under these noise bias conditions, the DHBT features $f_T = 127 \, \text{GHz}$ and $f_{\text{MAX}} = 186 \, \text{GHz}$. SiGe HBTs can offer noise figures of $0.2 \, \text{dB}$ and $1 \, \text{dB}$ at 10 and 20 GHz, respectively [103]. Commercial GaAs PHEMTs show $N_{\text{Fmin}} = 0.7 \, \text{dB}$ at 20 GHz [104]. The measured noise performance for
a 0.1 µm InP PHEMT fabricated in our laboratory is also included in Fig. 4.7 for comparison.

**Figure 4.7** $N_{F_{\text{min}}}$ and $G_A$ as a function of frequency under low-noise bias conditions. The solid curves are fitted to guide the eye. $N_{F_{\text{min}}}$ data from a 0.1 µm InP PHEMT that is fabricated in our group are also included for comparison (Source: Andreas Alt).

For low frequencies $f < f_T/\beta^{1/2} \approx 20$ GHz, the minimum noise figure $F_{\text{min}}$ can be approximated by Eqn. 4.1 [43, 102],

$$F_{\text{min}} = 1 + \frac{n_c}{\beta} + \sqrt{\frac{2 (R_B + R_E) I_C}{\beta V_T}}.$$  \hspace{1cm} (4.1)

The measured $F_{\text{min}} = 1.2$ dB (i.e., $F_{\text{min}} = 1.318$) shows that a 10× reduction of the $(R_B + R_E)/\beta$ factor would enable $N_{F_{\text{min}}} < 0.4$ dB based on the present performance. In the realm of III–V HBTs, it seems unrealistic to expect such a decrease of $(R_B + R_E)/\beta$ due to the limited current gain $\beta$ of high-speed III–V DHBTs. This stands in marked contrast with the situation in SiGe HBTs which can feature much higher current gain.
values $\beta > 1000$ [105]. We therefore expect that it will be difficult for InP/GaAsSb DHBTs to attain $NF_{\text{min}} < 1$ dB at low frequencies. However, for higher frequencies such as $f > f_T/\sqrt{\beta}$, $F_{\text{min}}$ increases linearly as expressed in Eqn. 4.2 [43]  

$$F_{\text{min}} = 1 + \left(\frac{f}{f_T}\right) \cdot \sqrt{2(R_B + R_E)I_C/V_T}$$  

(4.2).

The higher $f_T$ and lower gain of InP/GaAsSb DHBTs then in fact co-operate to widen the band of frequencies where $NF_{\text{min}}$ remains frequency independent with respect to SiGe HBTs, while the high $f_T$ subsequently limits the rise of $NF_{\text{min}}$ with frequency. We may conclude from the above that although InP/GaAsSb DHBTs are unlikely to challenge the best noise figures of ultrahigh-speed SiGe DHBTs at low frequencies (because of their limited current gain), they may become attractive for low-noise applications in the 50 – 80 GHz band. Future work should focus on the noise characterization of InP/GaAsSb DHBTs at V-band and above. In particular, the fast rise of $f_T$ with increasing $I_C$ seen in Fig. 4.6 calls for an investigation of the tradeoff between low-frequency $NF_{\text{min}}$ and the rate of rise of $NF_{\text{min}}$ with increasing frequency.

### 4.3 Base Contact Resistance Influence on the Noise Figure of Transistors with AlInAs Emitters

According to Eqn. (4.1), a reduction of $R_B$ and an increase of $\beta$ reduce the minimum noise figure. $R_B$ is the sum of the intrinsic base resistance, the extrinsic base resistance and the contact resistance. The intrinsic base resistance can be reduced by increasing the base doping level, which results in the degradation of the gain $\beta$. An improvement of the device fabrication process (e.g. reduction of the base contact resistance) becomes thus essential in order to achieve both a decreased base resistance and an increased gain, and thus a lower minimum noise figure.

In this section, we study the base surface treatment impact on the minimum noise figure of AlInAs/GaAsSb/InP DHBTs. The electron beam lithography fabrication process was applied to AlInAs/GaAsSb/InP DBHT wafer with the structure described in Sec. 4.1.
A combination of ICP dry etching and wet etching, was employed to etch the emitter cap, where the emitter metal was used as a mask. SiNx was then deposited by PECVD at a temperature of 120 °C. After deposition, a blank etching in RIE was performed at room temperature, creating the SiNx sidewall shown in Fig. 4.8. The sidewall profile is similar to that of the base/emitter SiNx sidewall discussed in Chapter 2. In this study, we utilize it as a mask during the AlInAs emitter wet etching step and to form the
AllInAs ledge shown in Fig. 4.9. The ledge should improve the device current gain [13] and reliability [106].

Three samples (sample A, B and C) with the emitter area of $0.4 \times 9.5 \, \mu m^2$ were prepared with different base surface treatments: the bases are treated with AZ developer, diluted (NH$_4$)$_2$S solution and diluted (NH$_4$)$_2$S solution followed by concentrated HCl for samples A, B and C, respectively.

Fig. 4.10 shows the Gummel plots of the three devices with an emitter area of $0.4 \times 9.5 \, \mu m^2$. The base and collector currents overlap very well, demonstrating an excellent process reproducibility. The base surface treatment condition does not have any apparent impact on the device Gummel characteristics.

![Gummel plots of devices with the emitter area of 0.4 × 9.5 µm² from samples A, B and C.](image)

The short-circuit current gain $|h_{21}|^2$ and the $U$ gain as a function of frequency are shown in Fig. 4.11 for samples A, B and C for an emitter area of $0.4 \times 9.5 \, \mu m^2$: the transistors are biased for peak $f_T$. A peak current-gain cutoff frequency of 280 GHz was achieved on sample C. This is the highest $f_T$ so far achieved for AllInAs/GaAsSb/InP DHBTs. The current-gain cutoff frequency $f_T$ is nearly the same
for all three samples, while the maximum oscillation frequency $f_{\text{MAX}}$ of sample A is to be found between those of sample B and C.

![Graph showing $|h_{21}|^2$ and $U$ as a function of frequency of devices with emitter area of 0.4 x 9.5 $\mu$m$^2$ from samples A, B and C.](image)

*Figure 4.11*  $|h_{21}|^2$ and $U$ as a function of frequency of the devices with the emitter area of 0.4 x 9.5 $\mu$m$^2$ from samples A, B and C.

The different $f_{\text{MAX}}$ for the three devices is a consequence of the different base surface treatment applied before the base contact evaporation. The base resistances extracted from the measured $S$ parameters are 39.0 $\Omega$, 47.5 $\Omega$ and 32.7 $\Omega$ for samples A, B and C, respectively. This implies that the base contact resistance of sample C is lower than the others, because the base sheet resistance and geometry sizes are the same for all devices. The additional HCl treatment removes the residual material at the emitter/base interface and improves the base contact resistivity, as discussed in Chapter 3. The AZ developer treatment applied to the base surface of sample A is not as effective as the concentrated HCl to remove the residual material, which cannot be removed by the AlInAs etchant.
The current-gain cutoff frequency $f_T$ and the maximum oscillation frequency $f_{\text{MAX}}$ versus the collector current of the devices are depicted in Fig. 4.12. The devices from the three samples exhibit nearly the same $f_T$ at collector currents lower than the Kirk current. Sample A shows a slightly earlier onset of the Kirk effect than sample B and C. According to the expression for the Kirk current equation in Ref. [67], the higher collector contact resistivity in sample A as determined from TLM measurements might produce a lower Kirk current.

Sample C exhibits the highest $f_{\text{MAX}}$ for all collector currents due to its lowest base contact resistivity, which results from the additional base surface treatment with concentrated HCl compared to sample B. As also noted, sample B exhibits the lowest $f_{\text{MAX}}$ due to the residual material on which the base contact was deposited.
Fig. 4.13 shows the minimum noise figure versus collector current for devices with an emitter area of $0.4 \times 9.5 \mu m^2$. The devices from sample C exhibit the lowest minimum noise figure over the entire collector current range due to their lowest base resistance. At 10 GHz, the devices from sample C feature a minimum noise figure of 2.4 dB and an associated gain of 21 dB. Simultaneously, the devices exhibit a current-gain cutoff frequency $f_t$ of 280 GHz. These performances are the best ever reported for AlInAs/GaAsSb/InP DHBTs. In conclusion, a base resistance decrease reduces the transistor minimum noise figure.
4.4 Comparison of Noise Performances of InP/GaAsSb DHBTs with AlInAs and GaInP Emitters

Fig. 4.14 shows the gain versus the collector current measured for InP/GaAsSb DHBTs with AlInAs and GaInP emitters and with an emitter area of $0.4 \times 4.5 \, \mu m^2$. A higher Kirk current is observed on devices with GaInP emitter. These devices show a higher gain over the entire collector current range than those with an AlInAs emitter. The higher gain is attributed to a lower surface recombination current, a lower space charge recombination current and a lower back injection current (see Chapter 3).
Figure 4.15 Minimum noise figure and current-gain cutoff frequency $f_T$ versus collector current for InP/GaAsSb DHBTs with AlInAs and GaInP emitters and with an emitter area of $0.4 \times 4.5 \, \mu m^2$.

Fig. 4.15 shows the evolution of $NF_{min}$ at 10 GHz and the current-gain cutoff frequency $f_T$ versus the collector current at $V_{CE} = 1 \, V$ for DHBTs with AlInAs and GaInP emitters. DHBTs with a GaInP emitter show a higher current-gain cutoff frequency $f_T$ and a lower minimum noise figure than devices with an AlInAs emitter. According to Eqn. 4.1, for $f < f_T/\beta^{1/2}$, the minimum noise figure of bipolar transistors is determined by a variety of factors including the collector current, current gain, as well as the emitter and base resistances. According to Fig. 4.14, at the collector current of 3.4 mA, the current gain of both devices is found to be similar (≈ 33). The lower minimum noise figure 2.72 dB of DHBTs with a GaInP emitter results from the lower emitter and base resistances extracted from the measured $S$ parameters. Fig. 4.15 shows that DHBTs with a GaInP emitter always show a lower $NF_{min}$ for a given collector current when compared to those with the AlInAs emitter. At higher collector currents, the shot noise contribution becomes dominant, explaining why the GaInP emitter DHBTs show a higher minimum noise figure at peak $f_T$ bias ($I_C = 6.34 \, mA$ for AlInAs emitter and $I_C = 12.4 \, mA$ for GaInP emitter).
Summary and Outlook

This thesis was aimed at the improvement of the DC and RF performance of InP/GaAsSb DHBTs through optimization of the epitaxial layer design and fabrication process. The highest $f_T$ achieved was 475 GHz for a transistor with a 50 nm thick collector and an emitter area of 0.4 × 8.4 $\mu$m$^2$. DHBTs fabricated using optical lithography, featuring an emitter area of 0.6 × 11.5 $\mu$m$^2$ and a collector thickness of 125 nm exhibited simultaneous $f_T$ and $f_{MAX}$ values of 388 and 350 GHz. Moreover, a minimum noise figure of 1.2 dB was measured for a transistor reaching $f_T/f_{MAX}$ of 400/322 GHz with an emitter size of 0.3 × 3.4 $\mu$m$^2$. 
5.1 Summary of This Work

In order to increase the DC current gain $\beta$, multiple approaches were investigated. The conduction band discontinuity $\Delta E_C$ at the staggered emitter–base junction was reduced by increasing the As concentration in the base. An increase of the As concentration from 51 to 64.5%, corresponding to a reduction in $\Delta E_C$ from approximately 100 to 50 meV, resulted in an increase of $\beta$ from 60 to 126 for devices with an emitter area of $80 \times 80 \mu m^2$ and $R_{\text{SH}} = 3350 \Omega/\square$. A further reduction of $\Delta E_C$ was achieved by introducing a (Ga,In)P composite emitter, yielding $\Delta E_C = 0$ for an As concentration of 60% in the base and a Ga concentration of 24% in the GaInP emitter layer. Compared to the pure InP emitter, a composite emitter with 24% Ga exhibited more than a fourfold increase in $\beta$. In both cases discussed above, the improvement of $\beta$ with reducing $\Delta E_C$ is attributed to a reduction of intrinsic recombination as well as emitter periphery surface recombination. An additional possibility to improve $\beta$ is the introduction of a composition gradient which creates a quasi-electric field across the base, and thus, reduces the base transit time. Grading the As concentration from 60% on the emitter side to 40% on the collector side of the base produces an energy difference in the conduction band of approximately 30 meV. For $R_{\text{SH}} = 1150 \Omega/\square$ this type of compositional grading yielded a $\beta$ of 57, whereas a $\beta$ of only 37 was obtained for a uniform base with a 60% As concentration and equal sheet resistance.

The current gain cut-off frequency $f_T$ is governed by the base and collector transit times, as well as the parasitic charging delays. By scaling down the collector thickness from 150 to 50 nm the approximated collector transit time was reduced from 263 to 145 fs, resulting in an increase of $f_T$ from 370 to 475 GHz. In order to reduce the parasitic charging delays, the capacitances can be minimized through downscaling of the device dimensions. The standard triple mesa process results in a base-collector junction that is naturally wider than the base-emitter junction, which leads to a significant extrinsic $C_{\text{CB}}$. A possible method of reducing this extrinsic capacitance is lateral etching of the base mesa. Lateral etching of up to 750 nm was demonstrated and lead to an increase in $f_T$ for devices fabricated with optical lithography. Reduction of the emitter width imposes stringent requirements on the contact resistivity, hence
several aspects affecting it were studied. The emitter contact resistivity showed a strong dependence on the In concentration in InGaAs emitter cap layer, dropping to $1.75 \times 10^{-8} \ \Omega \cdot \text{cm}^2$ for an In concentration of 83% from $3.07 \times 10^{-8} \ \Omega \cdot \text{cm}^2$ for 50% In. However, surface roughness due to excessive strain prevented the use of In concentrations above 80% for device fabrication. The doping level of the InGaAs cap layer also exhibited a substantial effect on the contact resistivity, which was reduced by a factor of five when the donor density was increased from $1 \times 10^{19}$ to $4 \times 10^{19} \ \text{cm}^{-3}$. A pre-metallization surface treatment consisting of oxygen plasma ashing followed by a dip in diluted HCl further improved the emitter contact resistivity and values as low as $0.52 \times 10^{-8} \ \Omega \cdot \text{cm}^2$ were achieved on an In-rich InGaAs cap layer. A slight reduction of the contact resistivity was observed after rapid thermal annealing; the optimal temperature was found to be 270°C, above which the contacts rapidly degraded.

Since the maximum oscillation frequency $f_{\text{MAX}}$ is proportional to $R_B^{-1/2}$, a minimized base resistance is pivotal. The total base resistance depends on a series of factors, including the base sheet resistance, the base contact resistance and the base access distance. The base sheet resistance can be minimized through an increase of the base doping level or the base thickness, both of which have a negative effect on $\beta$. Additionally, a thicker base also degrades $f_T$ due to the longer base transit time. For GaAsSb bases, an appropriate pre-metallization surface treatment proved to be of fundamental importance in achieving low resistivity base contacts due to the interface layer formed between the base and emitter during epitaxial growth, which was not removed by the standard emitter etching recipe. A treatment in concentrated HCl effectively removed this interface layer, leading to a substantial decrease of the base contact resistivity. The HCl treatment reduced the extracted base resistance from 35 $\Omega$ to 22 $\Omega$ and increased $f_{\text{MAX}}$ from 211 to 320 GHz for a device with an emitter area of $0.6 \times 11.5 \ \mu\text{m}^2$. Furthermore, a dry-etch process was introduced in order to obtain a smaller emitter mesa undercut, leading to a shorter access distance and reduced $R_B$. Although the reduced access distance only had a minor effect on $R_B$ for devices fabricated using optical lithography, it is expected to be beneficial for devices with smaller dimensions.
The suitability of InP/GaAsSb DHBTs as a potential candidate for low noise applications at high frequencies was investigated. For a device with an emitter area of $0.3 \times 3.4 \, \mu m^2$ and an $f_T$ of 400 GHz, a minimum noise figure of approximately 1.2 dB was measured at 20 GHz with an associated gain of 10 dB.

5.2 Outlook

With shrinking device dimensions new challenges arise continuously, which have to be addressed in order to fully benefit from the reduction in size. While emitter widths down to 0.1 \, \mu m are manufacturable using e-beam lithography, a degradation of $f_T$ was already observed at an emitter width of 0.2 \, \mu m, due to an increase in emitter resistance. This effect can be mitigated by an improvement of the contact resistivity or higher emitter doping for the static resistance, and an increase of current density for the dynamic resistance. Further reduction of the contact resistivity may be possible with in-situ deposited emitter contact metal, which would require pattern transfer by dry etching. An increased doping level would result in a lower Ohmic resistance of the emitter semiconductor layers as well as a reduced sidewall depletion width. The drawback of this approach is the increase of $C_{BE}$ and a possible reduction of $\beta$. The dynamic resistance can be reduced by suppression of the Kirk effect, which can be achieved by increasing the doping level of the whole collector or by introducing a spike in doping close to the base. Both methods may lead to undesirable effects, such as a reduction of the breakdown voltage and an increase of $C_{CB}$. The incorporation of a collector doping spike was examined, but additional optimization is required in order for this method to produce significant benefits.

While the base resistance has already been reduced significantly over the course of this work, further improvements are necessary to reach even higher $f_{MAX}$. Since the contact resistivity is a major component of the total base resistance, especially as the devices get smaller, continued research in this area is important. Possibilities to improve the contacts include increasing the base doping, refining the surface treatment, and optimizing the metal stack. Aside from allowing better contacts, a higher doping level will also reduce both the spreading and access resistances; however, a limit to increasing the doping level is given by the reduction of $\beta$. Novel
approaches to increase the gain must therefore be pursued to alleviate this restraint. Another way to reduce the access resistance is to minimize the emitter undercut, which can be achieved either by forming SiN$_x$ spacers prior to the emitter mesa etch or by reducing the thickness of the InP emitter layer.

A device yield of approximately 80% is achieved using the standard optical lithography fabrication process. While this may be sufficient for the realization of demonstrator circuits with low device counts, it limits the feasibility of circuits with higher complexity. In the case of the e-beam fabrication process the yield is lower, making this issue more severe. It is inherently difficult to establish a high-yield fabrication process in a multi-user university cleanroom with constantly varying conditions. Nevertheless, both the yield and uniformity can be improved by optimization in various areas. Three main yield-limiting factors were experienced: alignment inaccuracies associated with mix-and-match lithography, which can be reduced by improved alignment structures and a reduced e-beam write-field size; device damage arising from particle contamination, which can be minimized with the aid of particle monitoring in the work area; and problems related to the non-uniform etch-back utilized in the air-bridge process, which can be avoided by introducing a low-$K$ dielectric with superior planarization properties.
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2001-2003    Master studies in Physics/Electrical Engineering at National University of Singapore, Singapore
1998-2001    Master studies in Electrical Engineering at Jilin University, China
1994-1998    Bachelor studies in Electrical Engineering at Jilin University, China

Professional Experience

2003-2006   Research Assistant in Simon Fraser University
Publication Lists

Journal Papers

Conference Papers


