A Low Power CMOS GSM Transceiver for Small Mobile Stations

A dissertation submitted to the
SWISS FEDERAL INSTITUTE OF TECHNOLOGY ZURICH

for the degree of
Doctor of Technical Sciences

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2000
Acknowledgments

I would like to acknowledge the help and support of my advisor, Prof. Dr. Qiuting Huang and thank him for his patience and steady encouragement over the course of this project. For his incisive comments on my thesis, my gratitude must also go to my associate advisor and co-examiner, Prof. Dr. Werner Bächtold.

A special thank you to my colleague Francesco Piazza for introducing me to the world of RF-circuit design and for his priceless technical input throughout the duration of this project. Without his help, this work would not exist.

I would like to thank Martin Lanz and Hanspeter Mathys for their help in constructing the test prototypes, and also Ruedi Rheiner for his help in measuring system performance.

For his constructive proofreading, special thanks to Enrico Ferrari.

My gratitude also to our industrial partner Toshiba Corporation, Japan, for their financial support.

Finally and in particular, I would like to thank my parents Carmen and Janni, and my girlfriend Simona for their love and unconditional support at every step of the way.

Zurich, January 2000

P. Orsatti
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Abstract

This work describes the design, implementation and experimental characterization of a GSM transceiver IC in 0.25μm CMOS. In addition to obtaining GSM type approval, our main objectives centered on achieving robustness, low power consumption and minimizing the number of external components used in the chosen architecture. The resulting prototype is intended as the basis for a mass production implementation.

Points of reference for planning the system were the GSM type approval requirements, the characteristics of the available external parts (filters, power amplifier, baseband processor, ...) and the characteristics of the CMOS process. Thanks to the carefully chosen architecture and optimized transceiver planning, good trade-offs have been reached for the individual circuit blocks in terms of required performance and power consumption. The super-heterodyne receiver, with a single IF at 71MHz, has an overall worst case NF of 8.1dB with the effect of all filters included. The receiver consumes only 19.5mA while achieving the required blocking and intermodulation performance. The direct conversion transmitter provides a 2mW signal to the power amplifier with low levels of spurious emissions. The transmitted GMSK signal has an RMS average phase error < 2° and the overall current consumption of the transmitter is 57mA.

Although bipolar technologies still dominate the sphere of RF integrated circuits, this work demonstrates that a low power CMOS implementation is a feasible and competitive alternative to the commercial bipolar solutions that are currently available. A CMOS transceiver may be favored not only because of the lower costs of the technology, but also because it opens the way to successfully realize a complete system on a chip.
Riassunto

Questo lavoro descrive la progettazione, la realizzazione e la caratterizzazione di un chip ricetrasmittente per GSM implementato in tecnologia CMOS 0.25µm. Oltre a soddisfare i requisiti d'omologazione per GSM, gli obiettivi sono stati la robustezza del sistema, il basso consumo di potenza e la minimizzazione del numero di componenti esterni considerando l'architettura utilizzata. Questo prototipo può servire come base per lo sviluppo di una produzione di massa.

Punti di partenza per la progettazione del sistema sono stati le specifiche per l'omologazione GSM, le caratteristiche dei componenti esterni a disposizione (fistri, amplificatore di potenza, processore banda base, ...) e le caratteristiche della tecnologia CMOS a disposizione. Grazie all'accurata scelta dell'architettura e alla progettazione ottimizzata della ricetrasmittente, sono stati trovati dei buoni compromessi per i circuiti singoli sia in termini di prestazioni richieste che di consumo di potenza. Il ricevitore supereterodina, con una singola media frequenza a 71MHz, ha una figura di rumore, includendo tutti i filtri, che nel caso peggiore è di 8.1dB. Il ricevitore consuma 19.5mA rispettando le specifiche di blocking e di intermodulazione. Il trasmettitore direct conversion fornisce 2mW di segnale all'amplificatore di potenza aggiungendo un livello molto basso di spurie. Il segnale GMSK trasmesso ha un errore RMS medio di fase < 2°, mentre il consumo totale di corrente è di 57mA.

Nonostante le tecnologie bipolari continuino a dominare il mondo dei circuiti integrati RF, questo lavoro dimostra che una soluzione a bassa potenza CMOS non solo è fattibile, ma risulta anche essere competitiva con le soluzioni bipolari in commercio. Un chip ricetrasmittente CMOS può essere vantaggioso non solo per il risparmio dovuto all'uso di una tecnologia più economica, ma anche poiché apre la strada alla realizzazione del sistema completo su un solo chip.
Chapter 1

Introduction

1.1 Motivation

The rapidly evolving personal wireless communications market continues to show dramatic levels of growth. Just about 15 years ago, the story was somewhat different. Two-way mobile communication was a cutting-edge product available only to a small number of customers. Therefore, the first wireless phones using analogue technology were very expensive. Furthermore, bulky handsets with short operating times, limited coverage, limited capacity and limited service ranges prevented mainstream penetration of these products.

With this first generation of systems, the first step towards realizing wider market penetration was achieved thanks to the introduction of regional standards which increased coverage and capacity, the miniaturization of electronic components and reductions in power consumption which enabled the use of smaller batteries and resulted in increased operating times.

The next major phase centers on the introduction of second generation products using digital cellular technology. With these products, wider market penetration was achieved and wireless phones were transformed into mainstream consumer products. The computing power of digital signal processors (DSP) permits the use of more efficient modu-
lation schemes as well as the development of new products and services. As the product evolves, the shrinking of processing technologies will facilitate further reductions in size and power consumption and result in lower handset costs for the customer.

Nowadays, handsets are as small as cigarette packets, their size influenced more by ergonomics than by circuit sizes. Stand-by times of up to 7–10 days and talk time of up to 3–5 hours are claimed by some GSM handset manufacturers [1, 2]. The improvement in these products is reflected in the first watch-phone based on the Japanese PCS standard which recently appeared on the market [3].

With the introduction of third generation products, the launch of which is planned for the year 2002, the fusion between wireless communications and Internet will become an everyday reality and whether the portable device will come in the form of a small electronic agenda, handset or watch will depend more on the required human interface than on other factors.

Whilst the introduction of new standards, services and features has pushed the development of DSPs to higher complexity and integration levels, the analogue transceivers used in wireless systems have not evolved at the same pace. An analogue transceiver is still required in digital wireless systems to interface between the incoming analogue RF-signals and the base-band digital processor. The first transceivers in digital phones were almost completely built using discrete components similar to those found in older wireless analogue systems.

In 1994 a typical GSM phone was still made up of more than 400 components, 95% of which were required specifically by the RF-transceiver [4]. Some of the reasons why transceivers continued to comprise hundreds of external discrete components offering lower levels of integration are summarized in the following:

- The primary purpose of IC technologies is to permit the integration of digital functions. In the beginning these technologies were just inadequate to integrate analog functions, too.

- Conventional designs using well-proven architectures and discrete components can easily achieve the required performance at a moderate price.
1.1. Motivation

- The problem of transceiver size has been solved in the main by the introduction of SMD components.

The pressure to reduce manufacturing costs in a very competitive market, to increase the reliability of products which have sold in millions of units and the constant evolution in IC technologies pushed some companies in 1995 to introduce new GSM transceiver solutions based on bipolar technologies with a higher degree of integration [5, 6]. The choice of bipolar technology was due to the fact that bipolar transistors offer good performance at the RF-frequency, contrasting to the CMOS processes which used 1μm devices and offered poor high frequency characteristics. Even today, all commercially available GSM transceiver solutions use some sort of bipolar or BiCMOS technology.

With the introduction of sub-micron technologies, however, the gap between bipolar and CMOS has become smaller so that interest has been raised in the use of CMOS to integrate more than the base-band circuits. Again the driving force has been the search for cost reductions, made possible through the use of cheap technologies such as these. Another motivation, perhaps more of a dream than a driving force, is the possibility of integrating the whole system on a single piece of silicon, of creating the so called 'system on a chip'.

The first research in this direction was conducted at university level. At that time, the fundamental question was:

'Can we use CMOS to implement complete transceivers for wireless products?'

The first applications targeted for this research have been based on systems with less demanding requirements such as DECT and Wireless LAN (WLL) [7, 8]. These projects have demonstrated that although some minor problems must still be solved, CMOS can also be used to implement RF-circuits. Aware that CMOS can be used to design RF-circuits and of the continuous evolution of CMOS processes to deep sub-micron minimum feature size which further improves the performance of CMOS devices at high frequency, the essential question for us was:
'What kind of applications can be successfully implemented when also using CMOS for the RF front-end?'.

There is in fact a substantial difference between applications such as DECT and WLL on the one side and GSM on the other (where required performance is much higher and must be guaranteed (type approval) and low power is at a premium). It is in this context that at the end of 1995, collaboration between ETH and Toshiba Corporation began. The aim of the project was to develop a complete quarter micron CMOS GSM transceiver.

1.2 Design Methodology

The project goal was not to simply demonstrate that CMOS can be used in the construction of GSM transceivers but to build a prototype that forms the basis for a mass production implementation and is therefore competitive with commercially available (bipolar) products. This means, first of all, that the complete transceiver must satisfy all GSM type approval requirements.

The single circuit blocks are and must be seen as part of a whole system. In many publications in recent years, there is a tendency (especially at university level) to design 'new' circuits that only optimize specific parameters whilst disregarding other circuit parameters that are also fundamental for proper system operation. In doing so, it is forgotten the fact that the circuit is worthless if it cannot be used as part of a complete system.

In this project, we have at first sought to study the complete system in depth. The specifications for the transceiver have been formulated with prior knowledge of the characteristics of the external parts (power amplifier, filters and base-band processor). After careful planning to define and optimize the requirements for the various circuit blocks, we have tried to design the single circuits to be as robust and as reliable as possible, trying to optimize their performance particularly in terms of power consumption and focusing on the fact that the whole system must satisfy type approval specifications. We have also decided to use an evolutionary approach instead of trying to achieve the 'breakthrough'. This
means that we have avoided attempting the implementation of highly integrated architectures since there are already many challenges at circuit design level, caused by the worst characteristics of CMOS devices with respect to their bipolar counterparts. We have used well established architectures, trying instead to minimize the number of external components where possible. As a result of the experience gained during this research which demonstrates the achievable performance of CMOS structures, we believe that a successive project focusing on highly integrated architectures can be better executed.

Another important aspect of this project is the approach used in the design of the single circuit blocks, which can be divided into three basic steps:

- First of all, from personal experience and intuition, a circuit configuration is chosen that potentially fulfills the required specifications.

- The circuit is then analyzed by adequate means. Where possible, simple hand calculation is used. For more complex circuits such as the IF-amplifier, the principle is tested by hand calculation, while to test the complete circuit requires a simulator. For circuits which operate at the GHz frequency such as the LNA and the RF-mixer, their performance depends on effects which are technology as well as geometry dependent and cannot be easily quantified. Therefore, slightly different designs are implemented on the same run to gain some insight as to the actual influence of these effects.

- Finally, once a suitable circuit is chosen, it is designed and optimized to fit into the system. If required, further optimization is achieved in successive runs using the experience gained from the previous designs.

One last point to mention is the importance of the simulator. The simulator is used to confirm the expected results and not to design the circuits. It is important to understand that the simulator is a tool that uses imperfect models to calculate the circuit performance and this is even more true at RF-frequencies where many physical phenomena are not modeled at all. What is wrong for the simulated model may be good in reality and what is wrong in reality may be good for the
simulated model! Moreover, the circuit simulator does not provide any understanding of the insight of the circuits, so that a simulator-based optimization without a good understanding of how the circuits really work can hardly achieve good results.

1.3 Structure of the Thesis

This thesis describes the design, experience and results that have been gained during the development and testing of a low power 0.25\(\mu\)m CMOS GSM transceiver. The thesis is organized in seven chapters describing all the steps required to design the transceiver, from aspects of system design down to the implementation of the single circuits and back to the characterization of the complete system.

In Chapter 2 an overview of the GSM system including a brief history, the main features and services, and the network architecture are presented. In the second part of the chapter, the GSM radio subsystem is discussed. The basic GSM air-interface specifications relevant for the development of the GSM transceiver are summarized and the Gaussian minimum shift keying (GMSK) modulation format is presented.

In Chapter 3 the type approval requirements that have an influence in the development of the GSM transceiver are discussed. Where the requirements are specified for the complete system, a translation into requirements for the transceiver alone is derived.

The transceiver architecture is presented in Chapter 4. Single super-heterodyne and direct conversion have been chosen for the receive and the transmit section, respectively. The detailed transceiver planning to define the requirements of each circuit block is also presented.

In Chapter 5, after a general description of CMOS technologies for RF-design, the basic characteristics of the 0.25\(\mu\)m CMOS process used are discussed. The other issues which must be addressed early in the design phase such as independence on supply voltage, process parameter and temperature variations, as well as ESD protection are also discussed here.

The design of the receiver blocks is presented in Chapter 6. Care
has been taken in the description of the design and optimization of the LNA and the RF-mixer. The other critical block in the receiver, the IF-amplifier, is also discussed thoroughly. Each block has been characterized separately and the results are also presented here.

The modulator and the pre-amplifier, the two blocks that form the transmitter, are presented in Chapter 7 together with their performance as tested.

The characterization of the complete transceiver is reported in Chapter 8.

I would consider my task more than satisfactorily accomplished if, by the end of the book, the reader will not be tempted to paraphrase Oscar Wilde’s famous book review: “Good in parts, and original in parts; unfortunately, the good parts were not original, and the original parts were not good.”
Chapter 2

GSM System Overview

2.1 A Brief History of the GSM System

In Europe, during the early 80s, two distinct analogue cellular systems experienced rapid growth. They were the Total Access Communication System (TACS) and the Nordic Mobile Telephone (NMT). The TACS could be found in the United Kingdom, Italy and Spain and the NMT covered amongst others, the Scandinavian countries, Germany (C-Netz) and Switzerland (Natel C). However, whilst the different countries might have been using the same systems, their individual networks were entirely incompatible. This was an undesirable situation and the limitations of these analogue systems were becoming increasingly manifest. Mobile communication, from the user’s perspective, required better transmission quality, more comprehensive service packages and unrestricted international operation. Simultaneously, manufacturers and service providers were facing problems such as insufficient capacity to accommodate the ever-expanding customer base and an extremely limited market which prevented economies of scale.

The European countries realized that a global solution would be the best way to tackle these issues. In 1982, the Conference of European Postal services and Telecoms (CEPT) formed a group called Groupe Spéciale Mobile (GSM) to study and develop the so called *pan-European*
public land mobile system. The main system requirements were:

- Improved speech quality
- New services and network facilities
- International roaming support
- High spectral efficiency to increase capacity
- Low terminal, operational and service costs
- Ability to support low power hand-held terminals
- High level of security
- ISDN compatibility

That GSM be a digital cellular system was not a fundamental requirement. However, development work resulted in a digital system being adopted as it proved better suited than analogue systems in achieving the required characteristics.

In 1989, specification work was transferred to the newly established European Telecommunications Standards Institute (ETSI) and GSM Phase 1 specifications were published in 1990. The commercial launch of GSM service in Europe was in 1992 and by the end of 1993 there were more than 1.4 million subscribers. Since then, GSM, which now stands for Global System for Mobile communications, has seen exponential growth throughout the world. By the end of 1998, 321 GSM networks were operational in 118 countries with a total of more than 135 million subscribers. Moreover, this trend shows no sign of losing momentum. GSM is currently the dominant worldwide cellular system and will remain unchallenged at least until the introduction of the third generation wireless system. The commercial launch of the new system called Universal Mobile Telecommunications System (UMTS) is scheduled for 2002 although total market penetration can hardly be imagined before 2005.
2.2 Services Provided by GSM

The services provided by the GSM system are defined in the standard, and like the standard itself, are constantly evolving. To enable a speedy introduction of the system and to keep pace with new features, enhancements and services as required by customers, the standardization process has been divided into different phases. The basic services were defined in Phase 1 and include telephonic capability, short message services (SMS), synchronous and asynchronous data transfer up to 9'600bps, call forwarding and call barring. The enhancements provided by Phase 2 (halted in October 1995) were influenced in the main by the introduction of ISDN. Services such as calling/connected line identification, multi-party communication and access to call charge information were added. At present, development continues with Phase 2+ and in the last 4 years, significant effort has been focussed on increasing the maximum data rate transfer of 9600bps. Concepts are currently being introduced which will achieve data rates up to 100kbps such as high-speed circuit-switched data (HSCSD) which combines multiple time slots in the same channel and general packet radio service (GPRS) which also enables coding schemes incorporating different levels of error protection.

2.3 Architecture of the GSM Network

The GSM network is composed of several entities. In addition to the functions of each entity, the interfaces connecting them are defined in the standard. A block diagram of a typical GSM network is shown in Fig. 2.1. The mobile station (MS) is the terminal used by the subscriber to access the system. Mobile stations can be divided into different categories called classes distinguished by different transmit power levels. The most popular MS today is the hand-held portable (small MS) in power class 4 with a maximum permitted RF transmit power of 2W. The MS communicates with the base transceiver station (BTS) across the air interface. Each BTS defines a cell in the cellular system. The base station controller (BSC) monitors and controls up to several hundred base stations. It handles radio-channel setup, frequency hopping and handovers between BTS under its own control. The mobile service
switching center (MSC) provides the connection between the mobile system and the fixed networks such as the public switched telephone network (PSTN) and the Integrated Services Digital Network (ISDN). Together with the help of different customer database entities (HLR, VLR, EIR, AuC), it provides all the functionalities needed to handle a subscriber such as registration, location updating, authentication, external handovers and call routing to a roaming subscriber in the network.

2.4 The GSM Radio Subsystem

The first generation GSM system defines the bands 890—915MHz for the uplink (mobile station to base station) and 935—960MHz for the downlink (base station to mobile station). In the second generation system, which is called extended GSM (E-GSM), the two existing bands have been extended by 10MHz downwards (between 880—890MHz for the uplink channels and 925—935MHz for the downlink channels) adding another 40% capacity to the system. To provide simultaneous ac-
cess to multiple users, GSM employs a combination of Frequency- and Time-Division Multiple Access (FDMA/TDMA). The 25MHz bandwidth (35MHz for the E-GSM) is divided into 124 channels (174 for the E-GSM), 200kHz wide, called Absolute Radio Frequency Channel Numbers (ARFCNs). Two guard bands 100kHz wide are provided at the upper and lower end of the spectrum. Each ARFCN is divided in time using TDMA to permit the sharing of the same channel by multiple users. Information is sent in frame periods of 4.615ms duration. One TDMA frame is divided in 8 time slots called burst periods. Each burst period lasts 576.92μs and is composed of 156.25 bits. This gives a radio transmission data rate of 270.833kbps and transmission rate per user of 33.854kbps. In fact, 44.25 of the 156.25 bits in the burst period are used by the GSM system to permit communication and so the result is an effective user data rate of 24.7kbps. Correspondent transmit and receive ARFCNs are separated by 45MHz and correspondent transmit and receive burst periods are separated by 3 time slots. The GSM system employs Gaussian Minimum Shift Keying (GMSK) modulation with BT=0.3. The main factors leading to the GMSK modulation format are:

- Immunity against fading
- Power efficiency
- Spectral efficiency

Fading is typical in mobile communication radio channels. It is caused by the overlapping of two or more versions of a transmitted signal that arrive at the receiver through different paths and at different times. These waves combine at the antenna input and the resulting signal can vary widely in amplitude and phase. Being a constant-envelope modulation type, GMSK does not contain information in the signal amplitude and therefore, in respect to other modulation types, ensures higher immunity against fading.

Power efficiency is important to increase the talk time of battery powered hand-held terminals and constant-envelope modulations are eminently suitable since they enable the use of power efficient non-linear Class-C amplifiers in the transmitters.
Spectrum efficiency, on the other hand, is important to maximize the number of users in the limited bandwidth. To understand the transient as well as the spectral characteristics of a GMSK signal, we can refer to Fig. 2.2. GMSK modulation can be seen as a derivative of Minimum Shift Keying (MSK) which, in turn, is a kind of Binary Frequency Shift Keying (BFSK).

In Fig. 2.2a digital data stream is used to produce an incoherent BFSK signal. The modulated signal is generated by switching between two carriers with the same amplitude but different frequencies and with no phase relationship (low frequency for 0 and high frequency for 1 in the data stream). The resulting signal waveform and phase trajectory are discontinuous at the switching times. These discontinuities cause a widening in the spectrum, and as a result, the modulated BFSK signal requires a high transmission bandwidth.

The first step in improving spectral efficiency is to use MSK as shown in Fig. 2.2b. MSK is defined as a continuous-phase BFSK with a modulation index of 0.5. The name MSK comes from the fact that the modulation index of 0.5 corresponds to the minimum frequency spacing required by two FSK signals to be orthogonal. Two waveforms $v_{h}(t)$ and $v_{l}(t)$ are said to be orthogonal over a bit period if
Reverse Channel Frequency & 880–915MHz \\
Forward Channel Frequency & 925–960MHz \\
Channel Spacing & 200kHz \\
TX/RX Frequency Spacing & 45MHz \\
Number of Radio Channels & 174 \\
Modulation Data Rate & 270.833kbps \\
Frame Period & 4.615ms \\
User per Frame & 8 \\
Time Slot Period (Burst) & 576.92\mu s \\
Bits per Time Slot & 156.25 \\
TX/RX Time Slot Spacing & 3 time slots \\
Number of User Channels & 1392 \\
Modulation Type & GMSK (BT=0.3) \\

| Table 2.1: Basic GSM Air-Interface Specifications |

\[
\int_0^{T_{\text{bit}}} v_h(t)v_l(t)dt = 0 \quad (2.1)
\]

When orthogonal signals are used, orthogonal coherent detection can be applied and simple, high performance receivers can be built. In the GSM case, the data rate is 270.833kbps and to satisfy the orthogonality requirement with minimum occupied bandwidth, the two signal frequencies must be placed 135.4kHz apart, one 67.7kHz above and the other 67.7kHz below the channel center frequency \( f_l = f_c - 1/4T_{\text{bit}} \), \( f_h = f_c + 1/4T_{\text{bit}} \). To generate a MSK signal, the two carriers must be synchronized. When a switch in frequency is required, the new carrier is selected either as unchanged or is inverted in order to maintain continuous signal waveform and phase trajectory. In an MSK signal, the information is contained in the phase trajectory. During a bit period, the phase changes linearly by either \( +\pi/2 \) or \( -\pi/2 \). The digital data stream can be reconstructed from the relative phase changes of the transmitted waveform. Thanks to the elimination of discontinuities in time domain, the spectrum is shrunk, the sideband-lobes are reduced and 90% of the signal is contained in a bandwidth \( BW = 1.2/T_{\text{bit}} \).

To improve spectral efficiency further while limiting the introduction of intersymbol interference (ISI), a Gaussian pulse-shaping low pass filter is inserted as a premodulation filter to MSK modulation. The data
stream is shaped before modulation, the signal is smoothed and, as shown in Fig. 2.2c, the generated GMSK signal has smoother phase transitions compared to the MSK signal. The Gaussian filter characteristics are defined by the 3dB bandwidth-symbol time product (BT). When a Gaussian filter is used, a trade-off between signal bandwidth and irreducible error due to ISI is necessary. A decrease in the BT value corresponds to a decrease in the spectrum occupancy but it also corresponds to an increase in inter-symbol interference (ISI). The ISI, in turn, degrades the bit error rate (BER) and a higher signal to noise ratio (SNR) is required to achieve the defined performance. In the GSM system BT=0.3 and 30% increase in spectral efficiency is achieved with regard to a MSK signal with less than 1dB performance loss due to ISI. A summary of the GSM air-interface specification is shown in Table 2.1.

The GSM system uses many digital techniques to combat the effect of multipath-induced fading, additive received noise, channel-induced spectral distortion, etc. typical in mobile radio channels. During the channel coding process, redundancy is introduced in the transmitted data. Errors introduced by the radio channel can be detected and a certain degree of correction can be achieved during the decoding process. Frequency hopping and data interleaving is used to reduce the duration and depth of the fades. Furthermore, to compensate for ISI generated by multi-path propagation, adaptive equalization is used in the detector. Currently, the best detector is based on the optimal Maximum Likelihood Sequence Estimator (MLSE) technique, which is used to decide upon the most likely transmitted sequence. In practical implementations however, to minimize silicon area, memory requirements, computing needs and power consumption, sub-optimal detectors are usually preferred despite their slightly inferior performance.
Chapter 3

RF Transceiver
Requirements

To ensure compatibility and interoperability with any GSM network, to guarantee a minimum product quality and to make sure that radio emission interference criteria are met, base stations and mobile terminals must satisfy the type approval requirements dictated by the GSM standard [14]. As with most applications for which type approval exists, GSM type approval specifies the requirements for the complete system. For instance, the sensitivity of the receiver is specified by a maximum permitted BER for a given reference signal and the accuracy of the transmitted signal is specified as maximum permitted symbol phase error. Achieving these requirements depends not only on the quality of the analogue transceiver but also on the type and quality of the digital detector/modulator used. Therefore, during the first phase, the system specifications must be carefully examined, the relevant requirements must be selected and translated into meaningful analogue requirements for the RF transceiver with consideration for the specifications of the other components in the system. The relevant requirements for the receive and transmit section of the RF transceiver of a small mobile station (Class 4) are as follows:
3.1 Receiver Key Specifications

- **Sensitivity:** For an additive white Gaussian noise (AWGN) channel condition, a BER < $10^{-4}$ must be achieved for a $-102\text{dBm}$ reference input signal. As stated earlier, the achievable BER depends on the chosen GMSK detector type. To achieve $10^{-4}$ BER with an optimum MLSE detector, $9\text{dB}$ SNR is needed at the detector input ($A/D$ converter inputs). To achieve the same performance, a sub-optimal MSK detector needs $10\text{dB}$ [11]. Bearing in mind that the (antenna) source noise power density at 290K is $-174\text{dBm/Hz}$, the result is noise power of $P_n = -121\text{dBm}$ for a 200kHz channel. This noise power is $19\text{dB}$ below the reference input $P_i = -102\text{dBm}$. Since the noise introduced by a well-designed synthesizer (VCO) is negligible for our receiver architecture, the degradation in SNR is solely caused by the noise introduced by the blocks in the receiver chain. Therefore, to satisfy the specifications for a sub-optimal detector, the maximum noise figure (NF) for the complete receiver referred to the antenna input is:

$$NF = P_i - P_n - SNR = 9\text{dB} \quad (3.1)$$

- **Dynamic range:** To cope with the strong signals typical when a mobile station is very close to a base station and without resulting in degradation in the quality due to distortion within the receiver or the demodulator, the receiver is required to detect signals up to $-15\text{dBm}$ with a BER < $10^{-3}$. Considering that the reference sensitivity is specified for a $-102\text{dBm}$ input signal, the receiver must be able to detect signals over a range of $87\text{dB}$.

Since an unrealistically high resolution would be required in the A/D converters to handle such signal variations, automatic gain control (AGC) is used in the receiver. The gain in the receiver is regulated by an AGC algorithm implemented by the base-band processor so that a constant signal is provided at the A/D converter input. Actually the AGC algorithm is not fast enough to track the fast fades typical of a received signal. An example of the fading envelope as a function of time is shown in Fig.3.1a. The reference for the average received signal strength is set to 0dB. As shown in the figure, deep fades can be down as much as $30\text{dB}$ from the average signal. Considering that a) the minimum SNR
3.1. Receiver Key Specifications

Figure 3.1: Signal Level at A/D Converter Input

required by the detector is 10dB, b) to work properly the AGC algorithm must keep the signal in a 6—10dB range and c) a head room of 6—10dB is added on the top. 55—60dB SNDR is required in the A/D converters as shown in Fig.3.1b. A good example are the A/D converters in the Sceptre GSM baseband chipsets [16] which have 10bit resolution and an effective $SNDR_{min} = 55$dB.

To provide a constant signal to the A/D converters, the gain in the receiver must therefore be controlled in small steps over the whole 87dB range. Accounting for component tolerances, as well as temperature and process parameter variations, head room of 10—15dB is added, so that a total of 100dB gain control has been specified for the receiver.

- **Blocking characteristic and reference interference level:**

The cellular radio network environment is usually described as 'hostile' partly because of the high levels of interfering signals present. Interferers outside the GSM receive band (925—960MHz) such as UHF TV, which transmits with power levels easily as high as 50—100kW in the 500—800MHz band, must be rejected. To account for the near-far situation typical in cellular communication networks, minimum in-band blocking performance for adjacent channels is also specified in GSM type approval requirements. For a small MS, a $-99$dBm reference input signal must be demodulated with BER < $10^{-3}$, where there are different in-band and out-of-band blocking signals, the power level of which depend
Chapter 3. RF Transceiver Requirements

Figure 3.2: Power Level of Blocking Signals to Be Rejected

on their frequency offset from the desired channel frequency. See Fig. 3.2. As shown in Fig. 3.2, out-of-band blocking signals as high as 0dBm must not saturate the receiver, while in-band blocking components may be as high as -23dBm. For the active circuits in the receiver, the blocking specifications translate directly into compression point (CP) requirements.

- **Intermodulation performance**: Similar to blocking signals, interfering signals in adjacent channels also degrade signal quality through intermodulation. The principle of third order intermodulation is shown in Fig. 3.3. Due to non-linearities in the transfer functions of the circuits, harmonic components are generated during signal processing. In case of two intermodulating signals one placed at $\Delta f$ and the other one at $2\Delta f$ from the center frequency of the desired channel, third order distortion generates an intermodulation product that falls exactly in the desired channel. The result is a decrease in SNR. For a small mobile station, it is specified that a $-99$dBm reference signal must be correctly demodulated (BER < $10^{-3}$) in the presence of two $-49$dBm signals, 800kHz and 1.6MHz away respectively from the desired channel. Since with our implementation, the worst distortion is caused by the third order intermodulation product, a specification for the third order intercept point (IP3) for the various active blocks is sufficient.
The required overall IP3 at the receiver input can be derived using the graphical method shown in Fig. 3.4, where required SNR is 10dB, the signal output grows with a slope of 1 with the power of...
desired input and the intermodulation product \((-49\text{dBm} + 3\text{dBm} = -46\text{dBm})\) grows with a slope of 3 with the power of interfering signals. From the graph:

\[
x + 10 = 3(x - 53) \Rightarrow x = 84.5 \quad (3.2)
\]

\[
iIP3 = -99 + x = -14.5\text{dBm} \quad (3.3)
\]

### 3.2 Transmitter Key Specifications

- **Output power**: To compensate for the attenuation over different distances within a cell, the base station instructs the mobiles to use different power levels in such a way that the power arriving at the base station is approximately the same in each time slot. On the one hand, this means that the dynamic range requirements of the base station receiver are somewhat relaxed. On the other hand, the average power consumption of the mobile station is reduced since the transmitted signal is kept at the minimum power level needed for reliable transmission. A small mobile station must be able to control its output power over 28dB, between +5 to +33dBm in steps of 2dB.

- **Spectrum due to modulation and wide-band spurious emissions**: To avoid the disruption in communication between the base station and other mobile stations and to avoid interference in other radio systems, the spurious emissions from a GSM transmitter must be minimized. In-band requirements are specified by the GMSK modulation mask. Maximum out-of-band permitted emissions are especially limited for the GSM and E-GSM receive band. Since wide-band noise requirements are specified in absolute values and not relative to the transmitted signal, the worst case condition occurs when the transmitter must send in the channel nearest to the GSM receive band (915MHz) at the maximum output power of +33dBm. The spectrum mask defining the maximum permitted emissions in power density (dBc/Hz) for the worst case condition is shown in Fig. 3.5. Wideband noise 6MHz offset from the channel must be less than \(-129\text{dBc/Hz}\), while the maximum
3.2. Transmitter Key Specifications

- **Phased accuracy:** Since with a GMSK signal, the information is contained in the phase trajectory, phase errors generated in the transmitter must be minimized.

For every transmitted 148-bits pseudo-random sequence, the limits for an RMS average and peak symbol phase error are 5° and 20°, respectively. The phase error is measured by computing the difference between the phase of the transmitted waveform and the phase of the ideal one. The peak error indicates the maximum deviation from the ideal phase trajectory at the change of a bit. The RMS phase error is calculated as the RMS average value of all the 148 measured deviations. The symbol phase error arises from the inaccuracies of the baseband D/A converters, from the phase noise introduced by the synthesizer and from the inaccuracies of the modulator, the latter being the dominant disturbance. To keep some margin for the minor contributors, we attempt to maintain the RMS and the peak symbol phase error generated in the modulator below 3° and 10°, respectively. To understand how this system requirement is translated into an analogue specification for the modulator, we can refer to fig. 3.6. During the modulation process, effects such as offset, carrier feed-through, im-

![GSM Type-Approval Template](image)

**Figure 3.5:** *Maximum Allowed Spurious Emissions*

noise in the E-GSM and GSM receiver band is −150dBc/Hz and −162dBc/Hz, respectively.
perfect side-band suppression and non-linearities in the transfer function, add spurious signals to the transmitted signal as shown in Fig. 3.6a where a pure sine wave has been modulated. In a polar representation, these spurious components can also be explained as rotating vectors of different magnitudes and frequencies which adds to the ideal signal vector to form the actual transmitted signal, as shown in Fig. 3.6b. The rotating speed of the vectors is defined by their instantaneous frequency and the symbol phase error is the angle between the ideal signal and that transmitted at the sampling instant. The worst-case condition arises when all the random components are perpendicular to the desired signal.

![a) Sine-Wave Modulation Output Spectrum](image)

![b) Polar representation](image)

**Figure 3.6:** Effects of Modulator Non-Idealities on Symbol Phase Error
3.2. Transmitter Key Specifications

and in the same direction. In this case, since for small angles \( \arctan(x) \approx x \), the peak phase error \( (10^\circ = 0.176 \text{ radians}) \) is:

\[
\Phi_{\text{peak}} = \frac{\text{Carr.} + U2 + LSB + U3 + \ldots}{USB} = 0.176 \quad (3.4)
\]

The RMS symbol phase error can be approximated considering that signals at the same offset frequency from the desired signal rotate at the same speed in the polar plane. Therefore, for the worst-case condition, the RMS sum of such a pair of signals is the RMS value of the sum of the two peak values. On the other hand, signals at different offset frequencies rotate at different speeds and are uncorrelated. As a result, the RMS symbol phase error \( (3^\circ = 0.052 \text{ radians}) \) is calculated as follows:

\[
\Phi_{\text{RMS}} = \frac{1}{\sqrt{2}} \frac{\sqrt{(\text{Carr.} + U2)^2 + (LSB + U3)^2 + \ldots}}{USB} = 0.052 \quad (3.5)
\]

This means that to achieve the desired phase accuracy, the RMS sum of the random emissions must be suppressed by at least \(-22.7\text{dB} \ (0.052 \times \sqrt{2}) \) with respect to the desired signal.

Once the specifications have been established and satisfy type approval requirements for the RF transceiver, a suitable architecture for the receive as well as for the transmit section must be chosen and the specifications for the single blocks in the chains must be defined through transceiver planning.
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Chapter 4

Transceiver Architecture and System Planning

4.1 Transceiver Architecture

The first step in the implementation of the transceiver is to choose a suitable architecture for the receiver as well as for the transmitter. To be competitive with current commercial solutions, a new implementation must fulfill the following requirements:

- *Satisfy type approval requirements:* this is a mandatory requirement. If just one type approval specification is not achieved, the product cannot be sold.

- *Satisfy the customer:* the customer will choose a particular handset primarily considering the price/performance factor.

- *Satisfy the manufacturer:* assuming the same services and features are provided, a manufacturer will produce the telephone only if he can see an economical benefit.

The customer can indirectly judge the quality of the RF-transceiver through the cost, size and weight of the battery needed to achieve a
certain operating time. This is particularly true in stand-by mode where most of the power is used by the receiver. In talk mode, on the other hand, the power used by the transmitter will have a less significant influence since it is usually a fraction of the power needed by the power amplifier.

The manufacturer, on the other hand, will judge the quality of the RF-transceiver through the achievable savings in manufacturing a particular implementation. The manufacturing costs of a handset depend on many components such as the chipset, battery, mechanics, etc. To better understand the weight of each component relative to the overall cost, the breakdown for a typical (bipolar) hand-held phone terminal is shown in Fig. 4.1 [15]. The complete chipset, including the RF-transceiver and the digital baseband processor, takes up about 25% of the overall cost. Worth noticing is the fact that the battery alone takes up another 25%, while on the other hand, external passive components, filters and discrete components contribute approximately 5% each. The remainder is divided between manufacturing cost and the cost of the mechanical parts.

![Cost breakdown diagram](image)

**Figure 4.1:** Breakdown of the Costs for a Typical (Bipolar) Hand-Held Terminal
The choice of a particular architecture will have a major influence on the achievable performance, the number of external components as well as the required power consumption. Since there isn't an architecture that optimizes everything, the best compromise must be carefully studied. An architecture with a high integration level may be advantageous since fewer external components would be needed. This could increase reliability on the one hand and on the other, decrease the overall costs by some percent. An alternative architecture with a slightly higher number of external components may be even more advantageous if a very low power solution can be achieved. Low power would mean either that a cheaper battery could be used, the result being substantial cost savings, or that an increased operating time and therefore performance could be achieved.

In addition to these general considerations, the final choice in our case, has also been influenced by the fact that we use a CMOS process with all its advantages and drawbacks.

4.1.1 The Receiver

The usual architectures found in commercial GSM receivers chipsets are superheterodyne architectures (Philips SA3600, Hitachi HD155121F, Siemens PMB6250, Lucent W2020) and, in some cases, the more 'aggressive' direct conversion (Alcatel?, Nokia?).

A typical single superheterodyne GSM receiver is shown in Fig. 4.2. The integrated blocks are shown in light gray, while the external components are shown in dark gray. In a single super-het implementation, the input signal is filtered first by the duplexer and then amplified by a low noise amplifier (LNA). After the LNA the image filter further suppresses the image frequency. Afterwards, the signal is converted to a fixed intermediate frequency by a down-conversion mixer driven by a tunable local oscillator (VCO).

Once at IF the desired channel is selected by a SAW filter. Main amplification occurs at IF thanks to the variable gain IF-amplifier. The IF-signal is demodulated by a quadrature demodulator, which generates the I and Q base-band components required to detect the signal phase trajectory. After low pass filtering to further select the desired channel and anti-aliasing, the quadrature components are provided to the input
of the base-band A/D converters. Worth noticing is that this solution requires three external filters. On the other hand, just two blocks working at the RF-frequency (LNA and mixer) and which are intrinsically power hungry are required.

In a direct conversion receiver (see block diagram in Fig. 4.3) the signal, after the duplexer and the LNA, is directly converted to baseband by a RF quadrature demodulator. Channel filtering and main amplification are done at base-band. From a designer's point of view, this architecture is very attractive since it permits the highest integra-
4.1. Transceiver Architecture

At the end, together with our project partner, a single superheterodyne approach has been chosen due to the following reasons:

- With respect to direct conversion, the superheterodyne architecture is more suitable for a low power approach since it contains just two power hungry RF-blocks.

- Although two more external filters are required compared to direct conversion, the increase in cost will not have a substantial impact on the overall handset costs.

- Direct conversion receivers entail potential problems such as DC-offset, flicker noise, AM detection and re-radiation. These problems may assume particular importance due to the CMOS implementation.

- Superheterodyne is a very robust and well proven architecture. Therefore, since there are already many issues to be solved at circuit design level, a more conservative architecture was considered a better choice. In this way we avoid attempting to tackle too many problems simultaneously.

- Although a double super-het architecture would allow relaxed requirements for some of the receiver blocks (especially the IF-amplifier and the IF-filters), it has been discarded due to the added complexity. In fact, a double super-het requires one extra local oscillator, one extra external filter as well as a package with more pins.

4.1.2 The Transmitter

On the transmitter side, the situation is more varied. Many different architectures can be found in commercial products. Older chipsets are based on superheterodyne (Philips SA1620) or direct conversion with or without offset oscillator (Lucent W2020). The latest implementations, on the other hand, tend to use the offset-PLL principle (Hitachi HD155121F, Siemens PMB6250).
Chapter 4. Transceiver Architecture and System Planning

Figure 4.4: Single Superheterodyne Transmitter

Figure 4.5: Direct Conversion Transmitter

Figure 4.6: Offset-PLL Transmitter
A single super-het transmitter is shown in Fig. 4.4. Here a quadrature modulator converts the base-band signal to an intermediate frequency. A filter is used to suppress the IF harmonics as much as possible. After mixing to RF, the signal is filtered once more to suppress the image and is subsequently amplified by a pre-amplifier which is needed to drive the external power amplifier (PA).

In Fig. 4.5, a direct conversion transmitter is depicted. The base-band signal is directly converted to RF by the quadrature modulator. To avoid interference between the high output power from the transmitter and the voltage controlled oscillator (VCO pulling), the offset oscillator principle can be used. In this case, the required RF carrier is generated using two VCOs working at two different frequencies. The two frequencies are mixed to the required RF frequency and filtered by a simple LC-network to suppress the undesired image.

In the offset-PLL method shown in Fig. 4.6, after modulation to the IF, a phase locked loop (PLL) is used to generate the RF signal. This structure is becoming the dominant architecture adopted nowadays. This because with regard to other architectures, this kind of implementation entails many advantages such as lower wide-band noise, which allows the duplexer to be substituted with a simple switch, higher accuracy and lower power consumption. When defining our architecture however, this latter method was not yet widespread and therefore wasn’t considered. Instead, a direct conversion architecture with an offset oscillator was chosen. The most important considerations leading to this choice are summarized as follows.

- As shown in the previous chapter, one of the basic requirements for the transmitter is the generation of low levels of spurious signals. Compared to a superheterodyne solution, direct conversion generates fewer spurious components since no intermediate frequencies are required.
- Since the input signals power is relatively high, DC-offset and flicker noise are less of a problem and can be handled quite easily.
- Direct conversion is ideally suited for a fully integrated implementation and requires a small number of external components.
- The offset-LO principle is used to minimize the VCO pulling problem.
Although direct conversion with offset requires three mixers and a phase shifter working at the RF-frequency, the overall power consumption of the transmitter will still be dominated by the power amplifier if current consumption is optimized.

4.2 Transceiver Planning

Once the architecture has been chosen, careful planning is necessary to define the requirements of each individual block in the transceiver. In many cases, where all the parameters are known, the specifications can be derived by simple analysis. On the other hand, sometimes analysis is not possible or is too complicated. In this case, the requirements are derived using estimates based on previous work and relying on personal experience. In our work, considering that this is the first implementation of a complete CMOS GSM transceiver, the estimates are mainly based on experience gained in low frequency CMOS and RF bipolar solutions. Some overhead is added where there is uncertainty and therefore the final design will probably not be the best ever solution. Nevertheless, we think that good trade-offs have been found and that only minor changes would be required for the optimum solution.

4.2.1 The Receiver

The receiver architecture block diagram is shown in Fig. 4.7. The first critical point in receiver planning is the choice of the IF frequency which is usually a trade-off between image rejection and selectivity. A low IF imposes stringent requirements on the image-reject filter, while a high IF requires higher (IF) channel filter selectivity (i.e. expensive channel filter). In this implementation, the 71MHz IF was selected as a good compromise. The 71MHz IF favors image-rejection at the expense of channel selection and as a result, the requirements for the image-filter are relaxed. On the other hand, since a low cost IF-filter can not completely suppress the adjacent blocking components, tough requirements are placed on IF-receiver linearity, particularly for the IF-amplifier.

To achieve the frequency conversion, the LO signal frequency must be placed either at RF+IF or RF−IF. If no particularly big interferers
4.2. Transceiver Planning

Figure 4.7: Receiver Architecture Block Diagram

can be found at the image frequency, the higher frequency (RF+IF) is usually preferred since a higher center frequency reduces the required relative tuning range of the VCO and, as will be shown later, a slightly lower NF for the RF-mixer can be achieved.

After the choice of the IF and the LO frequency, the major requirements in terms of gain, noise contribution, linearity and power consumption must be defined for each block in the chain. Our optimization of the receiver plan is shown in Fig. 4.8. On the top graph, the requirements in terms of gain, compression point (CP) and third order intercept point (IP3) are shown. For the CP and IP3 requirements, a 3dB overhead have been added to the calculated specifications to allow some margin. In the middle, the required noise figure (NF) for each block, as well as their percentage contribution to the overall NF, are shown. To allow some margin, a worst case NF of 8dB has been planned. In the bottom graph, the requirements in terms of current consumption are also displayed. To achieve a low power solution, the aim is for an overall current consumption of 20mA.

Between the antenna and the LNA, a duplexer with an out-of-band attenuation of 25–30dB is used to suppress the out-of-band blocking signals that can be as strong as 0dBm. Thanks to the suppression of interference by the filter, the required linearity and therefore the LNA power consumption requirement are reduced. In fact, accounting for the 3.2dB insertion loss of the duplexer [19] and the 3dB overhead, −23dBm iCP is required at the input of the LNA. Since the inter-
modulating signals are not attenuated by the duplexer, the required LNA iIP3 can be calculated to be $-14\,\text{dBm}$. However, the duplexer passband attenuation translates directly into a serious NF degradation for the receiver. With its 3.2dB NF, the duplexer contributes as much as 35% to the overall noise. This leaves only a tight NF budget of 4.8dB at the LNA input for the rest of the receiver.

The main purpose of the LNA is to provide enough gain to the input signal in order to overcome the noise of the following stages. Clearly, amplification must be achieved adding as little noise as possible. Based on the achievable performance for bipolar and GaAs implementations and accounting for the slightly worse noise behavior of CMOS devices, 2dB NF and 15dB gain are specified. Although a higher gain would relax the NF requirements of the following circuit blocks, a high current would be required in the LNA to achieve the needed gain and linearity.
and to drive the $50\,\Omega$ RX image-reject filter in front of the mixer.

The RX-filter has a typical image attenuation of $35-40\,\text{dB}$ which is required to prevent strong interferers and noise at the image frequency from excessively degrading the SNR during the mixing process. The RX-filter, however, has an insertion loss of $3.8\,\text{dB}$ [19], which degrades the NF at the mixer input by the same amount. As a result, $12\,\text{dB}$ NF, a tough value even for bipolar implementations, is required for the mixer.

To save the external inter-stage filter and eliminate the adverse effects of its insertion loss on NF, image reject mixers can be used as an alternative. By operating two mixers in quadrature the image is usually attenuated by $30-35\,\text{dB}$, which is sufficient to prevent noise at the image frequency from excessively contributing to the total NF. On the other hand, to avoid the saturation of the mixers by interferers at the image frequency which are no longer suppressed by the image-filter, $30-35\,\text{dB}$ higher linearity is required in the mixers. Having two highly linear mixers and a phase shifter operating at $900\,\text{MHz}$ will result in roughly $4-5$ times higher power than that of one conventional mixer. As in the case of direct conversion, such high power consumption was considered unacceptable.

To prevent excessive NF contributions from the IF-strip and to keep the current consumption of the mixer to an acceptable level while still achieving the linearity requirements, an active gain of $10\,\text{dB}$ is specified for the mixer. Inter-modulation and in-band blocking signals are not affected by the image-filter so that the required iCP and iIP3 for the mixer are $-12\,\text{dBm}$ and $-3\,\text{dBm}$, respectively.

After the mixer, a $71\,\text{MHz}$ differential IF filter with $6.5\,\text{dB}$ insertion loss [19] and $330\,\Omega$ characteristic impedance selects the desired channel before main amplification. To achieve $8\,\text{dB}$ overall NF, this translates to a maximum NF of $5\,\text{dB}$ for the complete IF-strip. As shown in the figure, the mixer will be the major contributor to the overall NF, followed by the duplexer and the LNA.

The required $100\,\text{dB}$ variable gain is achieved with $20\,\text{dB}$ in the switchable LNA which can be bypassed by a $-5\,\text{dB}$ attenuator, and $80\,\text{dB}$ in the $71\,\text{MHz}$ IF-amplifier which is programmable between $-20$ to $+60\,\text{dB}$ in steps of $2\,\text{dB}$. By changing the gain, the desired channel is regulated to a constant level of $-35\,\text{dBm}$ at the IF-amplifier output.
The IF-amplifier is one of the most challenging blocks in the receiver. It must have high gain of up to 60dB at a relatively high frequency of 71MHz. It must be programmable in accurate 2dB steps as specified by the interface with the base-band chip. Moreover, since the low cost 71MHz IF filter does not completely suppress undesired channels, the IF-amp must also possess very high linearity. Even after IF-filtering, a —60dBm blocking signal can still be present at the input of the IF-amplifier, 1.6MHz away from the desired channel. Since the blocking signal will also be amplified by the 52dB gain needed to bring the desired (—99dBm) signal up to —35dBm, an oCP of at least —8dBm is required for the IF-AGC. On the other hand, adjacent channel signals specified in GSM for the Inter-modulation test are about 20dB higher than the same desired signal after the IF filter, at the amplifier input. This translates to —2dBm oIP3 for the 52dB IF-amplifier gain.

After IF amplification, the signal is down-converted to baseband and amplified by 16dB by the I,Q demodulator. Two 4th order low pass Bessel filters with 16dB gain are required in front of the A/D converters as anti-aliasing filter and for final channel selection. Again, high
4.2. Transceiver Planning

Linearity is required in the base-band blocks because although interfering signals are gradually suppressed, the desired channel is now growing to the $-3\text{dBm}$ output level required by the A/D converters for optimal detection.

To preserve the phase information of the desired signal at base-band, quadrature demodulation is necessary. To ensure that the degradation of SNR by the leakage of undesired side-band is negligible, the rejection of the latter must be above 30dB.

In the ideal case, the undesired side-band is completely suppressed by the quadrature demodulator. In an actual implementation, on the other hand, phase and amplitude mismatches between the quadrature channels will cause an imperfect rejection. In equation (4.1) the relationship between USRR, phase and amplitude mismatch is shown:

$$USRR = 20\log\left(\sqrt{\sin^2(\Delta\varphi/2) + \Delta A^2 \cos^2(\Delta\varphi/2)}\right)$$ (4.1)

where $\Delta A$ is the amplitude mismatch and $\Delta\varphi$ is the phase mismatch between the I,Q components. If the I,Q mixers are carefully designed with a symmetrical and matched layout, inaccuracies in the quadrature channels are mainly caused by the phase and amplitude mismatches of the sine and the cosine version of the LO signal that are generated in the phase shifter. To better visualize the achievable USRR versus $\Delta A$ and $\Delta\varphi$ as determined by (4.1), the graph shown in Fig. 4.9 has been

![Graph](image)

**Figure 4.10:** Passband Characteristic of a GSM Duplexer for Various Terminating Impedances
Another important characteristic of all the circuits connected to an external filter is that their input/output impedance must be matched to the characteristic impedance of the filter they are connected to. In fact, to work properly, the external filters must be doubly terminated to their characteristic impedance which, in this case, is $50\Omega$ for both the RX-filter and the duplexer and $330\Omega$ for the IF-filter. An improper termination would cause an alteration of the filter passband characteristic which may degrade the overall performance of the receiver. To better understand the consequences of mismatch, the frequency response at the RX-port of the duplexer foreseen for this implementation has been measured for various terminating impedances and is shown in Fig. 4.10. The thick black curve depicts the measured behavior with the right termination impedance of $50\Omega$, while the thin gray curves are measured with mismatched impedances having a return loss of $-6\,\text{dB}$ and phase angles of $45^\circ$, $135^\circ$, $225^\circ$ and $315^\circ$, respectively.

As shown in Fig. 4.10a and 4.10b, the wide-band as well as the in-band characteristics are distorted. The out-of-band response is degraded by as much as $8\,\text{dB}$, the in-band filter flatness is corrupted and ripples up to $3\,\text{dB}$ may be observed. The mismatch of $-6\,\text{dB}$ return loss has been chosen for this example since it is considered the minimum value required to maintain the filter characteristic in a tolerable range. A further increase in mismatch is hardly sustainable and must be avoided.

A summary of the basic requirements for the active blocks forming the receiver section is shown in Table 4.1. For the keener reader, a detailed derivation of the NF, blocking and inter-modulation requirements for each block in the receiver can be found in Appendix A.
4.2. Transceiver Planning

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>LNA</strong></td>
<td><strong>Gain (Switchable)</strong>: +15dB, -5dB, 2dB, -23dBm</td>
</tr>
<tr>
<td></td>
<td><strong>iCP</strong>: -14dBm</td>
</tr>
<tr>
<td></td>
<td><strong>Input/Output imp.</strong>: +15dB, -5dB, 2dB, 50Ω</td>
</tr>
<tr>
<td></td>
<td><strong>Current cons.</strong>: 10mA</td>
</tr>
<tr>
<td><strong>RF-Mixer</strong></td>
<td><strong>Gain</strong>: +10dB</td>
</tr>
<tr>
<td></td>
<td><strong>NF</strong>: 12dB</td>
</tr>
<tr>
<td></td>
<td><strong>iCP</strong>: -12dBm</td>
</tr>
<tr>
<td></td>
<td><strong>iIP3</strong>: -3dBm</td>
</tr>
<tr>
<td></td>
<td><strong>Input/Output imp.</strong>: 50Ω, 50/330Ω</td>
</tr>
<tr>
<td></td>
<td><strong>Current cons.</strong>: 5mA</td>
</tr>
<tr>
<td><strong>IF-amplifier</strong></td>
<td><strong>Gain</strong>: -20, +60dB</td>
</tr>
<tr>
<td></td>
<td><strong>Gain Step</strong>: 2dB ± 0.5dB</td>
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<tr>
<td></td>
<td><strong>NF (Max. gain)</strong>: 5dB</td>
</tr>
<tr>
<td></td>
<td><strong>iCP (52dB gain)</strong>: -60dBm</td>
</tr>
<tr>
<td></td>
<td><strong>iIP3 (52dB gain)</strong>: -54dBm</td>
</tr>
<tr>
<td></td>
<td><strong>Input imp.</strong>: 330Ω</td>
</tr>
<tr>
<td><strong>Down-conversion Mixer</strong></td>
<td><strong>Gain</strong>: +16dB</td>
</tr>
<tr>
<td></td>
<td><strong>iCP</strong>: -8dBm</td>
</tr>
<tr>
<td></td>
<td><strong>iIP3</strong>: -2dBm</td>
</tr>
<tr>
<td><strong>Phase shifter</strong></td>
<td><strong>Input level (LO)</strong>: -6dBm</td>
</tr>
<tr>
<td></td>
<td><strong>Output level (I,Q-LO)</strong>: 0dBm</td>
</tr>
<tr>
<td></td>
<td><strong>Phase error</strong>: &lt; 3°</td>
</tr>
<tr>
<td></td>
<td><strong>Amplitude error</strong>: &lt; 0.3°</td>
</tr>
<tr>
<td><strong>4th Order LPF</strong></td>
<td><strong>Gain</strong>: +16dB</td>
</tr>
<tr>
<td></td>
<td><strong>Cut-off freq.</strong>: 150kHz</td>
</tr>
<tr>
<td><strong>IF-baseband-strip</strong></td>
<td><strong>Current cons.</strong>: 5mA</td>
</tr>
</tbody>
</table>

Table 4.1: Receiver Specification Summary

4.2.2 The Transmitter

Fig. 4.11 depicts a block diagram of the transmitter. The generation of the local oscillator using the offset-LO principle is not shown since it is part of the external synthesizer.

At the input of the transmitter, a first order low pass filter is required to smooth the two waveforms generated by the D/A converters.
which provide differential I and Q base-band signals with 1.4V_{pp} amplitude and typical offsets of 5–7mV to the transmitter [16]. To provide a continuous phase signal without distorting the GMSK spectrum, the cut-off frequency is placed at 1.2MHz. To keep the quadrature characteristic (e.g. same amplitude and 90° phase difference) good matching between the two filters is required.

The quadrature components are subsequently modulated to the transmit frequency by the I,Q modulator driven by the offset LO. As shown in the previous section, to achieve the required symbol phase accuracy, the RMS sum of the amplitudes of the spurious components generated in the modulator must be 22.7dB below the desired signal. Accounting for 4–5dB margin, 27dB suppression must be achieved to guarantee an adequate performance. In the case of direct conversion, the principal spurious signals that contribute to the symbol phase error are:

- **Carrier feedthrough**: This signal is generated by the sum of two different components that are uncorrelated. The first component arises from the DC-offset at the input that is converted to the carrier frequency by the up-conversion mixers. The second component is due to the imperfect isolation between the LO and the RF port of the mixers which causes part of the LO to feedthrough and to appear at the output.

- **Inter-modulation products**: These terms derive from the non-linearities in the transfer characteristic of the up-conversion mixers which cause a deviation from the ideal behavior and the generation of harmonic components at the output of the modulator. The relative importance of an inter-modulation product usually decreases
with the increase of the harmonic number. If even harmonics are minimized by the use of differential structures, only the low-term odd harmonics will play a role with the third harmonic being the major contributor to the overall inter-modulation.

- Undesired sideband: As shown in the receiver planning section, this spurious component mainly results from the phase and amplitude mismatch generated in the phase shifter used in the modulator. For instance, as shown in Fig. 4.9, to achieve 30dB USRR, $\Delta A < 0.3$dB and $\Delta \varphi < 3^\circ$ accuracy is sufficient in the phase shifter, while to achieve 40dB, $\Delta A < 0.1$dB and $\Delta \varphi < 1^\circ$ are required.

The specification for the relative weight of each of these three components can be decided to optimize the design of the modulator ensuring a simple and low power implementation.

Although without some sort of cancellation scheme, carrier feed-through is quite high and difficult to control, it can be kept to an acceptable level with accurate design. If non minimum feature size transistors are used at the input in combination with a carefully symmetrical layout, 2—3mV offset for a CMOS device can be achieved. In worst-case conditions, this value adds up to the offset of the D/A converter and a total offset of 7—10mV results in each of the quadrature paths. For a 700mVp input signal, this corresponds to a DC component suppressed by about 36dB. At the output, the I,Q components add up to a total of 33dBc suppression results. Assuming the use of double balanced active mixers, local oscillator feedthrough mainly depends on the mismatch between the Miller capacitances of the switching devices. If proper layout techniques are employed, isolation between the LO input and the RF output of 35—40dBc can be achieved. All together, in worst-case conditions, the result is a signal suppressed by 30dBc. This value has been specified as a maximum for carrier feedthrough.

In a direct conversion implementation, the quadrature mixers convert base-band input signals to the RF frequency. Since linearity is dominated by the input stage of the mixers which work at base-band, feedback structures that increase the input linearity can be implemented and the generation of inter-modulation products can be minimized. Therefore, to relax the accuracy requirements of the phase shifter, 45dBc minimum suppression for the higher harmonics has been specified.
To achieve the maximum allowed RMS sum of spurious emissions of 27dBC, this leaves a margin of 30dBC for the undesired side-band. As shown in Fig. 4.9 this translates to $\Delta A < 0.3$dB and $\Delta \phi < 3^\circ$ accuracy required in the phase shifter.

A well designed direct conversion modulator can achieve $-140$dBc/Hz wide-band noise floor [17]. To realize $-162$dBc/Hz in the GSM receive band as required by the specifications, 22dB attenuation is needed. Accounting for 6–8dB margin a total attenuation of 30dB is required. This is achieved using two external filters [19], the TX-filter and the duplexer, having 15dB out-of-band attenuation each.

In commercial bipolar solutions, the TX-filter is usually placed between the pre-amplifier and the PA. In this way, the out-of-band products generated during the mixing process and the spurious components introduced by the pre-amplifier are suppressed before main amplification. In this way, a clean signal reaches the PA input, and the effective power efficiency of the PA is not degraded. On the other hand, the TX-filter has a worst-case attenuation of 3.8dB and to provide the 2mW (+3dBm) signal required at the input of the PA, the pre-amplifier must deliver 4.8mW (+6.8dBm) to the TX-filter. In case of CMOS, generating a 5mW output signal requires excessive power consumption. Therefore, in this implementation, the filter is placed in front of the pre-amp. No attenuation occurs between pre-amp and PA and the pre-amp is required to deliver just +3dBm. The main drawback is that the pre-amp must be highly linear to minimize distortion which would degrade PA efficiency. Nevertheless, since GMSK is constant-envelope, the pre-amp can be operated near compression. As a result, +5dBm output compression point (oCP) has been specified for the pre-amp. For a sensible current consumption partitioning, the modulator has been specified to deliver $-17$dBm to the TX-filter. Accounting for the 3.8dB attenuation in the TX-filter, 24dB gain are therefore required in the pre-amplifier. Main amplification is achieved using a power amplifier implemented as an external module. A Class-C PA with a typical power efficiency of 40–45% is used [18]. Class-C amplifiers can be used thanks to the constant-envelope nature of GMSK. Power control is performed in the PA which is programmable over 30dB in steps of 2dB. The PA has a maximum output power of 2.5W and must be driven by a 2mW input signal.

To suppress the spurious signals introduced by the PA, the duplexer
4.2. Transceiver Planning

<table>
<thead>
<tr>
<th>Block</th>
<th>Input, Output level</th>
<th>1V&lt;sub&gt;pp&lt;/sub&gt;</th>
<th>1.2MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPF (1st Order)</td>
<td>Cut-off freq.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Up-conversion Mixer</td>
<td>Input level</td>
<td>1V&lt;sub&gt;pp&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output level</td>
<td>-17dBm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Carrier suppression</td>
<td>&gt;30dBc</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Harmonic suppression</td>
<td>&gt;50dBc</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output impedance</td>
<td>50Ω</td>
<td></td>
</tr>
<tr>
<td>Phase shifter</td>
<td>Input level (LO)</td>
<td>0dBm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output level (I,Q-LO)</td>
<td>0dBm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Phase error</td>
<td>&lt;3°</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Amplitude error</td>
<td>&lt;0.3dB</td>
<td></td>
</tr>
<tr>
<td>Pre-amplifier</td>
<td>Input level</td>
<td>-20dBm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output level</td>
<td>+3dBm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>oCP</td>
<td>+5dBm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input/Output imp.</td>
<td>50Ω</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.2: Transmitter Specification Summary

is placed just in front of the antenna. In-band insertion loss is limited to 1.2dB and at maximum gain, a 2W output signal reaches the antenna. As for the receiver, the external TX-filter must be impedance matched to 50Ω. Furthermore, for maximum power transfer, also the PA input must be terminated to 50Ω.

A summary of the basic requirements for each block in the transmitter chain is shown in Table 4.2. Not being a critical parameter, power consumption is not specified for the different blocks. To set a goal in line with commercial bipolar solution a maximum of 60mA has been specified for the complete transmitter (without PA).
Chapter 5

0.25μm CMOS Process
And IC Requirements

In the first part of this chapter we look at the basic characteristics of deep sub-micron CMOS technologies, focusing on the advantages and disadvantages of the quarter micron process we use for RF design. Afterwards, we study two basic requirements which must be considered when developing integrated circuits. Firstly, circuit performance must not be overly dependant on variations on power supply, temperature and process parameters. Secondly, ESD protection is also discussed.

5.1 CMOS Technology for RF Design

For RF design, the achievable performance depends on both transistor transconductance and parasitic capacitance. The transconductance determines the current required for a given gain and noise figure at the desired RF frequency. The parasitic capacitance, on the other hand, limits the speed, has a strong influence on the achievable quality factor of resonant structures in matching networks and often forms undesirable coupling paths which reduce the isolation between different circuit nodes. Whilst the use of a deep sub-micron technology is advantageous in that performance similar to bipolar circuits in the 1 – 2GHz range is
achieved, it also important to understand the real advantages of such a technology and the new challenges to be confronted during development.

In Table 5.1 the key parameters of 5 generations of different CMOS technologies from a 0.8\( \mu \)m to the 0.25\( \mu \)m process (used in this project) are shown. It can be seen that although the oxide thickness scales with the feature size, the \( K_n' \) for a transistor biased at 200mV overdrive does not increase as fast as the feature size reduction. This is due to mobility degradation.

The gate capacitance \( C_{\text{gate}} \) for a normalized 1\( \mu \)m width transistor stays more or less constant over subsequent generations since in a first approximation, it is proportional to \( L_{\text{min}}/t_{\text{ox}} \). The normalized overlap and junction capacitances also stay constant over subsequent generations. The overlap capacitance stays constant since the increase in unit capacitance due to the decreased oxide thickness is compensated by accuracy improvements in the fabrication process which decrease the overlap length. The junction capacitance stays also constant since the increase in unit capacitance due to the higher doping concentration in the source and drain region is compensated by the smaller area required for these regions. As a result, for equal transistor width and equal current, halving the gate length translates to an increase of about 70—80\% in the transconductance value. In our case, however, the technology is derived from a 0.6\( \mu \)m CMOS process in which the transistor gate size and the doping concentrations have been scaled to allow the implementation of quarter micron transistors. The design rules for the drain and source area remain unchanged so that the influence of the correspondent junction capacitances increases by a factor of 3, thereby slightly reducing the advantages of scaling.

<table>
<thead>
<tr>
<th>CMOS Process [( \mu )m]</th>
<th>0.8</th>
<th>0.6</th>
<th>0.5</th>
<th>0.4</th>
<th>0.25</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{ox}} ) [nm]</td>
<td>20</td>
<td>15</td>
<td>12</td>
<td>10</td>
<td>6</td>
</tr>
<tr>
<td>( K_n' ) (( \Delta V_{gs} \approx 200mV )) [( \mu A/V^2 )]</td>
<td>100</td>
<td>115</td>
<td>125</td>
<td>145</td>
<td>190</td>
</tr>
<tr>
<td>( C_{\text{gate}} ) [fF/( \mu )m]</td>
<td>1</td>
<td>1</td>
<td>0.9</td>
<td>1</td>
<td>1.2</td>
</tr>
<tr>
<td>( C_{\text{overlap}} ) [fF/( \mu )m]</td>
<td>0.2</td>
<td>0.2</td>
<td>0.15</td>
<td>0.2</td>
<td>0.3</td>
</tr>
<tr>
<td>( C_{\text{junction}} ) [fF/( \mu )m]</td>
<td>0.7</td>
<td>0.68</td>
<td>0.68</td>
<td>0.65</td>
<td>1.92</td>
</tr>
<tr>
<td>( V_{dd} ) [V]</td>
<td>5</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
<td>2.5</td>
</tr>
</tbody>
</table>

Table 5.1: Trends in CMOS Scaling
One of the disadvantages of scaled technologies for analogue design is the required reduction in voltage supply in order that breakdowns may be avoided. Quarter micron processes usually use a 2.5V voltage supply. The low supply voltage limits the number of stacked devices that can be implemented. This may influence the maximum achievable accuracy since cascode structures can not be used everywhere. Moreover, the maximum overdrive on single transistors, which defines the small signal linearity, is also limited so that to achieve the required linearity, alternative structures must be used. Finally, there is also a limit in the maximum achievable swing on internal nodes.

Another challenge arises from the common substrate, which in our case has a resistivity of \(5\Omega \text{ cm}\). On the one hand, such a substrate is subject to high levels of noise. On the other hand, it may also create unwanted feedback paths in the circuits. Here the problem is exacerbated by the big junction capacitances that offer a bigger area to inject/collect noise from the substrate.

Some important characteristics of the Toshiba quarter micron pro-
cess (ADVANCE-C0) are summarized in Table 5.2. The ADVANCE-C0 is a p-substrate, 2-metal, developmental technology. In this technology, minimum length nMOS devices have an \( f_T \) around 40GHz with a \( K_n' \approx 190\mu A/V^2 \). The pMOS devices, on the other hand, have a smaller \( K_p' \) of about 35\( \mu A/V^2 \) so that they will be mainly used for biasing purposes, especially for the high frequency circuits. A salicided layer which reduces the sheet resistance to 5\( \Omega/\square \) and therefore improves noise behavior is deposited on the gate as well as the source and drain of the transistors. To realize the passive components, high and low resistance poly as well as dedicated metal-insulator-metal (MIM) capacitors offer better alternatives in terms of matching accuracy and silicon area required.

## 5.2 Independence on Parameter Variations

Insensitivity to tolerances on manufacturing and temperature variations is a very basic requirement if predictable circuit performance typical of mass production is expected. In our implementation, the nominal power supply is 2.5V and circuit performance must be guaranteed for power supply variations of ±10%. The required performance must also be met for temperatures ranging between −40 to +85°C. Typical variations in parameter values for a CMOS technology are shown in Table 5.3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>R Low Res. Poly</td>
<td>15 – 20%</td>
</tr>
<tr>
<td>R High Res. Poly</td>
<td>20 – 25%</td>
</tr>
<tr>
<td>C (MIM)</td>
<td>10 – 15%</td>
</tr>
<tr>
<td>( K_n' ) and ( K_p' )</td>
<td>20 – 30%</td>
</tr>
</tbody>
</table>

**Table 5.3: Parameter Tolerances**

By contrast to bipolar transistor, MOSFET parameters vary in a rather unpredictable way and 'perfect' compensation for all variations is difficult. Nevertheless, sufficient independence can be achieved with proper circuit design and biasing methods. Thus, guidelines are employed such as the placement of critical poles defining the circuit bandwidth at least 2–3 times higher than nominal value to account for component tolerances. Where matching networks are needed, their Q is limited to a maximal value of 2–3 so that a variation in absolute values
5.2. Independence on Parameter Variations

will not result in significant variations in circuit performance. Particular design techniques to minimize dependence on absolute parameter variations have been used in the implementation of some critical blocks such as the IF-amplifier and will be explained later. The use of structures subject to high tolerances which can only be compensated by complex biasing schemes is avoided.

Although a complete biasing scheme has not been implemented in the designed prototype, a simple general solution which can be used for most developed circuits to stabilize the gain has been studied and is the next topic to be presented. Assuming a gain is proportional to the transconductance of a transistor multiplied by a resistive load (which is almost everywhere the case), the dependence of gain over the different varying parameters can be expressed as follows:

\[ A_v \approx g_m \cdot R = f(k', I_{dd}, R, Temp., V_{dd}) \]  \hspace{1cm} (5.1)

The dependence of the parameter \( k' \) on temperature for a typical CMOS device is shown in Fig. 5.1a [20]. At low temperatures, \( k' \) is proportional to \( T^{1.5} \), while at high temperatures it is proportional to \( T^{-1.5} \). In the required temperature range (shadowed) \( k' \approx T^{-1} \ldots T^{-1.5} \). If a PTAT current source is used to generate the biasing current that defines the transistor transconductance, this temperature dependence can be partially compensated and independence from power supply variations can be achieved. To implement the PTAT current source, the

\[ \text{Figure 5.1: Biasing Principle} \]
ΔV_{be} principle shown in Fig. 5.1b can be used. To realize a bipolar transistor in our CMOS process, parasitic lateral PNP devices can be employed. If the same resistance type used in ΔV_{be} is used to define the gain in the circuits, the resulting gain will be:

\[ A_v \approx g_m \times R \approx \sqrt{I_b \times k} \times R \approx \sqrt{\frac{T}{R}} \times T^{-1.5} \times R = \frac{\sqrt{R}}{T^{1/4}} \] (5.2)

Accounting for ±25% variation in the resistance value as well as in temperature, this translates to a maximal gain variation of ±1.5dB over temperature, process parameters as well as power supply variations.

If even higher accuracy is desired, some sort of active regulated biasing method could be implemented. Since such methods are usually complex and since the accuracy achieved is usually not required, they are seldomly implemented in consumer products.

### 5.3 ESD Protection

A second unavoidable requirement to guarantee the necessary reliability is the implementation of ESD protection structures in all pads. These structures have a substantial effect at GHz frequencies since they add parasitic resistances as well as parasitic capacitances. Simply adding them to a circuit designed separately may lead to poor performance. Their influence must be considered when designing the circuits and, if advantageous, these parasitic elements may be even employed as useful parts in the design and not considered simply as nuisance components.

Since ESD structures are strongly technology dependent, the realization of effective ESD protection is a major undertaking requiring a separate treatment by itself. Different components such as diodes and clamps may be employed. Moreover, in addition to the size, the device geometry is of extremely high importance and must be carefully studied.

For the CMOS technology we used, since neither effective solutions nor general guidelines to develop ESD protection were available, simple ESD structures based on experience gained in other technologies have
been implemented. On all signal pads with signals below 200MHz, a sufficiently robust protection consisting of diodes to the supplies, as shown in Fig. 5.2a, has been used. The diode size is also shown in the figure. Each diode contributes about $250\,\text{fF}$ parasitic capacitance. Together with the $200\,\text{fF}$ parasitic capacitance of the pad, this translates to a total capacitance of about $700\,\text{fF}$.

To limit parasitic capacitance, pads for signals in the GHz range use a single small clamp nMOS transistor to ground as shown in Fig. 5.2b. This structure is less effective but should, in any case, guarantee sufficient protection. Clamp size is shown in the diagram and the corresponding parasitic capacitance is about $50\,\text{fF}$ so that total capacitance of $250\,\text{fF}$ results for these pads. A bigger clamp device is also used for supply pads.

The main purpose of these simple structures is twofold. On the one hand, they must provide sufficient protection to test the prototypes. On the other hand, whilst not being optimized for the best ESD protection, these components add a parasitic load, similar to that which will be added by the final solution to be used in mass production. The influence of the parasitics can therefore be incorporated during the design and measured during testing.
Chapter 6

Design of the Receiver Blocks

6.1 The Low Noise Amplifier

The basic requirements for the low noise amplifier are summarized in Table 4.1. The start point for choosing a suitable input configuration is the simultaneous requirement for a low noise figure and impedance matching. Since at both the input and output, the LNA must cope with single-ended RF-filters, to avoid the use of external single-to-differential converters (baluns), a single-ended design approach is used.

6.1.1 The Input Stage

In Fig. 6.1, four possible implementations for the input stage are presented. For each structure, the simplified equation for gain, noise figure and input impedance is also described. The parameter $\gamma$ used in the NF calculation depends on the channel device length. For long channel devices $\gamma=2/3$. The figure tends to increase slightly for short devices.

The straightforward approach to implement the LNA is to use the common-source amplifier with shunt input resistor as shown in Fig. 6.1a.
Resistor \( R_1 \) is used to achieve broadband impedance matching and the conversion gain is defined by the transconductance \( g_m \) of the device. Unfortunately, the thermal noise added by the shunt resistor limits the noise figure to 3dB, even assuming a noiseless input transistor. In real implementations, noise figures in the order of 5–6dB are common which makes this solution unsuitable for our implementation.

The transimpedance amplifier shown in Fig. 6.1b can be used instead. Once the load impedance is known, resistor \( R_1 \) and transconductance \( g_m \) can be sized to achieve broadband input impedance matching. If the transconductance \( g_m \) is high enough \( (g_m R_1 \gg 1, g_m R_s \gg 1) \), high gain and a good noise figure can be achieved. In practice, the level of \( g_m \) is limited by current consumption considerations and the NF is limited to 3–4dB which is still too high. Nevertheless, due to the broadband and linearity characteristics of this circuit, this kind of LNA input stage can be found in many applications, such as the HP 8970A noise figure meter.

Another method to achieve impedance matching is to use the common-gate structure shown in Fig. 6.1c. The input impedance is defined by the transconductance. To achieve 50Ω, the transistor must be designed to have a \( g_m \) of 20mS. In this case, the minimum achievable NF for
6.1. The Low Noise Amplifier

The ideal amplifier, assuming $\gamma = 2/3$, is 2.2dB. Actually, the NF with such a configuration tends to be around 3dB due to a slightly higher $\gamma$ value for minimum length devices, the contribution of pads, ESD protections, substrate and the load impedance (output stage). Although such an approach is still not suitable for the design of the LNA, due to its broadband characteristic, this solution has been extensively used during this development in the design of blocks that require broadband impedance matching as well as low but not critical noise figures.

A way to generate a real input impedance using a common-source configuration using only reactive components is shown in Fig. 6.1d [21, 22, 23]. The matching network formed by $L_1$, $L_2$ and the gate capacitance $C_{gs}$ has a voltage gain between the input and the gate-source of the transistor equal to the quality factor $Q$ of the matching network at resonance.

$$Q = \frac{1}{\omega L_2 g_m} = \frac{1}{\omega C_{gs} R_s} \quad (6.1)$$

If $Q$ is greater than one, this gain may help reduce thermal noise contributed to the overall LNA noise figure by the input transistor and the LNA load impedance (output stage). Indeed, in the ideal scenario, as shown in the NF calculation of Fig. 6.1d, the noise contribution of the input device can be reduced to insignificant levels with moderate $Q$ and $g_m$ values. In practice, NF of 1.5dB to 3dB is common even in GaAs and BJT implementations which suggests that at this noise level, the LNA NF is dominated by other noise sources which influence is less well defined. This latter category of noise sources includes the contribution of substrate resistance through capacitances under bonding pads and ESD protection structures, gate-induced current noise and the back-gating effect of the substrate resistance under the MOS transistor. As shown in the transconductance equation in Fig. 6.1d, under matching conditions and ignoring the parasitic capacitances associated with the input pads, a $Q>1$ which achieves some voltage gain in the input matching network is also advantageous since it reduces the required $g_m$, and therefore the associated current level for a given overall conversion gain of the input stage.

On the other hand, while a high $Q$ matching network allows LNA current consumption to be low, the level of the reactance associated
with the network inductors and capacitor becomes high. Although the nominal capacitive and inductive reactance should cancel each other if designed for 50Ω matching, the same 10% deviation from the nominal values results in higher residual (uncancelled) reactance for higher Q. The variability of the input reflection coefficient $S_{11}$ is therefore also worse. As explained in chapter 4, an excessively high deviation from the required 50Ω value causes a worsening in the RF filter passband characteristic and must be avoided.

In this design, a Q between 1.5 and 2.5 has been chosen for the input matching network, so that with 10–20% tolerance expected of $L_1$, $L_2$ and $C_{gs}$, the variation in $S_{11}$ is still very low. Using equation (6.1), this quality factor value translates into a $C_{gs}$ of about 1.2–1.5pF for a 50Ω source resistance at 1GHz frequency. For the CMOS technology we use this to limit the size of the quarter micron input device to a 500–700μm width depending on the influence of the Miller capacitance and the parasitic capacitance of the pads.

### 6.1.2 The Output Stage

To achieve the simultaneous requirements of 15dB gain and output matching, different load impedance structures have been studied and are presented in Fig. 6.2. The transconductance of the input stage is represented by $G_m$.

<table>
<thead>
<tr>
<th>Req. $G_m$</th>
<th>$Z_{out}$</th>
<th>$R_2$, $L_m$, $C_m$</th>
<th>$R_2$, $g_{m2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>220-250mS</td>
<td>$R_2$</td>
<td>110-125mS</td>
<td>110-125mS</td>
</tr>
<tr>
<td>110-125mS</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

![Figure 6.2: LNA Output Configurations](image-url)
6.1. The Low Noise Amplifier

The most straightforward way to achieve impedance matching is to use a 50Ω resistor load as shown in Fig. 6.2a. This implementation is very simple and permits broadband output matching limited at a high frequency by the drain capacitances of the input device. The biggest disadvantage of this approach is that to achieve 15dB overall gain, a $G_m$ of about 220–250mS is required and since the input transistor width is limited, this translates to a current consumption of 15–20mA.

A common method especially found in discrete implementations to achieve high gain with less current, is to use the principle depicted in Fig. 6.2b. The amplifier is loaded with higher impedance (250Ω in this case) and inductor $L_m$ and capacitor $C_m$ are used to match the 50Ω filter. To achieve impedance matching while avoiding excessively high degradation in filter performance in case of component value variations, a low Q matching network (Q=2) must be used. In this way, the required input $G_m$ is halved and a current of just 4–6mA is sufficient to achieve the desired performance. The matching inductor is also used to compensate for the parasitic drain capacitance of the input device, which, together with the high load impedance, forms a low frequency pole.

For a 1GHz LNA, the matching inductor and capacitor are in the region of 10–20nH and 1–2pF respectively and a fully integrated version is possible. In fact, the process we use has only 2 levels of metal and as a result, an integrated inductor will suffer substantial losses. Nevertheless, assuming a quality factor of 3 for $L_m$ and 1pF stray capacitance at node (a) the desired performance can be achieved by raising the load impedance to 1kΩ with a 12nH integrated inductor and a 1.2pF capacitor. Due to impedance transformation, at node (a) the signal is 6dB higher than at the output and can be in the region of 500mVpp. Therefore, since this node is centered at the supply voltage, the voltage supply must be shifted to a lower level to avoid damaging the device with signals higher than 2.5V. A minor disadvantage with this implementation is that with low Q inductors, the load impedance is mainly defined by their parasitic resistance. While with the right biasing scheme, the 250Ω poly resistor can be made insensitive to the usual parameter variations, the resistance of the inductor does not trace with the bias. Together with the inductance and capacitance variations of the matching network, this higher variation will cause higher deviations in gain as well as in $S_{22}$.
Due to these considerations, the method shown in Fig. 6.2c which favors gain control and broadband output matching has been used for the implementation of the load. A transimpedance stage similar to the one presented in Fig. 6.1b is used for the output. If the loop gain is sufficiently large, the approximate transimpedance of the output stage is given by the feedback resistance $R_2$, and the overall LNA gain is simply $G_m R_2$. Since the loop gain of the shunt-feedback scales down the input resistance of the transimpedance stage, $R_2$ can be raised to 100–200Ω without shifting the critical pole (a) to a lower frequency and 4–6mA in the input stage are sufficient to achieve the required $G_m$. The DC-output level can be easily controlled and with the right choice of $g_{m2}$ and $R_2$, a broadband output matching characteristic can be achieved. The main disadvantage of this third implementation is the high current required in the transimpedance stage to achieve the necessary output linearity. Nevertheless, with an optimized design, the target of an overall current consumption of 10mA can be achieved, as will be shown later.

The simplified schematic diagram of the 2-stage LNA is shown in Fig. 6.3. To achieve an overall $G_m \approx 120\text{mS}$ at 1GHz, $L_2$ lies around 1nH. This happens to be the value of a typical bondwire, so that no external inductor is necessary for $L_2$’s implementation. Inductor $L_1$, on the other hand, must be in the order of 12–18nH to compensate for $C_{gs}$ and is implemented by using a bondwire inductance in series with a high Q external inductor.

![Figure 6.3: LNA Schematic Diagram](image)
Without the cascode transistor \( M_2 \), the influence of \( M_1 \)'s Miller capacitance can add to that of the pad capacitance causing the design to deviate quite significantly from the ideal situation described by the equations shown in Fig. 6.Id. On the other hand, the cascode transistor may contribute some of its own noise to the amplifier because \( M_1 \)'s output impedance is low. This is due to the very short channel length and high current.

Having scaled down the contribution of the thermal noise of \( M_1 \)'s channel by the \( Q \) of the matching network, designing of the LNA input stage to achieve a low noise figure must concentrate on less well defined parasitic noise sources. Characterizing the transistors for NF before using them for the LNA, as is often done in traditional microwave LNA designs, is beyond our resources because this entails fabricating arrays of transistors of anticipated range of dimensions and bias currents, with anticipated layout. Since such devices are not designed to match the 50\( \Omega \) test environment, de-embedding the influence of pads and other test fixtures and measuring the intrinsic noise figure at 1GHz is a major undertaking. Further, minimum noise figure measurements from the CMOS process provider are usually based on transistors with a specific \( W/L \) ratio and layout and biased at unrealistically high currents such as 40–50mA. As a result, these figures are not particularly useful either. In the absence of accurate RF MOS transistor models, backed by reliable experimental verification, the low NF design for our LNAs was reached by combining general care in noise minimization and some specific, controlled experiments that were conceived to extract data on the relative importance of certain parasitic noise sources to the overall noise figure.

One such noise source is the induced gate current \([24, 25]\). At higher microwave frequencies, this noise source is important. Recently, a detailed analysis has been published \([22]\) which argues that induced gate current noise is also important for CMOS at the low gigahertz frequency range. It also proposed ways of optimizing the LNA design parameters, such as the matching network \( Q \), to achieve the minimum noise figure. Unfortunately, the optimal NF as predicted was not borne out by the results of their experiments, which still leaves the subject wide open.

Another important source of noise recently reported \([26]\) is the back-gating effect of the resistive substrate under the transistor channel. In the case of the 0.25\( \mu \)m used in our work, the substrate resistivity has
a fairly high value of 5Ω-cm, which could have an even higher effect. However, the experimental data given in [26], reported an NF difference of 1dB between a layout with good substrate contacts to ground and a layout with fewer contacts at a high level of 6–7dB overall noise figure. The important question for us was whether there will be much difference for LNAs which already have low noise figures.

6.1.3 Implemented LNAs

In the initial development stage, we succeeded in realizing a 0.25μm CMOS LNA, which we refer to as LNA-1. Care was taken in pad design, fingered gate layout etc. so that the noise figure was measured to be as low as 2dB. The substrate around the gate of M1 was already well grounded by rows of contacts surrounding the periphery of the 600μm gate formed by eighty 7.5μm by 0.25μm fingers, as shown in Fig. 6.4a. The input stage of the LNA-1 did not use the cascode transistor M2 so that the bias current was 6mA and the actual matching network Q was close to 1 due to the influence of Miller capacitance.

To investigate the influence of substrate resistance on achievable NF,
we integrated LNA-2, almost exactly the same as LNA-1, except that
the layout of the $M_1$ gate was changed to allow more substrate contacts
to be placed, as shown in Fig. 6.4b. The original LNA-1 was integrated
again in the same run as a reference to avoid confusing NF variation
from run to run thereby ensuring that the NF improvement is due to
difference in layout.

Realizing that $M_1$'s Miller capacitance is causing a significant deviation
of the matching network gain from that given in the ideal equations,
which results in higher current in the input stage, we also introduced the
cascode transistor $M_2$ at this stage. In doing so, the effective matching
network $Q$ increases from 1 to 2 enabling the bias current to be reduced
to 4mA. This has been implemented as LNA-3 in the same run as LNA-
1 and LNA-2. Although the change in $Q$ resulting from going from a
non-cascode configuration to one with a cascode is not exactly the same
as with designs for different matching network $Q$s for the same LNA
configuration, we believe that if the matching network $Q$ has as strong
an influence on the LNA NF as [22] seems to suggest, then we should
see some evidence of this by comparing LNA-2 and LNA-3. The gate
of $M_1$ in these two amplifier have exactly the same layout. All three
amplifiers should have noise figures less than or equal to 2dB.

We now turn our attention to the output stage. Resistors $R_1$ and
$R_3$ are used to bias the transistors. The use of PMOS current sources
was discarded due to the high parasitic capacitances associated with
them. The lack of voltage headroom combined with high bias cur-
rents constrained the $R_1$ and $R_3$ values to a couple of hundred ohms.
The limitation of $M_3$'s transconductance $g_{m3}$ by current and IP3 and
gate capacitance considerations means that only moderate loop gain is
achievable in the transimpedance stage and that the LNA gain must be
designed on the basis of the more accurate design equation:

$$A_v = \frac{1}{\omega_0 L_1} \left[ \frac{R_2 + R_L}{1 + g_{m3} R_L} || R_1 || Z_d12 \right] \frac{R_L}{R_L + R_2} \left( 1 - g_{m3} R_2 \right)$$  (6.2)

where $Z_d12$ is the output impedance of $M_1$ or the $M_1$-$M_2$ cascode and
$R_L$ is the parallel combination of the output impedance of $M_3$ ($Z_d3$),
the bias resistance $R_3$ and the 50Ω impedance of the inter-stage filter
($R_{50}$).
In addition to equation (6.2), the choice of $R_1$, $R_2$, $R_3$ and $g_{m3}$ are constrained by two other important requirements; realizing a 50Ω output resistance and providing a $-1$dB compression point that is sufficiently high. The latter is limited by the maximum output voltage for a given bias current $I_3$,

$$V_{o}^{\text{max}} = I_3 Z_3 = I_3 [(R_2 + R_1 || Z_{d12}) || R_3 || Z_{d3} || R_{50}] \quad (6.3)$$

where $Z_3$ describes the impedance seen by the drain terminal $M_3$. Because of the 50Ω input impedance of the inter-stage filter, $R_{50}$, $Z_3$ is less than 50Ω. This means that for a 0dBm (300mVp) CP requirement, the bias current $I_3$ must be no less than 6mA. In practice $R_1$ and $R_3$ can not be very high both because of voltage headroom and the need to implement the 50Ω output impedance for the LNA. In the worst case, $Z_3$ can be as low as 25Ω and twice the current is needed. The constraint on $R_1$, $R_2$ and $R_3$ in terms of 50Ω output impedance can be expressed as,

$$Z_o = \left( \frac{R_2 + R_1 || Z_{d12}}{1 + g_{m3}(R_1 || Z_{d12})} \right) || R_3 || Z_{d3} = 50Ω \quad (6.4)$$

where it can be seen that in the absence of $M_3$’s transconductance $g_{m3}$, the output impedance would be determined completely by $R_1$, $R_2$ and $R_3$, in which case $Z_3$ in eq. (6.3) would be as low as 25Ω. The design for the output stage is therefore primarily a trade-off of resistance values to satisfy eqs.(6.2)-(6.4) and minimize the required output current, while ensuring that $M_3$’s gate overdrive is sufficiently high to maintain a high IP3. The latter requirement sets a limit to $M_3$’s gate width.

A higher CP was aimed for with LNA-1, which led to higher output current. With the absence of the cascode device, the current of the input stage is also higher, resulting in lower values of $R_1$, $R_2$ and $R_3$. This leads to an output bias current of 12mA and an output CP measured at $-4$dBm. This output stage has been left unchanged for LNA-2 and LNA-3, so that only one thing is different between the two successive designs. Further optimization of the output stage, which took advantage of the lower bias current of the input stage, allows the level of $R_1$, $R_2$ and $R_3$ to be somewhat higher than before, so that only half of the
6.1. The Low Noise Amplifier

<table>
<thead>
<tr>
<th></th>
<th>$I_{M1}$</th>
<th>$I_{M3}$</th>
<th>$M1$</th>
<th>$M2$</th>
<th>$M3$</th>
<th>$R1$</th>
<th>$R2$</th>
<th>$R3$</th>
<th>Substr. contact</th>
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<tr>
<td>LNA-1</td>
<td>6</td>
<td>12</td>
<td>600</td>
<td>–</td>
<td>100</td>
<td>235</td>
<td>120</td>
<td>105</td>
<td>Fig. 6.4a</td>
</tr>
<tr>
<td>LNA-2</td>
<td>6</td>
<td>12</td>
<td>600</td>
<td>–</td>
<td>100</td>
<td>235</td>
<td>120</td>
<td>105</td>
<td>Fig. 6.4b</td>
</tr>
<tr>
<td>LNA-3</td>
<td>4</td>
<td>12</td>
<td>600</td>
<td>600</td>
<td>100</td>
<td>400</td>
<td>120</td>
<td>105</td>
<td>Fig. 6.4b</td>
</tr>
<tr>
<td>LNA-4</td>
<td>4</td>
<td>6</td>
<td>600</td>
<td>600</td>
<td>300</td>
<td>400</td>
<td>180</td>
<td>255</td>
<td>Fig. 6.4b</td>
</tr>
</tbody>
</table>

**Table 6.1: Summary of Implemented LNAs**

bias current is needed for the output stage with only a slight drop in the output compression point. The increase in resistance level is also expected to result in lower equivalent noise referred to the drain of $M_2$, so that the overall noise figure referred to the LNA input will be slightly lower. This design is referred to as LNA-4. The differences between the four designs and the key parameters of each design are summarized in Table 6.1.

**Figure 6.5: Complete LNA Schematic Diagram**
The actual schematic diagram of the complete LNA comprising a simple biasing scheme as well as the bypass switch attenuator is shown in Fig. 6.5. Signal $\bar{en}$ is used to select the desired gain. If $\bar{en}$ is set to ground, the LNA is active and 15dB amplification is obtained. In case of strong input signals, $\bar{en}$ is set to $V_{dd}$. The LNA is switched off and bypassed using transistor M4. The dimensions of device M4 are specific to realizing the 5dB attenuation at the output for a 50Ω load and transistor M5 is used to short circuit the network formed by $L_1,L_2$ and the gate capacitance of $M_1$.

### 6.1.4 Layout Considerations

![Figure 6.6: LNA Chip Microphotographs](image)

To characterize the LNAs, different chips have been implemented and measured. The chip microphotographs of LNA-2 and LNA-3 together with their pinout, are shown in Fig. 6.6a and b, respectively. For the RF-Input ($In$), the RF-output ($Out$) and the source of transistor $M_1$ where the bonding wire used in the input structure must be connected ($BW$), HF-pads have been used. The latter’s can be distinguished by the small clamp transistor used for protection and connected to the external padframe ($Gnd$). Wide connections have been used at
6.1. The Low Noise Amplifier

the source input output to cope with the high current levels involved. A wide connection has been also used for the gate input to minimize the gate resistance for better noise performance. In Fig. 6.6a, transistor $M_1$ with its fingered structure can be seen on the bottom left of the core, whereas the output transistor $M_3$ is shown on the bottom right. The cascode transistor $M_2$ (a replica of device $M_1$) can be seen in Fig. 6.6b. Input $V_h$, which is connected to a LF-pad, is used to bias the cascode transistor. The LF-pad can be distinguished by the two protection diodes, one connected to the external ($Gnd$) and one to the internal ($Vdd$) padframe. In the LNA-1 and LNA-2 versions that include the bypass switch, the upper-left pad has been replaced by a pad connected to $en$. LNA-3 and LNA-4 also use the same pad to switch the gain, while the biasing of the cascode transistor is done internally. The chip core size is about 300 x 150$\mu$m$^2$ depending on the implemented LNA.

6.1.5 Measured Performance

<table>
<thead>
<tr>
<th></th>
<th>LNA-1</th>
<th>LNA-2</th>
<th>LNA-3</th>
<th>LNA-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain [dB]</td>
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<td>14.2</td>
<td>14.3</td>
<td>16.4</td>
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<tr>
<td>NF [dB]</td>
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<td>1.74</td>
<td>1.97</td>
<td>1.6</td>
</tr>
<tr>
<td>iIP3 [dBm]</td>
<td>-2.0</td>
<td>-2.8</td>
<td>-7.3</td>
<td></td>
</tr>
<tr>
<td>iCP [dBm]</td>
<td></td>
<td>-17</td>
<td></td>
<td>-20</td>
</tr>
<tr>
<td>$S_{11}$ [dB]</td>
<td>-5.6</td>
<td>-6.8</td>
<td>-4.0</td>
<td>-8.0</td>
</tr>
<tr>
<td>$S_{22}$ [dB]</td>
<td>-8.0</td>
<td>-22</td>
<td>-11</td>
<td>-12</td>
</tr>
<tr>
<td>$S_{12}$ [dB]</td>
<td>&lt; -30</td>
<td>&lt; -30</td>
<td>&lt; -40</td>
<td>&lt; -40</td>
</tr>
<tr>
<td>$I_{dd}$ [mA]</td>
<td>18.3</td>
<td>18.1</td>
<td>16.6</td>
<td>10.8</td>
</tr>
</tbody>
</table>

Table 6.2: Summary of Measured Performance

The measured parameters of the implemented LNAs are summarized in Table 6.2. The reference amplifier LNA-1 achieves a low NF of 2dB, while providing the expected gain, input and output impedances and excellent linearity. With just an increase in the number of contacts, LNA-2 shows a significant improvement in noise figure to 1.74dB. This demonstrates the significant contribution of back-gate resistance to overall NF, at least for the 5Ω-cm substrate technology we used. The cascode transistor’s main influence on the input stage (LNA-3) is a 30%
reduction in current consumption in the first stage due to the higher Q and lower $g_m$ needed, and a 10dB improvement in reverse isolation. The price paid is a slight worsening of the noise figure which we believe to be due to the additional contribution of $M_2$. Although it was expected for the 0.35$\mu$m LNA in [22], no major improvement of NF is observed for a similar change of Q. The last amplifier, LNA-4, achieves the best performance trade-off for our application in terms of gain, noise figure and power consumption thanks to its better output stage design. The measured output compression point ($-5$dBm oCP) has only decreased slightly (1dB) from that of the other LNAs despite saving half of the output current. A very low noise figure of 1.6dB is measured near the optimum noise match.

In Fig. 6.7, starting with minimum noise figure at close to the center of the Smith-Chart, constant NF and gain circles have been measured in terms of the source impedance seen from the noise matched LNA. Thanks to the low Q design, these circles are large and widely spaced for small increments in gain and NF. This means that variations of matching network impedance due to component tolerances in production will not cause drastic gain and NF degradation.
6.1. The Low Noise Amplifier

Indeed, in 50Ω power matching conditions, the measurements of LNA-4 in Fig. 6.8 show that 15dB gain, -8dB S11 and 1.9dB NF can be simultaneously achieved. Due to the effect of the bond pad, the protection clamp and the PCB parasitic capacitances at both sides of L1, the actual 50Ω power match conditions of the LNA are slightly different from the ideal equations and to achieve the desired trade-off, a 2pF matching capacitor must be added at the input of the LNA.

Turning our attention to linearity, Fig. 6.9 shows the measured iIP3 and iCP of LNA-2 and LNA-4. High IP3 values far exceeding requirements have been measured, confirming the intrinsic high linearity of MOS devices. The measured compression points meet the requirements of the blocking test and as expected are 3–4dB below the limit set.
by the output current. Due to the purely resistive output matching, the measured $S_{22}$ has a broadband characteristic and is well within the specifications.

### 6.2 The RF-Mixer

As summarized in Table 4.1, the chief requirements for the RF mixer are 50Ω matching to the inter-stage and 330Ω to the IF-filter, a low noise figure, high IP3 and a moderate gain to reduce the noise contribution of subsequent stages to the receiver front-end. To satisfy every requirement, single-balanced (SBM) or double-balanced (DBM) mixers based on the Gilbert cell are virtually the only choice, as proven by the fact that they are found in virtually every BJT RF front-end IC.

![Figure 6.10: Basic Active Mixer Schematic Diagram](image)

The basic implementation of an active mixer is shown in Fig. 6.10. A single-balanced implementation is depicted by the black part only, while a double-balanced mixer is represented by the complete schematic diagram. In a Gilbert mixer, the incoming RF voltage input signal is converted to current by an input stage with overall transconductance $g_{mo}$. After the conversion, the signal passes through commutating switches $M_{sw}$ that perform the function of frequency translation.
6.2. The RF-Mixer

6.2.1 Conversion Gain of SBM and DBM Gilbert Mixers

In an SBM, assuming ideal switches, the signal current is effectively multiplied by a squarewave $S(t)$ whose frequency is that of the local oscillator and that switches either between 1 and 0 in case of a single-ended output or between $-1/2$ and $1/2$ if the output is taken differentially. In a DBM, on the other hand, the signal current is multiplied by a squarewave $S(t)$ that switches between $-1$ and 1 independently if the output is taken single-ended or differentially. The Fourier series of $S(t)$ for an SBM is shown in eq.(6.5), where in the case of a differential output, the DC-term is not present.

$$S(t) = \frac{1}{2} + \frac{2}{\pi} \left[ \cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t) + \frac{1}{5}\cos(5\omega_{LO}t) - ... \right] \quad (6.5)$$

For a DBM $S(t)$ is:

$$S(t) = \frac{4}{\pi} \left[ \cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t) + \frac{1}{5}\cos(5\omega_{LO}t) - ... \right] \quad (6.6)$$

For a sinusoidal input signal $V_{in} = V_{RF} \sin(\omega_{RF}t)$, after multiplication and filtering at the intermediate frequency, the useful output current is:

$$I_{out}(t) = \frac{1}{\pi} g_{mo} V_{RF} \cos [(\omega_{LO} - \omega_{RF})t] \quad (6.7)$$

for a SBM and

$$I_{out}(t) = \frac{2}{\pi} g_{mo} V_{RF} \cos [(\omega_{LO} - \omega_{RF})t] \quad (6.8)$$

for a DBM implementation. Therefore, in the ideal case, the effective conversion gain of a mixer is $g_{mo}/\pi$ for a SBM and $2g_{mo}/\pi$ for a DBM. Actually, the LO signal is a sine-wave generated by an LC-oscillator. The achievable LO amplitude is limited by power consumption considerations to values in the order of 300mVp (0dBµ). The switching process is less than ideal and the effective transconductance tends to decrease to $g_{mo}/4$ for a SBM and $g_{mo}/2$ for DBM, respectively.
6.2.2 Noise in SBM and DBM Mixers

The noise figure of a Gilbert mixer can be estimated calculating the contribution of the various sources of noise to the output. Two main sources can be identified:

- Noise of the input stage that is increased by folding.
- Noise of the commutating switches \( M_{su} \).

The noise introduced by the input stage can be calculated with the same method used to compute the LNA input stage noise. As shown in the previous section, a low noise input stage may have a NF of about 2–3dB. In a Gilbert mixer, this noise contribution is increased by the folding process of mixing. The principle of folding is shown in Fig. 6.11. Assuming white thermal noise generated by the input stage, the LO signal (composed by different harmonic terms) mixes noise at various frequencies down to the IF, where it is added together. As a result, the noise power at the output is increased by a factor of \( \pi^2/2 \) (or 6.9dB) for an SBM with a single-ended output where the DC term also contributes to the overall output noise and \( \pi^2/4 \) (or 3.9dB) in the case of a DBM or an SBM with a differential output.

![Figure 6.11: The Principle of Folding](image)

Figure 6.11: The Principle of Folding
6.2. The RF-Mixer

In fact, the presence of pole (a) (shown in Fig. 6.10) at the source of the switching devices (usually placed at 2–3 times the RF frequency) reduces the high-frequency noise contribution and an increase of 6.5dB and 3.5dB is more realistic. If one adds this value to the noise of the input stage, a lower bound for the NF of a Gilbert mixer can be found. In case of an SBM with a single-ended output, the minimum NF is therefore 9–10dB whilst for a DBM or an SBM with differential output, it is 6 – 7dB.

The second important source of noise comes from the switching devices. A qualitative understanding of the contribution of the commutating transistors to the overall output noise can be explained with the help of Fig. 6.12. As stated earlier, in a practical implementation, the LO signal used to drive the mixer is a sine-wave with limited amplitude. When the commutating transistors are completely switched, they act as cascode devices and a negligible amount of current noise $i_n(t)$ is added to the output. On the other hand, there are two time slots $\tau$ during each switching time period $T$ when all switching transistors conduct current.

![Figure 6.12: Noise Bursts due to Non-Perfect Switching](image)

**Figure 6.12:** Noise Bursts due to Non-Perfect Switching
During these time slots the switching devices act as differential pairs and bursts of noise are added to the output signal.

An exact calculation of this noise contribution is rather difficult since during the time slot $\tau$, the transconductance of the switching transistors $g_{mSW}$ varies in time and is different for each device. Furthermore, during the switching period, the devices pass through saturation, moderate and weak inversion so that their exact behavior can not be easily defined. To simplify the analysis somewhat, we assume that during $\tau$ the transconductance $g_{mSW}$ of the $M_{SW}$ is constant and equals the worst-case condition. The maximum amount of noise is introduced when $V_{LO}(t) = 0$ and the current is evenly split between the two devices. Assuming a simple quadratic model and considering that for small $\tau$ (which is needed to retain a sufficient conversion gain) $\sin(x) \approx x$, the output noise generated by the switching devices is calculated as follows:

$$
\frac{2}{T} \int_0^\tau i_{nSW}^2 \, dt = \frac{2\pi^2}{T} i_{nSW}^2 = \frac{2(\sqrt{2} - 1)}{\pi} \frac{\Delta V_{gs}}{V_p} i_{nSW}^2 \approx \frac{1}{4} \frac{\Delta V_{gs}}{V_p} i_{nSW}^2 \quad (6.9)
$$

As shown in eq.(6.9) this contribution can be reduced using a large LO signal but this is limited to about 300mVp as explained earlier. On the other hand, $i_{nSW}^2 \approx g_{mSW}$ and for a constant bias current $\Delta V_{gs} is \approx 1/g_{mSW}$. This means that with the first order approximation, the noise introduced by the switching transistors does not depend on their size. The only relevant design consideration for the switching pairs is that they must be as big as possible to allow the best conversion gain and that their size is limited by the increasing effect of the stray capacitances which cause a deterioration in performance at high frequency and represent a large load for the LO driver. Experiments show that the noise introduced by the switching devices is in the order of that introduced by the input stage [27]. The expected NF for our mixers is therefore about 3dB higher than the lower bound calculated before.

The other non-dominant sources of noise that may increase the mixer NF are:

- The wide-band noise that may reach the mixer input and that is folded to the IF frequency in the same way as the input stage noise.
6.2. The RF-Mixer

In our architecture, this contribution is minimized by the image filter which is necessary not only to suppress strong signals that may still be present at the image frequency, but also to suppress the out-of-band noise generated in the LNA.

• The noise that reaches the LO ports and that is amplified when the commutating devices act as a differential pair. It can be shown that this contribution is negligible for small \( \tau \) periods and for an oscillator with low phase noise.

• The load resistor thermal noise that can be minimized with sufficiently large loads (i.e. sufficiently high voltage gain). An upper limit to this voltage gain is given by the limited headroom available at the output and by linearity considerations for the blocks following the mixer. Moreover, should the output load have to be matched to a defined impedance (which is the case here) the voltage gain is also limited by the value of the Q of the matching network.

6.2.3 Implemented Mixers

During this project, the three different mixer configurations shown in Fig. 6.13 have been investigated. Since the noise of the input device is just a part of the overall noise, whether the input transconductor contributes 2dB or 3dB to the overall NF is not very critical. Therefore, to achieve broadband input impedance matching, all three mixers make use of a common-gate configuration. In bipolar implementations, some sort of degeneration in the input stage is usually needed to achieve the required linearity. Due to the higher linearity inherent in CMOS devices, a high gate-source overdrive is sufficient in CMOS mixers and the degeneration of the input stage is not required.

The simpler configuration implemented is the single-balanced mixer shown in Fig. 6.13a. One of the characteristics of a single balanced solution is that the LO-IF-feedthrough is not rejected. However, in the case of a super-heterodyne receiver, the LO signal is suppressed by the IF filter and a single-balanced structure can be used. Impedance matching is achieved with a \( g_m \) of 20mS in the input device. This limits the overall conversion gain to 6.35mS \( (g_m/\pi) \) in the ideal case and 5mS \( (g_m/4) \) in a practical implementation due to non-perfect switching. For
best noise performance, the output must be taken differentially. An external LC-matching network is required to achieve 10dB voltage gain as well as impedance matching to the 330Ω IF filter.

In Fig 6.14a, a configuration that can be used to match a differential IF filter is shown (as used in our project). A large load resistor $R_{L1}$ is employed to achieve high voltage gain. The DC-current flows through inductors $L_1$ which are also used together with capacitors $C_1$ to form the required matching network. Capacitor $C_d$ are added to sink the high frequency components that could saturate the mixer outputs.

If the IF filter is single-ended, the configuration shown in Fig. 6.14b can be used instead. Differential to single-ended conversion is achieved with the network formed by the two $C_2$’s and $L_2$. In this case, the output current $i$ can be calculated to be:

$$i = \frac{i_2(1 + s^2L_2C_2) - i_1}{1 + s^2L_2C_2 + 2sR_oC_2(1 + s^2C_2L_2/2)} \quad (6.10)$$

And if $\omega_{IF}^2 L_2 C_2 = 2$:

$$i = \frac{i_2(1 - 2) - i_1}{1 - 2 + 2sR_oC_2(1 - 1)} = i_1 + i_2 \quad (6.11)$$
6.2. The RF-Mixer

The voltage at node (b) is \( U_b = iR_o \), where \( R_o \) is the total resistance at node (b). At node (a) on the other hand, the voltage is \( U_a = i(R_o + 1/sC_2) \). Therefore, to avoid excessively high swing \( U_a \), a high capacitance \( C_2 \) is welcome. On the other hand, a high capacitance means a high \( Q \) in the \( C_2, L_2, R_o \) network and this must be avoided due to tolerances. Therefore, a \( Q \approx 4 \) has been chosen for this implementation. Impedance transformation and impedance matching is achieved with \( L_3 \) and \( C_3 \). The DC-current can flow in both mixer paths through \( L_3 \) and \( L_2 \). High frequency components are short circuited by capacitances \( C_2 \).

The design of the current and the transistor size are summarized in Table 6.3. The component values for a differential and a single-ended filter are summarized in Table 6.4. Minimum length devices have been used for the input stage as well as for the commutating devices to minimize the effect of the parasitic capacitances. The current consumption and the size of the input transistor are dictated by the IP3 requirement and the necessary input \( g_m \). To minimize noise, a small transistor is required to implement the current source. The size of the switches is limited by their associated stray capacitances. Due to the low conversion gain of the SBM, a relatively high impedance is required at its output to achieve 10dB gain. This involves a matching network with relatively high \( Q \). At node (a) of both implementations, the resulting signals are as high as \( 1.8V_{pp} \) which makes this implementation impractical.

A doubling of the conversion gain can be achieved with the double-
balanced mixer shown in Fig. 6.13b. Two 40mS transistors are required at the input to achieve impedance matching to the RF-image filter. The conversion $g_m$ is as high as 12.7mS in the ideal case and will be around 10mS for a real implementation. As stated earlier, the lower bound for the NF remains unchanged. The higher conversion gain relaxes the requirements at the output. Since a matching network with a lower Q is sufficient to achieve the desired amplification, the filter performance can be better controlled and the swing at the output is limited to less than $1V_{pp}$. Since the input devices are working near moderate inversion, to achieve the required input $g_m$ and the same linearity of the SBM, the DBM needs slightly less than twice the current and input transistors which are almost 4 times wider (exactly twice the current and 4 times wider transistors for ideal quadratic behavior). Optimum switching is achieved with transistors having the same size as the input devices. A summary of the design values are shown in Table 6.3 and Table 6.4. The main drawback of this implementation is that since the RF-image filter is single-ended, an external balun is required at the input to provide single-ended to differential conversion.

A third method to achieve high conversion gain without the need of external components is to use the single-ended double-balanced mixer (SE-DBM) depicted in Fig. 6.13c which has been derived from the Gilbert micromixer [28]. In the SE-DBM, the class-A differential input pair is replaced by a class-AB buffer. This buffer is a combination of a non-inverting common-gate and an inverting common-source amplifier. The transistor in the common-gate path is designed for 20mS transconductance to properly terminate the RF-filter. The same 20mS transconductance is assigned to the transistor in the common-source path to implement the differential structure. Since both paths are driven with a full swing signal, the same overall conversion gain of 12.7mS (10mS) achieved in the DBM configuration is retained. The noise of

<table>
<thead>
<tr>
<th></th>
<th>$I_{tot}$ [mA]</th>
<th>$M_1$ [μm]</th>
<th>$M_{sw}$ [μm]</th>
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<td>300</td>
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<tr>
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<td>300</td>
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Table 6.3: Mixers Design Parameters
6.2. The RF-Mixer

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<tr>
<th>Differential output</th>
<th>$R_{L1}$ [kΩ]</th>
<th>$C_1$ [pF]</th>
<th>$L_1$ [μH]</th>
<th>Q</th>
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</thead>
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<td>1.5</td>
<td>4</td>
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<td>DBM</td>
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<td>2</td>
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<tr>
<td>SE-DBM</td>
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<td>8</td>
<td>0.85</td>
<td>2</td>
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</tbody>
</table>

<table>
<thead>
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<th></th>
<th></th>
<th></th>
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</thead>
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<td>-</td>
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<td>14</td>
<td>-</td>
<td>0.7</td>
<td>-</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 6.4: Matching Network Parameters

The common-gate input device appears as a common mode noise at the output. Therefore, if the output is taken differentially, the lower bound for the NF is solely given by the noise of the common-source input device and is equal the one of a DBM configuration. Thanks to the class-AB structure, this mixer has a virtually 'unlimited' input capability and does not compress. The SE-DBM has been designed after the characterization of the SBM and the DBM. Its parameters have been optimized with the experience gained in these first two implementations, where a very high IP3 has been achieved. Therefore, the input devices are designed to work more in moderate inversion, the commutating transistors are the same as those used in the DBM implementation and 50% less power is needed in comparison to the DBM design.

6.2.4 Layout Considerations

The microphotographs of the the DBM and the SE-DBM are shown in Fig. 6.15a and b, respectively. The only difference in the pinout between the two designs is the differential vs the single-ended input and the absence of the biasing pad in the SE-DBM implementation.
The top of the core is composed by the inter-leaved commutating switches which use the same layout in both implementations whereas the bottom of the core is occupied by the input stage. The core size is approximately 160 x 150µm².

6.2.5 Measured Performance

The measurements of the mixers have been performed using a 1020MHz, 0dBm LO with 50Ω termination at the LO ports. The RF input signal was set to 949MHz so that the resulting IF frequency is 71MHz. The measured effective transconductances for the SBM and the DBM are 4.9mS and 8.5mS, respectively. As expected, these values are about 30% lower than the theoretical maximum due to imperfect switching.

The measured NF for the SBM is 9.9dB, whereas the DBM achieves a slightly better value of 9.6dB. In both cases, this means that the noise power due to the switching devices is in the order of that due to the input stage. The S₁₁ measurement for both mixers is shown in Fig. 6.16. The common-gate input guarantees excellent input matching with a broadband characteristic for both mixers. For the DBM, the balun needed at the input limits the impedance matching accuracy. The measured S₁₁ nevertheless stays under −8dB at all frequencies below 1GHz. The S₁₁ degradation at higher frequencies is due to the increasing influence of
parasitic capacitances. Figure 6.17a shows that the measured iIP3 for the DBM is as high as +9dBm and iCP is -4dBm, which meets specs outlined earlier by a comfortable margin.

The gain as measured for the SE-DBM is similar to that of the DBM. Unfortunately, the current source used in this design as well as the biasing method have not been optimized for low noise. As a
result, the measured noise figure is 3dB higher than expected. The IP3 measurement of the SE-DBM is shown in Fig. 6.17b. Also shown is the gain characteristic where we see no compression due to the class-AB operation. Due to the lower $g_m/I$ ratio used to design the input transistor, the IP3 is slightly lower. The performance of the mixers is summarized in Table 6.5.

<table>
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<th>SBM</th>
<th>DBM</th>
<th>SE-DBM</th>
</tr>
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<tbody>
<tr>
<td>Conv. Gain [mS]</td>
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<td>8.5</td>
<td>8.3</td>
</tr>
<tr>
<td>NF [dB]</td>
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<td>9.6</td>
<td>12.6</td>
</tr>
<tr>
<td>iIP3 [dBm]</td>
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<td></td>
</tr>
<tr>
<td>iCP [dBm]</td>
<td>-4</td>
<td>-4</td>
<td>N.A.</td>
</tr>
<tr>
<td>$S_{11}$ [dB]</td>
<td>$&lt;-15$</td>
<td>$-11$</td>
<td>$-17$</td>
</tr>
<tr>
<td>$I_{dd}$ [mA]</td>
<td>3.5</td>
<td>6</td>
<td>4</td>
</tr>
</tbody>
</table>

Table 6.5: Summary of Measured Performance

6.3 The IF-Amplifier

The basic specifications for the IF-amplifier are summarized in Table 4.1. As explained during receiver planning, this is probably the toughest block in the receiver section due to the required high gain at the 71MHz IF frequency, to the accuracy required in the 2dB gain steps and to the high output linearity which is needed to avoid saturation caused by interferers. These requirements are even more challenging considering that the CMOS technology we use has a limited voltage supply of 2.5V and that because of the common substrate, the combination of high gain and relatively high intermediate frequency may cause oscillation.

The basic configuration for the 71MHz IF-amplifier is shown in Fig. 6.18. It is an open loop, 3-stage differential amplifier with AC coupling between the stages [29]. Although a closed loop architecture may allow better gain and accuracy control for our combination of gain and frequency levels, it is not suited for our application due to high power consumption [30].

In an open-loop, multi-stage amplifier, the choice of the number of
gain stages is defined by power consumption and linearity considerations. Starting from a single stage implementation and increasing the number of stages, power and transistor size decrease in a nearly exponential way since they are mainly dictated by the GBW product of each stage. Once the minimum feature size permitted by the design rules is reached and transistor size cannot be decreased further, linearity requirements begin to dictate power consumption, which increases linearly with the number of stages. In our design, a 3-stage solution is the optimal choice. Each stage produces GBW of \( \approx 1.5 \text{GHz} \). Power consumption is still dictated by GBW but device size is reaching a value where a further decrease would affect good matching and therefore also gain accuracy.

To allow independent control of the DC input levels and limit the effect of DC-offset which could saturate the amplifier, AC coupling is used between stages. Differential design has been used, because of the advantages it brings such as suppression of even harmonics, rejection of common mode noise and double the signal swing for a given supply voltage (which is only 2.5V in our case).

Similar to the LNA and the mixer, the input impedance of the IF-amplifier must be matched to the characteristic impedance of the external IF-filter. To achieve impedance matching as well as a low noise figure, common-gate input structure is used in the first stage of the IF-amp. The second and third stages are identical and have a common-source input structure to achieve a higher input impedance.

Gain programmability is achieved with a switchable gain between 0 to 20dB in 2 dB steps in the first stage and between \(-10\text{dB}\) to 20dB in 2dB steps for the other two stages. The implementation of gain control
is realized by switching arrays of active devices. It is worth noting that the 2dB step which corresponds to a ratio of 1.259 is a stringent requirements since it does not allow the array to be split in identical blocks which could provide the best matching accuracy.

![Gain Principle of the IF-Amplifier](image)

**Figure 6.19: Gain Principle of the IF-Amplifier**

To obtain an accurate absolute gain which is independent of process parameters as well as temperature and supply voltage variations, the principle depicted in Fig. 6.19 has been used. Gain is defined by the $g_{mi}$ of an nMOS input device divided by the $g_{mo}$ of a diode-connected load transistor of the same type. Current density is similar in both transistors. A common drain buffer is provided at the output to drive the next stage.

A big challenge in the design of the IF-amplifier relates to the risk of instability due to the parasitic feedback between amplifier output and the sensitive input. When the gain is set to its maximum of 60dB, the isolation between the output and the input of the amplifier must be better than 60dB just to prevent oscillation. If accurate gain control is required as specified in our case, then the isolation may have to be 20–30dB better, as the parasitic feedback will make the closed-loop gain differ from that of the open-loop.

In bipolar technologies, substrate noise is less of a problem since the transistors are isolated by wells formed by the low-ohmic buried-layer and plugs which can be shorted to ground. Experience shows that typical isolation achievable between bipolar transistors can easily be around 40–50dB.

In many CMOS technologies, transistors are built with a lowly doped epitaxial layer with typical resistance of (5–20Ω-cm) deposited on a low-ohmic substrate (0.01–0.1Ω-cm) which is intended to prevent latch-up.
In such cases, it is virtually impossible to achieve the required isolation since signals can find a way through the low-ohmic substrate and spread all over the circuit without attenuation.

Realizing that with a careful and extensive use of substrate contacts, latch-up can be avoided even without a low-ohmic substrate and that without the epi-layer the process is less expensive, in the latest CMOS processes, the latter tend to be removed. This is the case in our technology, where there is no epitaxial layer and the transistors are directly built in the common substrate which has a fairly high resistivity of (5Ω-cm). Without the low-ohmic path the coupling problem is somewhat less severe and the required isolation becomes possible with a careful design and layout.

To achieve the isolation we need, the strategy presented in Fig. 6.20 has been adopted. The differential approach has been used in combination with a carefully symmetrical layout so that the signals injected in the substrate by the differential outputs sum up to form a common mode signal that is rejected by the input. Since better isolation can be achieved by increasing the distance between nodes that inject noise and nodes that collect it, the layout of the IF-amplifier has a rectangular shape with the inputs and outputs placed on the most distant edges.
To collect noise on surface, $p^+$ guard-rings connected to ground have been placed around the critical structures. It can be shown that for our $5\Omega$-cm substrate, well-designed guard-rings can reduce the parasitic feedback by at least an order of magnitude [31]. Moreover, some residual noise is collected at the back of the die which is also connected to ground.

### 6.3.1 First Stage

![Schematic Diagram of the First Stage](image)

**Figure 6.21: Schematic Diagram of the First Stage**

A simplified schematic diagram of the first stage of the IF-amplifier is shown in Fig. 6.21. In the shaded areas, the input differential structure used to generate the input transconductance ($g_{mi}$) are highlighted along with the transistors which define the load ($g_{mo}$). A current steering principle has been used to program the gain. The current passing through the various parallel input stages (11, just 2 of them are shown) can be either switched to the path defining the gain, or to $V_{dd}$, using transistors $M_{sw}$. The input impedance is defined by all the input transistors ($M_{1-0dB}$, $M_{1-2dB}$, $\ldots$, $M_{1-20dB}$) in parallel. It is equal to $330\Omega$, the characteristic impedance of the channel filter, independent of the selected gain.
6.3. The IF-Amplifier

\[ g_{m-\ln} = g_{m1-0dB} + g_{m1-2dB} + \cdots + g_{m1-20dB} \]

\[ = \frac{2}{R_{saw}} = 6mS \quad (6.12) \]

In a common-gate configuration, the minimum achievable NF is 2.2dB if just the input devices contribute to noise and other sources are negligible. In our design, relatively big transistors are needed for the current sources to keep their \( V_{dsat} \) low. The resulting transconductance \( g_{m-CS} \) is as high as 2/3 of the \( g_m \) of the input nMOS transistors and the noise contribution is no longer negligible. An estimate of the NF, referring to the input, is given by:

\[ g_{m-CS} \approx 0.67g_{m-\ln} \quad (6.13) \]

\[ NF = 10 \log(1 + \frac{2}{3} \frac{e^2_{IF}}{e^2_{330}}) \]

\[ = 10 \log(1 + \frac{4kT(\frac{2}{3g_{m1-n}} + \frac{2g_{m-CS}}{3g_{m-\ln}})}{4kTR_{saw}}) \quad (6.14) \]

Combining (6.13) and (6.14) we find:

\[ NF \approx 10 \log(1 + \frac{2}{3}(1 + 0.67)) \approx 3.3dB \quad (6.15) \]

To improve output linearity, the load transistors \( M_2 \) are linearized by source-degeneration using the voltage-controlled resistances \( M_3 \). For optimum linearity, the ratio between the widths of \( M_2 \) and \( M_3 \) is set to 6 [32]. Cascode devices \( M_4 \) and \( M_5 \) are introduced to improve accuracy. Firstly, they decrease the \( g_{ds} \) of each P-current source and that of each input transistor, thereby suppressing their parasitic effect. Furthermore, \( M_4 \) and \( M_5 \) decrease the parasitic capacitance at node (\( \bar{a} \)) where the dominant pole is placed, in addition to keeping the latter independent of gain selection. Source follower \( M_6 \), whose capacitive load to (\( \bar{a} \)) is low, is used to drive the next stage. The dominant pole, defined by the load resistance in parallel with all the stray capacitances at node (\( \bar{a} \)) is
placed at about 150MHz. This translates in an attenuation of 0.9dB for a 71MHz signal. A common mode feedback structure (not shown) is used to regulate the DC voltage.

To achieve high accuracy in the gain steps, all parallel input stages must have the same current density. To further improve matching, the length of the input transistors is set to 0.35μm instead of the 0.25μm minimum feature size. Moreover, to keep the same $V_{ds}$ on all input devices, the width of each switching transistor $M_{sw}$ scales with the width of its corresponding input transistor. The realization of 2dB steps (1.259 in voltage gain) does not allow the use of matched layout structures. Furthermore, at low gain where small devices are used, parallel connection of transistors cannot be used and different devices must be used to set different gains. To realize the desired gain steps, parallel input devices are used either alone or in combination, according to the switching scheme shown in Fig. 6.22.

The sizes of individual input transistors are shown on the top; each cross indicates that the transistor in the corresponding column is switched in; and the combined width of all the transistors switched in for a given gain is shown on the right. At 0dB (row 1) just one stage of 8.4μm width is directed to the gain path. On the other hand, to realize 12dB gain (row 7), 3 parallel stages must be switched in, resulting in a total

**Figure 6.22: Gain Setting Scheme and Input nMOS Width (1st Stage)**
width of 35.4μm. It is noted that to double the gain, size and current must be more than doubled. This is mainly due to the residual effect of the $g_{ds}$ of the input transistors which is shown in Fig. 6.23.

Taking $g_{ds}$ into consideration, a simple analysis for the input $g_m$ leads to:

$$g_{m\text{-eff}} \approx g_{m\text{-ln}} \left(1 - \frac{g_{ds\text{-ln}}}{g_{m\text{-casc}}} \right) \quad (6.16)$$

Doubling current and size of input nMOS doubles $g_{m\text{-ln}}$. On the other hand, the $g_{m\text{-casc}}$ of the cascode transistor is only increased by $\sqrt{2}$. Moreover, the increase in current in the cascode device decreases the $V_{ds}$ of the input transistors so that their $g_{ds}$ is more than doubled.
For short devices, the exact value of $g_{ds}$ is hardly predictable. Therefore, to allow simple refinements in the gain step accuracy, particular care has been taken in the layout as shown in Fig. 6.24. The poly defining the gates is drawn with an overhead that allows a 20% increase in size by stretching the mask that defines the active area. The source/drain contacts are placed in such a way that a 20% decrease in size can be also achieved. Therefore, if the input pairs as well as the corresponding current sources are stretched by the same amount, the $g_m$ of each element in the array can be varied by as much as ±20% while keeping the current density unchanged and this can be done by changing just one processing mask.

6.3.2 Second and Third Stage

![Figure 6.25: Schematic Diagram of the Second and Third Stage](image)

The simplified schematic diagram of the second and third stages with the input and load highlighted by the shaded areas, is shown in Fig. 6.25. To realize high input impedance, a common-source structure is used. Gain variation between 0 to 20dB is achieved by switching in different combinations of parallel input stages with their corresponding pMOS current sources. To achieve −10dB attenuation, a parallel output stage ($M_{2-10dB}$, $M_{3-10dB}$) can be switched in so as to decrease the
6.3. The IF-Amplifier

Figure 6.26: Gain Setting Scheme and Input nMOS Width (2nd-3rd Stage)

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<thead>
<tr>
<th>Size Gain</th>
<th>-10dB</th>
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<th>13.6μ</th>
<th>15.2μ</th>
<th>17.8μ</th>
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<td>-8dB</td>
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<td>20dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>79.6μ</td>
</tr>
</tbody>
</table>

load impedance. To realize the desired gain step, the switching scheme shown in Fig. 6.26 is used. Accuracy is again enhanced by the use of constant current density in the devices defining the gain and cascode transistors $M_4$ and $M_5$. To achieve the correct gain, compensation is still needed for the $g_{ds}$ effect of the input transistors. The same layout technique has also been used to allow a simple refinement of gain step. The dominant pole at node (a) is placed at about 150MHz for the 0dB load and increased to about 470MHz for the −10dB load. This means that for the 0dB load, the attenuation at the output is about 0.9dB and reduced to 0.1dB for the −10dB load. Therefore, to compensate for this 0.8dB difference, the −10dB load is sized to attenuate the gain by just 9.2dB.

As shown in the previous section, the IF-amplifier must be capable of handling blocking signals as high as −8dBm at the output without compressing. An output IP3 of −2dBm is also required to keep inter-modulation sufficiently low. The combination of differential implementation, linearized load, high linearity of MOS devices as well as sufficient gate-source overdrive, allows us to achieve excellent oCP and
oIP3 values without excessive current consumption.

The first IF-amp stage draws a constant current from the 2.5V power supply. Current consumption for the second and third stage depends on the selected gain. At 60dB the total current consumption is 2.6mA. Minimum current consumption is 1.8mA, which occurs when only the first stage is used for amplification, while the gain for the second and the third stage is set to 0dB.

6.3.3 Layout Considerations

![IF-strip Chip Microphotograph](image)

**Figure 6.27: IF-strip Chip Microphotograph**

In Fig. 6.27 the microphotograph of the complete (and bonded) IF-
strip comprising the IF-amplifier and the demodulator is shown. At
the bottom, the three amplifier stages can be seen. The amplifier gain
can be programmed in three 4-bit internal registers which are accessed
using pins En1 – 3 and Code1 – 4. Signals En1 – 3 select which register
(stage) must be programmed and Code1 – 4 are used to program the
gain (0000 for $-10$dB to 1111 for $+20$dB). The amplifier core size is
0.61 x 0.72mm².

### 6.3.4 Measured Performance

The same structure shown in Fig 6.27 but without the demodulator has
been used to characterize the IF-amplifier alone. In Fig. 6.28 both the
absolute gain and the differential gain error are shown. The minimum
gain is measured to be $-20.9$dB whereas the maximum is $58$dB, which
shows good absolute accuracy considering the open loop structure. No
sign of instability has been observed at maximum gain. This shows
that thanks to the differential implementation, a symmetrical layout
and extensive use of guard-rings, high isolation has been achieved and
the circuit does not oscillate despite the common substrate.

![Figure 6.28: IF-Amplifier Gain](image)

Figure 6.28: *IF-Amplifier Gain*
An excellent differential accuracy with typical error of 0.1–0.2dB has also been achieved, despite the difficulty in matching devices at such a high frequency, low supply voltage and low power. As expected, the maximum differential error is found when the gain changes from −2dB to 0dB and is limited to 0.4dB.

The measured NF is 3.8dB at high gain. This value is in line with the NF calculated at 3.3dB which accounts only for the contributions of the two main sources of noise.

Fig. 6.29 shows the linearity characteristics of the IF-amplifier. Both measurements have been carried out with the amplifier gain set to 50dB. To provide the 50Ω output required by the measurement instrument, a buffer has been added at the IF-amp output. This buffer has an attenu-

![Diagram](image)

**Figure 6.29: IF-Amplifier CP and IP3**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. gain [dB]</td>
<td>−20.9</td>
</tr>
<tr>
<td>0dB gain [dB]</td>
<td>−0.7</td>
</tr>
<tr>
<td>Max. gain [dB]</td>
<td>+58</td>
</tr>
<tr>
<td>Δ Error (typical) [dB]</td>
<td>&lt;0.2</td>
</tr>
<tr>
<td>NF−330Ω (max.gain) [dB]</td>
<td>3.8</td>
</tr>
<tr>
<td>IP3 (52dB gain) [dBm]</td>
<td>−34.5</td>
</tr>
<tr>
<td>iCP (52dB gain) [dBm]</td>
<td>−49.5</td>
</tr>
<tr>
<td>I_{dd} [mA]</td>
<td>2.6</td>
</tr>
</tbody>
</table>

**Table 6.6: Summary of Measured Performance**
6.4. The Demodulator

The demodulation of 20dB so that the measured gain is around 30dB. The compression characteristic shown in Fig. 6.29a is typical for the linearization technique we use. The effective 1dB loss in gain is achieved for an input signal of $-42.5\text{dBm}$ (CP2), but since for a $-47.5\text{dBm}$ input the loss is just below 1dB, we take the latter as the 1dB compression point. The iIP3 measurement is shown in Fig. 6.29b. Again, due to the linearized load, the IM3 characteristic has a particular shape and the measured iIP3 is as high as $-32.5\text{dBm}$. This means that even with 60dB amplification, the blocking signals will not saturate the amplifier and the inter-modulating components will stay well below the desired signal. A summary of the measured characteristics is shown in Table 6.6.

6.4 The Demodulator

The quadrature demodulator must split the IF input into I and Q baseband signals with sufficient amplitude and phase accuracy and amplify them by 16dB. As stated earlier, 30dB USRR are required to guarantee the performance. The gain is obtained in the down-conversion mixers which are also responsible for the linearity characteristics. Phase and amplitude accuracy, on the other hand, are mainly determined by the precision of the 90° phase shifter.

6.4.1 The Down-Conversion Mixer

The simplified schematic diagram of one down-conversion mixer is shown in Fig. 6.30. The 71MHz IF input signal is converted to base-band by a double balanced Gilbert mixer which is shown in the shaded area on the left. A common-source structure is used, which provides a high input impedance. The double-balanced configuration is needed mainly to reject the LO feedthrough which could saturate the following active low pass filters (LPFs). Due to the low supply voltage, the gate-source voltage overdrive of the input devices $M_1$ should be kept low, resulting in insufficient linearity. To allow input signals as high as $-8\text{dBm}$ to be handled without excessive distortion, resistive source-degeneration is provided. Minimum-length switching transistors $M_{sw}$ are sized to operate near weak inversion to guarantee good switching and therefore
a high conversion gain with a $-3\text{dBm}$ LO signal. Assuming perfect switching, the mixer conversion gain is given by (6.17).

$$G_m = \frac{I_{\text{out}}}{V_{\text{in}}} = \frac{2}{\pi} \frac{g_{m1}}{1 + g_{m1} \frac{R_1}{2}} \quad (6.17)$$

Once the signal is converted to base-band, it is amplified by the transimpedance stage shown in the shaded area on the right to provide the desired 16dB gain with sufficient linearity. With regard to the simple transimpedance stage shown in Fig. 6.1b, some other components have been added. Capacitor $C_2$ is used in parallel combination with resistor $R_2$ to form a pole at approximately 500kHz. This first order low pass filter is used to suppress any residual LO signal feedthrough and further attenuate the blocking signals, so that their output level is less than 0dBm. Resistor $R_3$ defines the DC operating point, while capacitor $C_3$ is used to short circuit high frequency components. Equation (6.18) describes the transimpedance stage gain characteristic.

$$\frac{V_{\text{out}}}{I_{\text{in}}} = -R_3 \left(1 - g_{m2} R_2\right) \frac{1 + s \left(\frac{C_2 R_2}{1-g_{m2} R_3}\right)}{\left(1 + g_{m2} R_3\right) \left(1 + s \left(\frac{C_3 R_3}{1+g_{m2} R_3}\right) \left(1 + s C_2 R_2\right)\right)} \quad (6.18)$$

Assuming $g_{m2} R_2 >> 1$, $g_{m2} R_3 >> 1$ as well as $R_2 = R_3$ and $R_2 C_2 = R_3 C_3$ the gain characteristic is simply:
6.4. The Demodulator

<table>
<thead>
<tr>
<th>nMOS</th>
<th>W</th>
<th>L</th>
<th>$I_b$</th>
<th>$g_m$</th>
<th>Res.</th>
<th>Cap.</th>
<th>[µF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>7.5x2</td>
<td>0.5</td>
<td>36</td>
<td>510</td>
<td>$R_1$</td>
<td>$C_2$</td>
<td>6</td>
</tr>
<tr>
<td>$M_{sw}$</td>
<td>5x2</td>
<td>0.25</td>
<td>18</td>
<td>540</td>
<td>$R_2$</td>
<td>$C_3$</td>
<td>7.5</td>
</tr>
<tr>
<td>$M_2$</td>
<td>10x4</td>
<td>1</td>
<td>36</td>
<td>590</td>
<td>$R_3$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$M_3$</td>
<td>10x4</td>
<td>1</td>
<td>72</td>
<td>830</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 6.7: Component Design Values

\[
\frac{V_{out}}{I_{in}} = \frac{R_3}{(1 + sC_2R_2)}
\] (6.19)

Actually, to minimize power consumption, the value of $g_{m2}$ is fairly limited and the complete equation (6.18) must be considered. The final DC-gain depends on $R_3$ as well as $R_2$ and $g_{m2}$. The zero formed by $R_2$, $C_2$ and $g_{m2}$ is compensated by the pole formed by $R_3$, $C_3$ and $g_{m2}$. Together they realize a doublet above 10MHz which in first approximation does not influence the gain characteristic.

Source followers $M_3$ are used to drive the LPFs. The LPF input impedance is planned to be in the region of $30k\Omega - 50k\Omega$, so that a good driving capability is achieved with just 0.8mS transconductance in the source followers. Due to the bulk transconductance $g_{mb}$, the latter's gain is limited to 0.85 or $\approx -1.5$dB. The transistor sizes as well as the values of all the components are shown in Table 6.7.

Although $\Delta A$ and $\Delta \varphi$ are mainly due to the phase shifter, any mismatch in the I and Q paths could increase these errors, thereby further degrading USRR. To ensure best matching, relatively long transistors have been employed as shown in Table 6.7. Devices $M_1$, which work at 71MHz, are 0.5µm long while devices working at base-band ($M_2$, $M_3$) are 1µm long. The total current consumption for each down-conversion mixer is 290µA.

6.4.2 The Phase-Shifter

There are many ways to realize a fully integrated phase-shifter. Each way has its own advantages and drawbacks and the choice of a suit-
able configuration depends on the required performance characteristics (i.e. power consumption level, bandwidth, accuracy, ...). Three basic configurations are briefly discussed below:

- **$\lambda/4$ transmission line**: a first way to implement a phase shifter is to use two transmission lines with different lengths as shown in Fig. 6.31.

![Figure 6.31: $\lambda/4$ Transmission Line](image)

If one path is $\lambda/4$ longer (electrical length) than the other one, the two outputs will display 90° shift in phase due to the time difference needed by the LO signal to reach the end of the lines. At the output, two termination impedances are required to avoid reflections. The shift in phase $\varphi$ depends on the transmission line length $l$ as well as on the substrate dielectric constant $\varepsilon_{r(sub)}$ as shown in equation (6.20).

$$\varphi \approx \frac{l}{\sqrt{\varepsilon_{r(sub)}}} \quad (6.20)$$

For a given technology, both parameters are well controlled and display small absolute variations. As a result, this phase shifter can be quite accurate, even if it is just at one single frequency. Moreover, since transmission lines are lossless, the only dissipated power is that required to drive the termination impedances, which is quite low. Unfortunately, this implementation is not advantageous at low frequencies since it requires a big silicon area to realize the required line lengths.

- **RC-CR network**: in this implementation, a low pass and high pass filter are used in combination to provide two signals with 90° phase difference as shown in Fig. 6.32.
At the output of the RC-CR network, the amplitude response $A_i$ and phase response $\varphi_i$ for the I-channel and $A_q$, $\varphi_q$ for the Q channel can be calculated to be:

$$A_i = \frac{1}{\sqrt{1 + (\omega R(C + C_p))^2}}$$  \hspace{1cm} (6.21)

$$\varphi_i = 0^\circ - \text{atan}(\omega R(C + C_p))$$  \hspace{1cm} (6.22)

$$A_q = \frac{\omega RC}{\sqrt{1 + (\omega R(C + C_p))^2}}$$  \hspace{1cm} (6.23)

$$\varphi_q = 90^\circ - \text{atan}(\omega R(C + C_p))$$  \hspace{1cm} (6.24)

As shown by eq.(6.22) and (6.24), assuming equal components $R$ and $C$ and parasitic capacitances $C_p$, the phase difference between the two paths is $90^\circ$, independent of the frequency. In fact, a typical mismatch for poly resistors and poly-poly capacitor is in the order of $1 - 2\%$. Parasitics, on the other hand, are less controlled and mismatches can be in the order of $4 - 5\%$. If the parasitic capacitance $C_p$ is kept smaller with respect to capacitor $C$ ($20 - 25\%$), the total mismatch is $4 - 5\%$ which translates to a phase error $\Delta \varphi \approx 1 - 2^\circ$.

On the other hand, the amplitudes are equal just at the cut-off frequency of the filters, when $\omega RC = 1$. However, if limiting amplifier are provided at the output, the amplitudes can be clipped and the mismatch $\Delta A$ can be reduced without affecting the phase

\[\text{Figure 6.32: RC-CR Network}\]
behavior so that an overall USRR in the order of 30—35dB can be achieved over about two octaves of bandwidth [33].

One problem of this phase shifter is power consumption. In fact, to drive the impedance associated with the RC-CR network, a buffer is required between the VCO and the phase shifter. Moreover, since the quadrature signals are attenuated by 3dB (at the center frequency) by the lossy RC-CR network and since the limiting amplifiers must provide enough gain to clip the amplitudes in case of mismatch, a quite high current consumption is also required here.

The second problem is tied up with component tolerances. Due to the variation of the absolute value of $R$ and $C$, which is out of the control of the designer, the actual center frequency may be up to ±40% out. As a result, in worst-case conditions, the useful bandwidth is reduced to about half an octave.

If higher accuracy or a higher bandwidth is required, phase corrector circuits can be added between the RC-CR network and the limiting buffer [6]. Another method to increase the operating bandwidth is to use a network based on polyphase filters. In both cases, improved performance must be paid with an increased complexity and power consumption.

- **Digital divider**: in the digital divider approach, two toggle flip-flops clocked on the opposite edges are used to generate the quadrature signals at half the clock frequency as shown in Fig. 6.33.

![Figure 6.33: Digital Divider Principle](image)

If the driving LO has a 50% duty cycle, high accuracy in the order of 40—45dB USSR can be achieved. Moreover, since the generation of the two phases does not rely on geometry or passive component values, this kind of phase shifter can achieve the
6.4. The Demodulator

widest bandwidth, ideally down to DC. Another advantage which makes it the best solution when compared to others is that this implementation is also very compact.

To guarantee 50% duty cycle in the driving LO, even harmonics must be minimized. To achieve this, a differential VCO can be used. In a CMOS implementation, the flip-flops are usually implemented using enhancement source-coupled logic (ESCL) [34] which has advantages such as low power consumption, independence on supply variations, low sensitivity to substrate noise and low noise injection.

Low power consumption is mainly a result of the low logic swing level which is compatible with the VCO signal swing and the LO swing required to drive the quadrature mixer, so that no buffers are required between the different circuits.

The main drawback of this phase shifter is that double the LO frequency is required at the input to generate the desired quadrature signals. The disadvantage is not the increase in current consumption required in the VCO to achieve the desired frequency. In fact, since no buffers are required, the overall current consumption of the VCO and phase shifter combination is still less than for a RC-CR implementation. The main problem is that the realization of a stable and accurate VCO at twice the LO frequency may be critical due to the characteristics of the given technology, so that such an implementation may not guarantee the required robustness.

As explained in the receiver planning section, the phase shifter for the demodulator must generate quadrature signals at a single frequency of 71MHz with 30dB USB which correspond to $\Delta A < 0.3$dB and $\Delta \varphi < 3^\circ$ and 300mVp amplitude. Although suited for a low power implementation of an accurate single frequency phase shifter, the $\lambda/4$ transmission line approach has been discarded due to the excessively low frequency ($\lambda/4 \approx 1m$). Since the generation of a 142MHz LO does not pose problems, the digital divider approach has been selected due to its superior performance. ESCL logic has been used to implement the flip-flops. To understand how ESCL works, we can refer to Fig. 6.34a where a simple inverter is shown. The inverter consists of a simple differential pair where the input transistor are used as switches so that the current flows in either one branch or the other depending on the
Chapter 6. Design of the Receiver Blocks

The polarity of the input signal. The resulting output signal is inverted.

The most important design considerations are the amplitude of the signal which is defined by $I_b R$, the speed which is limited by the capacitance associated with the output node and the inverter gain which must be higher than unity to guarantee proper signal propagation (we take 2 to allow sufficient margin). In the actual implementation, PMOS transistors biased in the triode region are used as resistive load as shown in Fig. 6.34b [35, 36]. The resulting load resistance is proportional to the inverse of $1/\sqrt{I_b}$. Since the $g_m$ of the input transistor is proportional to $\sqrt{I_b}$, the bandwidth of the inverter can be controlled varying the input current, without affecting the gain ($g_m R$) and with little effect on the output swing ($\sim \sqrt{I_b}$). A 1:1.2 ratio in the current mirror at the bottom is used to guarantee that the PMOS devices stay in triode region.

The schematic diagram of one flip-flop is shown in Fig. 6.35. Power consumption and transistor sizes are usually optimized considering the required bandwidth, gain and swing. Here, on the other hand, due to the low operation frequency and the CMOS technology used, such an optimization would lead to transistors smaller than the minimum feature size. Therefore, the strategy here has been to set the transistors width to 30% more than minimum for best matching. The resistor size (PMOS device length) is then defined by the required bandwidth (200MHz), and the current by the required swing. The resulting gain of each latch is around 3 which guarantees signal propagation. Resistor $R_1$ is used to set the DC-level needed to drive the mixer. The design
values are shown in Table 6.8. The overall current consumption of the phase shifter is 90\(\mu\)A.

<table>
<thead>
<tr>
<th></th>
<th>W [(\mu\m)]</th>
<th>L [(\mu\m)]</th>
<th>I [(\mu\A)]</th>
<th>Res. [k(\Omega)]</th>
</tr>
</thead>
<tbody>
<tr>
<td>(M_1)</td>
<td>3.2x2</td>
<td>0.25</td>
<td>(I_{b1}) 15</td>
<td>(R_1) 18</td>
</tr>
<tr>
<td>(M_2)</td>
<td>3.2x2</td>
<td>0.25</td>
<td>(I_{b2}) 30</td>
<td></td>
</tr>
<tr>
<td>(M_3(20k\Omega))</td>
<td>3.2</td>
<td>0.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(M_4(10k\Omega))</td>
<td>3.2</td>
<td>0.3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 6.8: Component Design Values

6.4.3 Layout Considerations

The layout of the complete demodulator is shown on top of Fig 6.27. The two down-conversion mixers can be easily distinguished while the phase shifter can be barely seen between the latter and the IF-amplifier.
Core size of both mixers is $600 \times 250 \mu m^2$ while the phase shifter occupies an area of just $100 \times 50 \mu m^2$.

### 6.4.4 Measured Performance

![TRACE A: Ch1+jCh2 Spectrum](image1)

TRACE A: Ch1+jCh2 Spectrum

- Offset: -24 000.0 Hz
- dBm: 20
- LogMag: 10 dB/div
- dBm: -80 dBm
- Center: 0 Hz
- Span: 100 kHz

![TRACE B; Ch1+jCh2 Main Time](image2)

TRACE B; Ch1+jCh2 Main Time

- BMkr: 992.1875 us
- 1.4616V
- -43.592 dB
- I-Q
- 1.2 V
- 20 mV/div
- 843.703713417 mV
- 1.23629628658 V
- 52.404 deg

Figure 6.36: Measured Demodulator Performance

The accuracy of the quadrature signals can be shown using Fig. 6.36. In the top-half, the sum and the difference of the quadrature output channels are displayed. The average suppression of the undesired sideband is more than 43dB, which corresponds to less than 1° phase error and less than 0.1dB gain mismatch respectively. A polar plot of the I and Q channels is shown in the lower half of the figure. As can be expected from the gain and phase accuracy, the result is a nearly perfect circle.

The linearity measurement is shown in Fig. 6.37. The input compression point is $-3$dBm. This value is dictated by the limited headroom at the output of the transimpedance stage. The input IP3, on the other hand, is $+10$dBm and is defined by the linearity of the degenerated input. A summary of the measured performance is shown in Table 6.9.
6.5 Design of the Output Filters

Two 16dB gain, 150kHz, 4th-order Bessel low pass filters are required at the end of the receiver chain. The filters serve as anti-aliasing filter for their corresponding A/D converter. They also complete the channel selection by further suppressing out-of-band blocking signals, the residual LO feedthrough and residual adjacent channel interferers. Bessel filters are employed due to their flat group delay characteristics which avoid dispersion.

Many techniques can be used to implement integrated filters. In our case, switched capacitor filters were ruled out to avoid aliasing. Since signals in the $1V_{pp}$ range must be accommodated within a 2.5V supply
with no more than $-45\text{dB THD}$, the $g_m$-C method was also ruled out as usually it is not sufficiently linear. Instead, active-RC filters have been chosen, for their high linearity and better noise characteristics.

The low sensitivity associated with the low Q characteristic of the filter transfer function allows cascaded Sallen-Key biquads to be used, as shown in Fig. 6.38 in single-ended representation. The Sallen-Key configuration enables the realization of two pairs of complex poles as well as active gain using just two op-amps. The main drawback of this kind of filter is that the cut-off frequency depends on the component tolerances so that in worst-case conditions, the cut-off frequency can vary as much as $\pm40\%$ from that designed. However, since the main purpose of the
6.5. Design of the Output Filters

The design of the output filters is anti-aliasing, this kind of behavior can be accepted. The gain characteristic, on the other hand, depends on the matching between resistors and is therefore well controlled.

Another advantage with this particular configuration is that the positive and negative inputs of the op-amps are at ground and virtual ground respectively, so that a large input swing capability is not required. This means that despite the high signal level, a rail-to-rail input op-amp with its associated increased distortion due to crossover is not required. At the output, on the other hand, rail-to-rail is required. Another requirement for the op-amp is the driving capability. The filter must be able to drive the A/D converter input impedance. Since the base-band chip used in the final implementation was not specified at this stage, an input impedance of 10kΩ/10pF has been assumed for the A/D converters. An appropriate op-amp structure that fulfills all the requirements has been presented in [37]. The schematic diagram of the amplifier used for this implementation is shown in Fig. 6.39.

The main characteristics are low voltage operation, low power con-

Figure 6.40: LPF Chip Photograph
sumption, and compactness. In the schematic diagram the PMOS folded cascode input stage and the class-AB rail-to-rail output are highlighted in the shadowed areas. The rest of the circuitry is needed to correctly bias the output stage.

The same op-amp has been used for both stages. The signal amplification has been evenly split between the two stages, so that each stage has 8dB gain. Since the required dynamic range is not critical, the impedance levels chosen for the filter are a compromise between the driving capability of the op-amp and the silicon area required to implement the resistors and capacitors. Each differential filter consumes 640μA and can handle large signals of up to +15dBm at the output.

6.5.1 Layout Considerations

The microphotograph of the chip containing the low pass filters is shown in Fig. 6.40. Worth noting is the highly symmetrical design. Most of the active area, which is 600 x 1'200μm² is used by the resistors and capacitors. Low-frequency pads have been used for all signal pads. The external reference signal \( V_{ref} \) is used to set the op-amp input DC-level at half the voltage supply.
6.5.2 Measured Performance

The filter has been tested at the nominal voltage supply of 2.5V and also at lower voltages. Thanks to the low voltage operation capability of the op-amps, good performance has been measured with the voltage supply down to 1.5V. The frequency and phase characteristics of the filters from 5kHz up to 0.5MHz, measured under nominal conditions are shown in Fig. 6.4. The measured pass-band gain is 15.7dB and the cut-off frequency has been measured to be 160kHz.
Chapter 7

Design of the Transmitter Blocks

7.1 The Modulator

In this section, the design of the complete modulator comprising the first order input LPF, the up-conversion-mixer and the phase shifter are presented. The specifications for all the blocks have been formalized during transmitter planning and are summarized in Table 4.2.

7.1.1 Up-Conversion Mixer

As shown during transmitter planning, the up-conversion mixers must provide a $-17$dBm signal to the RF-filter, minimize harmonic production and carrier feedthrough. To satisfy these requirements, a differential structure based on a double balanced Gilbert mixer with a regulated input stage (to ensure high linearity) has been implemented. A schematic diagram of a single up-conversion mixer is shown in Fig. 7.1. The differential structure is used to reject even harmonics. The double balanced configuration, on the other hand, suppresses the RF carrier at the mixer output. Since the I,Q signals at the input are at base-
band, a power efficient way to implement a highly linear circuit is to use negative feedback. The feedback loops based on the OTAs regulate the currents in transistors $M_1$ so that the differential input voltage $V_{in}$, assuming $R_1$ equals $R_2$, will appear on resistor $R_3$. The input signal voltage is therefore translated into an input signal current $I_s$ so that $I_s = V_{in}/R_3$. Assuming perfect switching devices $M_{sw}$, the mixer conversion $g_m$ depends only on the linear component $R_3$ and is calculated as:

$$g_m = \frac{2}{\pi} \times \frac{1}{R_3} \quad (7.1)$$

Since the main purpose of the 1st order LPF is to smooth the signal after D/A conversion, its cut-off frequency is not critical and typical absolute tolerances of RC realizations ($\pm 40\%$) can be tolerated. Therefore the 1.2MHz pole has been embedded in the feedback loop and is realized by resistor $R_2$ and capacitor $C_2$.

The purpose of capacitor $C_3$ is twofold. First, it is used as a com-
7.1. The Modulator

compensating capacitor for the OTA. Second, it is also used as a sink for high frequency spurious signals which could feed through the Miller capacitance of transistor $M_1$ and cause instability in the OTA. To minimize the input offset, particular care has been taken in the design of the OTAs. Large input transistors as well as well matched structures have been employed. Folded cascode OTAs with PMOS input stages are designed for 50MHz bandwidth and draw 500$\mu$A each from the 2.5V supply.

The minimum required bias current in each mixer can be calculated from the required output power of $-17$dBm ($20\mu$W) which the modulator must provide to the 50$\Omega$ RF-filter. Given the 50$\Omega$ output resistance $R_{out}$ of the modulator required to match with the filter impedance, the modulator must provide $40\mu$W total power to 25$\Omega$ total load. For a quadrature modulation scheme, this means that each mixer must provide $40\mu$W to the load and the peak current output signal is as follows:

$$I_{os} = \sqrt{2} \sqrt{\frac{40\mu W}{25\Omega}} = 1.8mA_p \quad (7.2)$$

Taking into account approximately 6dB of attenuation associated with the switching devices ($-3.92$dB in case of perfect switching), the base-band signal current $I_s$ flowing into $R_3$ is 3.6mA$p$. To guarantee a minimum current in device $M_1$, the bias current $I$ is set to 4mA, allowing for some margin. The total power consumption of the I,Q modulator, including the OTAs, is therefore 18mA.

For a $1.4V_{pp}$ input signal, the required impedance for resistor $R_3$ is 200$\Omega$. Gain accuracy is achieved using the same resistor type to implement resistances $R_3$ and $R_{out}$ (low-resistance poly, in this case). Assuming $\pm20\%$ maximum variation between the integrated resistors and the resistance of the RX-filter, the modulator gain will vary less than $\pm10\%$ which corresponds to less than $\pm1$dB.

Since the RF filter is single-ended and the modulator output is differential, an LC-matching network with a $Q = 1$ as shown in Fig. 6.14b is required at the output to convert the signal. For optimum matching and since they work at base-band, devices $M_1$ are 0.5$\mu$m long. Transistors $M_{sw}$, on the other hand, are minimum length devices whose
Chapter 7. Design of the Transmitter Blocks

Table 7.1: Component Design Values

<table>
<thead>
<tr>
<th>nMOS</th>
<th>W [µm]</th>
<th>L [µm]</th>
<th>I_b [mA]</th>
<th>g_m [mS]</th>
<th>Res. [kΩ]</th>
<th>Cap. [pF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>M_1</td>
<td>10x20</td>
<td>0.5</td>
<td>4</td>
<td>25</td>
<td>4</td>
<td>33</td>
</tr>
<tr>
<td>M_sw</td>
<td>5x48</td>
<td>0.25</td>
<td>2</td>
<td>27</td>
<td>4</td>
<td>3.8</td>
</tr>
</tbody>
</table>

dimensions are designed to work in weak inversion so that a $-3$dBm carrier is sufficient to guarantee good switching. The size of resistors $R_1, R_2$ and capacitor $C_2$ is a compromise between noise performance and required silicon area. A summary of the transistor as well as the component sizes is shown in Table 7.1.

7.1.2 Phase Shifter

One of the most challenging tasks in transmitter design is the realization of the integrated 900MHz, 90° phase shifter using CMOS technology. Although the digital divider approach would be the best choice in terms

Figure 7.2: Schematic Diagram of the Phase Shifter
of accuracy, achievable bandwidth as well as power consumption, the realization of a 2GHz VCO has been judged too risky for this first implementation. Therefore, since the transmission line method is narrowband and would also require too much silicon area even at 1GHz, a realization based on a RC-CR approach has been chosen. As shown in the previous section, this kind of phase shifter can achieve the required USSR of 30dB over a sufficiently large bandwidth even taking into account component tolerances. Because there is no requirement for higher accuracy, additional phase correction circuits have not been implemented to minimize power consumption.

The schematic diagram of the implemented phase shifter is shown in Fig. 7.2. To minimize LO feedthrough, the up-conversion mixers must be driven with a symmetrical signal. Therefore, a fully differential approach has been chosen for the phase shifter. Clipping source-coupled pairs have been used to implement the limiting buffers. Provided there is sufficient gain in the buffer stage, the output amplitude is defined by the voltage drop on the load resistor $R_L$ when all the current $I_b$ flows in the corresponding branch. At the buffer output, the pole formed by resistor $R_L$ and the sum of all stray capacitances $C_s$ has been placed to about 2.5GHz. The stray capacitance $C_s$ is formed in part by the gate capacitance of the switching device $M_{sw}$ of the up-conversion mixer and in part by the drain capacitance of the limiting buffer devices. The latter have a substantial influence due to the technology used. A relatively high frequency for the pole has been chosen so that any mismatch between the quadrature paths at this node (which may occur quite easily between stray capacitances), will have little impact on the phase accuracy.

To achieve sufficient gain despite the 3dB attenuation in the RC-CR network on the one hand and to get the 0dBm output signal on the other, 6mA is required for each source-coupled pair. The size of the

<table>
<thead>
<tr>
<th>nMOS</th>
<th>W [μm]</th>
<th>L [μm]</th>
<th>$I_b$ [mA]</th>
<th>$g_m$ [mS]</th>
<th>Res. [Ω]</th>
<th>Cap. [pF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>16x10</td>
<td>0.25</td>
<td>3</td>
<td>27</td>
<td>$R_1$</td>
<td>$C_1$ 1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$R_L$ 100</td>
<td></td>
</tr>
</tbody>
</table>

Table 7.2: Component Design Values
resistors $R_1$ and the capacitors $C_1$ forming the RC-CR network is a trade-off between the resulting phase shifter input impedance and the relative size of the $C_1$ with regard to $M_1$'s gate capacitance. In fact, on the one side, a high resistor $R_1$ and a low capacitor $C_1$ would achieve a high input impedance which would reduce the power consumption of the buffer required between the VCO and the phase shifter. On the other side, as shown in the previous section, to minimize the influence of $M_1$'s gate capacitance to the overall mismatch, $C_1$ should be at least 5 times bigger than the former. The values resulting from the design process are summarized in Table 7.2.

### 7.1.3 Layout Considerations

![Modulator Chip Microphotograph](image-url)
The chip microphotograph of the modulator is shown in Fig. 7.3. The two up-conversion mixers are at the bottom, separated by a biasing cell, while the top is occupied by the phase shifter. The layout of the resistors and capacitors forming the RC-CR network of the phase shifter uses symmetry and dummy structures for optimum matching. Since any stray in series with \( R_1 \)s and \( C_1 \)s will have a detrimental effect on phase accuracy, the phase shifter is also very compact and the necessary wiring is kept as short and as symmetrical as possible. High frequency pads have been used for the TX-outputs (RF-out) and the LO inputs (LO). The corners are filled with de-coupling capacitors connected between \( V_{dd} \) and \( Gnd \). The core size is 1200 x 750\( \mu m^2 \).

### 7.1.4 Measured Performance

The modulator output spectrum for a GMSK modulated input is shown in Fig. 7.4. A \(-3dBm, 915MHz\) LO carrier has been fed to the
phase shifter input, whereas the base-band I/Q input signal level has been set to $1.4V_{pp}$. The output characteristic is measured well within the specified mask. The total integrated power at the modulator output is $-17$ dBm as specified.

To appreciate the individual contribution of the various spurious components determining overall modulator accuracy, one can examine the output characteristic shown in Fig. 7.5 for a 67 kHz, $1.4V_{pp}$ quadrature input signal. As expected, the dominant contributor to phase error is the image signal. In fact, other spurious components are more or less negligible. The image signal is suppressed by about 31 dB, which means that an accuracy of $\Delta A = 0.3$ dB and $\Delta \varphi = 3^\circ$ has been achieved in the quadrature channels. The carrier component is suppressed by more than 50 dB thanks to the double balanced structure and the well matched OTAs. Higher harmonics are all suppressed by more than 50 dB as a result of the modulator’s differential implementation and the high linearity of the base-band feedback loop. A summary of modulator

---

**Figure 7.5: Single Sideband Modulated Sinewave**

<table>
<thead>
<tr>
<th>Ref Lvl</th>
<th>RBW</th>
<th>VSW</th>
<th>RF Att</th>
<th>Unit</th>
<th>dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>-10 dBm</td>
<td>204.40881764 kHz</td>
<td>5 kHz</td>
<td>0 dB</td>
<td>-17.04 dBm</td>
<td></td>
</tr>
</tbody>
</table>

---

**Table:**

<table>
<thead>
<tr>
<th>Channel</th>
<th>Frequency [kHz]</th>
<th>Power [dBm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>204.40881764</td>
<td>-17.04</td>
</tr>
<tr>
<td>2</td>
<td>204.40881764</td>
<td>-58.35</td>
</tr>
<tr>
<td>3</td>
<td>204.40881764</td>
<td>-34.66</td>
</tr>
<tr>
<td>4</td>
<td>204.40881764</td>
<td>-57.84</td>
</tr>
</tbody>
</table>

---
7.2. The Pre-Amplifier

performance as measured is shown in Table 7.3

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power [dBm]</td>
<td>−17</td>
</tr>
<tr>
<td>Carrier suppr. [dBc]</td>
<td>&gt;50</td>
</tr>
<tr>
<td>I,Q image suppr. [dBc]</td>
<td>&gt;31</td>
</tr>
<tr>
<td>Harmonics suppr. [dBc]</td>
<td>&gt;55</td>
</tr>
<tr>
<td>$I_{dd}$ [mA]</td>
<td>30</td>
</tr>
</tbody>
</table>

Table 7.3: Summary of Measured Performance

7.2 The Pre-Amplifier

The primary requirements for our pre-amp are 50Ω matching at both the input and output, a high gain of 24dB and high output power (for CMOS) of +3dBm with sufficient linearity to avoid the degradation of PA efficiency. To keep the output harmonics low, without further filtering before the PA, a class-A or a Class-B approach can be considered. Although more efficient, a class-B push-pull approach has been discarded due to the weakness of PMOS devices. Therefore, a two-stage class-A solution as shown in Fig. 7.6 has been chosen. Since transmitter power consumption is dominated by the PA, power consumption is not critical in the pre-amp. Attention is paid, however, to low power design.

The first stage, comprising $M_1$, its biasing and the matching network, is similar to the input stage of the LNA. Therefore the same principles and equations hold true. The main difference here is the relatively high input level of −20dBm. Since small signal linearity is proportional to the overdrive of an MOS transistor, a relatively small device biased at a relatively high current of 11mA has been used for $M_1$. Because of the large overdrive of $M_1$ and the low supply voltage, no cascode transistor has been used in this design to ensure that $M_1$ stays always in saturation. Due to the lack of the cascode transistor, the effect of the Miller capacitance at the input is increased. However, since $M_1$ is smaller, the total gate capacitance is more or less the same as in the LNA design: the Q of the input matching network is still approx. 2, inductor $L_1$ is approx. 1.2–1.5nH and can be still realized with a bonding wire.
The second stage is a transimpedance amplifier again similar to the LNA output stage. Here however, since there is no combination for \( M_3 \), \( R_2 \) and \( R_3 \) that can simultaneously achieve the desired gain, bandwidth, linearity, matching impedance and DC-operating point, the load resistance \( R_3 \) has been replaced by the external inductor \( L_m \). The purpose of this inductor is threefold. First it serves as a path for the DC-current. Second, some of its inductance is used to resonate with the drain capacitance of \( M_2 \) at 900MHz to achieve the desired bandwidth. Third, it is used together with external capacitor \( C_m \) to implement a low Q matching network. Thanks to the output matching network, the impedance seen by the drain of \( \text{M}_3 \) is increased so that less current is required in the output stage to deliver the required +3dBm output power to the 50\( \Omega \) load.

The Q of the matching network has been set to about 1.6. The reasons for choosing such a low value for Q is to retain low sensitivity on component tolerances on the one side and to limit the swing at the drain of \( \text{M}_3 \) on the other. In fact, +3dBm signal level means an output swing of about 900mV\(_{pp}\). Assuming a Q of 1.6, this translates to a swing of 1.5V\(_{pp}\) at the drain of \( \text{M}_3 \). The same Q will also scale the required pre-amp output impedance to about 130\( \Omega \) \( (50\Omega \times Q^2) \). To design the output stage, the same reasonings and equations (6.2)-(6.4) used in the
7.2. The Pre-Amplifier

<table>
<thead>
<tr>
<th>$I_{M_1}$ [mA]</th>
<th>$I_{M_2}$ [mA]</th>
<th>$M_1$ [µm]</th>
<th>$M_3$ [µm]</th>
<th>$R_1$ [Ω]</th>
<th>$R_2$ [Ω]</th>
<th>$R_{DC}$ [Ω]</th>
<th>$L_1$ [nH]</th>
<th>$L_2$ [nH]</th>
<th>$L_m$ [nH]</th>
<th>$C_m$ [pF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>16</td>
<td>400</td>
<td>300</td>
<td>200</td>
<td>200</td>
<td>60</td>
<td>15</td>
<td>1.2</td>
<td>12</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 7.4: Pre-amp Design Parameters

LNA design can therefore be used. The different parameters here are higher gain $A_v$, absence of $R_3$ which must be set to infinity, output impedance $Z_0$, load $R_{50}$ (which is now 130Ω) and maximum output swing $V_o^{max}$ which is 1.5Vpp.

To avoid a swing higher than the 2.5V power supply which could damage the devices, the DC-output is shifted to 1.5V using resistor $R_{DC}$ in series with $L_m$ and AC-bypassed by external capacitor $C_{DC}$ as shown in the figure. This leaves enough headroom at the bottom to always keep device $M_3$ in saturation. At DC, $R_3$ also helps stabilize the bias condition of transistor $M_3$ through feedback resistor $R_2$.

The required performance can be achieved with 16mA in the second stage for a total current consumption of 27mA. The key parameters of

Figure 7.7: Pre-amp Chip Microphotographs
the design are summarized in Table 7.4.

### 7.2.1 Layout Considerations

A chip microphotograph of the designed pre-amplifier is shown in Fig. 7.7. The pinout is the same used for LNA-2 so that the same PCB (with different external components) can be used to characterize the circuit. Worth noticing is the wide output path which is designed to conduct currents up to 30mA. The pre-amplifier core size is 220 x 170\(\mu m^2\).

### 7.2.2 Measured Performance

![Figure 7.8: Pre-amp Gain Characteristic](image)

The measurements of the transmitting pre-amplifier show that in addition to high gain and adequate input and output impedances, good linearity can be achieved even if relatively high power must be delivered. Fig. 7.8 shows the measured frequency response of the TX pre-amplifier. The measured iCP is \(-14.6\)dBm, which corresponds to \(+5.8\)dBm oCP.
This translates into more than 3.5mW power delivered to the 50Ω load at compression. A summary of the measured performance is shown in Table 7.5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain [dB]</td>
<td>21.1</td>
</tr>
<tr>
<td>ip3 [dBm]</td>
<td>-</td>
</tr>
<tr>
<td>ipc [dBm]</td>
<td>-14.6</td>
</tr>
<tr>
<td>s11 [dB]</td>
<td>-6.6</td>
</tr>
<tr>
<td>s22 [dB]</td>
<td>-8.5</td>
</tr>
<tr>
<td>Id [mA]</td>
<td>27.2</td>
</tr>
</tbody>
</table>

Table 7.5: Summary of Measured Performance
Chapter 8

Characterization of the Transceiver

The best of the building blocks discussed thus far have been combined in a single chip to realize the complete GSM transceiver. The receiver portion includes the LNA-4, the SE-DBM and the remaining circuits forming the IF and Baseband strip. The transmitter contains the modulator and the pre-amplifier.

A VCO and a buffer have also been included in the chip. They were originally intended to drive the LO port of the RF-mixer but unfortunately, the buffer for the VCO does not work properly at 1GHz. Therefore, to evaluate the receiver characteristics, the chip was repaired by using a focused ion beam to bypass the LO buffer and re-route an external LO signal to the RF-mixer. A chip microphotograph is shown in Fig. 8.1. The LNA, the VCO and the pre-amp have been placed in three different corners to minimize crosstalk. To minimize coupling between sensitive pads and bond-wires such as the LNA-input and LNA-output, AC-ground pads have been placed between them. The LNA output and the RF-mixer input are placed in the same corner but on different sides so that the external RX image-filter can be connected with minimal and distant routing on the PCB to avoid crosstalk. Two external nodes ($I_{b-RX}$ and $I_{b-TX}$) can be used to activate/deactivate the receiver and the transmitter independently so that they can be measured separately.
without mutual interference. To limit the number of pads and therefore the chip area, the same two pads have been used for the input of the IF-LO for the receiver and for the input of the RF-LO for the transmitter. The complete transceiver including pads occupies an area of 2.2 x 2.2 mm².

A photograph of the board used to test the GSM transceiver is shown in Fig. 8.2. The schematic diagram of the complete board can be seen in Appendix B. The GSM-chip is directly bonded onto the PCB without packaging. All the required external components are soldered on the
top plate, while the bottom plate acts as a large ground plane. Care has been taken with the LNA and pre-amp bonding wire length which defines the gain of the two circuits. The LNA and the pre-amp inputs are very sensitive to the size of the associated stray input capacitance. This capacitance is defined by the on-chip pad capacitance in parallel with the on-board capacitance. To reduce the size of the on-board capacitance, a hole is provided in the bottom ground plane of the PCB under these inputs.

Figure 8.2: Test Board Photograph
SMA connectors are used for high-frequency signals. While the final system will use differential signals, the generators and the measurement instruments employed to test the transceiver use single-ended signals. Therefore, the same (unpackaged) op-amps used to implement the Bessel filters are used here to implement on-board single-ended to
differential converters for the TX-base-band inputs and differential to single-ended converters for the RX-base-band outputs. The two circuits are shown on the bottom left (TX-BB-Input) and the bottom right (RX-BB-Output) of Fig. 8.2, respectively. As shown in the figure, the biggest components are the duplexer and the IF-filter, while the image filter (RX-Filter) and the TX-Filter are quite small. The receive path can be configured to test just the RF front-end (LNA and mixer with filters) or the complete receiver. The transmitter can be configured to test just the modulator or the complete transmit chain (without PA).

The system has been tested using the nominal 2.5V power supply. Baseband and RF GMSK signals have been generated using a R&S SMHU signal generator. The required external LO's are provided by Marconi 2042 low noise signal generators. Spectrum analysis and noise figure measurements have been performed using a R&S FSEB30, while to test the complete system, the a HP 89441A vector signal analyzer has been used.

The S11 measurement in RX-mode, referred to the antenna input, is shown in Fig. 8.3. In the whole GSM receive band (925-960MHz), the S11 is below -9dB, which guarantees sufficient matching to connect the 50Ω antenna.
The measurement of gain and NF for two different front-ends with duplexer, LNA, image-reject filter and SE-DBM is shown in Fig. 8.4. The shape of the frequency response in this measurement is determined by the matching network, used at the IF frequency to transform the 330Ω output impedance to the 50Ω impedance required by the noise figure meter, so that the only relevant performance is that measured at 71 MHz. Thanks to the characteristic of the filters used in this measurement, which is better than the one used to calculate worst-case performance, the measured NF is below 7 dB in both cases. The measured gain of about 10 dB, accounting for the 9 dB attenuation of the output matching network, is also in line with expectations.

To test the blocking performance, a −99 dBm input signal at 947 MHz and an out of band blocking signal have been provided to the antenna input. The blocking signal has been swept between 200−915 MHz and 970 MHz−2 GHz to search for the worst blocking performance. The worst-case conditions were found at 915 MHz. The blocking performance
In the graphs of Fig. 8.6, the measured gain, linearity, noise figure as well as current consumption for each block in the receiver is reported against the planned values. A comfortable margin of 6—9dB has been achieved in the compression point as well as in the intercept point measurement for all blocks in the receiver. Due to the unoptimized current source in the input stage, a slightly worse NF has been measured with regard to the projected results for the RF-mixer. The increased current consumption in the LNA is compensated by the lower current requirement in the mixer and the IF-strip.

The EVM measurement for the complete receiver is shown in Fig. 8.7 for a -75dBm input signal. The achieved S/N ratio is around 20—25dB and is limited by a rather strong interferer (probably a GSM control channel). This interferer could not be suppressed during the measurements and its effect is visible in the sinusoidal shape of the detected phase error. Without this interferer a sensitivity around 100—105dBm
can be therefore expected. Unfortunately an exhaustive sensitivity measurement was not possible due to the limited synchronization capability of the vector analyzer at low input signal levels.

In TX-mode the transceiver has been tested without the PA so that the transmit chain consists of modulator, TX-filter, pre-amp and duplexer. The GMSK modulated output is almost identical to that of the modulator as shown in Fig. 7.4. To show the wide-band noise characteristic, various points have been measured and are displayed in the log-log graph of Fig. 8.8. Curve (a) shows the measurement at the modulator output, before the TX-filter. For offset frequencies <5MHz, the modulator noise is clearly within the prescribed specifications while above 5MHz the measurement is limited by the noise floor of the spectrum analyzer at \(-112\text{dBc/Hz}\). To overcome the limited dynamic of the measurement instrument, the wide-band noise characteristic of the complete transmitter in the GSM receive band has been tested by inserting a notch filter to reduce the output signal power in the transmit band. The noise floor as measured is shown by curve (b). The value is \(-180\text{dBc/Hz}\) and is still limited by the instrument noise suggesting that even with the distortion introduced by a class-C PA, wide-band noise is within specs.

**Figure 8.8:** Transmitter Wideband Noise Characteristic
The EVM measurement in TX-mode for a GMSK input signal is shown in Fig. 8.9. The average RMS transmitter phase error is about 1.6°, while the peak error is less than 3°.

<table>
<thead>
<tr>
<th>RX-mode</th>
<th>Gain</th>
<th>NF(50Ω)</th>
<th>iCP</th>
<th>iIP3</th>
<th>Blocking</th>
<th>Gain Step Accuracy</th>
<th>USSR</th>
<th>Current Cons.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>101dB</td>
<td>8.1dB SSB</td>
<td>-16dBm</td>
<td>-4dBm</td>
<td>+6dBm @915MHz (w.c.)</td>
<td>0.1 - 0.2dB (Typical)</td>
<td>&gt;43dB</td>
<td>19.5mA @2.5V</td>
</tr>
<tr>
<td>TX-mode</td>
<td>Output power</td>
<td>RMS phase error</td>
<td>Peak phase error</td>
<td>Current Cons.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(without PA)</td>
<td>2mW</td>
<td>&lt;2°</td>
<td>&lt;5°</td>
<td>57mA @2.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 8.1: Summary of Measured GSM Transceiver Performance
In RX-mode the chip consumes 19.5mA from the 2.5V power supply, while 57mA are required in TX-mode. A summary of the measured GSM transceiver performance is shown in Table 8.1.
Chapter 9

Conclusions

In this work we have described a CMOS GSM transceiver that fulfills all type approval requirements and which is competitive to existing bipolar solution in terms of power consumption. All the important aspects required for a successful implementation are described. The relevant system type approval requirements have been described and translated into requirements for the transceiver. It is shown that with a suitable architecture and optimized transceiver planning adapted to the CMOS characteristics, good trade-offs can be found for the individual circuit blocks in terms of required performance as well as for power consumption. Circuit robustness is another fundamental requirement and it has been considered in the design of each block. Where possible the number of external components has been minimized.

The two stage LNA is based on an inductive degenerated input stage and a transimpedance output stage. With just two external components at the input, it achieves input and output matching, 15dB gain and less than 2dB NF. To realize the required linearity, the LNA consumes only 11mA from the 2.5V supply voltage.

Different mixer structures have been studied, all based on the Gilbert mixer. For the final design, a new mixer structure based on the Gilbert micromixer has been developed. This new mixer provides a 50Ω single-ended input, low power consumption and the same performance (in terms of conversion gain and linearity) as a double balanced mixer im-
plementation while sacrificing 3dB of noise performance.

The 71MHz IF-amplifier combines gains up to 60dB, high accuracy in the programmable 2dB steps, high linearity, as well as low NF and low power consumption. Furthermore, due to the $g_{mi}/g_{mo}$ gain principle, the IF-amplifier gain is insensitive to absolute parameter variations. Thanks to the differential implementation and the careful layout, the amplifier is perfectly stable at maximum gain.

For the demodulator, the digital divider approach in the phase shifter permits the generation of accurate quadrature LO signals resulting in excellent I/Q separation. The required linearity in the down-conversion mixers is achieved using resistive degeneration in the input stage and a transimpedance output stage.

The lowpass filters are constructed using an active-RC structure for optimum linearity and noise performance. To minimize the number of required op-amps, a Sallen & Key structure has been used. To achieve the required output linearity, rail-to-rail output op-amps have been implemented.

On the transmitter side, to realize the required symbol phase accuracy, a trade-off has been found between up-converting mixer linearity and phase shifter accuracy in the modulator. Thanks to the high linearity of the up-converting mixers based on a feedback input structure, the phase shifter accuracy requirements are somewhat relaxed, so that an RC-CR approach is sufficient to achieve the required overall performance.

The Class-A pre-amplifier is based on a similar structure as that used in the LNA with a modified output stage to achieve the required linearity. The main figures of merit are good input and output matching, 21dB gain and 2mW output power.

The complete GSM transceiver has been characterized. The prototype satisfies all planned requirements suggesting that a complete system will satisfy GSM type approval in receive as well as in transmit mode. The transceiver consumes 19.5mA in receive and 57mA in transmit mode. Although these values do not include the current required in the synthesizer, even adding 20% overhead to account for this, the design is competitive with the best implementations using the most advanced bipolar technologies [38, 39].
Since currently, all commercial GSM transceivers are bipolar, the major question concerns whether pure-CMOS transceivers will ever come to the market in the near future. This is surely a difficult answer. One trend indicates that RF-CMOS is no longer confined to the university laboratories. Major companies such as Infineon (Siemens) and Philips are also seriously investigating this topic.

On the other hand, since bipolar technologies will always stay one step in front of CMOS in terms of performance, a CMOS implementation is interesting only if the process is less expensive or if the complete system, including the base-band processors, can be integrated on the same chip. One example of product based on a system on a chip, intended for a low spec cordless phone has been recently presented [40]. For applications with higher specs such as GSM, much work must still be done before a similar implementation is possible.

It is my opinion that deep submicron CMOS implementations will replace bipolar solutions in the near future for low spec applications as well as for consumer applications working up to 3GHz such as GSM/DCS and UMTS. On the other hand, future standards may require even higher frequencies to achieve higher data rates and user capacity. For these future applications, many problems can be expected if a CMOS implementation is envisaged. Indeed, although thanks to scaling the operating frequency may not pose a problem in itself, scaling will inevitably result in other problems. For instance, scaled technologies require a lower supply voltage, e.g. around 1.5V for 0.13\(\mu\)m CMOS. As a consequence, due to the limited overdrive and reduced headroom, linearity and compression will become major issues. New circuit techniques (e.g. parallel in place of stacked) will be further developed and used. Leakage currents and substrate coupling will also became increasingly important, adding another level of difficulty to the design process.

Although the transceiver in a digital wireless application occupies just a fraction of the total required silicon area, it will continue to be the most critical part in product development. With the current trend of introducing new applications, new standards in addition to the pressure of using cheap technologies, I believe that CMOS-RF designers face a very challenging but also very bright future.
Seite Leer / Blank leaf
Bibliography

[1] Nokia 6150 handset, SLIM Battery BLS-2H 1000mAh LI-Ion.


[16] Lucent Technologies Sceptre Chipset (CSP1088).


[18] Datasheets Power Amplifiers: *Philips BGY204, Hitachi PF0145; Motorola MIM2908*.


[41] Datasheet: IF-Filter Murata SAFC71.0MC50T.
Appendix A

Receiver Planning

In Fig. A.1 a summary of the values used to calculate the overall noise figure referred to the input is shown.

In Fig. A.2 and Fig. A.3, the required iCP for each block in the receiver is calculated. The strength of all blocking signals defined in the type approval specification is computed at each point in the receiver chain, the worst case value is chosen, and the required iCP is calculated adding 3dB margin. For the external filters the worst case attenuation has been chosen. For the integrated filters the attenuation has been calculated assuming a 20% higher cut-off frequency.

The computation of the required iIP3 for each block in the receiver is shown in Fig. A.4. Since each block adds its own component to the total intermodulation signal, a margin of 6dB has been added in the planning. This means that each resulting intermodulating component is at least 12dB smaller than the limit and the sum of all of them is still well in specification. Since the IF-filter attenuates the interferers, the IP3 at the input of the IF-amp must be computed using the same method used to compute the overall iIP3.
Figure A.1: Noise Figure Calculation
## Blocking Signals (worst case)

<table>
<thead>
<tr>
<th>Plan</th>
<th>iCP (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>980M</td>
<td>0</td>
</tr>
<tr>
<td>3M</td>
<td>-23</td>
</tr>
<tr>
<td>1.6M</td>
<td>-33</td>
</tr>
<tr>
<td>600k</td>
<td>-43</td>
</tr>
<tr>
<td>600k</td>
<td>-99</td>
</tr>
<tr>
<td>600k</td>
<td>-43</td>
</tr>
<tr>
<td>1.6M</td>
<td>-33</td>
</tr>
<tr>
<td>3M</td>
<td>-23</td>
</tr>
<tr>
<td>915M</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Gain (dB)</th>
<th>.915M (dBm)</th>
<th>3M (dBm)</th>
<th>1.6M (dBm)</th>
<th>600k (dBm)</th>
<th>fo (dBm)</th>
<th>600k (dBm)</th>
<th>1.6M (dBm)</th>
<th>3M (dBm)</th>
<th>980M (dBm)</th>
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</thead>
<tbody>
<tr>
<td>Duplexer</td>
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<td>-28</td>
<td>-26.2</td>
<td>-36.2</td>
<td>-46.2</td>
<td>-102.2</td>
<td>-46.2</td>
<td>-36.2</td>
<td>-26.2</td>
</tr>
<tr>
<td>Mixer</td>
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<td>-61</td>
<td>-71</td>
<td>-66</td>
<td>-87</td>
<td>-66</td>
<td>-61</td>
<td>-61</td>
<td>-61</td>
</tr>
<tr>
<td>Ch. F.(B4568)</td>
<td>-6</td>
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<td>-71</td>
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<td>Demodulator</td>
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<td>-7</td>
<td>-12</td>
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<td>-1</td>
<td>-2</td>
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<td>-2</td>
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<tr>
<td>4.LPF (150kHz)</td>
<td>16</td>
<td>-44</td>
<td>-3</td>
<td>-44</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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</table>

**Figure A.2: Blocking Signals**

- Duplexer: out-of-band attenuation ≥ 28dB
- Image F.: out-of-band attenuation ≥ 30dB
- B4568: att. @ 600kHz ≥ 41dB
  - att. @ 1.6MHz ≥ 46dB
- Demod.: entails 1st Order LPF, cut-off freq = 500kHz ⇒ calculate with 600kHz (20% tolerance)
- 4.LPF: cut-off freq = 150kHz ⇒ calculate with 180kHz (20% tolerance)
Adjacent Channel Signals (worst case)

<table>
<thead>
<tr>
<th>Component</th>
<th>Gain (dB)</th>
<th>fo (dBm)</th>
<th>200k (dBm)</th>
<th>400k (dBm)</th>
<th>Plan iCP (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>-3.2</td>
<td>-85</td>
<td>-76</td>
<td>-44</td>
<td>-44</td>
</tr>
<tr>
<td>LNA (15dB)</td>
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<td>-73.2</td>
<td>-64.2</td>
<td>-32.2</td>
<td>-29</td>
</tr>
<tr>
<td>Image F.</td>
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<td>-68</td>
<td>-36</td>
<td>-33</td>
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<tr>
<td>Mixer</td>
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<td>-67</td>
<td>-58</td>
<td>-26</td>
<td>-23</td>
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<tr>
<td>Ch. F. (B4568)</td>
<td>-6</td>
<td>-73</td>
<td>-67</td>
<td>-52</td>
<td>-49</td>
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<tr>
<td>IF-Amp</td>
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<td>-35</td>
<td>-29</td>
<td>-14</td>
<td>-13</td>
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<td>Demodulator</td>
<td>16</td>
<td>-19</td>
<td>-13</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>4.LPF (150kHz)</td>
<td>16</td>
<td>-3</td>
<td>-11</td>
<td>-14</td>
<td>-1</td>
</tr>
</tbody>
</table>

Figure A.3: Adjacent Channel Signals

B4568:  
- att. @ 200kHz ≥ 9dB  
- att. @ 400kHz ≥ 26dB

Demod.:  
- entails 1st Order LPF, cut-off freq = 500kHz ⇒ calculate with 600kHz (20% tolerance)

4.LPF:  
- cut-off freq = 150kHz ⇒ calculate with 180kHz (20% tolerance)
**Figure A.4: Intermodule Signals**

### Intermodule Signals (IP3)

![Diagram of intermodulation signals](image)

- **RF Input signals**
  - ref. -99dBm
  - interm. -49dBm (2x = -46dBm) at 800,1600kHz
  - \( x + 10 = \frac{1}{3}(x - 53) \)
  - \( x = -84.5 \)
  - \( \text{IP3} = -14.5 \text{dBm} \)

- **IF Input signals**
  - ref. -87dBm (12dB gain)
  - interm. 800kHz, -72dBm -> -69dBm
  - \( x + 10 \geq \frac{1}{3}(x - (87-69)) \)
  - \( x = -32 \)
  - \( \text{IP3} = -55 \text{dBm} \)

<table>
<thead>
<tr>
<th>Device</th>
<th>Gain (dB)</th>
<th>IF3 (dBm)</th>
<th>Plan IP3 (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duplexer</td>
<td>-3.2</td>
<td>-14.5</td>
<td>-12</td>
</tr>
<tr>
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<td>-12</td>
</tr>
<tr>
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<td>-2.7</td>
<td>+3</td>
</tr>
<tr>
<td>Mixer</td>
<td>10</td>
<td>-6.5</td>
<td>-1</td>
</tr>
<tr>
<td>Ch. F.(B4568)</td>
<td>-6</td>
<td>+3.5</td>
<td>+9</td>
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<tr>
<td>IF-Amp</td>
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<td>16</td>
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<td>-5</td>
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<tr>
<td>4-LPF (150kHz)</td>
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Appendix B

Test Board Schematic Diagram

The schematic diagram of the board used to test the complete transceiver is shown in Fig. B.1.

In receive mode Ib – TX must be shorted to Vdd. The gain can be programmed by signals c̄n (LNA), En1 – 3 and Code1 – 4 (IF-amp). To characterize the front-end, connection b) must be shorted and the component values labeled with b) must be used. A single-ended output has been used for the mixer. To characterize the complete receiver, connection a) must be shorted and the respective component values must be used. Since the planned IF-filter was not available, another filter with the same characteristics, but 910Ω input impedance has been used. The component values are therefore different from the planned one and a matching network is also required between the IF-filter and the IF-amp.

In transmit mode Ib – RX must be shorted to Vdd. To characterize the modulator alone, connection c) must be shorted while to characterize the complete transmitter, connections d) must be shorted. To build the complete chain, a PA can be connected between output To – PA and input TX – Out.
Figure B.1: Test Board Schematic Diagram
# Curriculum vitae

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Born July 28, 1969 in Bellinzona  
Citizen of Bissone, Canton Ticino

<table>
<thead>
<tr>
<th>Time</th>
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<tr>
<td>Sept. 1984 - June 1988</td>
<td>Secondary School (Liceo) of Canton Ticino, Lugano</td>
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<tr>
<td>June 1988</td>
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<tr>
<td>Oct. 1988 - May 1993</td>
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<tr>
<td>May 1993</td>
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List of publications

Conference papers


Journal papers


