Doctoral Thesis

Realization of complex microsystems using custom microelectronics and standard components

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Publication Date:
2000

Permanent Link:
https://doi.org/10.3929/ethz-a-003912273

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Realization of Complex Microsystems using Custom Microelectronics and Standard Components

A dissertation submitted to the
SWISS FEDERAL INSTITUTE OF TECHNOLOGY
ZURICH

for the degree of
Doctor of Technical Sciences

presented by
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2000
Acknowledgments

I would like to thank my advisor, Prof. W. Fichtner, for his confidence in me and my work and for providing an excellent working environment at the Integrated Systems Laboratory (IIS) without whom this work would not have been possible.

I am grateful to Prof. P. Niederer from the Institute of Biomedical Engineering (IBT) for co-examining this thesis and for giving me the opportunity to be part of the endoscopic imaging (EIM) team.

My special thanks go to Norbert Felber for his encouragement and support during the work, for contributing many valuable ideas, as well as for constructive proofreading and commenting on my thesis. He found always time and was interested to discuss signal processing, test and measurement topics, and offered competent advice. Most of my knowledge of digital signal processing and real-world measurement techniques I owe to him.

This work would not have been possible without the collaboration with the IBT. Especially I want to thank Yves Lehareinger, Jürg Häfliger and Patrick Blessing for the fruitful discussions and their contributions.

I would like to thank Hubert Kaeslin and his members of the Microelectronic Design Center for their help in running the CAD tools and the support throughout my ASIC designs.

I was always supported by the whole staff of IIS. Special thanks go to Hanspeter Mathys and Hansjörg Gisler who always helped me in the laboratory and maintained the installations. I want to thank all the secretaries for handling the administrative work. I also want to thank Christoph Wicki and his crew for the excellent computer and network facilities and for always lis-
I would also like to thank all my colleagues at the IIS: Jürgen Hertle, Thomas Burger and Francesco Piazza for the introduction and advise on analog IC design and test; Matthias Brändli and Robert Reutemann for their support during my designs; Tom Heynemann, Andreas Stricker, Reto Zimmermann, Oliver Humbel and Tobias Wikström for their moral and technical support; Manfred Stadler and Thomas Röwer for the personal financial investment consulting; and all others I didn’t mention so far.

Finally, I would like to thank my parents who always supported me in every respect, as well as my sister and relatives.

This work was supported by the Swiss Priority Program MINAST (Micro and Nano System Technology).
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Abstract

In this thesis, the concept, design and realization of a complex microsystem with custom electronics and standard components is described taking a digital high-resolution camera system as example. Applications of this microsystem are in the fields of machine vision or biomedicine where the integration of the camera head into the hand-piece of an endoscope is required. To satisfy the ergonomic requirements of such an instrument, small camera head dimensions are imperative. This requirement can only be fulfilled with a single CCD sensor with color filter array (CFA). Nonetheless color fidelity and resolution should approximate 3-CCD camera quality.

In addition to the higher resolution of 1024x1024 pixels the main improvement over state-of-the-art miniaturized standard video cameras is the integration of a programmable pulse generator with a resolution of 500ps, and a high-speed 400Mbit/s data and control link into one ASIC. Alternative camera head design concepts are presented and compared in this work.

The reconstruction of the RGB image from the CCD with Bayer CFA requires an extremely high computation effort if reasonable frame rates and artifact-free interpolation quality are to be achieved. These tasks are performed in the back-end with a real-time image processor ASIC. Pixelwise black-current and white-gain balancing, color space transformation, focus criterion calculation, and standard video scan conversion for documentation and storage in real-time are additional highlights of this chip.
Zusammenfassung


1 Introduction

1.1 Motivation

The miniaturization of technical components and systems will always play an important role in scientific and industrial applications. Increased functionality has to be built in smaller, lighter and more compact units, and already miniaturized systems get more and more complex. A miniaturized system is often called a microsystem and contains different parts whereas at least a sensor and an actuator are present.

An example of a complex microsystem is a miniaturized digital camera system. There are various fields where miniaturized cameras are needed, e.g. in machine vision or biomedicine.

In this thesis, problems occurring during the design of complex microsystems are discussed and solutions are presented for a miniaturized digital cam-
era system. This camera system was developed for an Endoscopic IMaging system and is referenced as EIM camera system throughout this work.

Complex Microsystems such as the EIM camera system often combine different more or less excluding peculiarities such as:

- stringent space requirements
- high computation power
- low power dissipation
- parts with higher voltages (e.g. 20V signals)
- high-speed data interconnections
- noise sensitive analog parts
- cost

Various solutions with standard products, application specific integrated circuits (ASIC) and the combinations of both worlds were examined throughout this thesis. Furthermore system partitioning contemplations and different clocking strategies are presented. The blocks of the final realized EIM camera system are described in detail at the end of the related chapters.

1.2 Structure of Thesis

As starting point, examples of today's video and still camera systems are presented in chapter 2. These camera systems are compared using attributes such as color fidelity, size, resolution and frame rate.

Chapter 3 introduces the EIM camera system developed during this work. After a general system overview, some consideration aspects for choosing an image sensor (pick-up device) are discussed and the specification of the camera system is presented. According to this specification, the camera system is partitioned into a front-end part and a processing back-end.

In chapter 4, different solutions for a front-end design are compared, and the final EIM camera head is presented.
The control and data link between the front-end and the back-end of the EIM camera system is discussed in chapter 5. Clocking strategies and interface standards are of special interest in this chapter.

Chapter 6 explains the image processing part in the back-end of the EIM camera system. Various color interpolation algorithms are introduced, and a special image processor ASIC is presented.

Finally, the main results of the thesis are summarized and conclusions are drawn in chapter 7.
Seite Leer / Blank leaf
Examples of Digital Camera Systems

Today, video and still camera systems are available for a wide range of applications. They can all be classified with the following terms: color fidelity, size, resolution and frame rate. When cameras are especially good at one of these criteria, they lack in at least one of the others. If a camera is very small and has a high frame rate at a reasonable resolution, it either has a poor color fidelity or is black and white (b/w). A camera with a high resolution and a good color fidelity typically has a very low frame rate (still cameras) or it is too bulky.

As can be seen by the previous examples, these criteria are often correlated to each other. Figure 2.1 compares the color fidelity to the size of a video camera system (for a constant frame rate) and figure 2.2 tries to show the correlation between color and frame rate for the case of a single image sensor.
**Examples of Digital Camera Systems**

**Figure 2.1:** Color fidelity versus size at constant frame rate

**Figure 2.2:** Color fidelity versus frame rate for single image sensor cameras
Three different categories of state-of-the-art camera systems are compared in the following sections: 1Megapixel motion cameras, standard television cameras and digital still cameras.

Unfortunately, each manufacturer specifies his products in a different way. Either he indicates only the outstanding features of his product or the given data is measured under unknown conditions. For this reason, the costumer can not compare a camera system from one manufacturer to a system from another one without taking measurements on both systems by his own or reading test reports in dedicated magazines. This is also the reason why some data is missing in the following tables 2.1 to 2.3.

### 2.1 1Megapixel Motion Picture Camera Systems

Table 2.1 lists three digital motion cameras with one 1-million-pixel CCD sensor as image pick-up device. The A113C from BASLER [Dat98a] is a typical 1-CCD color camera with a color filter array (CFA) to capture RGB images. It consists of a small camera head which delivers digital pixel information to a personal computer (PC), where the color images are reconstructed. Due to the lack of computation performance, only 11.75 frames/s can be processed in real-time.

<table>
<thead>
<tr>
<th>Camera Type</th>
<th>Manufacturer</th>
<th>Resolution</th>
<th>Type</th>
<th># of Sensors</th>
<th>Color or B/W</th>
<th>Frames/s</th>
<th>Bit/Pixel</th>
<th>Readout Channels</th>
<th>Pixelclock [MHz]</th>
<th>Camera(head) Size [mm³]</th>
<th>Weight [g]</th>
<th>Back-end</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BASLER</td>
<td>1300x1030</td>
<td>Motion</td>
<td>1</td>
<td>CFA</td>
<td>11.75</td>
<td>8</td>
<td>1</td>
<td>25 / 10</td>
<td>45x62x62</td>
<td>320</td>
<td>PC</td>
</tr>
<tr>
<td></td>
<td>DALSA</td>
<td>1024x1024</td>
<td>Motion</td>
<td>1</td>
<td>B/W</td>
<td>40 / 8</td>
<td>8 / 12</td>
<td>2 / 1</td>
<td></td>
<td>89x89x105</td>
<td></td>
<td>PC?</td>
</tr>
<tr>
<td></td>
<td>KODAK</td>
<td>1008x1018</td>
<td>Motion</td>
<td>1</td>
<td>B/W</td>
<td>15 / 30</td>
<td>10 / 8</td>
<td>4</td>
<td>? / 20</td>
<td></td>
<td></td>
<td>stand alone?</td>
</tr>
</tbody>
</table>

Table 2.1: State-of-the-art 1Megapixel camera systems
The most important features of the CA-D7 from DALSA [Date] are the quite small camera head, and the capability to deliver 40 black & white (B/W) frames/s.

The last example of 1Megapixel motion cameras is the ES 1.0/10 Bit from KODAK [Dat]. It is a stand-alone B/W camera with 8bit per pixel at 30 frames.

### 2.2 Standard Television Camera Systems

Most available motion cameras provide standard television resolution and frame rates. They are built for a wide range of applications, e.g. low-cost consumer video recording, expensive professional imaging, surveillance, machine vision, biomedicine, and many more. A comparison of a HDTV studio camera and a NTSC television camera is presented in table 2.2.

<table>
<thead>
<tr>
<th>Camera Type</th>
<th>AK-HC830</th>
<th>GP-US522</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
<td>PANASONIC</td>
<td>PANASONIC</td>
</tr>
<tr>
<td>Resolution</td>
<td>1920x1080</td>
<td>768x494</td>
</tr>
<tr>
<td>Type</td>
<td>Motion</td>
<td>Motion</td>
</tr>
<tr>
<td>Standard</td>
<td>HDTV</td>
<td>NTSC</td>
</tr>
<tr>
<td># of Sensors</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Color or B/W</td>
<td>Color</td>
<td>Color</td>
</tr>
<tr>
<td>Frames/s</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Bit/Pixel</td>
<td>10</td>
<td>analog</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>54dB</td>
<td>62dB</td>
</tr>
<tr>
<td>Pixelclock [MHz]</td>
<td>74</td>
<td></td>
</tr>
<tr>
<td>Camera(head) Size [mm³]</td>
<td>34x44x52</td>
<td>206x44x250mm³</td>
</tr>
<tr>
<td>Weight [g]</td>
<td>5800 (All)</td>
<td>110 (Head)</td>
</tr>
<tr>
<td>Back-end</td>
<td>stand alone</td>
<td>1700g</td>
</tr>
</tbody>
</table>

Table 2.2: State-of-the-art camera systems for television standards

The AK-HC830 from PANASONIC [Data] is a typical portable HDTV camera using 3 separate CCD sensors each containing 2 million pixels. Its sole application is professional video.
The model GP-U5522 [Date] from PANASONIC is a standard (NTSC) video camera with 3 CCD sensors. This camera is partitioned into a small camera head and a back-end for the image processing. It is applied where stringent space requirements prohibit the use of normal video cameras.

### 2.3 Digital Still Camera Systems

Due to technological improvements and competition between the different manufacturers, digital still cameras have become affordable. Typical examples are compared in table 2.3.

<table>
<thead>
<tr>
<th>Camera Type</th>
<th>DCS 560</th>
<th>COOLPIX700</th>
<th>S 1 Pro</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
<td>KODAK</td>
<td>NIKON</td>
<td>LEICA</td>
</tr>
<tr>
<td>Resolution</td>
<td>3072x2048</td>
<td>1600x1200</td>
<td>5140x5140</td>
</tr>
<tr>
<td>Type</td>
<td>Still</td>
<td>Still</td>
<td>Scanner</td>
</tr>
<tr>
<td># of Sensors</td>
<td>1</td>
<td>1</td>
<td>3?</td>
</tr>
<tr>
<td>Color or B/W</td>
<td>Color</td>
<td>Color</td>
<td>Color</td>
</tr>
<tr>
<td>Frames/s</td>
<td>1/7</td>
<td>1.5</td>
<td>1/185</td>
</tr>
<tr>
<td>Bit/Pixel</td>
<td>36</td>
<td>24</td>
<td>48</td>
</tr>
<tr>
<td>Camera Size [mm³]</td>
<td>174x161x92</td>
<td>114x67x38</td>
<td></td>
</tr>
<tr>
<td>Weight [g]</td>
<td>1650</td>
<td>270</td>
<td></td>
</tr>
<tr>
<td>Back-end</td>
<td>stand alone</td>
<td>stand alone</td>
<td>PC</td>
</tr>
</tbody>
</table>

**Table 2.3: State-of-the-art digital still camera systems**

The DCS 500 from KODAK [Date] is a professional stand-alone camera with 6 million pixels. The heavy weight and the 7s needed for each frame are its main drawbacks.

As an example of todays digital still cameras for the consumer market, the COOLPIX700 from NIKON [Datb] is listed. Its resolution and speed is sufficient for most home applications.

For the professional photographer, the S 1 Pro scanner camera from LEICA [Datg] offers highest resolution but it can not be operated without computer, where the image processing is performed.
This chapter gives an overview of the EIM camera system developed during this work. Its main purpose is in the field of endoscopic and machine vision applications. After some sensor considerations the specification and the system partitioning is explained in detail.

As shown in chapter 2, a camera system can be characterized using color fidelity, size, resolution, frame speed and special features. Unfortunately, all these criteria are strongly dependent on each other. For the EIM camera, the frame speed was specified as 30 frames/s and the resolution as 1024x1024 pixels. For the other criteria, the best possible solution had to be chosen. Table 3.1 summarizes the basic specification of the EIM camera system. A secondary standard video output for image recording as well as support for autofocus and illumination control was also demanded.

Positioning these basic specifications in figure 2.1 of the previous chapter, the solution would be a true color camera system containing only one image
<table>
<thead>
<tr>
<th>Criterion</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame Speed</td>
<td>30 frames/s</td>
</tr>
<tr>
<td>Resolution</td>
<td>1024x1024 pixels</td>
</tr>
<tr>
<td>Size</td>
<td>as small as possible</td>
</tr>
<tr>
<td>Color Fidelity</td>
<td>as high as possible</td>
</tr>
<tr>
<td>Special Features</td>
<td>NTSC or PAL video output</td>
</tr>
<tr>
<td></td>
<td>autofocus and illumination control</td>
</tr>
</tbody>
</table>

Table 3.1: Basic specifications of the EIM camera system

sensor for minimal size. This is depicted in figure 3.1. Since minimal size is achieved with one image pick-up device, the specifications can also be applied to figure 2.2 resulting in figure 3.2.

![Color fidelity versus size at 30 frames/s for EIM camera](image)

Figure 3.1: Color fidelity versus size at 30 frames/s for EIM camera
3.1 Basic Camera System

A basic camera system consists of an optical part containing the lenses and the illumination, the electronic part, and a display and/or storage part. A general block diagram of the EIM camera system is shown in figure 3.3. In this work, only the electronic part will be discussed.

Figure 3.3: Block diagram of the camera system
The driver and control unit generates the signals required by the image sensor and the analog signal processor (ASP). The raw image data at the output of the ASP is further processed by the digital signal processing unit which converts the images for display and storage purposes. The detailed functionality of the blocks depend on the image sensors chosen and will be described later in this section in more detail. Aside the high-resolution video output, a low-resolution standard video output is provided to archive images on tape. Additional functionality such as autofocus and illumination control are also supported.

### 3.2 Sensor Considerations

#### 3.2.1 CCD versus CMOS image sensors

The image sensor type is one of the first decisions for the design of a camera system. There are the classic CCD sensors on one side and the advancing CMOS sensors on the other. Both technologies offer a wide range of sensor types. The architectures of CCD and CMOS sensors are described in detail in [The95].

Image sensors can be characterized by the following criteria: dynamic range, signal-to-noise ratio, analog or digital output, pixel arrangement readout sequence, how pixels are accessed and many more. A general comparison between CCD and CMOS sensors is shown in table 3.2.

The main advantage of the CMOS sensors is their normal CMOS fabrication process which is easy to produce, cheap, and allows to integrate analog-to-digital converters on-chip. They also do not need any special driver stages, which saves a lot of power and leads to less noise and less need for cooling, and they are addressed the same way as a SRAM by random pixel access. Due to the internal amplification of each pixels in a CMOS sensor, the optical-sensitivity characteristics of these sensors are outstanding. Nevertheless, each standard CMOS sensor has at least one of these main problems: nonuniform spectral response (from pixel to pixel), nonuniform dark current, fixed-pattern noise, or reset noise.


<table>
<thead>
<tr>
<th>Criterion</th>
<th>CCD</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>special process</td>
<td>enhanced standard process</td>
</tr>
<tr>
<td>Production</td>
<td>expensive</td>
<td>cheap</td>
</tr>
<tr>
<td>Cost (&gt;1M pixel)</td>
<td>1'000$ to 22'000$</td>
<td>50$ to 9'000$</td>
</tr>
<tr>
<td>Power required during operation</td>
<td>50x a.u. e.g. 2W</td>
<td>1x a.u. e.g. 80mW</td>
</tr>
<tr>
<td>Control Interface</td>
<td>none</td>
<td>row &amp; column selection</td>
</tr>
<tr>
<td>Pixel Readout Format</td>
<td>fixed sequential</td>
<td>random parallel</td>
</tr>
<tr>
<td>Integration Time Start/Stop</td>
<td>for all pixels at beginning of new frame</td>
<td>for each pixel when it is accessed</td>
</tr>
<tr>
<td>Output</td>
<td>analog</td>
<td>digital (some analog)</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>linear 54dB - 62dB</td>
<td>linear and logarithmic 70dB - 120dB</td>
</tr>
<tr>
<td>SNR</td>
<td>very good e.g. 10e-</td>
<td>quite good - poor e.g. 50e-</td>
</tr>
</tbody>
</table>

Table 3.2: CCD image sensors vs. CMOS image sensors in general

The CCD sensors on the other side have a better signal-to-noise ratio than the CMOS sensors. Due to the common output amplifier, the fixed-pattern noise as well as the other nonuniform effects are lower too. The power consumption of a CCD camera system is dominated by the power needed to drive the sensor (see section 4.2.1).

The (charge) information of each pixel can easily be retained in a CCD sensor allowing to store an entire frame on the sensor. This stored frame can be processed while the next frame is being acquired. The advantage of this principle is that the image integration starts and stops at the same time for all pixels even without any electrical or mechanical shutter.

In CMOS sensors, the integration time starts and stops for each pixel individually resulting in a slightly different time offset, which is not desired for high quality motion pictures. Special dummy read-out, reset or shutter sequences make a common integration starting point for all pixels possible. But a mechanical shutter would be needed to stop the integration for all pixels at
The EIM camera system was developed mainly for endoscopic and machine vision applications, where limited space often prevent mechanical shutters. These applications also often suffer from low light levels, which call for a sensor with low noise. Because of important these reasons, a CMOS sensor were discarded for the EIM camera system.

### 3.2.2 One versus Three Image Sensors

Another important decision is the use of one CCD or three CCDs. Professional motion cameras all use three CCDs whereas consumer products and still picture cameras are equipped with a single CCD (1-CCD) sensor. In a 3-CCD camera the red, green and blue information of the image is separated by a chromatic prism and processed by three black and white cameras. Each pixel element of a 1-CCD camera is coated with a color selective filter and the blocked color components are to be reconstructed from the neighborhood by the image processing section. Advantages and disadvantages of the two alternatives are summarized in table 3.3. For exact comparison of resolution and sensitivity the modulation transfer function (MTF) of the different solutions would have to be calculated according to [The95].

<table>
<thead>
<tr>
<th></th>
<th>one CCD</th>
<th>three CCDs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Space requirement</td>
<td>same as b/w camera except for interpolation</td>
<td>3x space of b/w camera except for timing generator</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>same as b/w camera</td>
<td>3x power of b/w camera</td>
</tr>
<tr>
<td>Resolution</td>
<td>same as b/w camera</td>
<td>same as b/w camera</td>
</tr>
<tr>
<td>Green (Luminance)</td>
<td>half of b/w camera</td>
<td>same as b/w camera</td>
</tr>
<tr>
<td>Red, Blue</td>
<td>quarter of b/w camera</td>
<td>same as b/w camera</td>
</tr>
</tbody>
</table>

Table 3.3: 1-CCD vs. 3-CCD camera system

Due to the space and power limitations of the EIM camera, a 1-CCD camera system with RGB Color Filter Array (CFA) was chosen. The drawback is the need for a real-time interpolation unit, and the reduced resolution.
3.2.3 Comparison of CCD Sensor Architectures

There are four main architectures of CCD array image sensors: full-frame, frame-transfer, interline-transfer, and frame-interline-transfer. The full-frame sensor has the simplest concept which is illustrated in figure 3.4. It contains a light sensitive two-dimensional CCD array (photon $\rightarrow$ electron conversion), a horizontal light-protected shift register and an output amplifier which transforms electron charge to voltage.

![Figure 3.4: Architecture of full-frame image sensor](image)

After the exposure time interval, some shutter mechanism interrupts the light path and the sensor is read out according to the following scheme: First, the charge information in the two-dimensional CCD array is vertically shifted down one line. The horizontal shift register, now containing the lowest light-sensitive line, is shifted to the output amplifier which generates a serial pixel stream that is available as voltage levels at the output of the sensor. After the line has been read out, the image is again vertically shifted down one line and the next line is read out. A new image can be acquired after the last line has been read out.

For video applications, it is not desired to wait with the exposure of the next frame until the whole previous frame is read out. Therefore a storage array is provided as temporary memory. This leads to the frame-transfer sensor depicted in figure 3.5.

The charge information of a whole frame is transferred to the storage area.
(light insensitive) by vertically shifting through all lines. After the image is in the storage section, it is read out using the same concept as the full-frame sensor. During the read-out of the storage section, the light sensitive part is acquiring the next image. Often this sensor type is used without mechanical shutter. The exposure during the vertical frame transfer leads to smear. The drawback of this architecture is the large chip area, which is twice the area of the full-frame type.

An alternative method to add a storage area without increasing the chip size is to integrate storage capability into the light-sensitive part. These pixels have the same size as a normal CCD cell and contain a photodiode, and a light insensitive shift register stage. This principle is called interline-transfer and is presented in figure 3.6. The whole image is transferred to the vertical shift registers in one shift cycle. Then, these registers are read out as with the full-frame sensor, while the new frame is exposed to the photo diodes.

The aperture ratio is defined as the light sensitive fraction of the complete pixel area (including the shift register stage). For the interline-transfer sensor...
is is typically 50% leading to half the sensitivity of the frame-transfer sensors. This drawback can be (partly) compensated by adding microlenses on-top of the photodiodes. The already high production costs are even more raised by this complex technology step.

![Architecture of interline-transfer image sensor](image)

**Figure 3.6: Architecture of interline-transfer image sensor**

At a first glance the smear problem seems to be solved, but it is still present with the interline-transfer architecture. Its cause, however, is of different nature and is discussed in [The95] in detail. The only way to minimize smear without mechanical shutter or other light controlling devices is to combine the frame-transfer with the interline-transfer architecture. This results in the frame-interline-transfer concept illustrated in 3.7.

First, the image information is immediately transferred to the vertical shift registers from where it is quickly shifted to the storage area. After the complete image is in the storage area, it is read out as in the full-frame concept. The smear level is drastically reduced at the costs of chip size (same as frame-transfer) and aperture ratio (same as interline-transfer).

There is a variety of different implementations of these sensor types, but the main advantages and disadvantages stay the same. Table 3.4 tries to compare the different architectures.

The EIM system specification favored the interline-transfer architecture due to the small chip size. The KAI-1010 (former KAI-1001) from KODAK (see [Dat98c]) was chosen for the EIM camera system (see also [vO97]).
Figure 3.7: Architecture of frame-interline-transfer image sensor

Table 3.4: Comparison of CCD array image sensor types
3.3 Specifications for the EIM camera system

The goal of the EIM system is a camera suitable for biomedical hand-held endoscopy and machine vision applications based on the CCD image sensor KAI1010 from KODAK. The specifications are summarized in table 3.5.

<table>
<thead>
<tr>
<th>Criterion</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensor</td>
<td>1x KAI1010 from KODAK</td>
</tr>
<tr>
<td>Resolution</td>
<td>1024x1024</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>30 frames/s</td>
</tr>
<tr>
<td>Bits/Pixel before digital signal processing</td>
<td>10bit</td>
</tr>
<tr>
<td>Bits/Pixel at high resolution output</td>
<td>24bit RGB</td>
</tr>
<tr>
<td>Total Power dissipation</td>
<td>less than 2.5W (camera head)</td>
</tr>
<tr>
<td>Size</td>
<td>suitable for hand-held applications</td>
</tr>
<tr>
<td>Special Features</td>
<td>• high resolution progressive scan output</td>
</tr>
<tr>
<td></td>
<td>• PAL standard video output</td>
</tr>
<tr>
<td></td>
<td>• support for autofocus control</td>
</tr>
<tr>
<td></td>
<td>• support for illumination control</td>
</tr>
<tr>
<td></td>
<td>• dark current correction</td>
</tr>
<tr>
<td></td>
<td>• white imbalance compensation</td>
</tr>
<tr>
<td></td>
<td>• true-color images with different illumination characteristics</td>
</tr>
</tbody>
</table>

Table 3.5: Specifications for the EIM camera system

Since the main applications requires hand-held operation, the camera, needs to be miniaturized to the minimal reachable size. This forces a partitioning of the system into front-end and back-end. Flexible handling of the hand piece, i.e. the front-end, is required. Therefore the cable to the back-end must be as "flexible" and "light" as possible. A lower number of data and power wires with smaller diameters is advantageous. Furthermore, experiments showed that the power dissipation of the hand-piece is to be limited to 2.5W without forced cooling (see Appendix B).

To achieve a dynamic range corresponding to 10bit with 30frames/s, a CCD sensor temperature is to be limited below 56°C. A tolerance of ±0.7°C at 56°C or ±2°C at 40°C is acceptable if no temperature dependent dark
current compensation is foreseen (see Appendix C).

To maintain the dynamic range over the full image area, a colorwise and a pixelwise correction mode are required. The colorwise correction mode which compensates the different light sensitivity of each color component. The advantage of the pixelwise correction mode is good image quality even with lower grade CCD sensors. Measurements showed that 10 bit gain correction and 6 bit offset correction for each pixel is sufficient (see [vO97]).

To reach 30 frames/s, two lines have to be read out of the sensor and processed simultaneously (double line read-out mode). This results in a (double-)pixel frequency of 20MHz leading to a bandwidth before the digital signal processing of 400Mbit/s, and a continuous bandwidth at the high resolution output of 90MB/s with a peak of 120MB/s.

### 3.4 System Partitioning

The complete camera system that can fulfill the specifications is shown in figure 3.8. The timing generator provides the image sensor, the correlated-double sampling (CDS) stage and the A/D converter with the pulses needed for operation. The driver stage converts the pulses for the image sensor to the corresponding voltage levels and drive strengths. The CDS stage is used to reduce the the reset noise introduced by the CCD output structure. The A/D converter provides the raw digital image data. The pixelwise dark current and white gain compensations are performed in the correction unit. The corrected CCD data gets interpolated to restore the missing two color components of each pixel. To achieve high color fidelity, a color space transformation is necessary. All aforementioned processes work on the two-channel data stream from the CCD sensor. The line serializer rearranges the data as to provide the usual progressive scan image to the high resolution frame grabber output. Aside this main data path the focus and exposure unit calculates the luminance components of the image and evaluates a two-dimensional focus criterion on a sizable window. The scan converter unit derives a standard digital image format to a PAL video encoder for low-cost long-time documentation storage on a video recorder.

The input signals of the CCD sensor need up to 20V swing and peak currents of 2.5A. To save power, reduce system noise and apply precise input signals, the driver stage has to be as close to the image sensor as possible. To
Figure 3.8: Camera system with interconnections
guarantee full bandwidth from the sensor output to the analog signal processing units, the CDS and A/D stages have to be placed as close as possible to the sensor.

The minimal front-end would contain the sensor, the driver stage, and the CDS and A/D stages without the timing generator. With this configuration, however, all seven CCD input signals and the seven signals for the analog signal processing need to be transmitted from the back-end to the camera head. This results in 14 separate wires. In addition, a timing variation of 500ps between some of these signals results in a lower image quality. For these reasons, the pulse generator too should be in the front-end.

To minimize power, space, bandwidth loss and noise in the camera head, all the digital signal processing is performed in the back-end. Therefore the digitized CCD data has to be transmitted to the back-end. To transmit the 400Mbit/s on few wires, special serial transmitters and receivers are needed. The partitioned EIM camera system is shown in figure 3.9.

Figure 3.9: EIM Camera System Architecture
3.5 Comparison of Camera Systems

Table 3.6 lists the sensor dependent features of the EIM camera system together with the 1Megapixel cameras presented in chapter 2. The EIM camera is equipped with the same CCD sensor as the ES 1.0 from KODAK. The dynamic range of the EIM camera system specification is 10bit @ 30frames/s compared to 8bit @ 30frames/s and 10bit @ 15frames/s.

<table>
<thead>
<tr>
<th></th>
<th>Resolution</th>
<th>Frame rate</th>
<th>Dynamic Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>EIM</td>
<td>1008x1018</td>
<td>30Hz</td>
<td>10bit</td>
</tr>
<tr>
<td>BASLER A113C</td>
<td>1300x1030</td>
<td>11.75Hz</td>
<td>8bit</td>
</tr>
<tr>
<td>DALSA CA-D7</td>
<td>1024x1024</td>
<td>40Hz</td>
<td>8bit</td>
</tr>
<tr>
<td>KODAK ES 1.0</td>
<td>1008x1018</td>
<td>30Hz/15Hz</td>
<td>8bit/10bit</td>
</tr>
</tbody>
</table>

Table 3.6: *EIM camera compared to other Megapixel cameras (part 1)*

The main advantage of the EIM camera is its color capability, as shown in table 3.7. The specification requires true-color with one CCD sensor at 30 frames/s. The BASLER camera is the only other camera of chapter 2 with real-time color images, but due to the limited computation power and bandwidth of a PC, only 11.75frames/s can be calculated, and the color fidelity is limited. The EIM camera system therefore requires a powerfull image processing back-end which is capable to process 30frames/s. The required autofocus support and scan conversion are not available in the other camera systems.

<table>
<thead>
<tr>
<th></th>
<th>Color Capability</th>
<th>Image Processing</th>
<th>Display Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>EIM</td>
<td>true-color</td>
<td>Back-end</td>
<td>PC/TV</td>
</tr>
<tr>
<td>BASLER A113C</td>
<td>Yes</td>
<td>PC</td>
<td>PC</td>
</tr>
<tr>
<td>DALSA CA-D7</td>
<td>No</td>
<td>PC</td>
<td>PC</td>
</tr>
<tr>
<td>KODAK ES 1.0</td>
<td>No</td>
<td>-</td>
<td>TV?</td>
</tr>
</tbody>
</table>

Table 3.7: *EIM camera compared to other Megapixel cameras (part 2)*
Seite Leer / Blank leaf
Front-end Design

The driver stage and the pulse generator used in the front-end of the camera system are described in this chapter. The analog signal processing can be performed with standard ICs and will not be described any further.

4.1 Front-end Overview

An overview of the signals used for the CCD camera head is shown in figure 4.1. The camera head uses three external input signals: the parameter link, the trigger input and the main clock. Over the parameter link, the complete camera head can be configured (see section 5) and with the trigger input, single frame or line sequences are started, depending on the configuration. The clocking strategy is described in section 5.1.
The pulse generator delivers the CCD pulses and the pulses for the analog signal processing stages. Some of them are programmable in phase offset and width with a resolution of 500ps. The timing of the CCD signals is shown in figure 4.2.

The transmitter gets the two CCD line data and transmits each of them serially to the back-end. The transmitter is described in section 5.4 in detail.

For correct operation of the CCD sensor, a dedicated driver stage is needed. To achieve the power limit of the EIM camera head, optimizing the driver stage was important. The different architectures and various realizations are elucidated in the following section.
Figure 4.2: Frame and line timing of the CCD image sensor
4.2 CCD Driver Stage Architectures

In order to operate the CCD sensor within its necessary specifications, special driver stages are required which convert the pulse generator signals to the corresponding voltages and drive strengths. After some power estimations, different driver stage principles and realizations are discussed in this section.

Throughout this work, the CCD signals are classified according to their loads and speeds. The first class is the reset signal (10ns pulse width; 20MHz; 5pF load). The second class contains the three horizontal signals (25ns pulse width; 1032 pulses/line; 2*100pF, 1*125pF load). In the last class are the two vertical signals (3µs pulse width; 2 pulses/line; 2*25nF load). The input to output signal correspondence of the driver stage with the CCD loads can be seen in figure 4.3 graphically. Table 4.1 shows the input to output mapping with the voltage level margins.

<table>
<thead>
<tr>
<th>Input</th>
<th>Level</th>
<th>Output</th>
<th>Level</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1H</td>
<td>x</td>
<td>ΦV1</td>
<td>L</td>
<td>-9.5±0.5V</td>
</tr>
<tr>
<td>V1L</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1H</td>
<td>0</td>
<td>ΦV1</td>
<td>M</td>
<td>0.2±0.2V</td>
</tr>
<tr>
<td>V1L</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1H</td>
<td>1</td>
<td>ΦV1</td>
<td>H</td>
<td>9.0±0.5V</td>
</tr>
<tr>
<td>V1L</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V2</td>
<td>0</td>
<td>ΦV2</td>
<td>L</td>
<td>-9.5±0.5V</td>
</tr>
<tr>
<td>V2</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>H1A/B</td>
<td>0</td>
<td>ΦH1A/B</td>
<td>H</td>
<td>3.0±0.5V</td>
</tr>
<tr>
<td>H1A/B</td>
<td>1</td>
<td>ΦH1A/B</td>
<td>L</td>
<td>-7.0±0.5V</td>
</tr>
<tr>
<td>H2</td>
<td>0</td>
<td>ΦH2</td>
<td>H</td>
<td>3.0±0.5V</td>
</tr>
<tr>
<td>H2</td>
<td>1</td>
<td>ΦH2</td>
<td>L</td>
<td>-7.0±0.5V</td>
</tr>
<tr>
<td>RSTP</td>
<td>0</td>
<td>ΦR</td>
<td>L</td>
<td>-6.0±0.5V</td>
</tr>
<tr>
<td>RSTP</td>
<td>1</td>
<td></td>
<td>H</td>
<td>0.0±0.5V</td>
</tr>
</tbody>
</table>

Table 4.1: Input/output signal mapping of the driver stage with voltage level margins
4.2 CCD Driver Stage Architectures

Input CMOS-Level Signals from pulse generator

Output Signals for KAI-1010 CCD Sensor

Horizontal Signals

Vertical Signals

Figure 4.3: Input/output signal correspondence of driver stage
4.2.1 Power Calculations for the CCD Sensor

4.2.1.1 Theoretical Power Consumption

The theoretical average power dissipation in the CCD and the theoretical average current with 30 frames/s for all the signal classes are compared in table 4.2. The detailed power calculations can be found in Appendix D.

<table>
<thead>
<tr>
<th>Signal Classes</th>
<th>Energy per frame</th>
<th>Average Power</th>
<th>Average Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>120µJ</td>
<td>3.6mW</td>
<td>0.6mA</td>
</tr>
<tr>
<td>H</td>
<td>17.18mJ</td>
<td>515mW</td>
<td>51.5mA</td>
</tr>
<tr>
<td>V</td>
<td>4.82mJ</td>
<td>145mW</td>
<td>14.9mA</td>
</tr>
<tr>
<td>Total</td>
<td>22.12mJ</td>
<td>663.6mW</td>
<td>67mA</td>
</tr>
</tbody>
</table>

Table 4.2: Theoretical energy, current and power consumption

4.2.1.2 Power boundaries for KAI1010

Specified and measured load characteristics of a KAI1010 image sensor from KODAK for all signal classes are shown in table 4.3. The measurements indicated that the values of all signals are frequency dependent. Therefore they were measured at the dominant frequencies (main frequency during the active phase) of the signals.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Freq.</th>
<th>C_{Spec}</th>
<th>C_{Load}</th>
<th>R_{Load}</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΦR</td>
<td>20MHz</td>
<td>5pF</td>
<td>4.2pF</td>
<td>4Ω</td>
</tr>
<tr>
<td>ΦH1A</td>
<td>20MHz</td>
<td>100pF</td>
<td>55pF</td>
<td>35Ω</td>
</tr>
<tr>
<td>ΦH1B</td>
<td>20MHz</td>
<td>100pF</td>
<td>50pF</td>
<td>35Ω</td>
</tr>
<tr>
<td>ΦH2</td>
<td>20MHz</td>
<td>125pF</td>
<td>80pF</td>
<td>30Ω</td>
</tr>
<tr>
<td>ΦV1</td>
<td>167kHz</td>
<td>25nF</td>
<td>18.5nF</td>
<td>30Ω</td>
</tr>
<tr>
<td>ΦV2</td>
<td>167kHz</td>
<td>25nF</td>
<td>16.3nF</td>
<td>39Ω</td>
</tr>
</tbody>
</table>

Table 4.3: Specified and measured RC loads of the KAI1010 image sensor at corresponding signal operating frequency
Typically the CCD capacitors are charged / discharged up to a voltage of 99% of a completely charged / discharged capacitor. Therefore, the time of \( t = 5RC \) is used in the following calculations to charge / discharge a capacitor according to (4.1)

\[
V_C = V(1 - e^{-\frac{t}{RC}}) = 99.3\% * V \quad for \quad t = 5RC \quad . \tag{4.1}
\]

This means that e.g. the reset signal with the specified pulse width of 10ns has to be charged in 10ns

\[
t_{\text{Reset}} = 5RRC_R = 10\text{ns} \quad . \tag{4.2}
\]

The total serial resistor (CCD input, driver stage output and wiring) for the reset signal has to be less than 23\( \Omega \). With the given CCD resistor of 4\( \Omega \) and a total resistor of 23\( \Omega \), only 17% of the total reset power is consumed in the CCD sensor itself.

With this assumption however, the CCD signal quality may degrade, because the CCD sensor needs its signals to keep their voltage level for a certain time before applying the next voltage level.

Table 4.4 shows the calculated total resistor and the ratio CCD resistor over total resistor for all the CCD signals. A larger total resistor than specified results in a more slowly charged / discharged capacitor.

<table>
<thead>
<tr>
<th>CCD Signal</th>
<th>Total Resistor</th>
<th>Driver Resistor</th>
<th>Ratio CCD/Tot.</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \Phi R )</td>
<td>23( \Omega )</td>
<td>19( \Omega )</td>
<td>17%</td>
</tr>
<tr>
<td>( \Phi H1A )</td>
<td>100( \Omega )</td>
<td>65( \Omega )</td>
<td>35%</td>
</tr>
<tr>
<td>( \Phi H1B )</td>
<td>90( \Omega )</td>
<td>55( \Omega )</td>
<td>39%</td>
</tr>
<tr>
<td>( \Phi H2 )</td>
<td>62( \Omega )</td>
<td>32( \Omega )</td>
<td>48%</td>
</tr>
<tr>
<td>( \Phi V1 )</td>
<td>32( \Omega )</td>
<td>2( \Omega )</td>
<td>94%</td>
</tr>
<tr>
<td>( \Phi V2 )</td>
<td>36( \Omega )</td>
<td>0( \Omega )</td>
<td>100%</td>
</tr>
</tbody>
</table>

**Table 4.4:** Total resistor, driver resistor and ratio CCD resistor over total resistor for all CCD input signals

The ratio of the CCD resistor over the total resistor equals the ratio of the power dissipated inside the CCD sensor over the total power. Therefore a
larger resistor in the driver stage and wiring reduces the power dissipation of the CCD sensor, which also reduces its temperature.

The calculated average current, the total average power consumption and the average power consumed by the CCD as well as the energy used for a full frame at 30 frames/s are shown in table 4.5.

<table>
<thead>
<tr>
<th>Signal Classes</th>
<th>Energy per frame</th>
<th>Average Power</th>
<th>Average Current</th>
<th>Average Power CCD</th>
<th>Average Power Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>101µJ</td>
<td>3mW</td>
<td>0.5mA</td>
<td>0.5mW</td>
<td>2.5mW</td>
</tr>
<tr>
<td>H</td>
<td>9.78mJ</td>
<td>293mW</td>
<td>29.3mA</td>
<td>122.5mW</td>
<td>170.5mW</td>
</tr>
<tr>
<td>V</td>
<td>3.35mJ</td>
<td>100.6mW</td>
<td>10.4mA</td>
<td>97.4mW</td>
<td>3.2mW</td>
</tr>
<tr>
<td>Total</td>
<td>13.23mJ</td>
<td>396.6mW</td>
<td>40.2mA</td>
<td>220.4mW</td>
<td>176.2mW</td>
</tr>
</tbody>
</table>

Table 4.5: Calculated power budget of the KAI1010 according to measured values of table 4.3

The total average power consumption is about 60% of the maximum specified power consumption in the previous sections. Even with the driver resistors specified in table 4.4, 56% of the power is dissipated by the CCD sensor itself.

4.2.2 Driver Principles

4.2.2.1 DC-coupled solution

Figure 4.4 shows the DC-coupled solution applicable to all signal classes. The driver stages convert the CMOS input signals to the levels needed by the CCD sensor. Since the CCD sensor uses different negative as well as positive voltage levels, two separate supply voltages are required for each signal class. If they are delivered over different wires to the camera head, a total of seven power wires with one common ground for the driver stage would be necessary.

Generating all the voltages out of one positive and one negative supply voltage inside the camera head, only two power wires with one common ground are necessary. Seven voltage regulator circuits are then required inside the camera head. This solution is indicated in figure 4.5 graphically.

For minimal space and power consumption, all the necessary voltages should be delivered to the camera head separately. This reduces the flexibil-
Figure 4.4: \textit{DC-coupled solution}

Figure 4.5: \textit{DC-coupled voltage level generation with two power wires and one return}
ity of the cable tremendously. For maximal cable flexibility, only two voltage levels and one return should be delivered to the camera head. But this results in more space and increases power consumption in the camera head.

These two solutions can be combined in order to get the best out of both. For example a solution with four power wires, one common ground and three voltage regulators is a good trade-off between power consumption, space and flexibility.

The currents needed by all parts of the camera head are blocked by capacitors. These capacitors filter the current peaks. They are charged by voltage regulators in the camera head or over the supply wires from the back end. The cable can be modeled as a resistor which is reduced by increasing the diameter (which reduces flexibility). Larger voltage tolerances allow larger resistors and/or smaller blocking capacitors. For precise voltage levels, however, voltage regulators are smaller than the required blocking capacitors, but they dissipate additional power in the camera head.

### 4.2.2.2 AC-coupled solution

Another driver stage solution is shown in figure 4.6. In the following sections, this is called AC-coupled solution. However, the correct name would be a DC-restoring solution.

![AC-coupled solution](image)

**Figure 4.6: AC-coupled solution**
With AC-coupling only one voltage reference for each signal class is required. However, considerable space is used by the AC-coupling components. The concerns about the supply voltages (wires or regulators) of the DC-coupled solution in section 4.2.2.1 stay the same for the AC-coupled solution.

The minimal number of power wires for the AC-coupled solution is one power wire and one return. The maximum voltage levels needed are four instead of seven with the DC-coupled solution. Figure 4.7 shows the voltage levels needed for AC-coupling graphically.

Figure 4.7: AC-coupled voltage level generation with one main power wire and one return

Comparing this solution with the DC-coupling, the number of power wires or the number of voltage regulator has decreased, but additional space for the AC-coupling components is used.
There is the possibility to combine DC-coupled and AC-coupled solution. An example would be a driver stage with DC-coupling for the vertical signal class and a driver stage with AC-coupling for the horizontal signal class and the reset signal.

### 4.2.3 Charge-Pump Solutions for the Frame Pulse

Since only one 5μs pulse per frame uses almost double the swing of all others, a charge-pump circuit for the frame transfer pulse is feasible with limited effort. The voltage levels for the DC and AC solutions of this variant can be found in figures 4.8(a) and 4.8(b) graphically.

![Figure 4.8: DC- and AC-coupled solutions with charge-pump](image)

The number of voltage reference circuits stays the same but the maximum required voltage range is now 6V resp. 8.5V smaller. Table 4.6 compares the DC with the AC solution. The power dissipation is evaluated using the
calculated current of the KAI1010 in section 4.2.1.2. The DC-coupled solution requires a positive voltage of 5V and a negative voltage of -11.5V. The AC-coupled solution needs one positive supply voltage of 12V only.

![Table 4.6: Total power dissipation of DC- and AC-coupled solutions with charge pump](image)

<table>
<thead>
<tr>
<th>Signal Classes</th>
<th>KAI1010 Current (mA)</th>
<th>Power DC (16.5V)</th>
<th>Power AC (12V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>0.5</td>
<td>8.25mW</td>
<td>6mW</td>
</tr>
<tr>
<td>H</td>
<td>29.3</td>
<td>483.45mW</td>
<td>351.6mW</td>
</tr>
<tr>
<td>V</td>
<td>10.4</td>
<td>171.6mW</td>
<td>124.8mW</td>
</tr>
<tr>
<td>Total</td>
<td>40.2</td>
<td>663.3mW</td>
<td>482.4mW</td>
</tr>
</tbody>
</table>

4.2.4 Driver Stage Implementation Variants

4.2.4.1 Bipolar

Concerning the output structure there are two main implementations for a driver stage: Bipolar and MOSFET. This subsection takes a closer look at the bipolar output structure. Figure 4.9 shows a block diagram of such a bipolar stage. Considering the high currents this output stage has to deliver, a bipolar implementation seems to be the best solution. Bipolar transistors dedicated for high-speed saturated switching at collector currents of 10mA to 100mA and collector-emitter voltages of 15V are desired. MMBT3640/MMBT2369 from National are examples of such devices. The process used for these bipolar transistor is an overlay, double-diffused, gold doped, silicon epitaxial process (e.g. National Process 21/22/65). Since such transistors are only available as discrete components, not in ASIC technologies, a bipolar driver solution with a discrete output stage is more promising.

4.2.4.2 MOSFET

Figure 4.10 shows a block diagram of a MOSFET output stage. A high-current high-voltage output stage is implemented with DMOS transistors or high-voltage (thick gate-oxide) NMOS and PMOS transistors.
**Figure 4.9:** DC-coupled driver stage with bipolar output structure

**Figure 4.10:** DC-coupled driver stage with MOSFET output structure
High-voltage NMOS and PMOS transistors are available in a standard HV ASIC technology. With these transistors, a CCD driver stage ASIC seems to be realizable.

### 4.2.5 Driver Stage Realizations

The different transistor types and symbols used in this section are explained in Appendix A.

#### 4.2.5.1 Discrete driver stage

A complete discrete driver stage for all signals has been realized and tested. AC-coupled driver blocks were used for the horizontal signals. The reset signal driver was realized with a normal HCMOS buffer with TTL compatible inputs (e.g. the TinyLogic HST 2-Input Exclusive-OR Gate NC7ST86 from Fairchild [Dat99e]) and AC-coupling. The vertical signals are driven by a DC-coupled driver stage with the driver ICs MIC442X from MICREL [Dat98d]. One horizontal driver block with discrete components is shown in figure 4.11, the driver for the reset signal in figure 4.12, and the one for both vertical signals in figure 4.13. The top level schematic of the driver circuit is shown in figure 4.14. The voltage needed by the CDS and A/D stages are either +5V for discrete analog signal processing implementation or +3V for the standard ICs performing both CDS and A/D conversion. The voltage levels required for the CCD sensor are derived from +12V, 5V resp. +3V and -12V with series regulators. Since the two positive voltages are also used for other parts in the camera head, only the -12V has to be delivered by the back-end dedicated for this circuit.

The MICREL driver ICs are well suited for the vertical class signals, but for the horizontal and reset signals they are too slow. Measurements were done with the MIC4467/4468/4469 series [Dat98e]. These ICs are designed to drive loads of 100pF up to 1000pF. In a test setup with 100pF load, 5V CMOS input with 50% duty cycle and 10V supply voltage they worked fine up to 8MHz. At 10MHz the duty cycle became strongly asymmetrical and at 12MHz the output signal was mainly low with some peaks towards the supply voltage. But our goal for 30 frames/s would be 20MHz!
Figure 4.11: AC-coupled discrete driver stage for a horizontal signal (H)

Figure 4.12: AC-coupled discrete driver stage for a reset signal (R)
Figure 4.13: DC-coupled driver stage for the vertical signals realized with driver ICs from MICREL (V)
Figure 4.14: The complete discrete driver stage
The number of components used for this circuit is shown in table 4.7. The letters C stand for a capacitor in a 0603 package, D for a SMD-Diode, R for a 0603-resistor and T for a bipolar transistor in a SOT-23 package. C\textsubscript{Big} represents a 1210-capacitor of 1\mu F. LVR stands for a Linear Voltage Regulator such as LM117 or LM137. MIC is the MICREL driver IC MIC4427/4428 and TLB is a TinyLogic Buffer or equivalent.

<table>
<thead>
<tr>
<th>Part</th>
<th>R</th>
<th>C</th>
<th>D</th>
<th>T</th>
<th>C\textsubscript{Big}</th>
<th>LVR</th>
<th>MIC</th>
<th>TLB</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 * H driver stage</td>
<td>3</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1 * R driver stage</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>V\textsubscript{Offset}</td>
<td>3</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1 * V driver stage</td>
<td>-</td>
<td>5</td>
<td>1</td>
<td>-</td>
<td>3</td>
<td>-</td>
<td>2</td>
<td>-</td>
</tr>
<tr>
<td>voltage regulation</td>
<td>10</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Total</td>
<td>26</td>
<td>29</td>
<td>10</td>
<td>8</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

**Table 4.7: Number of components for a discrete driver stage**

The total area of the circuit in figure 4.14 including the routing is 24mm x 28mm on a both side equipped six layer PCB. The total measured current used to operate the CCD sensor at 30 frames/s by the discrete driver stage is 73.2mA. This is 1.82 times the total average current calculated for the KAI1010 in section 4.2.1.2.

### 4.2.5.2 PALANTIR: a monolithic CCD driver stage ASIC

Since the discrete solution uses too many components (space), a complete driver stage was implemented in an ASIC. The ASIC is divided into two parts, the voltage regulators and the drivers. The voltage regulators require external buffer capacitors. The driver stages are all DC-coupled and for the frame transfer pulse a charge pump circuit with external capacitors is used. The supply voltages of this ASIC are +5V and -11.5V as in the example of section 4.2.3. The technology used is the HV BICMOS 2\mu m from Alcatel Mietec. The ASIC has a size of 5.6mm x 5.42mm.

A block diagram of the ASIC is shown in figure 4.15 and one complete signal path in figure 4.16. First a level-shifter shifts the CMOS input signal down by about 5V. Then the signal is amplified to full swing in a Schmitt-trigger stage. In order to switch the output driver stage fast enough, the signal’s
Figure 4.15: Block diagram of the PALANTIR ASIC

Figure 4.16: Block diagram of a signal path
driving strength is amplified in an inverter chain. The driver stage at the end is an inverter connected to the corresponding low and high voltage levels of the signal.

Tests were done with the ASIC mounted chip-on-board (see figure 4.17). The number of components used for this driver stage is shown in table 4.8 where R is a 0603-resistor, C a 0603-capacitor, C_{Big} a 1210-capacitor and C_{Huge} a capacitor with a value of 22\mu F (size: 7.3mm x 4.3mm x 2.8mm).

![Figure 4.17: Picture of the chip-on-board mounted PALANTIR ASIC](image)

<table>
<thead>
<tr>
<th>Part</th>
<th>R</th>
<th>C</th>
<th>C_{Big}</th>
<th>C_{Huge}</th>
<th>PALANTIR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total</td>
<td>7</td>
<td>22</td>
<td>5</td>
<td>3</td>
<td>1</td>
</tr>
</tbody>
</table>

**Table 4.8: Number of components for the PALANTIR driver stage**

The total area including the routing is 17mm x 21mm on a both side equipped six layer PCB with the PALANTIR as chip-on-board component. The total measured current consumed by the PALANTIR driver stage to run the CCD sensor at 30 frames/s is 194mA. The DC current itself is 29mA which is 72% of the calculated current in the power budget calculation of the KAI1010 in section 4.2.1.2. The total average current of the PALANTIR
driver stage is 2.65 times the current of the discrete driver stage and 4.82 times the calculated current.

These results show, that a fully integrated driver stage for a CCD sensor uses too much power and the space gained does not justify the additional power. Another reason against a fully integrated solution are the changing specification of the CCD sensor voltages and of the analog signal processing part.

### 4.2.5.3 THROXTIL: a combined driver-stage and pulse-generator solution

For the reasons explained in the previous section 4.2.5.2, a new semi-integrated driver stage was designed with the high-voltage technology of AMS which is a fast 0.8µm technology with dedicated high-voltage transistors (CMOS, DMOS and bipolar). The low-voltage NMOS transistors can be used at different bulk voltages than the substrate voltage by putting them in a separate p-well if desired. The CMOS high-voltage transistors come in three different versions: one for high source-drain voltage with a thin gate oxide, one for high source-drain voltage and high gate-source voltage (medium gate oxide) and one for high source-drain voltage, high gate-source voltage and high source-bulk voltage (medium gate oxide).

With the possibility to isolate the wells of the NMOS transistors and to mix fast transistors and high-voltage transistors ‘as desired’, a new ASIC driver concept for an AC-coupled approach was developed.

The horizontal driver signal path is shown in figure 4.18. In addition to the voltages used for the CCD sensor, this driver stage requires a +5V supply voltage. This 5V supply can also be used for the pulse generator ASIC and the discrete analog signal processing stages. The main advantage of this concept is that the transistors are about three times smaller than the normal HV transistors used in the PALANTIR ASIC. Simulations predicted half of the dynamic internal switching current of the PALANTIR ASIC.

In addition to the driver stage for the horizontal signals, the driver stage for the reset signal, a 200 MHz LVDS clock receiver, a parameter link and a fully digital pulse generator were integrated in the same ASIC. Over the parameter link the camera head can be configured and the focus can be controlled. A block schematic of this ASIC in the camera head is depicted in figure 4.19.
Figure 4.18: Horizontal driver stage using AC-coupling and AMS 0.8μm HV process features

Figure 4.19: Block diagram of THROXTIL
A mixed-signal simulation of the ASIC is shown in figure 4.20. The LVDS input signal is received and translated to a full swing CMOS signal. Out of this signal, all the necessary pulses for the camera head are generated with an accuracy of 500ps (e.g. PIXCLK, SAMP). The 10V horizontal signals and the 6V reset signal for the CCD sensor at the output of the ASIC can also be seen in the simulation.

![Mixed-signal simulation of THROXTIL](image)

**Figure 4.20: Mixed-signal simulation of THROXTIL**

The simulated average currents for the 6V reset and the 10V horizontal signals at 27 °C and typical process characteristics are shown in table 4.9 for comparison. The efficiency values can vary by ±2.3% because of process and temperature variation.

<table>
<thead>
<tr>
<th>Signal Classes</th>
<th>Theor. Current</th>
<th>Simulated (6V/10V)</th>
<th>Efficiency %</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>0.6mA</td>
<td>1.92mA</td>
<td>31%</td>
</tr>
<tr>
<td>H</td>
<td>51.5mA</td>
<td>67.98mA</td>
<td>76%</td>
</tr>
<tr>
<td>Total</td>
<td>52.1mA</td>
<td>69.9mA</td>
<td>75%</td>
</tr>
</tbody>
</table>

**Table 4.9: Average current of THROXTIL driver stages**
In the die photograph of figure 4.21 the on-chip driver stages (H2, H1B, H1A, R) and the clock receiver (Rx) are in the upper part of the ASIC. The standard cells in the lower part form the pulse generator and the parameter link. The delay lines (Δ) for fine pulse adjustment are the dense square blocks between the driver stages and the standard cells. The chip size is 3.92mm x 4.76mm.

Unfortunately, the ASIC could never be used in the camera head because of a processing fault during fabrication and a misjudged parasitic capacitance from poly to substrate. In addition, the digital and analog supply voltage of the camera head was changed from 5V to 3V which made the ASIC and its driving concept obsolete. Because of the ever changing specification and voltages of our system, e.g. KAI1001 replaced by KAI1010, an integrated driver stage is not economical, and the advantages over the discrete driver stage are negligible. Therefore, the final system is realized with the discrete driver stage.
4.3 Pulse Generator Architectures

The design of pulse generators operating at different system frequencies is discussed in this section. After the optimal system frequency is chosen, the final realized solution is described.

The task of the pulse generator is to provide all different parts in the camera head with the appropriate pulses. Pulse timing can be affected in three different resolutions: pixelwise (50ns), coarse tuned (5ns) or fine adjusted (0.5ns). The pixelwise adjustment defines whether a pulse occurs during a certain CCD pixel (PIXCLK period: 50ns). This scheduling is done by a state machine. The coarse tuning defines the pulse width as well as the pulse position within a PIXCLK period with a resolution of 5ns. For the fine adjustment a resolution of 500ps is desired. In the camera head, 6 fine adjusted signals, and 2 coarse tuned ones have to be generated with individual offset and pulse width.

A 200MHz clock (or 100MHz 50% duty cycle in a double edge triggered design) is needed for the transmitter in the EIM camera system to transmit the 10bit CCD data (@ 20MHz) of one channel over one differential wire pair. Since the pulse generator and the transmitter are integrated on the same ASIC, the 200MHz clock is also available to the pulse generator and its main clock frequency has to be derived out of this clock. Without the need of a PLL circuitry, the following clock frequencies are available to the pulse generator: 20MHz, 40MHz, 100MHz and 200MHz.

The principle of generating a 20MHz periodic signal at different operating frequencies is depicted in figure 4.22. For a pulse generator clocked with 20MHz, the pulse generation is based on an asynchronous clock doubling circuit using a delay line and an EXOR gate (see figure 4.22). For frequencies with a multiple of 20MHz, feedbacked shift registers are used to generate raw pulse sequences which are further adjusted by the delay stages to their corresponding resolution.

A delay stage is depicted in figure 4.23. It contains subsequent delay blocks which can be activated separately. Each of the delay blocks has $2^i$ fine resolution delay elements (500ps). If a delay element is not enabled, it’s delay path is deactivated by signal gating techniques in order to reduce switching noise.
4.3 Pulse Generator Architectures

System Clock frequency = 20MHz

![Diagram of Pulse Generator Architectures](image)

System Clock frequency = n \cdot 20MHz; n > 1

![Diagram of Pulse Generator Architectures](image)

**Figure 4.22:** Pulse generation principle for different system clock frequencies

**Figure 4.23:** Delay stage containing delay blocks with selectable $2^i$ delay elements
For a given clock frequency \((freq)\), the required number of shift register elements \((nsre)\) is:

\[
nsre = \frac{freq}{20MHz} . \tag{4.3}
\]

The number of delay blocks \((ndb)\) used to achieve \(\Delta_t\) resolution with a given clock frequency \((freq)\) can be calculated with the following equation:

\[
ndb = \left\lfloor \log_2 \left( \frac{1}{freq \cdot \Delta_t} \right) \right\rfloor . \tag{4.4}
\]

The gate equivalents \((GE)\) used by the fine adjustment circuit can be calculated with equation 4.5 (for \(ndb > 0\)). Note that a delay stage has an initial delay because of the signal gating and multiplexers. This delay has to be compensated by inserting the same delay into the undelayed signal path (signal path “Not Delayed” in figure 4.22)

\[
GE_{Fineadjust} = 2 \cdot [(2^{ndb} - 1) \cdot GE_{Delayelement} + ndb \cdot (GE_{Multiplexer} + 2 \cdot GE_{AND} + GE_{Inverter})] + ndb \cdot (GE_{AND} + GE_{Multiplexer}) + GE_{AND/EXOR} . \tag{4.5}
\]

Each shift register requires a parallel load for a freely programmable pulse sequence. Therefore an additional multiplexer is required for each storage element. The GE equation for each shift register is:

\[
GE_{Shiftreg} = nsre \cdot (GE_{Storageelement} + GE_{Multiplexer}) . \tag{4.6}
\]

The sizes of the individual cells are shown in table 4.10 for the AMS 0.35\(\mu\)m process. The final layout of the pulse generators is fully routed over the cells, and therefore the total area can be calculated with the previous equations by replacing the gate equivalents with the corresponding areas.
### 4.3 Pulse Generator Architectures

<table>
<thead>
<tr>
<th>Cell</th>
<th>Area [μm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay Element (0.5 ns)</td>
<td>152.1</td>
</tr>
<tr>
<td>Multiplexer</td>
<td>127.4</td>
</tr>
<tr>
<td>AND</td>
<td>81.9</td>
</tr>
<tr>
<td>Inverter</td>
<td>40.3</td>
</tr>
<tr>
<td>EXOR</td>
<td>145.6</td>
</tr>
<tr>
<td>Storage Element (D-Flipflop)</td>
<td>345.8</td>
</tr>
</tbody>
</table>

**Table 4.10:** *Area of cells used for delay line*

<table>
<thead>
<tr>
<th></th>
<th>20MHz</th>
<th>40MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td># Shift Reg. (nsre)</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td># Delay Blocks (ndb) [5ns]</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td># Delay Blocks (ndb) [0.5ns]</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>8*Area(_{\text{Shiftreg}})</td>
<td>473.2μm²</td>
<td>946.4μm²</td>
</tr>
<tr>
<td>2*Area(_{\text{Delay}}) [5ns]</td>
<td>8'197.8μm²</td>
<td>4'828.2μm²</td>
</tr>
<tr>
<td>6*Area(_{\text{Delay}}) [0.5ns]</td>
<td>44'885.1μm²</td>
<td>24'480.3μm²</td>
</tr>
<tr>
<td>Total Area</td>
<td>289'491.8μm²</td>
<td>164'109.4μm²</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>100MHz</th>
<th>200MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td># Shift Reg. (nsre)</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td># Delay Blocks (ndb) [5ns]</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td># Delay Blocks (ndb) [0.5ns]</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>8*Area(_{\text{Shiftreg}})</td>
<td>2'366.0μm²</td>
<td>4'732.0μm²</td>
</tr>
<tr>
<td>2*Area(_{\text{Delay}}) [5ns]</td>
<td>1'258.4μm²</td>
<td>0.0μm²</td>
</tr>
<tr>
<td>6*Area(_{\text{Delay}}) [0.5ns]</td>
<td>13'873.6μm²</td>
<td>8'134.1μm²</td>
</tr>
<tr>
<td>Total Area</td>
<td>104'686.4μm²</td>
<td>86'660.6μm²</td>
</tr>
</tbody>
</table>

**Table 4.11:** *Total area budget of pulse-generator alternatives with different system clock frequencies*
Table 4.11 compares the total area needed to generate all eight different pulse signals of the camera head for different main clock frequencies. The 20MHz asynchronous pulse generator has the largest area and the pulse position is more dependent on temperature, process and voltage variations compared to the other variants. The smallest area and the most precise timing can be achieved with the 200MHz solution. The drawback of this solution is the periodic noise from the clock frequency which can affect the analog signal quality in the camera head.

4.3.1 ZATHRAS: a Combined Pulse Generator and Transmitter ASIC

The final camera head ASIC was designed with the 0.35μm process of AMS using a 100MHz clock and double edge triggered design technique. This corresponds to the 200MHz version of the pulse generator in the previous section 4.3. A block diagram of the ZATHRAS ASIC is shown in figure 4.24.

The ASIC receives a 100MHz or 200MHz LVDS clock and translates it to an on-chip full swing CMOS signal. The driver stage is completely off-chip and corresponds to the discrete driver described in section 4.2.5.1. The ASIC supports CCD signal processor ICs from BurrBrown [Dat99i], Exar [Dat99j] and Analog Devices [Dat99a] which feature a CDS stage and an A/D converter in one chip. The integrated transmitter converts the raw CCD data and additional control signals into two 200Mbit/s datastreams which are sent to the back-end using integrated LVDS transmitters. LVDS receiver and transmitter are described in section 5.4.

Other ASIC-specific data is listed in table 4.12. A die photograph of ZATHRAS is shown in figure 4.25. An LVDS receiver (Rx) and three transmitters (Tx) are on the right side of the standard cells. The fine adjustment delay stages are visible at the bottom of the ASIC. The size of the pad-limited ASIC could be reduced further by using a staggered pad-frame, but this was not supported by available library.
Figure 4.24: Block diagram of ZATHRAS
Figure 4.25: Die photograph of ASIC ZATHRAS

Table 4.12: Chip overview of ZATHRAS

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fine delay resolution</td>
<td>501ps - 512ps</td>
</tr>
<tr>
<td>Delay range</td>
<td>full period (20MHz)</td>
</tr>
<tr>
<td>Gate Equivalents</td>
<td>approx. 37'000</td>
</tr>
<tr>
<td>Hand-layouted transistors</td>
<td>3136</td>
</tr>
<tr>
<td>Technology</td>
<td>0.35μm CMOS, 1-poly, 3-metal</td>
</tr>
<tr>
<td>Core size</td>
<td>1.6x1.6mm²</td>
</tr>
<tr>
<td>Die size</td>
<td>3.5x3.5mm²</td>
</tr>
<tr>
<td>Package</td>
<td>CQFP, 100 Pins</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>3V</td>
</tr>
<tr>
<td>Max. current consumption</td>
<td>33.6mA @ 3V</td>
</tr>
</tbody>
</table>

1 Measured process variations between different ASICs
In this chapter, the link between front-end and back-end is discussed. An overview of all the necessary signals in between these two parts are shown in figure 5.1. In order to have the camera synchronized with the display unit, frame synchronization pulses need to be transmitted to the front-end. A programming and configuration link provides full access to all camera-head parts over one single link. Furthermore, a clock distribution/synchronization is needed between the camera-head and the back-end which is discussed in section 5.1. The two lines of digital CCD data have to be transmitted to the back-end together with control information such as beginning of frame (BOF), beginning of line (BOL), autofocus information and other arbitrary sequences.
The minimal bandwidth of the data link for a 1Megapixel 1-CCD camera working at a frame rate of 30Hz with 10bit pixel data is 300Mbit/s. However, the data from a CCD sensor contains idle times during the frame and line transfer of the CCD sensor (see section 4.1). If no line memories in the front-end are implemented, which would allow a continuous transmission of data, a peak the bandwidth on the data link of 400Mbit/s results for both CCD lines together. With a special coding, the control information can be transmitted over the same data link during the idle times as described in section 5.5. For cable bandwidth reasons, the two CCD lines are transmitted separately resulting in a bandwidth of 200Mbit/s for each channel.

5.1 Clocking Strategies

Different clocking strategies were analyzed during the project. The first strategy (see figure 5.2) was based on a master clock for the whole camera system generated in the front-end next to the CCD pulse generator and transmitter.

Due to excess noise and power consumption, the master clock was moved to the back-end and the Low Voltage Differential Signaling (LVDS) standard [ANS96] was chosen (see section 5.3) to transmit the clock to the front-end as shown in figure 5.3. Together with the CCD data, a reference clock (which can either be the system clock or a reference signal derived from it by a divider) is sent to the back-end to guarantee loss-free data transmission. This
transmitter scheme is used in most of today's LVDS transmitter solutions, e.g.
for digital flat-panel links (see DS90CR483/484 48-Bit LVDS Channel Link
Serializer/Deserializer [Dat99c] or DS90C387/DS90CF388 Dual Pixel LVDS
Display Interface (LDI)-SVGA/QXGA [Dat99b]).

In order to reduce the number of wires between the front- and back-end, and
to have the back-end clocked even if the front-end is disconnected, the prin-
ciple of figure 5.4 was examined. The introduced PLLs, the transmitters and
receivers as well as the flexible cable connection between front- and back-end all introduce jitter. At data rates of 200Mbit/s per channel a total jitter from all these parts has to be less than 1ns to guarantee loss-free data transmission. The best way to guarantee this is to lock the PLL in the back-end to the input datastream. This requires special coding of the CCD data to prevent too long periods without any changes.

![Diagram](image)

**Figure 5.4:** *Master clock in back-end with PLLs*

An simpler solution without any PLL and jitter problems is illustrated in figure 5.5. The CCD data is coded in the transmitter to allow an easy clock restoration at the back-end out of the datastream itself without PLL. These datastreams are called self-clocked signals and one possible solution is described in section 5.2.

Another solution without PLLs and with a minimal numbers of wires, where the back-end is clocked even with disconnected front-end is depicted in figure 5.6. The phase shift between the system clock and the incoming CCD data stream is detected. According to this difference, the CCD data is delayed by a programmable delay line before is is sampled by the receiver. The key part of this solution is the phase detector whose quality decides if the data is been received correctly even with the jitter introduced by all the other parts of the system. To limit its complexity a coded data transmission is favorable.
Figure 5.5: Master clock without PLLs, using self-clocked data transmission to back-end

Figure 5.6: Master clock without PLLs, using self adjustable delay line in back-end
The general characteristics of all these solutions are summarized in table 5.1. Due to power, noise and jitter, the finally chosen solution is figure 5.3 with the master clock in the back-end, without any PLL, and the data and clock transmitted together using LVDS compatible signals.

<table>
<thead>
<tr>
<th>Characteristics of figure 5.2 5.3 5.4 5.5 5.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of wires</td>
</tr>
<tr>
<td>Noise</td>
</tr>
<tr>
<td>Power</td>
</tr>
<tr>
<td>Jitter</td>
</tr>
<tr>
<td>Special Data Coding needed</td>
</tr>
<tr>
<td>Back-end clocked without front-end</td>
</tr>
</tbody>
</table>

Table 5.1: Complexity comparison of all presented clocking solutions

5.2 Clock and Data Recovery Issues

In order to generate or adjust the system clock in the back-end to the incoming datastream, a minimal number of transitions has to be guaranteed. The easiest way to do this is to prevent the transmitter from sending blocks with all bits zero or one by limiting the range to 1..1022. For the 10bit CCD data, this limitation is acceptable because of the photon shot noise of a fully saturated pixel and the dark current in a black pixel. With this restriction, a PLL or self-adjustable delay line solution becomes feasible.

A more complex scheme is required for the self-clocked signal solution in figure 5.5, where the data stream is ‘mixed’ with the clock signal. To include this additional clock information into the datastream, either a higher data rate and therefore a higher bandwidth is required (e.g. [Dat99d]) or the signal is transmitted using a 3-level coding as described in [SY94].
5.3 Link Signaling Comparisons

Three different interface standards were considered while developing the EIM camera link: CMOS, Positive ECL (PECL) and low voltage differential signaling (LVDS). The following comparison is based on the Ultra High Speed Buffer NC7SZ125 [Dat99f] from Fairchild as a standard CMOS component and the TTL-PECL-TTL translators from Synergy (SY100ELT22L [Dat99g] and SY100ELT23L [Dat99h]) as positive ECL 100K compatible ICs. For the LVDS interface standard, the DS90LV031A [Dat97] from National was chosen as typical driver IC, and the DS90LV028A [Dat98b] as receiver. All data is worst case and compared at a supply voltage of 3.3V with a capacitive load of 15pF and a cable with an impedance of 100Ω. Table 5.2 compares the basic values of the three variants.

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>PECL</th>
<th>LVDS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single or Diff.</td>
<td>single</td>
<td>diff.</td>
<td>diff.</td>
</tr>
<tr>
<td>Max. Data Rate</td>
<td>≈200Mbit/s</td>
<td>320Mbit/s</td>
<td>500Mbit/s</td>
</tr>
<tr>
<td>Max. Output Swing</td>
<td>3.3V</td>
<td>±950mV</td>
<td>±450mV</td>
</tr>
<tr>
<td>Min. Output Swing</td>
<td>3.1V</td>
<td>±470mV</td>
<td>±250mV</td>
</tr>
<tr>
<td>Min. Input Swing</td>
<td>1.3V</td>
<td>±310mV</td>
<td>±100mV</td>
</tr>
<tr>
<td>Input Margin</td>
<td>1.8V</td>
<td>160mV</td>
<td>150mV</td>
</tr>
<tr>
<td>Quiescent Supply Current</td>
<td>≈10μA</td>
<td>12.5mA</td>
<td>7.5mA</td>
</tr>
<tr>
<td>Supply Current @ 200Mbit/s</td>
<td>≈16.5mA</td>
<td>12.5mA</td>
<td>7.5mA</td>
</tr>
</tbody>
</table>

Table 5.2: CMOS vs. PECL vs. LVDS

System noise is mainly introduced by two different sources: switching noise on the supply (ground bounce) and electromagnetic interference (EMI). The ground bounce can be (almost) eliminated by a constant current approach as in LVDS, and since the EMI is strongly dependent on the voltage swing of a signal, reducing the output swing of the signal also reduces system noise.

Noise and different ground levels between the front- and back-end ask for either a high input margin if the signal is transmitted over a single wire or differential signal transmission. But a high input margin requires a high output voltage swing which increases system noise.

As long as ground differences between front- and back-end are of no concern, the cable length is limited by the attenuation and load of the cable and
the input margin. For PECL and LVDS, a cable length of 10m is reasonable whereas CMOS allows even longer cables.

The power dissipation of the CMOS standard depends on the load and the frequency, while the other standards use a constant current circuit design, and therefore have a constant power dissipation. For PECL and LVDS, the load only reduces bandwidth.

The LVDS interface standard was chosen for the EIM camera system because the system noise introduced and the power dissipated is minimal and the bandwidth of 200MHz and cable length of 10m is sufficient.

## 5.4 Realized Transmitter and Receiver Modules

In order to save the space which would be needed for external LVDS transmitters and to reduce noise and power dissipation, different on-chip LVDS receivers (Rx) and transmitter (Tx) modules were developed. Table 5.3 lists the main features of all designed modules, which are level and impedance compatible to the LVDS standard [ANS96]. Figure 5.7 shows all integrated LVDS module layouts.

<table>
<thead>
<tr>
<th>Used in</th>
<th>Type</th>
<th>Technology</th>
<th>Area</th>
<th>Max. Freq.</th>
</tr>
</thead>
<tbody>
<tr>
<td>THROXTIL</td>
<td>Rx</td>
<td>0.8µm BiCMOS</td>
<td>360µm x 187µm</td>
<td>&gt;333MHz</td>
</tr>
<tr>
<td>other project</td>
<td>Rx</td>
<td>0.6µm CMOS</td>
<td>264µm x 222µm</td>
<td>&gt;333MHz</td>
</tr>
<tr>
<td>other project</td>
<td>Tx</td>
<td>0.6µm CMOS</td>
<td>296µm x 406µm</td>
<td>&gt;333MHz</td>
</tr>
<tr>
<td>ZATHRAS</td>
<td>Rx</td>
<td>0.35µm CMOS</td>
<td>240µm x 114µm</td>
<td>&gt;666MHz</td>
</tr>
<tr>
<td>LEELOO</td>
<td>Rx</td>
<td>0.35µm CMOS</td>
<td>232µm x 200µm</td>
<td>&gt;666MHz</td>
</tr>
</tbody>
</table>

**Table 5.3: LVDS modules**

Since these modules were never tested within a separate integration, their maximum frequency was always limited by the functionality of the other parts in the ASIC. Nevertheless, the desired frequency (bit rate) of 100MHz (200Mbit/s) was obtained in all cases.

The current consumed by the modules of the final integration in 0.35µm CMOS technology of AMS was 1.5mA per receiver and 3.5mA per transmitter
5.4 Realized Transmitter and Receiver Modules

(a) THROXTIL Rx; 0.8μm BiCMOS, 1-poly, 2-metal

(b) Rx; 0.6μm CMOS, 2-poly, 3-metal

(c) Tx; 0.6μm CMOS, 2-poly, 3-metal

(d) ZATHRAS Rx; 0.35μm CMOS, 1-poly, 3-metal

(e) ZATHRAS Tx; 0.35μm CMOS, 1-poly, 3-metal

Figure 5.7: Developed LVDS modules (same magnification)
at a supply voltage of 3V. Even at a supply voltage of 2.6V, they were able to handle the datastream of 200Mbit/s without any errors over a 6m long cable.

5.5 Data and Control Transmission in EIM camera system

There are two different transmission links in the EIM camera system: the parameter link from the back-end to the camera head and the image data stream with a few control codes in the other direction. Over the parameter link, the whole camera head can be configured and frame/line sequences requested. The link uses one wire and is based on a biphase protocol containing a start sequence, the data and a stop sequence. In case of an error, an error sequence (link cmd) is returned to the back-end.

The downlink contains the image information from the CCD with frame/line start sequences (BOF/BOL) and several other predefined codes. The two video channels (each with 10 parallel pixel bits @ 20MHz, 1024 image pixels per line) from the two CCD signal digitizers are transmitted separately as NRZ data streams over two LVDS channels (each 200Mbit/s). An third channel provides the 100MHz transmission clock for the not clock-restoring solution in the back-end.

Figure 5.8 shows the transmitter protocol. Immediately before the first image pixel of a double line, the BOL or the BOF code is transmitted. After the last image pixel, one word for an autofocus command (autofocus0/1) and one for the link command (link cmd) is reserved. The remaining time to the start of a new line is available for additional 8bit data words (info data), which is transmitted serially in between start and stop sequences.

Figure 5.9 shows the defined commands. The letters A and B refer to the two parallel 200Mbit channels. Autofocus0 and autofocus1 are predefined autofocus commands and link cmd is the error return sequence for the parameter link.

All sequences between the CCD line data transmissions allow an easy word synchronization of the receiver due to the code violation at the second last bit. Furthermore the image data is rounded to the range 1 to 1022 in order to have at least one transition per word even during degenerated image data transmission.
5.5 Data and Control Transmission in EIM camera system

Figure 5.8: Transmitter protocol

<table>
<thead>
<tr>
<th>Image timing</th>
<th>Image data</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOF A</td>
<td>10 bits/pixel NRZ</td>
</tr>
<tr>
<td>B</td>
<td>lsb first</td>
</tr>
<tr>
<td>BOL A</td>
<td>range: 1 .. 1022</td>
</tr>
<tr>
<td>B</td>
<td>A: even pix</td>
</tr>
<tr>
<td>RefCLK</td>
<td>B: odd pix</td>
</tr>
<tr>
<td>100MHz</td>
<td></td>
</tr>
</tbody>
</table>

Figure 5.9: Control commands of transmitter
Seite Leer / Blank leaf
Back-end Design

A simplified block diagram of the back-end is shown in figure 6.1. The raw image data from the camera head is transmitted as differential signal to the back-end. After passing the differential receiver it is conditioned by the protocol decoder for subsequent processing. The correction unit contains a wide-range dark current and white gain compensation which ensures good results even with lower grade CCD sensors at lower cost. For this purpose at least 2MB of correction memory is required. The CFA interpolator reconstructs the two missing color components for each pixel. RGB data now pass the color space transformation in order to achieve best color fidelity with different scene illuminations. All aforementioned processes work on the two-channel data stream from the CCD sensor. The line serializer rearranges the data as to provide the usual progressive scan image to the high resolution frame grabber output. Aside this main data path the autofocus and illumination unit calculates the luminance components of the image and evaluates a two-dimensional criterion on a sizable window. The scan converter unit which uses a separate
memory to store images derives a standard digital image for a PAL video encoder for low-cost long-time documentation storage on a video recorder.

**Figure 6.1:** Block diagram of complete back-end
6.1 Correction of CCD and CDS effects

6.1.1 Dark Current Compensation and White Gain Adjustment

CCD sensors are classified into different grades depending on the number of minor and major defective pixels. A pixelwise gain and dark current compensation allows sensors with degraded pixels to perform the same as sensors without any defects. This reduces system costs.

Besides the minor pixel defects, the different sensitivity for each color component may degrade image quality. Therefore, even with high-grade CCD sensors, at least the gain of each color has to be adjusted.

The correction algorithm chosen for the back-end is shown in figure 6.2. First the gain of each pixel is coarse-adjusted depending on its color. Then the dark current of the pixel is compensated by subtracting a previously stored value, and finally the white gain is fine-adjusted. This corresponds to the following equation:

\[
\text{Pixel}_{\text{Corrected}} = \left[ (\text{Pixel}_{\text{Raw}} \times 2^{\text{PreGain}}) - \text{Offset}_{\text{DarkCurrent}} \right] \times \text{Gain}_{\text{White}} 
\]

(6.1)

According to the camera specification, two different operation modes are desired. A colorwise correction mode where each pixel is corrected depending on its color and a pixelwise mode where the dark current offset (6bit) and the
white gain factor (10bit) are pixel dependent. The pre-gain is always colorwise and only uses one 6bit register. For the pixelwise correction, the 16bit correction data has to be stored separately. Therefore a storage space of 2MB per correction set is required. Since this exceeds the scope of an on-chip RAM, the data is stored in an external SDRAM, and its controller must provide a continuous data rate of 80MB/s. A block diagram of the complete correction unit is shown in figure 6.3.

![Block diagram of the correction unit](image)

**Figure 6.3: Block diagram of the correction unit**

### 6.1.2 Effects Introduced by the CCD Signal Processor

For optimal signal processing in the front-end, the CDS stage needs an adequate bandwidth. Normally, for black and white sensors, the values of neighboring pixels are in the same range. But with a color filter array (CFA), the difference between a green pixel and its red or blue neighbor is often high, and therefore a fast CDS stage with a high bandwidth is required. And even with fast CDS stages, a small amount of a pixel value is transferred to its neighbor. This non-linear effect can be reduced digitally after the CDS stage is fully characterized.

Another solution how this effect can be compensated is shown in figure 6.4. Instead of using one CDS stage for the multiple colored pixelstream,
6.2 CFA to RGB Interpolation Algorithms

The corrected CCD image data provides only one color component (green, red or blue) for each pixel because of the Bayer color filter array (CFA) on-top of the CCD’s photodiodes. In order to achieve the full RGB information of each pixel, different more or less complex algorithms are discussed in this section. Most of these algorithms are described in [Ada95] and [Ada97]. The Bayer CFA arrangement used for the following calculations is illustrated in figure 6.5. The interpolation is explained for the missing two color components of the marked 2x2 pixels. All other pixels are similar. The pixels at the border of the image are mirrored to get a “infinitely repeated” interpolation area. Since the pixels being interpolated are in a 2x2 area, it is assumed that
these two lines are accessible for the interpolation algorithm without any fur-
ther line memories. This corresponds to the EIM camera system, because the
KAI-1010 CCD sensor has the capability to output two CCD lines in parallel.

<table>
<thead>
<tr>
<th>$B_{1,1}$</th>
<th>$G_{1,2}$</th>
<th>$B_{1,3}$</th>
<th>$G_{1,4}$</th>
<th>$B_{1,5}$</th>
<th>$G_{1,6}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_{2,1}$</td>
<td>$R_{2,2}$</td>
<td>$G_{2,3}$</td>
<td>$R_{2,4}$</td>
<td>$G_{2,5}$</td>
<td>$R_{2,6}$</td>
</tr>
<tr>
<td>$B_{3,1}$</td>
<td>$G_{3,2}$</td>
<td>$B_{3,3}$</td>
<td>$G_{3,4}$</td>
<td>$B_{3,5}$</td>
<td>$G_{3,6}$</td>
</tr>
<tr>
<td>$G_{4,1}$</td>
<td>$R_{4,2}$</td>
<td>$G_{4,3}$</td>
<td>$R_{4,4}$</td>
<td>$G_{4,5}$</td>
<td>$R_{4,6}$</td>
</tr>
<tr>
<td>$B_{5,1}$</td>
<td>$G_{5,2}$</td>
<td>$B_{5,3}$</td>
<td>$G_{5,4}$</td>
<td>$B_{5,5}$</td>
<td>$G_{5,6}$</td>
</tr>
<tr>
<td>$G_{6,1}$</td>
<td>$R_{6,2}$</td>
<td>$G_{6,3}$</td>
<td>$R_{6,4}$</td>
<td>$G_{6,5}$</td>
<td>$R_{6,6}$</td>
</tr>
</tbody>
</table>

Figure 6.5: Bayer RGB color filter array (CFA)

To demonstrate the differences between the interpolation algorithms, the
extremely enlarged test image of figure 6.6 is presented. This image contains
several subsections of test pictures as well as some synthetical structures that
make it specially sensitive to in interpolation artifacts. These structures and
the Siemens Star intentionally include spacial frequencies above the Nyquist
limit for each of the color components of the CFA. This is often the case
in real situations due to residues of imperfect spacial anti-aliasing filters in
the optical path. Tolerant interpolation algorithms will treat aliasing errors
inconspicuously. This original RGB image, sampled by an ideal CFA filter,
yields the test image of figure 6.7 that is used for comparing and evaluating
the different interpolation algorithms.
Figure 6.6: Test image used for interpolation studies
Figure 6.7: Sub-sampled test image using Bayer color filter array

Figure 6.8: Nearest neighbor replication algorithm graphically
Figure 6.9: Interpolated image using nearest neighbor replication
Figure 6.10: Bilinear interpolation algorithm graphically
Figure 6.11: Interpolated image using bilinear interpolation
Figure 6.12: Smooth hue transition in linear exposure space graphically
Figure 6.13: Interpolated image using smooth hue (linear exposure space)
1. Green (Luminance) Interpolation
2. Red/Blue Interpolation using Hue in Logarithmic Exposure Space
   - Luminance (Green)
   - Subtraction
   - Addition
Figure 6.15: Interpolated image using smooth hue (log. exposure space)
Figure 6.16: Two Line algorithm graphically
Figure 6.17: Interpolated image using the two line algorithm
Figure 6.18: Adaptive edge sensing algorithm graphically. horizontal edge assumed.
Figure 6.19: Interpolated image using adaptive edge sensing interpolation
Figure 6.20: Enlarged neighborhood algorithm graphically, horizontal edge assumed
Figure 6.21: Interpolated image using enlarged neighborhood interpolation
Figure 6.22: Comparison of all explained interpolation algorithms
6.2 CFA to RGB Interpolation Algorithms

6.2.1 Nearest Neighbor Replication

Where speed is essential and calculation power is limited, the nearest neighbor replication technique ([O'87]) is the most common. The missing color components of the four pixels of figure 6.5 are obtained using the following equations:

\[
\begin{align*}
R_{3,3} &= R_{4,4} \\
G_{3,3} &= G_{3,4} \\
R_{3,4} &= R_{4,4} \\
B_{3,4} &= B_{3,3} \\
R_{4,3} &= R_{4,4} \\
B_{4,3} &= B_{3,3} \\
G_{4,4} &= G_{4,3} \\
B_{4,4} &= B_{3,3}
\end{align*}
\] (6.2)

The value of a pixel is copied to the neighboring pixel(s) within the 2x2 area. Figure 6.8 explains this algorithm graphically and figure 6.9 shows the resulting image. Significant color errors can be seen in the neighborhood of fine structures (or edges). For motion imaging, these effects are less visible due to averaging over the frames, but for still imaging they are unacceptable.

6.2.2 Bilinear Interpolation

The next approach is the bilinear interpolation ([Cok86b]). The following equations can be defined for the two color components of the 2x2 pixels:

\[
\begin{align*}
R_{3,3} &= \frac{1}{4}(R_{2,2} + R_{2,4} + R_{4,2} + R_{4,4}) \\
G_{3,3} &= \frac{1}{4}(G_{2,3} + G_{3,2} + G_{3,4} + G_{4,3}) \\
R_{3,4} &= \frac{1}{2}(R_{2,4} + R_{4,4})
\end{align*}
\]
\[ B_{3,4} = \frac{1}{2}(B_{3,3} + B_{3,5}) \]
\[ R_{4,3} = \frac{1}{2}(R_{4,2} + R_{4,4}) \]  
(6.3)
\[ B_{4,3} = \frac{1}{2}(B_{3,3} + B_{5,3}) \]
\[ G_{4,4} = \frac{1}{4}(G_{3,4} + G_{4,3} + G_{4,5} + G_{5,4}) \]
\[ B_{4,4} = \frac{1}{4}(B_{3,3} + B_{3,5} + B_{5,3} + B_{5,5}) \]

Each color component is either an average of four or of two neighboring pixels. The scheme of this interpolation is shown in figure 6.10 graphically. It can be implemented without much hardware effort. Only a few adders are needed. One additional line, compared to the previous algorithm, is used for the interpolation. The drawback is that for systems where the three lines are not accessible at the same time, line memories are required. The result is shown in figure 6.11. The overall color artifact errors are less extreme, but other artifacts become more visible. These so-called “zipper” effects may not be visible in video streams due to motion blur, but for still imaging they are still not acceptable.

### 6.2.3 Smooth Hue Transition Linear Exposure Space

Most of the pixel artifacts occur because the hue values of adjacent pixels change abruptly. The green channel of the Bayer CFA can be considered as the luminance channel and the red/blue pixels then contain the chrominance information. With this in mind, the luminance pixels can be interpolated as before and the chrominance pixels by imposing a smooth transition in hue from pixel to pixel ([Cok87]). Defining a red hue-value as \( R/G \) and a blue hue-value as \( B/G \), the interpolation equations for the 2x2 pixels are:

\[ R_{3,3} = \frac{G_{3,3}}{4} \left( \frac{R_{2,2}}{G_{2,2}} + \frac{R_{3,4}}{G_{2,4}} + \frac{R_{4,2}}{G_{4,2}} + \frac{R_{4,4}}{G_{4,4}} \right) \]
\[ G_{3,3} = \frac{1}{4}(G_{2,3} + G_{3,2} + G_{3,4} + G_{4,3}) \]
\[ R_{3,4} = \frac{G_{3,4}}{2} \left( \frac{R_{2,4}}{G_{2,4}} + \frac{R_{4,4}}{G_{4,4}} \right) \]
\[ B_{3,4} = \frac{G_{3,4}}{2} \left( \frac{B_{3,3} + B_{3,5}}{G_{3,3}} \right) \]
\[ R_{4,3} = \frac{G_{4,3}}{2} \left( \frac{R_{4,2} + R_{4,4}}{G_{4,4}} \right) \]
\[ B_{4,3} = \frac{G_{4,3}}{2} \left( \frac{B_{3,3} + B_{5,3}}{G_{3,3}} \right) \]
\[ G_{4,4} = \frac{1}{4} (G_{3,4} + G_{4,3} + G_{4,5} + G_{5,4}) \]
\[ B_{4,4} = \frac{G_{4,4}}{4} \left( \frac{B_{3,3} + B_{3,5} + B_{5,3} + B_{5,5}}{G_{3,3} + G_{3,5} + G_{5,3} + G_{5,5}} \right) . \]

With this algorithm the green-values of all pixels need to be known for the red and blue interpolation. This means that the green values have to be interpolated first and to be stored until needed. Another drawback of this algorithm is the division by a variable divisor which is extremely hardware intensive and not suitable for real-time implementations. This algorithm is visualized in figure 6.12. The result is shown in figure 6.13. Compared to the previous examples, the color artifacts of the pixels have been desaturated significantly leading to less objectionable errors in the final image.

### 6.2.4 Smooth Hue Transition Logarithmic Exposure Space

Moving from the linear exposure space (of the previous algorithms) to the logarithmic exposure space lets replace the divisions by subtractions. Therefore, the logarithmic red hue-value of a pixel is \( R - G \) and the blue hue-value \( B - G \). Despite less complex calculations, this leads even to better results. With these values, the smooth hue transition can be described with the following equations:

\[ R_{3,3} = G_{3,3} + \frac{1}{4} (R_{2,2} - G_{2,2} + R_{2,4} - G_{2,4} + R_{4,2} - G_{4,2} + R_{4,4} - G_{4,4}) \]
\[ G_{3,3} = \frac{1}{4} (G_{2,3} + G_{3,2} + G_{3,4} + G_{4,3}) \]
\[ R_{3,4} = G_{3,4} + \frac{1}{2} (R_{2,4} - G_{2,4} + R_{4,4} - G_{4,4}) \]
\[ B_{3,4} = G_{3,4} + \frac{1}{2} (B_{3,3} - G_{3,3} + B_{3,5} - G_{3,5}) \]
\[
R_{4,3} = G_{4,3} + \frac{1}{2}(R_{4,2} - G_{4,2} + R_{4,4} - G_{4,4}) \quad (6.5)
\]
\[
B_{4,3} = G_{4,3} + \frac{1}{2}(B_{3,3} - G_{3,3} + B_{5,3} - G_{5,3})
\]
\[
G_{4,4} = \frac{1}{4}(G_{3,4} + G_{4,3} + G_{4,5} + G_{5,4})
\]
\[
B_{4,4} = G_{4,4} + \frac{1}{4}(B_{3,3} - G_{3,3} + B_{3,5} - G_{3,5} + B_{5,3} - G_{5,3} + B_{5,5} - G_{5,5})
\]

The green values have to be known before applying the red and blue equations. The big advantage over the smooth hue transition in linear exposure space is that the variable divisions transformed into subtractions which can be implemented in hardware without much effort, and that the whole interpolation for a color pixel can be calculated with one special 5-input or 9-input adder. This makes the algorithm more suitable for real-time applications. Figure 6.14 depicts this algorithm and figure 6.15 shows the interpolated image. The quality of the picture is barely better than in linear exposure space but the algorithm is far more computationally efficient.

### 6.2.5 Reduction of Smooth Hue Interpolation to Two Lines

In order to implement the bilinear or the smooth hue algorithm in real-time, line memories are required, because in addition to the line(s) being integrated, the two neighboring lines are accessed. For the case of the 2x2 area, where two lines are processed in parallel, four lines are required. The previous algorithms can be reduced to use only the two active lines. A smooth hue transition in the logarithmic exposure space for two lines is described by the following equations:

\[
R_{3,3} = G_{3,3} + R_{4,3} - G_{4,3}
\]
\[
G_{3,3} = \frac{1}{3}(G_{3,2} + G_{3,4} + G_{4,3})
\]
\[
R_{3,4} = G_{3,4} + R_{4,4} - G_{4,4}
\]
\[
B_{3,4} = G_{3,4} + \frac{1}{2}(B_{3,3} - G_{3,3} + B_{3,5} - G_{3,5})
\]
\[
R_{4,3} = G_{4,3} + \frac{1}{2}(R_{4,2} - G_{4,2} + R_{4,4} - G_{4,4}) \quad (6.6)
\]
6.2 CFA to RGB Interpolation Algorithms

\[ B_{4,3} = G_{4,3} + B_{3,3} - G_{3,3} \]
\[ G_{4,4} = \frac{1}{3}(G_{3,4} + G_{4,3} + G_{4,5}) \]
\[ B_{4,4} = G_{4,4} + B_{3,4} - G_{3,4} \]

Since this algorithm can be implemented very efficiently with only six pixels of short-time storage, it is well suitable for digital motion camera applications where additional line memories are not preferred. The algorithm is visualized in figure 6.16 and the resulting image is shown in figure 6.17.

6.2.6 Edge Sensing Interpolation

The most dominant interpolation artifacts are mis-colored pixels and the “zipper” effect at edges which occur because the luminance (green) interpolation is averaging neighboring pixels indiscriminately. A method to reduce these effects is to use a neighborhood sensitive criterion where the green interpolation is restricted to the one dimension parallel to an assumed edge. This however can not be done with only two lines.

The simplest way of sensing an edge (for pixel \( G_{x,y} \)) in the pixel neighborhood is to calculate the differences of the green pixels in horizontal and vertical direction:

\[ \Delta H = |G_{x-1,y} - G_{x+1,y}| \quad (6.7) \]
\[ \Delta V = |G_{x,y-1} - G_{x,y+1}| \quad (6.8) \]

Depending on these differences, the green interpolation is performed only in the direction in which an edge is assumed.

There are three different ways to interpolate the green pixel out of its adjacent pixels ([Hib95]):

\[ G_{x,y}H = \frac{1}{2}(G_{x-1,y} + G_{x+1,y}) \]
\[ G_{x,y}V = \frac{1}{2}(G_{x,y-1} + G_{x,y+1}) \quad (6.9) \]
where \( G_{x,y}A \) corresponds to averaging the four neighbor pixels and \( G_{x,y}H \), \( G_{x,y}V \) to an edge enhancing interpolation in the horizontal or vertical direction. With a threshold value \( T \), the adaptive green (luminance) interpolation algorithm is expressed in figure 6.23. The blue and red interpolation stays the same as for the smooth hue transition in logarithmic exposure space.

\[
G_{x,y}A = \frac{1}{4} \left( G_{x,y-1} + G_{x-1,y} + G_{x+1,y} + G_{x,y+1} \right)
\]

**Figure 6.23:** Adaptive green interpolation using an edge sensing algorithm

To show this algorithm graphically in figure 6.18 two different green pixel values were chosen to differentiate direction dependent patterns of a subsampled image. Figure 6.19 shows the result of the edge sensing algorithm for the green pixels and the smooth hue transition in logarithmic exposure space for the red and blue pixels. The chosen threshold value \( T \) is 30. There is far less “zipper” in the image. Different regions in the image have different optimal threshold values, which prohibits a general constant threshold value for an image.

There are other more enhanced edge sensing algorithms such as the pattern recognition approach described in [Cok86a], but they will not be discussed in this thesis due to their excessive computation overhead for real-time implementation.

### 6.2.7 Enlarged Pixel Neighborhood Interpolation

In order to reduce the zipper artifacts even more, especially at diagonal or picket fence structures, a larger pixel neighborhood with special filter algorithms is required.
Unfortunately, diagonal differences for the green pixels cannot be calculated, because there are no green pixels on the diagonals. One solution is to use also the red and blue pixels to predict the missing green values which is possible under the assumption that the color channels are correlated. This results in the image model described in [Ada97] that supposes the red and blue values to be correlated with luminance (green) over the extent of the interpolation neighborhood by using the following equation:

\[ G_{x,y} = RB_{x,y} + k \]  \hspace{1cm} (6.10)

\( RB_{x,y} \) is either the red or blue value (whatever available) at location \( x,y \) and \( k \) is the appropriate bias for the given pixel neighborhood. To illustrate the reasonableness of this model, figure 6.24 shows the image in grey scale (6.24(a)), and its decomposition into green (6.24(b)), red-green (6.24(c)) and blue-green (6.24(d)) channels. The contrast of red-green and blue-green is flat over most of the image, except for the synthetical right part of the image.

![Image](image.png)

(a) Original image (grey scale)  \hspace{1cm} (b) Green channel

![Image](image.png)

(c) \( \text{abs}(R - G) \)  \hspace{1cm} (d) \( \text{abs}(B - G) \)

**Figure 6.24:** Contrast of luminance minus chrominance
An algorithm which takes advantage of this model is described in [AH96]. For the interpolation in the one-dimensional pixel neighborhood (corresponding to a vertical or horizontal interpolation), the following 5 point FIR filters are introduced for luminance (green) \( h_L \) and chrominance (red/blue) \( h_C \):

\[
\begin{align*}
    h_L &= \frac{1}{2} \begin{bmatrix} 0 & a_1 & 1 & a_1 & 0 \end{bmatrix} \quad (6.11) \\
    h_C &= \frac{1}{2} \begin{bmatrix} a_2 & 0 & a_0 & 0 & a_2 \end{bmatrix} . \quad (6.12)
\end{align*}
\]

With this FIR filter the green values can be calculated using the following equations:

\[
\begin{align*}
    h &= \begin{bmatrix} h_L & h_C \end{bmatrix} \quad (6.13) \\
    G_{x,y} &= h \cdot \begin{bmatrix} L \\ C \end{bmatrix} \\
    &= \begin{bmatrix} h_L & h_C \end{bmatrix} \cdot \begin{bmatrix} L \\ C \end{bmatrix} \quad (6.14)
\end{align*}
\]

where \( L \) stands for the luminance and \( C \) the chrominance vector. The final chosen FIR filter coefficients are:

\[
a_0 = \frac{1}{3}; a_1 = \frac{1}{2}; a_2 = -\frac{1}{6} \quad (6.15)
\]

resulting in the new equations for the green values:

\[
\begin{align*}
    G_{x,y}H &= \frac{1}{2} (G_{x-1,y} + G_{x+1,y}) - \frac{1}{6} RB_{x-2,y} + \frac{1}{3} RB_{x,y} - \frac{1}{6} RB_{x+2,y} \\
    G_{x,y}V &= \frac{1}{2} (G_{x,y-1} + G_{x,y+1}) - \frac{1}{6} RB_{x,y-2} + \frac{1}{3} RB_{x,y} - \frac{1}{6} RB_{x,y+2} \\
    G_{x,y}A &= \frac{1}{4} (G_{x,y-1} + G_{x-1,y} + G_{x+1,y} + G_{x,y+1}) . \quad (6.16)
\end{align*}
\]
6.2 CFA to RGB Interpolation Algorithms

This interpolation algorithm also predicts green values for regions where there is actually no green. In order to prevent such false predictions, the decision algorithm has slightly been changed compared to the edge sensing algorithm. The new decision algorithm is shown in figure 6.25. If the average of the neighbor pixels is larger than a programmable threshold value $T$, enough green information is assumed to predict an edge depending on the horizontal and vertical differences. The red and blue values are calculated using the smooth hue transition in logarithmic exposure space as before.

![Figure 6.25: Adaptive green interpolation using an enlarged neighborhood](image)

The complete algorithm is depicted in figure 6.20. Figure 6.21 shows the result of the enlarged interpolation neighborhood algorithm with a threshold value $T$ of 30 (range $[0..255]$). To interpolate a green value of an image line, a total of five lines are used. For the chrominance interpolation the green values of two more adjacent lines pixels need to be known. This means that a total of seven lines are accessed to reconstruct a red or blue pixel value. Therefore, this algorithm needs six line memories additional to the line(s) being processed. The computation effort for this algorithm is not very complex since everything can be implemented with adders and “multiplication by a constant” blocks (e.g. $\frac{1}{3}$).

6.2.8 Decision and Final Remarks

The resulting images of all the above introduced algorithms are summarized in figure 6.22. The pictures have the same pixel resolution as before but are printed in 200dpi instead of the previous 44.275dpi. Comparing the pictures at 200dpi, the differences of the interpolation algorithms are far less obvious than before, because the images are not compared pixelwise anymore. All the
algorithms using the smooth hue algorithm in logarithmic exposure space for the blue and red pixels (6.22(e), 6.22(f), 6.22(g) and 6.22(h)) perform more or less the same. Differences can only be seen in edges, synthetical patterns or while looking at the pixels themselves e.g. in 44dpi. The “best” algorithm is the algorithm with the enlarged pixel neighborhood, which was chosen for the EIM camera system.

6.3 From RGB to True Color

Unfortunately, the scene illuminations, the target object, the optics, the CCD sensor, the display device and the human eye all have different spectral response or sensitivity. Reproducing a target object on a display device with all these components of a camera system results therefore in a miss-colored image. In order to display a target object in the colors seen by the human eye, a true-color camera system is required. In such a system more or less complex algorithms adjust or transform the color information of an image taken with the camera to the color information of the same image ‘recorded’ by the human eye.

There are several approaches described in [vO97] and [Kan97] in more detail. A well known algorithm is the gamma correction, which only adjusts the luminance by a constant exponential (gamma) factor.

Other more complex algorithms perform a vector or even a matrix transformation. In a vector transformation, each RGB value is adjusted linearly using only its own color information. This corresponds to the previously described case of the colorwise pixel correction algorithm. Using a 3x3 matrix transformation, each color component is (linearly) adjusted by the pixels RGB color information. An even more complex algorithm applies a 6x3 matrix transformation (see figure 6.26) to the interpolated RGB values of each pixel. The coefficients $a$ to $c$ are the linear factors and $d$ to $f$ the non-linear ones. They are chosen to minimize the mean colorimetric error for a test set of color samples by the actual scene illumination.
$\begin{bmatrix} R & G & B & R\cdot G & G\cdot B & R\cdot B \end{bmatrix} \times \begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ c_1 & c_2 & c_3 \\ d_1 & d_2 & d_3 \\ e_1 & e_2 & e_3 \\ f_1 & f_2 & f_3 \end{bmatrix} = \begin{bmatrix} r \\ g \\ b \end{bmatrix}$

$R, G, B :$ values from interpolation
$r, g, b :$ corrected values

**Figure 6.26:** Color space transformation using a 6x3 matrix
6.4 LEELOO DALLAS MULTICHIP: a Real-Time CCD Signal Processor

The back-end was realized with a single ASIC containing all described functions except the PAL video encoder. The correction RAM as well as the RAM needed by scan converter are external SDRAMs. The memories required for the interpolation and the line serializer are on-chip SRAMs. The block diagram of the LEELOO DALLAS MULTICHIP is shown in figure 6.27 and a chip overview is listed in table 6.1. Figure 6.28 shows a die photograph of the 7mm x 7mm ASIC with an enlarged LVDS receiver. The ASIC was presented at the ISSCC 2000 [D+00].

Figure 6.27: Block diagram of LEELOO DALLAS MULTICHIP
Figure 6.28: Die photograph of LEELOO DALLAS MULTICHIP with enlarged LVDS receiver
Resolution: 1024x1024 pixels
Frame Rate: 30 frames/s
Correction: pixelwise (64Mbit SDRAM) or colorwise (registers)
Interpolation: over nine lines
Color Space Transf.: 6x3 matrix
Input Data Rate: 400Mbit/s
Output Data Rate: 120MByte/s
Computation Perf.: 1.82G fixed point ops./s
Technology: 0.35μm CMOS, 3 met, 3.3V
Power Dissipation: 324mW (120.0mA @ 2.7V)
Transistors: 2.7 million
Geometry: 7mm x 7mm, 224 pads
Clock Input Freq.: 200MHz
On-chip RAM: 10 SRAMs @ 256x48bit
Package: 208pin CQFP

Table 6.1: Chip overview

The ASIC receives the two 200Mbit/s datastreams from the front-end by its LVDS receivers. The serialized data is transformed into 10bit data with the special architecture shown in figure 6.29. After the LVDS receiver, a 10bit double edge triggered shift register clocked at 100MHz stores the data, which is transferred in parallel into a 20MHz clocked register. A protocol decoder and word boundary synchronizer state machine then extracts the received data and at the output the two CCD lines with the control signals are available for further processing.

The integrated correction unit corresponds to the one described in section 6.1.1. Its architecture is shown in figure 6.30. The two lines are multiplexed together and alternatingly pixelwise processed by common arithmetic sub-blocks using double edge triggered design technique. At the end of this unit, the two lines are demultiplexed for further processing by the interpolation unit. The pre-gain values are taken directly from the on-chip register file and the offset and gain values come from the correction SDRAM interface. The correction unit performs 80 million multiply-accumulate (MAC) operations each second.
Figure 6.29: Architecture of complete receiver

10 DET Shift Register Stages

Protocol Decoder & Word Boundary Synchronizer

LVDS Receiver

- CH A +
- CH A -

200Mbit/s
100MHz

LVDS Receiver

- CH B +
- CH B -

20MHz

10 DET Shift Register Stages

Even Line (Channel A)
Control Signals
Odd Line (Channel B)
Figure 6.30: Architecture of correction unit
The external 64Mbit RAM for black current and white gain compensation holds four programmable correction sets. This enables buffering and therefore allows loading and switching during operation without loss of frames. The SDRAM interface for the correction unit as well as the configuration interface are shown in figure 6.31 in more detail. Depending on the programmed mode, the correction data is taken from the register file (colorwise) or from an external SDRAM (pixelwise). Sixteen bits of data are required each 40MHz cycle. This gives a continuous bandwidth of 80MB/s. To guarantee this bandwidth even with the necessary address and control overhead of a SDRAM, a 100MHz 8bit SDRAM interface was implemented. Eight 8bit words are read or written each 100ns. The SDRAM has its own 100MHz single edge triggered clock domain. The data and control signals to and from this interface are synchronized to the 20MHz double edge triggered clock domain from the surrounding blocks. Over the HAPI (hardware assisted parallel interface) interface, which is supported by USB controller chips, the whole ASIC can be configured. The SDRAM can be written and read over this interface too.

Since the interpolation algorithm with the enlarged pixel neighborhood (see section 6.2.7) was chosen and the two lines are processed simultaneously, the interpolation unit needs seven additional lines to the two lines coming from the correction unit. The implemented architecture is shown in figure 6.32. It contains two parts. The upper half of the figure depicts the seven line memories connected as a huge FIFO with a register chain at each memory output, which form the actual CFA pixel array used for the interpolation of the two marked pixels. In the lower part the architecture of the arithmetic part of the algorithm is shown. First the pixel neighborhood is examined which decides on the algorithm chosen for the pixel. Then the needed green values are calculated. After the green values are known, the red and blue values of the pixels being interpolated are calculated using three smooth hue transition interpolators which work in the logarithmic exposure space. Finally the RGB values of each pixel are selected and output.

The complete unit works with double edge triggered flipflops clocked at 20MHz. The seven on-chip SRAMs are clocked with 20MHz. The required memory bandwidth of this interpolation algorithm is 700MByte/s. A total of 380 million additions, 40 million multiplications and 160 million MAC operations are performed each second, giving a total of 580 million operations/s not including round and shift operations.

The color space transformation unit performs the previously described 6x3 matrix transformation. Its architecture is presented in figure 6.33. First the
Figure 6.31: Architecture of SDRAM and configuration interfaces
Figure 6.32: Architecture of interpolation unit
$R \cdot G$, $G \cdot B$ and $R \cdot B$ terms are calculated. Then the complete six-dimensional vector is given into three equal sub-blocks (one for each color component) which perform the actual transformation. These sub-blocks are illustrated in figure 6.34. A pipeline stage was needed to reach the required speed for the 20MHz double edge triggered design. The color space transformation unit performs 240 million signed multiplications and 600 million signed MACs each second.

**Figure 6.33: Architecture of color space transformation**

To rearrange the two lines in order to have progressive scan video at the high resolution output, on-chip line memories for one and a half video line have been integrated. The architecture is depicted in figure 6.35. The two lines are stored in two different FIFOs which are accessed by the output controller sequentially. The unit was realized using double edge triggered storage elements clocked at 20MHz. The on-chip RAMs as well as the output register are clocked at 40MHz.
Figure 6.34: Architecture of the color space transformation sub-block for one color component

Figure 6.35: Architecture of line serializer unit
One of the additional features of this ASIC is the support for autofocus and illumination control. The ASIC calculates a luminance image and over a programmable window a focus criterion. The luminance image has a resolution reduced by 4 compared to the original image. The focus criterion is based on the square plane sum modulus difference (SPSMD) of the image which is explained in figure 6.36 and [Ble00]. The luminance \( Y \) differences \( \Delta_i \) of four adjacent pixels are squared and the sum of these squares represent the SPSMD. Because this value depends on the size of the programmed window, the focus criterion is the SPSMD value normalized by the total number of differences \( N \).

\[
\text{SPSMD} = \sum_{i=0}^{N} \Delta_i^2
\]

\[
\text{focus criterion} = \frac{\text{SPSMD}}{N}
\]

**Figure 6.36: Focus criterion and SPSMD algorithm**

The architecture of this focus and illumination unit is presented in figure 6.37. First the luminance of each pixel has to be calculated according to equation (6.17)

\[
\text{RGB} \rightarrow Y : Y = 0.3 \times R + 0.59 \times G + 0.11 \times B
\]  \hspace{1cm} (6.17)

This luminance value is passed to the SPSMD as well as for the illumination control. After a 4:1 decimation, the reduced luminance image is output during each frame at a 10MHz rate for further processing. The focus criterion is calculated and becomes available at the output of the ASIC at the end of each frame. The focus and illumination unit has a 20MHz double edge triggered
clock domain and it performs 70 million additions, 40 million multiplications and 120 million MAC operations each second.

Another function of this ASIC is the scan converter which makes long-time low-cost video storage and documentation possible. An SDRAM as temporary frame memory and a PAL video encoder IC are the only external components required. Figure 6.38 illustrates the architecture of this unit. Simultaneous write and read operations for the frame buffering of the scan converter required a complex scheduling solution. The 4:1 decimated progressive scan images are stored in the external memory with a rate of 30 frames/s. According to the field and line synchronization pulses of the video encoder IC, the fields are read out from the SDRAM in an interlaced frame format with 50 fields/s.

The scan converter SDRAM interface is again clocked at 100MHz. On-chip FIFO memories couple the 10MHz 24bit input pixel stream to the 100MHz clocked SDRAM control unit, and synchronize the digital image data to the 14.75 MHz domain of the external video encoder IC. To save some space, the FIFOs were realized with latches instead of flipflops. The only computation effort are the 90 million additions needed to get the reduced resolution.

Not the whole functionality of this multi-function ASIC is used for each application. In order to save power and to reduce noise in the back-end when certain blocks are not in use, each block has its own clock distribution network which can be shut down by clock gating. Figure 6.39 shows the clock generator of the ASIC. All clocks inside the ASIC are derived from a 100MHz clock with a duty cycle of 50%, and from the video encoder clock of 14.75MHz.

The complete power consumption of the ASIC with all blocks running at a frame rate of 30Hz for the high-resolution images is summarized in table 6.2 for different operating voltages.

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.7V</td>
<td>120.0mA</td>
<td>324mW</td>
</tr>
<tr>
<td>3.0V</td>
<td>143.2mA</td>
<td>430mW</td>
</tr>
<tr>
<td>3.3V</td>
<td>162.4mA</td>
<td>536mW</td>
</tr>
</tbody>
</table>

Table 6.2: Power dissipation LEelOO DALLAS MULTICHIP
Figure 6.38: Architecture of scan converter unit
Figure 6.39: Clock generation for all units
Conclusions

Issues concerning the design of a microsystem have been investigated in this thesis at the example of a digital high-resolution video camera system primarily suitable for endoscopic and machine vision applications. Different approaches have been presented and a final miniaturized camera system has been built.

7.1 Realized EIM Camera System

First the key component of the camera system, the image sensor, was chosen. Comparison of CCD and CMOS sensors showed that CCD sensors are better suitable for miniaturized biomedical camera systems, due to their outstanding signal-to-noise performance. Furthermore, only one image sensor was to be used in order to reduce size and power. After the image sensor selection, the system specifications could be listed. According to these specifications,
the system has been partitioned into a miniaturized front-end and an image processing back-end.

In order to find the most suitable front-end solution for miniaturization, three different concepts were evaluated and compared in this thesis: PALANTIR, THROXTIL, and ZATHRAS. The PALANTIR ASIC, a completely integrated driver stage ASIC, used too much power compared to a driver stage with discrete components. A semi-integrated solution with the THROXTIL ASIC was not as economical as expected, not at last due to changed system specifications during its development. The finally realized front-end consists of standard components combined with the ZATHRAS ASIC, which contains pulse generator, clock receiver, parameter link and transmitter.

System partitioning and the therefore needed interconnections as well as clocking strategies are often key factors while designing a complex microsystem. It has been shown that the most promising high-speed interconnection principle is the LVDS standard, which was also chosen for the EIM camera system.

Miniaturization can strongly influence the computation effort. In our example, the decision to use only one CCD sensor instead of three requires complex algorithms to reconstruct and process the image information. In this work, different interpolation algorithms have been investigated and a real-time image processor ASIC LEELOO has been presented. It is the main part in the back-end. Two SDRAMs and a video encoder IC are the only external components needed. The ASIC corrects black current and white imbalance pixelwise, and performs a color interpolation over nine lines of images. A 6x3 matrix color space transformation is implemented to achieve true-color motion images with frame rates up to 30 frames/s. Additional features include a focus and illumination criteria calculation and a Megapixel-to-PAL scan conversion.

The realized camera system is shown in figure 7.1. For the analog signal processing in the front-end, standard ICs containing CDS stage and A/D converter were chosen. The driver stage was realized with discrete components and the pulse generator and transmitter units were integrated into the ASIC ZATHRAS. In the back-end, all described units are integrated in the ASIC LEELOO. The correction unit and the scan converter use additional external SDRAMs.

The final EIM camera system is compared to the 1Megapixel cameras of chapter 2 in table 7.1. It is smaller than the other cameras and capable to
Figure 7.1: Realized Camera System
deliver true-color images at a frame rate of 30Hz. In addition, it provides the user with a variety of interesting features such as a scan converter for long-time documentation and storage.

<table>
<thead>
<tr>
<th></th>
<th>Front-end Size [mm$^3$]</th>
<th>Back-end Size [mm$^3$]</th>
<th>Frame Rate</th>
<th>Color Capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>EIM</td>
<td>38x30x18</td>
<td>64x48x10</td>
<td>30Hz</td>
<td>true-color</td>
</tr>
<tr>
<td>BASLER A113C</td>
<td>45x62x62</td>
<td>PC</td>
<td>11.75Hz</td>
<td>with PC</td>
</tr>
<tr>
<td>DALSA CA-D7</td>
<td>89x89x105</td>
<td>-</td>
<td>40Hz</td>
<td>No</td>
</tr>
</tbody>
</table>

Table 7.1: Realized EIM camera system vs. other Megapixel cameras

### 7.2 Outlook

A front-end ASIC for other resolutions and sensor timings, based on the presented ZATHRAS ASIC, can be designed using the principles explained in this thesis.

The LVDS standard can be used not only for system interconnections but could also be used as high-speed serial chip interconnections, reducing system noise, power dissipation and pin count of ICs.

This image processor with its algorithms could also be used to improve the quality of today’s CMOS image sensors. Especially the pixelwise correction mode would help to scale down some of the disadvantages of CMOS image sensors. Furthermore, implementing these algorithms together with a CMOS sensor on one (huge!) chip would result in an improved camera-on-a-chip solution.
A

Transistor Types and Symbols

In this work, several different transistor types are used. In figure A.1 the different symbols are introduced.

![Transistor Symbols](image)

Figure A.1: Different transistor symbols and their meaning
The bipolar transistors for the are the high-speed switching transistors mentioned in section 4.2.4.1. The standard MOS transistors are 5V/3V transistors used in the standard 5V/3V CMOS technologies. The HV transistors are normal high voltage transistors with a thick gate oxide used in HV ASIC technologies. The HV thin-oxide transistors are found in the new HV CMOS technology from AMS. These transistors have the same gate parameters as a standard 5V MOS transistor but have a high voltage well for the drain. This allows drain-source voltages of 35V. Table A.1 compares the different MOS transistors.

<table>
<thead>
<tr>
<th>Type</th>
<th>$V_{GS}$</th>
<th>$V_{DS}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>standard NMOS/PMOS</td>
<td>5.5V</td>
<td>5.5V</td>
</tr>
<tr>
<td>HV NMOS/PMOS</td>
<td>20V</td>
<td>40V</td>
</tr>
<tr>
<td>HV thin-oxide NMOS/PMOS</td>
<td>5.5V</td>
<td>40V</td>
</tr>
</tbody>
</table>

**Table A.1:** Absolute max. voltages of different MOS transistors (AMS 0.8μm HV process)
Temperature and Power Consumption

The temperature specification for the hand piece was evaluated using a closed aluminum tube with heating resistors inside for power generation. The tube has an inner diameter of 3cm, a wall thickness of 2.5mm and a length of 10cm. This is a simple model for a camera hand-piece which could adopt a packaged CCD sensor. The smallest inner diameter for a naked CCD die mounted vertically is 2cm. Table B.1 shows the tube temperature measured at the outer surface with different power dissipations for the tube diameters of 2cm and 3cm.

<table>
<thead>
<tr>
<th>Power Diss.</th>
<th>Temperature Tube Ø: 3cm</th>
<th>Temperature Tube Ø: 2cm</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.500W</td>
<td>37 °C</td>
<td>52 °C</td>
</tr>
<tr>
<td>3.125W</td>
<td>44 °C</td>
<td>58 °C</td>
</tr>
<tr>
<td>3.750W</td>
<td>53 °C</td>
<td>64 °C</td>
</tr>
<tr>
<td>5.000W</td>
<td>66 °C</td>
<td>76 °C</td>
</tr>
</tbody>
</table>

*Table B.1: Temperature at different power dissipations*
For biomedical applications, the maximum temperature of a hand-held device is 38°C (human skin temperature is 26°C). Therefore the maximum total power consumption of the camera head without active cooling is 2.5W.

Because the final camera head diameter will be between the 3cm and the 2cm, the estimated temperature for 2.5W is between 37°C and 52°C. Therefore the total power consumption has to be lower than 2.5W.
In this Appendix, the noise and dark-current effects of the KAI1010 CCD image sensor by KODAK [Dat98c] are calculated. They are used to specify the sensors operating temperature limits and deviations to achieve a dynamic range of almost 10bit.

The following investigations are based on the datasheet of the KAI1010 CCD image sensor by KODAK [Dat98c]. Since all values in the datasheet are specified at 40 °C, the calculations are all based on this temperature unless otherwise specified.

The dynamic range of the sensor is 60dB @ 40 °C. The goal is to reach almost 10bit resolution. From the output saturation voltage of 350mV it follows:

\[ 1\text{LSB} = \frac{350\text{mV}}{1023} = 342\mu\text{V} \quad (C.1) \]

or with a sensitivity of 11.5µV/e\(^{-}\) this corresponds to:

\[ 1\text{LSB} = 29.75e^{-} \quad . \quad (C.2) \]
There are three dominant error sources in a CCD sensor:

- photon shot noise
- dark current
- dark current shot noise

Other kinds of error sources are the transfer inefficiency and the reset noise. Nowadays, the transfer inefficiency of 8000 CCD cells is so small that it became imperceptible in all applications. The reset noise can be compensated by correlated double sampling or delay-line processing techniques. All these errors and their sources are explained in [The95] and [vO97] in detail.

The dark current is highly temperature dependent and may differ from pixel to pixel. It can be compensated by pixelwise image correction. The photon shot noise and the dark current shot noise are both stochastical and cannot be compensated.

**Photon shot noise:** The photon shot noise can be calculated with the following equation using $N_e^- = \frac{V_{sat}}{11.5 \frac{W}{e^-}} = 43478 e^-$ which is the total number of electrons in a saturated pixel. (see also [vO97]):

$$\frac{S}{N} = \frac{N_e^-}{\sqrt{N_e^-}} = 208.5 e_{\text{rms}} \equiv 46 \text{dB} \quad .$$

(C.3)

This means that for a saturated region, hardly 46dB Signal to Noise can be achieved, which would correspond to 8bit. Darker image regions however will exhibit also the LSBs.

**Dark current:** The error introduced by the dark current at 40 °C with an integration time $T_{int}$ corresponding to 30 frames/s is:

$$\frac{Q_{dark}}{q} = \frac{I_{dark} \cdot T_{int}}{q} = 99 e^- \equiv 3.5 \text{LSBs} \quad .$$

(C.4)

The value for $I_{dark}$ changes by a factor of 2 every 8 °C. This dark current can be compensated by subtracting a previously stored dark image of the sensor acquired at the operating temperature.
Dark current shot noise: The dark current noise measured in electrons is:

\[ n_{\text{dark}} = \sqrt{\frac{Q_{\text{dark}}}{q}} = 9.96e^{-\text{rms}} = 0.351\text{LSBs} \quad \text{(C.5)} \]

Since the value for \( Q_{\text{dark}} \) changes by a factor of 2 every 8°C, \( n_{\text{dark}} \) changes by a factor of 2 every 16°C.

Dark current calculations at different temperatures: If the temperature increases 2°C, the dark current error increases by a factor of \( \sqrt{2} \). For 42°C the dark current is:

\[ \frac{Q(42°C)_{\text{dark}}}{q} = \sqrt[2]{2} \times \frac{I_{\text{dark}} \times T_{\text{frame}}}{q} = 118e^{-} \equiv 4.1\text{LSBs} \quad \text{(C.6)} \]

This means that for a change of \( \pm 2°C \) the dark current changes by \( \pm \frac{1}{2}\text{LSB} \). If the dark current compensation is optimized for 40°C, the compensation has an error of \( \frac{1}{2}\text{LSB} \) for a sensor temperature of 42°C. Therefore, for this 40°C dark current compensation, the temperature tolerance of the CCD sensor is \( \pm 2°C \).

For a larger temperature range, the dark current compensation has to be performed temperature dependent. The dark current error for the operating temperature can be derived from a previously measured error by equation (C.7). The actual operating temperature can be obtained by using a temperature sensor or by measuring the dark current of the light insensitive pixels (dark pixels) of the sensor

\[ \frac{Q(40°C + \Delta T)_{\text{dark}}}{q} = 2^{\frac{\Delta T}{8°C}} \times Q(40°C) \quad \text{(C.7)} \]
Dark current shot noise calculations at different temperatures: The dark current noise is also temperature dependent. For 56 °C the dark current noise is 0.7LSBs (see eq. (C.8)). Since this error can not be compensated, the sensor temperature has to be lower than 56 °C

\[ n(56^\circ C)_{\text{dark}} = \sqrt{\frac{Q(56^\circ C)_{\text{dark}}}{q}} = 19.9e_{\text{rms}} = 0.7\text{LSBs} \quad . \]  

(C.8)
Basic Power Estimations for the CCD sensor

For a first power estimation, the CCD sensor loads are assumed as purely capacitive. The energy transferred to one of these capacitors during the charge phase and the energy removed from such a purely capacitive CCD load during the discharge phase was calculated. The energy transferred during the charge phase is called $E_{C_{\text{Charge}}}$ and the energy removed during the discharge phase $E_{C_{\text{Discharge}}}$. The total energy transferred to and from the sensor can therefore be calculated using the following formula (note that this is charge and discharge):

$$E_C = E_{C_{\text{Charge}}} = E_{C_{\text{Discharge}}} = \frac{1}{2} C (\Delta V)^2$$

$$E = E_{C_{\text{Charge}}} + E_{C_{\text{Discharge}}} = 2E_C = C (\Delta V)^2 \quad . \quad (D.1)$$

The energy transferred during one reset pulse is:

$$E_R = 5 \text{pF} \times (6 \text{V})^2 = 180 \text{pJ} \quad . \quad (D.2)$$

The energy for the horizontal signal generation per horizontal shift is:

$$E_{H1A} = E_{H1B} = 100 \text{pF} \times (10 \text{V})^2 = 10 \text{nJ} \quad \quad (D.3)$$

$$E_{H2} = 125 \text{pF} \times (10 \text{V})^2 = 12.5 \text{nJ} \quad \quad (D.4)$$

$$E_H = (100 \text{pF} + 100 \text{pF} + 125 \text{pF}) \times (10 \text{V})^2 = 32.5 \text{nJ} \quad . \quad (D.5)$$
The vertical signals transfer the following energy per vertical shift:

\[ E_{V1} = E_{V2} = 25nF \times (9.7V)^2 = 2.35\mu J \] \hspace{1cm} (D.6)

\[ E_V = 2 \times 25nF \times (9.7V)^2 = 4.7\mu J \] \hspace{1cm} (D.7)

Each frame pulse the following energy is transferred:

\[ E_f = 25nF \times (8.8V)^2 = 1.9\mu J \] \hspace{1cm} (D.8)

The total energy transferred to and from the capacitors for a full frame can now be calculated with equation (D.9). Since the reset signal is continuously running, its total energy is the energy of one pulse multiplied by the ratio pixelclock frequency over frame frequency

\[ E_{R_{total}} = \frac{20MHz}{30Hz} \times E_R = 120\mu J \]

\[ E_{H_{total}} = 512 \times (1032 \times E_H + 1 \times E_{H1A}) = 17.18mJ \]

\[ E_{V_{total}} = 512 \times 2 \times E_V + E_f = 4.82mJ \]

\[ E_{Total} = E_{R_{total}} + E_{H_{total}} + E_{V_{total}} = 22.12mJ \] \hspace{1cm} (D.9)

The average power consumption and the average current for 30 frames/s for all the signal classes are compared in table D.1.

<table>
<thead>
<tr>
<th>Signal Classes</th>
<th>Energy per frame</th>
<th>Average Power</th>
<th>Average Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>120\mu J</td>
<td>3.6mW</td>
<td>0.6mA</td>
</tr>
<tr>
<td>H</td>
<td>17.18mJ</td>
<td>515mW</td>
<td>51.5mA</td>
</tr>
<tr>
<td>V</td>
<td>4.82mJ</td>
<td>145mW</td>
<td>14.9mA</td>
</tr>
<tr>
<td>Total</td>
<td>22.12mJ</td>
<td>663.6mW</td>
<td>67mA</td>
</tr>
</tbody>
</table>

**Table D.1:** Theoretical energy, current and power consumption
Bibliography


Curriculum Vitae

I was born in Zürich, Switzerland, on December 22, 1971. After finishing high school at the Kantonsschule Zug ZG (Matura Typus C) in 1991, I enrolled in Electrical Engineering at the Swiss Federal Institute of Technology ETH Zürich. I received the Diploma (M.Sc.) degree in Electrical Engineering (Dipl. El.-Ing. ETH) in 1996. In August 1996 I joined the Integrated Systems Laboratory (IIS) of ETH, where I worked as a research and teaching assistant in the field of ASIC and system design and test. Besides the work at the EIM project presented in this thesis, my main interests include digital signal processing and mixed signal circuits with applications to image processing, digital audio/video, and system-oriented VLSI design.