Educational Material

Computation in neuromorphic analog VLSI systems
Lecture WS 2001/2002

Author(s):
Kramer, Jörg; Delbrück, Tobias; Liu, Shih Chi; Indiveri, Giacomo

Publication Date:
2002

Permanent Link:
https://doi.org/10.3929/ethz-a-004306354

Rights / License:
In Copyright - Non-Commercial Use Permitted
Automated Data Acquisition and Analysis

The objectives of this lab are as follows:

1. To become acquainted with the lab instruments and data-acquisition techniques.
2. To become acquainted with the MATLAB program for data acquisition and manipulation.
3. To measure simple linear and exponential I–V characteristics using the Keithley Source-Measure instruments.

The primary purpose of this first lab is to familiarize everyone with the lab equipment and software. All of the instructions in this lab will be very simple, but fundamental for future labs, so please read this handout carefully and follow all of the instructions.

1.1 Prelab – To be Handed in at Start of Section.

All questions refer to ideal meters, sources, and devices unless otherwise stated.

1.1.1 Very Basic Circuits

Make the correct choices in the following statements:

A voltmeter has (zero/infinite) impedance and should be connected in (series/parallel) with the circuit being tested.

An amp-meter has (zero/infinite) impedance and should be connected in (series/parallel) with the circuit being tested.
Using the symbols shown in Fig. 1.1, draw the test setups you would use to measure the current (as a function of voltage) through a resistor and a diode.

### 1.1.2 Very Basic Equations

There are two common methods for measuring the resistance of a device. One method is to apply a voltage across the device and measure the resulting current. The other method is to pass a known current through the device and measure the voltage drop across the device.

Given the circuit in Fig. 1.2, qualitatively sketch as a function of the resistance, $R$, as it varies from 0 toward $\infty$:

1. the current through the resistor if $S$ is a voltage source at voltage $V$.
2. the voltage across the resistor if $S$ is a current source supplying current $I$.

In V/I mode, the Keithley 236 Source Measure Unit (SMU), the electrometer that you will use in the lab, supplies a voltage and measures the resulting current. In I/V mode (‘V’), the 236 SMU measures voltage supplying a current.

What would happen if you open-circuited the 236 SMU while you were measuring voltage?

The current source on the 236 SMU limits at 1100V. CMOS chips (like those that you will be using in lab) are unable to discharge the capacitance of the meter when it is charged to 1100V without destroying the circuitry on the chip. This means: **never open circuit the 236 SMU while the current source is enabled, and always disable the current source and ground the active lead before connecting it to your chip.**
1.1.3 Accuracy of the Keithley Meters

One of the first pages of the 236 SMU manual gives specifications for the meter. The accuracy is listed as $\pm (rdg\% + value)$. $rdg\%$ is an error term in percentage of the reading that you are getting. For example, an error of $\pm 1\%$ on a reading of 100nA is $\pm 1nA$. $value$ is related to the measurement range and is the error due to the digitization process. A digitization error of $\pm 700pA$ at 100pA resolution (if the smallest digit stands for 100pA) means that a reading of 1.0000 $\mu A$ is actually a value between 0.9993 $\mu A$ and 1.0007 $\mu A$.

Look at the specification page in the 236 SMU manual. Calculate the error for a resistance reading of 100.00k$\Omega$:

1. measured in I/V mode with a current of 50 $\mu A$.
2. measured in V/I mode with a voltage of 5V.

Express your answers as a percentage of the reading. The error in V/I mode is simply the sum of the errors in the source and the electrometer. Is this procedure a legitimate way to calculate the measurement error in V/I mode? Why or why not?

1.1.4 MATLAB

For those who do not know matlab yet there is online help available. Type ’help help’ and ’help lookfor’ to get useful starting information.

Outline a method to produce a plot of a Sine from 0 to $2\pi$ with 20 points (try ’help plot’).

How would you add a plot of a Cosine with the same range to the Sine plot with a different point marker and color?
1.2 The Keithley Instruments

The primary instruments you will be using in the first few labs are a Keithley Programmable Voltage Source (Model 230), and a Keithley Source Measure Unit (Model 236). Both can be controlled externally (in our case by a PC).

1.2.1 The Keithley 230 Programmable Voltage Source

In its simplest manual mode, the 230 is a variable voltage source with output voltages from 0.1mV to 101V. Both positive and negative output voltages are available. The output is floating relative to the chassis ground. The output voltage is set by the following procedure:

(i) Ensure that the OUTPUT OPERATE light is off by pressing the OPERATE button. This disables the output.

(ii) Ensure that the DISPLAY SOURCE light is ON by pressing the VOLTS button beneath it.

(iii) Type in the voltage using the key-pad in the DATA section (some part of the display will flash to indicate that you are entering a value) and press the ENTER key in the DATA ENTRY section.

(iv) Press the OUTPUT OPERATE button to apply the voltage to the test device.

Please be careful in typing in voltages, especially in setting the sign of all numbers and the correct exponent (with the EXPONENT key): transistors can tell the difference between 100mV and 100V! This is why you should always disable the output before you type in a new value. In order to try to protect the load device, the 230 has an internal current limit. The default of 2mA is adequate for testing integrated circuits. If the output is current-limited, the SOURCE light will flash.

1.2.2 The Keithley 236 Source Measure Unit

The 236 SMU is really three instruments in one:

1. a sensitive electrometer that measures current and voltage;
2. an independent voltage source;
3. an independent current source.
You cannot use all these functions independently, though. They are selected by the SOURCE MEASURE button (V/I or I/V). You always need to source and measure from the same two pins, so you cannot supply a voltage and measure a current elsewhere.

**Front Panel Controls**

There are five groups of buttons on the front panel:

1. SOURCE
2. MEASURE
3. SWEEP
4. TRIGGER
5. DATA ENTRY

The most important button in the SOURCE group is the OPERATE button. When its light is off, the source is not active. In order to apply the displayed source voltage or current to the devices output you must press this button first. It is a good idea to set the source to the appropriate voltage first and then make the device operate and not vice versa! And do switch it off before changing the value again!

The COMPLIANCE button lets you set the measure range. This has two effects. First, when not in AUTORANGE mode it freezes the units: When you specify your range to be ±1mA and the current you want to measure is actually 46.7nA the 236 SMU will display 0.0000 mA. And second and most importantly it acts like the 230’s current limit when sourcing voltage and like a voltage limit when sourcing current, also in AUTORANGE mode. As soon as this limit (the specified range) is reached the 236 SMU won’t supply more than that to maintain the desired source and the light above the COMPLIANCE button starts to blink. This may help to avoid the expensive experience of cooking a chip or even injuries. Its default values are ±10V and ±100μA. Change them only when you really know what you are doing! Working with integrated circuits this current limit is usually too low. A good value for it will be 2mA.

The SOURCE MEASURE button already mentioned earlier toggles between V/I and I/V mode. The FUNCTION button allows you to switch to the sweep mode in which the 236 SMU itself (without being controlled by an external computer) can perform a sweep measurement. We won’t need it now.
The next group is the MEASURE group. The only button we mention there now is the AUTORANGE button. It sets the 236 SMU to the autorange mode, where the measure range is set automatically. This is the recommended mode of operation.

The SWEEP group is not of interest at the moment.

In the standard setup the device expects you to trigger measurements manually. So after setting a voltage and making the 236 SMU operate you need to press the MANUAL button in the TRIGGER section to make the measurement happen.

The DATA ENTRY section lets you for instance set the source value or choose from a menu.

**Connections**

The Output Hi comes as a triaxial connection from the device’s rear and should be connected to the Potbox socket labelled 'TRIAX 1’. The Output Low is a normal BNC cable and goes into one of the BNC connections of the Potbox. Whatever it is you want to source and measure goes between the TRIAX1+ and the Output Low BNC. Do not connect TRIAX1-.

**1.2.3 Documentation**

The 230 should have a brief guide attached to its top surface. For both instruments there is a Quick Reference Guide booklet. In addition, complete operation manuals for all lab equipment are available on a shelf in the lab.

We will use the computer program MATLAB for taking and analyzing data. It is a commercial program that has been extended with commands that can communicate with the GPIB boards in the PCs in the lab. MATLAB is a very flexible and powerful program and provides good online help (type 'help help' after having started MATLAB). We will use only a small fraction of its capability in this class.

You must have an account on the PCs in the lab. Your teaching assistant (TA) can get you one. After having logged into one of the computers you can open an xterm with the left mouse button. Then type 'matlab' (without quotes) into it. This should startup MATLAB and after a while a ‘>>’ should appear at the beginning of a new line.
1.3 Experiment: Voltmeter/Electrometer Computer Controlled Operation

In this section we will discuss using MATLAB to control the voltage sources and the electrometer. There will be a temptation to always use the programs. When first setting up a circuit, try to resist the temptation to immediately take multiple operating curves. We have seen many examples of students who spend an hour taking curves, only to discover that a voltage had the wrong sign after the fact. Try a little manual sanity checking first.

1.4 Manual Data Acquisition

Using the 236 SMU as a voltage source and as an ampere meter (and again using it as a current source and a volt meter), measure the resistance of a carbon resistor (provided by the TA). Take about 5 data points by hand, with currents (voltages) approximately one order of magnitude apart. It is better to plot the data on a log–log plot to avoid bunching up all your points at one end. From this data, determine the resistance and compare it with the value marked on the resistor. Comment on any discrepancies, and suggest possible explanations. Which technique (V source–I meter, or I source–V meter) is more accurate? Why?

1.5 Computer Controlled Data Acquisition

You are now ready to take data using the computer. Type GUITake in the command window to invoke the data taking MATLAB script.

The window consists of an 2-D coordinate system (where data will be plotted), and of two areas with controls: Everything to the left of the button ’Take’ controls the data acquisition. The fields to the left of the button ’Fit’ we will use later to fit theoretical curves to the data and so find out the parameters of the measured device. But for now we will only take data.

You need to specify the sweep vector for the source to be swept (either the 230 or the 236 SMU) in the ’sweeping’ field. For us, the most useful of MATLAB’s types of vector specification is

\[ \text{start:increment:end} \]

Note that the increment has to be negative if start is larger than end. Also check
that you have chosen the right device and mode (‘I’ or ‘V’) for the sweep and for the measurement.

To perform the data acquisition, click on the menu button labelled ‘Take.’ The data will be placed in two vectors, one with the swept vector (the X vector) and one with the actual measurements (the Y vector).

NOTE: After data acquisition, the data is available in matlab in the vectors ‘GT_source’ and ‘GT_measure’. In case you forget this, you can always get a list of the variables in use in the MATLAB text-window by typing ‘who’. Everything that starts with ‘GT_’ is used by GUITake.

The data is automatically displayed on a graph while it is taken. You can print out your plot directly by using the ‘File’ menu option. However, this will plot the controls too. Nicer plots are achieved by typing ‘figure(2);plot(GT_source,GT_measure,’b-*’)’ in the MATLAB text window and printing it with that figures ‘File’ menu option. You can also save the plot to a postscript file.

If you want to fit your data to a theoretical expression you can call the curve fitting routine GUITake. The GUITake routine has been integrated with GUITake, so that the button labelled ‘Fit’ calls it. Before fitting you have to choose the function which will be fitted to the data. You have three choices: linear, exponential and hyperbolic tangent. You also have to define a range of points that are taken into account for the fit (give upper and lower limit) and initial parameters from where the search will start. The initial parameters can be quite crucial: when the fit doesn’t work properly, you might be successful with a better estimate of initial parameters. The parameters are stored in the MATLAB variable ‘GT_pars’ and the function values for the fitted function are in ‘GT_fit’.

To save your data to a file you can use the save command in the MATLAB command window (‘help save’) saving GT_source and GT_measure (preferably after having copied them to other variables with names of your choice). When you want to retrieve previously saved data into MATLAB use the MATLAB command load (‘help load’).

1.5.1 Experiment: An Exponential Transfer Function

Your TA will provide you with a 2N3904 transistor, which is an NPN bipolar transistor. You can use either the base-emitter or the base-collector junctions as PN diodes by leaving the other pin open. (To use the bipolar to make current gain, apply base voltages $V_{BE}$ and measure $I_{CE}$ with the 236 SMU.)

Notice that the current limit of the 236 SMU is set to 2mA (with the COMPLIANCE button). This should become obvious if you exceed base voltages of about 0.7V.
Use MATLAB to measure the I–V characteristic of both diodes. Take data for about 10 orders of magnitude of current. Fit an exponential to the data you took using GUITake. Finally, save the measured data and the theoretical curve to a file in your folder. You should *always* show data points explicitly by using the appropriate plot style.

Experimental techniques and devices are never ideal.

1. Over what range of currents/voltages does the diode behave exponentially?

2. How small a current were you able to measure confidently?

3. What is the slope of the exponential, expressed in mV/e-fold and mV/decade of current? You can estimate the slope visually, or you can calculate it two ways: (i) by taking the logarithm of the curve and differentiating the result (one way of doing this is to fit the linear function to the linear part of the logarithm of the curve), and (ii) by fitting an exponential in the correct range.

   You can also use `plot182` to plot a curve and then measure it using the cursor.

Next week we will begin measuring on-chip MOS transistors. All of the above questions and techniques will be directly applicable.

### 1.6 What You Need to Hand in.

Obviously there will not be much to write up for this week’s lab. Your prelab answers should be handed in as part of the lab. You will need to include plots of the resistor and diode I–V characteristics, showing any linear or exponential fits to the data. Show and briefly discuss the limiting regions of the plots and the slopes you calculated. Exponential characteristics should always be plotted on semilog coordinates. Include a brief discussion which addresses any questions asked in this handout.

*Remember, the lab must be turned in latest at the next lecture.*

### 1.7 What We Expect You to Learn

Basic use of the instruments. Very basic knowledge of matlab. How to use the potboxes.

What neuromorphic aVLSI is about. Who came up with it. Where is it being done.
Semiconductors, bands, band gap of silicon, the Fermi-Dirac distribution, donors and acceptors, PN junction, reverse and forward characteristics.

1.8 Reading for Next Week

Next week in lecture, we will be reviewing device physics and covering subthreshold MOS transistor operation. We have handed out chapters 2 and 3 of the book. We suggest you read the Chapter 2 (Semiconductor Device Physics) to review this week’s lecture, and part of Chapter 3 (MOSFET Characteristics) if you want a head-start on next week’s material.
Subthreshold Behavior of Transistors

In this lab we will be investigating the subthreshold behavior of isolated $p$– and $n$–channel MOSFETs. Specifically, we will measure the currents through the transistors as a function of their gate and source voltages; determine how effective these terminals are at changing the current, and compare the characteristics of native and well devices.

In addition, we will simulate the operation of isolated transistors using the circuit simulator AnaLog.

This lab will take 3 hours to complete if you are well prepared. If not, it could take considerably longer.

2.1 Prelab

Make sure you have completed the assigned reading from the lecture handouts before attempting this prelab. The questions will also make much more sense if you read through the entire lab handout first. You are required to complete this prelab and have it checked by your TA before you can begin taking data.

For the following questions assume an $n$–well process – unless stated otherwise.

1. Draw four-terminal symbols for native and well transistors and label all the terminals; use $d$ for drain, $s$ for source, $g$ forgate, $b$ for bulk, and $w$ for well. Indicate the direction of current flow that is consistent with your choice of drain and source.

2. Write expressions for the subthreshold (weak inversion) current $I_{ds}$ for both types of transistors. Indicate how you would measure the voltages that appear in these expressions by adding voltmeters to the symbols you drew. Hint: Think about what is the appropriate reference voltage.

3. Obtain expressions for the saturation current of these transistors, that is the
value of the current when \( V_{ds} > 4kT/q \). For the remaining questions you may assume that the transistor is in saturation.

4. Briefly describe the difference between biasing a native and a well transistor. You should state explicitly what the signs of the terminal voltages should be, relative to the appropriate reference, and which rail of the power supply provides the reference.

5. For both a native and well transistor, derive an expression for gate voltage as a function of source voltage if the channel current is constant. In each case, what is \( dV_s/dV_g \)?

6. Draw the arrangements you will use in experiments 1, 2, and 3 of the lab for each type of device which is to be tested. Include the voltages you will be using to bias the fixed terminals of the device and the voltage range you plan on using to generate the required curve. Be explicit in showing the Keithley 236 Source Measure Unit (SMU) and the Keithley 230 Programmable Voltage Source and also which terminal of the instrument goes where. To make the in-lab work easier it is a good idea to also include pin numbers. Note: It is not necessary to measure positive currents, you can easily swap sign once you have the curve in MATLAB.

### 2.2 General Facts about CMOS Chips

#### 2.2.1 Static Protection Measures

All MOSFET chips are extremely prone to damage by static electricity. The current through the transistors is controlled by an insulated gate. Even a few tens of volts can blow up the gate. A short walk across the room can build up kilovolts of static potential. There are electrostatic discharge (ESD) protection structures on the chip inputs that are designed to leak off the static charge before it can damage the chip, but often this will not be enough.

There are two simple precautions that can definitely keep the chip safe.

1. **When the chip is not powered up in a socket, keep it stuck into a piece of black conductive foam.** This will short all the pins together.

2. **Always ground yourself to chassis (potbox) ground before picking up or touching a chip.** This will discharge the static charge.
2.2.2 Powering up The Chip

Before inserting a chip into the socket, hook up all the power and ground connections to the correct pins. You will need to hook up $V_{dd}$ and ground even when testing isolated transistors, because the static protection structures at the pads won’t work otherwise, and the transistor bulks need to be biased correctly.

Then, hook up whatever bias voltages you might need. Next, turn on the power supply, turn up the voltage to whatever you want (+5 volts for the n–well chips you will be testing), and then turn down the current limit until the voltage just begins to drop. Then turn up the current limit a little bit. This procedure will keep excessive current from flowing into your chip in the event you have messed up the sign of the voltage or something else.

Next, turn the power on the potbox off, disable any other voltage sources you have hooked up, and then put the chip in the ZIF (zero-insertion force) socket (make sure you put it in the right way!). You can now power the potbox back on and enable the other voltage sources – in that order. If the voltage from the power supply suddenly drops, it probably means you have something hooked up wrong and the power supply is current limiting. The chips we use should only draw a few milliamps.
2.2.3 The Classchip and Chip Pinout Numbering

Chip pins are numbered as shown in the inset of Fig. 2.1, looking down onto the top of the chip. A schematic for the first classchip (classchip1d, Fab ID T18K AQ) can be found in Fig. 2.4, on the last page of the handout. Note that pin 5 is tied to Padbias. Connect this pin to a pot on the potbox and set it at 0.7V. Connect pins 25 and 35 to $V_{dd}$, and connect pin 15 to ground. $V_{dd}$ is +5V for these chips.

The chips are numbered. Make sure you write down the number of the chip you use every week, so we can keep track of which chips might be bad. If you think you have a bad chip, **don’t just put it back and grab another one**, and don’t write “bad chip” on it either (in many cases the chip is fine and the chip tester is having problems!). Point out the problem to your lab TA and let him/her figure out what to do about it.

2.3 $n$–Well Process

Native transistors are transistors that lie directly in the substrate whereas well transistors are transistors that lie in wells. The classchip is an $n$–well chip. That means that the wells are $n$–type. The native transistors have $n$–type sources and drains, and the well transistors have $p$–type sources and drains. The channels formed by the native transistors in the $p$–type substrate will be $n$–channels. A vertical section through the silicon with both native and well transistors is shown in Fig. 2.2.

Since we are grounding the substrate and we are using an $n$–well chip, $V_{dd}$ is at 5V. This reverse biases the junction between the wells (which are tied to $V_{dd}$) and the substrate (which is tied to ground)?

![Figure 2.2: A cross section through an $n$–well chip.](image-url)
2.4 Experiments and Lab Reports

For the following experiments include in your lab reports graphs of all theoretical and experimental curves. Experimental data should be plotted in a point style so that individual data points are visible. Make sure you take enough data points! The theoretical fit should be graphed on the same plot in a line style.

Please include your TA, section, and both names of the people who worked on the lab write-up. Partners produce a single lab write-up.

Remember that the purpose of this lab is to investigate subthreshold transistor characteristics. Therefore, all voltage sweeps should span the entire subthreshold regime while extending just far enough above threshold to show where the threshold is.

2.4.1 The Setup

You will be testing the 32/32 (width/length in $\mu$m) native and well transistors. Fig. 2.1 shows the setup and pinout for the native transistor for Experiment 1.

Always measure the current at the node that is not shared with other transistors otherwise you may get a significantly higher noise floor. For the native transistor, it is better to measure the current at the source as shown in Fig. 2.1, although, in theory, there should be no difference between drain and source. (Why is there a difference in practice? Remember that we will be measuring currents that are so small that they are comparable to leakage currents in the reverse-biased $pn$ junctions.)

The 230 will be used to sweep the voltage on the gate of the transistor while the 236 SMU measures the current. Tie the drain of the native transistor directly to $V_{dd}$. After manually checking whether your setup makes sense, use GUITake to take a rough curve of $I_{ds}$ vs. $V_g$ to see if everything is behaving as expected. A typical drain current will be about one nanoamp at a gate voltage of 0.5 volts. The current should increase about a decade for every 100 mV of gate voltage increase.

Obviously, the setup for the well transistor will be similar. Here, you will get lower noise if you measure the current at the drain (why?). The pinout for the well device is: S(1), D(8), G(26), W(2). For the well transistor, you will have to hook up the 230 as a floating voltage source between source and the gate. You can use the isolated BNC connector on the Potbox to do this. Connect the $-$ terminal to gate and the $+$ terminal to source so that you can use positive values for the gate voltage.

It is important to put the lid on the Potbox when doing low-level measurements. The chips and instruments are very sensitive, and sometimes even breathing on the chip can make a large difference in the amount of leakage current. Be careful when
you are taking data.

### 2.4.2 AnaLog – A Circuit Simulator

After you log in and start X with `startx`, start the circuit simulator AnaLog in the background by opening a terminal window and typing `analog&` at the unix shell prompt.

**AnaLog Tutorial**

To learn about AnaLog you can study the 5 interactive lessons provided with the software. You should copy the files containing the lessons to your local directory by typing the following command from a terminal:

```
cp /usr/local/chipmunk/log/lib/lesson* .
```

Now you can load `lesson1` through `lesson5` into AnaLog and follow the instructions that appear in the main window of the circuit simulator.

Or, you can simply drag an n-fet, a voltage source, and some ground and $V_{dd}$ voltage rails onto the page and watch analog start to simulate the transistor. You can drag voltmeters and current meters onto the circuit and click on them to label them. Then you can plot these quantities in the scope by going to the scope window and typing in the labels. You can make voltage sources that staircase sweep from one level to another at a specified rate, so you can make $I_{ds}$ vs. $V_{gs}$ plots. An example AnaLog file you can start from for the nfet is the file `/home/avlsi/nfetsim.lgf`.

You can use the matlab script `readanalog` or the function `readlog` to read into matlab the files dumped from analog’s scope window.

### 2.4.3 Experiment 1: Current as a Function of Gate Voltage

For native and well devices, measure current as a function of gate voltage for fixed source, bulk (substrate or well), and drain voltages. Short the source to the bulk and bias the transistor into saturation (make the drain source voltage large enough that $e^{-V_{ds}} \approx 0$).

Fit the theoretical expression you derived in the prelab to the data using the MATLAB program GUITake. You should include one plot for this experiment showing both native and well $I_{ds}$ versus $V_g$ curves with $V_g$ referenced to the bulk. In other words, both curves should start at $V_g = 0$ on the left edge of the plot and increase to the right. That way, you can make a direct visual comparison of the two transistors...
in terms of their \( \kappa \)'s, their \( I_0 \)'s, their threshold voltages, and the current at threshold. This means that you should switch the sign of the well transistor’s gate voltage by swapping the + and – terminals of the 230, as described in Section 2.4.1.

At the same time, your partner should be setting up and running the AnaLog simulation of a single transistor. You will need to configure the transistor to have the same size (W/L) as the one on the class chip, and then you will need to sweep the gate voltage while measuring the drain current using an Imeter probe. Then, from the scope window in AnaLog, you will need to export the simulation data and import it into matlab.

Comment on the values of \( \kappa \) and \( I_0 \) you extracted from your theoretical fits for the two devices. Also, discuss any discrepancies between the values of \( I_0 \) extrapolated by the theoretical fits and the values you actually measured. Finally, extract the threshold voltage and the current at threshold, using the definition given in class. Compare and contrast the resulting values for the native and well devices. Does the difference in threshold currents correspond to the fact that electrons have 2.5 times the mobility of holes?

On a separate plot, compare the simulation results for either the nfet or pfet transistor from AnaLog to the measured data. Most likely, you will see a large difference between simulation and reality. Why?

### 2.4.4 Experiment 2: The Back Gate Effect

The idea here is to characterize the relationship between the gate and source voltages for both a native and a well device when the channel current is held constant. This experiment shows convincingly the relative effectiveness of each terminal and provides measurements of \( \kappa \) over the entire operating range.

For this experiment, use the native transistor with S(10), D(9), G(39) and the well transistor with D(8), S(1), G(26), W(2), since the pad protection circuitry of the previously used devices draws more current than the 230 can supply for high gate voltages. **Make sure that the current limit of the Keithley 230 is set at 20mA.**

Short the source and well of the well transistor (that is, tie pins 1 and 2 together). Set the 236 SMU to source or sink about 1 nA of current. For the both devices sweep the gate voltage from 1V to 5V (relative to each device’s bulk) and measure the source voltage. Use the MATLAB `diff` command to differentiate your \( V_s \) versus \( V_g \) data curve and obtain \( \kappa \) as a function of \( V_g \). When its argument is a vector, the `diff` command returns a vector of differences of adjacent elements. An approximate derivative can be obtained as

\[
\text{diff}(Vs)/\text{diff}(Vg).
\]
Hand in two plots: $V_s$ as a function of $V_g$ for each device and $\kappa$ as a function of $V_g$ for each device.

Compare how much $\kappa$ varies for these two devices. Is the value of $\kappa$ that you obtained in Experiment 1 consistent with those obtained in this experiment?

## 2.5 Postlab

*The answers to the postlab should be included with your lab writeup.*

For the following questions assume an $n$–well process with the transistor in saturation

Many differences in the properties of native and well transistors arise from the fact that the well is more heavily doped than the substrate. Well doping is large in order to overwhelm the carriers in the substrate and insure a predominance of the proper carrier type in the well. For a native device, the $n$–type material of the well is the bulk, while the active areas (source and drain) are $p$–type. The gate voltage must force all the electrons in the $n$–well away from the surface. The resulting depletion region provides a channel for holes through enemy territory ($n$–well) separating the $p$–type source and drain. Remember, an encounter with an electron will be fatal! If the bulk is heavily doped, the gate must work harder to repel electrons.

Another way of saying this is that the capacitance of this depletion layer and the gate oxide capacitance form a capacitive divider that determines how much of the gate voltage appears at the surface channel. If the depletion layer is thin, the depletion capacitance will be large and hence the divider ratio will be unfavorable.

1. How does the width of the depletion region depend on the doping and on the channel potential? Assume that the doping density is uniform.

2. Explain why $\kappa$ varies with the source voltage.

3. Do the differences in bulk doping account for differences in $\kappa$ between the native and well devices?

4. From your results in Experiments 1 and 3, state under what conditions the assumption that $\kappa$ is constant is reasonable.

5. By fabricating a well device in its own well, we can use the well as a second gate – this gate is called a back gate. Derive an expression for the current in a saturated well device that shows explicitly the role of the back gate (i.e., $V_w$).

6. The circuit in Fig. 2.3 is called a *source follower* because its output $V_{out}$ (the source voltage) follows its input $V_{in}$ (the gate voltage). Source followers
Figure 2.3: A simple source follower. The bias to the lower transistor sets the current through both transistors.

are commonly used as buffers. However, this circuit is not ideal because its incremental gain is less than one. Design an ideal source follower using a well transistor and a second well transistor for a current source.

2.6 What We Expect

Knowledge of how subthreshold transistor operation is essentially a diffusion process and why it depends exponentially on the terminal voltages. $I_{ds}$ vs $V_{gs}$ on log scale. Differences between n- and p-fets. Typical values of $I_0$, $\kappa$ and subthreshold operating range. What are wells and how should the wells be biased relative to the substrate. What is the “back gate.” How the back gate is related to $\kappa$. How to make a MOS capacitor and what is its C-V relationship. How a source follower works and how to compute the gain of a source follower.

2.7 Next Week

Above threshold behaviour.
Figure 2.4: Schematic of class chip with pinout.
Lab 3

November 27, 2001

Transistors II – Above Threshold and Drain Characteristics

The objectives of this lab are as follows:

1. To characterize drain current of a transistor as a function of gate voltage above threshold in the ohmic (triode) and saturation regions.
2. To characterize the drain saturation properties in sub- and above-threshold.
3. To characterize drain conductance (the Early effect) and how it scales with drain current and transistor length.

3.1 Reading

Read Chapter 3 of the handout.

3.2 Useful Quantities

The following is a list of the physical parameters and constants we will be referring to in this lab, along with their values when appropriate. The units that are most natural for these quantities are also included; these units are not self-consistent, so make sure you convert the units when appropriate.
\begin{align*}
\epsilon_s & \text{ Permittivity of silicon = 1.04 pF/cm} \\
\epsilon_{\text{ox}} & \text{ Permittivity of SiO}_2 = 0.34 \text{ pF/cm} \\
\mu_n & \text{ electron surface mobility, cm}^2/\text{V} \cdot \text{sec} \\
\mu_p & \text{ hole surface mobility, cm}^2/\text{V} \cdot \text{sec} \\
C_{\text{ox}} & \text{ gate capacitance across the oxide per unit area, } \text{fF/} \mu\text{m}^2 \\
C_{\text{dep}} & \text{ capacitance of depletion region per unit area, } \text{fF/} \mu\text{m}^2 \\
t_{\text{ox}} & \text{ gate oxide thickness = 400Å} \\
V_T & \text{ threshold voltage, } V \text{ (} V_{T0} \text{ is } V_T \text{ when } V_s = 0\text{).} \\
W & \text{ electrical width of transistor channel, } \mu\text{m} \\
L & \text{ electrical length of transistor channel, } \mu\text{m} \\
\beta & \equiv \mu C_{\text{ox}} W / L, \ \mu\text{A/V}^2 \\
V_E & \text{ Early voltage, characterizes drain conductance}
\end{align*}

### 3.3 Prelab

Assume that all questions apply to the native device in the \textit{n–well} process, i.e. an n–fet, unless stated otherwise.

1. Write the most general expression for \( I_{ds} \) above threshold in terms of \( V_g, V_s, V_d \) (all voltages are referenced to the bulk), and the parameters and constants given above. Leave out the drain conductance Early effect in this equation. What are the differences between this equation and that for the well device?

2. Sketch graphs of the drain current vs. the drain voltage \( V_d \) for several gate voltages \( V_g \) above threshold, with \( V_s = 0 \). Indicate the ohmic and saturation regions and the behavior of the saturation voltage \( V_{dsat} \) as the gate voltage increases. How do these characteristics differ from the subthreshold ones?

3. Derive an expression for the current in the ohmic region, in terms of \( V_g \) and \( V_{ds} \equiv V_d - V_s \), from the general \( I_{ds} \) equation. You may assume that \( V_s = 0 \). Sketch a graph of \( I_{ds} \) vs. \( V_g \), showing \( V_{T0} \) and an expression for the slope.

4. State the condition for above-threshold saturation and derive an expression for the saturation current, \( I_{dsat} \), from the general \( I_{ds} \) equation. Sketch a graph of \( \sqrt{I_{dsat}} \) vs. \( V_g \) with \( V_s = 0 \), showing \( V_{T0} \) and an expression for the slope.

5. Calculate \( C_{\text{ox}} \) for the classchip from the values given above. What is \( C_{\text{ox}} \) per square micron in fF?

6. Write the expression for the drain current in saturation including the Early effect, using \( I_{dsat} \) to represent the saturation current in the absence of the Early effect.

7. Sketch the setups you will use.
3.4 Experiments

First, we want to remind you to be careful of static protection. Review the section in the Lab 2 handout which deals with this topic. Also, make sure the current limit on your power supply is set LOW so if you hook the circuit up wrong, you won’t blow up your chip.

You will use the same chip as in lab 2 (classchip1d, Fab ID T18K AQ). The schematic is once more attached at the end of this lab.

In the following two experiments, you will use the 32/32 n and p devices. The only difference in the measurements is the drain source voltage: in the first experiment you will use a small \( V_{ds} \), in the second, a large \( V_{ds} \). You can take all the data for experiments 1 and 2 in one quick session.

3.4.1 Experiment 1: Drain current in the ohmic region

In this experiment you will characterize the linear dependence of the current on the gate voltage in the ohmic region. For both native and well devices, measure \( I_{ds} \) as a function of \( V_g \) with \( V_d = 50 \text{ mV} \) and \( V_s = 0 \). Sweep \( V_g \) from 0 to Vdd in steps of 100mV or less. From this curve, determine \( V_{T0} \) and \( \beta \) for both devices by fitting your data to the expression derived in the prelab. Include a single plot showing both native and well curves in your report. What is the ratio between \( \beta \) for the 2 devices? Is the relationship between \( I_{ds} \) and \( V_{gs} - V_T \) really linear? What is the likely cause of any discrepancy?

3.4.2 Experiment 2: Drain current in the saturation region

In this experiment you will characterize the quadratic dependence of the current on the gate voltage in the saturation region. Repeat Experiment 1, but this time use \( V_{ds} = 5 \text{ V} \). (If you planned ahead, you already have this data). Plot \( \sqrt{I_{ds}} \) with appropriate fits and determine values for \( V_{T0} \) and \( \beta \) for both transistors. Again, include a single plot showing both native and well curves in your report.

Are the measurements of \( V_{T0} \) and \( \beta \) from the saturation measurement consistent with the values obtained in the ohmic region?
3.4.3 Experiment 3: Drain characteristics, the Early effect and drain conductance

In this experiment, with possible parts, you will either characterize the drain conductance of a single transistor operating at several different current levels, or characterize 5 transistors of different lengths operating at the same gate source voltage. *Your TA will tell you which of these measurements your group should do.*

**Drain characteristics of a single transistor at different gate biases**

Use the 32/8 native transistor that shares the gate with the other native transistors. Measure $I_{ds}$ as a function of $V_{ds}$ for at least 5 values of $V_g$, spanning sub- and above-threshold operation. For each value of $V_g$, sweep $V_{ds}$ from 0 to Vdd in steps of 100mV or less. Include a single plot showing all this data. Fit a line to the "flat" part of each curve. Select a range of drain voltages to fit the line and use the same range for each curve, because the Early effect is actually curved in reality, and what you are actually seeing is the start of Drain Induced Barrier Lowering (DIBL). Compute the Early voltage for each drain curve and include another plot of Early voltage versus drain current.

**Drain characteristics of transistors vs. channel length**

At a single subthreshold gate voltage, for the 5 native transistors of different lengths, measure $I_{ds}$ vs $V_{ds}$. Do the drain currents scale with 1/length as you expect? Measure the Early voltages for each device over the same drain voltage range and plot the Early voltage versus drawn channel length.

How linear is the relationship between length and Early voltage? What is the slope in volts/micron? Would you expect the drain resistance to be higher for native or well transistors? For extra credit, you can measure the well transistors too.

3.5 Postlab

1. Come up with an intuitive explanation to why the relationship between the above–threshold current and the gate voltage is linear in the ohmic region but quadratic in the saturation region.

2. In the subthreshold region: (a) Is the current linearly proportional to the gate voltage in the ohmic region like it is above threshold? Why? (b) Does the drain–source voltage at which the current saturates depend on the gate voltage? Why?
3. It is common to use a transistor as a diode by connecting its drain to its gate. Explain why it behaves like a diode when connected like this. Draw a diode and show how you will replace it with (a) an n–fet and (b) a p–fet.

4. When a diode–connected transistor is forward biased is it operating in the ohmic region or the saturation region? Does it make any difference whether it is biased above or below threshold?

5. Imagine we want to use a single transistor plus a perfect current source to make an amplifier with voltage gain. We use a native transistor, ground the source and connect the drain to a current source coming from the positive supply. We apply a gate voltage, and measure the drain voltage. Suppose the drain is hooked up to a perfect current source of infinite impedance that sources a known current $I_b$. Calculate the voltage gain $A$ from gate to drain (that is, $A = \partial V_d/\partial V_s$) in subthreshold and above-threshold in terms of the bias current $I_b$ and the usual transistor parameters $\kappa$, $\beta$, $V_T$, and $V_E$.

### 3.6 Congratulations

If you did everything in this lab, you have done a lot! This is probably the hardest but also the most important lab, because practical and intuitive knowledge of transistor characteristics is crucial in understanding and synthesizing new circuits.

### 3.7 What we expect


### 3.8 Next Week

Differential pairs, bump circuits, and transconductance amplifier.
MOSFETs with different L

Figure 3.1: Schematic of classchip1d with pinout.
Differential Pair, Current Correlator, and Bump Circuit

The objectives of this lab are as follows:

1. To measure the differential-pair currents as a function of the input voltages.
2. To test a simple current-correlator.
3. To characterize a bump-antibump circuit and understand how the output current depends on the bias current.

4.1 Reading

Read the section on the differential pair from the class handout. Make sure you understand the phenomenon that gives rise to the restriction of the input voltage range. In addition, read the section on the current correlator and the bump circuit.

4.2 Prelab

1. All parts of this question refer to the differential pair shown in Fig. 4.1(a). Unless stated otherwise, assume that \( M_1, M_2, \) and \( M_b \) are in saturation, that they are operated in subthreshold, and neglect the Early effect.

   (a) When working with differential circuits, it is often advantageous to express results in terms of the *common mode* voltage (denoted by \( \bar{V} \) or \( V_{cm} \)) and the *differential mode* voltage (denoted by \( \delta V \) or \( V_{dm} \)). These voltages are defined in terms of \( V_1 \) and \( V_2 \) by \( \bar{V} \equiv \frac{1}{2}(V_1 + V_2) \) and \( \delta V \equiv V_1 - V_2 \). Solve for \( V_1 \) and \( V_2 \) in terms of \( \bar{V} \) and \( \delta V \).

   (b) Compute the common source voltage \( V_s \) of \( M_1 \) and \( M_2 \) as a function of the inputs \( V_1 \) and \( V_2 \), and the bias current \( I_b \).
Rewrite your expression for $V_s$ in terms of the differential input $\delta V$ and $V_2$ and sketch $V_s$ vs. $\delta V$. Simplify this expression assuming that $V_1$ exceeds $V_2$ by a few $U_T$ and vice versa.

What restrictions would you put on $V_1$ and $V_2$ to ensure that $M_b$ is in saturation?

(c) Compute the currents $I_1$ and $I_2$ as a function of $V_1$, $V_2$, and $I_b$. What is the relationship between the differential output current $I_1 - I_2$ and the differential input voltage $\delta V$?

Sketch a graph of $I_1$ and $I_2$ versus $\delta V$. Also sketch the sum $I_1 + I_2$ and the difference $I_1 - I_2$ on the same axes.

2. For the simple current correlator in Fig. 4.1(b) show that

$$I_{\text{out}} = \frac{r_1 I_1 r_2 I_2}{r_1 I_1 + r_2 I_2}, \quad (4.1)$$

where $r_1$ and $r_2$ denote the ratios of the $W/L$ ratios for the transistors connected to $V_1$ and $V_2$ respectively. This means that $r_1 = w_{1\text{out}}/w_{1\text{in}}$ and $r_2 = w_{2\text{out}}/w_{2\text{in}}$, where the $w$'s denote the $W/L$ ratios of the corresponding transistors. Assume that $M_{2\text{out}}$ is in saturation, but note that $M_{1\text{out}}$ may not be.

3. Let

$$I_1 = \frac{I_t}{2}(1 + x), \quad I_2 = \frac{I_t}{2}(1 - x), \quad (4.2)$$

where $I_t \equiv I_1 + I_2$ is the total current and $x \equiv (I_1 - I_2)/I_t$ is a dimensionless variable.
(a) Substitute these expressions into (4.1) and obtain an expression for $I_{out}$ in terms of $I_t$ and $x$.
(b) Simplify your result assuming $r_1 = r_2 \equiv r$ and sketch a graph of $I_{out}$ vs. $x$. How is the graph modified if $r_1 > r_2$ or $r_1 < r_2$?
(c) Show that if $I_1$ and $I_2$ are generated by a differential pair then

$$x = \tanh \left( \frac{\kappa(V_1 - V_2)}{2U_T} \right)$$

 organ 4.3 Fitting data

For fitting lines to some measured data, you can use the matlab `polyfit` function to compute the slope and axis intercept, and the `polyval` function to evaluate the line on your input points to plot it, in order to see how well it fits. Here is an example. The input is $vin$, the measured outputs are $vout$. You want to fit the line in the range of $vout$ from 1.5 to 3.5. You use the `find` function to get the indices of the $vout$'s that are between these levels, then use `polyfit` to compute the coefficients of the line. Finally, you plot the data together with the fit.
Figure 4.2: Pinouts of the different circuits used in the experiments. The numbers in the squares denote the pin numbers. The sizes of the transistors are given as $W/L$ in microns. Some transistors are shared between the three circuits. These are denoted with the same numbers. (a) Differential pair. (b) Simple current correlator. (c) Bump-antibump circuit.

```matlab
ind = find(vout < 3.5 & vout > 1.5); % find vout’s in range
p = polyfit(vin(ind), vout(ind), 1); % fit order 1 polynomial (line)
ameas = p(1) % slope is p(1), y intercept is p(2)
f(1); clf;
vfit = polyval(p, vin); % compute values of fit at all points
plot(vin, vout, ’bo’, vin, vfit, ’b-’);
xlabel (’V_{in} (V)’); % TeX formatting for subscripts
ylabel (’V_{out} (V)’);
legend (’Vout’, ’linear fit for Vout’);
title (’Output voltage vs. input voltage’);
```

### 4.5 Experiments

#### Experiment 1: Differential pair

In this experiment, you will measure the dependence of the differential pair currents $I_1$ and $I_2$ on the differential input voltage $\delta V$. Use a pot to bias $V_b$. Tie the Keithley 230 between $V_1$ and $V_2$ (use one of the isolated BNCs) so that the applied voltage corresponds to the differential voltage. In order to keep the common mode voltage $\bar{V}$ constant during the sweep, connect equally-sized resistors (approx. 10 k$\Omega$) from a second pot to both inputs $V_1$ and $V_2$ as shown in Fig. 4.3(a). Set the pot to a common mode voltage of 2 V. To measure $I_1$, tie the Triax lead of the Keithley 236 SMU to the drain of $M_1$ and its BNC lead to $V_{dd}$; $M_2’s drain should be tied directly to $V_{dd}$. Set the 236 voltage to zero. This setup will keep $M_1$, $M_2$ and $M_b$ in
saturation for the subthreshold measurements. Explain why.

After sanity checking by manually plugging in differential voltages, use GUITake to sweep the 230 and measure $I_1$. Do this for a subthreshold value on $V_g$. The voltage range of the sweep should be large enough to cover the full range over which the current varies. Now switch the connections between $M_1$ and $M_2$ and repeat the sweep, measuring $I_2$ instead of $I_1$. Hand in a plot with your subthreshold curves showing $I_1$, $I_2$, $I_1 - I_2$, and $I_1 + I_2$ with appropriate fits.

**Experiment 2: Simple current correlator**

In order to measure the input-output relationship of the current correlator you will generate two variable input currents $I_{1\text{in}}$ and $I_{2\text{in}}$ with a constant sum $I_t$ (cf. prelab) 

*Note that $I_{1\text{in}} = I_1$ and $I_{2\text{in}} = I_2$ in prelab.* This can be done by retaining the differential voltage setup used in the previous experiment and linearly converting the voltages into currents. We can make a good approximation of such a linear conversion by feeding the input voltages $V_1$ and $V_2$ via resistors into the circuit’s inputs at pins 39 and 40 respectively. Use 20 MΩ resistors to ensure subthreshold currents as shown in Fig. 4.3(b). The currents through transistors $M_1$ and $M_2$ are proportional to the currents we feed into the circuit. We will measure them and assume them to be the actual input currents. **Tie pins 16, 18, and 19 to Gnd.**

Set the pot determining the common-mode input voltage to 2.5 V, sweep the 230 from $-5$ V to $+5$ V, and measure $I_{1\text{in}}$, $I_{2\text{in}}$, and $I_{\text{out}}$, one after the other with the same sweep parameters. Make sure that pin 17 is tied to Vdd when measuring $I_{1\text{in}}$ and $I_{2\text{in}}$. Hand in a plot showing $I_{1\text{in}}$, $I_{2\text{in}}$, and $I_{1\text{in}} + I_{2\text{in}}$ as a function of the differential input voltage with linear fits. How are the slopes of the curves related to the values of the used resistors? Plot $I_{\text{out}}$ as a function of the differential input voltage together with the curve you expect to obtain from the measured values of $I_{1\text{in}}$ and $I_{2\text{in}}$, using (4.1) with the given values of the transistor sizes. Where do the discrepancies come from? Twiddle $r_1$ and $r_2$ to improve the fit and hand in a graph of $I_{\text{out}}$ with the best fit..

**Experiment 3: Bump-antibump circuit**

You are going to measure the input-output relationship of the bump-antibump circuit for different bias currents.

Choose a subthreshold value for the bias current and measure $I_1$, $I_2$, and $I_{\text{out}}$ as you did for the current correlator. Again, use the same sweep parameters for each curve with a sweep range of ±250 mV. Hand in a plot showing $I_1$, $I_2$, $I_{\text{out}}$, $I_1 + I_2$, and $I_1 + I_2 + I_{\text{out}}$. Take one more $I_{\text{out}}$ curves for different subthreshold biases and
two more $I_{\text{out}}$ curves for different above-threshold biases. Remember to increase the sweep range for the above-threshold curves. Hand in the two subthreshold $I_{\text{out}}$ curves on one plot and the two above-threshold curves on another plot. Comment on the dependence of the width and height of the bump on the bias setting.

### 4.6 Postlab

1. Consider a current correlator with three inputs and three stacked transistors. How does $I_{\text{out}}$ depend on the three input currents $I_1$, $I_2$, and $I_3$?

2. We have seen that $I_{\text{out}}$ in the bump-antibump circuit is large when $V_1$ and $V_2$ are similar and its complement, $I_{\text{sum}} \equiv I_1 + I_2$, is large when they are dissimilar. How would you modify the device geometries to get a larger fraction of the bias current to go to $I_{\text{out}}$ in the first case and to $I_{\text{sum}}$ in the second case?

3. In the prelab, we suggested using a differential pair to generate the inputs to a current correlator. Draw a circuit that does this and use your results from the prelab (with $r_1 = r_2 \equiv r$) to derive an expression for $I_{\text{out}}$ as a function of $V_1 - V_2$. Write this expression in terms of the sech=1/cosh function.

### 4.7 Next Week

Transconductance amplifier.
Lab 5

Transconductance Amplifier

The objectives of this lab are as follows:

1. To characterize a simple differential transconductance amplifier and understand its operation in terms of the behavior of the differential pair and the current mirror. Specifically, to understand the dependence of the output current on the input voltages.

2. To measure the open-circuit voltage and determine the voltage gain of a simple transconductance amplifier and a wide-output-range transconductance amplifier.

3. To measure the output conductance and transconductance of the simple transconductance amplifier and relate them to the voltage gain.

5.1 Reading

Read the section on the transconductance amplifier in Chapter 5 of the class book.

5.2 Prelab

1. In a simple differential transconductance amplifier built from a differential pair and a current mirror the output current should be equal to the difference of the two differential pair currents, i.e. $I_{out} = I_1 - I_2$. Is this statement true? Justify your answer and state your assumptions.

2. Consider a simple transconductance amplifier with the output open-circuited (i.e. no current flows into or out of the output node). Say $V_2$ is fixed at some voltage in the middle of the rails. Explain what happens to the output voltage as $V_1$ is swept very slowly (i.e. slowly enough so that the output voltage reaches a steady state) from below $V_2$ to above $V_2$ for a subthreshold bias. Discuss the current through the differential pair transistors and the current...
Figure 5.1: Pinouts of the different circuits used in the experiments. The numbers in the squares denote the pin numbers. The sizes of the transistors are given as $W/L$ in microns. The input pins are shared between the two circuits. (a) Simple transconductance amplifier. (b) Wide-output-range transconductance amplifier.

3. What is the transconductance $g_m = dI_{out}/dV_{in}$, where $V_{in} \equiv V_1 - V_2$, below threshold? How does it change if the circuit is operated above threshold?

4. Quantitatively, what is the relationship between transconductance, output resistance, and voltage gain of a transconductance amplifier?

5. Diagram the circuits that you will use for the experiments, including voltage ranges.

### 5.3 This Week’s Test Circuits

Both transconductance amplifiers you will be taking measurements from are on Classchip-2001a. Their pinout is shown in Fig. 5.1. Also connect ground (pin 15), $V_{dd}$ (pins 25 and 35) and PadBias (pin 5, say to 0.8V).
5.4 Experiments

Experiment 1: Output current vs. input voltage

The purpose of this experiment is to explore the transfer characteristics of a simple transconductance amplifier. In particular, you will measure the effects of the bias current and input voltages on the output current. This is done by sweeping the differential input voltage for each bias current.

Use a pot to directly bias $V_b$ to whatever is sufficient to keep $M_b$ in saturation and the 236 SMU to set $V_{out}$ (about 3.5 V will do). Reference the 236 SMU to ground. Use the 230 to apply a differential input voltage $\delta V \equiv V_1 - V_2$ and measure the output current as a function of the differential input voltage $\delta V$, sweeping over a large enough range to ensure that the output current saturates at each extreme. Do this experiment for two values of $V_b$ below threshold and one value above threshold.

Show all your sweeps on one plot. Fit a simple theoretical curve to one of your subthreshold sweeps. What circuit parameters can you extract from the fit? Explain any asymmetries in the amplifier’s I-V curve in terms of mismatch between devices in the mirror and differential pair, and the Early effect. How can you distinguish the effects of mismatch in the mirror and in the differential pair? The main point here is to recognize that there will be non-idealities, to understand where they arise, and to quantify them in the simplest manner possible.

Experiment 2: Open-circuit output voltage

In this experiment you measure the voltage at the output instead of the current. Use the same connections as in the previous experiment. On the 236 SMU put the sourced current to zero and measure voltage. Bias $V_b$ in the subthreshold region.

Measure the open-circuit output voltage of the transconductance amplifier as a function of $V_1$ for three different values of $V_2$. Sweep the 230 voltage such that $V_1$ goes from zero volts to at least $V_2 + 0.2$ V. Plot all curves on the same graph. Comment on what is happening to $V_{out}$ in the various regions. Extract the $\kappa$ of the differential pair from a simple fit.

Repeat the experiment using the wide-output-range transamp with one of the two output stages. You only need to rewire your output because all the input connections are shared with the simple transamp. Qualitatively compare the results to the curves you obtained from the simple transamp.
Experiment 3: Voltage gain, output conductance, transconductance

First, you will measure the open-circuit voltage gain \( A \equiv \frac{\partial V_{out}}{\partial V_{in}} \), then the output conductance \( g_d \equiv -\frac{\partial I_{out}}{\partial V_{out}} \), and finally, the transconductance \( g_m \equiv \frac{\partial I_{out}}{\partial V_{in}} \). From these measurements, you will see how well the gain \( A \) is predicted by the formula \( A = \frac{g_m}{g_d} \).

In this series of experiments, use the same measurement configuration as for the previous ones. Again, for the current measurements, set the SMU 236 to a voltage that keeps all transistors in saturation (about 3.5 V). For the voltage measurements, put the 236 SMU current to zero. Do all measurements below threshold and use the same value of \( V_0 \) throughout. Once you have set this up, you will not need to change any connections between the three measurements. They are done directly from GUITake.

Do all the following experiments for the simple transamp and, if you have time in the end, measure the voltage gain for the wide-output-range transamp. Does the gain depend on the size of the output stage as you would expect?

Voltage gain \( A \)

Set one of the two inputs to approximately 1.5V. Locate the differential input voltage range where the output voltage changes rapidly (it will be quite small, around 2 mV, and not necessarily centered around zero!). Find the range by manually entering voltages into the 230. The circuit will be driving the electrometer directly, and at a subthreshold bias the currents available to charge capacitances will be very small. Notice how long the output takes to settle, especially in the high gain region. Knowing this, make your sweeps small, otherwise you will be sitting around a long time! Remember that you are only interested in the high-gain transition region. You can use the matlab global variable \( GT\_settle \) to set a larger delay time between setting the input voltage and measuring the output. GUITake will then ignore the first \( GT\_settle - 1 \) measurements for each new input voltage before taking the actual data point. In order to have the output voltage settle during the first, say, four measurements, type

```matlab
global GT_settle;
GT_settle=5;
```

into the matlab window, while the GUITake window is already active.

Once you have taken a satisfactory curve fit a linear function to it to compute the gain. (Resist the temptation to obtain the gain by differentiating the curve, since this operation is very sensitive to noise.) Plot the data and the fit on the same graph.
Output conductance $g_d$

Now measure the output conductance of the amplifier at the same bias voltage. First of all, fix one input to the transconductance amplifier to a constant voltage (approximately 1.5V will still do). Now find where to set the 230 so that the output current is zero (measure current with the 236 SMU). Then sweep the output voltage (the 236 SMU voltage source) over the high gain output voltage region while measuring the output current. Do a linear fit to determine the output conductance from your data.

Transconductance $g_m$

Now measure the transconductance at the same bias voltage. Sweep the 230 to get a curve of $I_{out}$ vs. $V_1 - V_2$. Extract the value of $g_m$ from this curve.

Compute the expected voltage gain using $g_m$ and $g_d$ and compare with the measured voltage gain. How well do these measurements agree?

5.5 Postlab

1. When we set the output voltage of the amplifier to about 3.5 V and measured its output current, we found that at some nonzero input voltage the output current was zero. Will we get a different input offset voltage if we change the output voltage? Explain why.

2. Draw a simple transconductance amplifier like the one in Fig. 5.1(a) and another one “upside-down,” i.e. with a pFET used to bias a pFET differential pair, and label the noninverting (+) input (makes the amplifier push out more current when it is made more positive) and the inverting (−) inputs (makes the amplifier suck in more current when it is made more positive).

   What are the conditions for keeping $M_n$ in saturation for the upside-down transamp? How do they differ from the other amplifier?

3. What are the advantages and disadvantages of the wide-output-range transconductance amplifier vs. a standard transconductance amplifier? Consider layout area, output voltage swing, offset voltage, current asymmetries, and the gain $A$. Why is the wide-output-range transamp particularly suited for construction of a high-gain amplifier? *Hint: think about the necessary symmetries between pairs of transistors.*
5.6 What we expect you to remember

The I-V characteristics of a transconductance amplifier below threshold. How the open-circuit characteristics differ between simple and wide-output-range transamp. The subthreshold transconductance $g_m$. The relation between $A$, $g_d$, and $g_m$.

5.7 Next Week

Circuit configurations using transconductance amplifiers.
Operational Amplifier in Feedback Configurations

The objectives of this lab are as follows:

1. To explore the use of feedback in operational amplifiers in linear circuit applications.
2. To learn how to implement simple arithmetic functions with the help of a operational amplifier and a set of resistors.

6.1 Reading

The unity-gain follower is described in Chapter 5.4 of the class book. The other circuits used in this lab are on the additional class handout and can also be found in any standard text book on analog circuit design (see for example the lab copy of the Horowitz-Hill “The Art of Electronics” book).

6.2 Prelab

1. Explain how a follower-connected operational amplifier works by describing how the feedback responds to a change in the input voltage.
   What is the relationship between $V_{in}$ and $V_{out} - V_{in}$?
   How would you measure the open-circuit gain of the amplifier in a follower-connected configuration?

2. When you build a linear circuit with a operational amplifier how do you pick the resistances of your resistors? What happens if they are too large or too small?
   Can such linear circuits be conveniently integrated on a silicon substrate? If not, what is the problem?
3. Derive the input-output relationships of the circuits you will measure, using Kirchhoff’s current conservation law, Ohm’s law, and the assumption that both inputs of the transamp are at the same potential.

4. Sketch the circuits you will use for the experiments, including the ranges of currents and voltages you will apply to them.

6.3 This Week’s Test Circuits

You will be using the operational amplifiers on the National Semiconductor LMC6064 Precision CMOS Quad Micropower Operational Amplifier. The pinout of the device is shown in Fig. 6.1. Ground is on pin 11 and $V_{dd}$ on pin 4.

If you use the top proto-board on the pot-box, remember to connect the ground and power lines to the $gnd$ and $V_{dd}$ lines of the bottom proto-board.
6.4 Experiments

Experiment 1: Unity-gain follower

Configure the operational amplifier as a follower. Sweep the input voltage with the 230 between the voltage rails and measure the output voltage. Hand in a plot showing $V_{out}$ vs. $V_{in}$ with a linear fit. Determine the voltage gain from the fit.

Now, take data over the ‘unity gain’ region with the 236 SMU connected between the output and the input. Do you see any systematic offset voltage? Hand in a plot of $V_{out} - V_{in}$ vs. $V_{in}$ with a fit and compute the voltage gain from this fit.

Which one of your two fits gives you the more accurate value for the voltage gain? Why?

Experiment 2: Voltage amplifier/reducer

Use one of the operational amplifiers on the LM6064 to build a non-inverting voltage amplifier (Fig. 6.2(a)) with a gain of 2. Reference your circuit to ground.

Use the 230 to provide the input voltage and measure the output voltage with the 236 SMU. Hand in a plot showing the output voltage as a function of the input voltage with a linear fit. Over which input and output voltage ranges does the
circuit work? What restricts the accuracy of the slope and its linearity?

Repeat your measurement for an inverting voltage reducer (Fig. 6.2(b)) with a gain of -0.1. Provide a reference voltage of 2 V to the non-inverting input of the op-amp and connect the 230 between the input and the reference voltage and the 236 SMU between the output and the reference voltage.

**Experiment 3: Adder/Subtractor**

Build a unity-gain inverting adder (Fig. 6.3(a)) using another amplifier on the LM064. Use a reference voltage of 3 V for the circuit and for the 230 and 236 SMU. Bias one of the inputs to 4 V with a pot. Sweep the other input with the 230. What is the useful sweep range? Measure the output voltage with the 236 SMU. Repeat the sweep for a fixed input voltage of 5 V. Hand in a plot showing both traces with a linear fits.

Build a unity-gain subtractor (Fig. 6.3(b)). Set the reference voltage to 2 V. Bias the non-inverting input to 3 V with a pot and sweep the inverting one. Repeat the measurement for a non-inverting input voltage of 4 V. Show both traces with linear fits on one plot.

What are the limitations of the adder and subtractor circuits?

**6.5 Postlab**

1. Does a simple operational amplifier configured as a unity-gain follower suffer from a restriction in the input voltage range for proper operation? What
about keeping the bias transistor in saturation? What will happen if the input/output voltages drop near or below $V_s$? *Hint: consider the bias current and remember that voltages change really slowly when the current is very small.*

2. You used operational amplifiers for all experiments. In which circuits would the use of a simple subthreshold transconductance amplifier reduce the operating range?

3. Draw a circuit that computes a weighted sum of three inputs with weights 0.1, 0.3, and 0.6.

### 6.6 What we expect you to remember

How to use a non-linear circuit, such as a operational amplifier, to compute linear functions. What a unity-gain follower is used for. How to build a linear current-to-voltage converter (although we didn’t build one in the lab).

### 6.7 Next Week

Follower-Integrator.
Lab 7

March 20, 2002

Integrator Circuits

In this lab we will finally begin to explore the time domain.

The objectives of this lab are to:

- Learn how to use the Tektronix TDS 300 Series Digital Oscilloscopes and the HP 33120A Function Generator.
- Understand the behavior of the follower-integrator circuit in the time domain and the frequency domain.

7.0.1 Reading

Useful info about this subject can be found in the class-script and in Chapters 8 and 9 of the Carver Mead book (‘Analog VLSI and Neural Systems’) paying particular attention to the time and frequency domain treatments of the RC circuit, pages 129-130 and 137-140 in Chapter 8, and the follower-integrator circuit, pages 147-149 and 158-162 in Chapter 9.

7.0.2 Prelab

1. Derive the transfer function for the follower-integrator, using the s-plane notation.

2. Why is the transfer function not all there is to a circuit? Compare the simple RC integrator, constructed from a resistor and a capacitor, and the follower-integrator.

3. How are capacitors constructed in our technology? There are several different possible implementations. How are they constructed in neurons?

4. What does “small-signal” mean? In other words, what voltage range will this regime correspond to? For the follower-integrator circuit is it the amplitude of the input or the output or the difference between the two that matters? Why?
7.1 Experiments

Experiment 1: The RC integrator

This experiment examines the time-domain behavior of the simple RC integrator. Use a low amplitude square wave as input to the RC integrator and measure the output with the oscilloscope, as shown in Fig. 7.1. Use the SYNC output of the HP function generator as the external trigger for the scope (EXT TRIG input). Display the input and output voltage waveforms on the scope and adjust the HP33120A’s frequency so that the integrator’s time constant $\tau$ is about 20% of the high or low half of the cycle. In other words, adjust the period so that the rise time of the output waveform can be seen and the output rises to about the same maximum amplitude as the input waveform. Capture both waveforms and hand in a single plot showing both signals. For capturing the waveforms you can use

```matlab
>> [x, wf] = GetScope(tds320, <chan>)
```

where `<chan>` is the scopes channel number.

Determine the time constant of the circuit $\tau = RC$ by fitting the theoretical solutions to your data using GUITake and its ‘Import’ button and compare with the value calculated from the nominal values of the resistor and capacitor. Also compare this calculation to the automatic measurement given by the scope to see how accurate the scope’s algorithm is.

Experiment 2: Time-domain response of follower-integrator

This experiment examines the time-domain response of the follower-integrator circuit. You will be using Classchip 2001a this week. The circuit you will be testing consists of a wide-range amplifier with a capacitor at its output. As always, there are only a limited number of chips so please be careful! The $V_{dd}$ connection is on pins 25 and 35, the ground connection on pin 15. The PadBias connection is on pin 5.

Supply a square wave to the input using the HP signal generator. The HP signal generator has limitations on the amplitude of a signal with respect to the DC offset. In order to get small signal amplitudes we will have to supply our own DC offset. We will do so by applying a DC offset with a potentiometer (about 2V) and then superimposing the output of the function generator on top of it. This arrangement is shown in Fig. 7.2. Be sure to measure the input signal at the chip – not at the function generator – because the 2kΩ resistor attenuates the signal by a factor of 2 or so. The circuit’s output is buffered by a
follower pad so you must set the Follbias knob (pin 5) to about 1V.

Place a subthreshold bias on the $V_c$ knob (pin 40); about 0.65V will do nicely. Apply a small amplitude square wave – about 100mV peak to peak when measured at the input.

NOTE: Due to an input resistance problem when interfacing the function generator with our chips, you’ll have to program the HP for half the voltage difference that you want. E.g. for 100mV peak to peak you program it for 50mV.

Adjust its frequency so that $\tau$ is about 20 per cent of a half-cycle. Display both input and output waveforms on the oscilloscope (use AC coupling). The signals will be very noisy, about 10mV of noise is normal, so you have to average several traces to get a good measurement (You can either do this using the scopes average function in the ‘acquire’ menu). Capture the averaged trace into MATLAB, plot the curves, and determine the time constant $\tau$ of the integrator. Is there any difference between the rise and fall times?

**Experiment 3: Frequency-domain response of the follower-integrator**

In this experiment you will examine the frequency-domain response of the follower-integrator. You don’t have to modify your setup at all – just use a sine wave instead of a square wave. Measure the input and output amplitudes at ten or more different frequencies. Start a decade below the cut-off frequency and take data over at least two decades, doubling the frequency between successive points.

Plot your data on a log–log graph and determine the frequency at which the gain decreases by $\frac{1}{\sqrt{2}}$ and the corresponding value of $\tau$. How does your value for $\tau$ compare with that from Experiment 2?
**Experiment 4: Large signal behavior of follower-integrator**

This experiment examines the large-signal behavior of the follower integrator and some anomalous behavior at low input voltages. Apply a large amplitude square wave (> 400mV peak-to-peak) to the integrator. Observe that the behavior is no longer exponential. Explain your results in terms of the limiting behavior of the amplifier. Plot the response, showing the linear and exponential regions. Notice that the slew rates for up and down-going signals may be different. Explain why and determine their ratio. *Hint: It is either due to the Early effect or to device mismatch!*

Leaving the amplitude of the input signal at the large-signal level, turn up the $\tau$ knob (pin 40) until the output faithfully follows the input. Now decrease the DC level of the input. Capture a bunch of traces of any weirdness you observe and come up with an explanation. Consider the useful operating range of the transconductance amplifier and bear in mind that the scope has a 1MΩ input impedance (10MΩ with a ×10 probe).

### 7.2 Postlab

1. You may have noticed a difference in the up and down-going slew rates. Do you expect this difference to show up in the rise and fall time constants for linear operation of the circuit?

2. The asymmetry in the slew rate means that for large signals, the follower-integrator output will not average to the average level of the input signal. Explain why.

3. How would running the follower-integrator above threshold change the small and large signal operation of the circuit?

### 7.3 What we expect you to remember

How to use an oscilloscope and a function generator. How to compute the time-constant of a low-pass filter and how to estimate it from the measurements. How to change the time-constant of a follower-integrator circuit.

### 7.4 Next Week

Differentiators.
Differentiators

The objectives of this lab are to:

- Examine the characteristics and limitations of the follower-differentiator circuit, the diff1 circuit, and the hysteretic differentiator.
- Examine the frequency response of the hysteretic differentiator and relate it to the theoretical transfer function.

8.1 Prelab

1. a. Derive the small-signal transfer function for the follower-differentiator (Fig. 8.1). Hint: Assume $V_{ref}$ to be zero, and do not bother about parasitic capacitances.
   
   b. Over what frequency range does the circuit differentiate? What does it do over the rest of the range?
   
   c. The range over which a reasonable differentiation occurs can be increased by decreasing the time constant $\tau$, but at what expense?

2. a. Compute the I–V relationship for the non-linear element in the feedback loop of the hysteretic differentiator shown in Fig. 8.3. $I$ is the current in the non-linear element that charges/discharges the capacitor and $V = V_{hys} - V_c$. To develop intuition, consider the case where $\kappa = 1$.
   
   b. Draw the above I–V relationship.
   
   c. How does the I–V relationship differ when $\kappa \neq 1$.

3. Sketch the response you expect at $V_{hys}$ for square wave inputs with small and large amplitudes (what does small mean?).

4. Suppose we apply a triangular wave signal to the hysteretic differentiator and increase the frequency while the amplitude remains constant. Explain how the output amplitude changes. What is the functional form?

5. Sketch the setups for the experiments.
8.2 This Week’s Test Circuits

This week we will be using classchip2001a (T18K-AQ) again. Refer to the appropriate figures for pinouts. A complete schematic with pinout can be found in the classchip handbook. Don’t forget to set the follower bias! Also, write down the number of the chip you use.

You get the simple differentiator from the follower-integrator circuit you used last week, by supplying an input to the capacitor instead of tying it to ground (Chapter 7 of Classchip2001a handbook). You will need to build the diff1 circuit out of the differentiator plus the wide range amplifier (Chapter 8 of handbook). The hysteretic differentiator is shown in Chapter 9 of the classchip handbook.

8.3 Experiments

For each of the following experiments, you will supply an input signal from the HP function generator to the chip. You must apply a DC offset of about 2V to the input with a potentiometer and then superimpose the output of the function generator through an $\approx 2k\Omega$ resistor, like you did before.

Experiment 1: Follower-Differentiator

Bias the follower-differentiator (Fig. 8.1) in subthreshold, set $V_{ref}$ to the DC level of the input, and apply a 40mV peak-to-peak amplitude square waveform as input to the circuit. Display both input and output on the oscilloscope and trigger off the HP function generator SYNC output. Change the DC level of the input and observe what happens to the output. Explain the observed behavior.

Capture a nice example of the “differentiating” behavior and determine the time constant of the circuit by fitting the theory derived in the book. Adjust the frequency of the input and
note when it stops “differentiating.”

Apply a 40mV triangle wave to the input and look at the response. Vary the frequency of the input and observe how the amplitude of the output changes. Is this what you expected?

Now, apply a sine wave to the input and vary the frequency over several orders of magnitude to get a feeling for the frequency response. The input amplitude should be less than 40mV to guarantee linear operation. Measure and plot the frequency response. Remember to measure the input signal at the chip not at the function generator. What information can you obtain from the response curve?

Experiment 2: diff1 Circuit

Bias the integrator of the diff1 circuit (Fig. 8.2) in subthreshold and the output amplifier to 2V. Use an approximately 40mV peak-to-peak waveform as input to the circuit — measured at the chip itself. Display the input and output voltage waveforms on the oscilloscope. (Connect the SYNC output of the HP function generator as before.)

Adjust the time constant of the follower-integrator so that the circuit optimally “differentiates” a triangle wave. You will need to decide what optimal means. Make a plot showing input, integrated signal, and differentiated signal. Discuss the effect of amplifier offset on the output waveforms.

Experiment 3: Hysteretic Differentiator: Qualitative Behavior

You will use the variant of the hysteretic differentiator circuit shown in Fig. 8.3 for this experiment. Begin testing the chip with a large amplitude (> 400mV) 100 Hz sine wave centered about 2V with \( V_T \) set to about 0.9V. Capture traces of \( V_{in} \) and \( V_{hys} \) and plot them on the same graph. Explain the observed responses and why the circuit is especially sensitive to changes in sign of the first derivative. Reduce the input amplitude to about 100mV and vary the frequency. Explain qualitatively what you observe.

Vary the amplitude of the sinusoidal input. You will observe a wide range of responses.
For very small signals the circuit behaves like an ordinary high-gain amplifier and for large signals it accentuates changes in the first derivative. Hand in a single plot showing four or more output traces for a range of input amplitudes. The curves may be nicely offset in MATLAB. Explain your results, quantitatively when easily possible, otherwise qualitatively, in terms of circuit behavior.

**EXTRA CREDIT: Hysteretic Differentiator: Quantitative Behavior**

Theory predicts that the derivative of the input signal will be encoded in a logarithmically compressed fashion in the amplitude of the output. Why?

Use a fixed amplitude triangular wave input (over 100mV amplitude) and vary its frequency. You may have to use DC coupling on the scope and an external coupling capacitor to get down to very low frequencies. Remember to plot the output amplitude versus frequency — not the gain. What value for $\kappa$ does the slope of your curve correspond to? What does this relate to in the circuit?

Theory also predicts that the derivative will be encoded in the slope of the output signal where it makes sharp transitions. For this experiment use a fixed-frequency triangular wave and vary the amplitude. What value of open loop gain $A$ does the slope of your curve correspond to? You need to know the period to figure this one out.

### 8.4 Postlab

1. Compare the follower-differentiator and the diff1 circuit. Which circuit is more sensitive to offsets? More compact? Has more gain?

2. How does the hysteretic differentiator circumvent the offset problems that plague the diff1 circuit? What price do we pay for this?

3. The follower-differentiator circuit and the diff1 circuit straightforwardly embody our (linear systems) concept of differentiation. The hysteretic differentiator circuit is quite a different story. In what sense does the hysteretic differentiator differentiate?
8.5 What we expect you to remember

The idea of using a lowpass filter (an integrator) to make a highpass filter (a differentiator). How the differentiator circuit is not a real differentiator but only an approximation over some frequencies defined by the time constant. How to sketch the transfer function of a differentiator circuit, showing the time constant on the sketch. How to implement a simple follower-differentiator, a diff1 circuit, and a hysteretic differentiator, using followers. Why the diff1 is a bad idea. How to estimate the time-constants of both type of differentiators and how to estimate them from the measurements. How these circuits behave when driven with large signals.

8.6 Next Week

Silicon axon-hillock circuit (integrate and fire neuron).
Silicon Neuron Circuits

In this lab, we will be concerned with the testing of a circuit that generates action potentials (spikes) based on an integrate-and-fire model of a neuron spike initiation zone.

The circuit that you will be testing contains the voltage-threshold integrate and fire circuit depicted in Fig. 9.2.

The objectives of this lab are:

1. to understand the spiking properties of I&F circuits
2. to compare the different power consumption characteristics of I&F neurons
3. to measure the limits of operation of I&F circuits
4. to evaluate the effect of the I&F circuit’s different bias parameters on its spiking behaviour.

9.1 Prelab

In your prelab analysis, try to remember that most of the results can be obtained in a few lines of calculation, if you clearly understand what it is that you’re trying to compute.

9.1.1 Passive behavior and conductances

1. What do we mean by “passive behavior” of a neuron?
2. How do we model the passive behavior of a neuron with discrete circuit elements? How do we model it in VLSI?
3. Which are the relevant conductances involved in the spike-generating mechanism? Which one implements a positive feedback and which one implements the negative feedback?
4. In theoretical, mathematical and numerical simulations positive feedback is usually cause of major problems (diverging equations, overflow, etc.). Why does the positive feedback work without causing problems both in real neurons and silicon ones?
9.1.2 Power dissipation

Inverters, implemented using CMOS technology, dissipate power every time they switch. If the input to an inverter switches quickly, power dissipation is low.

1. Why is power dissipation a concern for the axon-hillock circuit?
2. Which inverter in the circuit Fig. 9.1 is the one that dissipates on average more power?

9.1.3 FI-curves and Refractory Period

1. What is the refractory period?
2. Why is there a refractory period in spikes generated by real neurons?
3. What is an FI curve?

Draw a typical FI curve, for three different refractory period values. Qualitative plots will do. You don’t need to specify numbers on the axes.

9.2 Experiments

For testing the axon-hillock circuit, you will be using chip2001a again. The pinout for the neuron circuit is shown in the chip handbook, or you can look on the whiteboard when you get to lab for a suggested setup.

Experiment 1: The Voltage-threshold I&F Neuron

In this experiment you will need to find the bias parameters of the circuit such that it will model a real neuron’s behavior as realistically as possible. You will be using chip
Figure 9.2: Integrate and fire neuron with controllable threshold and refractory period.

2001a. Refer to the Fig. 9.2 for the circuit schematics. (The circuit shown in Fig. 9.2 is actually slightly different from the one on the chip. Do you see what is different?)

9.2.1 Single spike plots

In this experiment we will look at the shape of one single action potential. Use the oscilloscope to view time evolution of $V_{\text{mem}}$. Capture and plot three traces of $V_{\text{mem}}$ for three different values of $V_{\text{pw}}$. Plot everything in the same figure and find values of $V_{\text{pw}}$ such that the differences are visible on the plot.

To capture and plot scope traces (e.g. from the scope’s channel 1) in matlab use the commands:

$$[t, sp] = \text{GetScope}('/dev/gpib0/tds320', 1); \text{plot}(t, sp);$$

9.2.2 FI curves

In this experiment we will compute the frequency of the spikes generated by the circuit, as a function of input current and bias voltages.

First fix $V_{\text{pw}}$ to a reasonably high subthreshold value (e.g. around 0.8V). Set $V_{\text{fr}}$ to a relatively low subthreshold value (e.g. around 0.4V) and by changing $V_{\text{in}}$ manually find the limits of the FI curve: at which value the neuron begins to spike, and after what value the frequency of the spikes stops increasing (saturates). Then connect $V_{\text{in}}$ to the Keithley 230 (and disconnect it from the pot), so that you can supply well-controlled input voltages. At this point measure the frequency of the spikes for at least 10 (but more are better) values of $V_{\text{in}}$ in the range you just found. You can use the scope’s measuring function to measure the frequency. Save both input voltage and frequency values in two vectors (within Matlab), and repeat the same procedure for 2 different values of $V_{\text{fr}}$. Set the different $V_{\text{fr}}$ values in a neighborhood of the first $V_{\text{fr}}$ setting, such that the ranges of valid $V_{\text{in}}$ voltages are approximately the same.
After you collected all the data, plot on the same figure the three curves. Assuming the input current $I_{in}$ changes exponentially with $V_{in}$, you should plot the curves on a semilog scale:

```
semilogx(Vin1,Fout1,Vin2,Fout2,Vin3,Fout3).
```

To place legends on the plot use the command “legend”:

```
legend('V_{ref}=0.35V','V_{ref}=0.4V','V_{ref}=0.45V').
```

Note: the values specified here are not necessarily the best values!

### 9.3 Postlab

The FI curves measured in the lab saturate because of the refractory period effect. Is there any other way of making the FI curves saturate? Would the FI curves saturate if you measured them from the plain Axon-Hillock circuit in Fig. 9.1?

The I&F circuit you used to measure spikes in this lab (see Fig. 9.2) differs from the one described in the class; the transconductance amplifier is of opposite polarity. Does this make any difference? If so explain why.

### 9.4 What we expect you to remember

What is a neuron and what are its components (synapse, soma, dendrite)? What types of models are used to simulate neurons? How does the spike-generating mechanism work? What is an FI curve? Can you draw the circuit schematic of the axon-hillock neuron?

See you next year.

### 9.5 Next Week

Device physics of learning mechanisms in silicon.
Tunneling and Injection

Biological systems have the ability to adapt to their environment. This adaptation happens over an enormous range of time scales. Short-term changes in the properties of cells can be brought about by storing charge on the membrane capacitance of a neuron, or by making conformational changes in certain molecules. These changes happen over millisecond time scales or less. There are many kinds of adaptation that happen at longer time scales. For example, we know that short-term memory must be due to changes somewhere in the brain that last of the order of minutes or hours, even though we don’t know exactly what those changes are or where they occur.

We refer to this behavior as learning or adaptation. We like to think that at some level, storing charge on a capacitor is not so different from memorizing a grocery list.

How can we make circuits that adapt? We already know how to store information for short times — by storing charge on a capacitor. But what about making changes that last minutes or hours? This lab will introduce a technique we use to make long-term changes to a circuit.

This lab will present two methods for moving charges to and from an electrically-isolated (floating) node in a circuit. By configuring the floating node as the gate of an MOS transistor, the stored charge can then be sensed as transistor channel current or channel conductance. The first technique for changing the amount of charge on a floating node uses the quantum-mechanical process of electron tunneling; this method is effective at removing electrons from a floating gate. The second technique involves injecting thermally ‘hot’ electrons from the silicon substrate into the conduction band of the silicon dioxide gate insulator; this technique is efficient at adding electrons to the floating node. The two processes together give us the ability to both add and subtract charge from a floating node. By means of a simple circuit, we can convert this stored charge to a precise, non-volatile rail-to-rail output voltage.

10.1 Prelab

1. Floating nodes in MOS technology (thermal equilibrium): We use an isolated piece of polysilicon as a floating node; it is entirely surrounded by silicon dioxide (SiO₂). How good an insulator is SiO₂? Well, we know that an electron requires an energy boost of about 3.2eV to enter the conduction band of SiO₂ from the conduction band of silicon. The band-gap is fixed at about 3.2eV, so we’ll get a leakage current through the oxide of $I_{\text{leak}} = I_0 \exp\left(-\frac{3.2eV}{kT}\right)$, where $I_0$ can be found approxi-
mately as follows:

We assume that at a barrier height of zero, all of the electrons in the vicinity of the barrier pass it. So we need to know the size of the device, the concentration of the electrons, and the velocity of the electrons. Thus,

\[ I_0 = qNAtv \]

where \( I_0 \) is the electron charge, \( q \) is the concentration of free electrons in the capacitor plate, \( A \) is the area of our capacitor plate, and \( v \) is the average thermal velocity of the electrons in the capacitor plate.

Compute the room-temperature leakage current from a typical floating node, where

\[ A = 2 \times 10^4 \mu m^2 \]
\[ N = 10^{19} \text{ electrons per cm}^3 \]
\[ v = 10^6 \text{ cm per second} \]
\[ kT = 0.026 \text{ eV} \]
\[ \text{thermal voltage at 30°C} \]
\[ \text{thermal voltage at 30°C} \]

The above estimates for values are very approximate, but it won’t matter much.

2. Figure 10.1(a) shows the circuit symbol for a differential amplifier. As its name suggests, a differential amplifier (or commonly known as an opamp) amplifies the voltage difference between the two inputs. Mathematically we write

\[ V_{out} = A \left( V_{in^+} - V_{in^-} \right) \]

(10.1)

where \( A \) is the amplifier gain. As we have seen in previous labs, this gain is usually quite large.

(a) Figure 10.1(b) shows a differential amplifier hooked up in a follower configuration. Explain both intuitively and analytically why the output voltage nearly
Analog VLSI Lab 10, 2001–2002

(b) Figure 10.1(c) shows a differential amplifier with a battery of voltage $V_c$ in the feedback loop. Again assume the amplifier gain is much larger than one. First, for three different values of $V_c$ (say $V_c = 0V$, 1V, and 3V, for instance), sweep $V_{in}$ from ground to +6V. Draw a graph of $V_{out}$ vs. $V_{in}$, labelling salient features, including the slope of the linear part of the curves. Second, for a fixed $V_{in}=5.5V$, sweep $V_c$ from ground to 4V. Draw a graph of $V_{out}$ vs. $V_c$, labeling salient features.

3. Figure 10.1(d) shows the amplifier circuit which is equivalent to the circuit you will use in this lab. The inputs to the differential amplifier are gates of nFET transistors; therefore the transistor’s gate is part of the floating gate. The circuit is fabricated with the same polysilicon gate completely surrounded by $SiO_2$, and hence, does not have any direct electrical connection with anything. The circuit is functionally identical to the circuit of Fig. 10.1(c), with the battery replaced by a capacitor whose voltage is given by $V_c = Q/C$.

(a) Add a $p$FET transistor to this circuit, such that electrons can be added to the floating node. Describe (in words) how electrons are added to the floating node by hot-electron injection.

(b) Assume that the initial quantity of charge on the floating gate is such that $V_{out} = 5V$. If electrons are then added to the floating gate at a constant rate (i.e., a constant current through the oxide), what happens to $V_{out}$? Draw a graph of $V_{out}$ vs. time, labeling salient features.

(c) Now add a tunneling junction to the circuit, such that electrons can be removed from the floating node. Describe (in words) how electrons are removed by tunneling.

(d) Assume that the initial quantity of charge stored on the floating gate is such that $V_{out} = 7V$. If electrons are then removed from the floating gate at a constant rate, (i.e., a constant current through the oxide), what happens to $V_{out}$? Draw a graph of $V_{out}$ vs. time, labeling salient features.

(e) If you have a graph of $V_{out}$ vs. time such as the ones from parts (b) and (d), how can you obtain the current through the oxide that gave rise to the change in $V_{out}$?

(f) Why is it reasonable to assume that the oxide current due to tunneling and injection is constant in this circuit?

4. Application of a high voltage to a CMOS gate: Figure 10.2 shows an RC-lowpass filter. Sketch the time response of $V_{tan}$ to an instantaneous step in $V_{in}$ from ground to $V_o$. Label salient features in your sketch, such as the time constant $\tau$ and the maximum value for $V_{tan}$.

5. Tunneling: Quantum mechanics tells us that an electron’s wave-function extends spatially somewhat beyond a barrier. If the barrier is thin enough, then, there is a reasonable probability that the electron will cross to the far side of the barrier. This process is called tunneling. A simple version of the theory for a square barrier of
height $\delta E$ and thickness $d$ gives the probability of an electron reaching the far side of a barrier as

$$P = \exp\left(-2d\sqrt{\frac{2m_e\delta E}{\hbar^2}}\right)$$  \hspace{1cm} (10.2)

For $\delta E = 3.2 \text{ eV}$, compute the “thinness” required to give a probability of 0.5. The electron mass $m_e$ is $5.7 \times 10^{-12} \text{ eV s}^2/\text{m}^2$ and $\hbar$ is $6.6 \times 10^{-16} \text{ eV s}$.

The gate oxide thickness in our fabrication process is about 43 nm. This is much too thick to have a significant tunneling probability, so how can we use tunneling at all? We have already seen that electrons can travel through SiO$_2$; we need not tunnel all the way to the other side of the oxide layer if we can somehow arrange for the electrons to tunnel into the oxide conduction band. This is called Fowler-Nordheim tunneling, and it happens when we apply a large enough electric field across the oxide. Draw a band diagram of this process.

From the band diagram, we see the electrons must tunnel through a triangular barrier. The probability of an electron tunneling through the potential barrier defined by $V(x)$ can be approximated by

$$P = e^{-\frac{2m_e}{\hbar^2} \int_{a}^{b} \sqrt{V(x)-E} \, dx}$$  \hspace{1cm} (10.3)

where $E$ is the starting electron energy, $a$ is the starting position of the barrier, and $b$ is the final position of the barrier at the electron energy. Assuming that the electrons start at the conduction band, derive the tunneling probability using this approximation. In addition, plug in the above parameters for the tunneling probability.

### 10.2 This Week’s Test Circuits

This week you will test a non-volatile analog memory cell. You will spend time familiarizing yourselves with the circuit, and with the tunneling and injection processes.

The circuits are on the chip (N7CKHV). Write down the number of the chip you are using.

A partial schematic of this chip is shown in Fig. 10.3. This circuit which can be used as a simple floating gate memory cell, consists of a capacitively fed-back amplifier, an FG.
programming transistor, and a tunneling control. Look at Fig. 10.3 and label the floating

gate. Do you see how the floating gate voltage can be controlled? Do you recognize the FG
pfET? Do you see the tunneling node?

Please be very careful with these chips since they are even more sensitive to static discharge
than the ones we used so far.

10.3 Experiments

Be sure to wire everything up, set the biases on the potbox, and have your setup checked by
a TA, before you insert the chip.

The experiments push the tunneling and injection structures close to their limits. In addition,
for all practical purposes the inputs have no static protection. The tunneling inputs have
only a 75 kΩ resistor to ground. The injection transistor drains are brought directly to a pad
with only a couple of protection diodes. These structures can thus very easily be destroyed
by static electricity or switching transients, so be VERY CAREFUL! Read the directions
before beginning the experiment, and stick to the following procedure to set up the injection
and tunneling inputs:

- Do not apply more than 11V to the pFET injection transistor’s drain or source. The
  junctions will be irreversibly damaged at voltages higher than this.

We will use the Keithley 230 Programmable Voltage Source to apply high voltages to the
tunneling junctions via an RC-lowpass filter. Build such a filter using a 1 kΩ resistor and a
10 µF capacitor (cf. Prelab). (This RC filter reduces the amplitude of overshoots and un-
dershoots from the Keithley when one punches in an input voltage that is a large difference
from the present voltage from the Keithley.) Do not put the chip in yet! Use the Matlab
command \texttt{tunv <voltage>} to set the K230 Source. Test your filter setup by applying a high
voltage, say 20 V, and measuring its output with the Fluke. After this works correctly, do
not touch the OUTPUT OPERATE button anymore during the experiments, but leave the
output enabled; if it gets disabled, the discharge from the coaxial cable may damage the
tunneling gate. Set the voltage (using \texttt{tunv}) to 0 V before inserting the chip. When the
experiments are over, reset the 230 to 0 V and disconnect it from the tunneling input.

Connect \(V_{\text{tun}}\) (pin 23) to the output of the RC filter through an additional 1 kΩ resistor as
shown in Fig. 10.2. This resistor will limit the current from the capacitor to the chip. (Make
sure the output of the 230 is at 0 V and OUTPUT OPERATE is on).

- Never exceed 30 V on the tunneling line, otherwise you will destroy the gate oxide.

- Do not touch the chips unless your other hand is grounded to the potbox.

- Do not touch the OUTPUT OPERATE button during the experiments. Use the Matlab
  command, \texttt{tunv}. 
For this experiment we will use the circuit shown in Fig. 10.3. Before inserting the chip, make all necessary connections and set all the used pots.

Set $PV_{dd}$ (pin 35) and $CV_{dd}$ (pin 25) to 10 V (from the power supply) and **limit the current to 80 mA**. Connect Gnd (pin 15) on the chip. Switch on the potbox and set $Padbias$ (pin 5) to 0.9 V. Tie the source (pin 22) and well (pin 20) of the pFET together; these are $V_{inj}$. Connect pins (21,24,26,4) to ground.

Turn on the Keithley 236 SMU and set it for the V-I mode (that is, source a voltage and measure the current) from the front panel. Put the Keithley in the continuous mode and set the voltage to 5V. Tie the BNC voltage output of the SMU to Gnd. Connect the pFET source, $V_{inj}$ (pin 22), to the Triax + of the Keithley 236 SMU. Connect the input voltage of the transconductance amplifier, $V_{inp}$ (pin 19) to 5V. The output voltage of the amplifier $V_{out}$ (pin 18) should be connected to the scope.

If you have read everything so far and the TA has checked your setup, switch off the potbox, but not the 230. Now insert the chip. Switch the potbox back on and check the current of the power supply. It should not be significantly higher than 70 mA. Use the MATLAB program, **tunv <voltage>** to apply a tunneling voltage from the K230. The program limits the maximum voltage to 32V. Do not touch the front panel of the K230. First, apply about 20 V to the tunneling line and check that the current has not increased. You will not get appreciable tunneling up to 20 V but switching the tunneling line from 20 V to 28 V induces much smaller capacitive coupling transients than switching the tunneling line from 0 V to 30 V. It also reduces the stress on the oxide. So it is best to leave the tunneling voltage at 20 V for the tunneling “off” state. **BUT put it back to 0 V before changing the tunneling connection or TAKING THE CHIP OUT OR SWITCHING THE POTBOX OFF!**
Select DC coupling on the scope and set the Vertical Offset for the scope trace of $V_{\text{out}}$ to 1 V. Your chips are likely to have a significant amount of residual charge on the floating gate (left there from the fabrication process or previous lab sections). This means the output may be stuck at a low or high voltage. To initialize the chip, you must first remove this charge by means of either tunneling or injection. If the cell output is stuck low, then you must inject it up. If it is stuck high, then you must tunnel it down. When tunneling, 28 V on the tunneling line should be sufficient for a good tunneling rate. Be patient — it may take a while to remove all the charge. When injecting, make sure the tunneling line is at 20 V. Then, set $V_{\text{inp}}$ (pin 19) to about 5.25 V. Turn up $V_{\text{inj}}$ by rotating the knob on the K236 until it reaches about 10 V. If the output voltage does not increase, slowly increase $V_{\text{inp}}$ and monitor the source current. The source current should not be more than 1 mA. The injection should turn on at some point. Begin your experiments once $V_{\text{out}}$ reaches 1 V. Turn off both the tunneling or injection process.

**Experiment 1: Measuring Injection and Tunneling Current**

Set the time scale of the scope to 2.5 s/div. Observe the value of $V_{\text{out}}$ on the scope. Familiarise yourself with the voltages needed for turning on the tunneling mechanism or injection mechanism. Given that $C=2\text{pF}$, how do you compute the tunneling or injection current? Move $V_{\text{out}}$ by a few 100mV up by hot electron injection and down by a few 100mV by tunneling (use the tunv program).

**Experiment 2: pFET Injection**

Increase the sensitivity and the offset settings of the scope such that you cover the whole signal range you will expect. Set the time scale of the scope to 2.5 s/div. Now measure the slope of the scope trace of $V_{\text{out}}$ for five different values of $V_{\text{inj}}$ between 10 V and 11 V (Hit the RUN/STOP button on the scope once you have enough data on the scope to measure the slope). For each value of $V_{\text{inj}}$, record the source current, $I_{\text{transistor}}$ through the transistor, $M_1$. Do not change $V_{\text{inp}}$ between the different values of $V_{\text{inj}}$. Compute $I_{\text{inj}}$ from the slope of the curve on the scope. After each measurement, decrease $V_{\text{out}}$ down to about 1 V by turning on the tunneling process (and turning off the injection!). Adjust the sensitivity and time scale as needed when increasing $V_{\text{inj}}$. Be careful not to reach $V_{\text{out}}$ values higher than 8 V during injection, since the slope of $V_{\text{out}}$ starts to flatten in this region. Finally compute and plot the injection efficiency ($I_{\text{inj}}/I_{\text{transistor}}$) as a function of the source current, $I_{\text{transistor}}$.

Is the injection current proportional to the source current?

**Experiment 3: Gate Oxide Tunneling**

Set $V_{\text{out}}$ to about 5 V by tunneling or injecting and then turn off tunneling as well as injection ($V_{\text{inj}} = 5 \text{ V}$ and $V_{\text{tan}} = 20 \text{ V}$). Now turn on the tunneling and measure the slope of $V_{\text{out}}$ for five different values of $V_{\text{tan}}$, between 27 V to 30 V. Compute and plot the tunneling
current as a function of the oxide voltage $V_{\text{tun}}$ across the tunneling junction. Fit the curve to the theoretical function

$$I = I_0 e^{-\frac{V_o}{V_{ox}}}$$

(10.4)

and record the model parameters $I_0$ and $V_o$ that best fit the data. What is the physical significance of $I_0$ and of $V_o$? Does the model reasonably fit the data? Make a semilogy plot of the oxide current versus $1/V_{ox}$ with a linear curve fit, labeling it with $I_0$ and $V_o$.

### 10.4 What we expect you to remember

How do tunneling and injection mechanisms work? What is the shape of the energy band diagram in the channel and oxide during tunneling and injection? How are the memory cell circuits used to control tunneling and injection?

### 10.5 Next Week

Silicon synapses.
Synapse Circuit

In Lab 9, we tested an I/F neuron circuit, where the current to the neuron was provided by a current source. This week, we will look at the firing characteristics of a neuron when stimulated through a synapse and at the firing properties of an adaptive I/F neuron.

The objectives of this lab are to:

- Characterize a silicon synapse.
- Characterize an adaptive I/F neuron.

11.1 Prelab

1. For a circuit consisting of a capacitor and a diode-connected nFET in parallel, as shown in Fig. 11.1, write the differential equation for the output current $I_{out}$ as a function of the input current $I_{in}$, the gain voltage $V_g$, and the capacitance $C$. Solve for the output current, when there is a step change in the input current. Draw a plot of $I_{out}$ versus time.

2. Write the corresponding equation when the input current is switched off.

11.2 This Week’s Test Circuits

This week we will be using the chip (N9BK-AR). The pinouts of the circuit are shown in Fig. 11.2.

11.3 Experiments

Experiment 1: AnaLog simulation of synapse circuit

We first simulate the behavior of the synapse circuit using AnaLog.\(^1\)

\(^1\)Remember, if AnaLog won’t start and you get some error about colormaps, it may be because your machine is set up to run X with too few colors, or some of the colors are already used up by running netscape
Copy over the file `classsyn.lgf` from the `~avlsi/lab11` directory. The input current to the synapse consists of two transistors in series; one is driven by the presynaptic input \( f1b \) and the other sets the synaptic weight \( syn\_wt \). Make the value of the capacitor around 300fF. Stimulate the circuit with a pulse train \( f1b \) of period 4ms and pulse width of 500\( \mu s \). Set \( syn\_wt \) to 4.4V and the gain of the synapse, \( Gain \), to 0V. Measure the steady-state current value of \( I_{out} \).

1. Change the gain of the synapse. How does the \( Gain \) voltage affect the output current?

2. Change the synaptic weight, \( syn\_wt \). How does the output current change as function of \( syn\_wt \)?

3. Change the period of the pulse train, \( f1b \). How does the output current change as function of the frequency of the pulse train?

Next, we connect the synapse circuit to the neuron circuit from Lab 9. Copy over the file `classneuron.lgf` from the `~avlsi/lab11` directory. The synapse circuit is now of opposite type so that synaptic current charges up the membrane. Set \( syn\_wt \) to 0.3V and the gain of the synapse, \( Gain \), to 4.9V. Set the presynaptic input \( f1 \) so that it is a pulse train with a period of 4ms and pulse width of 500\( \mu s \). Set \( syn\_wt \), \( Refr \) and \( Pw \) so that you get a firing frequency of around 200Hz and a pulse width of approximately 500\( \mu s \).

1. Plot the output spiking frequency as a function of the input spiking frequency.

Lastly, we look at an adaptive neuron. The adapting synapse for the neuron is similar to the input synapse circuit (see Fig. 11.2). The input to the adapting synapse comes from the first. Try quitting netscape and then starting Analog. Try quitting and restarting X this way: `startx -bpp 8`. 
neuron’s spiking output. Copy over the file classadapt.lgf from the \texttt{~avlsi/lab11} directory.  

Turn the input synapse circuit into a constant current source by setting the input \( f1 \) to 5V, \( \text{syn}_{\text{wt}} \) to 0.4V, and the gain of the synapse, \( \text{Gain} \), to 5V. Set the initial biases to the adapting synapse as follows: \( V_q \) to 4.4V, the gain of the synapse \( \tau_u \) to 0.2V, and the cascode bias \( V_{\text{cas}} \) to 0V. Change \( \text{syn}_{\text{wt}} \) so that you get an output frequency of 200Hz.  

Switch off the input current by setting \( f1 \) to 0V. Set \( V_{\text{cas}} \) to 2.5V so that the adaptive synapse will be turned on. Now turn on the input by setting \( f1 \) to 5V. See how the output frequency of the neuron changes over time. Also monitor the node \( \text{vadap} \). How does the adaptive property of the neuron change as a function of \( \tau_u \), and \( V_q \)?

**Experiment 2: Synapse circuit**

Before inserting the chip into the potbox, current-limit the power supply and wire up all the necessary pins, as shown in Fig. 11.2. Connect pin 15 to ground, pins 25 and 35 to \( V_{\text{dd}} \) and \( \text{Padbias} \) (pin 5) to a pot (0.9V). Also hook up pins 7, 8, 10, 11, 13, 14, 16, 19, and 20 to \( V_{\text{dd}} \) and pins 1, 3, 6, 9, 12, 17, 18, 24, 26, 29, and 40 to ground.  

Now bias the following pins for the neuron and synapse circuits by using the pots: the biases to the neuron, \( V_{\text{thresh}} \) (pin 23) to 2.5V, \( V_{\text{pw}} \) (pin 2) to 0.7V, and \( V_{\text{ref}} \) (pin 22) to 0.8V; the biases for the adapting synapse, \( V_{\text{gain}} \) (pin 4) to 0V, \( V_q \) (pin 21) to 5V, and \( V_{\text{cas}} \) (pin 28) to 0.9V (Note: pin 28 also drives the follower bias for the output signals, for example, the membrane potential of the neurons); the biases for the input synapse, \( V_{\text{syn}} \) (pin 27) to 5V, \( \text{syn}_{\text{wt}} \) (pin 39) to 0.8V, and \( V_{\text{cas}} \) (pin 38) to 3.5V. Hook up the input to the synapse (pin 34) to the output (pin 6) of a monostable chip (MC14538B) on your potbox. The input to the monostable comes from the function generator (this chip is already hooked up). Switch on the function generator and adjust it so that you get a square wave output from 0V to 5V with a duty cycle of 20\% and a frequency of 1kHz. The output of the monostable is a square wave with a fixed pulse width regardless of the input frequency. Switch off the potbox and insert the chip.  

Look at the membrane potential (pin 33) and the spike output (pin 32) of the I/F neuron on the scope. Use the “Peak Detect” mode in order to catch all the short spikes on the scope trace. Adjust \( \text{syn}_{\text{wt}} \) so that you get an output spiking rate of about 100Hz. How does the output frequency depend on the presynaptic frequency, the synaptic weight and the synapse gain? Measure the spiking frequency of the neuron in response to different presynaptic spiking frequencies for a fixed synaptic weight and gain. Compare the outputs of the chip with the simulation outputs.

**Experiment 3: Adapting neuron**

We now turn on the adaptation of the neuron by setting the biases for the adapting synapse, \( V_{\text{gain}} \) (pin 4) to 0.19V, \( V_q \) (pin 21) to 4.4V, and \( V_{\text{cas}} \) (pin 28) to 3.0V. We also change the biases to the input synapse so that it acts like an input current source. To do this, connect the presynaptic input (pin 34) and \( V_{\text{syn}} \) (pin 27) to \( V_{\text{dd}} \). Adjust \( \text{syn}_{\text{wt}} \) (pin 39) so that the adapted output frequency is around 500Hz. Now give a step input current to the neuron.
by connecting pin 34 directly to the function generator. Set the frequency to 1Hz and the duty cycle to 50%. Fine-tune $V_g$, such that the spike-frequency adaptation can nicely be seen on the scope. Submit a plot showing the adaptation in the neuron’s frequency over time after the step input. How do the adaptation dynamics change as a function of $V_{gain}$ and $V_q$? How does the steady-state frequency change as a function of $V_{gain}$ and $V_q$?

### 11.4 Postlab

1. Compare the simulation results and the experimental results. What are the differences?

### 11.5 What we expect you to remember

The schematic for a synapse circuit. How the synaptic current changes as a function of the presynaptic frequency and the synaptic weight. How the firing frequency of an adaptive
neuron changes as a function of the presynaptic frequency and the biases to the adapting synapse.

11.6 Next Week

Photoreceptors.
Photoreceptors I: Phototransduction and Receptor Circuits

These next two weeks we will be concerned with visual transduction by silicon. Our work will differ fundamentally from all the experiments we have done so far, in that our chip will interact with the world through light, and not through an electrical signal.

The object of this and the next lab is to obtain practical experience in working with light and silicon, and with a well-studied photoreceptor circuit, so that if you ever want to design your own circuits with integrated, continuous-time receptors, you’ll know several useful things and the practical problems involved in the interaction of light with silicon.

In this lab, you will examine the static properties of light interacting with semiconductor junctions and devices. Specifically, you will measure

1. quantum efficiency of a junction
2. generation of electrical power from light
3. properties of a parasitic vertical bipolar transistor
4. static properties of a simple non-adaptive logarithmic photoreceptor

12.1 Prelab

Read this lab handout carefully and plan your experiments in detail, including circuit diagrams and voltage ranges.

The prelab is important to help guide your measurements. In your prelab analysis, try to remember that most of the results can be obtained in a few lines of calculation, if you clearly understand what it is that you’re trying to compute.

Also in this lab we will look at a non-adaptive photoreceptor circuit which transduces optical signals into usable electrical signals for visual sensory processing. We will study a simple logarithmic photoreceptor circuit called the source-follower receptor. This circuit is a bridge to understand another photoreceptor circuit, the adaptive photoreceptor, which will be discussed next week.
12.1.1 Junctions and Photocurrent

Draw a schematic of a semiconductor junction. (For concreteness and to help you think about the lab you will be doing, you can draw the junction as an n–type source-drain diffusion sitting on a p–type substrate, because we’ll be using an n–well chip.) Draw the p and n regions, along with the depletion regions. Draw an arrow showing the electric field in the depletion region. Draw the electron potential energy diagram. Now imagine that a photon generates a hole-electron pair in the n region. What happens to the majority carrier? What happens to the minority carrier? (There are two possibilities for the minority carrier.) Now suppose the pair is generated within the depletion region. Now what happens? Finally, what happens to the pair if they are generated in the p region?

Imagine that the junction is open, so that the p and n regions are not shorted together. Now we shine light on the junction. What happens to the voltage between the p and n region? What is the sign of the voltage?

Now imagine that the junction is shorted, so that the p and n regions are at the same voltage. Now shine light again. Does a current flow? If so, which direction is the current?

Draw the expected I–V curve for the junction, in the absence and presence of light. Where do we operate the junction to generate the most power from it?
12.1.2 Source-Follower Receptor Circuit

Logarithmic photoreceptors have a property that makes them good for sensory perception. Why does the logarithmic response make them useful?

One of the simplest logarithmic photoreceptors, called the source-follower receptor, is shown in Fig. 12.1. Sketch a plot of the expected voltage, $V_{in}$, as a function of irradiance, for a constant bias voltage. What is the slope of the response?

12.1.3 Bipolar Junction Transistors

A bipolar device is basically a sandwich of three semiconductor layers, either P-N-P or N-P-N. The middle layer of these semiconductor sandwiches is called the base; the other layers are called the emitter or the collector, depending on their bias voltages. The region that is forward biased with respect to the base is called the emitter and the other region, which is assumed to be reverse-biased with respect to the base, is called the collector. When the device is biased in this fashion, carriers in the emitter region are injected into the base and then swept into the collector.

A good PNP device will be designed such that most of the holes injected into the base from the p-type emitter end up in the collector. Also, the concentration of electrons in the n-type base is made very small so that the number of electrons that are injected into the emitter via the forward-biased emitter-base junction is negligible. With very few electrons leaving the base and a long lifetime for minority holes, only a little base current is required to maintain a large current from the emitter to the collector.

1. Draw the circuit symbol for a PNP bipolar transistor, label the terminals and the currents, and show how you will bias the device by hooking it up to voltage sources.

2. Draw an energy diagram for the transistor and explain how conduction occurs. Are the carriers holes or electrons?

3. Compare your energy diagram with that for a MOSFET and pair up the terminals, i.e. base is to gate as...

4. The base current is made up of two components: the electrons that recombine with injected holes in the base, and the electrons that are injected into the emitter. How would you minimize these currents relative to the collector current? Consider changing the base thickness, the base doping, and the emitter doping.

12.2 Experiments

The devices and photoreceptor circuits that we will be testing in this lab are on cns182recep93, N3AB JC1. A partial schematic of the chip is shown in Fig. 12.3.
Some of the circuits are instrumented with well-type followers. You will need to bias the follower ($p\text{ follbias}$, pin 14) to see the output of the adaptive receptors, as well as the usual pad follower bias on pin 40. The adaptive elements and the photodiode use barepads with no static protection so please exercise some caution when handling the chips. You will be testing the following circuits:

1. the photodiode with pin 17 output.
2. the parasitic vertical bipolar transistor, with base pin 9, emitter pin 8, and collector Gnd.
3. The simple source-follower log receptor with output on pin 21. The source-follower bias is pin 20 and the well-type follower is biased with $p\text{ follbias}$, pin 14.

Since you will be using the chips with the lids taken off, we have taped little microscope coverglass slides on top of the chips. *When you slide light filters over the chip, be careful not to catch the filters under the edge of the glass. It is really easy to pull off bonding wires.*

We will supply you with the following equipment for this lab:

1. LED holders which fit over the 40 pin ZIF sockets.
2. Neutral density filter strips, consisting of 1, 2, 3 and 4 decade filters.
3. Resistor pairs and red LEDs.

**Experiment 1: Quantum efficiency of a photodiode**

The absolute quantum efficiency is defined as the number of collected electrons per incident photon. In this experiment, we’ll measure the absolute quantum efficiency of a simple semiconductor junction. You may discover that an absolute measurement can be difficult.

Using the photometer, along with the calibrated pinhole and the LED holder, measure the irradiance of a red LED, in units of W/m². (The irradiance is defined as the power per unit area incident on a surface.) The pinhole is 1/226 the area of the photometer. Power the LED with a 200 ohm resistor in series with the chip power supply. The photometer has a wide spectrum sensor with a flat response from 450 to 950nm.

We will supply you with pairs of 200 and 1500 ohm resistors, soldered together with female connectors at each of the three terminals. You can use these resistors to power the LED (with the 200 ohm resistor) and also to inject a small signal on top of the steady intensity by using the function generator (with the 1500 ohm resistor).

Now measure the current produced in the photodiode with an appropriate bias voltage. (What is appropriate?) Use the LED holder to position the LED over your chip in a stable position.
Repeat the entire measurement with the green LED shown in the table below.

Compute the absolute quantum efficiency. The size of the opening in the metal2 shield on top of the photodiode is 18 by 11 microns, giving an area of 198 square microns. The size of the source-drain p-type diffusion is 14 by 7 microns, which is an area of 98 square microns. Which dimension is important, in your opinion?

The LED’s peak spectral outputs are shown in the following table. All have a spectral half–width of less than 50 nm.

<table>
<thead>
<tr>
<th>COLOR</th>
<th>WAVELENGTH (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Red</td>
<td>635</td>
</tr>
<tr>
<td>Green</td>
<td>565</td>
</tr>
</tbody>
</table>

The energy of a photon is $h \nu / \lambda$. A useful form is $1.24 eV / \lambda$, if $\lambda$ is measured in $\mu m$.

1. Why do these devices have the measured spectral response? Consider the relative absorption lengths of different colors of light in silicon, the effectiveness of photons of different colors in producing an electron-hole pair, and consider what happens to a pair after it is produced.

2. How would the quantum efficiency change if you used a $p^+$ photodiode sitting in a $n$-well, instead of one sitting over the substrate? What happens to the electron hole pairs that are generated in the substrate? What wavelengths contribute to the generation of the electron-hole pairs in the substrate? Would the current from the $p^+$ node be larger or smaller than the $n^+$ node in the $pn$ photodiode in this experiment? How do imager manufacturers use this property?

**Experiment 2: Photogeneration of electrical power**

In this experiment, we will study how power can be generated by light absorption. The experiment consists of taking an I-V curve for the junction under illumination.

Take off the cover over your setup so that the chip is illuminated by the fluorescent lights in the room. Take an I-V curve of the junction over the relevant region of operation. (The lights flicker at 100 Hz, but the electrometer will average over these ripples.) Measure the irradiance of the chip.

Questions:

1. What is the power efficiency? By that we mean the power the device can generate per unit incident power.

2. Approximately how much power can you generate with the small photodiode (20 $\mu m$ by 20 $\mu m$) on the chip, under room fluorescent light? About how much power can you generate under room light and under sunlight using 1/4 of a TinyChip (an area of 1 square mm)?
Figure 12.2: Parasitic vertical bipolar transistor.

Experiment 3: Current gain $\beta$ of the phototransistor

Figure 12.2 shows a cross-section through one of these parasitic vertical bipolar transistors for an $n$-well chip. The emitter is $p^+$ diffusion (ordinarily the source/drain for MOS devices in the well), the base is the $n$–well, and the collector is the $p^-$ substrate. These transistors are operated by default with the collector connected to ground.

With no light shining on the chip, measure the base $I_b$ and emitter $I_c$ currents as a function of $V_{bb}$. Fit appropriate regions of the graph, and discuss the fits you obtain. $\beta$ is defined as the ratio of the collector current to the base current. Calculate and plot this ratio both for your data and the fits to the data. Remember that $I_c = I_c + I_b$.

Questions:

1. Does $\beta$ change with current level?
2. If the base width, $W$ is $5\mu m$ (it is about that) then based on the measured $\beta$ what is the minority carrier diffusion length, $L$? (Use the following equations: $L = \sqrt{D\tau}$, $\beta = \frac{2D\tau}{W^2}$. where $D$ is the diffusion constant, $\tau$ is the time constant.)

Now, let the base terminal float. Use the red LED to shine a constant amount of light on the chip. Measure the photocurrent going into the emitter for four orders of magnitude of light intensity (use the neutral density filters to attenuate the light from the LED). Plot the resulting photocurrent vs relative intensity (in log units) on a semilog scale. What is the slope of the curve?

Experiment 4: Source-follower receptor

Verify qualitatively that the simple source-follower receptor works correctly by observing the output voltage. The voltage should be below the source-follower bias voltage (towards Gnd), and should move towards one rail (which rail?) when the receptor is shielded from light (cover the chip). Bias the source-follower bias transistor $V_{srcf,ol}$ (pin 20) at whatever voltage you like–it shouldn’t make much difference where you put it except to change the DC output.
Set up the LED to deliver only a DC light intensity. Measure the output voltage of the source-follower receptor (pin 21) as a function of relative light intensity over four orders of magnitude. Change the light intensity with a neutral-density filter strip. Plot the voltage as a function of log intensity. Does the circuit act as you expect? What happens at very low intensities? Do you see any potential problems with this receptor?

What is the output voltage of the source-follower circuit when the chip is covered up? Does the leakage current of the junction affect the output voltage? (this is also called dark current in photosensors). Draw a horizontal line in your plot showing where the dark current dominates the output voltage of the circuit.

### 12.3 Postlab

None this week.

### 12.4 What we expect you to remember

How does the I-V curve of a diode change in the presence of light? How does phototransduction occur in silicon?

### 12.5 Next Week

Photoreceptors II. Dynamic properties of photoreceptors.
Figure 12.3: Chip schematic diagram.
Lab 13

Photorceptors II: Phototransduction and Receptor Circuits

The object of this lab is to obtain practical experience in working with light and silicon, and with a well-studied photoreceptor circuit, so that if you ever want to design your own circuits with integrated, continuous-time receptors, you'll know several useful things and the practical problems involved in the interaction of light with silicon.

In this lab, you will examine behavior of an adaptive photoreceptor. Specifically, you will measure

1. properties of hysteretic adaptive elements
2. properties of the adaptive photoreceptor circuit

13.1 Prelab

Read this lab handout carefully and plan your experiments in detail, including circuit diagrams and voltage ranges.

The prelab is important to help guide your measurements. In your prelab analysis, try to remember that most of the results can be obtained in a few lines of calculation, if you clearly understand what it is that you're trying to compute.

Also in this lab we will study two photoreceptor circuits which transduce optical signals into usable electrical signals for visual sensory processing. We will study the a simple logarithmic photoreceptor circuit called the source-follower receptor, mainly as a bridge to understand the other photoreceptor circuit, the adaptive photoreceptor. The adaptive receptor centers its operating point around the past history of the input intensity. This adaptive property allows the receptor to respond with high gain over a wide range of input intensities without saturating. More importantly, it amplifies the interesting signal (the change in intensity around its DC value), and not the built-in static noise due to transistor mismatch.

In this lab we will understand the operation of the adaptive receptor circuit and study the effect of feedback on gain and response speed. You will learn several interesting and useful design tricks:
Figure 13.1: The tobi element. What you draw on a schematic is just the pFET, with the bulk connected to one side and the gate to the other. You get the bipolar transistors for free as part of the resulting fabricated structure.

1. The use of adaptation in a feedback loop to cancel out circuit mismatch
2. How to build a fast logarithmic current-sense amplifier
3. How to use a capacitive divider in the feedback loop of an amplifier to set a gain
4. The use of feedback to make a virtual ground and to speed up the measurement of a current
5. How a cascode configuration can be used to increase effective drain resistance
6. The Miller effect, and how a cascode can be used to nullify it

These tricks are useful in a vast variety of circuits, not just this example.

### 13.1.1 Adaptive elements

Fig. 13.1 shows an adaptive element with a sinh-like I–V characteristic. It is called an adaptive element because it controls the change in charge stored on a capacitor used for adaptation, as shown in Fig. 13.2(b). It has a very nonlinear resistor-like characteristic. It is commonly called “tobi element” (after Tobi Delbrück, who invented it by accident). It consists of a diode-connected well transistor in one direction and a parasitic vertical bipolar transistor in the other.

Draw a physical cross section of the tobi element after fabrication and indicate where current flows both when \( V_g > V_w \) and when \( V_g < V_w \). Sketch the I–V curve for the tobi element on both a linear and semilog plot. No need to get too detailed here – just consider the bipolar and MOS modes of operation. Remember that the tobi element will have two I-V curves, one for each terminal. Show the expected slope and the relative magnitude that you expect for each I-V curve on the semilog plot.
13.1.2 Photoreceptor circuits

Logarithmic photoreceptors have a property that makes them good for sensory perception. Why does the logarithmic response make them useful?

One of the simplest logarithmic photoreceptors, called the source-follower receptor, is shown in Fig. 13.2(a). (An adaptive logarithmic photoreceptor is shown in Fig. 13.2(b).) Sketch a plot of the expected voltage, \( V_{\text{in}} \), as a function of irradiance, for a constant bias voltage. What is the slope of the response?

The following questions pertain to the receptor gain in both the source-follower receptor and the adaptive receptor:

1. Compute the small-signal\(^1\) gain of the source-follower receptor and of the adaptive receptor. By small-signal gain, we mean the output voltage change \( \Delta V_{\text{out}} \) relative to the thermal voltage \( V_T = kT/q \) caused by a small change \( \Delta i \) in the background irradiance.

\(^1\)Denote small-signal with small letters and DC components with caps, as in \( V_{\text{in}} + v_{\text{in}} \).
For the adaptive receptor, compute the transient gain $A$ and the DC gain $A_{dc}$. The transient gain is the gain of the receptor in response to a sudden change in the input. The DC gain is the gain after a long steady intensity. Assume that the gain $A_{imp}$ of the feedback amplifier consisting of $Q_a$ and $Q_p$ is large compared with the capacitive divider ratio $(C_1 + C_2)/C_2$. (This assumption makes the calculation a one-liner.) In the typical configuration, $C_1 \approx 10C_2$.

2. How do the logarithmic properties of the amplification appear in the small-signal gain expressions? In other words, if $y = \ln(x)$, then how is $dy$ related to $dx$?

3. What does “small-signal” mean in terms of the input irradiance?

4. Assuming an early voltage $V_o$ of, say, 20 V for the transistors in the feedback amplifier, what is the expected subthreshold gain, $A_{imp}$, of the amplifier? This computation shows that we can probably safely make the assumption that $A_{imp}$ is larger than $(C_1 + C_2)/C_2$.

5. Assume that the gain $A_{imp}$ is not infinite, and compute the response of the input node $v_{in}$ in response to $i$. (If $A_{imp}$ is infinite, then $v_{in}$ doesn’t move at all.) We will use the gain of $V_{in}$ in later questions about the time-response of the adaptive receptor.

The following questions are about the time response of the source-follower receptor circuit. In these computations, we will only consider small-signal inputs. (The large-signal cases are nonlinear, since the system resembles a diode-capacitor, but are still explicitly solvable.) The small-signal cases will tell us about the speed of the receptor in the case of a small perturbation on top of a large background signal, which is the real-world situation for natural images.

1. Consider the simple source-follower receptor shown in Fig. 13.2(a). The capacitance $C_{in}$ and the background photocurrent $I_{bg}$ determine how fast the receptor responds to a small change $i$ in the irradiance. Compute the first-order time-constant $\tau_i$ of the response for a subthreshold background current. The subscript $in$ refers to the fact that the output of the source-follower receptor is the input stage of the adaptive receptor.

2. If $C_{in}$ is dominated by the capacitance of the photodiode junction, approximately how will $\tau_i$ change if we make the photodiode area twice as large? You can neglect junction perimeter capacitance.

The following questions are about the time response of the adaptive receptor. Assume that the charge on the $V_{cap}$ node is fixed. Assume small signal behavior, but do not assume that the gain $A_{imp}$ of the feedback amplifier is infinite.

1. What is the time-constant $\tau_{in}$ of the small-signal response? Assume that the feedback amplifier is infinitely fast, but that the gain is not infinite.
Figure 13.3: Pinout of the adaptive photoreceptor and non-adapting source-follower photoreceptor. The followers in this figure are p-type, and are actually nearby the circuit on the chip to minimize capacitive loading. They are biased by pfollbias.

2. What is the **total loop gain**, $A_{\text{loop}}$, of the adaptive receptor? The total loop gain is the gain all the way around the loop, multiplying all gain elements in series. Don’t forget the gain of the feedback transistor $Q_{fb}$.

3. What is the speedup of the adaptive receptor over the speed of the simple source-follower log receptor? Express this speedup in terms of the total loop gain $A_{\text{loop}}$. This result is generally true for all transimpedance amplifiers.

### 13.2 Experiments

The adaptive photoreceptor circuit that we will be testing in this lab is on the chip N3ABJC2. It is the circuit in Fig. 13.2(b) and its pinout is shown in Fig. 13.3. For comparison, we will simultaneously be measuring the output of the simple non-adapting logarithmic photoreceptor in Fig. 13.2(a) whose pinout is also shown in Fig. 13.3.

Wire up the necessary connections to test the photoreceptor. As usual, pins 15 and 25 are hooked to ground and pins 5 and 35 to $V_{dd}$. The bias for the follower pads (FollBias) goes to pin 40 and should be set to about 1.3V. The local followers are p-type and are biased by pfollbias, pin 14. Set this to about 4V. For now, to neglect the effect of the cascode transistor, set the cascode bias on pin 16 to 5V. Set the photoreceptor bias on pin 13 to 2

---

2The pinout of the entire chip is attached as Fig. 13.5
about 3.9V. This bias setting will result in a bias current of about 1μA. Set the bias of the source-follower receptor to about 2V.

The HP33120A function generator cannot generate a small AC signal on top of a large DC offset. So to drive the LED, you can use the following trick invented by Jorg Kramer. We supply a DC current by tying a 100Ω resistor to Vdd. The bottom of the resistor is tied to the top (plus side) of the LED. The minus side of the LED is tied to the output of the function generator. The minus of the function generator is chassis ground. Now you can use a small AC signal from the function generator (with no offset) to modulate the LED intensity. Use the SYNC signal of the function generator to trigger the scope.

You can mount the LED over the chip using one of the LED holders, and you can control the DC light intensity over a wide range using the strips of neutral density filters by sliding them under the LED holder. Each step of filter opacity cuts the light intensity by an factor of 10.

Now insert the chip with the usual precautions. Place the holder with the LED on the chip and center it.

**Experiment 1: Adaptive Photoreceptor Gain**

In this experiment, you will measure the small-signal characteristics of the adaptive photoreceptor and calculate its gain, in comparison with the non-adapting source follower receptor.

Using a 20Hz square wave measure the transient response of the adaptive photoreceptor (on pin 11) at two different DC input levels (using the neutral density filters). At the same time, capture the output of the non-adapting receptor. Do you see the difference in the AC and DC response properties?

Plot the captured scope traces\(^3\) for both receptors and both DC light levels on the same plot. Do the responses have the amplitudes and DC levels you expected from what you calculated in the prelab?

**EXTRA CREDIT: Loop gain**

In this experiment, we measure the step response of the adaptive photoreceptor output and its internal nodes to measure the total loop gain of the receptor’s amplifiers. This number tells you how much speed-up you can expect over a completely passive feedback scheme. Take the probe off the non-adapting receptor and use it to measure one of the other nodes in the adaptive receptor.

Use a larger signal to measure the signals at the output (pin 11), at the adaptation node (pin 10), and at the photodiode node (pin 12). The signal at the photodiode node will be very small. You will thus have to average a lot of traces to be able to measure anything. You can now directly measure the capacitive divider ratio and the amplifier gain. What are they?

\(^3\)Use \([t,x]=\text{GetScope}('/dev/gpib0/tds320',1)\) to capture the trace from scope channel 1 to matlab.
Experiment 2: Photoreceptor Time Response

In the following experiments, we will study the time-response of the adaptive photoreceptor.

Experiment 2.1: Adaptation time-constants

In this experiment, we’ll investigate how fast the photoreceptor adapts to a step change in illumination.

Using the same bias settings of the previous experiment, set the frequency of the function generator to 2Hz and apply a square wave with about 3V offset and 2V amplitude. Measure the voltages at the adaptive photoreceptor’s output and feedback node (pins 11 and 10 respectively). How do the adaptation time constants for onset and offset of light compare? This tells you how unsymmetric is the adaptive element.

Experiment 2.2: Effect of illumination on the response time and using the cascode to increase the bandwidth

In this experiment, we will see how the bandwidth (1/(rise time)) scales with DC illumination and how the cascode can be used to increase the bandwidth.

For this experiment we need to go back into the small signal domain. Set the frequency of the function generator back to 20Hz and select an appropriate amplitude for the input square-wave signal. Using the oscilloscope functions, observe the rise and fall times of the adaptive photoreceptor in response to the input. If the signal is truly small, then the rise and fall times will be the same. Now, measure the rise time (the fall time will be the same) as a function of DC irradiance, using the neutral density filters. Control scattered room light by using the potbox cover. Does the step-response time constant behave as you expect with changes in irradiance?

Now activate the effect of the cascode by decreasing the voltage on the cascode transistor bias pot (pin 16). You will need to set the bias below (approximately) 2.5V to start seeing an effect. Can you see how the step responses speed up and the noise increases? Measure the rise and fall time as a function of irradiance again (for a reasonable cascode bias setting). Plot the 2 sets of data (with and without the effect of the cascode) on the same graph. Use the command legend in MATLAB to indicate the value of the bias used.

EXTRA CREDIT: The tobi element

In this experiment we will characterize the photoreceptor’s adaptive element and compute its I-V curve. The pinout of an isolated adaptive element is shown in Fig. 13.4.

First connect $V_w$ (pin 7) to $V_{dd}$, and $V_g$ (pin 3) to the TRIAX connector of the 236 SMU.
Measure the current at $V_g$ while sweeping the voltage (at that same node) from 5V down to 0V. In what mode is the device operating with these settings (i.e. MOS or bipolar)?

Now swap connections: set $V_g$ to $V_{dd}$ and measure the current at $V_w$ using the same sweep parameters.

Plot both curves on a single graph. Rearrange the data so that the graph resembles a sinh function. Again, use the commands `legend` and/or `gtext` in MATLAB (type “help gtext” for details) to point out what part of the curve denotes the MOS mode of operation and what part the bipolar mode.

### 13.3 Postlab

In this optional postlab, we’ll consider the second-order temporal behavior of the adaptive receptor, in order to understand the effect of the speed of the feedback amplifier. This analysis includes the time constant $\tau_{\text{amp}}$ of the amplifier output, as well as the time constant $\tau_{\text{in}}$ of the input node. $\tau_{\text{in}}$ is the same time constant as computed earlier for the simple source-follower log receptor. $\tau_{\text{amp}}$ is the time constant of the output node of the amplifier, i.e., $C_{\text{out}}/g_{\text{out}}$.

1. Write the second-order transfer function of the system from small-signal input $i$ to output $v_{\text{out}}$. To do this computation, you can write small-signal equations governing each of the nodes $v_{\text{in}}$, $v_{\text{cap}}$, and $v_{\text{out}}$ and then go to the $s$-plane. It is then easy to solve for the ratio $v_{\text{out}}/(|i|/I_{bg})$.

2. Show that the $\tau_{\text{out}}$ that results in a damped, maximally sped-up response is such that $\tau_{\text{out}} \approx \tau_{\text{in}}/A_{\text{amp}}$. Show that when $\tau_{\text{out}} \approx \tau_{\text{in}}$, then the amount of ringing is maximal, i.e., the circuit has maximum $Q$.

3. What do the preceding results indicate, qualitatively, about the necessary level of bias current in the feedback amplifier, relative to the input photocurrent, to ensure a damped, nonringing response?

### 13.4 What we expect you to remember

How does the I-V curve of a diode change in the presence of light? How does phototransduction occur in silicon? How you can use adaptation in a feedback loop to cancel out
circuit mismatch. How you can build a fast logarithmic current-sense amplifier, by using feedback to make a virtual ground. How you can use a capacitive divider in the feedback loop of an amplifier to set a gain. How you can use a cascode configuration to increase effective drain resistance. What is the Miller effect, and how a cascode can be used to nullify it.

13.5 Next Week

DEMOS!!! NO LAB!!!!
Figure 13.5: Chip schematic