Device-grade SiGe heterostructures grown by plasma assisted techniques

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Device-grade SiGe heterostructures grown by plasma assisted techniques

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2001
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Abstract

With the current Si-based mainstream technology for microelectronics approaching an increasing number of fundamental physical limits in the near future, its extension towards silicon-germanium (SiGe) receives much interest. By taking advantage of superior intrinsic properties of Ge as well as new degrees of freedom for device design, the performance range of the Si-based technology can be significantly extended on a highly economic route. While first commercial devices based on bipolar SiGe designs are already available (HBT’s and BiCMOS IC’s), there still exists a huge potential for field-effect based SiGe devices, possibly replacing Si CMOS in the end. However, to transfer these new designs from research laboratories into production lines, new techniques for epitaxy in a mass production environment are badly needed.

With LEPECVD, such a novel process is already on the way of being implemented in a commercial production system. Here we demonstrate its successful application to the fabrication of virtual SiGe substrates in the whole concentration range of SiGe alloys, as well as to the growth of complete electronic device layer sequences.

Chapter 1 presents an introduction to SiGe technology. First, the electronic properties of both bulk and thin films are briefly reviewed for Si and Ge. Then the electronic and structural issues of SiGe heterostructures are discussed. The issue of the substrates for strained-layer SiGe applications is addressed next, followed by a short review of the present epitaxy techniques in use for SiGe research and production.

In chapter 2 several improvements of the LEPECVD process and the experimental system as well as further applications are presented. For homoepitaxial Si films, novel self-organized surface morphologies are presented. The deposition of microcrystalline Si films shows an enormous potential of LEPECVD for applications making use of cheap substrates like displays, solar cells or photodetectors.

Chapter 3 then addresses the fabrication of electronic device structures. The optimization of virtual SiGe substrates containing up to 100% Ge is discussed with respect to surface morphology, structural quality and dislocation density. The application of such substrates for combinations with traditional epitaxy techniques is exemplified with the demonstration of n-type modulation doped quantum well (n-MODQW) and modulation doped field effect transistor (n-MODFET) structures grown by MBE on LEPECVD-grown substrates. In both cases highly promising results can be presented, with a low-temperature electron mobility of up to 159’000 cm²/Vs in the MODQW and a maximum transconductance of the MODFET of $g_m = 230$ mS/mm. Modulation doping by LEPECVD alone is also demonstrated in the case of an n-MODQW, where still some room for improvements is found. The ultimate proof for the electronic
quality of strained-layer heterostructures grown by LEPECVD is given with the
demonstration of p-type MOSFET's, showing peak values of $g_m = 118 \text{ mS/mm}$
and a saturation current of up to $410 \text{ mA/mm}$ at a gate length of $2 \mu \text{m}$.

Chapter 4 deals with detailed studies of some microscopic structural aspects of the SiGe system. For this purpose, magnetron sputter epitaxy (MSE) was employed, which had been shown in the past to result in epitaxial layers of comparable quality and thickness control like MBE. The first stages of overgrowth of self-assembled Ge nanoclusters are studied by scanning tunneling microscopy (STM). The observed shape changes are relevant for possible device applications of these quantum-size structures, which for this purpose have to be embedded in some matrix material. The combination of MSE and STM is further applied to an atomic-scale study of the surface of relaxed graded SiGe buffer layers. A novel step structure is found, leading to $D_A$ steps and double layer islands which would not be expected in the Si(001) system. A qualitative model is presented, based on the anisotropic surface strain fields induced by the misfit dislocation network in the relaxed buffer.

The development of novel epitaxial deposition systems and processes implies the need for suitable analytic techniques, capable of obtaining detailed information from sometimes highly defected thin films. This issue is discussed in the case of X-ray diffraction techniques applied to MSE material deposited under non-optimal process conditions. As traditional diffraction techniques apparently cannot unambiguously reveal the true structure, the combination with the X-ray standing wave (XSW) technique is shown to result in a consistent picture.
Kurzfassung

Während die aktuelle Si-basierte Mikroelektronik an eine stetig wachsende Zahl von fundamentalen physikalischen Grenzen stößt, kommt ihrer Erweiterung in Richtung Silizium-Germanium (SiGe) großes Interesse zu. Durch Ausnutzen sowohl der überlegenen Eigenschaften von Ge als auch von neuen Freiheitsgraden im Design von Bauteilen, kann die Leistungsbandbreite der Si-Technologie auf einem höchst ökonomischen Weg markant erweitert werden. Erste Bauteile basierend auf bipolaren SiGe-Designs sind zwar bereits kommerziell erhältlich (HBT's und BiCMOS IC's), doch es bleibt noch immer ein gewaltiges Potenzial für Feldeffekt-basierte SiGe-Bauteile, die am Ende Si-CMOS ersetzen könnten. Um jedoch diese neuen Designs aus den Forschungslabors in die Produktionslinien zu bringen, werden dringend neue Epitaxie-Techniken für die Massenproduktion benötigt.

Mit LEPECVD steht ein solcher Prozess kurz vor seiner Umsetzung in einem kommerziellen Produktionssystem. Hier zeigen wir seine erfolgreiche Anwendung für die Herstellung von virtuellen SiGe-Substraten im gesamten Konzentrationsbereich, wie auch für das Abscheiden von kompletten Schichtfolgen für Bauteile.

Kapitel 1 gibt eine Einführung in die SiGe-Technologie. Zuerst werden die elektronischen Eigenschaften von Volumenmaterial sowie von dünnten Filmen von Si und Ge kurz zusammengefasst. Dann werden die elektronischen und strukturellen Aspekte von SiGe-Heterostrukturen diskutiert. Weiter wird das Problem der Substrate für Anwendungen verspannter SiGe-Schichten behandelt, gefolgt von einem kurzen Abriss über die gegenwärtigen Epitaxie-Techniken, die für die SiGe-Forschung und -Produktion im Einsatz sind.

In Kapitel 2 werden verschiedene Verbesserungen des LEPECVD-Prozesses und des experimentellen Systems sowie sein Einsatz für weitere Anwendungen präsentiert. Im Fall von homoepitaktischen Si-Filmen werden neuartige selbstorganisierte Oberflächen-Strukturen präsentiert. Das Abscheiden von mikrokristallinem Si offenbart ein enormes Potential für den Einsatz von LEPECVD in Anwendungen, welche billigere Substrate verwenden, wie etwa Displays, Solarzellen oder Fotodetektoren.

Kapitel 3 behandelt die Herstellung von Strukturen für elektronische Bauteile. Die Optimierung von virtuellen SiGe-Substraten mit bis zu 100% Ge-Gehalt wird diskutiert im Hinblick auf deren Oberflächen-Morphologie, strukturelle Qualität und Versetzungsdichte. Der Einsatz solcher Substrate für die Kombination mit herkömmlichen Epitaxie-Techniken wird beispielhaft demonstriert anhand von n-Typ-modulations-dotierten Quantenendopf- (n-MODQW) sowie Feldeffekt-Transistor-Strukturen (n-MODFET), welche mit MBE auf LEPECVD-beschichteten Substraten hergestellt worden sind. In beiden Fällen können äußerst vielversprechende Resultate gezeigt werden, mit
Kurzfassung

Tieftemperatur-Beweglichkeiten für Elektronen von bis zu 159'000 cm²/Vs im MODQW und einer maximalen Steilheit des MODFET’s von $g_m = 230$ mS/mm. Modulations-Dotierung mit LEPECVD alleine wird ebenfalls demonstriert anhand eines n-MODQW, wo sich jedoch noch Raum für Verbesserungen findet. Der abschliessende Beweis für die elektronische Qualität von verspannten Heterostrukturen, hergestellt mit LEPECVD, wird mit der Demonstration von p-Typ MOSFET’s gegeben, welche selbst bei einer Gate-Länge von 2 μm Steilheits-Werte von $g_m = 118$ mS/mm und Sättigungsströme von bis zu 410 mA/mm aufweisen.


Chapter 1

Introduction

1.1 SiGe technology

Undoubtedly, microelectronics has been a field of unique technological advances during the last 50 years. However, regardless of its huge importance and the size of the associated economic market which pushes research and development further with enormous impetus, electronics has been largely dominated by a single material, namely silicon (Si). The ultimate reason for the huge success of Si is cost. To date, no competing material has been found to really challenge silicon on that point. An illustrative comparison which is frequently cited is shown in table 1.1. Although the absolute values may be somewhat out-dated, the relations will still roughly apply.

On the one hand, this low cost is due to the comparably low price of the raw material, even when refined to ultra high purity. On the other hand, compared to other materials, its physical and chemical properties make processes for fabricating electronic devices at ever higher integration scales relatively cheap and easy; e.g. the availability of processes for producing large perfect single crystals

<table>
<thead>
<tr>
<th>Technology</th>
<th>Cost per mm² [USD]</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>0.01</td>
</tr>
<tr>
<td>SiGe epitaxy</td>
<td>0.60</td>
</tr>
<tr>
<td>GaAs epitaxy</td>
<td>2.00</td>
</tr>
<tr>
<td>InP epitaxy</td>
<td>10.00</td>
</tr>
<tr>
<td>Tokyo real estate</td>
<td>0.01</td>
</tr>
</tbody>
</table>

Table 1.1: Cost of different materials (1995) [1]
or the superior quality of its natural oxide with respect to both electronic and chemical properties.

Interestingly, the total of electronic circuits produced today consists to a large part of one single device: the Si metal oxide semiconductor field effect transistor, or MOSFET, in a wide variety of different designs. Apart from improved material quality, the main path of improvements since its first implementation has been a constant reduction in size, reducing the path travelled by carriers and diminishing parasitic capacitances limiting the switching speed of transistors. As device dimensions keep shrinking, they start to approach fundamental physical limits, like the insulating gate oxide layer coming close to the thickness of one single molecular layer. There is thus a huge interest in finding ways for improving device speed and power efficiency without the need for down-scaling.

Silicon-germanium (SiGe) is able to address both points simultaneously, as will be explained in detail below. By providing novel designs and better intrinsic material properties, SiGe can significantly extend the performance range of silicon devices, giving access to applications and markets which have been dominated by more expensive technologies so far. The biggest interest for novel devices operating at higher speed presently arises from wireless communications applications operating in the GHz frequency range. The first Si-based device entering these markets has been the SiGe hetero bipolar transistor (HBT), for which a maximum operation frequency in excess of 200 GHz has been demonstrated. By combining with standard Si CMOS, advanced SiGe BiCMOS processes have already been developed [2, 3]. The reason that makes integration of the SiGe HBT into traditional CMOS processes relatively easy is the small number of additionally required process steps [4].

The recent years have seen a world-wide boost in research effort attributed to SiGe, with eventually all major semiconductor device manufacturers involved in the Si market presenting or at least announcing SiGe development programs and first commercial products. This has become possible as the result of at least 20 years of academic and industry research programs targeted at bringing back Ge to where it once used to be in the early years of microelectronics — the mainstream production lines.

1.2 Physics of SiGe devices

1.2.1 Electronic properties

Bulk materials

The enhancements provided by the introduction of Ge into Si technology can be roughly divided into superior properties of bulk Ge on the one hand, and benefits
from heterostructure designs on the other hand, the latter including strain or band structure engineering, modulation doping and improved interfaces of active layers.

The main quantity characterizing the motion of charge carriers in a solid driven by an electric field $E$ is their mobility $\mu$, defined in the simplest case of the Drude theory by

$$\mu = \frac{j}{qnE} = \frac{q\tau_t}{m^*}$$

where $j$ denotes the current density, $q$ the charge per carrier, $n$ their density, $\tau_t$ the mean transport scattering time and $m^*$ the effective mass in the direction of the motion. Consequently, enhanced mobility directly results in higher current density. Compared to Si, bulk mobilities of both electrons and holes in Ge are significantly higher, as shown in table 1.2: $\mu_{e,Ge}/\mu_{e,Si} = 2.89$ and $\mu_{h,Ge}/\mu_{h,Si} = 3.96$ at room-temperature (RT). Additionally, the RT hole mobility in Ge (1900 cm$^2$/Vs) significantly surpasses that of compound semiconductors like InP ($\approx 100$ cm$^2$/Vs), Al$_x$Ga$_{1-x}$As ($< 300$ cm$^2$/Vs), GaAs ($\approx 400$ cm$^2$/Vs) or InAs ($\approx 500$ cm$^2$/Vs), making Ge the favorable material for p-type devices [5]. While for most discrete device applications one type of transistor would be sufficient (i.e. the n-type with the higher carrier mobility), the availability of p-type transistors with comparable performance becomes important for complementary circuit designs with strongly reduced power losses. The vast majority of highly integrated circuits is heavily relying on the complementary metal-oxide-semiconductor (CMOS) technology [6], which suffers from this distinct asymmetry in the mobility of electrons and holes in Si. High-hole-mobility SiGe devices could enable truly symmetric implementation of complementary designs [7].

Of great importance for optical applications like infrared (IR) photodetectors or solar cells, is the lower band gap of Ge (table 1.2). For detectors, this extends the wavelength range where they can operate, while for solar cells a larger part of the electromagnetic spectrum can be exploited for power generation.

In unstrained bulk silicon, the sixfold degenerate conduction band minima are located along the $\{100\}$ axes close to the X point — usually referred to as $\Delta_6$ minima. In Ge, on the other hand, the conduction band minima are located at the Brillouin zone boundary in the $\{111\}$ directions and hence are eightfold degenerate ($L_8$ minima). In both cases, the longitudinal effective masses are considerably higher than the transversal ones. For both materials the valence band maximum is in the zone center, with the light-hole (LH) and the heavy-hole (HH) band being degenerate and the spin-orbit (SO) band lying somewhat lower (44 meV for Si and 290 meV for Ge). SiGe alloys show a Si-like band gap ($\Delta_6 - \Gamma$) up to about 85% Ge concentration, where a crossover to Ge-like ($L_8 - \Gamma$) occurs.
Table 1.2: Selected RT electronic properties of Si and Ge: direct and indirect bandgaps \( E_g^d \) and \( E_g^i \) [eV], bulk mobilities for electrons and holes \( \mu_e \) and \( \mu_h \) [cm\(^2\)/Vs], transversal and longitudinal electron masses \( m_t \) and \( m_l \), and the heavy hole, light hole and spin-orbit hole masses \( m_{hh}, m_{lh}, m_{so} \) (from [5, 8]). Masses are in units of the free electron mass \( m_0 \).

<table>
<thead>
<tr>
<th></th>
<th>( E_g^d )</th>
<th>( E_g^i )</th>
<th>( \mu_e )</th>
<th>( \mu_h )</th>
<th>( m_t )</th>
<th>( m_l )</th>
<th>( m_{hh} )</th>
<th>( m_{lh} )</th>
<th>( m_{so} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>3.40</td>
<td>1.11 (( \Delta ))</td>
<td>1350</td>
<td>480</td>
<td>0.19</td>
<td>0.98</td>
<td>0.53</td>
<td>0.15</td>
<td>0.23</td>
</tr>
<tr>
<td>Ge</td>
<td>0.80</td>
<td>0.664 (L)</td>
<td>3900</td>
<td>1900</td>
<td>0.082</td>
<td>1.64</td>
<td>0.28</td>
<td>0.04</td>
<td>0.09</td>
</tr>
</tbody>
</table>

Strained layers and heterointerfaces

The issues of interest for strained heterostructures are the band alignment between layers and the effect of strain, which is inevitable due to the 4.2% lattice mismatch of the two elements, with the lattice constant to a good approximation scaling linearly for alloys (see also appendix A). In addition, the general features of two-dimensional transport have to be taken into account.

Instead of treating all the different possible band alignments between SiGe layers with different composition and different strain state in detail, we will give a brief overview of the cases which are relevant for the devices covered in this work. For a general treatment, one usually resorts to self-consistent local-density-functional calculations, which were first performed by Van de Walle and Martin [9] for the band alignment at the Si/Ge interface. Complete recipes derived from that data for practical applications can be found in review papers like [8, 10], an in-depth theoretical treatment, e.g., in [11].

In the case of a \( \text{Si}_{1-x}\text{Ge}_x \) alloy grown on Si(001), a type II (staggered) band alignment results with the discontinuity lying almost exclusively in the valence band with

\[
\Delta E_V \approx 0.74x \text{ eV}
\]

(1.2)

(the band edge lying higher in energy in the SiGe layer), while \( \Delta E_C < 20 \text{ meV} \). In the case relevant for the p-type structures discussed in section 3.3.3, where a strained \( \text{Si}_{1-x}\text{Ge}_x \) layer is grown on a relaxed \( \text{Si}_{1-y}\text{Ge}_y \) substrate, the valence band discontinuity amounts to

\[
\Delta E_V \approx (0.74 - 0.06y) \cdot (x - y) \text{ eV},
\]

(1.3)

also with a type-II alignment.

For Si-channel-based n-type applications, in order to obtain efficient electron confinement a substantial lowering of the conduction band in the Si has to be achieved, which is only possible by applying tensile strain to the channel.
1.2. Physics of SiGe devices

Biaxial strain lifts the degeneracy of the $\Delta_6$ minima, in the tensile case resulting in a lower twofold $\Delta_2$ (perpendicular) and a higher fourfold $\Delta_4$ (in-plane) minimum; in addition, the degeneracy of the LH and HH valence bands is lifted. The eightfold degenerate L-band, on the other hand, is not affected. Its lower energy leads to preferential population of the $\Delta_2$ band, for which the in-plane effective mass is $m_t = 0.19m_0$, which directly enhances the mobility (equation 1.1). For the strain-induced lowering of the conduction band edge in Si grown pseudomorphically on $\text{Si}_1-x\text{Ge}_x$ one obtains

$$\Delta E_C \approx 0.6x \text{ eV}$$

for $x < 0.6$ (higher $x$ are of no technological relevance due to the low critical thickness resulting for the Si channel).

For the value of the band gap one obtains for the Si-like and Ge-like regime, respectively [10]:

$$E_g = 1.155 - 0.43x + 0.0206x^2 \text{ eV}, \text{ for } x < 0.85$$

$$E_g = 2.010 - 1.27x \text{ eV}, \text{ for } x > 0.85.$$ 

The electronic properties of two-dimensional carrier gases (2DCG) are of very general interest for device applications, as the most numerous electronic devices are all of the field-effect type, which heavily rely on the transport properties of a thin, quasi-2D sheet of carriers (for a review, see [12]). Thus a thorough understanding of 2D carrier dynamics and scattering mechanisms is of vital importance for the optimization of these devices. While in the traditional MOS (most important for the Si technology) or metal-semiconductor (MES, found mainly in GaAs devices) system the 2DCG is located at the interface between structurally and electronically completely different materials, semiconductor heterostructures in the ideal case make use of a perfect interface between very similar materials. This can result in a reduction of scattering potentials which are due to interface roughness, electronic interface states or, in the MOS case, space-charge in the oxide layer close to the carrier sheet. Additionally, band offsets between different materials and band structure modifications by strain, as discussed above, can be exploited for forming quantum wells confining carriers supplied by remote doping layers (modulation doping), which eliminates scattering at ionized dopant atoms in the active channel itself.

1.2.2 Structural issues

The 4.2% lattice mismatch between Si and Ge imposes severe difficulties on the fabrication of epitaxial layer sequences consisting of both materials or their alloys. When depositing a material onto a substrate with a different lattice constant, the deposited layer will be strained to the underlying lattice at first. As
the accumulated strain energy in the growing film becomes high enough, elastic and plastic relaxation will set in (for details refer to appendix A). As epitaxial growth usually is a highly non-equilibrium process, strained films usually are metastable. For active layers, strain thus imposes restrictions to their maximum thickness, as both elastic and plastic relaxation are highly deleterious to electronic transport. As often metastable states are exploited, limitations arise for the total thermal budget during any kind of device processing subsequent to the epitaxy. The same is true for interdiffusion at heterointerfaces and doping layers.

Another issue is the formation of abrupt heterointerfaces by itself. The different chemical potentials of Si and Ge can lead to strong segregation during deposition, leading to intermixing and smearing out of nominally abrupt interfaces. The microscopic processes involved in interface formation depend strongly on the deposition technique used and can be modified by using additional species changing the surface chemistry of the growth interface (so called surfactants, relevant for the SiGe system are, e.g., Sb or H).

While many of the problems associated with the fabrication of semiconductor heterostructures have been dealt with in different materials systems (the traditional materials for heterostructure devices are found among the III-V compound semiconductors), the issue of a substrate possessing a lattice constant tuned to a specific application has been most successfully addressed in the SiGe system. Apart from devices which make use of strained Si$_{1-x}$Ge$_x$ layers on Si, like the SiGe HBT or certain types of strained-SiGe MOSFET’s or MODFET’s, strained-layer Si or SiGe applications require a substrate with an intermediate lattice constant between that of Si and Ge. We will only concentrate on such applications in this work.

1.3 Virtual SiGe substrates

There has been much research over the past years targeted at the economic fabrication of substrates with a larger lattice constant than that of Si. Apart from novel devices based on strained-layer SiGe heterostructures, further motivation arises from the prospect of the integration of other materials like III-V semiconductors for optical applications with standard Si technology. To be suitable for mass production, such a substrate must meet the high benchmarks of cost and compatibility with Si processing, imposing restrictions on its chemical behavior, availability of standard (which means large) wafer sizes and mechanical stability. These requirements have led to different kinds of substrates based on standard Si wafers, which in fact can be used in standard or only slightly modified CMOS production lines. Such substrates, consisting of an epitaxial film with an intermediate lattice constant between Si and Ge on a standard Si
1.3. Virtual SiGe substrates

Virtual SiGe substrates (VS). There have been many different approaches, including growth on silicon-on-insulator (SOI) substrates [13, 14], introducing a low-temperature Si buffer with a high density of point defects as dislocation nucleation sites underneath the SiGe film [15, 16, 17, 18], or creating highly damaged sub-surface layers by means of ion implantation to promote dislocation nucleation below the SiGe film [19, 20, 21, 22]. However, the most mature technique consists of growing a thick, compositionally graded relaxed SiGe buffer layer with final Ge concentration $x_f$ followed by a SiGe layer of constant composition $x_f$ [23] (cf. Fig. 3.1 on page 30).

The purpose of the graded buffer layer is to vertically distribute the network of strain-relieving misfit dislocations (MD), thus reducing dislocation blocking [24], promoting longer MD segments and, consequently, a lower density of threading dislocations (TD). The constant composition buffer, on the other hand, serves to isolate the active device layers from the strain fields induced by the MD network. The result is a SiGe substrate with a lattice constant equal to that of bulk SiGe with a Ge concentration $x_f$. The main issues which have to be addressed are the degree of relaxation (which should be as complete as possible), the surface morphology (in view of lateral carrier transport or subsequent lithographic processing steps), and the TD density (limiting device performance and production yield).

The major drawback of this kind of SiGe substrates is the large thickness needed for the graded buffer layer. To achieve a sufficiently low defect density and smooth surface, Ge concentration gradients on the order of 10%/$\mu$m have to be used, leading to film thicknesses of several $\mu$m. Considering typical growth rates of traditional epitaxy techniques like MBE or UHV-CVD, which normally lie below 10 Å/s at temperatures $\leq 750\,^\circ$C, this results in unacceptably long deposition times. Low temperatures are mandatory in order to suppress excessive surface roughening. A further problem for solid source MBE systems is the capacity of the deposition sources, which have to be refilled after growth of only a few of these thick layers, which is also not acceptable for mass production. Hot-wall processes like UHV-CVD, on the other hand, suffer from rather complex process control due to the large thermal capacity of the deposition reactor, which makes it virtually impossible to employ temperature ramps during growth. While the problem of growth time could in principle be addressed with batch processing, the actual trend in industrial production is heading towards single-wafer processes, motivated, e.g., by the growing substrate dimensions which make batch handling increasingly complex.

---

1 A SiGe layer of constant composition grown directly on a Si(001) substrate results in a TD density on the order of $10^9 - 10^{11}$ cm$^{-2}$. By introducing a graded buffer layer, this number could be reduced to $10^5 - 10^8$ cm$^{-2}$. It has been shown that a TD density below $10^8$ cm$^{-2}$ will not affect carrier mobility [25].
\section*{1.4 Established epitaxy processes for SiGe}

Due to the rapidly increasing number of both publications and research groups involved over the last few years, it is becoming increasingly difficult to give a complete overview of the ongoing research in the field of SiGe. Nevertheless, a brief look at the growth techniques used, reveals that the vast majority of the results has been achieved using just two basic techniques, namely molecular beam epitaxy (MBE) and ultra high vacuum chemical vapor deposition (UHV-CVD). Since the latter had been developed at IBM \cite{26}, except for a few relatively early studies done with MBE almost all the work published by IBM uses this technique, which has been shown to have a great potential for commercial HBT-based products. As of today, in terms of device market volume UHV-CVD is believed to dominate by far over the other deposition techniques. Other important research groups substantially employing UHV-CVD include the DERA crew at Malvern, UK, Fitzgerald’s group at the MIT and, earlier, the former group of Houghton in Ontario, Canada, before he also, like IBM, started to commercialize the process.

Most other groups are using MBE, just a few employ LPCVD (low pressure CVD) or RTCVD (rapid thermal CVD), and there have also been reports on APCVD (atmospheric pressure CVD) or LPE (liquid phase epitaxy). Most record devices, though, have been obtained using the two mainstream processes mentioned.

This brief summary might give an impression of how relevant the successful implementation of a completely new technique, aimed specifically at economic production, could be for the further development of this field. From the above, the most important properties such a new technique should ideally possess can be summarized with the following keywords: it should be a single wafer process, provide a high dynamic range of growth rates and allow for easy control in a large process window, e.g. allowing for a fast change of all the important process parameters.
Chapter 2

Low energy plasma enhanced chemical vapor deposition (LEPECVD)

2.1 The process and the experimental system

The LEPECVD process is based on a DC arc discharge between a heated filament and the grounded chamber walls. A schematic of the experimental system is shown in Fig. 2.1. The discharge voltage lies in the range of $V_{\text{arc}} = 15 - 30$ V, depending on the discharge current, focusing magnetic field strength, gas composition and working pressure. The arc discharge current normally lies between $I_{\text{arc}} = 20 - 70$ A. To stabilize and constrain the plasma, an external focusing magnetic field parallel to the chamber axis is applied by means of copper coils wrapped around the chamber, carrying a current of up to $I_{\text{coil}} = 10$ A. To improve the lateral homogeneity of the intensity distribution in the plasma, four electromagnets on the sidewalls of the chamber can be used to constantly move the plasma column horizontally, thus sweeping the intensity maximum over the substrate area (we call this the *wobbler*). Between the plasma source and the substrate, we use a ring-shaped auxiliary anode, which is electrically connected to the chamber wall potential, to further stabilize and focus the discharge. This auxiliary anode is made up of six 5 mm thick molybdenum segments, forming a ring with an inner diameter of 100 mm and outer diameter fitting to the vacuum vessel. The potential of the substrate can be controlled externally, raising it by the use of shunt resistors, or further lowering it with a voltage source. The floating potential usually lies between $-10$ V and $-20$ V with respect to the chamber walls. The substrate is completely immersed in the plasma. It
can be heated from the backside by means of a resistance heater consisting of a graphite resistor enclosed between two boron nitride disks. The temperature is measured with two thermocouples located on the backside of the heater, where they are shielded from the plasma. The temperature readings are calibrated using an infrared pyrometer. The chamber is pumped to a base pressure of below $10^{-9}$ mbar with a turbo molecular pump and a rotary prevacuum pump. During process, the working pressure amounts to $1 - 3 \cdot 10^{-2}$ mbar. The system is equipped with a load lock chamber for exchanging substrates without breaking the vacuum. In its present setup, the experimental LEPECVD system can handle 3-inch (75 mm) and 4-inch (100 mm) substrates in single-wafer operation.

Originally, this system was designed for RT cleaning of Si substrates in a low-energy hydrogen plasma [27] for subsequent epitaxy in an attached MBE system. Due to extensive coating of system components during deposition, in the present configuration of a single-chamber reactor this plasma cleaning is not feasible any more, as will be discussed below in section 2.2.1.

The specific properties of this kind of low-voltage, high-current arc discharge are the key to the stunning results achieved with LEPECVD. The huge density of low-energy ions serve to efficiently crack the precursor gases and to promote hydrogen desorption from the growth surface of the substrate, which is directly immersed in the plasma column, without causing ion damage to the films. The result are very high epitaxial growth rates of up to 10 nm/s, which to date seem to be limited only by the maximum flux of precursor gases, determined by the employed mass flow controllers. In addition, the purely
non-thermal origin of the energy supplied by the plasma leads to deposition highly independent of temperature and gas composition. This is of specific interest for low-temperature growth of alloyed materials as in the case of SiGe heteroepitaxy.

Substrates

Normally, we used 4-inch Si (001) substrates as-delivered, only applying a dilute HF dip for oxide removal and subsequent rinsing in de-ionized water prior to inserting them to the load lock. Only in case of excessive contamination of delivered wafers an additional RCA clean was employed. The substrates were then outgassed in UHV for 20-60 min at a moderate temperature of about 250°C. In addition to using Si substrates, we have performed several successful experiments using glass substrates (for poly-Si or microcrystalline Si films) and Si wafers with anodized (porous) surface layers.

2.2 Improvements to the process

2.2.1 Enhanced reproducibility

The previous stages of the development of the LEPECVD process and the experimental system have been reported in [28]. While relatively soon very promising results had been achieved during that period, reproducibility was a certain issue as detailed knowledge of several aspects of the process had yet to be acquired. In the course of this work, the reproducibility between samples prepared under nominally identical conditions could be significantly improved compared to the earlier experiments. At the same time, the number of samples which failed for unknown reasons was reduced. The aim of this section is to identify the most important problems which had limited the reproducibility before, and to outline how they have been addressed.

Re-deposition from the chamber

One of the key properties of LEPECVD is its ability to very efficiently decompose the precursor gases and incorporate their constituents without the need of chemically reactive and thermally activated surfaces as in normal CVD. As a rather undesired side effect, a significant amount of material is being deposited on different parts of the growth chamber, with the amount deposited being the larger, the higher the plasma density to which a specific part is exposed. Especially on components reaching high temperatures, i.e. the parts surrounding the heater and the auxiliary anode, it is highly probable that significant Ge segregation takes place. The abundance of atomic hydrogen during deposition,
but especially during a hydrogen cleaning cycle, can then lead to the etching of significant amounts of Si and Ge, part of which will find their way onto the wafer surface. During normal deposition conditions, this fraction is negligible due to the comparably large flux of Si and/or Ge supplied by the precursor gases. During a hydrogen cleaning cycle, on the other hand, the amount of Ge redeposited on the wafer can in fact be sufficient to cause strain-induced three-dimensional roughening of the initial growth interface. This rough surface morphology then leads to the nucleation of a high density of defects, normally rendering a sample totally unusable.

Leakage flux through mass flow controllers

A second origin of Ge deposition during a hydrogen cleaning cycle is the ‘standby flux’ of the GeH₄ mass flow controller (MFC). Some of the MFC’s have a relatively large residual flux even if their control valve is fully closed¹. In the case of the MFC we used for GeH₄, this flux can reach several percent of an sccm, which can lead to the deposition of several monolayers of Ge during a cleaning cycle of 120 s. The magnitude of this flux is documented in Fig. 2.2, where X-ray rocking curves of two Si samples are compared, one of which has been grown with the GeH₄ gas line filled with gas, while for the other one it had been evacuated before growth. While the sample grown with the GeH₄ gas line pressurized contains 2.23% Ge, which corresponds to a residual flux of 0.068 sccm GeH₄, no traces of Ge are found in the other sample. This problem has been addressed in the meantime with the addition of bypass valves for both the SiH₄ and GeH₄ gas lines, installed after the MFC’s and diverting the leakage flux directly to the pumping system instead of the chamber.

Improved initial growth procedure

Before these problems of unintentional Ge deposition had been identified, the normal procedure for obtaining a clean, flat growth interface on a newly inserted wafer was to perform two hydrogen cleaning cycles of 120 s each at 330°C and 740°C², respectively, using a discharge current I_{arc} = 30 A, coil current I_{coil} = 9 A, H₂ flux Φ_{H₂} = 5 sccm and Ar flux Φ_{Ar} = 50 sccm. Thereafter, a Si buffer layer was grown using a discharge current of I_{arc} = 40 – 50 A and a SiH₄ flux of Φ_{SiH₄} = 3 sccm at 740°C. A major improvement could be achieved by omitting the initial H₂ cleaning cycles, during which the most part of the Ge had been deposited from the etching of machine parts and the residual MFC

¹At present, Brooks 5850S MFC’s are used.
²This was a typical T_{max} reached with the current setup of heater and temperature controller. Depending on the exact mounting position of the thermocouples, this maximum temperature was between 720°C and 750°C, limited by the measuring range of the temperature controller used.
2.2. Improvements to the process

Values used for simulation:
- thickness: 210 nm,
- Ge content: 2.23%

Growth parameters:
- $T=500^\circ\text{C}$, $\Phi_{\text{GeH}_4}=3$ sccm,
- $I_s=30$ A, $I_m=3$ A,
- $t=2800$ s

Figure 2.2: X-ray rocking curves measured in the wafer center of samples #5874 and #5875. Both samples have been grown using the same parameters as indicated. For #5874, the GeH$_4$ gas line was filled; the GeH$_4$ MFC was in controller position ‘Normal’ with a valve value of 11668 (the values of the Brooks 5850 MFC have a working range of 0-62500) and measured flux of 0.0 sccm. Although only for the SiH$_4$ MFC a non-zero setpoint had been chosen, the resulting film contained 2.23% Ge. No indication of Ge is visible, on the other hand, in #5875, where the GeH$_4$ gas line had been evacuated before growth.
Table 2.1: Process parameters of the old and the new procedure for obtaining the initial clean, flat growth interface

<table>
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<tr>
<th>T [°C]</th>
<th>( \Phi_{H_2} ) [sccm]</th>
<th>( \Phi_{SiH_4} ) [sccm]</th>
<th>( I_{arc} ) [A]</th>
<th>( I_{coil} ) [A]</th>
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<td></td>
<td></td>
<td></td>
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<td>3</td>
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<td>50</td>
<td>9</td>
<td>150</td>
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</table>

flux. Even better results could be obtained by additionally reducing the plasma density during the first 150 s of Si deposition. A comparison of the old and new procedure is shown in table 2.1.

2.2.2 Long-term stability of the process conditions

One of the major concerns during the early stages of the development of LEPECVD has been the change of process conditions with the growing amount of material deposited. It was believed that the growing coverage of machine parts, especially of the auxiliary anode, leads to a significant change of the discharge characteristics of the plasma, causing an increasing number of ion-induced defects in the films. As a consequence, frequent opening of the UHV chamber was believed to be inevitable in order to remove the deposited material from the auxiliary anode and the most critical parts of the heating stage. In the course of this work, it could be shown during a period of more than nine months where the system was constantly closed and pumped to UHV conditions, that only a minor change in the discharge voltage and floating potential is observed even though the accumulated thickness of the deposited films exceeded 2 mm. No detrimental effects to the film quality could be observed, as can be seen in Fig. 2.3. There we show an X-ray rocking curve of a 15 µm thick Si layer deposited 8 months after cleaning the chamber. Only after the breakdown of both thermocouple insulations the system had to be opened and cleaned again. In its current configuration, these parts turned out to be ultimately limiting the up-time of the experimental system.
2.2. Improvements to the process

2.2.3 Influence of the substrate potential

According to early experience, an externally controlled substrate potential of $-8 \text{ V}$ was believed to be suitable for achieving optimal structural film quality. The substrate potential was raised from the floating potential by means of external resistors, connecting the substrate holder and additional molybdenum spring contacts to the wafer backside with ground, and kept constant at $-8 \text{ V}$ with an external voltage source. The floating potential of the wafer normally lies between $-10 \text{ V}$ and $-20 \text{ V}$, depending on the discharge parameters, working pressure and substrate temperature. The additional spring contacts had been introduced earlier in order to achieve a better contact and a more homogeneous potential distribution across the wafer. Unfortunately, because they had to be mounted between the radiation heater and the substrate, they led to significant inhomogeneity in the temperature distribution across the substrate, which often was reflected in a higher defect density in the areas underneath these contacts due to the locally lower substrate temperature (see section 2.3.1-2.3.2).

To systematically study the influence of the substrate potential on the structural quality of the deposited films, a series of samples has been prepared applying different potentials to the wafers. The samples have been grown under otherwise identical conditions: $T = 500\degree \text{C}$, $\Phi_{SiH_4} = 20 \text{ sccm}$, $I_{arc} = 50 \text{ A}$, $I_{coil} = 9 \text{ A}$, $t = 1500 \text{ s}$, resulting in a growth rate of $2.8 \text{ nm/s}$ and nominal thickness of $4.2 \mu \text{m}$. To compare the structural quality, the FWHM of X-ray rocking curves have been evaluated. In order to suppress the influence of
peak broadening caused by some residual Ge due to the problems described in section 2.2.1, the secondary Bartels monochromator was used during the measurements (see appendix B), thus filtering out fluctuations in the lattice constant parallel to the growth direction. The results are shown in Fig. 2.4. A minimum in peak width is observed around $-12$ V for the substrate potential, which was close to the floating potential of the wafer ($-13.5$ V) without any external shunt resistor or voltage source connected. These results could be correlated to the surface morphology observed by optical microscopy in Nomarski contrast. The samples showing larger peak widths exhibited also higher defect densities and/or higher surface roughness.

As a consequence of these results, the standard value normally used for the substrate potential was changed back from $-8$ V to the floating potential. As the use of the external resistors and voltage source in normal operation became obsolete, the molybdenum spring contacts could be removed again, significantly improving temperature homogeneity.

### 2.2.4 Process homogeneity

An important benchmark for a deposition process in view of commercial applications is its homogeneity across the substrate surface. Due to the position of the plasma source, the anode geometry, and the focusing of the plasma discharge by means of the axial magnetic field, the lateral plasma intensity distribution is highly nonuniform, showing a maximum in the center and decreasing to-
2.2. Improvements to the process

Towards the chamber walls. In order to nevertheless achieve sufficiently uniform deposition across the substrate surface, four electromagnets had been mounted outside the chamber walls, which serve to horizontally sweep the plasma column across the wafer (the wobbler). It had been shown that for 3-inch substrates the resulting homogeneity even under fully focused plasma conditions (i.e. maximum axial magnetic field) was satisfactory [28]. With the conversion of the system to 4-inch substrates, this problem became much more pronounced. It turned out that under fully focused plasma conditions, the maximum resulting film thickness exceeds the average thickness by up to 50%. We examined the dependence of the homogeneity on different process parameters by means of spectral ellipsometry [29]. A high-resolution X-ray measurement (not shown) done for comparison showed good agreement. The results are presented in table 2.2. All the samples consisted of a 100-200 nm thick Si$_{0.5}$Ge$_{0.5}$ film, grown at 500°C using a flux of 8.1 sccm SiH$_4$, 8.1 sccm GeH$_4$, and 5 sccm H$_2$. 7 samples have been prepared at a growth rate of \( \approx 3.5 \text{ nm/s} \) (averaged over the wafer), and 2 have been grown at lower arc and coil current, resulting in a lower growth rate of \( \approx 3 \text{ Å/s} \).

Three important conclusions can be drawn from these results:

- The wobbler in its present setup is not efficient (\( \sigma = 24\% - 32\% \) with wobbler compared to 33\% without).
- A higher coil current (stronger focusing) enhances the inhomogeneity, as expected.
- Despite the apparent failure of the wobbler to efficiently broaden the intensity distribution, it is basically possible to deflect the plasma intensity maximum completely to the wafer edge of a 4-inch substrate as shown in Fig. 2.5.

From these experiments it follows that the problem of insufficient homogeneity can in principle be solved by the use of stronger wobbler magnets, and possibly a modified design of the plasma source and the auxiliary anode providing a broader plasma intensity distribution. These issues will have to be addressed in the future.

2.2.5 Demonstration of ultrathick epitaxial films

To demonstrate the feasibility of very thick epitaxial films, Si layers up to nominally 50 \( \mu \text{m} \) and VS's up to nominally 17 \( \mu \text{m} \) thickness have been prepared. In Fig. 2.6(a) we show an AFM image clearly exhibiting mono-atomic steps on the surface of the 50 \( \mu \text{m} \) thick Si film, proving its epitaxial nature. Fig. 2.7 shows an X-ray \( \theta - 2\theta \) scan (cf. appendix B) obtained from a virtual SiGe substrate containing a 7 \( \mu \text{m} \) thick graded buffer layer with a Ge content increasing from 0
<table>
<thead>
<tr>
<th>Sample</th>
<th>(\frac{I_{\text{arc}}}{I_{\text{coil}}} ) [A]</th>
<th>Thickness [nm]</th>
<th>(\sigma ) [%]</th>
<th>Wobbler</th>
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<tbody>
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<td>50/9</td>
<td>139</td>
<td>28</td>
<td>10 V</td>
</tr>
<tr>
<td>#5853</td>
<td>50/9</td>
<td>131</td>
<td>31</td>
<td>12.5 V</td>
</tr>
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<td>#5877</td>
<td>50/9</td>
<td>139</td>
<td>32</td>
<td>10 V, new position</td>
</tr>
<tr>
<td>#5879</td>
<td>50/9</td>
<td>125</td>
<td>24</td>
<td>12.5 V, new position</td>
</tr>
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<td>33</td>
<td>—</td>
</tr>
<tr>
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<td>50/9</td>
<td>131</td>
<td>28</td>
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</tr>
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<td>#5890</td>
<td>50/9</td>
<td>82</td>
<td>44</td>
<td>Static</td>
</tr>
<tr>
<td>#5862</td>
<td>30/3</td>
<td>237</td>
<td>18</td>
<td>12.5 V</td>
</tr>
<tr>
<td>#5863</td>
<td>30/3</td>
<td>183</td>
<td>16</td>
<td>—</td>
</tr>
</tbody>
</table>

Table 2.2: Results of the deposition homogeneity measurements done by spectral ellipsometry. The thickness has been determined at discrete points in a rectangular grid with a 1 cm spacing (cf. Fig. 2.5). The thickness values given are the arithmetic means. \(\sigma\) denotes the standard deviation of the measured thickness values. Where a voltage is given in the wobbler column, the plasma was swept in a circular motion across the substrate by applying two sine-shaped AC voltages with a frequency of 2 Hz, offset by \(\pi/2\), to the 2 pairs of wobbler magnets. For samples #5877 and #5879, the wobbler magnets have been moved upwards to lie above the auxiliary anode, while for the other samples they were mounted just below the position of the anode. For sample #5890, the plasma has been statically deflected to one side with a strong permanent magnet, whereas for #5886, this permanent magnet has been rotated in the same position outside the chamber, also leading to a periodic movement of the plasma column.

Figure 2.5: Results of the homogeneity measurements done by spectral ellipsometry. The plots show isocontour lines of the thickness distribution across a 4-inch wafer for samples (a) #5863 (low focusing, no wobbler, cf. Table 2.2) and (b) #5890 (plasma statically deflected). The crosses mark the points where the thickness has been measured; the contours correspond to a 4th order fitted surface.
2.3. Si homoepitaxy

Figure 2.6: (a) AFM image of a 50 µm thick homoepitaxial Si film (sample #5919). Mono-atomic steps are clearly visible, indicating still perfect epitaxial growth in step-flow mode after 50 µm. (b) AFM image of a 17 µm thick Si$_{0.3}$Ge$_{0.7}$ virtual substrate, containing a 7 µm thick compositionally graded SiGe buffer layer and a 10 µm thick Si$_{0.3}$Ge$_{0.7}$ layer of constant composition (#6056). The surface exhibits the usual cross hatch morphology typical of relaxed, graded SiGe layers. No defects are visible.

to 70% followed by a 10 µm thick Si$_{0.3}$Ge$_{0.7}$ layer. The sharpness and intensity of the peak originating from the constant composition SiGe layer indicates its good structural quality. In Fig. 2.6(b) an AFM image of the surface morphology of this sample is shown, exhibiting a perfect, defect free surface showing the normal cross hatch morphology as expected from a relaxed, virtual SiGe substrate (cf. section 3.1.1). The samples have been grown at average growth rates of $\approx$4.5 nm/s and $\approx$8 nm/s, respectively.

2.3 Si homoepitaxy

The deposition of Si films on Si(001) substrates by LEPECVD had been used extensively during the early stages of the development of the process. As the research moved on towards SiGe technology later, no detailed Si homoepitaxy studies have been performed. Nevertheless, due to the generally lower adatom mobility of Si, the deposition of pure Si films is much more sensitive to any kind of contamination or process-induced defects. Already at relatively low Ge concentrations, segregation can lead to a significant surface concentration of Ge atoms exhibiting higher adatom mobility and at the same time a higher hydrogen desorption rate due to the lower energy of the Ge-H bond compared to Si-H. These effects lead to a an improved self-annealing of surface defects during growth in the presence of Ge. It is therefore favorable to use homoepitaxial
Figure 2.7: X-ray $\theta - 2\theta$-scan of the same sample as in Fig. 2.6(b). The strong, sharp peak at a Ge concentration of 70% originating from the top constant composition part of the virtual substrate confirms the good crystalline quality even after 17 $\mu$m of epitaxial growth.

Si films for optimizing growth conditions and assessing the purity level of the process and the sample preparation.

### 2.3.1 Identification of growth defects

An important task during process development is the identification of growth defects, the careful examination of which can lead to a better understanding of the microscopic mechanisms prevailing during deposition. Here only a a short treatment of the commonly observed surface features will be given. The analytic technique of choice for their examination is optical microscopy, AFM or an equivalent method like scanning electron microscopy (SEM), due to the easy and fast application to process control.

**Stacking fault mounds**

The most commonly observed surface features are pyramid-shaped mounds, which are the traces of stacking faults nucleated either at the substrate interface or during layer growth [30]. They have been referred to as “plasma defects” in [28], as they were believed to be due to ion damage caused by the plasma. This hypothesis was based on their disappearance upon the introduction of molybdenum spring contacts to the wafer backside in order to improve control.
over the substrate potential and hence ion energies. However, it could be shown later that they still can appear, e.g. due to contamination. So they were found to nucleate preferentially in chemically contaminated areas on the wafer, e.g. decorating the cleaning stains resulting from handling errors during RCA cleaning steps or during the HF dip employed for oxide removal. This is consistent with very early observations [30]. Defects of this kind have as well been found in samples prepared with MBE [31], UHV-CVD [26] and LPCVD [32].

The often distinctly inhomogeneous distribution excludes nucleation of purely plasma induced defects. To date it has not become ultimately clear whether a homogeneous background density of these defects, which is sometimes observed, is due to a homogeneously contaminated substrate surface or process-based contamination sources like outgassing system parts or insufficiently purified process and precursor gases. Further clarification is to be expected as a result of the installation of point-of-use gas purifiers, which have been added to the experimental system as a result of this work.

Also as yet unclear is the exact interplay between the plasma intensity and the substrate temperature in the formation of these defects, as usually their density is found to increase towards the sample border, where the plasma density as well as the temperature are lower. This behavior suggests either some influence of the plasma (with a higher intensity suppressing or slowing down defect nucleation) or the temperature (with a higher temperature promoting self-annealing of already nucleated defects).

The pyramidal shape aligned along (110) is a consequence of the intersection of the stacking-fault-propagating {111} planes with the (001) surface. An example of a 1.8 μm thick Si film grown at 600°C exhibiting these defects with a density of about 10⁶ cm⁻² is presented in Fig. 2.8. They are rather dome-shaped at this temperature; for higher temperatures, however, the pyramidal shape is quite well defined as shown in the inset. There one single defect is shown on the surface of a 14 μm thick strained graded SiGe film with x_f = 1%, grown at 675°C. As expected from the formation mechanism, the lateral dimension of the observed surface features scales linearly with film thickness, which is also consistent with the assumption of the nucleation site being located at the substrate interface. This is also indicated by the rather homogeneous size distribution observed here.

2.3.2 Self-organized Si structures

With the advent of deposition techniques capable of atomic-layer control of film thickness in combination with atomic-resolution scanning probe microscopy techniques, a large field of self-organized nano-structures has opened up. Most of the work deals with strain-induced formation of ripples or islands, with the
strain provided by the epitaxial growth of lattice mismatched films. But also in homoepitaxy self-organization can be observed, either by externally applying mechanical stress or by exploiting the surface step structure and dynamics.

Recently, Schellmg and co-workers have studied in detail self-organization phenomena observed on vicinal Si(001) and SiGe(001) surfaces. They identified novel kinetic growth instabilities during Si homoepitaxy by MBE at low temperatures and attributed them to effects caused by the dynamics of surface step motion and step bunching. They found rather narrow temperature-growth rate parameter windows for these structures to be observed [33, 34, 35, 36].

In a different range of temperatures and growth rates, we observed self-organized structures also in LEPECVD-grown homoepitaxial Si films, though with a rather different appearance. The temperatures we used were between 500°C and 720°C, and the growth rates in the range of 0.3–3 nm/s. We found rather puzzling surface structures, exhibiting a strong temperature dependence. Due to the inhomogeneous temperature distribution across the wafer, a certain temperature range was accessible simultaneously for each sample. Fig. 2.9 shows a set of AFM images taken at different locations from the surface of a Si film grown at nominally 700°C with a growth rate of 3 nm/s to a nominal thickness of 50 µm. Fig. 2.9(f) shows a sketch of the wafer with the locations indicated where the different images have been taken. In addition, the three small rectangular areas represent the spots where the wafer was supported by the substrate holder, and the shaded areas correspond to regions where the sample surface is covered by a huge density of stacking fault mounds, giving it an optically rough appearance. It is reasonable to assume that these contours follow precisely the temperature distribution, which is influenced by heat con-
2.4 Microcrystalline silicon

production from the substrate support and by shielding from the additional spring contacts mounted between the substrate and the heater, located in the spaces between the supporting plates (cf. section 2.2.3). The temperature is highest in the center and decreases towards the border. Unfortunately, the absolute value of the temperature lowering is unknown.

Three completely different regions can be identified apart from the defective areas shown in Fig. 2.9(f). Starting from the cooler temperatures, at position (a) the Si film appears to be atomically flat with an rms roughness < 1 nm; only a very faint cross-hatch-like structure is visible, whose origin remains unknown. A significant Ge concentration in the film can be excluded, as the sample has been prepared after the GeH₄ gas line had been evacuated (section 2.2.1) and prior to this sample, more than 100 μm of material has been deposited since the last sample with a Ge concentration larger than 1%. The epitaxial growth is indicated by the presence of a well ordered, flat surface step structure (an AFM image taken at higher resolution of this area can be found in Fig. 2.6(a) on page 19). At position (b), shallow round pits with diameters of 0.1 – 1 μm start to appear, slightly raising the rms roughness to about 1 – 2 nm. As the substrate temperature increases to position (c), the surface becomes completely dominated by shallow, rather round crater-like features whose boundaries show no preferential orientation. At this stage, the rms roughness reaches 5 – 6 nm. As the substrate temperature increases further to (d), the boundaries of these craters start to align themselves along (110) directions with the rms roughness remaining unchanged. At the highest temperature in (e) finally, the craters have disappeared, completely leaving behind a disordered array of (110) oriented ripples while the rms roughness doubles to about 12 nm.

The strong temperature dependence of the observed features in combination with their obvious crystalline nature suggests a kinetic origin similar to the findings by Schelling et al. However, for a detailed interpretation of the features found in the case of LEPECVD further research will be needed.

2.4 Microcrystalline silicon

Hydrogenated microcrystalline Si (μ-Si(H)) and amorphous Si (α-Si(H)) films fabricated on cheap substrates like glass or flexible polymers are becoming increasingly interesting due to their applications in solar cells, liquid crystal displays, image sensors, and printer arrays. The growth mechanisms and the control over the microstructural properties of such films are crucial for their electronic properties and they strongly depend on the growth technique. The most important method for the growth of such Si films is plasma enhanced chemical vapor deposition (PECVD). It may therefore seem straightforward to apply LEPECVD to this task and study the basic features of microcrystalline
Figure 2.9: $10 \times 10 \, \mu m^2$ AFM images taken at different locations of sample #5919 as indicated in (f). The different locations correspond to different substrate temperatures during deposition — see text for discussion.
2.4. Microcrystalline silicon

<table>
<thead>
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<th>Sample</th>
<th>$\Phi(\text{SiH}_4)$</th>
<th>$\Phi(\text{H}_2)$</th>
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Table 2.3: Parameters used for the $\mu/\alpha$-Si(H) samples (silane and hydrogen flows in sccm, resulting dilution factor $d = \Phi(\text{SiH}_4)/\left(\Phi(\text{SiH}_4) + \Phi(\text{H}_2)\right)$, nominal thickness $t$ and growth time $\tau$). The growth temperature for all samples was 450°C.

films synthesized using this process and their dependence on some process parameters. The control over the structure and the size of the grains, passivation of defects and grain boundaries is essential during the growth of microcrystalline silicon films. Modern device fabrication technologies require high crystalline quality, preferably large grains in a columnar structure and a large growth rate, two requirements which normally counteract one another.

2.4.1 Sample preparation

4-inch glass substrates were outgassed at 450°C for 30 min, then a 2-min hydrogen plasma clean was applied at the same temperature using a gas flow of 5 sccm H$_2$ and an Ar flow of 50 sccm. The films were then deposited at the same substrate temperature of 450°C, using different SiH$_4$ and H$_2$ flows leading to different dilution ratios $d = \Phi(\text{SiH}_4)/\left(\Phi(\text{SiH}_4) + \Phi(\text{H}_2)\right)$. The arc current used was $I_{\text{arc}} = 40$ A and the magnetic field coil current $I_{\text{coil}} = 9$ A. To improve the heating of the transparent glass substrates, a Si wafer was brought in contact with the substrate on the back side. Table 2.3 shows the parameters used for the series of samples.

2.4.2 Results

Deposition rate

Fig. 2.10 shows the growth rate as a function of the hydrogen dilution $d$. For its determination, the thickness of the films has been measured by optical interference and was checked with an alpha-step profiler. TEM cross-sections further confirmed the obtained values, which lie somewhat higher than the
Figure 2.10: Deposition rate as a function of hydrogen dilution. The diamonds show the absolute deposition rate, the boxes correspond to the deposition rate normalized to a silane flow of 20 sccm. The growth rate is roughly proportional to the silane flux, but decreases with increasing hydrogen dilution \( d \): upon diluting the silane to 9.1\%, the deposition rate decreases by about 30\% compared to the growth from pure silane.

nominal values, with \( \approx 1.5 \mu m \) for \( \#5762 - \#5766 \) and \( \approx 4.5 \mu m \) for \( \#5767^3 \). Taking into account the inhomogeneity of the deposition and the determination of the film thickness in the center, the growth rates do not differ substantially from the ones observed for epitaxial growth by LEPECVD. As expected, with increasing hydrogen dilution the growth rate decreases due to the lower flux of silane. When the deposition rate is normalized to a constant silane flow of 20 sccm, it becomes obvious that the deposition rate decreases slightly with increasing hydrogen dilution, dropping by as much as 30\% for the highest dilution (to 9.1\%) compared to the growth from pure silane. This indicates that, despite of the efficient enhancement of the growth kinetics by means of the plasma, the growth can still be influenced by the presence of high concentrations of hydrogen.

**Crystalline structure**

The crystalline structure of the obtained films was investigated with standard X-ray diffraction (XRD) using FeK\(_\alpha\) radiation at \( \lambda = 1.93604 \) Å (see appendix B). The results are presented in Fig. 2.11. The films at low dilution appear to be amorphous; for \( d \leq 50\% \) crystallites with (111) and (220) orientation are formed, with the degree of crystallinity increasing with increasing dilution \( d \).

\(^3\)The nominal values correspond to a thickness average over the substrate, while the measured values correspond to the sample center, where the plasma intensity is the highest — cf. section 2.2.4.
2.4. Microcrystalline silicon

Figure 2.11: XRD measurements of the microcrystalline Si samples. While for low dilution of the silane with hydrogen the films turn out to be amorphous, crystallites showing (111) and (220) reflections appear for $d \leq 50\%$.

These findings could be corroborated from Raman scattering measurements carried out at an excitation wavelength of 537 nm (Fig. 2.12). For the samples with $d = 1$ and $d = 0.75$, only a shallow peak around 480 cm$^{-1}$ attributed to amorphous Si is observed, whereas for increasing dilution a sharp peak at 520 cm$^{-1}$ originating from the Si-Si mode of crystalline silicon appears.

Influence of film thickness

To investigate the influence of the film thickness on the crystallinity, sample #5767 with $d = 50\%$ has been grown to a nominal thickness of 4 $\mu$m. XRD measurements comparing the two $d = 50\%$ samples are shown in Fig. 2.13. The thicker film exhibits a higher degree of crystallinity and a higher (220) orientation. This has great impact on the device performance. Normally a high degree of (220) orientation leads to the desirable columnar morphology; here, at a dilution ratio of $d = 50\%$, we obtain a degree of (220) orientation that is usually only achieved for significantly higher dilution ratios ($d \leq 10\%$).

Conclusions

These first experiments to deposit hydrogenated microcrystalline Si on glass substrates by LEPECVD led to very promising results, showing the great potential of the process for applications reaching beyond epitaxial growth. Clearly this is just a beginning, and much more work has to be done to really assess the possibilities offered for the deposition of amorphous, micro- and polycrystalline materials.
Figure 2.12: Raman spectra of the $\mu/\alpha$-Si(H) sample series. The findings of the XRD measurements are confirmed, with the Si-Si line at 520 cm$^{-1}$ originating from crystalline silicon appearing for $d \leq 50\%$, while for higher silane concentrations only the signal from the amorphous phase at 480 cm$^{-1}$ is observed.

Figure 2.13: Thickness dependence of the crystallinity as measured by XRD.
Chapter 3

SiGe device applications

3.1 Virtual SiGe substrates

As already pointed out in section 1.3, the fabrication of virtual substrates is of key importance for SiGe devices. In this section, we will discuss the application of LEPECVD to the growth of SiGe VS’s.

The basic structure for many kinds of SiGe devices is shown in Fig. 3.1. Although this concept of the VS has been established for more than 10 years now, most of the work has been focused on Ge concentrations up to only 30 – 40%, which are used for strained Si channels exhibiting high-mobility electron transport. The main reason is that the higher concentration range is not easily accessible due to the low grading rate needed in order to keep the TD density low. For higher Ge concentrations, the resulting film thickness starts to exceed the range that is easily achieved with traditional epitaxy techniques due to their low growth rates. Other problems concern limitations of the deposition mechanisms; in UHV-CVD, e.g., the growth temperatures needed for sufficiently high growth rates lead to massive roughening of the Ge rich films. The goal of this work was to exploit the large experimentally accessible range of parameters of LEPECVD to study the dependence of several properties of such VS’s on different parameters for higher Ge concentrations, in view of device applications relying on strained Ge-rich or pure-Ge channels. The results have been used to optimize process parameters in order to achieve good structural and electronic quality of the VS for use in different types of strained-layer SiGe heterostructure devices. The different parameters employed were the final Ge concentration $x_f$, the grading rate $r_G$ in the graded buffer layer, the thickness of the constant composition layer, and the temperature profile.

We have prepared different VS’s with Ge end concentrations between 40%
Figure 3.1: The basic structure of a SiGe device based on a virtual SiGe substrate. The figure shows the case of a structure consisting of a graded buffer layer followed by a constant composition layer of Ge concentration $x_f$, on top of which a thin, strained pure Ge film is grown which forms a channel for high-mobility holes.

and 100%, with grading rates between 5%/um and 40%/um, average growth rates of 5-7 nm/s and using different temperature profiles. It turned out that a grading rate of 10%/um and temperatures between 500°C and 750°C lead to good results, where the temperature is lowered for higher Ge concentrations to reduce thermally activated, strain-induced roughening of the films. The VS’s have been characterized using atomic force microscopy (AFM), high-resolution X-ray diffraction (HR-XRD), cross-sectional transmission electron microscopy (X-TEM), and defect etching in combination with AFM.

3.1.1 Surface morphology

AFM was used in order to optimize the growth parameters in terms of surface roughness caused by the relaxation mechanism and strain modified growth kinetics. We used a ParkScientific M5 scanner, usually in non-contact mode in air, using standard Si cantilevers and tips. The surfaces of relaxed lattice mismatched epitaxial films in the diamond or zinc blende crystal structure exhibit a characteristic ‘cross hatch’ pattern [37], as visible e.g. in Fig. 3.2(b), as a consequence of the MD network in the graded SiGe buffer layer (cf. appendix A). The MD’s, aligned along (110) with a Burgers vector $b = a/2 \langle 011 \rangle$, cause a crystal displacement perpendicular to the film surface of $a/2$ (where $a$ is the lattice constant). In addition, the strain field from the dislocation line, when extending up to the growth surface, can modify the growth kinetics, leading to a further enhancement of the amplitude of this surface slip [38]. The high density of MD’s required for fully relaxing a VS can thus lead to significant surface roughening, which could adversely affect subsequently grown strained-
layer heterostructures. While the length scale of these surface features usually is too large to affect transport properties, they remain a major concern in view of subsequent device processing (e.g. for photolithography). In addition, the surface strain fields due to the most pronounced cross hatch lines have been shown to block dislocation propagation, resulting in band-shaped dislocation bunches (cf. Fig. 3.10) causing an increase in TD density [39] and eventually limiting device performance and production yields.

One approach for obtaining a smoother surface is the use of ex-situ chemical-mechanical polishing (CMP), which has been successfully applied to UHV-CVD grown samples by Fitzgerald et al. [39, 40]. The reason for the high surface roughness in those UHV-CVD films is the relatively high growth temperature, which was kept at close to 800°C for concentrations up to pure Ge. At these temperatures, for high Ge concentrations the surface mobility of adatoms during growth is high enough to keep the growth interface close to its thermodynamic equilibrium shape, which is strongly affected by the long-range strain fields from the MD network and local surface strain fields from pre-existing cross hatch ridges and trenches.

The ability of LEPECVD to grow thick SiGe layers in a wide temperature range without affecting the growth rate and film quality, allows for lowering the temperature during growth as the Ge content is increased, which suppresses roughening of the surface without the need for additional processing steps. While the growth is started at temperatures above 700°C for low Ge concentrations to propagate dislocation nucleation and motion at the beginning of the graded buffer layer, a gradual reduction of the growth temperature for Ge concentrations higher than \( \approx 30\% \) successfully lowers the strain-induced surface roughening, without prohibiting further relaxation, at least at \( T \geq 500°C \) and at grading rates \( \leq 10\%/\mu m \).

To illustrate the effect of lowering the temperature on surface morphology, in Fig. 3.2 we show AFM surface images of two \( \text{Si}_{0.3}\text{Ge}_{0.7} \) VS’s grown using different final temperatures \( T_f \). The lower \( T_f \) leads to a significantly improved surface morphology. For VS’s graded to pure Ge, we were able to find an optimized growth sequence resulting in an astonishingly flat surface exhibiting only mono-atomic steps, as shown in Fig. 3.3.

### 3.1.2 Structural assessment

HR-XRD has been used extensively to assess the structural properties of the LEPECVD VS films. Of special interest was the determination of composition, relaxation, and crystallographic tilt. For an introduction to the experimental setup and the different measurement types employed, refer to appendix B. To obtain direct-space information about the dislocation network and the substrate interface, cross-sectional TEM has been employed in a few cases.
Figure 3.2: Comparison of the surface morphology of two VS’s with $x_f = 0.7$ imaged by AFM. Both samples consist of a graded buffer layer with a grading rate of 10%/μm and a 1 μm thick $Si_{0.3}Ge_{0.7}$ layer. For both samples growth started at $T_i = 740° C$. The temperature was lowered to $T_f$ during the concentration range of 35-70%. (a) Shows sample #6055 with $T_f = 620° C$, (b) #6059 with $T_f = 500° C$. Not only is the rms roughness of the low-temperature sample with $≈ 2.5$ nm much smaller than for the higher-temperature one ($> 10$ nm), but the surfaces look qualitatively different. At $T_f = 620° C$, the surface exhibits a mosaic-like structure, with narrow, 100-200 nm deep trenches running along (110) directions, while lowering the temperature to 500°C results in a smooth, continuous cross hatch pattern with a maximum amplitude of only $≈ 15$ nm.

Composition

The most suitable measurement type for determining the composition of SiGe alloys with known strain state is the HR-XRD $\omega - 2\theta$ scan of the (004) Bragg peak (thus for (001) oriented samples, $\omega = \theta$). As all of the thick relaxed SiGe buffer layers involved in our VS study showed complete relaxation within the measurement accuracy, their composition could easily be determined by this technique. Apart from the Si substrate peak always present, the obtained spectra show a continuum of scattered radiation towards lower $\theta$ values corresponding to the larger vertical lattice constant of the SiGe alloy layers with increasing Ge composition. In the presence of a layer of constant composition $x_f$, a second peak at the corresponding $\theta$ value is obtained. From equation (B.1), the spacings of the (004) planes and thus the vertical lattice constant can then be calculated directly

$$a_{\perp} = 4 \cdot d_{004} = 4 \frac{\lambda}{2 \sin \theta} \approx \frac{3.081 \text{ Å}}{\sin \theta}$$  (3.1)
3.1. Virtual SiGe substrates

Figure 3.3: AFM image of a pure-Ge virtual substrate. Growth started at $T_i = 720^\circ C$, the temperature was lowered during deposition to $T_f = 500^\circ C$. After a 10 $\mu$m thick graded buffer layer and 1 $\mu$m of pure Ge, growth was interrupted and the sample was annealed for 10 min at 700$^\circ C$. Then, an additional 3 $\mu$m of pure Ge has been deposited at 650$^\circ C$. The surface exhibits, apart from mono-atomic surface steps that indicate the perfect epitaxial growth in step-flow mode, only single slip lines from misfit dislocations introduced presumably during cool-down to room temperature.

for CuK$\alpha_1$ radiation. In the case of fully relaxed films with an undistorted cubic crystal lattice, the concentration $x$ can then easily be determined by using the inverse of (A.4).

Fig. 3.4 shows an example of such a $\omega - 2\theta$ measurement obtained from a nominally 70% VS with a 1.5 $\mu$m thick constant composition layer. The peaks have been fitted to Gaussians in order to calculate their FWHM, which is useful for qualitative comparison of differently prepared samples. The resulting $x_f$ of 68.7% instead of the intended 70% is due to a small calibration error in the settings of the mass flow controllers. It turned out that the employed MFC’s do not show a perfectly linear behavior, which makes an accurate calibration of the flow ratio over the whole concentration range a tedious task. For these studies, which did not require a stringent control of the absolute value of $x_f$, a simple linear extrapolation of the flow ratio giving rise to a 40% alloy was employed. However, the scattering of the real alloy concentration between different samples grown using the same gas compositions was < 1%.

Crystallographic tilt

It has been known before that the growth on vicinal surfaces can modify the nucleation behavior of dislocations, leading to preferred orientations for the
Figure 3.4: HR-XRD θ–2θ scan through the (004) Bragg peak of a 70% VS, revealing peaks originating from the Si substrate, the graded buffer and the constant composition SiGe top layer with $x_f = 68.7\%$. As can be seen from the small FWHM of the SiGe peak, the spread in Ge concentration is very small.

misfit dislocations which results in a net crystallographic tilt of the epilayer with respect to the Si(001) substrate [41]. This is due to the inclination of the Burgers vector both with respect to the surface normal and the surface plane. Every MD thus causes a small tilting of its surrounding crystal lattice. By multiplication and glide in one single {111} glide plane, several of these microscopic tilts can add up. The resulting mosaicity could be observed directly by X-ray microdiffraction [42], where a map of the local tilt distribution of graded SiGe layers has been determined using an extremely narrow X-ray beam (1 µm×5 µm). This mosaic structure could not be resolved, however, in the case of constant SiGe layers grown directly on Si(001), which is a consequence of the much higher density of (very short) MD’s all located at the substrate interface, causing the tilted regions to be much smaller than the beam dimensions. A small miscut of the substrate (deviation from a perfect (001) surface orientation) can now change the driving forces for both nucleation and motion of MD’s by affecting the projection of the Burgers vector to the surface plane, thus giving rise to a preference of one glide system and consequently a macroscopic tilt of the relaxed layer.

An example of two HR-XRD rocking curves obtained from a 70% VS exhibiting this crystallographic tilt is shown in Fig. 3.5. The observed $\omega$-shift can be used to accurately determine the amount of tilt, if it is measured for several angles of sample rotation. The $\omega$-separation of the SiGe and the Si peak will
3.1. Virtual SiGe substrates

Figure 3.5: HR-XRD (004) rocking curves obtained from a 70% VS with a 7 µm thick constant SiGe layer (#6043), which is tilted with respect to the Si(001) substrate. This tilt leads to an ω-shift of the peak as the sample is rotated around its surface normal; RC2 has been measured after rotation of 180°.

then show a sinusoidal dependence on the sample rotation angle, which can be numerically fitted resulting in the average peak separation (corresponding to $x_f$) and the amplitude of the peak shift (equal to the tilt angle). This procedure is demonstrated for the same sample in Fig. 3.6.

Relaxation

In view of device applications, it is of utmost importance for the VS's to be fully relaxed. Significant residual strain could lead to further relaxation during device processing or operation, changing the strain state and thus the electronic properties of device layers or even introducing defects. To determine the strain state distribution in the VS, HR-XRD reciprocal space mapping is the method of choice as it delivers all the necessary information. However, the presence of tilting as described above complicates the situation, as the influence of the tilt on the angular shift of diffraction peaks has to be separated from the shift arising from changes of the unit cell dimensions due to compositional changes and strain. The usual approach is to first consider a Bragg peak, whose corresponding scattering vector lies in the growth direction, usually the (004) peak due to its high intensity. From the resulting data, the relation between the perpendicular component of the scattering vector and the tilt $\Delta \omega(q_{\perp})$ can be calculated by determining the deviation of the center-of-mass of the diffracted intensity distribution from $q_{\parallel} = 0$ for every value of $q_{\perp}$. The resulting (numerical) correction function can then be applied to the measurement of a second Bragg peak, whose diffraction vector now also has an in-plane component $q_{\parallel}$,
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Sample rotation

Figure 3.6: Sinusoidal fit to the $\omega$ peak separations obtained from several HR-XRD rocking curves from #6043. The fit results in accurate values for $x_f$ and the tilt angle.

For this correction to be applicable, great care must be taken not to change any adjustments of the X-ray apparatus between the two measurements — a slightly different orientation or location of the illuminated part of the sample can distinctly change the local tilt distribution.

The corrected data from this measurement reflect the profile of the true shape of the unit cell throughout the concentration range involved. Such a combined RSM obtained from a 56% VS grown at 720 – 680°C is presented in Fig. 3.7. The inclined dashed line in the (224) plot represents the connection between the Si(224) peak and (000) and thus corresponds to the locus of all the (224) reflections originated from layers with cubic unit cell. As can easily be seen, throughout the VS the center-of-mass of the intensity distribution follows this line, indicating that all the layers have cubic unit cell and thus are fully relaxed. The faster decaying intensity towards the substrate in the (224) measurement is a direct consequence of the longer X-ray path leading to higher absorption in the sample due to the significantly smaller angle of incidence ($\omega \approx 8^\circ$ for the (224) peak compared to $\omega \approx 35^\circ$ for the (004) peak).

As it turned out that for Ge-rich VS’s the substrate temperature has to be lowered substantially during growth in order to obtain a flat surface morphology, it has to be shown that full relaxation is still achieved at these temperatures. For this purpose we show the same kind of RSM for a 100% VS, for which the temperature had been lowered to 550°C in Fig. 3.8. Unfortunately, the condition of identical adjustment of the sample between the two measurements could not be fulfilled in this case, due to problems with the sample holder. This is reflected in the tilt correction not being exactly accurate as can
3.1. Virtual SiGe substrates

Figure 3.7: 2-peak RSM obtained from the 56% VS #5711. From the (224) intensity distribution following the inclined line representing cubic unit cells, full relaxation throughout the film can be deduced.

be seen from the Ge peak in the (224) plot showing a slightly smaller $q_{\perp}$ value than in the (004) plot, what indicates that the (224) data should have been shifted a bit farther towards the top right (positive $\Delta \omega$ direction).

Both the 'realistic' (224) data obtained in this way and the (004) data then show a tensilely strained or overrelaxed Ge top layer! The only reasonable explanation for this behavior is the different thermal expansion coefficient of Ge and Si. While during deposition at 550°C the Ge layer is fully relaxed, upon cool-down to RT it would like to contract faster than the underlying Si substrate leading to tensile thermal stress (see section 3.1.4 below). Because the temperature is not sufficient for plastic relaxation any more, the film will end up being strained. As a consequence, the concentration of the top layer seems to be slightly lower than 100% if one considers the lattice constant in the growth direction ($a_{\perp}$) only, due to the crystal lattice being contracted in the growth direction. Nevertheless, the measurement serves as a proof for full relaxation even at the reduced growth temperature.

Once the composition of the alloys with intermediate Ge concentrations has been calibrated with RSM's taken from fully relaxed VS's, it is sufficient to measure $\theta - 2\theta$ scans for subsequent samples, as then the final concentration is known and $a_{\perp}$ is measured, from which the degree of relaxation can be directly derived. In this way it has been verified that VS's with $x_f = 0.7 - 1$, even when grown with $T_f = 500°C$, are still fully relaxed.
Figure 3.8: 2-peak RSM obtained from a pure-Ge VS grown with reduced temperature $T_f = 550^\circ C$. The top Ge layer appears to be tensilely strained, which can be attributed to thermal stress caused by the different temperature expansion coefficients of Si and Ge.

3.1.3 Threading dislocations

Apart from the surface morphology and the degree of relaxation, the third important property of a VS for device applications is the density of threading dislocations penetrating its surface. The parameter most strongly affecting the TD density is the grading rate in the graded buffer layer. The first attempts using single-step buffers (without a graded buffer layer) resulted in TD densities between $10^9$ and $10^{11}$ cm$^{-2}$, resulting in a poor performance of the first modulation doped heterostructures [43]. It could be shown later that a TD density below $10^8$ cm$^{-2}$ is necessary in order not to limit carrier mobility in the active layers [25]. A second issue raised by TD’s is an increase in leakage current of field effect transistors fabricated on VS’s with too high a TD density. For realistic applications a VS should have a TD density on the order of $10^6$ cm$^{-2}$ or below. We have prepared a series of 70% VS’s with grading rates between 40%/μm and 5%/μm, each one with a 1 μm thick constant composition $Si_{0.3}Ge_{0.7}$ layer on top, resulting in a nominal film thickness between 2.75 μm and 15 μm. The average growth rate was 4.2 nm/s for all samples. Growth started at $T_i = 740^\circ C$ and was lowered towards higher Ge concentration to $T_f = 620^\circ C$. The TD density was determined by defect etching and subsequent AFM imaging. The results are shown in Fig. 3.9. As expected, the TD density decreases with decreasing grading rate and starts to saturate at
3.1. Virtual SiGe substrates

![Graph showing TD densities of 70% VS's with different grading rates](image)

Figure 3.9: TD densities of 70% VS's with different grading rates as measured by defect etching and subsequent AFM imaging. The substrate temperature during growth was initially $T_i = 740^\circ C$, and was lowered to $T_f = 620^\circ C$ as the Ge concentration was increased. For determining the densities, areas on the order of $2 \times 10^4 \mu m^2$ have been examined for each sample.

At higher grading rates, the TD density is strongly affected by the formation of clusters of a high number of dislocations in (110) oriented bands, as demonstrated in Fig. 3.10. The mechanism leading to this behavior can be understood as follows: during the evolution of the cross hatched surface, the accumulation of surface strain in the most pronounced trenches can lead to a local lowering of the effective strain which drives the TD motion during the relaxation process. This can eventually arrest the TD's in the vicinity of this cross hatch line, leading to a further local strain lowering, blocking even more TD's. In the end, a large number of TD's is resting immobile close to the cross hatch line, preventing their associated MD segments from growing in length and necessitating the nucleation of additional dislocations, hence raising the TD density.

3.1.4 Thermal stress

As shown above under section 3.1.2, the different thermal expansion coefficients $\alpha$ of Si and Ge can lead to thermal stress. The values for Si and Ge at 300 K (800 K) are $2.5 \cdot 10^{-6} \text{ K}^{-1}$ ($4.3 \cdot 10^{-6} \text{ K}^{-1}$) and $5.7 \cdot 10^{-6} \text{ K}^{-1}$ ($7.2 \cdot 10^{-6} \text{ K}^{-1}$), respectively, with a difference of $\Delta \alpha \approx 3 \cdot 10^{-6} \text{ K}^{-1}$. Cooling a film of pure Ge on a Si substrate from 550°C to RT thus results in a thermally induced strain of $\varepsilon_{th} \approx 0.16\%$ in the Ge film, which amounts to 3.8% of the mismatch between Si and Ge. By linear interpolation, for a Si$_{0.3}$Ge$_{0.7}$ film cooled down from 650°C to RT, we obtain $\varepsilon_{th} = 0.13\%$, which corresponds to the mismatch of a SiGe film with $x = 3.2\%$ with respect to Si (with opposite sign). In other words,
cooling down a Si$_{0.3}$Ge$_{0.7}$ layer from 650°C to RT results in a tensile strain, the magnitude of which is comparable to the compressive strain of a SiGe film with 3.2% Ge content grown directly on Si. This might seem relatively small, but one has to take the film thicknesses of several μm into account. As plastic relaxation by dislocation glide is suppressed at low temperatures, for thick films the resulting stress can become large enough for macroscopic cracks to be formed. This has also been observed in Ge-rich films grown by UHV-CVD [40].

In fact this has been experimentally observed from 70% VS's grown at relatively high temperatures ($\geq 650^\circ$C) or with very thick constant composition layers ($\geq 7$ μm). Upon scratching these samples with a diamond needle along (110) directions, orthogonal cracks running over the whole 4-inch wafers can form. In extreme cases, such cracks have even found to form spontaneously.

Apart from this instability against mechanical treatment, this built-in stress can be a severe problem for low-temperature electrical measurements, where it can happen that a sample behaving perfectly at RT will fail at very low temperatures due to crack formation.

Conclusions

From the surface studies and structural investigations, suitable parameters are obtained for the fabrication of VS's containing a high Ge concentration. While initially temperatures around 720 – 740°C are favorable in order to ascertain the formation of an optimal MD network, for higher Ge concentrations the
growth temperature has to be significantly lowered to \( T_f \) on the order of 500°C to prevent strain-induced, kinetically driven surface roughening. Consistent with the findings for lower values of \( x_f = 30\% - 40\% \), a grading rate around 10%/\( \mu \)m is needed in order to lower the TD density. Further lowering of the grading rate is not found to lead to a significant improvement. Additionally, increasing the thickness of the constant composition layer has been found to adversely affect the structural stability of the films, which is attributed to the accumulated thermal stress in the thicker films. Thermal stress is also an issue with respect to the growth temperature; apart from the surface morphology this serves as additional motivation for lowering \( T_f \) for high Ge concentrations.

### 3.2 Strained SiGe heterostructures

In order to fabricate complete SiGe device structures by LEPECVD, the formation of sequences of thin, strained films with sharp interfaces has also to be mastered. As could be shown in the past, the process parameters used for the deposition of VS’s are not suitable for this purpose, because of strongly enhanced intermixing at the heterointerfaces [28]. However, substantially lowering the plasma density near the substrate has been found to solve this problem. While for the fast growth efficient desorption of hydrogen from the wafer surface by means of the plasma is required, this surface passivation is rather desirable for the growth of abrupt interfaces due to the surfactant effect of hydrogen [44]. By varying the plasma geometry, the amount of surface hydrogen can be tuned in a wide range. To further enhance the surface passivation, the hydrogen concentration in the chamber can be increased by introducing additional \( H_2 \). As an example, Fig. 3.11 shows a HR-XRD rocking curve obtained from a strained-layer superlattice consisting of 10 periods of 1 nm pure Ge and 20.7 nm pure Si. The reasonably slow decay of the superlattice diffraction peaks when compared with the simulated curve, which assumes perfectly abrupt interfaces, indicates the good interface quality achieved using these process parameters. The film has been grown using a lowered coil current of \( I_{\text{coil}} = 3 \) A, resulting in significantly weaker lateral confinement of the discharge column and hence lower plasma density. Consequently, the growth rate decreased by more than an order of magnitude to 2 Å/s, indicating the important role of the plasma for hydrogen desorption from the growth interface. While the reduction of discharge current from \( I_{\text{arc}} = 50 \) A to 30 A had been shown to only marginally affect the rate of precursor gas decomposition, the reduction in growth rate must be attributed to the lower plasma density at the position of the substrate, which will lead to less efficient hydrogen desorption reducing the reactivity of the growth interface.

These process parameters have consequently been employed for all the strained heterostructures requiring sharp interfaces.
3.3 Electronic devices

As important as detailed structural investigations are, the ultimate goal of this research work was the successful fabrication of working electronic devices, showing preferentially superior properties than comparable structures grown using traditional techniques. After process parameters and sequences have been optimized with respect to structural quality, the next step thus has been to assess the electronic quality of LEPECVD-grown material by the fabrication and characterization of electronic device structures. These data are considered to be the main results of this research work.

3.3.1 n-Type modulation doped quantum well (n-MODQW)

Due to the lower Ge content needed in the VS for strained-Si channel based n-type devices, these are easier to fabricate and thus often investigated first. In order to separate the influence of the VS and the quality of the active heterostructure from each other, we fabricated two different kinds of n-type modulation doped quantum well structures (n-MODQW). The first set of samples was grown in a single run using LEPECVD only; for the second, the LEPECVD-grown VS was used for fabricating a state-of-the-art n-MODQW by MBE. The layer stacks used are shown in Fig. 3.12.

**Figure 3.11:** (004) HR-XRD rocking curve of a strained-layer superlattice (#5869) consisting of 10 periods of 1 nm Ge and 20.7 nm Si. The points correspond to the experimental data; the solid line is a simulation using dynamical diffraction theory [45].
3.3. Electronic devices

![Layer structure of the n-MODQW samples. The left stack shows the layer sequence used for the LEPECVD sample, the right one that for the LEPECVD+MBE sample with the MBE-grown part shown shaded.](image)

**LEPECVD n-MODQW**

The best LEPECVD sample obtained during this work consisted of an 8 µm thick VS with $x_f=35\%$, which has been grown at a rate of 5.2 nm/s and a temperature of 720°C. The temperature was then lowered to 520°C, and the plasma density in the vicinity of the substrate was reduced, resulting in a growth rate of about 1 Å/s for the deposition of the MODQW layer stack. The supply layer has been doped using a mixture of 100 ppm phosphine (PH$_3$) in Ar.

For the electrical characterization, a standard Hall bar geometry has been used. The Hall bars have been defined by photolithographic mesa etching; contacts have been fabricated by sputter deposition of Sb/Cr/Au with subsequent rapid thermal annealing (RTA) at 580°C for 120 s.

Low-temperature magnetoresistance and Hall data obtained at 1.7 K are shown in Fig. 3.13. Clearly observable Shubnikov-de Haas (SdH) oscillations in the longitudinal magnetoresistance $\rho_{xx}(B)$, accompanied by integer quantum Hall effect (IQHE) plateaus in the Hall resistance $\rho_{xy}(B)$, indicate the formation of a two-dimensional electron gas (2DEG). From the spacing of the SdH minima a sheet carrier concentration $n_s = 8.2 \cdot 10^{11}$ cm$^{-2}$ can be derived. Putting $n_s$ into equation 1.1 with $E/j = \rho_{xx}(0)$ results in a mobility $\mu=24'000$ cm$^2$/Vs. Although the structure shows a clear mobility enhancement over bulk Si, the observed value is distinctly lower than current record mobilities from the literature exceeding 500'000 cm$^2$/Vs [46]. Although there are also design issues (the record structures used a thicker spacer layer and...
backside gating), it is perfectly clear the material itself still suffers from substantial problems concerning the purity. Due to the very low SdH oscillation amplitude, a precise determination of the single particle relaxation time (see the section on the LEPECVD+MBE n-MODQW below) is not feasible. Regardless of the large uncertainty, the data gives evidence for a low Dingle ratio of the order of 1, which points to the predominance of large-angle scattering. Possible candidates for sources are Coulomb scattering centers in the channel or surface roughness. Excessive surface roughening of the channel can be ruled out as evidenced from earlier TEM measurements performed on similar structures and the current investigation of strained-channel structures at higher Ge concentrations, which are even more critical for channel roughening (section 3.3.3). The sources for a background concentration of charged species in the channel are background doping or contamination by other electrically active species from the precursor and process gases and the chamber parts.

An additional shortcoming of this structure is the occurrence of appreciable parallel conductance, indicated by the higher sheet carrier density determined from the Hall resistance \( n_{s,H} = 1.1 \cdot 10^{12} \text{ cm}^{-2} \), which is probably due to background doping of the VS, caused by the well-known problem of redeposition from the chamber which leads to a strong memory effect (section 2.2.1).

For future experiments, the doping efficiency should be improved by using a different doping procedure. In the present sample, the 25 nm thick supply layer has been homogeneously doped by adding 4.5 sccm PH\(_3\) (100 ppm) in Ar to the total precursor gas flow of 5 sccm \( \Phi(\text{SiH}_4) + \Phi(\text{GeH}_4) \), resulting in a nominal P concentration of \( 4.5 \cdot 10^{18} \text{ cm}^{-3} \). From the observed \( n_s \) in the channel one obtains that only 7.3% of the donors have been ionized and their electrons been

Figure 3.13: Low-temperature magnetoresistance and Hall resistance of the all-LEPECVD sample (#5722) at 1.7 K.
transferred to the channel. First promising experiments indicate that the use of a small number of δ-like doping spikes results in improved behavior. The doping spikes are achieved by stopping the SiH$_4$ and GeH$_4$ gas flows and introducing solely the PH$_3$/Ar mixture into the growth chamber while sustaining the plasma discharge.

The problem of the background doping could further be addressed by a more careful conditioning of the growth chamber or the development of an in-situ cleaning procedure of the system, while the contamination arising from the gases should be strongly reduced in the future with the recent installation of point-of-use gas purifiers.

**LEPECVD/MBE n-MODQW**

In the case of the LEPECVD/MBE sample, the VS has been grown in the same way as for the LEPECVD sample, with a slightly smaller thickness of 7 μm. The wafer was then removed from the chamber, transferred by mail to the MBE lab at DaimlerChrysler in Ulm, Germany, where a standard RCA clean was performed before introducing the wafer into the MBE system, followed by oxide desorption at 800°C and growth of the layer stack at reduced temperature.

Fig. 3.14 shows a low-temperature (1.7K) measurement of the LEPECVD/MBE sample performed in the group of Dr. Paul at the Cavendish Laboratory, University of Cambridge, UK. The high electron mobility of 159'000 cm$^2$/V·s is a proof for the quality of the LEPECVD virtual substrates for the fabrication of advanced electronic devices. This value has to be compared to the best published results obtained from similar structures: from a MODQW using the same spacer thickness of 10 nm, but showing a lower carrier density of $6.9 \cdot 10^{11}$ cm$^{-2}$ compared with $9.9 \cdot 10^{11}$ cm$^{-2}$ in our sample, Schäffler et al. [47] obtained a mobility of 173'000 cm$^2$/V·s at 1.5 K. It is thus justified to claim that LEPECVD virtual substrates are of a quality comparable to state-of-the-art material obtained by other techniques, despite the significantly higher growth rate. This results in the important conclusion for the LEPECVD sample discussed above, that surface roughness or any other structural imperfection of the VS cannot account for the distinctly lower mobility in that structure.

In order to more accurately evaluate the transport parameters, the same sample has been measured at a lower temperature of 300 mK. The data are shown in Fig. 3.15 for low magnetic fields and in Fig. 3.16 for high fields, respectively. The mobility was found to decrease slightly to 155'000 cm$^2$/V·s, while the sheet carrier density increased to $n_s = 1.07 \cdot 10^{12}$ cm$^{-2}$. Also here significant parallel conductance is found, as indicated by $\rho_{xx}$ not vanishing during the Hall plateaus. A fit of the SdH oscillation amplitude to equation (3) from [48] at low fields yields a single-particle lifetime of $\tau_s = 1.1$ ps, while
Figure 3.14: 1.7 K magnetoresistivity and Hall resistance of the combined LEPECVD+MBE sample (#5881/#C2712). The derived values for the sheet carrier density $n_s$ and the mobility $\mu$ are indicated.

The transport scattering time is found to be $\tau_t = 17$ ps, resulting in a Dingle ratio of $\tau_t/\tau_s = 14$. This has to be compared to values of $\tau_t/\tau_s \geq 20$ in the best SiGe MODQW's reported so far [48, 46], and indicates the almost complete absence of large-angle scattering which could be caused by interface roughness or ionized impurity scattering.

### 3.3.2 n-Type modulation doped field effect transistor (n-MODFET)

While the SiGe n-MODQW is well suited as a test structure for the ultimate assessment of the device-grade quality of the material, it also forms the underlying structure for the n-type modulation doped field effect transistor (n-MODFET), which has already demonstrated its outstanding potential for high-frequency applications [49, 50].

For a transistor, instead of simply optimizing the carrier mobility, high transconductance and drain currents have to be achieved. Good transistor properties normally require a higher sheet carrier density in order to lower the sheet resistance, which can be achieved by using two supply layers on either side of the strained Si channel, employing higher doping concentrations and reducing the thickness of the spacer layers.
3.3. Electronic devices

Figure 3.15: Low-field magnetoresistivity and Hall resistance of the combined LEPECVD+MBE sample (#5881/#C2712) at 300 mK. SdH oscillations can be observed even down to 0.4 T. From the spacing of the oscillations against \( 1/B \) (see inset), \( n_s = 1.07 \times 10^{12} \text{ cm}^{-2} \) and \( \mu = 155'000 \text{ cm}^2/\text{Vs} \) are derived. Spin splitting is already visible below 1.2 T, and SdH oscillations can be observed for Landau levels up to almost \( \nu = 100 \).

Figure 3.16: High-field magnetoresistivity and Hall resistance of the combined LEPECVD+MBE sample (#5881/#C2712) at 300 mK. As can be seen from \( \rho_{xx} \) not vanishing during the Hall plateaus, significant parallel conductance is taking place, which also leads to a lowering of the observed \( \rho_{xy} \) from the theoretical values of \( R_K/\nu \) (\( R_K = \frac{\hbar}{e^2} = 25812.807572 \Omega \)).
Experimental

We have fabricated n-MODFET's in the same way as the mixed-technology n-MODQW described above, by growing a SiGe VS with LEPECVD on a high-resistivity 4-inch Si(001) substrate. Then the wafer has been shipped to the DaimlerChrysler laboratory, where the MODFET layer stack was deposited by MBE. A reference sample has been grown completely by MBE. After deposition of the layer stacks the samples were identically prepared using standard processes. Mesas have been dry chemically etched by reactive ion etching (RIE), then the field oxide was deposited by low-pressure CVD at 350°C. The mesas were opened by wet chemical etching using HF. For the source and drain contacts, a phosphorous implant of $2 \times 10^{15}$ cm$^{-2}$ was performed at an energy of 20 keV, followed by a rapid thermal annealing (RTA) step for dopant activation at 650°C. Pt Schottky gates have been formed using e-beam lithography; a thick Au top resulting in a T-shaped gate was then applied to lower the gate resistance, which is crucial for the high-frequency performance. Contact pads were formed by lift-off metallization. The maximum temperature reached during the complete process sequence was 650°C in order to prevent relaxation of the metastable Si channel and interdiffusion at heterointerfaces and dopant diffusion.

TEM micrographs of the layer structure are shown in Fig. 3.17. The left side is an overview of the complete epitaxial film, showing basically the LEPECVD VS with a thickness of 7.5 μm. The right hand side shows the topmost part in high resolution, consisting of the MBE-grown active layer stack and revealing the 10 nm thick Si channel.

Results

We limit ourselves here to a summary of the electrical properties of the LEPECVD/MBE MODFET and a general comparison with the MBE reference sample. Resistance, mobility and carrier concentration have been determined by Hall measurement at 300 K (77 K), resulting in $R_s = 1080$ (454) Ω/□, $\mu_H = 760$ (2037) cm$^2$/Vs and $n_s = 7.6 \times 10^{12}$ (6.8 $\times 10^{12}$) cm$^{-2}$.

For the DC performance assessment, more than 100 randomly selected transistors have been analyzed. The majority of the test devices was found to be working and showed very high performance with only slight variations. Good Schottky behavior was found for the gates with small gate leakage currents of < 5 μA/mm at a gate voltage $V_g = -1.5$ V. Output characteristics showed excellent pinch-off behavior and a drain saturation current of $I_{max} = 230$ mA/mm at a drain voltage of $V_d = 1.5$ V and $V_g = 0.5$ V. The high $n_s$ results in a maximum transconductance of $g_m = 230$ mS/mm at $V_g = -0.3$ V and $V_d = 1$ V. The threshold voltage $V_{th} = -0.8$ V indicates operation in depletion mode.
Figure 3.17: TEM micrographs of the SiGe n-MODFET layer structure. The left image is an overview of the structure, showing basically the 7.5 μm thick LEPECVD VS. Only on the very top does the MBE layer stack appear, shown in higher magnification on the right side, revealing the 10 nm thick Si channel.
Figure 3.18: Direct comparison of the SiGe n-MODFET sample fabricated on the LEPECVD virtual substrate with the pure-MBE reference sample.

These data have been obtained from 0.48 µm Π-gate devices at room temperature.

RF measurements performed at the CNRS Orsay, France, have confirmed the excellent high-frequency behavior, in spite of known design issues which still have to be addressed, like too high contact resistances. Recent advances in this point are expected to lead to a further distinct performance improvement. The devices considered contained mushroom gates with a base length of \( l_g = 100 \text{ nm} \), a top length (of the head) of \( \approx 400 \text{ nm} \) and a width of \( w_g = 30 \text{ µm} \). Correcting the data for parasitics arising from the design flaws mentioned, a transit frequency \( f_T = 61 \text{ GHz} \) and maximum oscillation frequency \( f_{\text{max}} = 107 \text{ GHz} \) are obtained, which are indeed already very promising numbers for Si-based FET's.

The comparison of the LEPECVD/MBE with the pure-MBE device is presented in Fig. 3.18. The figures of merit we examined were the total growth time (without transfers and preparation), the degree of relaxation of the virtual substrate as determined from X-ray diffraction (important for long-term stability of the devices), sheet resistance \( R_s \) of the conducting channel, maximum drain current \( I_{\text{max}} \) and maximum transconductance \( g_m \). As can easily be seen, the mixed-technology sample exceeds the MBE reference in all figures by 10-20%, despite of the total growth time being shorter by a factor of 2.5 (note the logarithmic scale!). In view of applications, it must be stressed that the (solid source) MBE is capable of growing less than 10 virtual substrates before the sources have to be replenished.
3.3.3 p-Type metal oxide field effect transistor (p-MOSFET)

The previous sections have shown promising results obtained from the combination of LEPECVD with MBE for modulation doped structures, where LEPECVD provides the VS part. However, the results obtained from the n-MODQW where the active layer stack has been fabricated by LEPECVD raise questions concerning the device-grade quality of modulation doped strained heterostructures deposited by this technique alone. In order to examine the behavior of undoped layer sequences, SiGe p-MOSFET’s using high-Ge-content channels have been used.

Layer sequence and deposition

Relying on a strained conducting channel with a high Ge concentration between 80% and 100% (Fig. 3.19), this device is ideally suited to make use of the advantages of LEPECVD. The high Ge concentration is favorable for making use of the high intrinsic hole mobility of Ge. As a consequence, the final Ge concentration $x_f$ of the virtual substrate should lie between 50% and 70% in order for the channel to stay fully strained and flat. The growth parameters for the strained channel have to be chosen carefully to avoid a roughening of the upper heterointerface to the Si cap. The quality of this interface is crucial for the performance gain over the Si p-MOSFET, for it is along this boundary that the free carriers in the channel move on their way from source to drain. In a standard Si device, on the other hand, the current flows along the Si-oxide interface with its higher density of interface states. The superior quality of the (Si)Ge/Si interface is the second important reason for the higher hole mobility observed in the SiGe p-MOSFET.

Apart from separating the carriers from the oxide interface, the Si cap also serves to improve the quality of the gate oxide: in contrast to standard Si devices, high-temperature thermal oxidation cannot be used for the formation of the latter due to the limitations imposed by the strained heterostructures on the total thermal budget. Hence the oxide has to be formed by means of deposition, normally using plasma enhanced CVD (PECVD). The quality of deposited oxides on pure silicon is somewhat better than for SiGe; in this way the Si cap serves to lower the interface state density at the oxide interface. In addition to the enhancements of the electronic properties, the Si cap also serves to compensate the strain of the high-Ge-content channel, thus improving the thermal stability of the device. In our case, the thickness of the Si cap was chosen to be 5 nm; about 2 nm are sacrificed in cleaning steps during the device processing, leaving nominally 2-3 nm of pure Si.

The virtual substrate was grown in the same way as for the n-MODQW and
Figure 3.19: Schematic of a SiGe p-MOSFET based on a high-Ge-content channel on a VS with an intermediate Ge concentration $x_f = 50 - 70\%$.

n-MODFET samples, but to higher final Ge concentrations, between 50% and 70%. The structural quality has been assessed with HR-XRD reciprocal space mapping (RSM) and TEM. A RSM of a p-MOS structure based on a channel with 90% Ge concentration on a virtual substrate with $x_f = 60\%$ is presented in Fig. 3.20. The diffracted intensity around two Bragg reflections is shown using iso-intensity contour lines. The regions of diffracted intensity can be attributed to the different parts of the sample as indicated, where the inclination of the region from the virtual substrate in the asymmetric measurement indicates the full relaxation (cf. appendix B). The thin channel, on the other hand, results in a diffracted intensity distribution lying vertically below the constant Si$_{0.4}$Ge$_{0.6}$ layer, which means it is fully strained to the lattice constant of the virtual substrate. A TEM micrograph of the same structure is shown in Fig. 3.21.

Device processing and characterization

As for the n-MODFET’s, device processing and characterization has been carried out at DaimlerChrysler. Device fabrication consisted of standard processing steps similar to the n-MODFET. After dry etching of adjustment marks, P was implanted around the active transistor region serving as channel stopper, followed by dopant activation. A 200 nm thick field oxide has then been deposited by PECVD and subsequently patterned by photolithography. The nominally 10 nm thick gate oxide has then been deposited by PECVD, followed by a curing step in order to lower the interface state density at the Si-cap/Si-oxide interface. Ohmic source and drain contacts have then been formed by B implantation, followed by activation annealing. The next step consisted in a large area deposition of a 300 nm thick Al gate layer, followed by another curing step. The Al gates have then been wet chemically patterned with overlap to source and drain in order to reduce source and drain resistances. Finally,
3.3. Electronic devices

Figure 3.20: HR-XRD RSM around two Bragg reflections of a complete high-speed pMOS layer sequence. The areas of the strained channel have been measured with reduced resolution and extended exposure time to compensate for the low intensity resulting from the small layer thickness.

Ohmic Ti/Pt/Au contacts for source and drain have been formed by standard lift-off metallization.

Transistors have been fabricated from two different samples: a 50% VS with an 80% channel (#5888) and a 60% VS with a 90% channel (#5889). They will be compared to sample #5660 from [51], which, despite its record mobility value, has been shown to exhibit strain-induced roughening at the upper channel interface. In contrast to this older sample, #5888 and #5889 have been grown using optimized parameters for the channel, which could be proven to lead to a perfectly flat upper interface (cf. Fig. 3.21).

On processed samples from all three wafers capacitance-voltage (CV) measurements were carried out from which oxide and Si cap layer thicknesses could be determined. Taking into account the respective drain currents, the modified split CV technique [52] yielded the carrier density and mobility in the channel. The Si cap layer was between 3 and 4 nm thick in all cases. The oxide thickness was determined to be 12.5 nm (#5660), 9.5 nm (#5888) and 5.5 nm (#5889). The undesired small oxide thickness in the latter case resulted from unidentified problems arising during the PECVD oxide deposition process. In Fig. 3.22 the mobility is plotted against the gate voltage $V_G$ and the sheet carrier density, respectively.

From Fig. 3.22 the maximum mobilities are found to be
Figure 3.21: TEM micrograph of the same p-MOS structure. The inset shows the topmost part with the strained channel in high resolution. The channel interface is sharp and well defined, and the channel itself is completely flat without any surface undulations.
3.3. Electronic devices

Figure 3.22: Effective mobilities as a function of the gate voltage (left) and as a function of the sheet carrier density (right).

They are hence higher by a factor of 2.5 to 3.5 than the ones of comparable Si-p-MOSFET’s. On the other hand it is evident that the mobility does not scale directly with the Ge content of the channel. It is influenced rather significantly by the oxide thickness, i.e., by the device processing. According to Fig. 3.22 the mobility maximum is reached at a higher carrier density for lower oxide thickness. At equal gate voltages the samples with thinner gate oxides are therefore characterized by a lower sheet resistance (Fig. 3.23).

The electrical DC properties were evaluated with a semiautomatic probe station. The gate width of all transistors was equal to 50 μm. The nominal gate lengths were 50, 10, 5 and 2 μm. For shorter gate lengths the photolithographic patterning used here did not allow for a defined overlap between the gate metal and the implanted contacts. The large gate lengths as well as the high substrate doping did not allow any high-frequency measurements. Fig. 3.24 shows the output characteristics and resulting transconductances of comparable transistors fabricated from the 3 wafers.

According to Fig. 3.24 the saturation current and the transconductance both scale with the sheet resistances displayed in Fig. 3.22. The saturation currents, obtained at a gate bias of $V_g = -5$ V and drain bias of $V_d = -3$ V, are:

- #5660 (50%/80%): 10.5 mA
- #5888 (50%/80%): 16.0 mA
- #5889 (60%/90%): 20.5 mA
Upon scaling with the gate width of 50 \( \mu \)m we obtain the following current densities and corresponding transconductances:

<table>
<thead>
<tr>
<th>sample</th>
<th>current density</th>
<th>transconductance</th>
</tr>
</thead>
<tbody>
<tr>
<td>#5660 (50%/80%)</td>
<td>210 mA/mm</td>
<td>48 mS/mm</td>
</tr>
<tr>
<td>#5888 (50%/80%)</td>
<td>320 mA/mm</td>
<td>75 mS/mm</td>
</tr>
<tr>
<td>#5889 (60%/90%)</td>
<td>410 mA/mm</td>
<td>118 mS/mm</td>
</tr>
</tbody>
</table>

Both values are very high in view of the large gate lengths and relatively thick gate oxides. They should be compared with those of a standard Si p-MOSFET with 10 nm gate oxide and 2 \( \mu \)m gate length using comparable processing, for which the saturation current amounts to 120 mA/mm and the maximum transconductance 40 mS/mm [53].

The only negative issue is the relatively poor pinch-off behavior of sample \#5889. At a gate bias of \( V_g = 0 \) V (lowest curve on the left hand side of Fig. 3.24) the drain current may be seen to rise significantly above a drain voltage of \( V_d = 1.5 \) V. This indicates an increased leakage current.

Fig. 3.25 shows the dependence of the saturation current and the transconductance on the gate length at \( V_g = V_d = -5 \) V. The scaling with the sheet resistance in the channel is again apparent from this figure. In addition, it is very clear that there exists a huge potential for further device improvement by reducing the gate length.

Another issue of interest for a MOSFET is its sub-threshold behavior. The corresponding measurement range can be seen at low gate voltages \( V_g \) in Fig. 3.26. For all three samples there is a strong increase in \( I_d \) with increasing \( V_d \) for gate voltages \( |V_g| = 0 \ldots 0.5 \) V. Comparable Si-MOSFET’s show closely
3.3. Electronic devices

Figure 3.24: Measured DC output characteristics $I_D(V_D)$ for different gate voltages $V_G$ and deduced transconductance $g_m(V_G)$ for different drain-source voltages $V_{DS}$ for the three p-MOS samples. Gate length was $l_g = 2 \, \mu m$ and gate width $w_g = 50 \, \mu m$ for all transistors.
Figure 3.25: Saturation current (left) and maximum transconductance (right) as a function of the gate length for $V_g = V_d = -5$ V. For comparison the values for pure Si p-MOSFET’s are shown for a gate length of 2 μm.

As spaced horizontal curves in this range with drain currents around $I_d = 1 \ldots 5 \cdot 10^{-8}$ A and a strong $V_d$-dependence can only be observed for very small gate lengths (short-channel effect). The large drain leakage currents observed here are a trade-off to the high saturation currents and could be drastically reduced by reducing the oxide thickness, as then the control efficiency of the gate is enhanced. A common measure for the turn-off behavior is the minimum drain current $I_{d,min}$ at $V_g = 0$ V and $V_d = 0.1$ V (the intersection of the lowest curve with the y-axis in Fig. 3.26). It characterizes the static power loss of the transistors and influences the storage behavior of DRAM cells. These values are shown on the left side of Fig. 3.27 as function of the gate length.

The next important quantity is the threshold voltage $V_t$, shown on the right side of Fig. 3.27. $V_t$ is normally defined as the gate voltage resulting in a drain current $I_d = 1 \cdot 10^{-7}$ A/μm (in our case $5 \cdot 10^{-6}$ A) at $V_d = 0.1$ V. The absolute value of $V_t$ is important for the design of integrated circuits and can be adjusted in a wide range with a suitable channel doping. In our undoped case, $|V_t| < 1$ V for all samples (except for very long channels), reflecting the high conductance of the layers. Of some relevance is the homogeneity across the wafer — the data set for the 5 μm transistors of samples #5888 and #5889 in the $V_t$ plot of Fig. 3.27 shows a mapping over the wafers and shows in both cases a good homogeneity below 0.1 V (#5888) and 0.15 V (#5889).

The last figure we will discuss is the sub-threshold transconductance or gate swing, defined as $\frac{dI_d}{dV_g}$ for $V_d = 0.1$ V in the linear range below $V_t$. It reflects the turn-off behavior of the transistor and should be as small as possible. The theoretical minimum is around 60 mV/decade, good MOS transistors reach
3.3. Electronic devices

Figure 3.26: Sub-threshold behavior of the drain current $I_d(V_g)$ for different drain voltages $V_d$.

Figure 3.27: Minimum drain currents $I_{d,min}$ (left) and threshold voltages $V_t$ (right) of the SiGe p-MOSFETS.
values around 80 mV/decade. For our 5 µm transistors we measured 166, 100, and 220 mV/decade for the samples #5660, #5888 and #5889, respectively, while for the Si reference it was 120 mV/decade. The values are satisfactory or even good (#5888), but increase significantly when determined for higher $V_d$.

### 3.3.4 Conclusions

The feasibility of using LEPECVD for fabricating virtual substrates for future SiGe device applications has been proven both for stand-alone applications, where complete device layer sequences are deposited by LEPECVD, and for combinations with established epitaxy techniques like MBE.

The evidence for 2D transport and mobility enhancement in the LEPECVD n-MODQW indicates that modulation doping is actually possible with this process, although further research will be needed in order to improve the resulting electronic quality.

The devices employing modulation doped structures grown by MBE on LEPECVD VS’s serve as an ultimate prove for the outstanding structural quality of these substrates for strained-layer SiGe applications. In the n-MODQW, a mobility of $159'000 \text{ cm}^2/\text{Vs}$ has been found at 1.7 K and $n_s = 9.9 \times 10^{11} \text{ cm}^{-2}$. The n-MODFET showed a maximum transconductance of $g_{m} = 230 \text{ mS/mm}$, maximum saturation current of $I_{max} = 230 \text{ mA/mm}$, transit frequency of $f_T = 61 \text{ GHz}$, and maximum oscillation frequency of $f_{max} = 107 \text{ GHz}$ after correcting for device parasitics at a gate length of $l_g = 100 \text{ nm}$.

We could further demonstrate the successful fabrication of working SiGe p-MOSFET’s for which the complete layer sequence has been deposited using LEPECVD. Compared with standard Si p-MOSFET’s, the electronic properties are significantly improved with respect to mobility, saturation current and transconductance, showing the large potential of strained-layer SiGe p-MOSFET’s fabricated on SiGe VS’s. The non-optimal sub-threshold behavior is a natural drawback of the present device design in combination with the otherwise highly desirable high conductance, and might be significantly improved by reducing the gate oxide thickness.

Due to the large epitaxial thicknesses needed for all of these devices, LEPECVD with its high deposition rate is ideally suited, while the device performance also proves the electronic quality of the strained-layer heterostructures deposited by LEPECVD.
Chapter 4

Magnetron Sputter Epitaxy (MSE)

4.1 Description of the process and the system

While the strengths of the LEPECVD process are lying in the fast, economic deposition of virtual SiGe substrates and the easy fabrication of complete device layer stacks, the experimental system at hand lacked the possibility of detailed in-situ analysis. Although several analytic techniques used to be accessible to this system by transferring the samples in UHV to a neighboring multichamber MBE and analysis system, the complete work described here has been carried out after the LEPECVD chamber had been modified from handling 3-inch substrates to 4-inch. To complement the structural and electronic studies performed on LEPECVD-grown material, detailed UHV scanning tunneling microscopy (UHV-STM) examinations have been undertaken on Si and SiGe samples fabricated by magnetron sputter epitaxy (MSE) in a different system [54, 55].

MSE is a very versatile process, comparable in many aspects to MBE, especially for what concerns the resulting structural material quality, while being somewhat more flexible in operation due to the simple use of the deposition sources. The current limitation of the experimental sputter system consists of a non-negligible background metal contamination, which has been shown to limit low-temperature electron mobilities in n-MODQW’s to below 20000 cm²/Vs, both in structures grown completely by MSE [55] and in combining MSE with LEPECVD [28]. Nevertheless, state-of-the-art structural quality had been evidenced with TEM and X-ray diffraction; in [55] even photoluminescence from MSE films could be demonstrated. During this work, great efforts have been
put into eliminating possible contamination sources, with only unsatisfactory results. As it turned out, only a major modification of the deposition system, using a different design of the sputter sources would fully eliminate this problem. As this was beyond the scope of this work, we will only report on further structural investigations performed with this system.

The MSE system was equipped with 3 2-inch magnetron sputter sources operated at RF (13.6 MHz) with powers up to 100 W (for Ge) and 200 W (for Si). The source materials used were intrinsic Si, P-doped n-Si, and intrinsic Ge. The growth rates reached at maximum power were 2.8 Å/s for Ge and 1.6 Å/s for Si. The source shutter system allowed for the concurrent operation of one or two sources, thus allowing for the deposition of arbitrary SiGe alloys. Ultrapure Ar was used as process gas; the background pressure of the growth chamber was in the $10^{-9}$ mbar regime.

A commercial room-temperature Omicron UHV-STM was mounted in a separate chamber with a base pressure below $10^{-10}$ mbar attached to the growth chamber. Samples could be transferred between the chambers in vacuum.

The samples used were low-resistivity Si(001) pieces, 5.5 × 14 mm in size, mounted in sample holders which could be used both during deposition and STM imaging. Sample preparation consisted of a high-temperature oxide desorption and cleaning step at ≈ 1200°C for 1-10 min by means of dc heating, passing a current on the order of 15 A through the sample. Sometimes an additional pre-bake of ≈ 1 h at temperatures between 500 – 700°C was employed.

During growth, the samples were radiation heated from the back side, an additional sample shutter close to the sample surface prevented sample contamination from outgassing system parts during temperature ramps and allowed for well-defined deposition times. Additional details about the process, the system and its development can be found in [54, 55, 56]

4.2 Self-assembled Ge clusters

4.2.1 Semiconductor nanostructures

Semiconductor structures with sizes on a nanometer scale have attracted much interest in recent years. The motivations for research into these kinds of new materials and structures are as broad as their possible applications in the future, either by exploiting their intrinsic quantum behavior directly ("qubit", single electron transistor), or by providing new properties for well-known materials (e.g. optical devices in the near-IR for communication applications based on Si). While there are still many technological obstacles to be overcome as far as the actual fabrication of such small structures by means of lithography is
concerned, the principle of self-assembling provides a very efficient and elegant way to obtain them. One of the most promising mechanisms for obtaining self-assembled nano-structures is the Stranski-Krastanow growth mode observed in lattice-mismatched systems like SiGe/Si, resulting first in a 2-dimensional flat wetting layer followed by the formation of 3-dimensional islands. In the SiGe/Si(001) system, these islands are identified to exhibit either \{105\} side facets (dubbed “hut clusters” [57]), or, as their size increases, \{113\} facets (usually called “domes” due to their rather round shape [58]), normally mixed with different facets of higher index. For any technological application, these clusters have to be embedded in a matrix material while preserving their shape as fully as possible. As a consequence, amongst other key issues like size uniformity or regular spatial arrangement, it is of great interest to understand the processes in the initial stages of overgrowth of those clusters. It has been shown by several analytical methods (e.g. RHEED/TEM [59, 60] or LEEM [61]) that Ge or SiGe islands can change their size and shape depending on their initial size as well as on the conditions during Si overgrowth, in the extreme case leading to their complete dissolution in a two-dimensional SiGe alloy layer. As an additional technique, we use scanning tunneling microscopy (STM) to study these processes both on the scale of a single quantum dot and on larger areas, providing some statistical information on the shape evolution during the initial stages of overgrowth.

4.2.2 Sample preparation

The 5 x 14 mm Si(001) (n+ (As) doped) samples were cleaned in UHV by the procedure described above. Before growing the Ge layers, a 100 nm thick Si buffer was deposited at 450°C to ensure a clean Si surface. The Ge layer was grown at 525°C to a thickness of 6.3 ML at a growth rate of 0.45 ML/s, resulting in the formation of both hut clusters and domes, at a density suitable both for imaging single islands as well as for performing statistical analysis on a larger scale. The Ge islands were then overgrown with Si at a substrate temperature of 450°C and thicknesses (in different experiments) of 3.2 ML, 4.4 ML, 5.6 ML, and 22.4 ML, at a growth rate of 0.4 ML/s. After growth, the samples were transferred in UHV into the STM for imaging.

4.2.3 Evolution of the surface morphology

The initial surface morphology (before Si overgrowth) exhibited both hut clusters and domes, with a base length of 30-60 nm for the hut clusters, the domes being somewhat larger and distinctly higher. To study the mechanisms prevailing at the initial stages of the overgrowth on the scale of a single dot, we will consider only hut clusters (see Fig. 4.1 a), and a substrate temperature
during Si capping of $450^\circ \text{C}$. 

Figure 4.1: a) Ge hut cluster before Si capping. Z scale is 30x enlarged. b), c) Single hut cluster after the deposition of 3.2 ML Si, and 5.6 ML Si, respectively, at $450^\circ \text{C}$. Z scale is 30x enlarged. d) Larger area after deposition of 22.4 ML Si at $450^\circ \text{C}$, showing overgrown Ge islands apparently rotated by $45^\circ$. Grey scale corresponds to a z range of 5 nm.

In the following we will discuss the results and compare with studies using other techniques. As becomes clear from the STM images shown in Figs. 4.1 b) and c), in the case of hut clusters the apex starts to dissolve and form an (001) top facet at Si coverages as low as 3.2 ML already. On the left and front facet of the hut cluster in Fig. 4.1 b), one can see the growth of additional layers, while the \{105\} orientation of the facets is still preserved. Considering the formation of the flat top facet, it seems natural to assume that the material added to the side facets originates not only from the deposited Si, but also from the island apex. This becomes even more striking when looking at the later stage of the capping process, shown in Fig. 4.1 c) for a Si coverage of 5.6 ML. The top facet
4.2. Self-assembled Ge clusters

has grown considerably, reducing the island height by a factor of 2. While there are still areas where the \{105\} side facets are intact, at the edges they seem to become unstable, forming new facets with their bases aligned along (110) directions. We thus conclude, that upon further overgrowth, Ge from the island apex diffuses onto the side facets where it forms an alloy with the incident Si, leading to a growth of the side facets mainly at their center regions where the amount of elastic relaxation is smaller. As a result, at the edges new facets are formed, eventually leading to an alloyed island which appears to be rotated by 45° (Fig. 4.1 d)). From BEEM investigations, we get evidence that this is indeed the final shape of the buried Ge islands [62].

The diffusion of Ge away from the apex can be explained by a lowering of the effective strain, as Si gets incorporated into the island and lowers its Ge content. Thus the original driving force for the formation of the \{105\} facets decreases, and it becomes energetically more favorable to form a (001) top facet. This transition should happen first at the island apex, where the surface-to-volume ratio is largest, as was confirmed using real-time LEEM in [61], and using RHEED and TEM in [59, 60]. In the latter two studies it is suggested that this mechanism only prevails for slow growth rates during Si overgrowth (few Å/min), whereas for faster growth kinetics the island shape would be preserved. The explanation for this behavior would be a preferential surface diffusion of the incident Si atoms away from the more relaxed island apex, leading to a fast flattening of the growth front and burying of the intact Ge islands, which is assumed to occur on a faster time scale than Ge segregation and intermixing with Si. Our results essentially agree with the observations in these studies as far as the shape change of the islands is concerned. But we get strong evidence that the intermixing of Si and Ge, and thus the flattening of the islands, occurs even at faster growth kinetics, as our growth rates are of the order of Å/s.

Another indication for the incorporation of Si into the island itself is the formation of a nearly perfect 2 × 8 reconstruction on the top (001) facet (Fig. 4.1 c)), which can be explained by a return of the in-plane lattice constant of the elastically relaxed island apex towards the value for Si, combined with Ge segregation to the surface. This partial reversal of the elastic relaxation seems to be driven by the incorporation of Si into the hut cluster itself.

To obtain a more quantitative view, we analyzed larger STM images (400 nm × 400 nm and 1µm × 1µm) and studied the distribution of the aspect ratio (chosen as \(z/x\)) of the islands and its evolution during the Si capping. Those results are shown in Fig. 4.2, where the histograms of the distribution of the aspect ratio are shown for several Si coverages. The plot for the sample without Si capping nicely reveals the bimodal distribution (see [58]) between hut clusters (theoretical value for hut clusters with a quadratic base: \(z/x = 0.1\)) and domes (theoretical value for purely \{113\} faceted islands: \(z/x = 0.24\). The
combination with higher-index facets somewhat lowers this value). After the deposition of 3.2 ML Si, the two peaks are still clearly separated, but both are markedly shifted towards smaller aspect ratios, i.e. flatter island shapes. The different ratio between the number of huts and domes for this sample can be explained with a slower cool-down ramp between Ge growth and Si capping, leaving more time for Ostwald ripening of the island distribution towards a larger dome population (see, e.g., [63]). It seems obvious that the steeper \{113\} facets become unstable much faster than the \{105\} facets, shifting the aspect ratio from that of the former domes towards the one of the capped hut clusters. This must be explained by an alloying of the island leading to a shape change through mass transport away from the apex onto the side facets or into the wetting layer. Heterogeneous deposition of Si around the island alone cannot account for this fast flattening. As the Si capping thickness increases, the bimodal distribution even seems to disappear (Fig. 4.2 for 4.4 and 5.6 ML Si), leaving in the end, only shallow hills with bases aligned along the \langle 100 \rangle \) directions (Fig. 4.1 d)).

Figure 4.2: Histograms of the distribution of the aspect ratio of the islands, for several Si capping thicknesses
4.2.4 Conclusions

The STM measurements presented here show direct observations of the shape changes during the initial stages of the Si capping of Ge quantum dots. The observed processes are well in agreement with studies using other analytical techniques, but raise questions regarding the dominance of heterogeneous Si deposition driven by surface stress gradients, as described in [60]. Nevertheless, the first steps of the flattening of hut clusters provide further evidence for the incorporation of Si into the dot itself, leading to an alloying of the island material and thus lowering its strain. This mechanism leads to a transition of the original Ge hut clusters towards truncated pyramids, accompanied by the formation of a 2 × 8 reconstructed (001) facet. We further have studied the evolution of the distribution of the island aspect ratio upon Si capping, which shows a distinct flattening not only for hut clusters, but especially for the domes. The amount and velocity of this flattening process cannot be accounted for solely with the assumption of surface stress driven heterogeneous Si deposition, but must be explained by a real shape change of the islands themselves.
4.3 Novel step structures in the Si(001) system

For the development of novel Si based devices relying on heterointerfaces, exact knowledge of the microscopic structure (and the mechanisms involved in their formation) of growth interfaces between layers is indispensable. As buried interfaces are extremely difficult to experimentally examine on atomic scales, one often has to resort to the study of surfaces at intermediate stages of epitaxial layer growth. This part of the work was dedicated to the study of the atomic step structure of the surface of virtual SiGe substrates.

4.3.1 Step structure of Si(001)

The surface steps on singular or slightly misoriented clean Si(001) are of monolayer (ML) height. The Si(001) surface exhibits a characteristic (2×1) reconstruction with dimer rows oriented perpendicular to one another on adjacent terraces. The terraces are bounded by two distinct types of steps: $S_A$ steps to which the upper-terrace dimer rows are oriented parallel, and $S_B$ steps to which they are perpendicular. By contrast, steps of double layer height are not stable on these surfaces. Bilayer $D_B$ steps, with dimer rows perpendicular to the step edge, can be stabilized by applying uniaxial stress [64]. $D_B$ steps also become stable on vicinal surfaces for misorientation angles above 2.5° [65]. By contrast, $D_A$ steps have never been observed on clean Si surfaces, because their energy is much too high [66, 67].

4.3.2 Modifications induced by Ge

The behavior is different when Ge or Si$_{1-x}$Ge$_x$ alloys are grown epitaxially on vicinal or uniaxially strained Si surfaces. In both cases the high-energy $D_A$ steps have been found to form [68, 69]. For vicinal surfaces strain relaxation by dimer vacancy lines (VLs) is thought to be responsible for the preference of $D_A$ steps [69]. For Ge-rich alloys on well oriented but uniaxially strained Si substrates the surface stress field favors the domain for which the dimer lines are along the direction of the applied compressive stress, leading to the same result [68].

During our studies of SiGe VS's, a third configuration leading to $D_A$ steps has been discovered, i.e. the local modification of surface strain and misorientation by the cross hatch morphology found on these structures. Ultimate device performance may depend critically on the step structure at the epitaxial interfaces. Exact knowledge of the surface step structure on graded buffer layers may therefore be of practical importance.
4.3.3 Experimental

Owing to the distinctly lower growth rates of MSE compared with LEPECVD and the limitations imposed by the solid sources, we limited ourselves for this study to VS’s with $x_f = 0.3$ and comparably low thickness and only partial relaxation. However, the qualitative aspects of these relatively thin VS’s are by no means different from the fully relaxed, thick LEPECVD counterparts. Furthermore, the lower density of MD’s allows for a detailed study of the effects of a low number or even single dislocations.

A 1000 Å Si buffer, grown at 500°C, separated the substrate from the step graded buffer, which was grown at 485°C. Starting with a Ge mole fraction of $x=0.12$, $x$ was raised in increments of $\delta x=0.01$, up to the final Ge mole fraction of $x_f=0.30$. Typical growth rates were between 1.5 (pure Si) and 2.1 Å/s for Si$_{0.7}$Ge$_{0.3}$. The total thickness of the graded buffer was 500 nm, which, together with the low substrate temperature, results only in a partial relaxation of the misfit strain.

4.3.4 Step structure of SiGe VS’s

The surface of relaxed graded SiGe buffer layers has already been described in section 3.1.1. As will be shown in the following, the local strain associated with the cross-hatch pattern affects the surface step structure decisively.

Fig. 4.3 shows an STM image of the step structure in the region of a surface slip. Due to Ge segregation, the surface is (2×8) reconstructed, the larger period of the reconstruction being formed by lines of dimer vacancies oriented perpendicular to the dimer rows [70]. All dimer vacancy lines (VLs) are aligned perpendicular to the surface slip, the latter being formed exclusively by $D_A$ steps of double layer height. The sole presence of double layer steps follows immediately from the fact that all VLs have the same orientation in Fig. 4.3. It is important to emphasize that STM images taken in many different surface areas show that the occurrence of $D_A$ steps does not require the surface gradient to be large. By contrast, $D_A$ steps are present also in more planar regions, such as the one shown in Fig. 4.4. The inset shows the structure resolved in more detail, and emphasizes that the VLs are aligned across the surface steps.

Let us first discuss the occurrence of $D_A$ steps close to a surface slip, as shown in Fig. 4.3. On counting the number of steps present in the region of the surface slip ($\approx 8 D_A$), we may conclude that the slip must be the signature of a pile-up containing several dislocations, each of them contributing a surface slip equal to one $D_A$ step (cf. section 3.1.1). The (2×8) reconstructed terraces in the region of the step bunch are very narrow ($\approx 50$ Å on average), a situation resembling closely the one of a pseudomorphic Si$_{1-x}$Ge$_x$ alloy grown on a Si(001) substrate misoriented by 3.1°. Thin Si$_{1-x}$Ge$_x$ layers on such vicinal
Figure 4.3: The step structure of a relaxed, graded Si$_{0.70}$Ge$_{0.30}$/Si(001) buffer. The high local misorientation at the surface slip favors $D_A$ steps of double layer height, with the dimer vacancy lines (VLs) perpendicular to the steps.

Figure 4.4: $D_A$ steps form even in planar regions, despite their higher energy per ledge atom. The inset shows, that due to the short-range attractive interaction between single dimer vacancies on adjacent dimer rows, the VLs are aligned across a step of double layer height.
Si(001) surfaces were shown to exhibit $D_A$ steps [69], as a result of the efficient strain relaxation by the $(2 \times 8)$ reconstruction when the dimer VLs are oriented perpendicular to the steps [70].

On flat surfaces, i.e. for larger terraces such as the ones present in Fig. 4.4, the argument no longer holds, and we might expect the step structure to revert to monolayer steps. Yet Fig. 4.4 shows the exclusive presence of $D_A$ steps even in these regions. Similar observations have been made in other quasi-planar regions in the vicinity of a small surface slip, and in the regions farther away from the ridge sidewalls of larger slips, such as the one of Fig. 4.3. Note also that according to the inset of Fig. 4.4 the VLs are aligned across the $D_A$ steps. This indicates that the $(2 \times 8)$ reconstruction influences the step structure decisively even in these quasi-planar regions. The occurrence of the $(2 \times 8)$ reconstruction as such does not, however, explain the observed step structure, since it is also present on biaxially strained alloy surfaces, and these exhibit exclusively monolayer $S_A$ and $S_B$ steps. There must hence be an additional mechanism at work here, which we can identify with anisotropic strain as follows: The misfit dislocations (MDs) release misfit strain locally in the direction perpendicular to the slip. As a result, the misfit stress becomes anisotropic in this region, with the direction of higher compressive stress parallel to the MDs.

Generally, the $(2 \times 8)$ reconstruction releases more misfit strain perpendicular to the VLs than parallel to them [70]. Thus, if anisotropic strain is present, it is favorable to align the VLs perpendicular to the direction of larger compressive strain. We may hence conclude that the anisotropic strain in the vicinity of a surface slip will favor the alignment of the VLs in the direction perpendicular to the slip. This obviously requires adjacent terraces to be bounded by $D_A$ steps and hence explains our observations presented in Fig. 4.4. Our STM studies on buffer layers which are close to the onset of strain relaxation (not shown) indicate that the transition from monolayer steps to $D_A$ steps takes place even when very few MDs are present. This emphasizes the sensitivity of the step structure on local stress anisotropy.

A close inspection of the STM images reveals that the bilayer steps are present not only at the boundary of large terraces. The 2D islands present in the planar regions and marked by the arrows in Fig. 4.5 are all of double layer height as well. Again, this follows from the orientation of the VLs on these islands parallel to those in the adjacent surface regions. By contrast, 2D islands of double layer height never form on unstrained Si(001) and Ge(001) surfaces. Similarly, 2D islands on biaxially strained $Si_{1-x}Ge_x/Si(001)$ layers remain of monolayer height. The presence of the 2D islands of double layer height must hence again be related to the locally anisotropic strain due to the cross-hatch pattern\(^1\), and to the way in which this strain affects the $(2 \times 8)$ reconstruction

\(^1\)The crucial role played by the anisotropy in determining the height of 2D islands could be further corroborated by moving the STM tip along a $(100)$ direction, starting from the
reconstruction, as will be discussed in more detail below.

In order to get a more quantitative measure of the strain anisotropy, this quantity was evaluated from the STM images in the following way.

From STM cross-sections taken in the direction perpendicular to a slip line the surface deformation was obtained as a function of the distance from the slip. These profiles were then fitted to the theoretical expressions describing the surface distortion caused by the strain field around buried misfit dislocations. The number of dislocations giving rise to the slip in question followed directly from the slip height. For strain modeling elastic isotropy was assumed. The displacement field was calculated for a free surface by applying the method of image dislocations [71] to the edge component of dislocations with Burgers vector $\vec{b} = \frac{a}{2} \langle 011 \rangle$, under the additional constraint of zero net force in the direction perpendicular to the surface. For the fits of the calculated surface displacements to the measured STM profiles, the dislocations were allowed to be arbitrarily distributed between the interface and a shallowest depth $L$, with $L$ entering as a fit parameter. A value of $L$ consistent with cross-section transmission electron microscopy of 200 nm was found to give very good fits. Finally, the component $\varepsilon_{xx}$ of the strain tensor in the direction perpendicular to a given slip was obtained from the derivative of the appropriate displace-

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**Figure 4.5:** The islands marked by the arrows are of double layer height, as can be concluded by comparing the orientation of the VLs on the islands and the surface underneath. Fig. 4.3 shows the upper right quarter of this figure in greater detail.
Figure 4.6: When the lateral extension of an island in the direction perpendicular to the VLs underneath, $N$, exceeds a critical value, $N_c$, the second layer starts to form. Despite of the larger area of island 1, $N_c$ is only exceeded for island 2. The black lines represent the VLs, running perpendicular to the slip line indicated on the left hand side.

ments and the misfit stress. Since great care was exercised in order to ensure that any perpendicular slip lines were far from the analyzed region, the strain component parallel to the slip, $\varepsilon_{yy}$, is given directly by the misfit stress. The strain anisotropy is then defined as $\delta = |\varepsilon_{xx} - \varepsilon_{yy}| / |\varepsilon_{xx} + \varepsilon_{yy}|$.

Since the formation of the 2D islands of double layer height is connected with the $(2\times8)$ reconstruction, there must be a critical lateral size beyond which a transition from monolayer height to bilayer height occurs. More precisely, we expect an island’s extension, $N$, in the direction perpendicular to the VLs of the surrounding region to determine whether it is energetically favorable to grow to double layer height, since in this direction the $(2\times8)$ reconstruction will be most effective in relieving the anisotropic misfit strain. In this scenario, cf. Fig. 4.6, islands of monolayer height would nucleate, grow laterally at first and then double in height after reaching a critical size, $N_c$, the latter depending on the local strain anisotropy.

For a statistical analysis of island height vs. island size, more than 60 islands located in five regions of two identical STM samples were examined. The islands could be assigned to three groups, with strain anisotropy of $\delta = (4.0 \pm 0.6) \times 10^{-3}$, $(2.8 \pm 0.4) \times 10^{-3}$ and $(1.6 \pm 0.3) \times 10^{-3}$, respectively. Fig. 4.7 (a) shows the second layer coverage of the islands versus their lateral extension, $N$, in units of VLs. This plot suggests that both the critical lateral size, $N_c$, and the range of $\Delta N$ within which the transition takes place, depend on the local strain anisotropy. The larger the strain anisotropy the smaller $N_c$ and $\Delta N$, giving rise to a curve with a lower onset saturating very quickly. With decreasing
anisotropy saturation to double layer height becomes more and more gradual, until for biaxially strained regions the islands are of monolayer height for all $N$.

In order to describe the data of Fig. 4.7 in terms of a thermodynamic model, the energies of the relevant steps ought to be balanced in the presence of anisotropic strain. These numbers are not available, however, and their $ab$-initio calculation is beyond the scope of this work. On the other hand, the data can equally well be described by a phenomenological kinetic model in which the effect of the strain anisotropy on the island height is cast into an asymmetric Schwoebel barrier [72, 73]. This barrier is assumed to be operative at the bounding step of an island of monolayer height. The probability for an adatom to cross the step in the up-direction and in the down-direction is designated as $P_{up}$ and $P_{down}$, respectively. The ratio $P_{up}/P_{down}$ is assumed to be given by the local strain anisotropy at the position of the island, $\delta$, and by the size of the island area remaining at monolayer height. Considering for simplicity circular islands with radius $r$, the barrier asymmetry is hence taken to be $P_{up}/P_{down} = 1 + \alpha \cdot \delta \cdot (r_{ML} - r_{DL})$. Here, $r_{ML}$ is the outer radius of the island, $r_{DL}$ is the radius of the second layer part, assumed to be circular in shape as well, and $\alpha$ is a constant.

The asymmetric Schwoebel barrier causes the adatom concentration to be higher on top of the monolayer island, leading to the nucleation of a second layer growing rapidly at first, and then slowing down as the entire island approaches double layer height. According to the model, $\delta$ is predicted to be proportional to $1/N_c$. In Fig. 4.7 (b) the fitted values of $1/N_c$ are plotted against the strain anisotropy $\delta$ evaluated experimentally from the STM images in the way described above. The data points do indeed scatter around a straight line through the origin, indicating good agreement between the model and the STM data.

### 4.3.5 Conclusions

In conclusion, we have observed the surface step structure of partially relaxed, graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}(001)$ buffers to reveal $\text{D}_A$ steps and 2D islands of double layer height. $\text{D}_A$ steps are a result of the locally anisotropic misfit strain due to the pile-up of misfit dislocations. Anisotropic strain and the possibility of the $(2\times8)$ Ge reconstruction to release more strain perpendicular to the VLs, lead to 2D islands of double layer height. The nucleation and growth of the second layer are well described by a phenomenological model in which a strain-induced asymmetric Schwoebel barrier is assumed.

There is hence evidence for local modifications of the step structure, induced by the locally anisotropic strain fields from the MD’s, already at relatively low temperatures (485°C). Higher temperatures, as used for the LEPECVD VS’s or
Figure 4.7: (a) The second layer coverage of a 1 ML high island as a function of its lateral extent $N$ in units of VLs for islands found in regions with high ($\bullet$), intermediate ($\triangle$) and low ($\times$) strain anisotropy, determined from the STM images as $\delta = (4.0 \pm 0.6) \times 10^{-3}$, $(2.8 \pm 0.4) \times 10^{-3}$ and $(1.6 \pm 0.3) \times 10^{-3}$, respectively. The solid lines result from a fit to a model assuming an asymmetric Schwoebel barrier due to strain anisotropy. (b) The reciprocal of the critical island size, $1/N_c$, is plotted against the experimentally determined strain anisotropy, $\delta$. 

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in some of the UHV-CVD studies, will lead to even more distinct modifications by means of the enhanced surface diffusion kinetics, which could eventually explain on a microscopic scale the corrugation enhancements observed for the cross hatched surface at higher temperatures.
4.4 X-ray investigations of defective MSE films

In the course of the development of new processes, the search for suitable machine configurations and process parameters leads to a large number of structurally highly imperfect samples. This raises a certain demand for analytic techniques able to yield quantitative information about the degree of structural disorder. An elegant and experimentally relatively simple method for structural investigations is X-ray diffraction, where normally no additional sample preparation is needed. For (hetero-)epitaxy processes, high-resolution X-ray diffraction (HR-XRD) is routinely used to investigate the composition, strain, orientation and overall quality of thin films. Theoretical models for the simulation of rocking curves are well established [45]. However, HR-XRD is not sensitive enough in the case of an extended modified subsurface area, especially if it is smoothly profiled and highly defected. In such structures also the well-known problem of the non-unique solutions [74], caused by the loss of phase information in diffraction measurements, becomes very pronounced. In triple-crystal diffractometry [75] (TCD), where the detailed structure of the angular distribution of the diffracted beam is studied by means of an additional analyzer crystal, it is possible to separate the elastic component of the scattered intensity from the diffuse one and, thus, to considerably improve the signal-to-noise ratio in diffraction intensity measurements as well as to study diffuse scattering due to defects of the crystal lattice [76].

The X-ray standing wave (XSW) technique [77] based on the measurement of the yield of the secondary radiation (fluorescent quanta, photo- and Auger-electrons) in dynamical Bragg diffraction conditions is a well-established method for studying the structure of surfaces and shallow interfaces (see reviews in Refs. [78, 79, 80] and references therein).

Interference of the refracted and diffracted waves, which are of the same order of magnitude near the exact Bragg angle, leads to the formation of a standing wave field with the same periodicity as the diffracting planes in the substrate. The intensity of the secondary radiation emitted from the structurally modified area directly reflects the phase of the XSW. Fluorescent radiation, usually used in the case of impurity atoms adsorbed on the surface or situated in thin layers, is of little use for thick films and homoepitaxial structures, because of the big escape depth of fluorescent quanta. Due to their small escape depth (0.01-0.5 μm) X-ray photoelectrons can be effectively used for the XSW-phase study in such structures and help in selecting the most appropriate strain and disorder profiles among a set which results in similar fits of the diffraction curves.

This approach was applied to the characterization of ion-implanted layers [81, 82], superlattices [83] and ultrathin quantum wells [84]. In this work we used the high sensitivity of the photoelectron yield to study lattice disordering.
in the subsurface area of films grown by MSE under non-optimal conditions.

The reciprocal space mapping [15] (RSM) is a powerful tool for evaluating the strain state of thin layers. Due to the much more limited vertical divergence and the very small horizontal divergence of the RSM setting, it is possible to get a "δ-function like" reciprocal-space probe which is almost invariant over the Ewald sphere. We show that the detailed information provided by the TCD measurements could be proved by XSW- and RSM-measurements. The combination of the different methods leads to more accurate results than a simple rocking curve simulation.

4.4.1 Measurement set-ups

The homoepitaxial Si film under investigation here has been grown by MSE, at a substrate temperature of 570°C, on a p-(B)-doped 3-inch (001) Si substrate. Sample preparation consisted of a standard RCA clean, followed by outgassing the wafer for 1 h at 600°C, and oxide desorption at 840°C under a very low Si flux. The original purpose of the film growth was to measure the background contamination level in the UHV sputter system, it has been grown under conditions which were known to lead to a certain degradation in film quality (especially, a low Ar flux was chosen, leading to a significant amount of high-energy ions bombarding the sample surface). This resulted in a sample well suited for the investigation of the influence of lattice disorder on the different X-ray techniques used in this study.

The intended nominal thickness of the epitaxial layer was 1 µm. The HR-XRD-, TCD- and XSW-measurements were performed in a triple-axis diffractometer. A Rigaku RU-200 rotating anode generator was used as a source of CuKα radiation. The incident beam was conditioned by a channel-cut (004) Si monochromator. In the TCD-arrangement with parallel (+−+) setting, a third crystal (perfect Si(004)) was used as analyzer. In each angular position of the specimen Δθ, where Δθ is the deviation from the exact Bragg angle θB, the analyzer performed a scan near the position δθan = 2Δθ, where the diffraction peak is situated.

The XSW measurements were carried out in a double crystal (−−) set-up in the dynamical domain −20 ≤ Δθ ≤ 20 arc sec. The specimen was mounted inside a gas-flow proportional counter supplied with transparent mylar windows for the incident and diffracted beams [85]. A gold-plated tungsten wire 20 µm in diameter was used as an electrode for recording the photoelectron emission. A gas mixture (90% He₂ + 10% CH₄) flowing through the counter provided nearly 100% effectiveness of photoelectron detection. The energy resolution of the counter was about 18% (at 8 keV). The low energy band (2.5 < E < 3.5 keV) containing mainly high-energy-loss Si K photoelectrons was used in the experiment. Why this kind of photoelectrons were chosen is
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Figure 4.8: CuKα (004) experimental HR-XRD curve from the MSE sample #546 consisting of a partly disordered homoepitaxial Si film.

clarified below.

X-ray reciprocal space mapping (RSM) measurements were performed using a Philips MPD 1880 high resolution diffractometer with a Ge(220) monochromator in the (+-++) mode. The diffraction space maps were obtained by an additional channel-cut Ge (220) analyzing crystal between sample and detector. The illuminated area on the sample was about 1 mm x 0.1 mm.

4.4.2 Results and discussion

The experimental HR-XRD curve measured for the symmetric (004) Bragg reflection is shown in Fig. 4.8. The curve displays a smooth behavior with a weak asymmetry of the tails at angles ranging from -150 to +300 arc sec. However, fitting dynamical theory to this curve did not lead to a satisfactory result.

The RSM data is shown in Fig. 4.9. The plot shows iso-intensity contour lines in the reciprocal space around the Si (004) peak. There is a slight asymmetry in the intensity distribution, towards positive q∥ values, which can be explained with diffuse scattering from crystal defects. A reciprocal space map around the (224) Bragg peak has also been measured, confirming that the asymmetry seen both in the (004) RSM and the HR-XRD measurement does not originate from strain effects.

To evaluate the contribution of diffuse scattering caused by defects and dis-
order in the epitaxial film, a few complete TCD spectra, obtained by scanning a wider range of angles $\Delta \theta_{an}$, were measured. Fig. 4.10 depicts two such TCD spectra measured at two different positions of the specimen $\Delta \theta = \pm 45$ arc sec, symmetrical relative to the exact Bragg position. Each spectrum consists of three peaks [75]. The so-called “main” peak (MP) characterizes the tail of the rocking curve of the crystal under investigation and is formed by X-rays incident on the first crystal (the monochromator) at an angle $\theta_B$, and reflected by the specimen beyond the reflection maximum. X-rays incident on the first crystal at an angle $\theta_B - \Delta \theta$ are reflected by the specimen in the reflection maximum and form the so-called “pseudo” peak (PP), which depends on the tail originating from the monochromator crystal and is of no interest in our case. For the symmetrical Bragg diffraction the main and pseudo-peak are located at angular positions of the third crystal (the analyzer) $\Delta \theta_{an} = 2 \Delta \theta$ and $\Delta \theta_{an} = \Delta \theta$, respectively. The location and shape of the diffuse peak (DP) are completely determined by crystal defects. It can be seen that the intensity of the DP is quite large, and bigger for negative angles than for positive ones. This fact explains the asymmetry of the HR-XRD curve.

In each angular position of the specimen, after background subtraction, the intensity has been integrated over the MP, giving the total intensity of “pure” diffraction scattering. Results of the TCD measurements of MP intensity are collected in Fig. 4.11, as well as a part of the HR-XRD curve, for comparison. The diffracted intensity decreases rapidly, and for angles $|\Delta \theta| > 100$ arc sec it practically drops to zero. Such a behavior of the elastic scattering component indicates the presence of a thick, strongly disordered subsurface layer [82]. It is obvious that only diffuse scattering forms the tails of the HR-XRD curve at higher angles and, actually, there is no asymmetry in the angular dependence of the intensity of the elastic component of scattering, in spite of oscillations. From the period of the oscillations the total epilayer thickness of about 1.1 $\mu$m can be derived, in accordance with the nominal thickness of 1 $\mu$m. The
Figure 4.10: TCD spectra for $\Delta \theta = +45$ arc sec (solid line) and $\Delta \theta = -45$ arc sec (dashed line). MP: main peak; PP: pseudo peak; DP: diffuse peak.
TCD data simulations were carried out in the domain of the kinematical approximation, where the scattering amplitude is small. The layer thickness, the static Debye-Waller factor \( \exp(-W) \) and the lattice spacing modification \( \Delta d/d \) entered as fit parameters. A least-square fit was performed for the difference \( \chi \) between the experimental and the calculated rocking curves, starting from different initial sets of parameters. The simulated curve resulting from one parameter set is presented in Fig. 4.11 (solid line). The corresponding strain and damage profiles are shown in Fig. 4.12 (solid line) as solution A. The epitaxial layer appears to be strongly defective, with disorder increasing towards the surface. A big value of \( \Delta d/d \) in the range of 0.2 \( \mu m \) has not a real physical meaning, because of the static Debye-Waller factor there being practically zero. Deeper in the layer, the modification of the spacing is very small (\( |\Delta d/d| < 10^{-5} \)). There are several equivalent strain and damage profiles resulting in \( \chi^2 \) values rather close to each other. To illustrate this, the simulated curve and corresponding set of profiles of an alternative solution B, which provided practically the same \( \chi^2 \) value as solution A, are presented in Figs. 4.11 and 4.12 (dashed line).
4.4. X-ray investigations of defective MSE films

Figure 4.12: Two equivalent sets of depth profiles of the static Debye-Waller factor (upper curves) and lattice spacing modification (lower curves) of the sample. Profiles A (solid line) and B (dashed line) are results of equivalent simulations A and B of Fig. 4.11, respectively.

Despite of the similar behavior of the simulated curves (Fig. 4.11), the differences between solutions A and B are essential. Model B suggests a good crystalline quality surface area and shifts the strongly disordered region deeper into the film. It is obvious, that the problem of uncertainty of found solutions strongly depends on the experimental accuracy and the presence of a well-defined initial model. It is important to examine the obtained solutions independently. In our study we used the XSW technique as such an additional tool. All equivalent strain and damage profiles found were then tested in the dynamical domain by comparing the calculated and experimental photoelectron yield curves to obtain the most realistic one. It should be noted that in this homoepitaxial layer, the use of the XSW method to obtain information about the phase of the diffracted wave near the crystal surface or, in other words, about the total surface displacement with respect to the substrate, may not be enough. The total displacement of atomic planes underneath the 0.2 μm nearly amorphous area (where it is not defined) is too small to create a phase shift detectable by the XSW technique. Nevertheless, if the escape depth of photoelectrons is comparable with the thickness of the tested area, the high sensitivity of XSW yield to lattice disordering [79] can be effectively used. As is well known, low-energy-loss electrons escape from the shallow depths close to the surface, whereas those that have lost a significant part of their energy in
Figure 4.13: Experimental (004) curve of the yield of high-energy-loss SiK photoelectrons (dots). The solid- and dashed-line graphs were calculated assuming profiles A and B of Fig. 4.12, respectively.

Figure 4.13: Experimental (004) curve of the yield of high-energy-loss SiK photoelectrons (dots). The solid- and dashed-line graphs were calculated assuming profiles A and B of Fig. 4.12, respectively.

inelastic collisions with the crystal atoms originate mainly in the deeper layers. In our case, the normally used [81] low-energy-loss photoelectrons with mean escape depths less than 0.07 \( \mu \text{m} \) [86] (in silicon) are, of course, sensitive to the strong subsurface disordering but not suitable to test the specific behavior of the obtained damage profile. To probe deeper layers, photoelectrons with high energy losses (with the biggest escape depth) were registered. The probability \( P \) of escape from different depths \( z \) in the silicon crystal for such electrons is well approximated by a linear function \( P(z) = 1 - z/L \), where \( L = 0.68 \mu \text{m} \) [86]. The experimental XSW curve, normalized to the photoyield far from the Bragg angle, is shown in Fig. 4.13 (dots). The solid and dashed lines in Fig. 4.13 are the XSW simulations based on damage and strain profiles A and B, respectively. A good agreement between the experimental XSW curve and the one calculated based on model A permitted us to make an obvious choice and confirmed the increasing crystalline quality in layers deeper than 0.2 \( \mu \text{m} \), as well as the absence of the additional completely amorphous surface layer, which could not be extracted from the X-ray diffraction fit [87]. Small deviations in the tails of the XSW curve can be explained by the fact that in the calculation the diffuse scattering has not been taken into account.
In conclusion we can say that the combination of different X-ray diffraction techniques can be used as a powerful tool to accurately and quantitatively characterize even strongly disordered epitaxial thin films. The accurate TCD measurements allowed to separate the strong diffuse scattering and, thus, to measure precisely the angular dependence of the elastic component of the diffraction scattering. The RSM data confirmed the presence of the strong diffuse scattering asymmetrically distributed around the Si (004) peak. An additional (224) peak RSM (not shown) confirmed the absence of strain effects. The XSW photoelectron yield measurements permitted to select the most appropriate strain and damage profile among those which are practically equivalent from the point of view of the kinematical X-ray diffraction theory. The lattice spacing of the epitaxial film was found to be practically unmodified. The lattice disordering almost linearly increases towards the surface, starting from the substrate/film interface. The topmost 0.2 μm thick surface layer was found to be nearly amorphous. Finally, we show that the detailed information provided by the TCD measurements could be proved by XSW and RSM measurements. The combination of the different methods leads to more accurate results than a conventional HR-XRD measurement alone.
Conclusions and outlook

In this work, we present the current state-of-the-art of LEPECVD and its application to the still emerging field of SiGe heteroepitaxy for microelectronic device applications. We have been able to achieve several important improvements to the process and to open up new areas of application as in the case of microcrystalline Si. By successfully employing LEPECVD in the fabrication of several basic SiGe devices exhibiting properties, which at the very least can be called promising, the relevance of the process for commercial applications could be further corroborated. In particular, SiGe n-MODQW’s exhibiting low-temperature electron mobilities of up to nearly 160’000 cm²/Vs and SiGe n-MODFET’s with a maximum transconductance of $g_m = 230$ mS/mm, fabricated with MBE on LEPECVD-grown virtual SiGe substrates have been demonstrated. SiGe p-MOSFET’s with a maximum transconductance of $g_m = 118$ cm²/Vs and saturation current $I_{max} = 410$ mA/mm have been shown, based on heterostructures fabricated with LEPECVD alone.

By the application of MSE in combination with STM to the SiGe system, important novel insights into microscopic structural aspects of this material could be gained.

The extensive use of different sophisticated X-ray diffraction techniques helped to rather efficiently optimize the structural quality of all the investigated structures by providing the necessary detailed insights with minimum delay time.

With the presentation of this work, we bring LEPECVD to a level of maturity which makes it ready for first implementations in commercial production processes. Nevertheless, the broad field of opportunities opened up by SiGe will make the research topics for LEPECVD even more numerous in the future. Still more questions remain for the application of this process to different material systems than SiGe epitaxy for electronic devices — epitaxy using other semiconductors, amorphous or polycrystalline Si or SiGe for solar cells, nitrides, oxides, ...
Appendix A

Relaxation of virtual SiGe substrates

Strain and elasticity

The growth of a Si$_{1-x}$Ge$_x$ film with a lattice constant $a(x)$ on a Si(001) substrate results in an in-plane misfit strain

$$\varepsilon_{||}(x, r) = \frac{a_{||}(x, r) - a_c(x)}{a_c(x)}$$  \hspace{1cm} (A.1)

where $a_{||}$ denotes the actual in-plane lattice constant, which depends on the degree of relaxation

$$r = \frac{a_{||} - a_{Si}}{a_c - a_{Si}}.$$  \hspace{1cm} (A.2)

Thus, for a film coherent to Si, $a_{||} = a_{Si}$ and $r = 0$. The maximum value for $|\varepsilon_{||}|$ of a film with composition $x$ is the total misfit

$$f = \frac{a_{Si} - a_c(x)}{a_c(x)}$$  \hspace{1cm} (A.3)

($\varepsilon_{||} < 0$ always for SiGe on Si). $a_c(x)$ is the lattice constant of a relaxed (bulk) Si$_{1-x}$Ge$_x$ alloy with cubic unit cell. In a first approximation $a(x)$ follows Vegard’s law: $a(x) \approx a_{Si} + x(a_{Ge} - a_{Si})$. The slight deviations from this proportionality have been taken into account by adding a quadratic term

$$a(x) = a_{Si} + c_1 \cdot (a_{Ge} - a_{Si}) + c_2 \cdot (a_{Ge} - a_{Si})^2$$  \hspace{1cm} (A.4)
with the constants $c_1$ and $c_2$ obtained from a fit to the data presented by Dismukes et al. [88]. Upon applying in-plane strain, the Poisson effect requires the cubic unit cell to become tetragonally distorted by

$$
\varepsilon_{\perp} = \frac{2\nu}{\nu - 1} \cdot \varepsilon_{\parallel}
$$

(A.5)

with Poisson’s number

$$
\nu(x) = \frac{c_{12}(x)}{c_{11}(x) + c_{12}(x)}
$$

(A.6)

depending on the elastic material constants, which have been linearly interpolated between the values for Si and Ge (in GPa):

<table>
<thead>
<tr>
<th></th>
<th>$c_{11}$</th>
<th>$c_{12}$</th>
<th>$c_{44}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>165</td>
<td>63</td>
<td>79.1</td>
</tr>
<tr>
<td>Ge</td>
<td>129</td>
<td>48</td>
<td>67.1</td>
</tr>
</tbody>
</table>

The elastic energy associated with strain in a film of thickness $h$ is

$$
E_e = \frac{2G(1 + \nu)}{1 - \nu} \varepsilon^2 h
$$

(A.7)

where $G$ is the shear modulus.

**Plastic relaxation by misfit dislocations**

**Energetics and equilibrium critical thickness**

This energy can be lowered by introduction of dislocations with an in-plane edge component of the Burgers vector. The energetically favorable type found in diamond lattice systems are $60^\circ$ dislocations with Burgers vector $a/2 \langle 011 \rangle$. The energy associated with a square grid made up of two perpendicular, non-interacting arrays of dislocations can be expressed as [89]

$$
E_d = (f - \varepsilon_{\parallel}) \frac{Gb}{2\pi(1 - \nu)} \left( \ln \frac{h}{b} + 1 \right)
$$

(A.8)

where $b$ is the in-plane component of the Burgers vector. By minimizing the total energy $E_e + E_d$, one obtains the film thickness, at which it becomes energetically favorable for dislocations to form [89]

$$
\frac{h_{MB}}{b} = \frac{1}{8\pi f(1 + \nu)} \left( \ln \frac{h}{b} + 1 \right)
$$

(A.9)
$h_{MB}$ is the Matthews-Blakeslee critical thickness [90, 91], predicting the onset of plastic relaxation in thermal equilibrium. Experiments usually yield significantly higher values for this critical thickness, which can be understood from the fact that the exact structure of the dislocation core (which enters in the form of $E_d$) is not experimentally accessible and one has to resort to theoretical models, and that the kinetics involved in the nucleation of dislocations have not been taken into account. Several authors have developed kinetic models which better fit the experimental data, e.g. Dodson and Tsao [92], Fischer and Zaumseil [93], or Hull, Bean et al. [94]. For a good review of similar models see, e.g., [95].

Nucleation

MDs can be introduced either by heterogeneous nucleation at local stress centers like interface contaminants or surface ripples [96, 97], by dislocation multiplication or by homogeneous nucleation. The latter can be excluded under normal epitaxial growth conditions due to the high energy barrier associated with it (the dislocation self-energy per length is on the order of several eV/b, which does not allow thermal activation). The glide of dislocations preexisting in the substrate is irrelevant in the case of Si substrates due to their level of perfection. Nucleation by the formation of surface ripples (i.e. a two-step relaxation process where plastic relaxation follows an elastic surface deformation that relieves part of the strain) normally is not expected in compositionally graded structures, as the surface strain is kept relatively low at all times.

The relevant nucleation mechanisms for MD’s in SiGe films thus are substrate interface imperfections (which never can be totally eliminated) and multiplication of pre-existing dislocations.
Appendix B

High-resolution X-ray diffraction

In this appendix, we give a brief overview of the X-ray diffraction (XRD) techniques relevant for this work. The general experimental setup for an XRD apparatus is shown in Fig. B.1. For our X-ray investigations we used a Philips MPD 1880 high-resolution diffractometer with CuKa radiation, Gutmann optics, as well as primary and optional secondary Ge(220) Bartels monochromators. The basic equation underlying XRD is the Bragg equation

\[ n\lambda = 2d\sin\theta \]  

linking the spacing of diffracting crystal planes \(d\) to the angle of diffraction \(\theta\), with the relation depending on the wavelength of the (monochromatic) radiation \(\lambda\) and the order of diffraction \(n\). Not all geometrically possible values of \(n\) need lead to non-vanishing diffraction intensity, though — the structure factor of the unit cell of the investigated crystal lattice has to be taken into account, which exhibits extinction effects for certain orders of diffraction. In the case of the Si(001) lattice plane set, e.g., the lowest order of diffraction is 4, making the (004) Bragg reflection peak the most intense one for symmetrical diffraction of a (001) oriented sample.

XRD

In standard XRD, the detector is scanned over a large range of \(2\theta\) values corresponding to a range of lattice plane spacings \(d\), while normally the sample is rotated at half the speed of the detector, resulting in an \(\omega - 2\theta\) scan where always \(\omega = \theta\).
this way can then be attributed to different systems of lattice planes present in the sample, identifying constituent materials, phases and preferred orientations. As this method relies on at least partially random orientations present in a sample\(^1\), it is usually applied to polycrystalline materials. Here, XRD was employed for investigating the crystallinity and preferred orientation of the crystallites in microcrystalline Si films grown by LEPECVD (e.g. Fig. 2.11 on page 27). For this type of measurement, the opening angle of the detector is of no importance, as only the angular locations of the Bragg peaks are of interest, but not their detailed shape. For samples exhibiting a high degree of preference in crystallite orientations, the remaining two rotational axes of the sample can be scanned at fixed \(\theta\) values, resulting in pole figures, showing the hemispherical distribution of orientations for a specific set of lattice planes.

### HR-XRD

In contrast to XRD, where one is interested in the number and angular position of Bragg peaks and possibly their relative intensities, high-resolution XRD (HR-XRD) addresses the detailed shape of single Bragg peaks. This is achieved either by rotating only the sample (\(\omega\)-scan) with high angular resolution, while the detector is placed at the correct 2\(\theta\) position with a reasonable opening angle

\(^1\)Only sets of lattice planes parallel to the sample surface can fulfill the Bragg condition! In the case of a single crystal, most of the lattice plane sets would be excluded due to this restriction.
(typically \(\approx 5^\circ\)), what results in a so-called rocking curve. Another possibility is to again scan the detector through the \(\theta\) range, this time with a very narrow angular opening, at double the speed of the \(\omega\) motion, only considering diffracted radiation fulfilling the Bragg condition at all times, resulting in a \(\omega - 2\theta\) scan (or \(\theta - 2\theta\) for lattice plane sets parallel to the sample surface where \(\omega = \theta\)), which, on the other hand, is nothing else than a high-resolution scan through a range of lattice spacings. This type of measurement is very useful for a fast and precise determination of varying lattice constants in a film. The extremely high angular resolution achievable for the detector, when a secondary Bartels monochromator is placed in front of it (B2 in Fig. B.1), can also be exploited for \(\omega\)-scans (i.e. rocking curves) taken for one single lattice spacing \(d\), reflecting the spread in orientation (e.g. caused by dislocations or other types of defects) for a specific part of a film, if consisting of layers with different lattice constants. When such rocking curves are measured at different values of \(2\theta\), they can be combined to a 2-dimensional map of the reciprocal space around a given Bragg peak — a reciprocal space map or RSM is obtained. A representation of the different types of HR-XRD scans in reciprocal space is shown in Fig. B.2.

The purpose shared by the different HR-XRD techniques is to obtain information about the sub-structure of single Bragg peaks, which is a reciprocal-space representation of the detailed real-space structure of a single crystal. In addition to the purely geometrical information, by employing numerical simulation to the absolute or relative intensities, taking into account the different scattering cross sections for different atoms, also chemical compositions can be determined.

**Interpretation of measurements**

**Rocking curves**

The simplest measurement type is the rocking curve (RC). The opening angle \(\Delta \theta\) of the detector leads to an integration of intensity along the \(2\theta\)-direction, intermixing peak shape broadening along \(q_{\parallel}\) and \(q_{\perp}\). Nevertheless, for many applications this does not matter, e.g. if only features along \(q_{\perp}\) are expected as in the case of a fully strained superlattice, where from the angular peak positions directly the spacings of the different super-periods can be derived (cf. Fig. 3.11 on page 42). On the other hand, if more detailed information is needed as in the case of partial relaxation, different Bragg peaks corresponding to different non-parallel \(\vec{q}\) can be examined, providing independent information about the \(q_{\parallel}\) and \(q_{\perp}\) components.
Appendix B. High-resolution X-ray diffraction

(a) rocking curve (b) $\omega-2\theta$ scan (c) RSM

Figure B.2: Reciprocal space representation of the different HR-XRD scan types employed. $\vec{k}_i$ and $\vec{k}_f$ denote the wave vectors of the incident and diffracted beams, respectively, $\vec{q}$ is the diffraction vector $\vec{k}_f - \vec{k}_i$. For (a), $\vec{q}$ is scanned as a reciprocal space probe with angular opening $\Delta \theta$ (the detector opening angle) in $\omega$-direction. In (b), the orientation of $\vec{q}$ is kept fixed; only its length is varied, corresponding to a scan of a range of lattice spacings. In (c), both the length and orientation of $\vec{q}$ are varied, resulting in a 2-dimensional reciprocal space map. In (b) and (c), a secondary Bartels monochromator is used, giving $\vec{q}$ the shape of a $\delta$-like space probe.

$\omega-2\theta$-scans

Due to the reduced width of the reciprocal space probe employed in an $\omega-2\theta$-scan, the resulting data contains much less ambiguity as it corresponds to a quasi-1-dimensional section through reciprocal space: a measurement contains a direct representation of the distribution of lattice spacings in the lattice plane set considered.

Reciprocal space maps

The most detailed insight into the substructure of a Bragg peak and hence the structure of the sample crystal lattice naturally gives the reciprocal space map (RSM). One single measurement contains information about lattice spacing distortions (connected to compositional variations, strain etc.), crystal perfection (defects) and tilt.

To demonstrate how an RSM can clarify observations, which may be hard to interpret by simply considering rocking curves, Fig. B.3 compares two RC’s with the corresponding RSM obtained from a 40% SiGe VS. RC2 has been measured with the sample rotated by 90° around its surface normal. When looking at the two curves, one easily identifies the (004) Bragg peak of the Si substrate. But the intensity distribution to the left, originating from the
SiGe alloy in the VS and extending towards lower diffraction angles and hence larger lattice constants corresponding to higher Ge content, looks rather different for the two curves. The reason for this behavior is easily seen from the RSM: towards the top of the VS (i.e. higher Ge concentrations), the crystal lattice appears to be increasingly tilted towards negative $q_{\parallel}$ values. During the measurement of RC1, the sample had been oriented in a way which shifted the SiGe layer peak towards higher $\omega$, moving it closer to the Si substrate peak compared with RC2. This demonstrates that for more complicated structures, the interpretation of RC’s can become increasingly difficult, where an RSM measurement reveals much more details at once. The Ge scale shown on the right axis of the RSM plot is calculated directly from the $q_{\perp}$ values, assuming a fully relaxed lattice with a cubic unit cell.

To justify this assumption, the complete relaxation has to be proven. However, in order to determine the degree of relaxation of the complete structure, the symmetric RSM shown in Fig. B.3 is not sufficient, as the (001) set of planes involved in the (004) Bragg reflection contains no information about the in-plane lattice constant. To access this quantity, a second Bragg peak has to be evaluated, e.g. (224). To arrive at an accurate measurement of the strain state, the shift in $q_{\parallel}$ due to the tilt in the upper layers has to be taken into account now. This is achieved by evaluating the tilt from the (004) RSM for each $q_{\perp}$ value, and correct the (224) data by this amount. The resulting two-peak RSM is presented in Fig. B.4.
Figure B.4: Combined RSM obtained around (224) and (004) Bragg peaks from the same 40% VS (#5721). The data has been corrected by the tilt visible in Fig. B.3, so from the (224) plot the degree of relaxation can be determined immediately by comparing the intensity distribution with the inclined dashed line of full relaxation (the connection between the substrate peak and (000), corresponding to cubic unit cells). The vertical dashed line corresponds to layers fully coherent to the Si lattice (i.e. possessing the same in-plane lattice constant and hence resulting in the same $q_\parallel$ values).
Publications and presentations

Publications


19. A. Rastelli, M. Kummer and H. von Känel, Shape evolution of Ge domes on Si(001) during Si capping, Physica E, in press


Presentations

1. STM Study of Si$_{1-x}$Ge$_x$ buffer layers grown by Magnetron Sputter Epitaxy, Annual Meeting of the Swiss Physical Society, Bern, Switzerland, February 27, 1998 (talk)

2. STM Study of Step Graded Si$_{1-x}$Ge$_x$/Si(001) Buffers, Spring Meeting of the European Materials Research Society, Strasbourg, France, June 16-19, 1998 (poster)
3. Characterization of Si$_{1-x}$Ge$_x$ buffers by HRXRD, Annual Meeting of the Swiss Physical Society, Bern, Switzerland, February 25, 1999 (talk)

4. Si overgrowth of self-assembled Ge clusters on Si(001) — a scanning tunneling microscopy study, Spring Meeting of the European Materials Research Society, Strasbourg, France, June 1-4, 1999 (talk)

5. Strain anisotropy and step structure of relaxed step-graded Si$_{1-x}$Ge$_x$ buffer layers, EPS-CMD 18, Montreux, Switzerland, March 13-17, 2000 (poster)

6. Ge segregation in thick strained SiGe/Si(001) films grown at high rates, Fall Meeting of the Materials Research Society, Boston, USA, November 27 - December 1, 2000 (poster)

7. Structural quality of virtual substrates and Ge-rich channels for high-speed SiGe p-MOS devices, Fall Meeting of the Materials Research Society, Boston, USA, November 27 - December 1, 2000 (poster)

8. Low Energy Plasma Enhanced Chemical Vapor Deposition, Spring Meeting of the European Materials Research Society, Strasbourg, France, June 5-8, 2001 (invited talk)

9. LEPECVD — a novel process for high-speed heterostructure SiGe FET’s, 10th International Conference on Modulated Semiconductor Structures (MSS10), July 23-27, 2001, Linz, Austria (poster)
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[22] S. Mantl. Strain relaxation of pseudomorphic $\text{Si}_{1-x}\text{Ge}_x$ layers on Si(100) after helium ion implantation (presented at the Spring Meeting of the European Materials Research Society 2001, Strasbourg, France).


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