Doctoral Thesis

MCM integration technologies for 60-80 GHz applications

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MCM Integration Technologies for 60–80 GHz Applications

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Contents

Abstract vii

Zusammenfassung ix

1. Introduction 1
   1.1. Motivation and Objectives ........................................... 2
   1.2. Thesis structure ..................................................... 5

I Technologies 7

2. Technology alternatives for millimetre wave applications 9
   2.1. Low Temperature Co-fired Ceramic (LTCC) ......................... 9
   2.2. MCM-L ............................................................... 12
   2.3. MCM-D ............................................................... 13
   2.4. Bulk micromachining techniques ................................... 14
      2.4.1. Membrane-supported technology ................................ 14
      2.4.2. Micromachined shielded quasi-planar circuits .............. 16
      2.4.3. Discussion ....................................................... 17
   2.5. Integrated rectangular waveguides ................................ 19
      2.5.1. Multi-layer dielectric-filled waveguides .................... 19
      2.5.2. Micromachined waveguides ................................... 20
      2.5.3. Discussion ....................................................... 22

3. An MCM-D build-up for single substrate integration 23
   3.1. A modified MCM-D technology for single substrate integration 24
      3.1.1. CPW versus microstrip lines ................................... 25
      3.1.2. Performance-oriented BCB dielectric thickness optimisation ....................................................... 26
      3.1.3. Technological requirements ..................................... 32
   3.2. Technology setup ................................................... 35
   3.3. Simulation and measurement techniques ............................ 38
   3.4. Examples of integrated passives ................................... 39
      3.4.1. Transmission lines and discontinuities ...................... 39
      3.4.2. Series resistors and compensated loads .................... 47
3.4.3. Low-pass filters at 65 GHz and 79 GHz .......................... 51
3.4.4. Band-pass filters at 59 GHz, 76 GHz and 94 GHz .... 53
3.4.5. Wilkinson power divider at 60 GHz and 94 GHz .... 56
3.4.6. Branch-line coupler at 60 GHz ............................... 59
3.4.7. Balun at 58 GHz .............................................. 59
3.4.8. Rat-race at 78 GHz ........................................... 62
3.4.9. Single-section line coupler at 78 GHz ..................... 62
3.4.10. Patch Antennas ............................................... 63
3.4.11. Antenna arrays at 78 GHz .................................. 68
3.5. An MCM-D/L technology for patch antenna performance enhancement ................................................................ 76
3.6. CPW on a low dielectric constant MCM-D substrate ........................................................................ 78
3.7. Quasi-CPW and quasi-ACPS transmission line media ........................................................................... 81
3.7.1. Applications ........................................................ 86
3.8. Summary .................................................................... 89

4. An MCM-L process for mm-wave applications ................................................................. 91
4.1. Process development .................................................................................. 93
4.1.1. Base material selection ................................................................. 93
4.1.2. Laminate material selection ............................................................ 93
4.1.3. Metal pattern ................................................................................. 96
4.1.4. Formation of vias and cavities ....................................................... 97
4.1.5. Chip-to-PWB transition ............................................................. 98
4.2. Summary ......................................................................................... 101

II De-embedding and extraction techniques ..................................................................... 103

5. VNA measurement technique with probe-tips .......................................................... 105
5.1. Introduction .................................................................................. 106
5.2. Two-tier calibration for 2-port on-wafer measurements ............................................ 108
5.2.1. Measurement results and accuracy considerations ........................................ 110
5.3. Characteristic impedance de-embedding for CPW lines ...................................... 112
5.3.1. Methods and limitations ................................................................ 112
5.3.2. Problem formulation ....................................................................... 113
5.3.3. Characteristic impedance de-embedding for tapered-fed CPW lines .......... 117
5.3.4. Experimental results ...................................................................... 119
5.4. Characteristic impedance de-embedding for CBCPW lines ............................ 126
5.4.1. Experimental results ..................................................................... 127
5.5. Characteristic impedance de-embedding for microstrip lines 133
  5.5.1. FW-CBCPW-microstrip transition modelling ...... 134
  5.5.2. Experimental results .............................. 138
5.6. Multi-port measurements ................................. 140
  5.6.1. Characterisation of the reciprocal 3- and 4-ports ... 142
5.7. Summary .................................................. 143

6. Extraction of dielectric properties for thin dielectric layers 145
  6.1. Problem statement ........................................ 146
    6.1.1. Printed line resonators ............................ 148
  6.2. Overview of the extraction procedure .................. 153
  6.3. Testing the accuracy of the closed-form equations .... 156
  6.4. Single dielectric configuration ......................... 157
    6.4.1. Quasi-static analysis ............................... 158
    6.4.2. Modelling of high-frequency dispersion ............ 160
    6.4.3. Accuracy results .................................... 162
  6.5. Multi-layer dielectric configurations .................. 166
    6.5.1. Quasi-static analysis ............................... 167
    6.5.2. Modelling of high-frequency dispersion ............ 171
    6.5.3. Dielectric loss tangent ............................. 172
    6.5.4. Accuracy results .................................... 173
  6.6. Extraction results ...................................... 180
  6.7. Summary .................................................. 187

7. Conclusions ................................................ 189

A. Reciprocity relations in waveguide junctions 193
B. Higher-order effects in wafer probing environment 197
C. High-frequency dispersion of microstrip lines 201
D. Conformal mapping for multi-layer microstrip lines 205

Glossary .......................................................... 209

Bibliography ..................................................... 213

Curriculum Vitae ................................................. 235
Abstract

This research addresses the development of a set of MCM (Multi-Chip Module) integration technologies for 60–80 GHz applications. It spans different topics related to their extensive characterisation and to the establishment of precise measurement and de-embedding methods of series of material and circuit parameters at mm-wave frequencies.

The first developed technology aims at a single substrate integration of mm-wave modules. It is a modified multi-layer BCB-based (Benzocyclobutene) MCM-D (Multi-Chip Module with deposited interconnect) process with a performance-oriented optimally chosen dielectric thickness. An extensive study of various factors determining the performance of integrated interconnect structures, distributed passives and antennas at frequencies up to 100 GHz was carried out. This information was used to justify the choice of the microstrip configuration based on the BCB dielectric only with its appropriate thickness. To outline the potential of the developed technology for the integration at 60–80 GHz, over 1000 S-parameter measurements of different transmission line elements, loads, distributed passives and antennas were performed up to 100 GHz. The simulated performance of some other integrated passives at 78 GHz and 94 GHz, including patch antenna arrays, shows the capability of the developed technology for applications at even higher frequencies. A concept of a mixed MCM-D/L technology was developed for an enhancement of the patch antenna efficiency and bandwidth. Additionally, the constraints of the CPW configuration usage in hybrid technologies at mm-wave frequencies were analysed. On the basis of this analysis, a two-layer quasi-CPW configuration, formed by an elevated centre conductor, was proposed. It results in a via-less realisation of bridges and tunnels, therefore, promoting further miniaturisation of different transmission line discontinuities, required at these frequencies.

The other developed process is an MCM-L (Multi-Chip Module with laminated interconnect) build-up. It is supposed to be used for the realisation of SMT (Surface Mount Technology) compatible single die packages and standard functional units consisting of several chip bare dies and some optional integrated passive components at V-band, allowing an efficient implementation of a modular approach for the system integration. Active and passive devices integrated in the modules are positioned in cavities, allowing wire-bond suppression. Of special importance was the use of the liquid crystal polymer
(LCP) laminates, showing excellent thermo-mechanical, chemical and electrical properties at V-band frequencies.

In order to accurately characterise the performance of the newly developed MCM processes, reliable calibration techniques had to be developed. Relying on an off-wafer calibration only can lead to erroneous measurement results at mm-wave frequencies. An accurate on-wafer fabrication of calibration standards is, however, difficult if the goal is the characterisation of a newly established technology. Therefore, a technique, accounting for the differences between off- and on-wafer feed structures, was implemented using a principle of the calibration-comparison method [1–4]. Moreover, a thorough study of the state-of-the-art methods for de-embedding of the CPW line characteristic impedance was performed. As a result of this study, a novel technique with an automatic detection of the reference plane position was developed. This procedure was extended to the taper-fed CPW and Finite-Width CBCPW lines. Furthermore, a state-of-the-art two-step characteristic impedance de-embedding technique for microstrip lines, valid at mm-wave frequencies, was developed.

Finally, an in-situ procedure for a wideband determination of dielectric permittivities for thin dielectric layers was developed. It is based on the probe-tip measurements of microstrip line sets consisting of different line cross-sections and lengths. The high-frequency line dispersion at mm-wave frequencies and the low-frequency dispersion caused by slow-wave effects, considerably influencing the behaviour of thin microstrip lines, are addressed with high accuracy. Not only standard single-layer microstrip lines are considered but also more realistic in interconnect technologies composite dielectric build-ups and substrates with passivation layer.

This work was conducted within the European research projects LAP\textsuperscript{1} and LIPS\textsuperscript{2}.

\textsuperscript{1}LAP, Low Cost Large Area Panel Processing of MCM-D Substrates and Packages, Esprit Project no. 26261, BBW no. 97.0286

\textsuperscript{2}LIPS, Low Cost Interconnect, Packaging and Sub-system Integration Technologies for Millimetre-wave Applications, IST Project no. 30128, BBW no. 01.0301
Zusammenfassung


Der zweite entwickelte Prozess ist ein MCM-L-Aufbau, der für die Realisation von SMT-kompatiblen Einzel-Chip-Packages und funktionellen Standard-Einheiten mit mehreren, unverpackten, integrierten Schaltungen
und einigen optionalen integrierten passiven Elementen im V-Band verwendet werden kann. Er erlaubt eine effiziente Implementation eines modularen Ansatzes für die Integration. Aktive und passive Bauteile sind in Kavitäten positioniert, was das Verzicht auf Bonddrähten erlaubt. Von spezieller Bedeutung ist die Verwendung der Flüssigkristall-Polymer-Laminate (LCP), welche ausgezeichnete thermomechanische, chemische und elektrische Eigenschaften bei V-Band Frequenzen aufweisen.


Diese Arbeit wurde im Rahmen der europäischen Forschungsprojekte LAP³ und LIPS⁴ durchgeführt.

³LAP, Low Cost Large Area Panel Processing of MCM-D Substrates and Packages, Esprit Project no. 26261, BBW no. 97.0286
⁴LIPS, Low Cost Interconnect, Packaging and Sub-system Integration Technologies for Millimetre-wave Applications, IST Project no. 30128, BBW no. 01.0301
Introduction

Recently, there was a significant growth in wireless telecommunication applications such as cellular phones, wireless local area network, global positioning satellite communication, etc. However, $V$ (50–75 GHz) and $W$ (75–110 GHz) frequency bands were previously reserved for military and space applications.

Nowadays, new telecommunication services such as LMDS (Local Multi-point Distribution System) and MVDS (Microwave Video Distribution System) are generating growing market segments for microwave monolithic integrated circuits (MMIC) above 6 GHz [5]. Two important applications are observed for upcoming markets: point-to-point broadband radio links at 60 GHz [6–8] and intelligent adaptive cruise control (ACC) systems for automotive applications at 77 GHz [9], not to forget the ongoing activities in the space, defence and medical millimetre-wave markets which are also shifting towards low-cost solutions [10, 11]. Moreover, high resolution radiometric imaging at 94 & 140 GHz has a number of important applications, including aircraft landing systems or finding victims trapped in fires. Ultra-high data rate optical communications, using a ‘radio-fibre’ type of systems at 180 GHz could transform the way networks are distributed in the landscape. Finally, future directives on environmental pollution monitoring may require sophisticated terahertz sensors to be mass-produced cheaply.
1.1. Motivation and Objectives

Considering the importance of the above-mentioned new applications, a paradigm change in the system integration of millimetre-wave applications from high budgets and low volumes towards low costs and high volumes is underway. With respect to mm-wave front-end, this leads to great challenges for both transmitter/receiver circuitry and antenna. Today’s packaging technology of complex RF products based on traditional Chip & Wire approach on the single-layer structured ceramics and soft substrates assembled into metallic boxes with complex geometries, hermetic sealing and ceramic coaxial feedthroughs cannot be the answer for high volume production. A complete reformulation of this issue leads to the so-called System-on-Package concept (SoP) [12], wherein the traditional approach with sub-unit substrates is replaced by a common package base architecture [13] with a common multi-layer substrate. This approach allows the reduction of the overall substrate area required and a lower number of interfaces (lower loss). It also enables integration of matching structures, lumped and distributed passives, and antennas. Advantages of integrated passives over hybridally mounted devices are:

1. improved package efficiency
2. improved electrical high-frequency performance due to the reduced parasitics, leading to better performance or lower power consumption
3. elimination of a separate package for passives yielding the lower cost, reduced profile and weight
4. no assembly to board and thus reduced cost
5. improved reliability due to reduced solder joint failures.

Integration of RF elements with digital and low-frequency analog circuits on the same substrate is also essential to reduce the overall cost and physical dimensions of the entire system. The proposed approach also opens the perspective to integrate MEMS circuits.

An integrated antenna T/R module is a very interesting alternative for applications where compact design, low cost and high volume are important factors. However, integration of antennas or antenna arrays in a single substrate module is usually difficult because technological requirements driven by their performance characteristics (radiation efficiency, bandwidth) are opposite to those of non-radiating elements, where radiation effects are undesirable. Present solutions of the T/R systems with antennas are mainly hybrid
1.1. Motivation and Objectives

integration. They are bulky, often demand waveguides and introduce extra parasitics at the transition between antenna and transceiver. Monolithic integration of planar antennas in a few millimetre size MMIC was also shown to be possible above approximately 60 GHz [14–16]. It provides the possibility of reduced interconnect parasitics, small size and light weight. Nevertheless, it is expensive and causes parasitic radiating coupling between antenna and circuit because of very limited space available. Larger arrays are also impossible due to the same reason. The high dielectric constants of MMIC semiconductor materials imply that surface waves are more easily triggered in the substrate, thus, greatly deteriorating antenna radiation properties, especially radiation efficiency. To overcome this drawback, expensive micromachining techniques are used, artificially removing a substrate below antenna and, thus, locally synthesising a low dielectric constant region [17].

A feasibility of low-cost implementation of a system-on-a-package concept [12, 18] (SoP) for lower microwave frequency range based on multi-layer low-temperature cofired ceramic (LTCC) has been reported in [19, 20] and in [21–23] using fully organic multi-layer thin-film sequential build-up (SBU). An attempt to develop a mm-wave integration technology has been presented in [24, 25] utilising multi-layer BCB/Kapton films and in [26] using mixed glass/silicon process. The ability of the BCB-based MCM-D technology for integration of high performance RF and microwave circuits has already been demonstrated for lower frequencies [27–35]. Some integrated antennas realised using this technology were also presented [36, 37]. Recently, the use of spin-coated BCB films has also been reported for successful MMIC’s embedding into micromachined cavities on a silicon host substrate [38, 39].

Until now, however, there has been no major research above 50 GHz undertaken worldwide in MCM technology leading to comprehensive feasibility study of a system-on-a-package concept for the V and W frequency bands. The reason is that short wavelengths and increased reflections at discontinuities require a technology with very tight tolerances. As a result, monolithic processing techniques are thus far generally preferred, where possible. Among others, a silicon micromachining was identified as an enabling technology for higher integration and better performance at higher operating frequencies. It was used to improve the performance of conventional transmission lines and simple circuits up to W-band [40–47] and to develop integrated rectangular waveguides [48]. Recent advances in wafer stacking and vertical wafer transition designs opened the possibility for three dimensional micromachined ICs [49]. Nevertheless, expensive state-of-the-art manufacturing associated with this process disables the more widespread use of millimetre wave systems in the V and W frequency bands in a form and cost accessible
to everyday consumer.

On the basis of the above analysis, the first objective underlying this thesis can be formulated as follows:

**Objective I:** To develop a more cost-effective, high-performance, single substrate integration technology concept for 60–80 GHz applications. For successful implementation of this concept, an extensive study of various factors determining the performance of integrated interconnect structures, distributed passives and antennas at frequencies up to 100 GHz was required. This information was used for the simultaneous choice of the appropriate transmission media and technology setup with its consecutive modification in order to fulfil the demanding requirements imposed by mm-wave systems.

There is also a need to develop new cost-effective interconnection technologies for packaging of single mm-wave chip bare dies and sub-unit modules realising standardised functions that are compatible with high-volume mass production. Several ceramic-based packages for a surface mount in the V-band have been proposed [50–52]. Although, these packages show good RF performance, the cost issue still remains for the consumer products. Plastic packages are supposed to lower the costs but their poor fabrication accuracy has prevented the achievement of high performance at mm-wave frequencies. Moreover, vias were often considered unsuitable for vertical transitions in the mm-wave frequency range because of typical poor transmission characteristics [51]. The coupling slot, replacing vias, was reported above Ka-band (26.5–40 GHz) [51, 53]. However, its passband is limited. In spite of these obstacles, attempts to develop a plastic surface mountable package in the V-band using a general PWB process and a wire-bond technique were reported [54]. Concerning the above, the next objective of this thesis was:

**Objective II:** To develop a low-cost, fully organic interconnection process suitable for realisation of high-performance, SMT compatible, single die packages or standard functional sub-units consisting of several chip bare dies and some optional integrated passive components in the V-band. This approach allows efficient modular system implementation, according to different product specifications.

The other main objectives of this work are:

**Objective III:** To simulate, design and measure a comprehensive set of interconnect elements and discontinuities, lumped and distributed passives, antennas, and antenna arrays in order to validate the performance of the developed technologies for the V- and W-band applications.
Objective IV: To provide the precise characterisation methods of the process- and material-related parameters for the developed technologies up to 100 GHz, specifically addressing an in-situ wideband determination of dielectric permittivities for the thin dielectric layer materials used.

Objective V: To develop a set of calibration and de-embedding techniques allowing accurate characterisation of the designed structures. Relying only on an off-wafer calibration, performed by means of a calibration substrate with CPW calibration standards, can lead to erroneous measurement results at mm-wave frequencies, specifically if the transmission line topology differs from the CPW configuration.

1.2. Thesis structure

The main part of this thesis is divided into two parts. Part I is focused on the technology development process. It includes Chapters 2, 3 and 4. Part II is related to the de-embedding and extraction techniques applied in this work for accurate characterisation of the developed set of technologies. It consists of Chapters 5 and 6.

As a starting point, today’s available, state-of-the-art, integration and miniaturisation technologies, that could be taken into account as candidates for the realisation of mm-wave modules and systems, are summarised in Chapter 2. Their benefits and limitations are thoroughly discussed, specifically addressing their potential to realise different transmission media in the V-, W-band and above. A set of the considered technologies includes LTCC, MCM-L, MCM-D and bulk micromachining techniques.

The development of a mm-wave single substrate integration concept for 60–80 GHz applications utilising a modified multi-layer BCB-based MCM-D technology with a performance-oriented optimally chosen dielectric thickness is presented in Chapter 3. For successful implementation of this concept, an extensive study of various factors determining the performance of integrated interconnect structures, distributed passives and antennas has been carried out. This information was used to justify the choice of the microstrip configuration based on the BCB dielectric only with its appropriate thickness. Numerous measurements and simulation results were presented to show the potential of the developed technology for the 60–100 GHz applications. A concept of a mixed MCM-D/L technology was developed for an enhancement of the patch antenna efficiency and bandwidth. Furthermore, the analysis of constraints of the CPW configuration usage in hybrid technologies at V- and W-band frequencies led to the implementation of a two-layer quasi-CPW...
configuration, formed by an elevated centre conductor. This topology allows via-less realisation of bridges and tunnels, allowing higher miniaturisation of transmission line discontinuities required at these frequencies.

The other developed MCM-L process for the realisation of the SMT compatible single die packages and standard functional mm-wave units in the V-band is demonstrated in Chapter 4. The use of the recently developed liquid crystal polymer (LCP) laminates allowed a successful combination of excellent thermo-mechanical, chemical and electrical properties at V-band frequencies with a very low material cost.

Chapter 5 analyses the issues related to reliable VNA (Vector Network Analyser) measurements and calibrations in a mm-wave environment, emphasising the importance of an on-wafer calibration for the dielectric substrate permittivities and transmission line topologies considerably different from those for the off-wafer standard calibration substrates. However, an accurate fabrication of on-wafer calibration standards can be difficult if the goal is the characterisation of a technology under development. Therefore, a two-tier technique, accounting for the differences between off- and on-wafer feed topologies, was implemented using a principle of the calibration-comparison method [1, 2]. Moreover, a novel technique for de-embedding the CPW (Coplanar Waveguide) line characteristic impedance with an automatic detection of the reference plane position, valid for both lossless and lossy substrates, was developed. This procedure was extended to the taper-fed CPW and Finite-Width CBCPW (Conductor-Backed CPW) lines. Furthermore, a state-of-the-art two-step characteristic impedance de-embedding technique for microstrip lines, valid at mm-wave frequencies, was established.

In Chapter 6, a problem statement for determination of dielectric permittivities of thin dielectric layers, used in the developed process setups, is presented. The significance of in-situ de-embedding is underlined and the choice of the microstrip configuration as a measurement cell is explained. Furthermore, a detailed analysis of many drawbacks of a classical printed-resonators measurement technique at mm-wave frequencies is given. It justifies the decision of developing a novel, wide-band technique based on the probe-tip measurements of microstrip line sets consisting of different line cross-sections. This procedure allows direct separation between the dielectric material properties and and the metallisation-related parameters, without exact modelling of the latter. The high-frequency line dispersion at mm-wave frequencies and the low-frequency dispersion caused by slow-wave effects, considerably influencing the behaviour of thin microstrip lines, are addressed with high accuracy.

Finally, the main results of the thesis are summarised in Chapter 7.
Part I

Technologies
For the realisation of high-performance mm-wave systems, an integration technology capable of providing this state-of-the-art performance is essential. There are a number of technologies available to be considered for fulfilling these demanding requirements.

2.1. Low Temperature Co-fired Ceramic (LTCC)

Recently, low temperature co-fired ceramic (LTCC) has gained more popularity for its claimed low-cost processing. One of the main drawbacks of
this process, limiting its accuracy, is the shrinkage of ceramic tapes during the firing process. Typically, the tapes shrink between 12–16% in the horizontal dimensions and 15–25% in the vertical. Typical shrinkage tolerances are +/-0.2% and +/-0.5% for both directions, respectively, and are dependent on the amount of conductor material on every layer. Fabricating multi-layer structures with typical dimensions of 5” x 5” results in length and width differences between layers as large as 250 µm, thus, possibly leading to opens and shorts in a high density design incorporating fine lines and spacings. As a result, a dense packaging and miniaturisation is achieved by exploiting three dimensional capabilities of this technology. Unfortunately, this 3D configuration causes large modelling difficulties even at lower microwave frequencies, limiting the use of LTCC for practical circuit design. The realisation of this 3D packaging scheme becomes difficult at mm-wave frequencies because of considerably higher coupling between elements in thick substrates.

Another basic limitation of LTCC process is a coarse metal definition. The minimal line width and spaces that may be achieved with normal thick film techniques are typically 125 µm with a typical tolerance of +/-25 µm. The minimal conductor thickness is around 25 µm. The other two issues related to LTCC, which considerably influence mm-wave performance, are usually high loss tangent, \( \tan \delta \), values of the order of \( 10^{-2} \) and low quality of surface finish. Additional disadvantage is that ceramic-based tapes show high dielectric constant, \( \varepsilon_r \), typically 7–10. This, combined with a high minimum feature size for thick-film patterning process, results in a low reproducibility of the mm-wave circuits.

During last years, many efforts were undertaken to improve the quality of LTCC process.

To eliminate shrinkage altogether, some manufacturers promoted a tape on substrate technology (TOS) [55–57]. Shrinkage is virtually eliminated by laminating and firing each layer of tape on a substrate made of \( Al_2O_3 \), \( BeO \) or \( AiN \). While this eliminates any component assembly alignment problems associated with shrinkage, tape on substrate is a serial process requiring expensive ceramic substrate carrier and thus resulting in higher manufacturing costs. Another approach to solve the shrinkage problem was the development of Low Temperature Co-fired Ceramic on Metal (LTTC-M) [58] with a specially formulated multi-layer ceramic structure attached to a metal core. In this case, the ceramic firing and core attachment process occur in one and the same step, which is more cost-efficient solution than TOS. The resulting structure exhibits virtually no shrinkage in the plane of the substrate. However, vertical shrinkage is still an issue.

A family of photo-patterned thick-film materials have been developed to
address the lack of precision in thick-film technology. The FODEL material system [59–61] from Du Pont Inc., including photoimageable gold and silver conductors, yields 50 +/- 5 μm lines and gaps, and vias of 125 μm in diameter. The surface finish of a fired layer deposited on a 96% alumina substrate is in the range of 0.4–0.5 μm and a post-fired conductor thickness is around 10 +/- 2 μm. The drawback of this process is a still existing shrinkage of the fired layers equal to about 25 μm. Another state-of-the-art photo-processable thick-film material system, KQ [56, 57, 62], from Heraeus Inc. consists of a thick-film gold and a novel low dielectric constant (ε_r = 3.9), low loss (tanδ = 0.0018 at 40 GHz), LTCC material and is compatible with TOS technique. The lines and spaces as narrow as 25 μm are well defined for a 5 μm thick conductors. The process allows to resolve 75 μm vias and the surface finish of a fired layer on a 96% alumina is about 0.4 μm. A line attenuation of 0.04 dB/ mm and 0.165 dB/ mm at 40 GHz for for two different 290 μm and 80 μm wide 50 Ω microstrip lines on a 130 μm and on a 40 μm thick dielectric tape, respectively, was reported for this material system [63]. For comparison purposes, a line loss of 0.035–0.05 dB/ mm at 40 GHz for a 400 μm wide microstrip line on different 330 μm thick, low-loss, dielectric tapes realised using standard screen printing techniques was reported [64].

While substantially finer lines and spaces are available with photopatterned thick-film, this reduces the claimed cost benefits.

**Discussion**

As long as the frequency is low or the system specifications are relaxed, LTCC may be successfully used. At 60–80 GHz, however, the application of this technology for the practical integration of high-performance passive structures using planar transmission line media (microstrip lines or CPW) seems to be difficult. For the microstrip realisations, the dielectric tapes should offer very consistent and predictable thickness. As the thin dielectric layers are necessary for operation at 60–80 GHz, it imposes the accuracy limit on the thickness of LTCC tapes that is difficult to achieve. Furthermore, the use of thin dielectric tapes involves the need for precisely defined narrow strips and spaces required for the repeatable performance of many passive structures (see Sec. 3.1.2).

Taking into account a high dielectric constant of LTCC tapes, the realisation of precise CPW structures with appropriately narrow ground-ground spacing, necessary for avoiding substantial coupling and leakage to substrate modes at 60–80 GHz, seems to be also impossible.

However, LTCC technology can be very promising for the implemen-
tation of integrated waveguides at 80 GHz or above as the typical dimensions required for their realisation with ceramic tapes are in the range of 0.5–1.5 mm, thus, substantially relaxing requirements on metal pattern accuracy [65]. Unfortunately, the use of waveguides needs substantially higher amount of real-estate at the frequency range of interest when compared to the planar quasi-TEM lines. Additionally, there are no commercially available mm-wave active devices and MMICs that would be directly compatible with this transmission medium. This makes the idea of a complete mm-wave system integration using integrated waveguide structures still out of reach.

2.2. MCM-L

MCM-L (Multi Chip Module with laminated interconnect) is considered a low-cost technology and can be regarded as a laminated printed wire board (PWB) scaled to meet the requirements and dimensions of an MCM. Generally, the laminate layers are clad with a metal foil, resulting in rough metal surfaces at the laminate side. The conductor width and spaces as well as the via dimensions are typically 100–150 μm. A poor dimensional and electrical stability of laminate materials with both temperature and humidity, and a high coefficient of thermal expansion (CTE) are additional problem. The quality of MCM-L integrated passives is relatively poor due to low-quality dielectric materials used.

However, an emerging set of polymer dielectrics in sheet/film or liquid formulation offers a combination of low loss and low CTE [18]. The thinner films (20–60 μm per layer) used in new organic build-up technologies [22] offer the ability to design and implement modules at microwave frequencies. A better control of etching tolerances is achieved by electroless and electrolytic copper plating and UV lithography. Aggressive feature sizes of 25–50 μm lines with 50 μm spacings and 50 μm microvia technology were shown to be possible in the organic process [18, 66]. High quality factor of passive components within a multi-layer organic-based process was reported [18, 22], allowing successful integration of complete passive RF front-end functional building blocks for lower microwave frequencies. The quality factor of over 160 for a 3.4 nH (0.6 x 0.6 mm²) inductor with a self resonant frequency of 11.5 GHz was achieved [22]. Quality factors greater than 250 at 2.4 GHz were obtained for embedded capacitors [18].

In spite of these recent process developments, the accuracy control of the narrow metallisation feature sizes and of the dielectric thickness still prohibits a feasibility of many high-performance integrated passives at 60–80 GHz, specifically those based on tight coupling between the line sections. Never-
theless, this set of technologies seems to show potential to realise low-cost packaging schemes for single dies and standard functional mm-wave units consisting of several chip bare dies with some optional integrated passives.

2.3. MCM-D

Thin-film multi-layer MCM-D (Multi Chip Module with deposited interconnects) technology is fabricated by a sequential deposition of conductor, typically Cu or Al, and dielectric layers, usually polyimide or benzocyclobutene (BCB), on a substrate base made of ceramic, silicon, metal or laminate [28]. Thin dielectric layers are usually deposited by spin-coating process, yielding a very uniform, well-controlled thickness and almost mirror-like surface finish. The latter is important for ohmic loss minimisation at mm-wave frequencies. Vias can be formed by laser ablation, reactive ion etching or wet etching. Thin metal layers are deposited by sputtering. Further, additive processing by electroless plating or electroplating may also be done. The curing of dielectrics requires much lower temperature steps compared to LTCC. Temperatures are in the range of 200°C for BCB to 400°C for polyimide. The minimum conductor widths and spaces range from about 30 μm down to a few μm, depending on the metal thickness and exact process flow. The spin-coated thin dielectric layers generally show much lower dielectric permittivities than ceramic materials. This translates to longer physical lengths for a given electrical length, resulting in easier dimensional control.

A high reproducibility of small metal pattern features and precise dielectric thickness control offered by these technologies make them excellent candidates for the realisation of a fully integrated mm-wave system.

Discussion

As a typical dielectric layer thickness in MCM-D process varies between 2 μm and 7 μm, and a standard stack-up includes no more than 3 layers, the realisation of low-loss microstrip lines at mm-wave frequencies is impossible. In a result, the CPW configuration is used in the microwave integrated modules based on MCM-D process. In this case, thin-film dielectric can be coated on different substrates with varying dielectric constant from low to high. Both substrate options can generate feasibility problems for CPW realisation when moving to higher mm-wave frequencies.

The performance of CPW realisations on high dielectric constant substrates deteriorates dramatically because of leakage to substrate modes supported by a dielectric slab. Coupling to these parasitic modes, in general de-
dependent on the line ground-ground spacing, can be considerable higher for MCM-D than for MMIC because of substantial differences in metal pattern resolution (see also Appendix B and Sec. 3.1.1).

Low dielectric constant substrates allow better overmoding characteristics but they lead to wide CPW lines and thus high line width/wavelength ratio at higher mm-wave frequencies. This results in high reactances, radiation loss and phase shifts at meander and junction discontinuities, disabling the efficient realisation of high-performance mm-wave system (see Sec. 3.1.1). Two alternative approaches could be used for lowering a ground-ground spacing of the CPW lines: the use of quasi-CPW configuration, formed by an elevated centre conductor above the ground planes on both sides of the centre strip ([67]) or increasing a reference impedance of the realised structures. The former solution leads to an increased line loss, whereas the latter can result in compatibility problems with the commercially available MMIC circuits that are supposed to work in a 50 Ω environment.

2.4. Bulk micromachining techniques

Micromachining techniques can be applied to any semiconductor substrate but the use of silicon has major advantages in cost and direct integration of active circuits. Using semiconductor micromachining, a variety of quasi-TEM planar transmission lines can be developed that is able to have superior electrical performance at mm-wave frequencies. Basically, there are two techniques to realise this novel approach. The first utilises a membrane to support transmission line elements [40]. The other technique introduces integrated shielding cavities [40].

2.4.1. Membrane-supported technology

A membrane-supported transmission line may be considered as an evolution of the conventional microstrip or CPW lines (Fig. 2.1). It is able to support almost pure and non-dispersive TEM wave propagating through a two-conductor system embedded in a homogeneous environment. Homogeneity of the environment can be accomplished by a micron-thick diaphragm supporting the lines, while ground is provided by a metallised micromachined cavity. The pyramidal cavity in Si wafers can be fabricated using anisotropic etchant such as EDP (ethylene diamine pyrocatechol) and the vertical by means of deep reactive-ion-etching (DRIE) techniques [68]. In the process setup in [40], the applied membrane is a tri-layer SiO$_2$/Si$_3$N$_4$/SiO$_2$ configuration with the constituent thicknesses of 7000, 3000 and 4000 Å, respectively. Such
a thin membrane makes is transparent to propagating signals up to 3 THz. To date, membrane dimensions as large as 2 mm × 1.9 cm were reported [40].

Two basic membrane-based transmission line topologies were proposed: microshield line and shielded membrane microstrip (SMM).

Microshield line

The line geometry of a microshield line [40] can be seen as a CPW structure situated above a metallised, air-filled cavity (see Fig. 2.1). Its formation requires the use of two wafers: one with a micromachined cavity and the other with a metallised ground plane fully enclosing the cavity. Typical cavity height, \( h_c \) and width, \( w_c \), for circuits operated at 10-40 GHz were designed to be 350 \( \mu m \) and 800-2000 \( \mu m \), respectively.

7\(^{th}\)-order Chebyshev (0.5 dB pass-band ripples) stepped-impedance low-pass filters with the cut-off frequency at 25 GHz [40] and 85 GHz [41] were realised in the membrane-supported microshield line configuration. They showed a pass-band insertion loss of 0.5 dB and 1 dB, respectively. The following line dimensions, \( w \) and \( s \), were used for the low and high impedance sections: 40/680 \( \mu m \) (265 \( \Omega \)), 1320/40 \( \mu m \) (45 \( \Omega \)) for the first filter and 20/280 \( \mu m \) (277 \( \Omega \)), 540/20 \( \mu m \) (63 \( \Omega \)) for the second. The corresponding cavity widths, \( w_c \), were 1800 \( \mu m \) and 800 \( \mu m \) for both circuits. The filters were fed by a 75 \( \Omega \) (350/35 \( \mu m \)) and a 92 \( \Omega \) (220/50 \( \mu m \)) line, respectively.

Figure 2.1: Microshield line (left figure) and shielded membrane microstrip line (SMM) (right figure).

Shielded Membrane Microstrip (SMM)

Thin dielectric membranes also provide the foundation for SMM [41]. The SMM line is essentially a shielded microstrip line with an air dielectric, resulting in low dispersion and low dielectric loss (see Fig. 2.1). Manufacturing of the SMM lines requires a three-wafer assembly, including the incorporation of an upper-half micromachined wafer with a partially removed silicon to
provide a ground plane for a microstrip signal. Formation of the ground-plane cavity (upper-half) requires specific attention. The etching depth, $h$, must be precisely controlled since it is crucial for tight control of the transmission line parameters. Temperature and etch area dependencies of the etch rate create difficulties in precise control of the cavity depth. The reported accuracy is in the range of ±5 μm for a nominal cavity depth of 100 μm. The analysis presented in [41] showed that this tolerance produced 1% deviation in both the centre frequency and the bandwidth for a 5-section coupled-line bandpass filter at 94 GHz with a nominal bandwidth of 4.3%. For thinner microstrip lines, preferable at this frequency (see Sec. 3.1.2), a tight thickness control can become problematic for many narrowband passive structures.

Three 5-section coupled-line band-pass filters at 94 GHz with equal-ripple Chebyshev characteristic were realised in the SMM configuration [41]. The circuits were normalised to the 90 Ω feed line. The heights of both upper and lower shielding cavities were 100 μm and 500 μm, respectively. The following insertion loss was achieved for the three different realisations:

1. $f_c = 94.7$ GHz, $B = 6.1\%$, passband insertion loss $= 3.6$ dB
2. $f_c = 95$ GHz, $B = 12.5\%$, passband insertion loss $= 2.2$ dB
3. $f_c = 94.9$ GHz, $B = 17.7\%$, passband insertion loss $= 1.4$ dB

2.4.2. Micromachined shielded quasi-planar circuits

Micromachining may also be used to develop the completely shielded planar circuits (see Fig. 2.2) [40, 42, 43] that are printed directly on the underlying substrate without the membrane support. Planar lines are defined on a high-resistivity, polished, silicon wafer using standard photolithography and electroplating process. This technique requires the use of two silicon wafers, one of which has upper-half shielding cavities, while the other accommodates planar circuits and substrate-filled lower-half cavities. The two wafers are attached using regular adhesion methods or Si-to-Si electrobonding.

Additionally, a variable thickness micromachining option [43] realised by selective time etching techniques extends the flexibility to the design of shielded circuits with locally reduced substrate thickness (see Fig. 2.2). Application of the partial depth micromachining was demonstrated in the design of different microstrip step-impedance low-pass filters with cutoff frequencies at 20 GHz and 35 GHz [44] for creation of an increased impedance ratio between the high and the low impedance line sections. In a result, a sharper cut-off frequency and a higher stop-band attenuation could be achieved, when compared to conventional realisations. Two approaches were
2.4. Bulk micromachining techniques

![Diagram of completely shielded planar line and partially shielded microstrip line](image)

**Figure 2.2:** Completely shielded planar line (left figure) and partially shielded microstrip line on a locally thinned silicon wafer (right figure).

applied. The first attempted to decrease the characteristic impedance value of low impedance line sections by local substrate thinning. In the second, local micromachining of an air cavity resulted in an increased characteristic impedance value for high-impedance line sections.

An insertion loss of 0.075 dB/mm at 40 GHz for a completely shielded line was reported in [42]. The line dimensions, \( w \) and \( s \), were 180 \( \mu \)m and 130 \( \mu \)m, respectively. The upper cavity was 280 \( \mu \)m high (\( h \)), whereas the lower 350 \( \mu \)m (\( h_s \)). Both were 800 \( \mu \)m wide (\( w_c \)).

A 43 \( \Omega \) microstrip line embedded in a lower shielding cavity in a locally thinned silicon wafer (\( h_s = 100 \ \mu \)m) showed an insertion loss of 0.14 dB at 40 GHz [45]. The line and cavity dimensions were: line width, \( w \), of 94 \( \mu \)m, distance to planar ground plane, \( s \), of 89 \( \mu \)m, cavity width, \( w_c \), of 413 \( \mu \)m.

### 2.4.3. Discussion

The evident drawback of the membrane-supported microshield line structures is a high minimal feasible characteristic impedance. The width of a 50 \( \Omega \) line realised in this technique would considerably exceed 1 mm, which is comparable to the wavelength at mm-wave frequencies. This minimal impedance value grows considerably with the frequency increase as the dimensions of cavities embedding the line structures are forces to be small enough in order to keep the waveguide modes under cut-off. Furthermore, the inherent high line width to wavelength ratio at higher mm-wave frequencies can lead to substantial degradation of behaviour of meander-like and junction-like discontinuities (see Sec. 3.1.2). This can limit the application of this technique to the integration of only some in-line passive circuits. The real advantage of this approach is represented by avoiding the radiation loss at higher frequencies and high isolation due to the inherent shield.

The micromachined shielded structures from Sec. 2.4.2 without membrane support seem to deliver more functionality as the presence of silicon
under the lines considerably lowers their width. Nevertheless, the lines are no more non-dispersive and they require the use of high-resistivity silicon for dielectric loss minimisation. Furthermore, the underlying silicon substrate should be substantially thinned to avoid surface wave excitation at mm-wave frequencies, which, in turn, requires local variation of etch depth.

The shielded membrane microstrip (SMM) configuration also seems to support the required functionality at mm-wave frequencies, if a substantially hollow cavity (defining the height of the microstrip line) is machined. However, with the so far reported process tolerances of the etch depth, some difficulties in the circuit realisations at higher mm-wave frequencies can arise if a precise frequency location or a narrow bandwidth is a must.

Concluding, micromachining technology can support the ultimate performance for many mm-wave applications but at the expense of state-of-the-art fabrication processing. For truly monolithic implementation, employing high performance active devices, multiple semiconductor layers have to be grown at the same time using expensive epitaxial growth techniques. This seems to be uneconomical when compared to hybrid solutions, employing drop-in active devices. None of the commercial monolithic technology vendors caters for micromachining. The development costs required for setting up a viable micromachining process could far exceed the returns expected from future commercial activities, especially if multi-layer hybrid equivalents are able to present more cost-effective alternative.

In typical mm-wave applications, where metallic housing is used to protect circuit components from the environment, unwanted parasitic modes and multiple resonances are introduced due to the presence of a large metallic shielding package. The micropackaging concept, allowed by micromachining, is able to eliminate these resonances by developing shielded structures that are small in size and can follow individual circuit paths [46, 47]. These self-packed circuits can therefore be effectively used within larger conventional housing, where the circuit response is now electrically decoupled from interactions with the larger metallic package. For this purpose, the use of bulk micromachining techniques seems to be interesting because the higher production cost could be offset by the required high isolation level and simplicity of the resonance-free package design at mm-wave frequencies. However, it should be noted that not only semiconductor substrates can be a subject of micromachining to produce micropackages. Commercially available SU-8 negative photoresist [69], showing excellent micromachining properties combined with photolithographical techniques and curing temperatures below $100^\circ C$ could be an alternative solution substantially decreasing a pro-
2.5. Integrated rectangular waveguides

At mm-wave frequencies, the metal pipe rectangular waveguide (MPRWG) can be an alternative choice for implementing a high performance guided-wave structure [70]. It shows much lower current densities compared to conventional microwave transmission lines and the propagating fields are contained within the enclosed cylinders, resulting in no leakage of electromagnetic energy. This solution presents the opportunity for realising high-Q cavity resonators, low loss coupled-cavity and $E$–& $H$–plane filters, or compact end-fire antennas.

Conventional machining techniques for waveguides operating above 80 GHz are complicated and costly. Development of low-cost fabrication techniques for integrated counterparts is of special importance for millimetre and submillimetre wave system integration. Essentially, there are two possibilities to create metal pipe rectangular waveguides:

- micromachining resulting in air-filled structures
- multi-layer technologies leading to dielectric-filled geometries.

Attempts to develop the integrated waveguide structures by each of the above-mentioned processing methods were reported by different authors. The following subsections present a concise summary of the reported results.

2.5.1. Multi-layer dielectric-filled waveguides

The multi-layer technologies show two basic advantages for creation of waveguide structures when compared to micromachining techniques:

- A multi-layer MPRWG having a dielectric filler with relative permittivity, $\varepsilon_r$, can achieve a reduction in the physical area by factor of $\varepsilon_r$ for the fixed $f_o/f_c$ value ($f_o$ is an operating frequency and $f_c$ is a waveguide mode cut-off frequency) at the cost of small loss increase for low-loss dielectrics.

- With dielectric-filled MPRWG, more innovative structures can be investigated, when compared to air-filled counterparts. This is especially the case when other forms of rectangular waveguides are employed, such as fin lines and dielectric-slab waveguides. These other forms of guided-wave structures can be used to implement effective transitions
between dielectric filled MPRWG and free-space or planar transmission lines [70, 71].

However, the filling dielectrics have to show the lowest possible loss and constant permittivity at millimetre frequencies. The presence of unwanted molecular resonances can exclude the use of many dielectrics at these frequencies such as spin-on polyimide and glass dielectrics based on polysiloxan polymers with similar characteristics as amorphous $SiO_2$ [71]. They should allow creation of very smooth surfaces, thereby minimising losses. Thin-film BCB and spin-on glasses are good candidates, when material dielectric properties are considered. The major problem is that the layers tend to crack as the thickness increases and, thus, they cannot support the appropriate waveguide height for loss minimisation. LTCC and thick-film photoimageable materials can support the right thickness but dielectric loss and the difficulty of the screen printing process for precision multi-layering can be of concern.

A rectangular waveguide operating at 60-90 GHz ($TE_{10}$) constructed using thick-film photoimageable TOS (Tape on Substrate) technology was presented in [72]. The standard dimensions, 3.1 mm $\times$ 1.5 mm, of the hollow rectangular waveguide could be scaled down to 1.22 mm $\times$ 0.6 mm for a photoimageable dielectric paste ($\epsilon_r = 7$). Unpolished 99.6% alumina was used as a substrate carrier. The side walls were produced by 100 $\mu$m wide rectangular vias. Only 2 prints were used because of a difficulty of the screen printing process for precision multi-layering. It resulted in the waveguide height of only 18 $\mu$m and high loss of 0.5 dB/mm in the E-band (60–90 GHz).

In [65], a 1.2 mm $\times$ 0.6 mm rectangular dielectric-filled waveguide operating at 75–90 GHz with side walls constructed by lined via-holes and edges of metallised planes was realised in LTCC technology. A low-loss ($\tan\delta = 0.0008$ at 60 GHz) glass-ceramic of relative dielectric constant, $\epsilon_r$, equal to 5 was used as the filling material. The reported insertion loss was 0.085 dB per wavelength at 83 GHz. Due to the multi-layer flexibility of LTCC process, the laminated waveguide structures could be wired in three dimensions. Fundamental interconnect structures such as bends, branches, power dividers and vertical connections between upper and lower layers with sufficient performance were also presented. A 3-layer feed network based on the demonstrated waveguide elements was used to feed an array consisting of 16 x 16 Laminated Resonator Antenna (LRA) elements [73], resulting in an overall gain of 28.1 dB and an efficiency of 23% at 76.5 GHz.

2.5.2. Micromachined waveguides

Several micromachined waveguide structures were reported in literature:
• A 2.5 mm × 1.25 mm rectangular waveguide operating at 75-110 GHz was presented by W. R. McGrath et. al [48]. It is made of two half 1.25 mm polished silicon wafer sections split along broadwall. The vertical walls are formed by KOH (potassium hydroxide) etching and Cr/Au (200 Å/3.5 μm) metallisation layer is used for the waveguide walls. A very low loss of 0.04–0.06 dB per wavelength across most of the 75-110 GHz band (WR-10) was measured. It was suggested that active and passive devices could be integrated within the waveguide parallel to its length in the E-field direction using the previously described membrane-support technique (see Sec. 2.4.1).

• The waveguide designed by C. E. Collins et. al [74, 75] is 1.84 mm wide and has a cut-off frequency of 81.5 GHz for $TE_{10}$ mode. It is fabricated by first metallising a semiconductor wafer with a Ti/Au layer to form the bottom wall. A photoresist former defining the internal dimensions of the waveguide is then produced on top of this layer using photolithographic techniques and then coated with a 50 μm gold. Subsequent removal of the photoresist with solvent leaves an air-filled rectangular waveguide. The maximum height of the waveguide was limited to 100 μm by the maximum photoresist thickness. The theoretical calculated insertion loss of the designed waveguide was found to vary between 0.33 dB and 0.227 dB per wavelength over the 90–110 GHz frequency range. The measured attenuation was between 0.133 dB and 3.33 dB, being substantially higher than the calculated. The high loss was attributed to mismatches caused by the difficulty in achieving a precise transition to the full height waveguide that fed the measured structures.

• A recently introduced negative photoresist SU-8 [69] is capable of producing features in excess of 1 mm in height with large aspect ratios in a single UV exposure. This property was used by C. E. Collins et. al [76, 77] for manufacturing a substantially higher waveguide than the above-mentioned for reducing the attenuation. The structure is fabricated by consecutive spinning a thick layer of SU-8 onto a semiconductor substrate, exposing, baking and development to reveal ’throughs’ which will become the waveguide structures. These are sputtered with gold to form the inside walls. Finally, a pre-sputtered lid is attached over the lithographically formed throughs to complete the waveguide. For the waveguide cross-section of 2.54 mm × 0.7 mm (half height), an insertion loss of 0.2–0.3 dB per wavelength at 85–100 GHz was measured. This high loss was attributed mainly to the
join between the two waveguide side walls and the top lid.

2.5.3. Discussion

The major drawbacks of the micromachined waveguides seem to be [71]:

- High production cost resulting from a large number of processing steps and non-standard processing techniques, contrary to the dielectric-filled MPRWGs or classical quasi-TEM lines.

- The amount of real-estate required for one wavelength section of air-filled MPRWG is much larger than that for the same electrical length of quasi-TEM line or dielectric-filled MPRWG. Therefore, they are too expensive for monolithic integration below \textit{circa} 200 GHz.

- Fabrication of large hollow structures may be more susceptible to processing defects, compared to conventional quasi-TEM lines. The resulting low yield can considerably inflate costs.

- Above \textit{circa} 200 GHz, the kind of ubiquitous applications required to bring the cost down to affordable level do not exist and may not exist in the foreseeable future. Therefore, the benefits of high volume production for bringing down costs may not be achieved.

Despite the numerous attempts to develop integrated waveguide structures, a consistent integration technology of the entire millimetre wave systems combining the advantages of the waveguide structures as a transmission media with fully integrated active devices does not exist. Contemporary MMICs are realised in planar technologies which makes them incompatible with the waveguide technology and requires the design of complex transitions usually with poor performance. Therefore, it becomes important that when such chips are brought together the overall system performance degradation is not further compromised. This requires a complete reformulation to provide state-of-the-art performance of a complete sub-system, manufacturable without the need for bulky and expensive conventionally machined waveguide components. A new interesting concept for realising such an integrated system within an advanced low-loss multi-layer technology with a novel chip assembly technique was reported in [70, 71]. In this approach, MMIC circuits are supposed to be realised in fin-line or slot-line topology, and positioned inside the waveguide’s slots in order to achieve the most efficient coupling between the MPRWG and the active devices on the chip side.
An MCM-D build-up for single substrate integration

In this chapter, the development of a mm-wave single substrate integration concept for 60–80 GHz applications utilising a modified multi-layer BCB-based MCM-D technology with a performance-oriented optimally chosen dielectric thickness is presented [140, 141].

For successful implementation of this concept, comprehensive understanding of the problems encountered at mm-wave frequencies is critical. For this purpose, an extensive study of various factors determining the performance of integrated interconnect structures, distributed passives and antennas has been carried out and the findings are presented in Section 3.1. The constraints of the CPW configuration usage in hybrid technologies at higher mm-wave frequencies are outlined and their implications for the design and performance of different passive elements analysed. This information is used to explain the choice of the microstrip configuration based on the BCB dielec-
tric only with its appropriate thickness. The process of finding this optimal thickness is also described. Section 3.2 gives a brief description of the developed technology setup. In Section 3.3, a general overview of the simulation and measurement techniques used is presented.

To outline the potential of the developed technology for the integration at 60–80 GHz, Section 3.4 presents the measurements results of a number of basic elements: transmission lines and discontinuities, series resistors, frequency compensated loads, low-pass and band-pass filters, Wilkinson power divider, branch-line and rat-race couplers, balun and patch antennas [141]. The full-wave simulated performance of some different integrated passives at 78 GHz and 94 GHz, including patch antenna arrays, is also presented, showing the potential of the developed technology for applications at even higher frequencies. In Section 3.5, a concept of a mixed MCM-D/L build-up was proposed [140] for enhancing the patch antenna efficiency and bandwidth. The results reported in this work demonstrate, for the first time, a low-cost integration of ultra low-loss, low parasitic interconnects and high performance passive components in the 60–80 GHz frequency band. To the knowledge of the author, such performance was never reported before for many of the presented structures or achieved using more expensive processing techniques such as micromachining [40–42, 44, 142, 143].

For comparison purposes with the above proposed microstrip configuration oriented technology build-up, an alternative MCM-D technology setup, allowing the use of the CPW line topology, was investigated in Section 3.6.

On the basis of numerous full-wave simulation and measurement results of different transmission line discontinuities and distributed passives, a set of critical drawbacks of the CPW topology in hybrid technologies above 50 GHz was presented. It led to the proposal of the quasi-CPW and quasi-ACPS transmission line alternatives (Sec. 3.7), taking advantage of a multi-layer technology build-up.

The chapter concludes with a summary in Section 3.8.

### 3.1. A modified MCM-D technology for single substrate integration

There are several advantages related to the use of thin-film MCM-D technology for system integration as compared to more traditional hybrid technologies (PWB or LTCC). This technology yields high precision components, very good manufacturability and repeatability of complete RF structures. It also opens the perspective to integrate MEMS and antennas or antenna arrays, which is not possible in a single chip solution [28]. It allows common
low-cost digital and high performance analog integration, especially if a large area processing option [144–148] is used.

The spin-coated BCB shows some important advantages: low dielectric constant (in-house extracted 2.635–2.65; see Sec. 6.6) with high temperature stability, low loss tangent (0.0008–0.002, depending on frequency), photosensitivity and insensitivity to moisture absorption (self-protection feature). It allows fine line resolution, very precise thickness definition of 0.3–0.5 \( \mu m \) per layer (see Sec. 3.2) and shows very low surface roughness (a few nm; see Sec. 3.1.3). The latter is critical for ohmic losses at mm-wave frequencies.

The low BCB dielectric permittivity leads to the similar phase velocities for even and odd modes of the coupled-line sections, allowing broadband characteristics and high directivities of the elements based on the coupled-line topology without the need for any compensation techniques (see Sec. 3.4).

3.1.1. CPW versus microstrip lines

As discussed in Sec. 2.3, a typical dielectric layer thickness in MCM-D process varies between 2 \( \mu m \) and 7 \( \mu m \), and a standard stack-up includes no more than 3 layers. Using such a dielectric build-up, the realisation of low-loss microstrip lines at mm-wave frequencies is unfeasible. This leads to the common use of the CPW topology. In this case, a thin-film dielectric can be coated on different substrates with varying dielectric constant from low to high. Both substrate options can generate feasibility problems for the CPW realisation when moving to higher mm-wave frequencies. The performance of CPW structures on high dielectric constant substrates (typically ceramics) deteriorates dramatically because of surface wave excitation and the presence of parallel plate waveguide modes. The latter are caused by a backside metallisation normally existing in a packed module [149–153]. Furthermore, box-type resonances can occur due to a finite substrate size [104, 105, 154]. These issues can lead to complex and costly solutions such as wafer thinning, backside processing or multi-layer composite dielectric substrates [155–157]. Coupling to these parasitic modes, in general dependent on the line ground-ground spacing, can be considerable higher for MCM-D than for MMIC because of substantial differences in a metal pattern resolution (minimum slot width of 20 \( \mu m \) for MCM-D is assumed for high yield). The finite-ground CPW (FGCPW) configuration [158, 159] is able to minimise the influence of some of the above-mentioned parasitic coupling effects. Unfortunately, its use for backside metallised substrates is not straightforward because of possible conversion to the microstrip-like (MSL) modes (see Appendix B) at different discontinuities, specifically open-ended structures [103, 160, 161].
Choosing a low dielectric constant substrate, such as the one of our substrate options, ROGERS 4003 (nominal $\varepsilon_r = 3.38$), allows using larger processing panels with increased thickness, offering higher mechanical and processing stability with better overmoding characteristics. On the other hand, its use results in wide CPW lines and, thus, in high line width/wavelength ratio at higher mm-wave frequencies. The ground-ground spacing for a 50 $\Omega$ line on a BCB-ROGERS 4003 dielectric build-up exceeds 200 $\mu$m (assuming minimum 20 $\mu$m slot). This leads to high reactances and phase shifts at meander and junction discontinuities, often disabling the realisation of distributed passives without matching or isolation problems. The issue of high line width/wavelength ratio could partially be solved using a two-layer quasi-CPW configuration, formed by an elevated centre conductor above the ground planes on its both sides [67] (see Sec. 3.7 for the line geometry definition). This topology allows to arrive at narrower lines for the same characteristic impedance in comparison to the standard single-layer CPW configuration.

Taking into account the above discussed complexity of the CPW solution, the author opts for the microstrip configuration based only on the BCB dielectric with its appropriate thickness. In this case, choice of the main substrate carrier plays no role from the electrical performance point of view because the carrier and the thin-film layers are separated by a buried ground plane.

### 3.1.2. Performance-oriented BCB dielectric thickness optimisation

At lower microwave frequencies, the dielectric thickness optimisation for the circuits realised in the microstrip configuration is usually viewed as a simple substrate thickness increase in order to arrive at wider microstrip lines, thus, implying lower line loss. This approach indicates that insertion loss of a straight line section is one of the most important factors determining the performance of interconnect elements, integrated passives and entire integrated system. It is, however, absolutely false for mm-wave frequencies. When considering the performance of a mm-wave system, a substantially larger number of factors has to be taken into account (see Table 3.1). Due to the short wavelengths at 60–80 GHz, the loss of straight transmission line sections is of lesser importance for the performance of typical passives in comparison to the influence of transmission line discontinuities. Too thick substrates cause strong coupling to surface waves. This, in turn, results in highly dispersive and lossy non-quasi TEM transmission line elements with poor inter-circuit isolation. They also lead to a high line width/wavelength ratio, resulting in large parasitics, radiation and high phase shifts at meander or junction-like transmission line discontinuities and, thus, making the system design impos-
3.1. A modified MCM-D technology for single substrate integration

Table 3.1: Factors determining the performance of a mm-wave system taken into consideration in the process of the BCB thickness optimisation. Parameters marked with (+) increase the system performance with a thicker dielectric substrate, whereas those marked with (−) decrease it.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>BCB dielectric thickness increase</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line loss</td>
<td>(+)</td>
</tr>
<tr>
<td>Patch antenna efficiency</td>
<td>(+)</td>
</tr>
<tr>
<td>Line dispersion</td>
<td>(−)</td>
</tr>
<tr>
<td>Line width/wavelength ratio</td>
<td>(−)</td>
</tr>
<tr>
<td>Radiation at discontinuities</td>
<td>(−)</td>
</tr>
<tr>
<td>Reactances at discontinuities</td>
<td>(−)</td>
</tr>
<tr>
<td>Inter-circuit isolation</td>
<td>(−)</td>
</tr>
<tr>
<td>Shorting ground inductance</td>
<td>(−)</td>
</tr>
<tr>
<td>Design simplicity</td>
<td>(−)</td>
</tr>
</tbody>
</table>

The goal of the BCB thickness optimisation for the microstrip configuration at 60–80 GHz is to achieve a trade-off between relatively low microstrip line loss, relatively good patch antennas efficiency on one side and low line dispersion, low line width/wavelength ratio, low reactances, low radiation, low surface wave excitation at transmission line discontinuities, high inter-circuit isolation, short grounding paths on the other side. It needs very careful judgement considering the performance of different interconnect structures, distributed passives, antennas and antenna array feed networks. This trade-off defines a technology platform allowing to avoid complex physical effects deteriorating the performance of a mm-wave system and to make its design as simple as in the lower microwave frequency range. A brief analysis of the above-mentioned factors in view of their relation to the BCB dielectric thickness will be presented below.

Table 3.2 presents the simulated loss of a 50 Ω microstrip line for different BCB thickness. It can be seen that the loss is already reasonably low for the thickness of 45–60 μm and decreases slowly for thicker BCB. For a 45 μm thick BCB, it results in a 1.25% power loss at 100 GHz for a quarter wavelength line section, typically existing in distributed passives. The same line section on a 100 μm thick BCB shows only slightly better power loss of 0.84%. The main contributors are ohmic losses (80%), according to the simulations. Table 3.3 shows the simulated line loss and wavelength for different microstrip line geometries on a 45 μm thick BCB and, for comparison purposes, for CPW lines on a 45 μm/500 μm ROGERS 4003. It can be noticed
Table 3.2: Simulated attenuation of a 50 Ω microstrip line vs. BCB thickness. Simulations were performed with HFSS. A 3 μm thick copper conductor and the BCB loss tangent of 0.002 were assumed in the simulations.

<table>
<thead>
<tr>
<th>BCB thickness in [μm]</th>
<th>50 Ω line width in [μm]</th>
<th>α [dB/mm] at 60 (80 GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>30</td>
<td>0.18 (0.21)</td>
</tr>
<tr>
<td>30</td>
<td>70</td>
<td>0.1 (0.115)</td>
</tr>
<tr>
<td>45</td>
<td>112</td>
<td>0.067 (0.086)</td>
</tr>
<tr>
<td>60</td>
<td>150</td>
<td>0.058 (0.072)</td>
</tr>
<tr>
<td>100</td>
<td>240</td>
<td>0.045 (0.055)</td>
</tr>
</tbody>
</table>

Table 3.3: Simulated line attenuation and wavelength at 60 GHz for different microstrip lines on a 45 μm thick BCB and CPW lines on a 45 μm/500 μm BCB-ROGERS 4003 build-up. Simulations were performed with HFSS (Parameter ‘w’ denotes a strip width for both microstrip and CPW configurations, whereas ‘s’ slot width for CPW lines only).

<table>
<thead>
<tr>
<th>Config.</th>
<th>Geometry [μm]</th>
<th>Z₀ [Ω]</th>
<th>α [dB/mm] at 60 (80 GHz)</th>
<th>λ [mm] at 60 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microstrip</td>
<td>w = 194</td>
<td>35</td>
<td>0.068 (0.082)</td>
<td>3.28</td>
</tr>
<tr>
<td>Microstrip</td>
<td>w = 112</td>
<td>50</td>
<td>0.067 (0.083)</td>
<td>3.35</td>
</tr>
<tr>
<td>Microstrip</td>
<td>w = 62</td>
<td>70</td>
<td>0.072 (0.086)</td>
<td>3.42</td>
</tr>
<tr>
<td>Microstrip</td>
<td>w = 28</td>
<td>100</td>
<td>0.082 (0.098)</td>
<td>3.5</td>
</tr>
<tr>
<td>CPW</td>
<td>w/s = 230/20</td>
<td>50</td>
<td>0.076 (0.092)</td>
<td>3.61</td>
</tr>
<tr>
<td>CPW</td>
<td>w/s = 166/52</td>
<td>70</td>
<td>0.052 (0.063)</td>
<td>3.59</td>
</tr>
<tr>
<td>CPW</td>
<td>w/s = 90/90</td>
<td>100</td>
<td>0.05 (0.06)</td>
<td>3.59</td>
</tr>
</tbody>
</table>

that the microstrip line loss is only slightly dependent on a strip width because the current density at 60–80 GHz is the highest in the corners of a strip cross-section. Thus, the loss for a 50 Ω transmission line can be considered as a representative value. Moreover, the lines show no high-frequency dispersion up to 100 GHz and well above, as it will be shown in Sec. 3.4.1 due to the low BCB dielectric constant and its relatively low thickness.

The line width/wavelength ratio is another very important factor, determining the performance of meander and junction-like discontinuities and, thus, of different functional elements. It increases approximately linearly with the BCB dielectric thickness increase within the range of the considered thicknesses. For example, changing the BCB thickness from 45 μm up to 100 μm results in a considerable increase in the line width/wavelength ratio from 5.5% at 100 GHz up to 12% for a 50 Ω line. Furthermore, it can be noticed that a 45 μm thick 50 Ω microstrip line reduces the
line width/wavelength ratio by a factor 3 in comparison to the BCB-ROGERS 4003 CPW configuration, also considered in this work (see Table 3.3).

In order to investigate the influence of the BCB dielectric thickness on the performance of different distributed passives and antenna array feed networks, the behaviour of a variety of different transmission discontinuities was simulated. As the detailed investigation results are out of the scope of this section, only some simple examples, illustrating the influence of the substrate thickness, are presented:

- The first element is an open-ended 50 Ω transmission line which shows 1% and 5.5% power loss at 100 GHz on a 45 μm and on a 100 μm thick BCB, respectively. For the same thicknesses, the corresponding line extension values of the considered 50 Ω open-end constitute 1.2% and 3.5% of the wavelength at 100 GHz. As the radiation at discontinuities is an increasing squared (space waves) or cubed (surface waves) function of frequency, its influence on a mm-wave system performance is more important than that of the straight transmission line loss.

- The next structure is a 50-100-100 Ω T-junction with a right angle geometry. On a 45 μm thick BCB, it is possible to achieve a return loss better than 30 dB at the 50 Ω port and 1.2% power loss at 80 GHz. The same junction on a 100 μm thick BCB shows only 17 dB return loss and 7% loss (mainly radiation). After its optimisation, by changing the angle between the two output branches, it was possible to achieve only 4% radiation loss.

- The last example is a 50 Ω right angle meander line consisting of 8 chamfered bends and 9 (each 500 μm long) line sections (for more detailed description of the structure, refer to Sec. 3.4.1). The structure was designed so that the influence of parasitics associated with bends is cumulative at 80–90 GHz. The worst simulated return loss within the considered 1–100 GHz frequency band is 26 dB (at 95 GHz) and 15 dB (at 85 GHz) for the realisations on a 45 μm and on a 100 μm thick BCB, respectively. Furthermore, the power lost on the meander and on the equivalent transmission line of the same length differ by only 3% at 100 GHz for the former, whereas for the latter by as much as 28%.

As a typical dielectric layer thickness in MCM-D process is between 2 μm and 7 μm, and a standard stack-up includes no more than 3 layers (see Sec. 2.3), patch antennas realised using only thin-film dielectrics can achieve about 25% efficiency at frequencies even as high as 80 GHz [147, 148, 162].
The use of a few hundred μm thick substrate carrier, on which thin-films are coated, typically used at lower microwave frequencies to enhance the patch antenna performance, cannot be applied because of strong surface wave effects. As a consequence, process enhancement is needed in order to obtain thicker film and, therefore, an increase in antenna efficiency.

Fig. 3.1 presents the simulated efficiency of a directly fed rectangular patch antenna at 77 GHz with a width/length ratio of 1.5 versus BCB thickness. The efficiency increases slowly for BCB thicker than 45-55 μm (not shown) and achieves its maximum of 81% for a 100 μm thick film. Further thickness increase will result in a lowered efficiency due to the higher loss associated with surface waves. For a 45 μm thick BCB, the following antenna parameters are achievable for a single linearly polarised patch: radiation efficiency of 65–68%, directivity of 7.2–7.5 dB and bandwidth of 1.6 GHz (SWR = 2). The exact values within the presented ranges depend on the patch width.

![Figure 3.1: Simulated efficiency of a directly fed rectangular patch antenna at 77 GHz with a width/length ratio of 1.5 versus BCB thickness. The simulations were performed with HFSS. A 3 μm thick copper metallisation and the BCB loss tangent of 0.002 was assumed. An additional 8 μm thick BCB passivation on top was used.](image)

Concluding, it was found out that performance of a variety of open-ended, meander and junction-like discontinuities rapidly deteriorates for BCB thicknesses above 45–55 μm, while the line loss and patch antenna efficiency tend to saturate, showing already small changes with a dielectric thickness increase. In a result, these both groups of contrary factors define the “performance plateau” for the specified BCB thickness range that can be considered
3.1. A modified MCM-D technology for single substrate integration

as optimum in view of the performance of a general integrated mm-wave module.

**Antenna arrays**

Some applications such as a gaining popularity collision avoidance automotive radar at 77 GHz demand high antenna gain (see Table 3.4). The feasibility study of the antenna array integration in the developed MCM-D process was performed [140]. Two examples of the investigated structures are the hypothetical short-range and long-range radar arrays [163].

**Table 3.4: Estimated specifications for automotive radar antennas**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Short-range sensor</th>
<th>Long-range sensor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Centre frequency</td>
<td>76–77GHz</td>
<td>76–77GHz</td>
</tr>
<tr>
<td>Antenna gain</td>
<td>≥ 20dB</td>
<td>≥ 36dB</td>
</tr>
<tr>
<td>Main lobe width</td>
<td>10° x 20°</td>
<td>3° x 3°</td>
</tr>
<tr>
<td>Bandwidth [SWR = 2]</td>
<td>500 MHz</td>
<td>500 MHz</td>
</tr>
</tbody>
</table>

Taking into consideration typical directivity and dimensions of our patch antennas on a 45 μm BCB (see previous section), approximately 9 x 4 and 33 x 31 elements (a bi-static antenna topology with five beams of 2.7° width is assumed) are required for the short-range array and long-range array, respectively [163], according to the specifications from Table 3.4. As high power levels are difficult to achieve at 80 GHz, the goal is to maintain the highest possible efficiency of the entire array. As a result, the typical corporate feeding, most often used, is rejected. In this case, the estimated efficiency of the 9 x 4 array is only about 25% (assuming an 68% patch antenna efficiency from previous section) due a long feeding path to every patch consisting of a 7λ long straight transmission line and 5 T-junctions. A hybrid-fed array with every 9 elements arranged in a series-fed row (see Sec. 3.4.11 for more detailed design analysis) allows to increase the array efficiency up to 53%. This is a result of the nature of a series feed, where the total equivalent feed path per radiating element can be approximated by a 3λ long transmission line section and 2 T-junctions. This array, integrated in a single substrate together with other T/R module elements, can be considered as a low-cost competitive solution to the externally connected antenna with even higher efficiency because the total effective efficiency, including necessary transition between the external antenna and integrated T/R module, does not seem to be higher [164].

The realisation of a planar array with a 36 dB gain and an efficiency higher
50% at 78 GHz, although dimensionally possible, is unfeasible because of the physical limits imposed by the skin effect defined ohmic losses. An alternative compact solution could be achieved by the integration of slot antennas on a thin-film deposited on dielectric lenses [165]. This approach, however, is more expensive and no longer flat (radius of 15–20 \( \lambda \) for the lenses is needed, i.e. a few centimetres).

**3.1.3. Technological requirements**

**Metallisation process vs. line loss**

The following factors related to the metallisation process have to be addressed while considering the transmission line losses at higher mm-wave frequencies: choice of a conductor material, its layer thickness, line width and edge profile, surface roughness of an underlying dielectric, metal deposition and patterning method.

Copper conductors are often used in hybrid technologies for their high conductivity (\( \sigma = 5.88 \times 10^7 \, \text{\mho m}^{-1} \)). However, they require a passivation layer against oxidation and a barrier layer to avoid electromigration. Gold conductors have slightly lower conductivity (\( \sigma = 4.55 \times 10^7 \, \text{\mho m}^{-1} \)) but they require no passivation or barrier layers. A choice between different conductor materials in view of the ohmic losses at 60–80 GHz plays no role for a typical conductor thickness above 1-1.5 \( \mu \text{m} \). This is a result of the reduced cross-sectional area of the current flow defined by the skin depth in a metal conductor, which is lower for the higher conductivity materials and and higher for the lower conductivity metallisations. In order to avoid excessive ohmic losses, metal thickness must be in the range of three to five times the skin depth. Excessively thick conductors will only decrease accuracy of the line width definition.

Another issue is the microstrip line width. For higher mm-wave frequencies, the current density in metal strip is the highest in the lower corners of a strip cross-section. As a result, microstrip line ohmic losses are only slightly dependent on the strip width (see Table 3.3). The factors becoming important are the strip edge profile and quality of the edge definition. A desirable edge profile without acute angles can be seen in Fig. 3.2, where SEM photos of the copper conductors in the developed MCM-D technologies are shown. The last factor, influencing the ohmic losses, is the metallisation surface roughness. At millimetre-wave frequencies, where the skin depth, \( \delta \), in a metal conductor is very low (\( \delta = 0.22 \, \mu\text{m} \) for Cu and 0.25 \( \mu\text{m} \) for Au at 80 GHz), it is a critical parameter for the ohmic loss minimisation. If its root-mean-square (RMS) value, \( R_q \), gets close to or exceeds the skin depth, the line
3.1. A modified MCM-D technology for single substrate integration

Figure 3.2: SEM pictures of (a) sputtered/etched and (b) electroplated copper conductors for the developed MCM-D technology (courtesy of Acreo).

Figure 3.3: AFM measurements of the BCB roughness before and after RIE (the two measured profiles are superimposed in the left figure). (Courtesy of Acreo)

Ohmic loss ($\alpha_c'$) can even be doubled [166] due to the considerable increase in the current flow path:

$$\alpha_c' = \alpha_c \cdot c_{R_q}$$  (3.1)
The metallisation roughness is determined by the roughness of the underlying dielectric layer and the quality of the deposition and patterning processes. The spin-coated BCB shows almost mirror-like roughness (see Fig. 3.3). Two metal deposition and patterning options are used for the MCM-D technology set-up: sputtering with subsequent wet etching and electroplating inside a resist mask with initial seed layer deposition. Electroplating shows faster deposition rate than sputtering and is therefore preferred for thicker layers. The drawbacks are lower within-wafer homogeneity and higher surface roughness as compared to the sputtered metals (see Fig. 3.2).

Additionally, the thickness and magnetic properties of the intermediate metallisation layers in a complex metal layer build-up (in our case Ti, TiW and NiCr), in relation to the frequency of interest, have to be investigated because they can also contribute to line ohmic loss.

**Metal pattern and dielectric thickness dimensional control**

We limit our considerations on the required processing accuracy to patch antennas and antenna arrays at 60–80 GHz only because a precise and repeatable antenna resonant frequency location and its input match are the most demanding factors in view of the technological requirements. This issue is of considerable importance because of the inherent narrow bandwidth of single microstrip patch antennas and even more important for the series-fed arrays. For the latter, an input match is very sensitive to the phase errors along the line connecting the patch elements in a row. For long arrays, even a small error can prohibit the proper match in the desired frequency range. The main sources of phase errors along the line and of resonant frequency detuning are: inadequate dielectric constant value and process tolerances for the dielectric thickness and metallisation lithography. The main process tolerances of our MCM-D technologies are 0.6 µm per layer for a dielectric spin-coating and 1 µm for an edge metallisation definition (see Sec. 3.2). The corresponding changes of a single patch resonant frequency are: 70 and 130 MHz, respectively.

Taking the above-mentioned factors into account, it can be stated that the MCM-D technology with its repeatability and accuracy meets the high technological requirements needed for precise antennas and any other narrow-band elements at 60–80 GHz. None of the screen-printed co-fired ceramic (LTCC) or advanced high-density printed laminate-based technologies seems
3.2. Technology setup

to support the solution. Additionally, as the dielectric and metallisation surface roughnesses for these technologies are in the range of or even exceed the skin depth at 60–80 GHz in normally used conductors, considerable thicker substrates are needed to achieve the same antenna efficiency and line loss. The thicker substrates will, in turn, substantially deteriorate the performance of transmission line discontinuities and distributed passives (see Sec. 3.1.2).

As the requirements on the metal pattern dimensional control for the precise realisation of narrowband elements are very stringent, a complex and thick metal layer build-up has to be avoided. For this reason, a copper-nickel-gold (Cu/Ni/Au) set-up, usually applied on a top metal layer in hybrid technologies, cannot be used for the entire module surface. It could result in an undercut (over-etching) problem, thus, implying substantial difficulties in dimensional control of a metallisation pattern. It should only be applied to local areas such as contact or bonding pads, where its use is necessary.

Eventually, only simple gold or copper conductors for the two different developed MCM-D processes were used on the top metal layer. For the option with a copper conductor, an additional 5 μm thick BCB was applied as a passivation layer to avoid copper oxidation.

3.2. Technology setup

There is a practical limit how thick a single BCB layer and how thick a BCB layer stack can be manufactured. The problem here is mainly that the coefficients of thermal expansion (CTE) of different materials used in the build-up differ considerably and, thus, non-negligible mechanical tensions develop in the temperature range of 20–250°C, used during different processing phases. A final BCB stack-up consisting of 3 layers, 15 μm each, was fixed, corresponding to the optimum thickness range, defined in Sec. 3.1.2, maximising the performance of a general mm-wave module at 60–100 GHz.

Two technology set-ups, supposed to work with interconnects in the microstrip configuration, were investigated:

1. **Configuration I** - 1 mm thick aluminium substrate carrier, 3 x 15 μm BCB, electroplated NiCr/Au (80 nm / 3 μm) as top metallisation, electroplated TiW/Cu (80 nm / 3 μm) for internal layers (see Fig. 3.4).

2. **Configuration II** - 625 μm thick low resistivity silicon substrate carrier, 3 x 15 μm BCB and 5 μm BCB passivation, sputtered Ti/Cu (70 nm / 1 μm) for all metal layers.

As the microstrip structures are based only on the BCB dielectric, choice of the main substrate carrier plays no role from the electrical performance point
of view because the carrier and the thin-film layers are separated by a buried ground plane (see Fig. 3.4).

The main advantage of silicon wafers is their compatibility with the thin-film process, since standard processing equipment can readily handle these. Furthermore, low-resistivity silicon wafers are inexpensive and have very high surface quality, meaning that no planarisation layer is required to provide the necessary level of ground plane smoothness. Aluminium substrate shows very good thermal and electrical conductivity, which is of importance for power applications. Its good mechanical properties are well suited to assembly the structure on the equipment.

The smallest allowed via diameter of 60 μm was necessary to result in the appropriate via-yield (see Fig. 3.5). As a result of the chosen technology setup, stacked grounding vias for microstrip lines are impossible, only the staircased-like with a minimal via spacing of 15–20 μm. Straight vertical vias with a higher height/width ratio could be created by laser ablation or anisotropic etching but with additional cost. A very high degree of planarisation (DOP [167]) above 90% could be achieved for the BCB layers due to a high ratio of dielectric height to metal strip thickness.

For realisation of integrated decoupling and polarisation capacitors, $Ta_2O_5$ has been chosen (see Fig. 3.4) for its high dielectric constant ($\epsilon_r = 20$). A uniform 600 nm layer of this dielectric is deposited between two conductive layers (electrodes) by RF cathodic sputtering, resulting in a capacitance value of about 300 $pF/mm^2$.

The NiCr (38 Ω/square) and Ti (17 Ω/square) layers are deposited on the entire surface to avoid additional processing steps for definition of resistors. They are created by local conductor patterning only. As a result, every trans-
3.2. Technology setup

mission line on the top layer possesses NiCr or Ti materials under main conductor. The layer thicknesses of 80 nm and 70 nm for NiCr and Ti materials result in a typical in-panel variation of 0.5 Ω/square. As these layers do not show magnetic properties and can still be considered as thin at the frequency range of interest, their influence on the line loss even at 80 GHz can be neglected (see Sec. 3.4.1). The realisation of resistors on the top metal layer allows via-less connection with transmission lines which is of importance at mm-wave frequencies.

Chip bare dies could be placed in cavities created in the BCB only or also in the carrier, similarly as presented in [38, 39], shortening connections to the substrate interconnects.

Table 3.5: Parameter description of the developed thin-film technologies. The variations are specified as ± 3σ deviations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>low-profile thin-film</th>
<th>Configuration I</th>
<th>Configuration II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal thickness (t) [µm]</td>
<td>4.0 ± 0.5</td>
<td>3.0 ± 0.5</td>
<td>1 ± 0.15</td>
</tr>
<tr>
<td>Line width accuracy (w) [µm]</td>
<td>±2</td>
<td>±1.5</td>
<td>±1.0</td>
</tr>
<tr>
<td>Metal conductivity (σ) [S/m]</td>
<td>5.84×10^7 ± 0.04</td>
<td>4.53×10^7 ± 0.02</td>
<td>5.88×10^7 ± 0.00</td>
</tr>
<tr>
<td>BCB thickness/layer (h) [µm]</td>
<td>6.5±0.5</td>
<td>15.0 ± 0.8</td>
<td>15.0 ± 0.6</td>
</tr>
<tr>
<td>BCB permittivity (εr) [1]</td>
<td>2.64 ± 0.015</td>
<td>2.64 ± 0.015</td>
<td>2.64 ± 0.015</td>
</tr>
<tr>
<td>Sheet resistance (Rsheet) [Ω/sq.]</td>
<td>n/a</td>
<td>38.0 ± 2.5</td>
<td>17.0 ± 2.0</td>
</tr>
<tr>
<td>Res. width accuracy (w) [µm]</td>
<td>n/a</td>
<td>±1.5</td>
<td>±1.0</td>
</tr>
</tbody>
</table>

1) parameter uncertainties represented as variations

In order to measure process variations and to investigate the sensitivity of integrated passives performance to these variations, a set of test vehicles for technology characterisation (TCTV) was developed (see Fig. 3.6) [168]. Table 3.5 summarises the measured basic technology parameters with the corresponding ±3σ deviations. The parameters of the low-profile thin-film

Figure 3.5: Metallised vias in: (a) technology configuration I - 70µm in diameter (b) technology configuration II - 60µm in diameter.
**Table 3.6:** Variations of the microstrip characteristics as a result of the ±3σ technology parameter deviations from Table 3.5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>low-profile thin-film</th>
<th>Configuration I</th>
<th>Configuration II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Characteristic impedance [Ω]</td>
<td>$Z_0 = 50 \pm 5.3$</td>
<td>$Z_0 = 50 \pm 2.9$</td>
<td>$Z_0 = 50 \pm 2.2$</td>
</tr>
<tr>
<td>Resonance frequency [GHz]</td>
<td>$f_{res} = 77 \pm 0.60$</td>
<td>$f_{res} = 77 \pm 0.34$</td>
<td>$f_{res} = 77 \pm 0.26$</td>
</tr>
</tbody>
</table>

**Figure 3.6:** A 22 mm × 22 mm TCTV for the technology configuration I.

build-up from the previous EU LAP project [144–146], representing a typical MCM-D technology, are included as a reference. Table 3.6 presents the statistical variations of the microstrip characteristic impedance and resonance frequency for a 50 Ω microstrip line section as a result of the ±3σ technology parameter deviations from Table 3.5. The results of a more detailed analysis show that the characteristic impedance value is mainly affected by dielectric thickness variations within the supported technological parameters values. However, the location of the resonance frequency at 77 GHz strongly depends on the exact permittivity value. About 1/3 of its variation is due to the permittivity uncertainty even within a very narrow ±3σ deviation range of 2.64±0.015 (see Table 3.5), underlining the importance of an accurate in-house material characterisation.

### 3.3. Simulation and measurement techniques

The simulations were performed using a variety of full-wave solvers: HFSS, ENSEMBLE, Sonnet and LINMIC Interconnect. The measurements were performed using a 2-port HP8510XF VNA with 150 μm pitch wafer probes.
3.4. Examples of integrated passives

The system was calibrated with TRL and LRRM standards on the alumina calibration substrate from Cascade Microtech. After this initial off-wafer calibration, the second on-wafer calibration step was performed using the techniques developed in Secs. 5.2 and 5.5) [4, 96, 98–100, 110, 111]. All multiport structures were characterised by measuring between two ports while the unused ports were terminated by the on-wafer loads. For this purpose, different numbers of the same realisations with differently terminated ports were measured, depending on element symmetries (see Sec. 5.6) [169–171]. The reference geometry of the load was laid separately in close proximity of the measured structures. The influence of this non-ideal load was subsequently removed using the appropriate matrix transformation (see Sec. 5.6). Precision of such a de-embedding procedure is limited by the process-defined dimensional repeatability of the load, feed structures and elements being measured, probe contact quality, its repeatability and positioning accuracy.

The elements at 60 GHz, presented in the next sections, are realised in technology configuration I, whereas those at 80 GHz in configuration II.

3.4. Examples of integrated passives

3.4.1. Transmission lines and discontinuities

The de-embedded line loss for a 50 Ω microstrip line realised in both developed technology options (see Sec. 3.2 or Fig. 3.7 for the build-up definition) is shown in Fig. 3.7. A very small insertion loss of 0.074 dB/mm and 0.08 dB/mm at 60 GHz for both realisations can be noted, being very close to the simulated (see Table 3.3) due to almost mirror-like BCB surface. The small differences between the simulated and measured values are due to the influence of thin NiCr and Ti layers under Au and Cu conductors, not taken into account in the simulations. Fig. 3.8 shows the de-embedded line loss and line effective permittivity for a set of 30-300 μm wide microstrip lines in the technology configuration I. As stated in Sec. 3.1.2, the line loss is weakly dependent on the line width, excluding very narrow lines (w < 40μm). The lines practically show no high-frequency dispersion in the measured frequency range of 1–100 GHz as a result of the low BCB dielectric constant and its appropriately chosen thickness. The ultra-low loss and low dispersion characteristics of the presented microstrip lines are only comparable to those realised using more expensive micromachining techniques, where the dielectric substrate is removed [40, 142, 172].
Open-ends

The de-embedded equivalent line extension values for a set of the open-ended 25–100 Ω microstrip lines (28–300 μm line width) in both technology options (configuration I and configuration II) are within 25–31 μm and show no frequency dependence in the entire measured frequency range of 1–100 GHz because of negligible surface-wave effects due to the low BCB dielectric permittivity and its appropriate thickness. These values constitute 1.1-1.6% of the wavelength at 100 GHz and can still be considered as a design parameter of secondary importance. The measured and simulated values (HFSS and ENSEMBLE) do not differ by more than 10%. The return loss of these open-ends, simulated with HFSS, is within 0.035–0.07 dB at 100 GHz, which is equivalent to 0.8–1.5% power loss (1% for a 50 Ω line) and is in a good agreement with the measured values. However, it should be noted that the full-wave simulations deliver more precise values of the power lost on the open-ended structures because of the amplitude noise in the measured reflection coefficients, normally considerably higher than that for the transmitted signals. The losses are associated with space waves only and the influence of surface waves can be neglected. This is different from the open-circuits on a 100 μm thick GaAs substrate, where about 35% of the lost power at 100 GHz is due to surface waves [173].

The behaviour of the open-ended 50 Ω microstrip lines on a 100 μm thick
3.4. Examples of integrated passives

Figure 3.8: De-embedded: (a) line effective permittivity and (b) line loss for a variety of microstrip lines realised in technology configuration I (see Fig. 3.7 for the technology build-up definition) (w denotes a microstrip width).

GaAs (w = 70 µm) and on a 100 µm thick hypothetical BCB substrate (w = 260 µm) was also simulated (HFSS and Ensemble) and compared to that in the developed technology build-up (see Table 3.7). It can be noticed that the line extension and power loss values for both simulated build-ups are substantially higher than those for the proposed 45 µm thick BCB build-up.

Short-end

One of the main drawbacks of using the microstrip configuration at mm-wave frequencies can be a high end inductance of the grounding path associated
Table 3.7: Comparison of the open-ended $50 \, \Omega$ microstrip lines on the developed $45 \, \mu m$ thick and a $100 \, \mu m$ thick hypothetical BCB dielectrics, and on a $100 \, \mu m$ thick GaAs substrate.

<table>
<thead>
<tr>
<th>Open-end configuration</th>
<th>Line extension at 100 GHz in $\mu m$ and in % of the wavelength</th>
<th>Power loss at 100 GHz in % of the input power</th>
</tr>
</thead>
<tbody>
<tr>
<td>114 $\mu m$ wide line on a $45 , \mu m$ BCB</td>
<td>$28 , \mu m$ (1.35%)</td>
<td>1%</td>
</tr>
<tr>
<td>260 $\mu m$ wide line on a $100 , \mu m$ BCB</td>
<td>$68 , \mu m$ (3.5%)</td>
<td>5.5%</td>
</tr>
<tr>
<td>70 $\mu m$ wide line on a $100 , \mu m$ GaAs</td>
<td>$38 , \mu m$ (3.8%)</td>
<td>2.3%</td>
</tr>
</tbody>
</table>

with shorting vias.

A geometry of the designed grounding path is the same as that used in case of the compensated loads (see Sec. 3.4.2) and can be seen in Fig. 3.13(a). As only a staircased via geometry is allowed, the terminating path was divided in two, using 3 vias per shorting branch, to minimise its inductance. A via diameter of 70 $\mu m$ and a space between vias of 30 $\mu m$ were used. The de-embedded end inductance values cover the range of 5–9 pH at the low frequency end and 8–12 pH at 100 GHz for the 100–50 $\Omega$ grounded transmission lines. Their equivalent line extension values are within 10–32 $\mu m$ at low frequencies and increase to 15–45 $\mu m$ at 100 GHz. They constitute 0.7–2.2% of the wavelength at 100 GHz and their influence on the circuit design is still one order of magnitude less than that of the line parameters. It can be noticed that the short-ends of the high impedance lines can be the better choice in terms of the line extension value than the open circuits (see Table 3.7), even if shorted using long grounding paths. A frequency dispersion of the end inductances comes from the 3D current distribution at the line-short-circuit interface and from the frequency increasing via inductance (towards a quarter-wavelength resonance for a via shorted to ground on one end). For precise circuit design purposes, this dispersion can be assumed a linear function of frequency because the reported line extensions still constitute a small fraction of the wavelength even at 100 GHz.

The HFSS simulated end inductance for a $50 \, \Omega$ line grounded using a 70 $\mu m$ stacked via (the same diameter as for the designed short-circuit) constitutes 75% of the value for the designed staircased grounding path.

The HFSS simulation results of the implemented grounding paths for the 50–100 $\Omega$ lines show a return loss of about 0.035 dB (0.8% power loss) at 100 GHz. The measured return loss is in this range but it cannot be used for precise reading due to the calibration noise of 0.03–0.05 dB at 100 GHz in the measured reflection coefficients.
3.4. Examples of integrated passives

**Via chain**

The layout and the measured S-parameters of a via chain between 50 Ω lines located on the top and intermediate (15 μm below) metal layers are shown in Fig. 3.9. The chain consists of 4 vias, 3 and 2 transmission line sections on the top and intermediate layers, respectively. The measured return loss is better than 26 dB up to 100 GHz, indicating that the excessive shunt capacitance to ground (the main parasitic effect of every via transition) is still acceptably small as compared to that of the regular 50 Ω transmission lines on the top and intermediate layers. The insertion losses of the measured chain and of

![Image of via chain layout and S-parameters](image)

**Figure 3.9:** Via chain between 50 Ω microstrip lines located on the top and intermediate (15 μm below) metal layers: (a) layout geometry (b) measured S-parameters. (Every microstrip line section is 200 μm long. The line widths are 114 μm and 72 μm for the top and intermediate layers, respectively. The vias are 60 μm in diameter and are surrounded by an additional 10 μm metallisation at each side for misalignment, according to the standard layout design rules for our technology set. ‘S_{21}-1.34 mm line’ denotes the measured insertion loss of an equivalent 1.34 mm long line consisting of 770 μm and 570 μm long line sections on the top and intermediate metal layers, respectively.)
the equivalent 1.34 mm long line length (770 μm and 570 μm on the top and intermediate metal layers, respectively) differ only by 0.03 dB at 100 GHz, indicating very low additional power lost at every via transition.

**Bends**

The parasitics associated with bends define the behaviour of meander lines which are often used as delay, slow-wave lines or for the phasing of radiating elements in antenna arrays. Successful design of such structures at mm-wave frequencies requires very small reactances and radiation at bend discontinuities, and low electromagnetic coupling between meander line sections.

Different bend geometries for the 28–200 μm wide lines (100–35 Ω) were characterised. In order to minimise the influence of the calibration noise at high mm-wave frequencies on the measured bend characteristics, some number of bends and transmission line sections were cascaded, resulting in meander line structures.

The measured performance of a 50 Ω right angle meander line (Fig. 3.10) consisting of 8 chamfered bends and 9 transmission line sections is presented in Fig. 3.11. A 500 μm separation between the parallel line sections was chosen so that the influence of bend parasitics is cumulative at about 80–90 GHz. For comparison purposes, the ENSEMBLE simulated performance of a similar 50 Ω (250 μm wide) meander line on a hypothetical 100 μm thick BCB substrate is also included. The mean path lengths, including bends, are 5.15 mm and 5.9 mm for both structures, respectively. The worst measured return loss of the meander line on a 45 μm thick BCB is equal to 26 dB at 95 GHz. Moreover, it is better than 35 dB up to 75 GHz, being comparable to the measured return loss of the equivalent 5.15 mm long straight transmission line. The power lossess along the meander and the equivalent transmission line

![Figure 3.10: Layout of the measured 50 Ω (114 μm wide) meander line. (Every line section is 500 μm long, resulting in an overall mean path length of 5.15 mm, including chamfered bends. A 50% meter was used to decrease the excess capacitance at the bends and to lower the radiation loss at higher frequencies.)](image-url)
3.4. Examples of integrated passives

Figure 3.11: Performance comparison of the 50 Ω meander lines on a 45 μm and on a 100 μm thick BCB substrate: (a) return and insertion losses (b) power lost along the meander lines. ('bend-chain (45 μm BCB)-meas' and 'bend-chain (100 μm BCB)-sim' denote the measured and ENSEMBLE simulated characteristics of the meander lines on a 45 μm and on a 100 μm thick BCB, respectively, whereas 'ustrip 5.15 mm (45 μm BCB)-meas' and 'ustrip 5.9 mm (100 μm BCB)-sim' the measured and simulated characteristics of the equivalent transmission line sections of the same length as the corresponding meander structures).

are practically equal up to 75 GHz and differ only by 3% at 100 GHz. For a 100 μm thick BCB substrate, the transmission through the meander line and its return loss beyond 60 GHz deteriorate rapidly. The return loss approaches 15 dB at 85 GHz and 37% of the total input power is lost at 100 GHz, while only 10% is dissipated on the equivalent 5.9 mm long straight transmission line.
T- and X-junctions

T- and X-junctions composed of different line widths within 28–114 μm (100–50 Ω) were characterised. S-parameters of the junctions were determined using the technique from Sec. 5.6.1 ([174]) for the characterisation of reciprocal 3- and 4-ports. The orthogonal ports were subsequently terminated by the on-wafer short, open and load. Finally, the S-parameters were obtained from the in-line measurements and measured characteristics of the terminations.

Due to its asymmetric structure, a simple T-junction can give rise to considerable phase and amplitude imbalance between its orthogonal branches. For all considered junction geometries, this phase imbalance is kept below 0.5 – 3° up to 100 GHz, very close to the ideal value of zero. Similarly, the phase deviations of the reflection coefficients from the ideal +/− 180° stay within 3°. Furthermore, the absolute values of the phase shifts of the transmission coefficients are kept below 1 – 4° at 100 GHz, very close to the zero degree phase shift for an ideal T-junction. 1

The junctions composed of the widest considered 50 Ω (114 μm) main transmission line and an equal width or a narrower orthogonal line show very low phase imbalance, not exceeding 0.5° at 100 GHz. However, the high frequency deviation of the power division between orthogonal branches is more pronounced. The highest amplitude imbalance of 0.25 dB and 0.8dB at 100 GHz for the transmitted and reflected signals on the orthogonal ports, respectively, is measured for the largest considered 50-50-50 Ω junction. The wide orthogonal lines connected to the narrow main lines, contrary to the previous ones, show frequency-stable amplitude response but lower phase balance. A good example is the measured 50-100-100 Ω junction with an extremely flat power division up to 100 GHz. A further improvement in the frequency stability of the power division coefficients can be achieved by simple chamfering of the outer edge of the junction. The ENSEMBLE simulations of the mentioned 50-50-50 Ω junction show that this technique can reduce the amplitude imbalance from 0.25 dB and 0.8dB down to 0.06dB and 0.2 dB at 100 GHz for the transmission and reflection coefficients, respectively. A similar procedure applied to a 50-100-100 Ω junction results in an improved (by 3 dB) input return loss of 29 dB at 100 GHz for the 50 Ω port.

The ENSEMBLE simulated loss of the considered right angle T-junctions stay within 1.2–1.6% at 100 GHz, depending on the line widths being connected. The corresponding values de-embedded from the measurements stay

---

1Defining the phase shifts, the reference plane located directly at the crossing point of the three lines is assumed.
in good agreement with the simulated ones but they are less accurate because of the measurement noise.

The characterised X-junctions show a slightly lower radiation loss because none of the port currents terminate at the strip edge. The amplitude imbalance is also slightly better due to the higher level of symmetry. For the largest characterised 50-50-50-50 Ω junction, the amplitude imbalance between transmitted signals on orthogonal ports is equal to 0.17 dB at 100 GHz.

3.4.2. Series resistors and compensated loads

Series resistor

The series resistors are located on the top metallisation layer and do not include any via transitions with the connecting transmission lines (see Sec. 3.2). As a result, they can be modelled by a simple RLC transmission line model, wherein $R$, $L$, $C$ represent the series resistance, inductance and capacitance per unit length, respectively. Shunt conductance to ground $G$ was omitted as the dielectric loss associated with BCB is low in comparison to the ohmic loss of the resistive layer. $R$ was verified (using the developed de-embedding techniques from Secs. 5.2 and 5.5) to be constant up to 100 GHz due to the negligible skin effect in the very thin, high-resistivity Ti and NiCr layers. If the resistor and the feed transmission line differ in width, the influence of an additional step-in-width discontinuity should also be considered. For typical resistor widths of 30–120 μm connected to a 50 Ω (114 μm wide) microstrip line, the largest parasitic capacitance and inductance values of 1.5 fF and 1.2 pH, modelling the behaviour of a step-in-width discontinuity, were extracted from the HFSS simulations. Their influence on the frequency-dependent characteristics of the series resistors can be neglected in the entire frequency range of 1–100 GHz. The lower resistor width of 30 μm is a result of the etching accuracy and the upper one is limited by transmission line effects for the typical resistance value required at mm-wave frequencies.

For the considered 30–120 μm wide resistors that are shorter than 250 μm (equivalent to an electrical length of 45° at 100 GHz), their de-embedded transmission and reflection amplitude characteristics are very flat up to 100 GHz. As a result, the maximum resistance values of 80–320 Ω and 38–152 Ω with the frequency stable amplitude responses can be realised for NiCr and Ti resistive layers, respectively. These values correspond to $-5 - -12$ dB and $-2.7 - -7.5$ dB attenuations if the resistors are embedded in a 50 Ω transmission line environment. Their measured amplitude characteristics show a maximum decrease of only 0.1–0.2 dB at 100 GHz.

ENSEMBLE simulations show that performance of the same resistor ge-
ometries deposited on a 100 μm thick GaAs is considerably degraded due to the more pronounced transmission line effects related to the high GaAs dielectric constant. A 38 Ω (114/114 μm) NiCr series resistor, connected to a 50 Ω microstrip line, shows an increase in its insertion loss from 3.2 dB up to 3.65 dB at 100 GHz, whereas that on a 45 μm BCB practically does not show any noticeable frequency dependence. Concluding, the low BCB dielectric constant allows to use considerably larger resistor geometries for higher power dissipation, assuming the same resistance value and similar transmission line effects.

Compensated loads

In [141], it was shown that both the load with the used staircased grounding path, shown in Fig. 3.13(a) (see also Sec. 3.4.1 for its detailed description), and the one with a single stacked via need compensation for better return loss in the frequency range of interest. The influence of the resistor dimensions on the input match of an uncompensated 50 Ω load was also studied. Some results of this study are depicted in Fig. 3.12. It can be noticed that the matching of the longer and wider load (158/120 μm) is only a bit worse (1 dB at 80 GHz) than the one of its smaller counterpart (79/60 μm) because the same grounding path inductance is transformed to the input through more capacitive length of the wider resistor. Furthermore, both geometries show a return loss worse than 20 dB beyond 50 GHz and require compensation for the 60–80 GHz applications.

The measured return loss of the 50 Ω and 70 Ω compensated loads used as terminations for the multi-port elements at 50–60 GHz is shown in Fig. 3.13(b). Similar loads were designed for the 80 GHz elements. A full-wave 3D FEM solver (HFSS) was used in the design process because of a 3D nature of the structures. The inductive influence of a grounding path is compensated by adding simple open stubs in the front and shortening the resistor length. The 38 Ω and 61 Ω DC resistance values for the 50 Ω and 70 Ω loads, respectively, were used. As a result of the sheet resistance tolerances, the measured loads are not perfectly matched at 60 GHz but still at very good level (see also Fig. 3.12 for the tolerance analysis results). The 70 Ω termination is better matched at low frequencies than the 50 Ω because a smaller reduction of the resistor length (related to its nominal DC resistance value) was needed for compensation purposes.
3.4. Examples of integrated passives

Figure 3.12: HFSS simulated return loss of two different uncompensated 50 Ω loads and the compensated from Fig. 3.13(a), including a 20% sheet resistance tolerance (‘50 Ohm 158/120 μm’ and ‘50 Ohm 79/60 μm’ denote a return loss of the 158/120 μm and 79/60 μm large uncompensated loads, whereas ‘Comp 50 Ohm’, ‘Comp 50 Ohm + 10 Ohm’ and ‘Comp 50 Ohm - 10 Ohm’ an input match of the compensated load with pm 20% sheet resistance tolerances).

Figure 3.13: The 50 Ω and 70 Ω compensated loads: (a) geometry of the 50 Ω termination (b) measured return loss (The length, $R_L$, and the width, $R_W$, of the intrinsic resistor are 121/120 μm and 100/62 μm for the 50 Ω and 70 Ω loads, whereas the length, $S_L$, and the width, $S_W$, of the front stub are 69/110 μm and 60/61 μm, respectively).

Ultra wideband load

An alternative ultra wideband 50 Ω termination, using a topology similar to that reported in [24] for multi-layer BCB/Kapton organic MCMs, was also
designed. The goal was to achieve the best input match for the 70-110 GHz band. The geometry of this load is shown in Fig. 3.14(a). The first resistor, R1, is connected to ground using the same staircased shorting path as for the previous compensated loads. Its DC resistance is 59 Ω and it presents considerably inductive behaviour at very high frequencies. Its input impedance is equal to 71 + j30 Ω and 100 + j53 Ω at 100 GHz and 160 GHz, respectively. The second resistor, R2, together with a line section located behind creates a tuning open stub and it is connected in parallel with R1.

![Diagram of load](image)

**Figure 3.14:** An ultra wideband 50 Ω load: (a) geometry (b) simulated input impedance ('Sim. Z11') and return loss ('Sim. S11'), including a 10% sheet resistance tolerance. (The length, r11, and the width, rw1, of the main resistor are 125 μm and 80 μm, respectively. Whereas, r12 and rw2 of the open-ended resistor are 250 μm and 60 μm. For the stub, the respective dimensions are 65 μm (sw1) and 85 μm (sl1)).

The HFSS simulation results of the return loss and input impedance of this compensated load are shown in Fig. 3.14(b). A constant and frequency independent value of the NiCr sheet resistance was assumed in the simulations (verified by measurements up to 100 GHz). The load’s return loss can be kept better than 22 dB up to 160 GHz for a nominal value of the sheet resistance. For a 10% tolerance, the return loss still stays below 20 dB for the most part of the considered band. Very stable real (50–60 Ω) and imaginary (-5 +2 Ω) parts of the input impedance, and the fact that the imaginary part crosses zero value axis for the two frequency points, 100 GHz and 160 GHz, are responsible for this broad-band behaviour.

The standard tuning element, consisting of the electrically small R2 and the open stub behind it, can compensate for the inductive behaviour of the
main resistor, R1, at a single frequency only. At lower frequencies, the real part of the input impedance for such a topology is almost equal to the DC resistance value of R2 and the imaginary part is defined by the capacitive behaviour of the open-ended stub. However, the behaviour of this structure is considerably different if the resistor surface constitutes most of the stub length. First, the real part of the input impedance can be substantially lower than DC resistance of R2 even at lower frequencies. Our resistor, R2, shows a DC resistance of 158 Ω, whereas the input impedance of the entire stub is equal to 86 − j6586 Ω at 1 GHz. In general, its input impedance at lower frequencies depends on the percentage coverage of a stub length with a resistive surface. The second property of this configuration, unlike in a standard connection of a short resistor with a long stub, is the avoidance of a quarter wavelength resonance due to the transmission properties of a long resistor. A standard open-ended stub, equally long as that used in the designed compensated load but totally covered with a copper conductor, should resonate at about 150 GHz. For the implemented stub, 75% (250 μm) of its length is covered with the resistive NiCr layer which causes that its input impedance stays very capacitive at 150 GHz and well above. The advantage of this property for the compensation of an inductive behaviour of R1 at very high frequencies was taken into account in the design process. The simulated input impedance of the used stub is equal to 84 − j54 Ω and 96 − j32 Ω at 100 GHz and 160 GHz, respectively. These values combined with (parallel connection) the above-mentioned input impedance of the uncompensated load, R2, result in a zero input reactance value at both frequencies.

The proposed compensated load topology proves that the design of ultra wideband terminations at high mm-wave frequencies is possible even with dimensionally large resistors and grounding paths.

**3.4.3. Low-pass filters at 65 GHz and 79 GHz**

For demonstration purposes, the performance of two stepped-impedance low-pass filter realisations with cut-off frequencies at 65 GHz and 79 GHz are presented. 9th-order Chebyshev prototypes with 0.04 dB and 0.5 dB passband ripples, and return losses better than 20 dB and 9.6 dB were used for both structures, respectively. The minimum line width, determining maximal feasible line impedance, was chosen to be 20 μm to assure highly repeatable geometry in the mass production. The line widths and their corresponding impedances for high and low impedance filter sections are given in Fig. 3.15. The total filter lengths are 2565 μm and 2306 μm, respectively.

The layout of the 65 GHz realisation together with the simulated and mea-
Figure 3.15: Layout of the 9th-order Chebyshev low-pass filter with the cut-off frequency at 65 GHz (The line widths and their corresponding impedances for high and low impedance filter sections are $Z_h = 125 \Omega$ ($w = 20 \mu m$) and $Z_l = 20 \Omega$ ($w = 400 \mu m$). The total filter length is 2565 \mu m).

Figure 3.16: Insertion loss and return loss of the 9th-order Chebyshev low-pass filters with the cut-off frequencies at: (a) 65 GHz (b) 79 GHz. The former is realised in the technology configuration I and the latter in the technology configuration II (see Sec. 3.2 for the build-up definition). ('$s11meas$' and '$s11sim$' denote the measured insertion and return loss, whereas '$s21meas$' and '$s21sim$' the simulated using ENSEMBLE with a 3D metal conductor geometry).

Measured frequency response for both filters is shown in Fig. 3.15 and Fig. 3.16. Note the very good correspondence between simulated and measured results. To achieve this, the inclusion of a 3D metal geometry in the ENSEMBLE simulations was necessary, especially for a 3 \mu m thick gold metallisation used in the 65 GHz filter. The reason is that very narrow microstrip lines change their impedance value considerably with metallisation thickness. The maximum pass-band insertion losses are 0.8 dB and 1 dB for the 65 GHz and 79 GHz structures, respectively. Both filters preserve the return loss of their prototypes very well and show sharp rejection-band edge. The 35 dB out-of-band attenuations fall at 85 GHz and 100 GHz.
Some discrepancy in the location of a cut-off frequency for the 79 GHz filter between the simulation and measurement results can be observed because of the Ni/Au deposition non-uniformities within the open contact pads (in the BCB passivation layer) observed for some structures realised in the technology configuration II (see Sec. 3.2 for the the build-up definition). As a result, it lowers the needed very high repeatability of the probe contact and, thus, of the extracted at the calibration stage feed error boxes (see Sec. 3.3). The very high frequency involved considerably affects the quality of this process because of an increased influence of the parasitics associated with the probe-tip feed discontinuities.

Table 3.8: Performance of different realised stepped-impedance low-pass filters.

<table>
<thead>
<tr>
<th>Filter prototype</th>
<th>Cut-off frequency</th>
<th>Max passband insertion loss</th>
<th>35 dB stop-band attenuation</th>
<th>Filter length</th>
</tr>
</thead>
<tbody>
<tr>
<td>$9^{th}$-order Chebyshev max 0.04 dB pass-band ripples max 20 dB return loss</td>
<td>65 GHz</td>
<td>0.8 dB</td>
<td>85 GHz</td>
<td>2565 µm</td>
</tr>
<tr>
<td>$9^{th}$-order Chebyshev max 0.5 dB pass-band ripples max 9.6 dB return loss</td>
<td>79 GHz</td>
<td>1 dB</td>
<td>100 GHz</td>
<td>2306 µm</td>
</tr>
<tr>
<td>$9^{th}$-order Chebyshev max 0.04 dB pass-band ripples max 20 dB return loss</td>
<td>78.5 GHz</td>
<td>1 dB</td>
<td>100 GHz</td>
<td>2100 µm</td>
</tr>
<tr>
<td>$9^{th}$-order Chebyshev max 0.5 dB pass-band ripples max 9.6 dB return loss</td>
<td>63 GHz</td>
<td>1 dB</td>
<td>81 GHz</td>
<td>3074 µm</td>
</tr>
<tr>
<td>$8^{th}$-order Bessel</td>
<td>55 GHz</td>
<td>0.5 dB</td>
<td>100 GHz</td>
<td>2173 µm</td>
</tr>
</tbody>
</table>

1) specified for 32 dB stop-band attenuation

The overall performance of some other realised low-pass filters together with the above analysed is gathered in Table 3.8. All of them preserve the maximum passband return loss given by the appropriate prototype. The same line widths for low and high impedance sections were used for all realisations.

A comparable performance has been reported in [41] for 94 GHz microshield line low-pass filters but using a more expensive micromachining process.

3.4.4 Band-pass filters at 59 GHz, 76 GHz and 94 GHz

The frequency response of the 3- and two 4-section coupled-line band-pass filters at 59.5 GHz and 75.9 GHz with $2^{nd}$- and $3^{rd}$-order Butterworth low-pass prototypes, respectively, are shown in Figs. 3.17(b) and 3.18. The layout of the 3-section filter is also depicted (Fig. 3.17(a)). The structures are
2560 μm, 3390 μm and 2560 μm long, respectively. The physical dimensions for every line section are summarised in Table 3.9.

Figure 3.17: The 3-section band-pass filter at 59 GHz: (a) layout (b) insertion loss and return loss (The total filter length is 2560 μm. The appropriate dimensions of the coupled-line sections are given in Table 3.9).

Figure 3.18: Insertion loss and return loss of the 4-section band-pass filters at: (a) 59 GHz (b) 76 GHz. The former is realised in the technology configuration I and the latter in the technology configuration II (see Sec. 3.2 for the build-up definition). ('s21mea' and 's11mea' denote the measured insertion and return loss, whereas 's21sim' and 's11sim' the simulated using ENSEMBLE with a 3D metal conductor geometry).
Table 3.9: Dimensions of the coupled-line sections for the 3- and 4-section band-pass filters at 59 GHz and 76 GHz.

<table>
<thead>
<tr>
<th>Number of a coupled-line section</th>
<th>@ 59 GHz 3-, 4-sec @ 76 GHz 4-sec</th>
<th>@ 59 GHz 3-, 4-sec @ 76 GHz 4-sec</th>
<th>@ 59 GHz 3-, 4-sec @ 76 GHz 4-sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>width [μm]</td>
<td>slot [μm]</td>
<td>length [μm]</td>
</tr>
<tr>
<td>1</td>
<td>70, 72, 64</td>
<td>24, 18, 20</td>
<td>860, 855, 645</td>
</tr>
<tr>
<td>2</td>
<td>105, 112, 112</td>
<td>80, 78, 90</td>
<td>840, 840, 635</td>
</tr>
<tr>
<td>3</td>
<td>70, 122, 112</td>
<td>24, 78, 90</td>
<td>860, 840, 635</td>
</tr>
<tr>
<td>4</td>
<td>—, 72, 64</td>
<td>—, 18, 20</td>
<td>—, 855, 645</td>
</tr>
</tbody>
</table>

The measured passband insertion loss is 2.75 dB and 3.35 dB for the 3- and 4-section filters at 59.6 GHz, and 3.2 dB for the 4-section filter at 75.9 GHz, respectively. Similarly, passband bandwidths are 3.45 GHz (5.7%), 3.8 GHz (6.4%) and 3.9 GHz (5.1%). A stopband attenuation of 40 dB is located at 45, 51 GHz and 77, 68 GHz for the two 59.6 GHz filters. The same attenuation value for the 75.5 GHz realisation falls at 65 GHz and 85 GHz. Excellent agreement between the full-wave ENSEMBLE simulation and the measurement results can be seen, excluding some small discrepancies in the 76 GHz realisation. It was necessary to include 3D metallisation geometry in the simulations to achieve this, specifically for the 59 GHz filter realised in the technology configuration I with a 3 μm thick metal strip (see Sec. 3.2 for the build-up definition). This is due to the sensitivity of mode impedances and phase velocities to a metal strip thickness, especially for odd modes on the coupled line sections with narrow slots (18,20 and 24 μm in Table 3.9). Similar passband insertion loss has been reported in [41] for 94 GHz shielded membrane microstrip (SMM) coupled-line band-pass filters but with noticeably weaker return loss and utilising a more expensive multiple-step micromachining process with a three-wafer assembly.

Band-pass filters at 94 GHz

The performance and geometry of the two 4-section coupled-line band-pass filters at 94 GHz with a 3\textsuperscript{rd}-order Chebyshev and Butterworth low-pass prototypes, respectively, are shown in Fig. 3.19 and Table 3.10. Simulations were performed with ENSEMBLE, assuming a 3 μm thick gold strip. (technology configuration I). Both filters possess low insertion loss of 4.2 dB and 2.6 dB and show very good input match within the passband frequency range.
Table 3.10: Dimensions of the coupled-line sections for the two 4-section band-pass filters at 94 GHz. (*B* stands for the filter bandwidth and is equal to 3.5% for the Chebyshev realisation and 6.6% for the Butterworth realisation).

<table>
<thead>
<tr>
<th>Number of a coupled-line section</th>
<th>( B = 3.5%, 6.6% )</th>
<th>( B = 3.5%, 6.6% )</th>
<th>( B = 3.5%, 6.6% )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( n )</td>
<td>width [( \mu )m]</td>
<td>slot [( \mu )m]</td>
<td>length [( \mu )m]</td>
</tr>
<tr>
<td>1</td>
<td>116, 72</td>
<td>16, 20</td>
<td>516, 538</td>
</tr>
<tr>
<td>2</td>
<td>116, 112</td>
<td>140, 80</td>
<td>516, 529</td>
</tr>
<tr>
<td>3</td>
<td>116, 122</td>
<td>140, 80</td>
<td>516, 529</td>
</tr>
<tr>
<td>4</td>
<td>116, 72</td>
<td>16, 20</td>
<td>516, 538</td>
</tr>
</tbody>
</table>

Figure 3.19: Simulated performance (ENSEMBLE) of the two 4-section band-pass filters at 94 GHz: (a) Chebyshev realisation with a 3.5% bandwidth (b) Butterworth realisation with a 6.6% bandwidth. (A 3 \( \mu \)m thick gold conductor for the microstrip was assumed in simulations, according to the configuration I technology build-up (see Sec. 3.2 for the build-up definition)).

3.4.5. Wilkinson power divider at 60 GHz and 94 GHz

The Wilkinson power divider from Fig. 3.20 shows an ultra low insertion loss of 0.2 dB at 60 GHz and better than 0.25 dB in the 28–72 GHz frequency range (excluding 3 dB power split), almost equal to the ENSEMBLE simulated values. A wideband return loss better than 20 dB in the 50–70 GHz and 35–70 GHz bands for the input and output branches, respectively, and an isolation of 20 dB within 50–70 GHz were obtained. Such a good performance is possible due to the very low BCB surface roughness, its low dielectric constant and optimally chosen thickness (see Sec. 3.1.2). Note that, due to the appropriately thin dielectric thickness, it was possible to lay both output
branches and both parallel quarter wavelength line sections in a short distance of 132 μm (equal the series resistor length) without losing a high isolation of the divider. At the same time any bend discontinuities along the path of the latter were avoided (see Fig. 3.20). From the performance point of view, it

**Figure 3.20:** Layout of the Wilkinson power divider at 60 GHz. (The length and width of the series NiCr resistor are 132 μm and 50 μm, respectively. The overall element dimensions are 1150 μm x 360 μm).

**Figure 3.21:** The Wilkinson power divider at 60 GHz: (a) return loss at the input and output ports (b) isolation and transmission (‘s11mea’, ‘s11sim’, ‘s22mea’ and ‘s22sim’ denote the measured and simulated (ENSEMBLE) match at the input and output ports, respectively. Whereas, ‘s21mea’, ‘s21sim’, ‘s23mea’ and ‘s23sim’ stand for the measured and simulated transmission and isolation between both output branches).
Figure 3.22: Simulated performance of the Wilkinson power divider at 94 GHz (‘$s_{11}$’, ‘$s_{22}$’, ‘$s_{23}$’ and ‘$s_{21}$’ denote the input and output match, isolation and transmission, respectively. A 3 μm thick gold metallisation was used in the ENSEMBLE simulations as a metal strip conductor, according to the configuration I technology build-up (see Sec. 3.2 for the build-up definition)).

was also important to locate a NiCr resistor layer on the top metallisation level, enabling via-less connection with the remaining structure.

Compared to the results of the Wilkinson power divider at 60 GHz presented in [25], realised in a multi-layer BCB/Kapton technology, a noticeably better performance was achieved, especially in isolation (30 dB vs. 15 dB). The insertion loss of the element integrated in the developed technology is comparable to that of the ultra low-loss Wilkinson power divider at 33 GHz (loss of 0.19 dB) reported in [143] and realised in a more expensive micromachined membrane-based microstrip line configuration.

**Wilkinson power divider at 94 GHz**

The Wilkinson power divider at 94 GHz is designed with a larger, 260/100 μm, series resistor, constituting a 13% of the wavelength at 94 GHz. Its use allows to minimise a frequency shift between the location of the minima in the input match and the isolation due to a wider separation between both parallel quarter wavelength line sections and between both output branches, thus, lowering the inter-circuit coupling. Additionally, some improvement in the input match at both ports is also achieved. The simulated performance (ENSEMBLE) of the divider is excellent. A 20 dB return loss for both input and output branches falls within 74–118 GHz and 31–114 GHz, respectively. A 20 dB isolation is within 78–110 GHz. The insertion loss at
94 GHz is 0.41 dB and better than 0.5 dB within 35–105 GHz. The divider takes an area of $0.35 \, mm^2$ ($795 \, \mu m \times 440 \, \mu m$).

3.4.6. Branch-line coupler at 60 GHz

The layout geometry of a branch-line coupler is shown in Fig. 3.23. It shows a very low insertion loss of 0.25 dB at 60 GHz (excluding 3 dB power split), an amplitude balance of 0.5 dB in the 55–70 GHz band and a phase balance of $89.25^\circ \pm 0.75^\circ$ for the 55–65 GHz band. Its 20 dB return loss and isolation fall within 55–61 GHz and 55.5–61 GHz, respectively. Their minima reach even 37 dB. Very good correspondence between simulations (ENSEMBLE) and measurements can be observed.

![Figure 3.23: The branch line coupler at 60 GHz: (a) layout (b) phase balance.](image)

Figure 3.23: The branch line coupler at 60 GHz: (a) layout (b) phase balance (The overall element dimensions are 1010 $\mu m \times 1160 \, \mu m$. 'mea' and 'sim' stand for the measured and ENSEMBLE simulated results).

3.4.7. Balun at 58 GHz

The presented balun at 58 GHz (Fig. 3.25(a)) is a multi-layer realisation of an open-ended topology with broadside-coupled lines, wherein the coupled lines are laid on the two uppermost metal layers. The input port is located on the top layer and the balanced ports on the lower. A complete balun structure also includes via transitions between the lower and the top metal layer at the two output ports. In order to obtain a 3 dB coupling level, we applied the broadside-coupled line sections because a single-layer realisation with
edge-coupled lines is impossible due to a technologically limited slot width of 20 μm.

The even-odd mode analysis for broadside-coupled line sections cannot be applied in the design procedure. Instead, normal mode parameters [175] must be found for the two characteristic modes, \( c \) and \( \pi \), of general asymmetric, inhomogeneous, uniformly coupled line sections. These parameters are effective permittivities (\( \varepsilon_c \) and \( \varepsilon_\pi \)), voltage ratios between the upper and the lower conductor (\( R_c \) and \( R_\pi \)), and line characteristic impedances (\( Z_{c1} \), \( Z_{c2} \), \( Z_{\pi 1} \) and \( Z_{\pi 2} \)). Using a four-port network model for the coupled line sections, an equivalent network model of a balun can be synthesised by means of the network theory [176]. From this analysis, normal mode parameters for our broadside-coupled line sections were obtained: \( R_c = 0.0749 \), \( R_\pi = 1.5748 \), \( Z_{c1} = 16.15 \Omega \), \( Z_{c2} = -1.9 \Omega \), \( Z_{\pi 1} = -393.2 \Omega \), \( Z_{\pi 2} = 46.3 \Omega \). The corresponding physical line widths for these modal parameters were determined using LINMIC Interconnect [177], a 2D full-wave simulator based on the spectral operator expansion (SOE) technique. Both lines are 120 μm wide. The length, "s", of each quarter wavelength coupled line section is determined from an average value of the phase velocities for both modes at the centre frequency and is equal to 750 μm. The length, \( g = 150 \mu m \), of the line on the top metal layer, connecting the two sections of broadside-coupled lines, was optimised in view of the input return loss.
3.4. Examples of integrated passives

The measured and simulated balun characteristics are shown in Fig. 3.25. A insertion loss for both output signals is 3.2 dB and 3.3 dB at 58 GHz, respectively, indicating that output signals are slightly undercoupled in comparison to the simulation results. This small difference can be a result of a bit higher measured line loss than simulated but also due to the measurement noise. The balun shows an amplitude balance of 0.5 dB for the 50–68 GHz band and 180° phase difference at 58 GHz. A 15 dB return loss at the input port falls within 50–70 GHz.

Figure 3.25: Balun at 58 GHz: (a) layout (b) phase balance between the two output signals (c) transmissions ('s21' and 's31') (d) input return loss ('s11'). The element dimensions, g and s, are 150 μm and 750 μm, respectively. ('sim' and 'mea' stand for the ENSEMBLE simulated and measured values).
3.4.8. Rat-race at 78 GHz

The performance of a rat-race coupler at 78 GHz is shown in Fig. 3.26. An ultra-low insertion loss for the transmitted signals of 0.2 dB±0.05 at 78 GHz is measured for both in-phase (port 2 is fed) and 180° phase (port 1 is fed) excitation alternatives. The element shows an amplitude balance of 0.5 dB in the 67.5–87.5 GHz frequency band for both feed conditions. Similarly, a 20 dB input match at all ports and isolations are held within 63–92 GHz and 67–90 GHz, respectively. A phase error between transmitted signals is kept below 8° for the similar frequency band. Almost the same measured characteristics for both excitation configurations, indicating very good element symmetry, are due to small line losses and almost negligible influence of the T-junction discontinuities, being a result of the optimised BCB thickness. The reported performance is very close to that of the ideal structure [178].

A further bandwidth enhancement of the rat-race coupler can be achieved by replacing the classical 180° phase shifter with an alternative, realised using broadside coupled lines available in the multi-layer MCM-D technology [179, 180], or by adding the unit elements to each port (increasing the order of circuit response) [179].

3.4.9. Single-section line coupler at 78 GHz

Microstrip directional couplers consisting of parallel coupled lines suffer from poor directivity due to the inhomogeneous dielectric build-up, resulting in different phase velocity of the even and the odd mode. The directivity becomes worse as the coupling is decreased or as the dielectric permittivity is increased [181]. Several methods of improving the directivity of such couplers were proposed, e.g. adding lumped capacitors at each end [182], the use of inductive feedback [183] or using a dielectric overlay of different permittivity on the top of the coupled lines [184].

The ENSEMBLE simulated performance of a -15 dB coupler realised in the technology configuration II with a 5 μm BCB passivation layer (see Sec. 3.2 for the build-up definition) is shown in Fig. 3.27. The element shows very flat and stable coupling level of 15.25±0.5 dB within 53–97 GHz and insertion loss of 0.3–0.37 dB for the transmitted signal (0.15–0.22 dB taking into consideration the coupled power). The isolation and the input match in the entire frequency band are better that 42 dB and 29 dB, respectively, resulting in the worst directivity of 27 dB at 97 GHz. The low permittivity environment created by the BCB dielectric, equalising the even- and odd-mode phase velocities, results in excellent performance, comparable only with the realisations in the micromachined shielded membrane-supported microstrip
3.4. Examples of integrated passives

3.4.10. Patch Antennas

Test substrates with different antenna geometries and configurations were designed and measured for technology characterisation purposes. The basic topology [185]. The achieved high directivity and input match is also due to the excellent high-frequency performance of the bend discontinuities at all four ports of the coupler, being a result of the optimised BCB dielectric thickness.
Figure 3.27: Simulated performance of a 15 dB single-section line coupler at 78 GHz: (a) layout (b) return loss (‘s11’), transmission (‘s21’), isolation (‘s31’), coupling (‘s41’). (The length, width and separation of the coupled line section are 696 μm, 105 μm and line 20 μm, respectively. The coupler is realised in the technology configuration II with a 5 μm BCB passivation layer (see Sec. 3.2 for the build-up definition). Simulations were performed with ENSEMBLE.)

Antenna parameters achieved for simple rectangular patches at 60 GHz and 80 GHz are summarised in Table 3.11. The exact values within the presented ranges depend on the patch width and feed type (directly fed or proximity coupled). The 60 GHz antennas are implemented in the technology setup denoted as Configuration I in Sec. 3.2 and the 80 GHz antennas in Configuration II. The first configuration uses a 3 μm thick gold conductor on the top metal layer, where the patch is located, and copper for all other metal layers. Whereas, for the second configuration, a 1 μm thick copper is applied for all metal layers and an additional 5 μm thick BCB passivation is used on top of the patch antennas. For demonstration purposes, a more detailed analysis

<table>
<thead>
<tr>
<th>Specification</th>
<th>60 GHz</th>
<th>80 GHz</th>
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<tbody>
<tr>
<td>Efficiency [%]</td>
<td>61-64</td>
<td>65-68</td>
</tr>
<tr>
<td>Directivity [dB]</td>
<td>7.2-7.6</td>
<td>7.2-7.5</td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>5.2-5.7</td>
<td>5.5-5.9</td>
</tr>
<tr>
<td>Imp. bandwidth [SWR = 2]</td>
<td>1.2 GHz</td>
<td>1.6 GHz</td>
</tr>
</tbody>
</table>
for the two antenna examples only is presented. The first one is a proximity coupled rectangular patch at 59.5 GHz (Fig. 3.28(a)) and the second a stacked patch configuration at 78 GHz (Fig. 3.28(b)). Both antennas are designed to be matched to a 50 Ω line without additional matching elements. As the degree of planarisation plays a role for multi-layer antennas, the substrates were cross-sectioned in order to validate their build-up.

![Figure 3.28](image)

**Figure 3.28:** Layouts of the microstrip patch antennas: (a) proximity coupled patch at 59.5 GHz (b) stacked patch at 78 GHz.

The proximity coupled patch is fed by a 72 μm wide microstrip line located 15 μm below the patch with a 520 μm long inset. Patch width and length are 2491 μm and 1491 μm, respectively. For the stacked patch antenna, the main radiator is located on the top layer, being 1148 μm long and 1148 μm wide. The second patch is located one layer below and is fed by a 72 μm wide microstrip line. Its width and length are 1708 μm and 1138 μm, respectively. (The former is realised in the technology configuration I, while the latter using configuration II (see Sec. 3.2 for the build-up definition)).

The geometry, return loss and input impedance of the proximity coupled antenna are shown in Figs. 3.28(a) and 3.29. The antenna shows a bandwidth of 1.2 GHz for SWR = 2. One can observe a frequency shift of about 250 MHz between the simulated and the de-embedded measured curves. As every layout geometry and build-up cross-section was verified, and the BCB dielectric constant extracted (in the range of 2.635–2.65), the difference can be attributed to the simulation model truncation. In order to increase the level of confidence, the same measurements were repeated at different times with both TRL and LRRM calibrations and for similar antennas in different places on the panel. The location of the measured return loss minimum practically did not change. Two different simulation tools were also used: Ansoft HFSS and Ansoft Ensemble with a 3D metal geometry. The former might be preferred because one can control model truncation by changing the distance
between the absorbing boundary conditions and the radiating element. It was noticed that changing this distance from half a wavelength to one wavelength still produced a change of the resonant frequency by 400 MHz (0.66% of the resonant frequency). Further model increase is limited by the computational resources. The comparison of the results from ENSEMBLE with those from this larger model, reveals a frequency shift of 150 MHz towards the measured results. The simulation results presented in this work come from the larger HFSS model.

![Graphs showing return loss and input impedance for a proximity coupled patch at 59.5 GHz](image)

**Figure 3.29:** A proximity coupled patch at 59.5 GHz from Fig. 3.28(a): (a) return loss (b) input impedance ($Z_{in}$) (‘meas’ and ‘sim’ stand for the measured and the HFSS simulated values).

Precise determination of the antenna input impedance requires de-embedding of the feed pad structures. Also the reference characteristic impedance and propagation constant of the feed line have to be found. These variables are extracted by means of our in-house procedure [98–100, 110, 111]. After de-embedding of the feed pad structure, the reference plane is shifted down to the antenna input and then its return loss is converted to the input impedance using the known feed line characteristic impedance. Very good coincidence between the simulated and de-embedded input impedances can be noticed, excluding the already mentioned frequency shift. The absolute values and curve shapes of both real and imaginary parts show very good correspondence. Precise de-embedding of the antenna input impedance curve, specifically the input resistance at resonance, enables precise indirect extraction of its efficiency. Antenna input conductance at resonance can be calculated from the radiated power and the conductor, dielectric...
and surface wave losses. The same power contributors define antenna efficiency. As a result, there exists a one-to-one correspondence between input conductance and efficiency which allows the reading of the efficiency from the corresponding input impedance results. The gain and efficiency of the analysed proximity coupled antenna are 5.4 dB and 63.5%, respectively. The latter value stays almost constant within ± 1 GHz around the resonant frequency.

Figure 3.30: A stacked patch at 78 GHz from Fig 3.28(b): (a) return loss (b) input impedance \( (Z_{in}) \) (‘meas (full extr.)’ and ‘meas (cal. substr.)’ denote the de-embedded antenna input match after the full 2-step on-wafer calibration (see Secs. 5.2 and 5.5) and after the calibration with a standard calibration substrate only. ‘simul’ stands for the HFSS simulated results).

The stacked patch antenna is designed to operate at 78 GHz. The geometry, return loss and input impedance of this antenna are shown in Figs. 3.28(b) and 3.30. Once again, a very good correspondence between the simulation and the measurement curves can be seen, excluding a frequency shift of 300 MHz. For comparison purposes, the measured return loss after the first calibration step with a standard calibration substrate (‘meas (cal. substr.)’ in Fig. 3.30) is shown. One can observe its noticeably different frequency behaviour from the simulated and from the exactly de-embedded in the two-step extraction procedure. The absolute values of the return loss and the location of its minima are remarkably different in both cases. It illustrates the need for an exact on-wafer de-embedding technique for a precise antenna resonant frequency measurement at mm-wave frequencies. Using this stacked patch topology, a 2.6-fold impedance bandwidth increase up to 4.15 GHz \((\text{SWR} = 2)\) was obtained in comparison to the single patch. The price for that
is a lower gain of 4.85 dB and an efficiency of 55% because of the limited substrate thickness. HFSS simulations show that the same stacked patch antenna topology, realised using the enhanced MCM-D/L technology [140] (see Sec. 3.5), is able to keep an 80% efficiency.

3.4.11. Antenna arrays at 78 GHz

For the antenna array synthesis, some preliminary parameter values have to be found. These are the required maximum side lobe level determining the array tapering functions, the main lobe beamwidth determining the required antenna array aperture, the supposed array arrangement defined by different system requirements, frequency of operation, technology, etc.

In case of the uniform antenna array, a typical attainable sidelobe level is in the range of -13 dB. Lower values can be achieved by applying array tapering with different optimal arrangement functions, e.g. Dolph-Chebyshev or Taylor-N-parameter distributions, according to the radiation pattern specifications. After fixing the radiation characteristic, the approximate dimensions of the radiating aperture for the required main lobe beamwidth can be found. For instance, specifications of the hypothetical short-range radar from Sec. 3.1.2 with a sidelobe level better than -18 dB realised by the Taylor-one-parameter distribution require approximately an aperture of 11 mm x 22 mm. According to the Nyquist criterion, the free-space wavelength normalised distance between the antenna elements allowing diffraction limited field sampling for the broadside radiation should be considerably lower than one (0.7 results in only one grating lobe for the considered sensor). Taking into account the approximate patch dimensions, an aperture of interest should require approximately 9 x 4 patch elements.

Because of radiation efficiency reasons, the array should accommodate series feed distribution, where possible (see Sec. 3.1.2). The series feed technique has also the advantage that steered and switched beams can easily be achieved. The known drawback is a limited bandwidth in terms of pattern performance, namely the frequency dependence of the side lobe level and beam squint. Nevertheless, these effects can be neglected for the frequency bandwidth of interest (1 GHz). Additionally, a resonant arrangement for every row is chosen because of the broadside radiation considered. The antenna rows are supposed to be fed at their endpoints for minimisation of the feed line length. As this excitation is asymmetrical, it is prone to phase errors along the line. A different arrangement with the feed at the centre of a row can be applied to overcome deviation of the main lobe position in the E-plane due to the induced asymmetry. This type of feed, however, requires longer feed paths to
every row in an array if a multi-layer distribution network is not considered, esp. for high count rows. The parallel arranged series-fed rows within an array are connected by a corporate feed network. The considered hybrid feed (series-corporate) distribution network enables easy beam steering in one direction (by inserting phase shifters for every row) and a minimal row spacing. The reduced feed line lengths and minimised number of junctions is superior in terms of the parasitic radiation and phase shift control at high mm-wave frequencies.

**Synthesis issues of a series-fed patch antenna array**

For an ideal patch antenna, the real part of its input impedance curve is symmetrically distributed around the resonance peak with its maximum value at resonance. The input reactance is zero at resonance and presents an odd symmetry around the zero-crossing point. In this trivial case, the input admittance of every series-fed antenna row at resonance is simply the sum of the element admittances and the power radiated by each element is equal to the ratio of the element admittance to the input admittance of a row. Moreover, all elements in a row are equally excited and radiate in-phase. The input impedance curve of a real patch at higher mm-wave frequencies is not perfectly symmetrical. The main causes of this asymmetry are the reactive behaviour of step-in-width discontinuities at the patch feed points and the higher-order mode loading. The presence of these modes causes an inductive shift of the input impedance plot and, more important, it creates an ascending slope of the input impedance at frequencies higher that the resonance frequency. Of special importance for the array input impedance synthesis is the latter effect, being a result of a resonant curve of the orthogonal $TM_{02}$ mode. Even, if the resonant frequency of this parasitic mode for a single patch seems to be sufficiently far apart, so that this ascending behaviour around the main resonant frequency is still weak, its impact on the input impedance characteristic of a series-fed row can be substantially amplified. This happens because of the series feed arrangement due to which this parasitic impedance behaviour at every patch is Moebius-transformed to the input of an antenna row. Finally, it comes to a complex voltage splitter at every radiating slot of the patch antenna which manifests itself in a non-negligible influence on the amplitude and phase distribution along the row. These, in turn, cause a descending excitation value on every patch along the line, resulting in a weak forming of dips in the radiation pattern. The changed phasing of the excitation from patch to patch also leads to a beam squint of the main lobe.

The above considered parasitic effect is more pronounced for wider
patches due to a decreasing frequency separation between both the main and parasitic resonances, making the input impedance synthesis of a series-fed row more difficult. Taking into consideration that wider patches show an increased radiation efficiency some trade-off is needed while choosing the patch widths for the array synthesis.

Figure 3.31: Equidistant 4x1 series-fed patch antenna array: (a) simulated input impedance (b) simulated return loss (The length and width of the patch elements in a row are 1150 \( \mu \)m and 1550 \( \mu \)m, respectively. The simulations were performed with Ensemble. A 1 \( \mu \)m thick Cu conductor, a 45 \( \mu \)m thick BCB and a 5 \( \mu \)m thick BCB passivation layer on the top were assumed (technology configuration II).

Consequently, a trivial design approach based on the above-mentioned
3.4. Examples of integrated passives

ideal antenna behaviour (\(N\) equal patches connected by half a wavelength line segments) does not yield a valid design. The ENSEMBLE simulated input impedance of the \(4 \times 1\) array, designed using this trivial approximation, is shown in Fig. 3.31(a). The length and width of a single patch antenna used in the array are 1150 \(\mu\text{m}\) and 1550 \(\mu\text{m}\), respectively. The resonant frequency and the input impedance at resonance of this single patch alone are 76.7 GHz and 180 \(+ j 2\). Four such patches are connected by half a wavelength 50 \(\Omega\) transmission line sections. Theoretically, such a configuration should result in a single resonance input impedance curve at about 76.7 GHz that is well matched to the 50 \(\Omega\) reference impedance. As it can be observed in Fig. 3.31(a), up to four different resonant peaks can be read out of the presented plot, instead of one. A closer look to the field distribution on the patch antenna shows that only one peak at about 76.75 GHz corresponds to a resonance of the main mode. The input match at this frequency is only -8.3 dB (see Fig. 3.31(b)). The other peaks in the plot result from the impedance transformations of the non-ideal input impedance characteristics of the single patch elements, i.e. the inductive shift and the ascending slope caused by higher order modes and step-in-width junctions. The resulting beam squint for this small array approaches 4\(^\circ\).

Summarising, a successful and systematic synthesis of a series-fed antenna row requires simultaneous consideration and optimisation of the all patch antenna resonant lengths and lengths of the line sections separating radiation elements in a row in order to compensate for the parasitic effects. This compensation is non-uniform, i.e. the length shortening varies from element to element because each patch is differently loaded, depending of its position in a row. A cut-and-try empirical tuning procedure based on full-wave simulations is a tedious task and it is not an efficient way to find the desired array geometry because of a number of geometrical parameters to be set. The solution to this issue should rely on the implementation of a simplified antenna model, which would allow much faster computation of the array input impedance. Only final verification and fine-tuning of the geometry could be performed using a full-wave simulator.

Optimisation routine

Several theoretical models for microstrip patch antennas have been developed that are based on either resonant cavity or transmission line models of the microstrip circuit. For the cavity analogy, the applicability of the modal-expansion technique by Carver and Mink [186] with an impedance boundary condition at the magnetic wall accounting for the loss was verified within this work. The attempts to build the extended version of the analytical transmis-
Figure 3.32: Optimised non-equidistant 4x1 series-fed patch antenna array from Fig. 3.31: (a) simulated input impedance (b) simulated return loss (The spacing between the patches are 925 µm, 1200 µm and 1200 µm, counting from the end-feed point. The simulations were performed with Ensemble).

sion line model [187], that could account for dissipation losses on the patch and the parasitic reactances at the antenna feed, were also undertaken. The accuracy of both approaches, when compared to the full-wave HFSS simulation results, was found to be insufficient. When these models were applied to practical synthesis of series-fed antenna arrays, serious anomalies in the full-wave simulated input impedance, unpredictable beam position and sidelobe levels were observed, similar to those reported in [188].
3.4. Examples of integrated passives

Figure 3.33: Simulated gain pattern of the optimised non-equidistant 4x1 series-fed patch antenna array from Fig. 3.32 (The simulations were performed with Ensemble).

An optimisation routine for the input impedance synthesis of a series-fed antenna row was established in which the behaviour of a set of patch geometries, represented by a 2-port impedance matrix, was extracted from the full-wave simulations. In a result, only a simplified synthesis procedure, based on searching for the optimum lengths of the lines sections connecting the patches, was possible.

Figs. 3.32(a) and 3.32(b) presents the results of this synthesis for the same 4 x 1 array from Fig. 3.31(a). A classical, single peak, resonant curve with almost zero value reactance at the resonance was achieved. The resultant spacing between the patches are 925 μm, 1200 μm and 1200 μm, counting from the end-feed point. The input match at the resonance frequency is better than 35 dB. As depicted in Fig. 3.33, a gain of 11.8dB and a beam squint smaller than 0.5° (E-plane) was achieved. A side lobe level is -11.4dB which is good, taking into account that no tapering has been applied yet. A radiation efficiency of 62% was calculated.

Using the same optimisation routine some larger arrays were designed. Fig. 3.35 presents the input impedance and gain pattern at 80.5 GHz of the synthesised 6 x 4 array from Fig. 3.34. The array was not tapered and, thus, a uniform power distribution along the row was realised. The length and width of the patch element are 1110 μm and 1000 μm, respectively. The array aper-
Figure 3.34: Layout of the optimised non-equidistant 6x4 series-fed patch antenna array. (The length and width of every patch element are 1110 μm and 1000 μm, respectively. The overall aperture dimensions are 14 mm × 7 mm and the separation between the rows is 1000 μm).

The large input impedance bandwidth (see Fig. 3.35) is a result of the previously analysed influence of impedance transformations along a row and it is not an inherent property of the patch used. The proper resonance of the array is located at 80.5 GHz. The simulated (Ensemble) gain and cross-polarisation level in the H-plane (not shown) are 17.6 dB and -34 dB, respectively. A considerable beam squint of 2.5° and side lobe level in the gain pattern can be observed. The simulations results of the two smaller, 6 x 1, 6 x 2, arrays show practically the same side lobe and cross-polarisation levels in the E-plane as for the 6 x 4 array, indicating that corporate feed network consisting of the three T-junctions, some bends and quarter wavelength transformers do not contribute to the parasitic radiation (see Secs. 3.4.1 and 3.4.1). Moreover, very low reactances associated with these discontinuities will not limit the input impedance bandwidth even for larger arrays.

As far as the input impedance synthesis problem was investigated, the array radiation pattern was not considered in the optimisation routine. It could be noticed that the input impedance synthesis routine is not coherent with the radiation pattern optimisation. The ultimate automation procedure should be first focused on this latter aspect and the appropriate input impedance match could be then achieved in the next step by building some matching circuitry. The procedure for a pattern synthesis can be formulated similarly to that reported in [189]. For this purpose, transmission line models of the patch antennas with the values extracted from full-wave simulations and related to
3.4. Examples of integrated passives

Figure 3.35: Optimised non-equidistant 6x4 series-fed patch antenna array from Fig 3.34: (a) simulated return loss (b) simulated gain pattern (The simulations were performed with Ensemble).

the physical patch dimensions by a functional approximation are necessary. Two basic criteria for the row arrangement optimisation in terms of a radiation pattern are the equal phase of excitation on every patch and 180° phase shift between both patch radiating edges. Hence, the excitation voltages at the radiation conductances of a distributed transmission model should be reverse
phased along the patch row. Moreover, the absolute value of the excitation voltages should be constant along the row.

Based on these preliminary results, it can be stated that an array required for the short range ACC radar sensor at 78 GHz with an efficiency better that 50% can be integrated within the developed MCM-D process. The only factor limiting an array growth in one of the dimensions is the loss associated with the corporate distribution network. For the implementation of large arrays in two directions with high radiation efficiency, more advanced technologies are required, allowing the integration of alternative low-loss feed transmission media such as waveguides.

### 3.5. An MCM-D/L technology for patch antenna performance enhancement

In order to achieve higher patch antenna efficiency, assuming maximum available BCB thickness of 45μm (3x15μm), a concept of a mixed MCM-D/L build-up was proposed [140].

The maximum achievable patch antenna efficiency for a given dielectric material and a resonant frequency corresponds to the substrate thickness with which the total loss, consisting of the dielectric and conductor dissipation losses (decrease with dielectric thickness) on one side and the surface wave loss (increase with dielectric thickness) on the other, is minimised. For the thickness satisfying

\[
\frac{h_s}{\lambda_0} \leq \frac{0.3}{2\pi \sqrt{\varepsilon_r}}
\]

the surface wave loss can be neglected [190].

An additional 50 μm thick layer of high-frequency laminate Speedboard C (\(\varepsilon_r = 2.56\)) or a 63 μm thick combined layer of Microlam 410 (\(\varepsilon_r = 3.4\)) and Biac LCP (\(\varepsilon_r = 3\)), underlying a 45 μm thick BCB film (see Sec. 4.1.2), increases the total patch antenna thickness up to around 100–110 μm. It results in a radiation efficiency increase up to 80-83% and an impedance bandwidth increase up to 2.5 GHz for a single directly-fed patch. Further thickness increase results in a decreasing radiation efficiency, indicating growing influence of the surface waves. Taking into consideration that the dielectric permittivities of the laminate layers are close to that of the BCB, the chosen total thickness is close to 113 μm, calculated from Eq. 3.3 for the BCB dielectric constant and the frequency of 77 GHz.

With these build-ups, the radiation efficiency of the stacked patch antenna from Sec. 3.4.10 can be increased up to 80%.
As a precise resonant frequency location of the patch antennas at 77 GHz requires high metal trace accuracy (see Sec. 3.1.3), patterning a thick copper plated on a laminate is prohibited. Furthermore, ohmic loss at 80 GHz for such a metallisation is considerably larger than on the BCB film because of the higher laminate surface roughness of 400–600 nm (see Sec. 4.1.3). In the proposed mixed laminate-BCB build-up, the required accurate metal pattern is defined on the BCB film and the copper-plated laminate delivers only a ground plane for the patch antennas. The other non-radiating passive elements and interconnections still make use of the ground plane patterned on a 45 μm thick BCB film to keep their advantageous performance (see Sec. 3.1.2). With such a module realisation, one needs to connect these two separate ground planes at the antenna feed. The HFSS simulation results of this transition, presented in Fig. 3.36, show that its return and insertion loss at 80 GHz can be superior to 30 dB and 0.06 dB, respectively. An influence of the reactances introduced by a via wall connecting both ground-planes is compensated using the appropriate microstrip line width in the overlapping area between both ground planes.

The disadvantage of the proposed mixed build-up is a higher roughness of the laminate layers. It can lead to untolerably low quality of the consecutive
metallisation layer used as a ground plane for the non-radiating passives. This issue is partly solved by adding a 5 \( \mu \)m thick BCB planarisation layer. The measured \textit{rms} roughness of the consecutive ground plane layer on such a preconditioned surface is 110 nm. This value is supposed to increase the line loss at 80 GHz only marginally because the roughness of a top metallisation layer, used for the microstrip definition, is almost unaffected. Furthermore, some loss in the metal lithography precision, being a result of less accurate surface underlying the BCB film, can still be tolerated for the previously considered non-radiating passives and patch antennas.

The first MCM-D/L test vehicles are still under prototyping.

### 3.6. CPW on a low dielectric constant MCM-D substrate

The constraints of the CPW configuration usage in hybrid technologies at higher mm-wave frequencies were already outlined in Chapter 2, Sec. 3.1.1 and Appendix B. It was shown that both high and low dielectric constant substrates can generate feasibility problems. The former are a source of substantial leakage to substrate modes due to the large lateral dimensions of the interconnect elements, being a result of a low metal pattern resolution. The latter can result in better overmoding characteristics but they create a high line width to wavelength ratio, leading to high reactances, radiation loss and phase shifts at meander and junction-like discontinuities.

For comparison purposes with the proposed microstrip configuration (45 \( \mu \)m thick BCB), the performance of different interconnect and distributed passives at 50–70 GHz, realised in the FGCPW topology on a low permittivity substrate, was investigated. On this basis, some critical drawbacks of this solution, not reported before, will be outlined. The investigations are conducted for a 45 \( \mu \)m thick BCB (the same thickness as for the microstrip configuration) on a 500 \( \mu \)m thick Rogers 4003 laminate carrier (\( \varepsilon_r = 3.38 \)), the technology build-up investigated within the frame of the LIPS project [117]. This substrate can be viewed as representative for MCM technologies based on a laminate carrier.

From Table 3.3 in Sec. 3.1.2, gathering the line widths and line wavelengths at 60 GHz for both microstrip and CPW configurations applied in this work, it can be noticed that a 50 \( \Omega \) CPW line requires a 230 \( \mu \)m centre strip, assumed a minimum slot width of 20 \( \mu \)m. This results in a line ground-ground spacing approaching one-tenth of the guided wavelength at 60 GHz and electrically large discontinuities, contrary to MMIC counterparts. Specifically addressed are transmission elements requiring the use of bridges or tunnels for the parasitic slotline mode suppression [191] such as bends and junctions. A
3.6. CPW on a low dielectric constant MCM-D substrate

common thread in each case is the compensation of the excess capacitance introduced by bridge or tunnel, considered as one of the dominant performance limiting factors at mm-wave frequencies. The impact of this capacitance can outweigh that of the parasitics inherent to bend or junction itself, especially for wide centre strips of the lines such as the ones used in our build-up.

A finite-ground CPW (FGCPW) configuration with a ground-plane width of 300 μm was used to minimise the influence of parasitic surface waves and parallel-plate modes (see Appendix B and Sec. 3.1.1). For the considered dielectric build-up, the location of critical frequencies defining the CPW mode coupling to the lowest order $TM_0$ and $TE_0$ surface wave modes falls approximately at 100 GHz and 125 GHz for the grounded and air-suspended substrate, respectively (see Eq. B.1).

In a conventional MMIC process, airbridges are used for suppression of the parasitic slotline mode, whereas both bridges and tunnels can be applied in a multi-layer MCM-D process. As the considered CPW lines are realised on the top metallisation layer, only tunnels located on the lower layer (15 μm below) were investigated.

On the basis of numerous investigations and performance analysis of basic FGCPW interconnect elements realised using the considered BCB/Rogers 4003 MCM-D build-up, the following set of critical disadvantages, substantially limiting the electrical performance of this topology above approximately 50 GHz, was found:

1. Complex design techniques and long time design cycles of distributed passives, distribution networks and systems at mm-wave frequencies are required due to the electrically large cross-sections of discontinuity elements and, thus, an increased influence of boundary conditions on the backside of a finite thickness substrate. Substantial effort is required for appropriate compensation of the parasitic behaviour at discontinuities requiring the use of bridges and tunnels. Without this improvement, the cumulative effect of input mismatch at various elements comprising larger and more complex functional elements will easily lead to the circuit malfunction. A large line cross-section also raises important problem concerning the modelling. A simple approach based on the equivalent models applied in most of the circuit simulators is able to give only very rough approximations and in many cases is likely to fail completely. As a result, full-wave electromagnetic simulations are required in order to properly predict an element’s behaviour, considerably increasing the optimisation and design cycles.

2. The required full-wave electromagnetic simulations are related to a
large computational effort. For example, 3D FEM simulations (HFSS) of a single tunnel-based discontinuity with the appropriate accuracy can take up to 15 min per frequency point and require up to 200 MB memory on a Sun Ultra 60 with 2 GB RAM. Moreover, typical distributed elements with a higher number of tunnels lead to substantially larger computational problems. Simulations of a Wilkinson power divider (HFSS) and a Lange coupler (Sonnet) at 60 GHz required 60 min per frequency point, 1 GB memory on a Sun Ultra 60 with 2 GB RAM and 300 min per frequency point, 800 MB memory on a PC Pentium III with 1 GB RAM, respectively. In a result, full-wave optimisation of these structures is a very time consuming process.

3. A high line width to wavelength ratio in the frequency range of interest very often deteriorates the performance or even disables the realisation of many distributed passives based on a combination of quarter-wavelength transmission line sections (900–800 μm at 60–70 GHz in our case), bends and T-junctions. The reason is that every compensated bend or junction generates a high phase shift ($40 - 50^\circ$ at 60–70 GHz) because of its large cross-section and reactive behaviour. The theoretical quarter-wavelength long line sections and a space between parallel CPW lines must be reduced even down to 200-300 μm to account for these phase shifts. This leads to coupling between the lines, affecting the broadband match at the inputs and the isolation between some appropriate branches. A representative example can be a Wilkinson power divider for which a simultaneous achievement of 20 dB match at all ports and 20 dB isolation between output ports was practically impossible. A similar problem in the design of a Wilkinson divider at 50 GHz on a high resistivity silicon substrate was encountered in [192].

4. Designing high-selectivity elements for which the confinement of electromagnetic fields is a problem, eg. narrow-band coupled-line filters, is practically impossible. The required high separation between the coupled line sections forces the use of even larger ground-ground spaces and, thus, larger tunnel or bridge elements. This, combined with very short line sections at the frequencies of interest, leads to the situation that the widths of the designed structures are comparable to their lengths and the frequency characteristics are practically dominated by the parasitic behaviour of electrically large discontinuities. In [193], it was demonstrated that even very high resolution MMICs have reached their limits in the realisation of narrow-band coplanar coupled-line filters at 60–95 GHz. It was also emphasised that the development of new
3.7. Quasi-CPW and quasi-ACPS transmission line media

technological concepts, such as multi-layer or 3D technology, is necessary to design such critical devices.

5. As a result of the minimum slot width of 20 μm, the range of characteristic impedance values is lower-limited to 50 Ω for a 270 μm line ground-ground spacing. This causes that some elements such as a 3 dB branch line coupler, requiring 35 Ω lines, are unfeasible. This minimum characteristic impedance value could be decreased to approximately 40 Ω for a thin BCB layer on a ceramic substrate, assuming the same minimum slot width. For comparison purposes, a 30-80 Ω impedance range is realisable for GaAs or InP substrates, assumed a minimum strip width of 10 μm and a ground-ground spacing of 100 μm.

6. Long grounding paths lead to the higher end inductance values than those for the microstrip configuration in the developed technology build-up. As a result, the performance of uncompensated loads is worse than their microstrip counterparts, even without grounding vias. The return loss of an uncompensated 75 μm long and 60 μm wide 50 Ω NiCr (38 Ω/square) load embedded in a 270 μm wide 50 Ω FGCPW transmission line is inferior to 20 dB above 17 GHz. A modified geometry with a line ground-ground distance around the load locally narrowed down to 100 μm shows a return loss better than 20 dB below 30 GHz. Both 79/60 μm and 158/120 μm uncompensated 50 Ω microstrip loads from Sec. 3.4.2 show a return loss better than 20 dB up to 50 GHz.

7. The inter-circuit isolation is low due to the large cross-sectional dimensions of transmission lines and discontinuities on a non-negligibly thick (electrically thick) substrate, promoting space wave radiation, leakage to surface waves and MSL modes (the latter for a backside metallised substrate) (see Appendix B). For the same reason, the open-end elements show considerably larger losses and end extension values than their microstrip counterparts in the developed technology build-up.

The above discussed drawbacks indicate that the electrical performance of the CPW realisation in the frequency band of interest is expected to be far below that of the applied microstrip configuration on a 45 μm thick BCB.

3.7. Quasi-CPW and quasi-ACPS transmission line media

To alleviate some of the previously analysed issues encountered in a classical FGCPW realisation, the advantage of a multi-layer build-up was taken into
account in order to create a transmission line media, which will be called a finite-width quasi-CPW line [67]. It is a two-layer configuration formed by an elevated centre conductor above the ground planes on its both sides (see Fig. 3.37).

![Figure 3.37: Geometry of a finite-width quasi-CPW transmission line (w, s and g denote a centre strip width, a slot width and a ground-plane width, respectively).](image)

With this approach, a considerably wider range of feasible characteristic impedances is allowed for the fixed line ground-ground distance, when compared to the previously considered classical CPW line topology. A typical range of characteristic impedances for a ground-ground spacing of 240 μm (similar to that used for a standard CPW configuration) with the corresponding line dimensions, attenuations and wavelengths at 60 GHz is presented in Table 3.12. Some classical CPW line geometries are also included for comparison purposes. Characteristic impedance values as low as 20 Ω can be realised without enormous widening of the centre strip. A negative value for the slot width for this low impedance line means that the strip and the lower ground planes overlap. In this case, the electric fields are highly concentrated in the overlap area, thus locally resembling a microstrip-like field distribution and rapidly reducing the impedance value at the cost of some increase in a line attenuation constant. This attenuation, however, still remains below typical values reported for GaAs or InP CPW lines (0.12 dB/mm at 20 GHz for a 40/30 μm 50 Ω CPW on InP substrate). Furthermore, the lines still show very low high-frequency dispersion, keeping the advantage of the standard CPW topology. For example, the line effective permittivity of the mentioned 20 Ω quasi-CPW line is equal to 2.45 and 2.41 at 10 GHz and 100 GHz, respectively. The ground-ground distance of a quasi-CPW line can be further decreased at the cost of some additional line loss, reducing the line width to wavelength ratio and, thus, allowing to cover the higher frequency range of operation. (see 50.3 Ω quasi-CPW line with a ground-ground spacing of 150 μm in Table 3.12).

The prediction of electrical behaviour of the via-based tunnels or any
Table 3.12: Comparison of the line geometry, characteristic impedance, line attenuation and wavelength at 60 GHz for CPW and quasi-CPW lines. (Both CPW and quasi-CPW lines are finite-width realisations with a ground-ground distance, g, of 300 µm. The values are simulated with HFSS. A 3 µm copper conductor was used for the metallisation layer. The BCB and Rogers 4003 loss tangents of 0.002 and 0.0027, respectively, were assumed in simulations.)

<table>
<thead>
<tr>
<th>Config.</th>
<th>GG [µm] (ground-ground)</th>
<th>w/s [µm] (strip/slot)</th>
<th>$Z_0$ [Ω]</th>
<th>$\alpha$ [dB/mm] at 60 GHz</th>
<th>$\lambda$ [mm] at 60 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPW 270</td>
<td>w/s = 230/20</td>
<td>50.4</td>
<td>0.08</td>
<td>3.6</td>
<td></td>
</tr>
<tr>
<td>CPW 270</td>
<td>w/s = 166/52</td>
<td>71.2</td>
<td>0.053</td>
<td>3.572</td>
<td></td>
</tr>
<tr>
<td>CPW 270</td>
<td>w/s = 90/90</td>
<td>100.2</td>
<td>0.05</td>
<td>3.576</td>
<td></td>
</tr>
<tr>
<td>CPW 270</td>
<td>w/s = 30/120</td>
<td>146</td>
<td>0.063</td>
<td>3.61</td>
<td></td>
</tr>
<tr>
<td>Q-CPW 240</td>
<td>w/s = 206/17</td>
<td>49.7</td>
<td>0.079</td>
<td>3.464</td>
<td></td>
</tr>
<tr>
<td>Q-CPW 240</td>
<td>w/s = 140/50</td>
<td>73.4</td>
<td>0.054</td>
<td>3.512</td>
<td></td>
</tr>
<tr>
<td>Q-CPW 240</td>
<td>w/s = 76/82</td>
<td>102</td>
<td>0.053</td>
<td>3.546</td>
<td></td>
</tr>
<tr>
<td>Q-CPW 240</td>
<td>w/s = 240/0</td>
<td>35.7</td>
<td>0.12</td>
<td>3.376</td>
<td></td>
</tr>
<tr>
<td>Q-CPW 240</td>
<td>w/s = 300/-30</td>
<td>20</td>
<td>0.16</td>
<td>3.222</td>
<td></td>
</tr>
<tr>
<td>Q-CPW 150</td>
<td>w/s = 130/10</td>
<td>50.3</td>
<td>0.1</td>
<td>3.462</td>
<td></td>
</tr>
</tbody>
</table>

other underpass-based discontinuities without an exact visual inspection of their cross-section is difficult because of the possibly considerable planarisation issues. Hence, they are definitely measurement-based elements [194]. The underpass geometry in the quasi-CPW topology allows direct ground-plane connection on both sides of a centre strip without the use of vias. It allows better attenuation of the parasitic slotline mode and considerably higher dimensional miniaturisation, required for higher frequency operation. Furthermore, via-less structures result in a lower computational effort for the full-wave electromagnetic simulations and, thus, allow faster design cycles. The geometry and HFSS simulated return loss of an optimised tunnel for a 50 Ω quasi-CPW line (240 µm ground-ground distance) are shown in Fig. 3.38. A 30 µm wide underpass was applied and a ground-ground distance was reduced to 80 µm under the underpass for better parasitic slotline mode suppression. The simulated return loss is better than 28 dB up to 80 GHz.

A similar concept can be applied to arrive at the quasi-ACPS lines (Asymmetric Coplanar Stripline). These, combined with the quasi-CPW lines, show an important advantage in the design of T-junctions. A standard CPW T-junction requires three compensated tunnels or bridges to suppress the slotline mode, whereas the simultaneous use of the quasi-CPW and quasi-ACPS topologies reduces this number to one because the two quasi-ACPS lines do not excite the slotline mode. This approach substantially simplifies the de-
Figure 3.38: Optimised 50 Ω quasi-CPW tunnel: (a) geometry (b) simulated return loss (HFSS). ‘Opt’ and ‘non-opt’ correspond to a return loss of the optimised and non-optimised tunnel geometry. For both structures, a centre strip width, \( w \), a line ground-ground spacing and a ground plane width, \( g \), are 206 \( \mu m \), 240 \( \mu m \) and 300 \( \mu m \), respectively. For the non-optimised tunnel, \( p = 0 \ \mu m \), \( l' = w \), \( Tl = 240 \ \mu m \) and \( Tw = 30 \ \mu m \). Similar parameters for the optimised tunnel take the following values: \( p = 75 \ \mu m \), \( l' = 60 \ \mu m \), \( Tl = 80 \ \mu m \) and \( Tw = 30 \ \mu m \).

Sign of distributed elements and can lead to better performance at mm-wave frequencies.

The geometries of a 50-50-35 Ω T-junction realised in the quasi-CPW configuration only, and using both quasi-CPW and quasi-ACPS topologies are shown in Fig. 3.39. Both junctions were used in the design of different 3dB branch line couplers, previously unfeasible in the standard CPW configuration. The HFSS simulated transmission coefficients of the T-junction realised using only the quasi-CPW topology are shown in Fig. 3.40. A very stable power division ratio can be observed in the entire simulated frequency range, being of importance for successful and simple design procedures of distributed passives comprising a larger number of T-junctions.

As the elements realised in the quasi-CPW configuration need to be connected to the standard CPW lines in some points (for the measurement or chip connection purposes), a high performance transition is required. The geometry of such a transition for the 50 Ω lines, together with its HFSS simulated return loss, is depicted in Fig. 3.41. This very simple transition allows to keep a return loss better than 28 dB up to 80 GHz at the 50 Ω CPW input port and, thus, does not influence the overall performance of the elements in the quasi-CPW topology.
3.7. Quasi-CPW and quasi-ACPS transmission line media

Figure 3.39: Geometries of a 50-50-35 $\Omega$ T-junction realised in: (a) the quasi-CPW configuration (b) the mixed quasi-CPW/quasi-ACPS configuration. '1' and '3' are the 50 $\Omega$ ports, whereas '2' is a 35 $\Omega$ port.

(For the (a) realisation: $w_1 = w_3 = 210$ $\mu$m, $s_1 = s_3 = 15$ $\mu$m, $w_2 = 250$ $\mu$m, $s_2 = -5$ $\mu$m, $T_{w1} = T_{w3} = 30$ $\mu$m, $T_{i1} = T_{i3} = 100$ $\mu$m, $T_{w2} = 50$ $\mu$m, $T_{i2} = 70$ $\mu$m, $p_1 = p_3 = 70$ $\mu$m, $p_2 = 85$ $\mu$m, $l_1 = 65$ $\mu$m, $l_2 = 80$ $\mu$m and $l_c = 200$ $\mu$m.)

(For the (b) realisation: $w_1 = 210$ $\mu$m, $s_1 = 15$ $\mu$m, $w_2 = 190$ $\mu$m, $s_2 = -40$ $\mu$m, $w_3 = 190$ $\mu$m, $s_3 = -10$ $\mu$m, $T_{w1} = 30$ $\mu$m, $T_{i1} = 240$ $\mu$m and $l_c = 210$ $\mu$m).

Figure 3.40: Simulated (HFSS) transmission coefficients of the 50-50-35 $\Omega$ T-junction from Fig. 3.39(a) realised in the finite-width quasi-CPW configuration. ($s_{12}$, $s_{13}$ and $s_{23}$ stand for the transmission coefficients between the appropriate ports numbered from 1 to 3. A 3 $\mu$m copper conductor was used for the metallisation layer. The BCB and Rogers 4003 loss tangents of 0.002 and 0.0027, respectively, were assumed in simulations).
Figure 3.41: Transition between the 50 Ω finite-width CPW and finite-width quasi-CPW lines: (a) geometry (b) simulated return loss (HFSS) at the finite-width CPW port (HFSS). (The transition employs 3 vias (60 μm in diameter) on every side of the centre strip and an overlap, gg, of 80 μm between the ground planes of a finite-width CPW and a finite-width quasi-CPW line. The line dimensions for both connecting transmission lines are: w = 240 μm, w' = 210 μm, s = 20 μm, s' = 15 μm, g = 300 μm and g' = 315 μm).

3.7.1. Applications

To demonstrate the application of the quasi-CPW and quasi-ACPS line configurations, a variety of different distributed passives were designed. For demonstration purposes, a Gysel power divider at 60 GHz, a branch-line coupler at 20 GHz and a set of stepped-impedance low-pass filters at 60 GHz will be presented.

A Gysel divider (Fig. 3.42(a)) [195] was implemented because of the previously mentioned problems in the design of a Wilkinson power divider (see Sec. 3.6). Due to its specific topology, the two output branches (’2’ and ’3’ in Fig. 3.42(a)) are separated by half a wavelength distance. It alleviates the problem of inter-line coupling, the main issue in the design of a CPW Wilkinson divider. For the successful realisation of a Gysel divider, a compensated 50-50-70 Ω T-junction in the mixed quasi-CPW/quasi-ACPS configuration was designed. The HFSS simulated insertion loss of the divider is 1 dB at 58 GHz (excluding power split), being substantially higher than that of the Wilkinson divider at 60 GHz (0.2 dB) from Sec. 3.4.5 realised in the optimised microstrip topology. Such high insertion loss is attributed to radiation loss at still electrically large junctions and higher line attenuation of the quasi-ACPS line sections with an overlap between the ground plane and the strip.
3.7. Quasi-CPW and quasi-ACPS transmission line media

Figure 3.42: Gysel power divider at 60 GHz in the finite-width quasi-ACPS configuration: (a) geometry (b) simulated S-parameters (HFSS). Both an input port, 1, and two output ports, 2 and 3, are connected to 50 Ω quasi-CPW lines. (A 3 μm copper conductor was used for the metallisation layer. The BCH and Rogers 4003 loss tangents of 0.002 and 0.0027, respectively, were assumed in simulations. The strip and slot widths of the 50 Ω and 70 Ω quasi-ACPS line sections are 190/15 μm and 180/10 μm, respectively. An underpass within the T-junctions is 40 μm wide and 100 μm long, whereas that at the input port, 1, 30 μm wide and 240 μm long. The lengths 'l70' and 'l50' are 1250 μm and 570 μm, respectively).

Figure 3.43: Branch line coupler at 20 GHz in the finite-width quasi-ACPS configuration: (a) geometry (b) simulated S-parameters (HFSS). (The lengths 'l50' and 'l35' are 2480 μm and 1810 μm, respectively. A 50-50-35 Ω T-junction from Fig. 3.39 was applied in the design of this element).
The geometry of a branch line coupler at 20 GHz in the quasi-ACPS configuration is shown in Fig. 3.43(a). It shows very good return loss ('Return') and isolation ('Isolation') but an insertion loss of 0.5 dB (excluding power split) for both output ports ('Direct' and 'Coupled') is incomparably higher than 0.25 dB for the microstrip branch line realisation at 60 GHz from Sec. 3.4.6.

A 9th-order Chebyshev prototype with 0.04 dB ripples and return loss better than 20 dB in the passband was chosen for a 60 GHz stepped-impedance low-pass filter realisation in order to demonstrate the potential of the quasi-CPW configuration for an improved impedance ratio between high- and low-impedance line sections. A schematic drawing of the filter geometry and the HFSS simulated S-parameters of three different realisations are shown in

Figure 3.44: Stepped-impedance low-pass filter at 60 GHz in the finite-width quasi-CPW configuration: (a) geometry (b) simulated S-parameters (HFSS). (The S-parameters of 3 different realisations are shown: a classical finite-width CPW denoted as 'CPW 144/47 Ω' (270 μm line ground-ground spacing) and two finite-width quasi-CPW, 'QCPW 156/27 Ω' and 'QCPW 173/23 Ω' (240 μm line ground-ground spacing), with different high-, \( Z_H \), and low-impedance, \( Z_L \), line sections. The overall filter length, \( l_f \), varies between 3100 μm and 3700 μm for the 3 considered filter geometries. For the tunnel geometry at the input 50 Ω ports, see Fig. 3.38.)
Fig. 3.44. For the first, the standard CPW configuration was applied with the 47 Ω low-impedance and 144 Ω high-impedance line sections, respectively. The other two are implemented in the quasi-CPW configuration. The corresponding impedance ratios were chosen to be 156/27 Ω and 173/23 Ω. The higher achievable impedance value for the high-impedance line sections in the quasi-CPW topology is a result of the larger distance between the centre strip and the ground plane located on the lower metallisation layer. The considerably lower impedances for the low-impedance line sections are realised by the suitable overlap between the centre strip and the ground-plane.

Only the filter realisation with the highest impedance ratio of 173/23 Ω preserves the passband return loss of its prototype (20 dB). Both quasi-CPW layouts show low passband ripples and a sharp rejection-band edge. A 35 dB out-of-band attenuation falls at 85 GHz for both of them. The filter based on the standard CPW topology shows only a 10 dB return loss with substantially higher ripples in the passband and a maximum stop-band attenuation of only 24 dB at 90 GHz.

3.8. Summary

This chapter presented the development of a single substrate integration concept at 60–80 GHz using a modified multi-layer BCB-based MCM-D technology with a performance-oriented, optimally chosen dielectric thickness. The limitations of the CPW configuration usage in hybrid technologies above 50 GHz were discussed. They supported the choice of the microstrip configuration, assuming that the appropriate BCB thickness can be achieved. The process of finding this optimal thickness was thoroughly analysed.

The final technology build-up is based on a 3-layer BCB film with an overall thickness of 45 μm. It allows the realisation of low-loss transmission lines without high-frequency dispersion up to 100 GHz and low parasitics at discontinuities. The low dielectric permittivity of BCB and its low surface roughness support this performance. The potential of the developed process is verified by over 1000 measurement and simulation results [141], including:

- transmission lines and discontinuities
- series resistors and frequency compensated loads, including an ultra wide-band termination with an input match better than 20 dB up to 160 GHz
- low-pass and band-pass filters
- Wilkinson power dividers
• branch-line, rat-race and single-section line couplers
• multi-layer balun
• patch antennas and patch antenna arrays

The full-wave simulated performance of some other integrated passives at 94 GHz was also presented, showing the potential of the developed technology at even higher frequencies. With the proposed MCM-D process, the design of high-performance passive elements at 60–100 GHz frequencies can be as simple as in the lower microwave frequency range because most of the deteriorating high-frequency effects are eliminated. The performance is highly repeatable due to the accurate metallisation definition and precise BCB thickness control.

Furthermore, a concept of a mixed MCM-D/L build-up was proposed [140] for enhancing the patch antenna efficiency and bandwidth. The first processed substrate samples show promising results.

For comparison purposes with the proposed microstrip-oriented technology build-up, an alternative BCB/Rogers 4003 MCM-D technology setup, allowing the use of the CPW configuration, was investigated. On the basis of numerous full-wave simulation and measurement results of different transmission line discontinuities and distributed passives, a set of critical drawbacks of the CPW topology in hybrid technologies above 50 GHz was presented. It led to the proposal of the quasi-CPW and quasi-ACPS transmission line alternatives [67], taking advantage of the multi-layer build-up. The use of these line topologies allows to alleviate the problem of the high line width to wavelength ratio, critical at mm-wave frequencies, and to arrive at a substantially wider range of feasible characteristic impedance values for the fixed line ground-ground spacing. This approach also results in a high planarity via-less realisation of bridges and tunnels. Avoiding vias in these structures promotes further miniaturisation of transmission line discontinuities and, thus, easier realisation of distributed passives. The full-wave simulations of such structures are less time- and memory-consuming. The use of quasi-ACPS lines in T-junctions avoids the slotline mode excitation and, thus, leads to further design simplifications. Additionally, the realisation of some elements such as a 3 dB branch line coupler, unfeasible with the standard CPW configuration due to the too low required characteristic impedance, is possible with the proposed line topologies. The performance of other elements such as stepped-impedance low-pass filters can also be considerably improved due to the wide range of feasible characteristic impedance values.
An MCM-L process for mm-wave applications

In this chapter, the development process of an MCM-L (Multi-Chip Module with laminated interconnect) interconnection and packaging technology (also called M-HDI - Microwave High-Density Interconnect) for mm-wave modules in V-band is presented.

It is supposed to be used for the realisation of the mm-wave front-end of a 60 GHz Point-to-Point T/R module demonstrator (see [117]). A general build-up of the packaging concept is shown in Fig. 4.1. For compatibility with low-cost manufacturing, the developed technology favours collective processes with every processing step performed for a large number of modules at the same time. Active and passive devices, including MOS decoupling capacitors, are positioned in cavities in a common substrate, allowing wire-bonding suppression. At mm-wave frequencies, the high wire inductance and low bond repeatability can require tuning and rework at the module level, im-
pacting cost and production yield. A silicon or a copper substrate is considered as a heat sink. A dielectric layer made of polymer films is laminated on the top. A classical photolithographic process and chemical etching are used for the copper interconnects in order to arrive at appropriate reproducibility at mm-wave frequencies. Connecting vias are defined directly above the dies thanks to alignment marks left on the substrate and drilled by laser ablation. The last processing steps are related to the solder bumps formation for compatibility with SMT assembly. They include patterning for an electrolytic gold finish, spin-coating of a 7–8 μm thick Probimer 77 solder mask (good high-frequency loss) for bump localisation and Sn-Pb electroplating followed by solder reflow for ball-shape formation. The bump diameter is 200 μm. The proposed technology concept was already verified by the LIPS project partners for applications up to 20 GHz [196–199]. During this work, a considerable process extension was achieved, allowing its use for applications at 60 GHz. The main issues were:

1. The selection of dielectric materials and establishing of a reliable lamination process. The following factors, determining a potential applicability of a given dielectric, have to be taken into account: moisture absorption, thermo-mechanical properties, surface roughness, dielectric permittivity, loss tangent and layer thickness.

2. Scaling down the minimum feature size of the metallisation pattern with the process tolerances appropriate for small wavelengths in V-band. Of importance are the optimisation of the electroplating process for the proper definition of a metal track profile and the minimisation of a metal strip thickness for higher etching accuracy.

**Figure 4.1:** Concept of the plastic SMT compatible packaging technology.
4.1. Process development

Some of the most important aspects of the process development according to the above-mentioned main objectives will be discussed in this section.

4.1.1. Base material selection

Two materials were considered as a carrier substrate: silicon and copper. Copper shows very good thermal conductivity, whereas silicon has good thermal properties and can be easily machined by dry etching.

The lamination of a 625 μm thick silicon with different resins, evaluated within the project, resulted in an excellent substrate flatness, required for further processing. Unfortunately, some preliminary analyses and measurements of the transmission characteristics of the entire module mounted with solder balls on a second-level interconnect PWB (200 μm thick Rogers 4003) showed some ripples beyond 50 GHz. They are due to parasitic surface wave modes excited in the silicon carrier at the PWB-module transition (see Sec. 4.1.5 for a detailed problem analysis). Finally, the silicon wafer was replaced with a 150 μm thick Microlam 410 resin laminated on the top of a 450 μm copper carrier. It resulted in good substrate flatness and surface uniformity, required for the next processing steps and proper mounting of the chip bare dies in cavities.

4.1.2. Laminate material selection

The appropriate combination of dielectric permittivity and layer thickness are some of the most important factors, when choosing a material for a laminated dielectric layer. From the point of view of the MMIC perturbation and the required metal pattern accuracy, the relative dielectric constant should be as close to one as possible. Furthermore, considering the electrical performance of microstrip interconnects (supposed to be used within the module)
at mm-wave frequencies, the corresponding polymer thickness, defining the microstrip line height, should be a trade-off between the line loss on one side and the high-frequency behaviour of the transmission line discontinuities, including the connecting vias, on the other side (see Sec. 3.1.2). Performing a similar analysis to that reported in Sec. 3.1.2 for the BCB film leads to the observation that the preferred combination of dielectric constant and thickness values for the laminated layer seems to be 2.5–4 and 50–70 \( \mu m \).

The achievable polymer surface roughness is another important factor to be considered for mm-wave applications. It defines the roughness and the line edge definition for the subsequent plating process (see Sec. 3.1.3). For dielectric loss minimisation, the dielectric loss tangent is a parameter of interest. Also, the moisture absorption and thermo-mechanical properties have to be carefully analysed. A proper match of coefficients of thermal expansion (CTE) between the copper and the dielectric layers increases the reliability of the via formation and allows to decrease the strip conductor thickness. The latter lead to better etching accuracy.

From the processing point of view, the chosen materials have to be compatible with the laser drilling process. Some other factors related to the lamination process have to be also investigated. These are the appropriate flatness after lamination (required for further processing), the bonding strength between the adhesive film and the copper layer, and the bonding strength between the laminate and the adhesive film. The lamination was performed using a vacuum press with a separately optimised lamination cycling for each of the considered dielectric layers. Within this work, the following laminate build-ups were evaluated for their electrical and thermo-mechanical properties:

1. Speedboard C/ Espanex NSC - 38 \( \mu m \)/25 \( \mu m \)
2. Speedboard C/ Arlon 85NT - 38 \( \mu m \)/25 \( \mu m \)
3. Speedboard C - 50 \( \mu m \)
4. Speedboard C/ Biac LCP - 38 \( \mu m \)/25 \( \mu m \)
5. Microlam 410/ Biac LCP - 38 \( \mu m \)/25 \( \mu m \)
6. Microlam 410/ Espanex NSC - 38 \( \mu m \)/25 \( \mu m \)
7. Microlam 410/ Arlon 85NT - 38 \( \mu m \)/47 \( \mu m \)
8. Microlam 410 - 63 \( \mu m \)
The first material for each of the mixed dielectric layers is an adhesive film and the other is a laminate. A detailed description of the electrical and physical parameters for each of the listed materials can be found in [117]. After numerous processing and characterisation experiments, two dielectric buildups, Microlam 410/Biac LCP and Speedboard C/Biac LCP, were chosen as the ultimate solutions.

Speedboard C from Gore is an epoxy resin coated on micro-porous expanded PTFE. Its main advantages are the excellent dielectric properties ($\varepsilon_r = 2.57$, $\tan \delta = 0.004$ @ 10 GHz) and high transition temperature of $220^\circ$. Its basic disadvantage is high CTE coefficient in all directions (60 ppm/$^\circ C$). Microlam 410 prepreg from Gore is also an epoxy resin coated on micro-porous expanded PTFE. It shows good electrical properties ($\varepsilon_r = 3.4$, $\tan \delta = 0.008$ @ 10 GHz), high transition temperature (225$^\circ$) and excellent isotropic CTE of 19 ppm/$^\circ C$ matched to copper. The excellent surface planarity and uniformity of this material allows fine lines and spacing.

Biac LCP is a liquid crystal polymer (LCP) laminate from Gore. LCP is a thermoplastic polymer much cheaper than LTCC and teflon-like dielectrics. It shows an excellent combination of electronic, thermo-mechanical and chemical properties. Its mechanical stability is a few times higher than that of a polyimide. Its low CTE (16 ppm/$^\circ C$) matches that of a copper metallisation, providing low warpage after etch. High moisture and chemical resistance enhance LCP performance to aggressive operating conditions [200]. LCP absorbs 50 to 100 times less moisture than polyimide films, resulting in very stable electrical and mechanical properties in the normal and humid environments [201]. Because of its low moisture permeability, the packages can be made hermetic without heavy expensive housing. It shows a high modulus and a high transition temperature (335$^\circ$). Since LCP is low-cost, it can be suitable in all applications where FR4 is used nowadays. LCPs have not been widely used because of the weak interaction with copper. A substantially roughened copper foil surface is used in conventional lamination process in order to improve the bonding strength, being unacceptable for mm-wave frequencies. Recently, surface activated bonding based on a surface cleaning process has been performed to achieve a strong bonding with a simultaneous low surface roughness of 100 nm [201]. Furthermore, the high transition temperature of LCP requires the use of prepregs as bonding ply.

In [202, 203], it was reported that LCP provides a nearly constant dielectric constant and a low dielectric loss tangent over a wide frequency range ($\varepsilon_r = 3$, $\tan \delta = 0.004$ @ 35 GHz). However, the potential of LCP for microwave and mm-wave circuits still has not been fully explored from a material characterisation standpoint. This was one of the objectives of this work.
4.1.3. Metal pattern

The plating process applied in this work consists of surface cleaning and sputtering of a 200 nm chromium and 500 nm copper, followed by a 9.5 μm electrolytic copper [204]. The measured rms roughness of both Biac LCP and copper surfaces taken by Atomic Force Microscopy (AFM) are 440 nm and 620 nm, respectively (see Fig. 4.2). Such values exceed the skin depth of 0.2–

![Surface roughness of Biac LCP (R_q=440 nm) (a) copper on Biac LCP (R_q=620 nm) (b).](image)

0.3 μm in copper at 60–80 GHz, leading to practically doubled ohmic losses due the longer effective current path. In that aspect, the process still needs some improvement. Nevertheless, the reported roughness for the underlying Biac LCP dielectric surface in combination with the use of electro-deposited resist equipment resulted in a fine pitch patterning and a very good line profile definition, the parameter of interest for loss minimisation at mm-wave frequencies (see Sec. 3.1.3 and Fig. 6.20 for a more detailed line loss analysis at mm-wave frequencies). A very low ±1μm in-panel variation of a metal strip thickness was achieved. Line widths and gap spaces larger that 50 μm were very well reproducible with an in-panel variation below ±2.5 μm. Even lines as narrow as 25 μm were rather properly defined with a width variation of ±2.5 μm along their length.

The frequency-dependent line loss and line effective permittivity (see Figs. 4.4 and 4.5) for different microstrip lines on the Speedboard C/Biac LCP and Microlam 410/Biac LCP build-ups were de-embedded up to 100 GHz using the technique presented in Sec. 5.2. The attenuation of the lines on the composite Speedboard C/Biac LCP dielectric is within 0.1–0.12 dB/mm at 60 GHz for the considered strip width range of 30–485 μm. Similar loss for a
4.1. Process development

A wide range of strip widths is a result of the non-uniform current density distribution at the frequencies of interest (see Sec. 3.1.3). Dielectric loss, ohmic loss for a perfect mirror-like surface and a finite surface roughness contribute equally to the overall line attenuation. The corresponding loss at 60 GHz for the Microlam 410/Biac LCP lines is in the range of 0.13–0.17 dB/mm, being higher than that for the Speedboard C/Biac LCP build-up due to the larger loss tangent of Microlam 410. Both configurations show practically no high-frequency dispersion within the entire measured frequency band.

Figure 4.3: A set of 30–485 μm wide microstrip lines on the Speedboard C/Biac LCP build-up.

4.1.4. Formation of vias and cavities

The formation of vias and cavities in the dielectric layers is achieved with an excimer laser, whereas for the silicon substrate by dry etching. For the chosen dielectric thickness of 63 μm, a reliable drilling with an aspect ratio equal to one can be performed. The minimum required via pad overlap was found to be about 30 μm.

MMIC bare dies, supported with a few μm thick BCB layer on top for an active surface protection, and decoupling capacitors are supposed to be located in cavities (see Fig 4.6). They are glued with a 50 μm thick electrical conductive adhesive. A high positioning accuracy of ± 10 μm was achieved, suitable for repeatable chip-module transitions at 60 GHz. A space around the components and in the ground vias is filled with an epoxy resin to arrive at the required planarisation before the lamination process.
Figure 4.4: De-embedded line loss for a set of 30–485 \( \mu \text{m} \) wide microstrip lines on: (a) 38 \( \mu \text{m} / 25 \mu \text{m} \) Microlam 410/Biac LCP ('MLam/Biac') (b) 38 \( \mu \text{m} / 25 \mu \text{m} \) Speedboard C/Biac LCP ('Spd/Biac') build-up. A 10 \( \mu \text{m} \) thick copper strip was used in both configurations.

4.1.5. Chip-to-PWB transition

A chipset from UMS, realised in the microstrip configuration, is chosen to be used for the 60 GHz technology demonstrators within the frame of the
Figure 4.5: De-embedded line effective permittivity for a set of 30–485 μm wide microstrip lines on: (a) 38 μm/25 μm Microlam 410/Biac LCP ('Mlam/Biac') (b) 38 μm/25 μm Speedboard C/Biac LCP ('Spd/Biac') build-up. A 10 μm thick copper strip was used in both configurations.

LIPS project [117]. The performance of a chip-to-module transition is not critical because of the tight tolerances of the developed process and the small dimensions of the vias connecting chip bare dies with transmission lines on
If the module is supposed to be mounted on a PWB and guide 60 GHz signals, the performance of the module-PWB transition is of importance. This is due to the substantially higher manufacturing tolerances of a standard printed circuit board and considerable dimensions of this transition, that has to be compatible with a standard SMT process (bump diameter of 200 \( \mu \text{m} \)). Because of these large dimensions and low thickness (63 \( \mu \text{m} \)) of the laminated dielectric layer on the module, the proper match to a microstrip feed on the underlying PWB (200 \( \mu \text{m} \) thick Rogers 4003) needed the conversion to the CPW mode. This, in turn, required local removal of the ground plane on the module (separating the laminated layer from the underlying silicon substrate), resulting in parasitic surface mode excitation within the silicon substrate. This led to a new substrate build-up, shown in Fig. 4.7, composed of a copper heat sink with a 150 \( \mu \text{m} \) thick Microlam 410 resin laminated on
the top (see Sec. 4.1.1). This modified setup replaces the CPW mode with the conductor-backed CPW (CBCPW) and allows proper isolation between inputs and outputs of MMIC chips.

**Figure 4.7: The final build-up of the developed M-HDI technology.**

Furthermore, it was noticed that after the module mounting on PWB, a parasitic parallel-plate mode created by the proximity of both ground-planes on the module and on the Rogers 4003 substrate resulted in a resonant behaviour around 60 GHz. The use of shielding via holes populated in the circuit board and electrically connected with the ground plane on the module by means of solder bumps could easily remove this parasitic effect.

Full-wave 3D HFSS simulations of the entire single transition between a packaged MMIC and a microstrip transmission line on a 200 μm thick Rogers 4003 PWB substrate, performed in [205], show that a return loss better than 20 dB up to 70 GHz is possible.

The simulated performance comparison between a 60 GHz LNA (UMS 9512) bare die and that packaged in a module and mounted on a 200 μm thick Rogers 4003 PWB substrate is shown in Fig. 4.8. In this analysis, the characteristics of the active unit, represented by the measured S-parameters, are connected with those of the transition path. The latter are simulated using HFSS. The worst-case tolerance analysis for the mounted module shows no noticeable differences in the performance. The critical process parameters for this analysis are: track etching accuracy on the PWB and dielectric thickness tolerances for both the module and PWB.

### 4.2. Summary

In this chapter, the development process of an interconnection and packaging MCM-L technology for the integration of mm-wave modules in V-band
was presented. The developed process is supposed to be used for the realisation of SMT compatible single die packages and standard functional units (consisting of several chip bare dies and some optional integrated passive components), allowing efficient implementation of a modular approach for mm-wave systems. The achieved tight design rules should allow integration of numerous passive elements. However, structures demanding very narrow line widths and spacings are still out of reach.

A large variety of process and material characterisation experiments were performed to arrive at the appropriate material combination and reliable process flow with tolerances appropriate for the wavelengths in V-band. Of special importance was the use of the recently developed liquid crystal polymer laminate *Biac LCP* from *Gore*. This material shows excellent thermo-mechanical and chemical properties, making it an ideal candidate for low-cost packaging schemes. During this work, it was verified that *Biac LCP* allows fine pitch metal patterning and shows outstanding dielectric properties up to 100 GHz, comparable to ceramics. A broad set of the measured thin microstrip lines demonstrates practically no high-frequency dispersion within the measured frequency range of 1–100 GHz and the line loss as low as 0.1 dB at 60 GHz.

**Figure 4.8:** Simulated performance comparison between a 60 GHz LNA bare die (UMS 9512) and a packaged module mounted on a single-layer 200 μm thick Rogers 4003 board (Courtesy of Thales RT).
Part II

De-embedding and extraction techniques
Precise S-parameter VNA measurements at the component level are essential to obtain designs operating within their target specifications. As a result, reliable calibration techniques have to be developed in order to accurately characterise the performance of the new developed MCM technologies. Relying on an off-wafer calibration only, performed by means of a standard calibration substrate with CPW calibration standards, can lead to erroneous measurement results at mm-wave frequencies, specifically if the transmission line topology used is different from the CPW configuration. Therefore, accurate on-wafer S-parameters measurements require an on-wafer calibration to be performed. Typically, it needs an exact knowledge of the behaviour of the calibration standards supposed to be used. An accurate fabrication of on-wafer calibration standards is, however, difficult with non-precision processing techniques (low-cost technologies) or if the goal is the characterisation of a newly estab-
lished technology. As a result, many practical measurements rely on off-wafer calibrations only. However, for accurate on-wafer measurements at mm-wave frequencies, a technique is necessary to account for differences between off- and on-wafer feed structures, and substrate permittivities.

In this chapter, such a technique is implemented using a principle of the calibration-comparison method [1, 2]. It performs a full TRL or LRRM off-wafer calibration and a second-tier on-wafer calibration based on the measurement technique of two transmission lines of different lengths [3, 4] (see Sec. 5.2). Moreover, a set of procedures for de-embedding the characteristic impedance of different planar transmission line configurations, validated at mm-wave frequencies, was developed: CPW lines (Sec. 5.3), tapered-fed CPW lines (Sec. 5.3.3), CBCPW lines (Sec. 5.4) and microstrip lines (Sec. 5.5). In Sec. 5.6, the methods used within this work for characterisation of multi-port networks with two-port VNA measurements are presented.

5.1. Introduction

The non-idealities of the measurement system are quantified using mathematical error correction models. The purpose of the calibration procedure is to solve for the error coefficients in these models. This is done by measuring some calibrations standards.

Basic two-port calibration procedures have an 8-term error model, which requires the measurements of at least 3 calibration standards. A modified 12-term model is able to take into account cross-talk and effects of impedance discrepancies at the RF switches in the VNA test set [78]. At the expense of an increased number of measurements (at least 5 measurements) a 16-term error model can also be used [79]. It is able to account for electromagnetic coupling between the probe heads. For practical measurements, however, the distance between the probe tips vary according to the layout of the measured DUT, such that the actual coupling will differ from the value measured during calibration [80].

Several calibration techniques are routinely available in the network analyser: SOLT, TRL, LRM or LRRM.

SOLT (Short-Open-Load-Thru)

This is the most popular calibration technique, especially on the lower microwave frequency band. The short, open, load and thru standards are measured to calculate the 12-term error model. The method assumes that the behaviour of the calibration structures is completely known. For this purpose,
a model is defined in a calibration kit for the set of measurement probes and the calibration substrate used. The accuracy with which the impedance parameters of the lumped-element standards are known can be questionable at mm-wave frequencies [81, 82].

**TRL (Thru-Reflect-Line) / LRL (Line-Reflect-Line)**

Basically, three standards are measured to characterise the 8-term error model: a thru, a line and a reflect [83]. The thru may also be replaced by a line (LRL) [84, 85]. In this calibration, the reference impedance of the S-parameters is set to the characteristic impedance of the thru/line and an identical reflect is assumed at both ports. The method allows for self-calibration, meaning that an exact knowledge of the line characteristic impedance and frequency behaviour of the reflect standard are not required because they are eliminated from the calculations. The multi-line TRL technique [86] uses multiple, redundant transmission lines to minimise the effect of random errors such as caused by imperfect contact repeatability.

**LRM (Line-Reflect-Match) / LRRM (Line-Reflect-Reflect-Match)**

The LRM technique [87] requires the measurement of a 50 Ω load, a thru and a reflect. The basic algorithm is the same as for TRL: the load can be considered as an infinitely long transmission line while the thru has a zero length. This implies that the reference impedance of the measurements is set by the 50 Ω load. As in the TRL calibration, the reflect does not have to be accurately known. The zero-length assumption for the thru standard implies that the reference planes are located in the centre of the thru after calibration. They are shifted towards the probe-tips by subtracting a time-delay corresponding to one half of the electrical length of the thru, resulting in the neglected line losses.

The LRRM technique is a variation of LRM. Both the open and short standards are used but the load is measured on only one of the two ports. This way, discrepancies in the measured load impedance at both ports can be avoided [88]. Small inconsistencies in calibration due to these discrepancies are thus removed. A technique to automatically determine the load’s inductance was also presented in [88]. An accurate model for the load’s impedance is thus not needed, making this technique very suitable for mm-wave calibrations.

Each of the above-mentioned calibration techniques has a number of advantages and disadvantages. From the operator’s point of view, SOLT and
LRM are preferable as they require a limited number of measurements for broadband calibrations. They have also better contact repeatability as a constant probe-probe distance is used. TRL and LRM rely less on the accurate knowledge of the reflects which makes them better suited for high-frequency on-wafer measurements. The characteristic impedance of a transmission line at high frequencies, used as a reference in TRL technique, is easier to predict than the behaviour of a lumped resistor with frequency-dependent resistance, reactance and possibly influenced by substrate effects.

Concluding, techniques based on self-calibration are superior at mm-wave frequencies as they rely less on the exact knowledge of the calibration standards. Because of this reason, LRRM with an automatic determination of the load inductance and LRL techniques were used within this work for the measurements within 1–100 GHz frequency band.

5.2. Two-tier calibration for 2-port on-wafer measurements

As previously outlined, accurate on-wafer S-parameter measurements require the calibration standards to be accurately known. However, accurate on-wafer fabrication of calibration standards is difficult because our goal is the characterisation of the MCM technologies under development. This means that SOLT calibration standards with the a priori known performance are automatically rejected. Also LRM calibration, requiring an accurate 50 Ω load, is not well suited for the technologies of interest. For the MCM-D build-up, sheet resistance wafer-to-wafer tolerances do not support the required accuracy without trimming. In case of the considered MCM-L build-ups, a special resistive layer is not taken into consideration. A set of calibration standards based on TRL technique can only be taken into account. However, for the lower frequencies, the short, open and 50 Ω load standards are still required.

As a result of the above mentioned issues, many practical measurements rely on off-wafer calibrations only using a calibration substrate from an external manufacturer. Usually, a contact geometry for the probe-tips, a substrate material (losses and permittivity) or the line topology differ between a calibration substrate and a measured DUT. A technique is needed to account for these differences as they deteriorate the measurement accuracy [89, 90], especially at mm-wave frequencies. If these effects are compensated for, the accuracy is comparable to an on-wafer calibration [89].

Taking the above into account, a calibration technique was implemented using a principle of the calibration-comparison method [1, 2]. First, a full TRL or LRRM off-wafer calibration and a second-tier TL on-wafer calibration are performed. Next, a set of error boxes, denoted as $R_A$ in Fig. 5.1, relating both
calibrations is found. These trans-wafer error boxes describe not only any contact-pad parasitics unaccounted for by the reference calibration but also an impedance transformation that translates the reference impedance to that of the second-tier TL calibration (equal to the characteristic impedance of the measured on-wafer lines). The reduction of a number of on-wafer standards to only two transmission lines of different lengths can be achieved under assumption that the trans-wafer error boxes, $R_A$, on both sides of the measured on-wafer lines are equal after the initial off-wafer calibration [3, 4].

![Block diagram of a two-port measurement problem.](image)

**Figure 5.1:** Block diagram of a two-port measurement problem.

With reference to Fig. 5.1, we will apply the THRU and LINE connections at the reference planes for DUT (in case of a THRU standard both DUT reference planes are in the middle of a THRU) and measure the S-parameters for these two cases at the measurement planes. The error boxes are characterised by S-matrix $[S_r]$ and alternatively by the chain matrix $A_r, B_r, C_r, D_r$. The measured S-parameter matrices for the THRU and LINE connections are denoted as $[T]$ and $[L]$, respectively. By symmetry of the error boxes we have $T_{11} = T_{22}, L_{11} = L_{22}$ and by reciprocity $T_{21} = T_{12}, L_{21} = L_{12}$. Solving for a propagation constant in terms of the measured S-parameters of both line standards we arrive at:

$$e^{-\gamma l} = \frac{L_{12}^2 + T_{12}^2 - (T_{11} - L_{11})^2}{2L_{12}T_{12}} \pm \sqrt{\frac{[L_{12}^2 + T_{12}^2 - (T_{11} - L_{11})^2]^2 - 4L_{12}^2T_{12}^2}{2L_{12}T_{12}}}$$

(5.1)

$$S_{22r} = \frac{T_{11} - L_{11}}{T_{12} - L_{12}e^{-\gamma l}}$$

(5.2)

$$S_{11r} = T_{11} - S_{22r}T_{12}$$

(5.3)

$$S_{12r} \cdot S_{21r} = T_{12}(1 - S_{22r})$$

(5.4)
The choice of sign can be determined by the requirement that the real and imaginary parts of \( \gamma l \) to be positive. The parameter \( l \) denotes the length difference between THRU and LINE standards, which is usually accurately defined by metallisation process resolution. Knowing \( l \), it is possible to determine \( \gamma = \alpha + j\beta \) or, equivalently, the line loss and line effective permittivity. The de-embedded \( \gamma \) values are precisely defined for the line standards arbitrarily mismatched with a measurement system. They are also unaffected by the ill-conditioned S-parameter matrix equations at frequencies corresponding to the multiples of half a wavelength on a line. It means that LINE standards can be arbitrary long, thus, providing sufficiently high accuracy level for the de-embedded line loss and line effective dielectric constant. To develop the above equations no model for the feed transition was needed. The only parameter to be known at this de-embedding stage is the length difference, \( l \), between both line standards.

5.2.1. Measurement results and accuracy considerations

The measurements were performed using a HP8510XF VNA. The system was initially calibrated with both TRL and LRRM techniques using alumina calibration substrate from Cascade Microtech. A 150 \( \mu \)m pitch probes connected to the VNA by means of a waveguide were used. To estimate the accuracy and repeatability of our measurement set-up, several measurements on different microstrip lines realised in the developed BCB-based MCM-D process were performed. The error due to a finite contact repeatability during the two-step calibration and the differences due to the selected off-wafer calibration method were estimated by performing independent LRRM and TRL calibrations on different days. Fig. 5.2 shows the de-embedded 50 \( \Omega \) microstrip line loss for different calibrations. It can be noticed that all values differ only by at most 0.017 dB within the entire measured frequency range.

The next figure, Fig. 5.3, presents the measured insertion and return loss of a 3.2 mm long 50 \( \Omega \) microstrip line in the MCM-D technology after the off-wafer and after the proposed two-step on-wafer calibrations. Substantial differences in the de-embedded values can be observed for both cases. The insertion and return losses of the single probe-tip-microstrip transition (see Fig. 5.21(a) for the transition geometry) unaccounted for by off-wafer calibration are 0.2 dB and 22 dB at 60 GHz, and 0.65 dB and 17 dB at 100 GHz. Thus, without the second de-embedding step, the measured line loss can be substantially overestimated and the performance characteristics of different functional elements considerably changed.

Using the presented technique, line losses and line effective permittivities
5.2. Two-tier calibration for 2-port on-wafer measurements

Figure 5.2: De-embedded line loss of a 50 Ω (111 μm wide) microstrip line standard on a 45 μm thick BCB film for different calibrations (accuracy and repeatability of the 2-step de-embedding procedure).

Figure 5.3: Measured insertion and return losses of a 3.2 mm long 50 Ω microstrip line standard on a 45 μm thick BCB film after off-wafer calibration and after 2-step on-wafer de-embedding procedure.

for different line configurations (CPW, CBCPW and microstrip lines) were extracted. The appropriate line and feed structure geometries together with the de-embedded values can be found in the following sections focused on the line characteristic impedance de-embedding and in Chapters 3, 4 and 6.
5.3. Characteristic impedance de-embedding for CPW lines

The presented two-step de-embedding procedure, similarly to the TRL method, results in a consistent calibration with reference impedance equal to the characteristic impedance of the measured lines. S-parameter measurements taken with respect to an unknown, frequency-dependent reference impedance can be difficult to interpret and their corresponding impedance parameters cannot be found. Furthermore, since characteristic impedance can be complex in the presence of loss, the measured reflection coefficients of the passive device may exceed unity in magnitude. If characteristic impedance can be determined, a complex impedance transformation [91] (see Appendix A) can be used to shift to a constant, real reference impedance, thus eliminating these S-parameter anomalies.

5.3.1. Methods and limitations

In [92], the characteristic impedance of CPW lines on non-dispersive, lossless substrates is indirectly determined from the extracted propagation constant using the TRL algorithm. This method assumes that the frequency dependence of the line capacitance per unit length, $C$, is weak and may be well approximated by its DC value, $C_{DC}$. The method assumes perfect conductors and that the line conductance per unit length, $G$, is negligible, which is not true for lossy substrates. A procedure to determine $C_{DC}$ from the measurements of a line DC resistance or from the reflection coefficient of a small resistive load is proposed in [93] but it only holds for low frequencies.

A common way of measuring the characteristic impedance of planar transmission lines is presented in [94]. Its value is determined by comparing the S-parameters of a single line measured by probe-tip calibration to those of an ideal transmission line. As a result, the influence of the feed transition discontinuity at the probe-tips is not taken into account. This leads to large errors, particularly when the measured line impedance substantially differs from the calibration reference impedance.

In [95], the characteristic impedance of lossy silicon lines is determined by direct measurements of all feed parasitics. The method needs 5 additional measurements, besides the calibration standards. It neglects the parasitics induced by differences between the measurement and the calibration wafer, thus leading to non-optimal results.

In the calibration comparison method [96], the feed trans-wafer error boxes, obtained by comparison of a second calibration (with unknown characteristic impedance) to a reference calibration, were used for the character-
istic impedance de-embedding. The basic algorithm [93] could only account for the reference plane shift and impedance transformation at the probe-tips. In [89, 90], the differences in both the feed pad geometry and the substrate permittivity between on- and off-wafer calibrations were taken into account, modelling them by a residual shunt capacitance at the probe-tips. Approximate methods, based on a separate characterisation of the contact pads, were given to estimate this capacitance value.

An alternative treatment of the error boxes measured by the calibration comparison method was presented in [1, 2]. In this approach, any arbitrary large shunt contact pad capacitance and conductance can be accounted for, without any additional contact pad characterisation.

A procedure accounting for a presence of any parasitic shunt admittance and any parasitic series impedance at the probe-tips (for example due to a step-in-width between probe and strip) was presented in [4]. The applied error box model is of a lumped nature and it consists of a shunt admittance \((G + j\omega C)\) and a series impedance \((R + j\omega L)\). The accuracy of the model relies on an accurate position of the probe tips and it requires that the probe over-travel is approximately known. A complementary method accounting for a shunt parasitic admittance and a reference plane shift (for example due to the imprecise probe-tips positioning) was also given by the same authors [97].

5.3.2. Problem formulation

All of the above reviewed de-embedding procedures calibrate the measured standards to the probe-tips. This involves a reference plane shift from its initial position in the middle of the \(THRU\) to the probe-tips. The location of a new reference plane is not exactly known because of a limited positioning precision of the probe-tips and a distributed nature of the feed transition.

We present a procedure that does not involve the reference plane shift in the calibration procedure [98, 99]. On the contrary, due to a different formulation of the problem, it enables extraction of the equivalent reference plane position. Equivalent means that it is the exact physical position of the probe tips if the parasitic series impedance at the probe-tips can be neglected. Otherwise, it is different from its physical counterpart by some transmission line length, modelling this effect. Using a concept of the equivalent reference plane position also makes the method less sensitive to the probe positioning errors. The presented problem formulation also results in explicit analytical formulas relating the de-embedded line characteristic impedance and the elements of an error box model to the measured parameters of the calibration standards.

The first step of the procedure treats the entire \(THRU\) as a connection of
only two error boxes with their chain matrices denoted as $A_r, B_r, C_r, D_r$. Using the chain matrix formulation for the measured THRU ($A_T, B_T, C_T, D_T$) and \textit{LINE} ($A_L, B_L, C_L, D_L$) standards, relating them to those of the error box and of the transmission line section, one is able to solve for $A_r^2 Z_0, B_r$ and $C_r$ matrix elements without any modelling of the feed discontinuity:

$$A_r^2 Z_0 = -4(\cosh\gamma l \cdot B_T - B_L \pm \sqrt{\Delta}) \over 8\sinh\gamma l$$  \hspace{1cm} (5.5)

$$\Delta = 16[(\cosh\gamma l \cdot B_T - B_L)^2 - \sinh^2\gamma l \cdot B_T^2]$$  \hspace{1cm} (5.6)

$$B_r = \frac{B_T}{2} \sqrt{\frac{Z_0}{\psi}}$$  \hspace{1cm} (5.7)

$$C_r = \frac{A_T - 1}{B_T} \sqrt{\frac{\psi}{Z_0}}$$  \hspace{1cm} (5.8)

where $A_r^2 Z_0$ is denoted by $\psi$. $D_r = (1 + B_r C_r)/A_r$ from the reciprocity condition for the passive error box model. The values of $A_T B_T C_T D_T$ and $A_L B_L C_L D_L$ are known from the measured S-matrices of both line standards and the known reference impedance of a measurement system. $l$ is the length difference between \textit{LINE} and \textit{THRU} standards, known from the first part of the calibration procedure (see Sec. 5.2).

The equivalent circuit of the applied error box model is shown in Fig. 5.4. Its chain matrix representation has the form:

$$\begin{bmatrix}
\cosh\gamma d_1 & Z_0 \sinh\gamma d_1 \\
\frac{1}{Z_0} \sinh\gamma d_1 + j \cdot \tanh\gamma d_2 \cdot \cosh\gamma d_1 & \cosh\gamma d_1 + j \cdot \tanh\gamma d_2 \cdot \sinh\gamma d_1
\end{bmatrix}$$  \hspace{1cm} (5.9)
5.3. Characteristic impedance de-embedding for CPW lines

$d_1$ denotes a distance between the equivalent probe-tip reference plane and the middle of the *THRU* line. $d_2$ denotes a length of the open-ended stub connected in front of the equivalent probe-tip reference plane. It reflects the difference in shunt admittances of the on- and off-wafer open stubs seen at the probe-tips. It can be noticed that $A_r^2Z_0$ is equal to $Z_0\cosh^2 \gamma d_1$ for the applied error box model. The proper choice of root in Eq. 5.5 is made by $\Re(A_r^2Z_0) \geq 0$. Calculating $B_r/A_r$ leads to the solution for $d_1$:

$$\tanh \gamma d_1 = \frac{B_r}{2\psi}$$

(5.10)

$$d_1 = \frac{1}{\gamma} \arctan \left( \frac{B_r}{2\psi} \right)$$

(5.11)

Then $Z_0$ and $d_2$ take the form:

$$Z_0 = \frac{B_T}{2\cosh \gamma d_1 \cdot \sinh \gamma d_1}$$

(5.12)

$$\tanh \gamma d_2 = -j \cdot Z_0 \left( \frac{A_T - 1}{B_T} - \frac{B_T}{2Z_0^2 \cosh^2 \gamma d_1} \right) =$$

$$-j \cdot Z_0 \left( \frac{A_T - 1}{B_T} - \frac{\tanh \gamma d_1}{Z_0} \right)$$

(5.13)

Note that, only $A_r$ and $B_r$ are involved in the $Z_0$ extraction process and that, due to the shunt-series nature of the model, they are not affected by the shunt part. This means that the shunt part, practically representing the feed geometry behind the probe-tips, does not influence the extraction process. As a result, it does not need to be modelled and can be of any arbitrary complexity.

Furthermore, as the real and imaginary parts of the possible series impedance at the probe-tips (modelled by an excess transmission line length) are forced to be related in the same manner as the real and imaginary parts of the transmission line parameters of the measured line standards, the procedure is slightly limited in a precise determination of the series resistance at the probe-tips. In practice, it is, however, of lesser importance because the series impedance is dominated by the reactive behaviour and the influence of the real part can be neglected. The additional shunt admittance introduced by this excess transmission line length is automatically taken into account by the appropriate modification of $d_2$ or, equivalently, of the shunt admittance at the probe-tips.
Applying the chain matrix formulation of the de-embedding problem to the classical approach calibrating the measured standards to the probe-tips, a similar set of equations for $A_r^2 Z_0$, $B_r$, and $C_r$, independent of any probe-tip discontinuity model, can be developed [98–100]:

$$A_r^2 Z_0 = \frac{\Delta^2}{2 \left( \chi \pm \sqrt{\chi^2 - \Delta^2} \right)}$$  \hspace{1cm} (5.14)

$$B_r^2 = \frac{Z_0}{2} \left( \chi \pm \sqrt{\chi^2 - \Delta^2} \right)$$  \hspace{1cm} (5.15)

$$C_r = \frac{A_L - \cosh \gamma l_{(LINE)} - \frac{B_r \sinh \gamma l_{(LINE)}}{Z_0 A_r}}{2B_r \cosh \gamma l_{(LINE)} + A_r Z_0 \sinh \gamma l_{(LINE)} + \frac{B_r^2 \sinh \gamma l_{(LINE)}}{Z_0 A_r}}$$  \hspace{1cm} (5.16)

$$\chi = A_r^2 Z_0 + \frac{B_r^2}{Z_0} = \frac{B_L \cosh \gamma l_{(THRU)} - B_T \cosh \gamma l_{(LINE)}}{\cosh \gamma l_{(THRU)} \cdot \sinh \gamma l_{(LINE)} - \cosh \gamma l_{(LINE)} \cdot \sinh \gamma l_{(THRU)}}$$  \hspace{1cm} (5.17)

$$\Delta = 2A_r B_r = \frac{B_L \sinh \gamma l_{(THRU)} - B_T \sinh \gamma l_{(LINE)}}{\cosh \gamma l_{(LINE)} \cdot \sinh \gamma l_{(THRU)} - \cosh \gamma l_{(THRU)} \cdot \sinh \gamma l_{(LINE)}}$$  \hspace{1cm} (5.18)

$A_r B_r C_r D_r$ represents the chain matrix of the error box after reference plane shift to the probe-tips. $l_{(THRU)}$ and $l_{(LINE)}$ represent line lengths between probe-tips on both sides of the line standards for $THRU$ and $LINE$, respectively. They are related by the previously defined length difference $l = l_{(THRU)} - l_{(LINE)}$.

To model the probe-tip discontinuity, the state-of-the-art lumped element model from [4] (see also Sec. 5.3.1), shown in Fig. 5.5, was applied in this case. The feed transition is represented by a cascade connection of a shunt admittance and a series impedance. The chain matrix representation of the
model is of the form:

\[
\begin{bmatrix}
1 & R_p + j\omega L_p \\
G_p + j\omega C_p & 1 + (R_p + j\omega L_p)(G_p + j\omega C_p)
\end{bmatrix}
\]  
(5.19)

It can be noticed that \( A_r \) is equal to 1, allowing to de-embed the measured line characteristic impedance from Eq. 5.14. Proper choice between two roots is provided by \( Re(Z_0) > 0 \). Then \( B_r \) takes the form \( \Delta / 2 \) and leads to the formulas for the series parasitic inductance and resistance:

\[ L_p = Im\left(\frac{\Delta}{4\pi f}\right) \]  
(5.20)

\[ R_p = Re\left(\frac{\Delta}{2}\right) \]  
(5.21)

\( C_p \) and \( G_p \) are found from \( C_r \):

\[ C_p = Im\left(\frac{C_r}{2\pi f}\right) \]  
(5.22)

\[ G_p = Re(C_r) \]  
(5.23)

5.3.3. Characteristic impedance de-embedding for tapered-fed CPW lines

In many practical situations, a geometry of the CPW lines supposed to be measured does not match a pitch of the probe-tips. Very wide interconnect lines are often used for ohmic loss minimisation. For MMIC’s, contrary to the previous case, very narrow lines may be required. In both cases, the measurement standards are fed by a short transmission line section matching the probe-pitch (pad) followed by a tapered line. A general layout of a wide CPW line standard with such a feed structure is shown in Fig. 5.6.
In this section, a technique allowing characteristic impedance determination of the tapered-fed CPW lines is presented [98, 100]. The procedure consists of two steps. In the first (see Fig. 5.6), the influence of only probe-tip discontinuity is de-embedded by means of any of the two models from Sec. 5.3.2. For this purpose, an additional CPW line pair with the same geometry as the feeding pads for the taper-fed lines is required. If more taper-fed line geometries are measured, they can be fed by the same geometry of the probe-tip contact pad and, thus, share the same model for the probe-tip discontinuity. De-embedding the influence of the tapered feed and determination of the characteristic impedance of the measured lines is performed in the second step (see Fig. 5.6).

If the reciprocal feed discontinuity can be assumed to be symmetric with a sufficient accuracy, then it is possible to de-embed the line characteristic impedance from the chain matrices of the two measured line standards without modelling the internal structure of this discontinuity. Using the symmetry condition $A_r = D_r$ for the chain matrix representation of the reciprocal error box and combining it with Eqs. 5.15-5.16 for $A_r, B_r$ and $C_r$ elements from Sec. 5.3.2 results in the following formula for the line characteristic impedance:

$$\frac{1}{Z_0} = \frac{2\eta}{\Delta^2} \left( 1 + \frac{A_L - \cosh\gamma l_{LINE} - \sinh\gamma l_{LINE}/\Delta}{2\cosh\gamma l_{LINE} + \sinh\gamma l_{LINE} \cdot (\eta/\Delta + \Delta/\eta)} \right)$$  \hspace{1cm} (5.24)

$$\eta = \chi \pm \sqrt{\chi^2 - \Delta^2}$$  \hspace{1cm} (5.25)

A proper choice of the root for $\eta$ is provided by $Re(Z_0) > 0$.

The developed formulation can be of special interest for mm-wave frequencies because by not using any fixed model it is able to take into account
the distributed nature of the feed transition. This feature will be used for modelling a taper feed in the second step of the de-embedding procedure. At this extraction stage, $A_T B_T C_T D_T$ and $A_L B_L C_L D_L$ matrices refer to the line standards after de-embedding the influence of probe-tip discontinuities in the first step of the procedure. Similarly, $l_{THRU}$ and $l_{LINE}$ represent the lengths of the intrinsic line standards between tapers on both sides.

If the ratio of a centre strip to a ground-ground spacing of a CPW line, defined by its characteristic parameter $'K'$, is chosen to be the same for both the feed and the taper-fed lines being measured, the characteristic impedances of both are theoretically the same. In practice, they will be different but still close to each other. The difference may come from the influence of a finite metallisation thickness, a strip profile and processing inaccuracies. As long as the characteristic impedances of both lines are close to each other, even an electrically long taper can be seen as an element approaching a uniform transmission line section with uniformly distributed parasitics and, thus, modelled as symmetric. The electrical length of the tapers connecting CPW lines of considerably different characteristic impedances should be made short enough to provide the validity of a symmetric model (approximation by a single transmission line section with dimensions in between the connecting CPW lines).

### 5.3.4. Experimental results

Different CPW lines on a 500 $\mu$m thick fused silica and a 45/500 $\mu$m thick BCB/Rogers 4003 MCM-D substrate (see Sec. 3.6) were characterised to verify the developed set of de-embedding procedures. The lines were realised in the FGCPW configuration. All measurements were performed in the conductor-backed environment created by the presence of a metal chuck in the probing station. Such a probing arrangement is prone to couple to the MSL modes (see Appendix B) and, thus, it requires a careful choice of the line geometries. Considering the coupling effects to surface waves, the conductor-backed measurement setup results in the lowest critical frequency for the $TM_0$ surface wave mode located around 100 GHz for both considered dielectric substrates (see Eq. B.1).

The geometries of the considered lines are gathered in Table 5.1. An overall width of the 240/30/400 $\mu$m lines on fused silica does not allow to match a 150 $\mu$m pitch of the probe tips. As a result, they are fed by a cascade of a 300 $\mu$m long, 150/20/300 $\mu$m wide, line followed by a 350 $\mu$m long tapered line. Such a wide geometry was intentionally chosen to verify the developed two-step procedure for characteristic impedance de-embedding for the tapered-fed lines. The relatively long taper was chosen to demonstrate the
Table 5.1: Finite-Ground CPW (FGCPW) line geometries on a 500 μm thick fused silica and on a 45/500 μm thick BCB/Rogers 4003 substrate. (A 5 μm thick silver and a 4 μm thick gold was used as a metal conductor for the lines on a fused silica and on a BCB/Rogers 4003 build-up, respectively).

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Fused silica</td>
<td>47</td>
<td>100</td>
<td>14</td>
<td>200</td>
<td>128</td>
</tr>
<tr>
<td>Fused silica</td>
<td>48</td>
<td>150</td>
<td>20</td>
<td>300</td>
<td>190</td>
</tr>
<tr>
<td>Fused silica</td>
<td>49</td>
<td>240</td>
<td>30</td>
<td>400</td>
<td>300</td>
</tr>
<tr>
<td>BCB/Rogers4003</td>
<td>65</td>
<td>120</td>
<td>20</td>
<td>250</td>
<td>160</td>
</tr>
<tr>
<td>BCB/Rogers4003</td>
<td>70</td>
<td>114</td>
<td>23</td>
<td>250</td>
<td>160</td>
</tr>
<tr>
<td>BCB/Rogers4003</td>
<td>95</td>
<td>70</td>
<td>45</td>
<td>250</td>
<td>160</td>
</tr>
<tr>
<td>BCB/Rogers4003</td>
<td>130</td>
<td>26</td>
<td>67</td>
<td>250</td>
<td>160</td>
</tr>
</tbody>
</table>

potential of the symmetric error box model to catch the distributed nature of the tapered transition. The de-embedded results for this line will be analysed separately at the end of this section.

To investigate the influence of a bottom metal plane on transmission characteristics of the FGCPW lines on a fused silica substrate, the quasi-static line effective permittivities and characteristic impedances of both 100/14/200 μm and 150/20/300 μm line geometries were calculated for both an air-suspended and a conductor-backed substrate [101, 102]. The differences in εreff and Z₀ between both configurations were found to be below 0.002 and 0.3 Ω, respectively, indicating weak influence of a bottom ground-plane on transmission line properties of infinitely long lines. Even smaller differences were obtained for the BCB/Rogers 4003 lines.

Furthermore, a total line width (sum of a centre strip, two slots and two ground planes) is kept below half a wavelength in the substrate up to 142 GHz, 95 GHz and 67 GHz for the 100/14/200 μm, 150/20/300 μm and 240/30/400 μm wide lines, respectively.

The lengths of THRU and LINE standards for the lines on a fused silica are 2 mm and 11.5 mm, respectively. These long lines are chosen to investigate the intensity of mode coupling effects, being length dependent. Both lengths differ by 9.5 mm, resulting in a minimum phase difference of 30° at 2 GHz and, thus, allowing wide-band de-embedding. At the same time, a phase difference of 180°, known to lead to some instabilities in the de-embedded characteristic impedance values, occurs at multiples of 10 GHz. The lengths of THRU and LINE standards for the BCB/Rogers 4003 lines were chosen to be 1 mm and 1.9 mm, respectively, to allow smooth resonance-free characteristic impedance de-embedding within the entire measured frequency band of 1-100 GHz.

The de-embedded line effective permittivity, line loss, characteristic
5.3. Characteristic impedance de-embedding for CPW lines

Impedance and equivalent parameters, $d_1$ and $d_2$, of the distributed feed error box model (see Fig. 5.4) for both FGCPW geometries on a fused silica substrate are shown in Figs. 5.7, 5.8 and 5.9. The smooth monotonic form of $\varepsilon_{\text{reff}}$, line loss and $Z_0$ indicate no sign of parasitic coupling up to 110 GHz and 95 GHz for the 100/14/200 $\mu$m and 150/20/300 $\mu$m wide lines,

![Figure 5.7](image1)

**Figure 5.7:** De-embedded $\varepsilon_{\text{reff}}$ and line loss of the 100/14/200 $\mu$m and 150/20/300 $\mu$m wide FGCPW lines on a fused silica substrate from Table 5.1.

![Figure 5.8](image2)

**Figure 5.8:** De-embedded (a) $\text{Re}(Z_0)$ and (b) $\text{Im}(Z_0)$ of the 100/14/200 $\mu$m and 150/20/300 $\mu$m wide FGCPW lines on a fused silica substrate ('HFSS' curves correspond to the HFSS calculated values. The surface impedance formulation for conductors was used in the simulations. This approach is fully justified, as the skin depth in a 5 $\mu$m thick silver strip is equal to 1.4 $\mu$m at 2 GHz).
respectively. The wider geometry starts showing some instabilities of the de-embedded parameters around 100 GHz, close to the previously calculated half a wavelength in the substrate. Local non-monotonic behaviour of the de-embedded equivalent lengths, $d_1$ and $d_2$, and $Z_0$ are a result of long line standards leading to multiple half a wavelength phase differences between LINE and THRU.

The de-embedded lengths, $d_1$ and $d_2$, are approximately constant over the entire frequency range. Their equivalent average values in the measured band are $d_1 = 972 \mu m$, $d_2 = -10 \mu m$ and $d_1 = 959 \mu m$, $d_2 = -5.5 \mu m$ for the 100/14/200 $\mu m$ and 150/20/300 $\mu m$ lines, respectively. As the probes were located 25 $\mu m$ from the physical beginning of the lines, $d_2$ can be seen as a shunt capacitance. Its equivalent average value in the measured band is $-2.56$ fF and $-1.4$ fF for both lines, respectively. Its values are negative because the dielectric permittivity of an alumina calibration substrate is higher than that of a fused silica. Comparing $d_1$ with its physical counterpart (975 $\mu m$), it can be seen that they differ only by 3 $\mu m$ for the 100/14/200 $\mu m$ lines. It means that the parasitic series inductance is negligible in this case. The same length for the wider lines differs by 16 $\mu m$ from its physical counterpart, indicating higher value of the parasitic series inductance.

For comparison purposes, the de-embedding procedure with the lumped probe-tip-line transition model from Fig. 5.5 was performed for the same line geometries. The de-embedded characteristic impedances were practically the
same as the exact probe-tips position read was performed. The de-embedded element values of the equivalent error box model averaged in the measured band are gathered in Table 5.2: The \( L_p \) values show good agreement with the corresponding parameter, \( d_1 \), accounting for the parasitic series impedance at the probe-tips. For the 100/14/200 \( \mu \text{m} \) lines, \( L_p \) is negligible but its value is about 8 times larger for the 150/20/300 \( \mu \text{m} \) lines and it justifies the reference plane shift in the distributed model with an automatic detection of the reference plane position. The origin of the parasitic inductance can be regarded as a different step-in-width discontinuity at the probe-tips for the on- and off-wafer calibration standards, resulting mainly from different line ground-ground spacings.

### Table 5.2: De-embedded average element values of the equivalent lumped error box model from Fig. 5.5 for the 100/14/200 \( \mu \text{m} \) and 150/20/300 \( \mu \text{m} \) wide FGCPW lines on a fused silica substrate.

<table>
<thead>
<tr>
<th>Line conf.</th>
<th>( R_p ) [( \Omega )]</th>
<th>( L_p ) [( \mu \text{H} )]</th>
<th>( G_p ) [( \mu \text{S} )]</th>
<th>( C_p ) [( \text{fF} )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>100/14/200</td>
<td>-0.81</td>
<td>-0.48</td>
<td>50</td>
<td>-2.8</td>
</tr>
<tr>
<td>150/20/300</td>
<td>-0.57</td>
<td>-3.95</td>
<td>21</td>
<td>-3.11</td>
</tr>
</tbody>
</table>

Figure 5.10: De-embedded (a) \( \text{Re}(Z_0) \) and (b) \( \text{Im}(Z_0) \) of the FGCPW lines on a BCB/Rogers 4003 MCM-D substrate from Table 5.1.

Comparing the de-embedded values of the parasitic shunt capacitance for both models, differences in the determined values can be observed. Where does this difference come from? The parasitic series inductance represented by some additional transmission line length in \( d_1 \) cannot be considered sep-
Figure 5.11: De-embedded lengths, (a) $d_1$ and (b) $d_2$, of the distributed feed error box model from Sec. 5.4 for the FGCPW lines on a BCB/Rogers 4003 MCM-D substrate.

arately without noticing that a transmission line section also contributes to some shunt capacitance according to its equivalent LC model. This value is automatically subtracted from the shunt open-end capacitance at the probe-tips by the de-embedding algorithm with an automatic detection of the reference plane. In a result, the shunt capacitances at the probe tips are different for both models. The influence of $R_p$ and $G_p$ resistive elements is negligible for the considered line set.

Figs. 5.10, 5.11 and 5.12 present the de-embedded $Z_0$ values of different FGCPW lines on a BCB/Rogers 4003 build-up (see Table 5.1) and the corresponding equivalent element values for both distributed and lumped error box model. A smooth behaviour of the extracted parameters can be noticed, being partly a result of the appropriately short line standards used in the de-embedding process. It can be seen that the $d_2$ values are relatively large if compared to those for the fused silica lines. This is a result of high characteristic impedances of the measured lines and even larger difference in the substrate dielectric permittivity between the alumina calibration substrate and the BCB/Rogers 4003 build-up.

Concerning $d_1$, it can be noticed that almost the same series inductance at the probe-tips for the all measured BCB/Rogers 4003 build-up lines (similar step-in-width discontinuity) is modelled by different shift in the reference plane position, $d_1$, relative to its physical position (475 $\mu$m). This is a result of different characteristic impedances of the measured lines.

The loss, line effective permittivity and characteristic impedance of the
5.3. Characteristic impedance de-embedding for CPW lines

Figure 5.12: De-embedded (a) $C_p$ and (b) $L_p$ elements of the lumped feed error box model from Sec. 5.5 for the FGCPW lines on a BCB/Rogers 4003 MCM-D substrate.

Figure 5.13: De-embedded (a) line effective permittivity and (b) line loss of the taper-fed 240/30/400 μm wide FGCPW lines on a fused silica substrate.

taper-fed 240/30/400 μm wide lines on a fused silica substrate de-embedded using the two-step procedure from Sec. 5.3.3 are shown in Figs. 5.13 and 5.14. Instable behaviour of the line loss can be observed beyond 60 GHz, indicating some coupling phenomena. This is due to a large lateral line geometry approaching or exceeding half a wavelength in the substrate beyond 60 GHz. The same effect can be observed in the de-embedded $Im(Z_0)$, responsible for loss (see Fig. 5.14(a)). The real part of $Z_0$ (Fig. 5.14(b)) shows a good
correspondence with the HFSS calculated values up to about 60 GHz.

![Graph](image)

**Figure 5.14:** De-embedded (a) $Re(Z_0)$ and (b) $Im(Z_0)$ of the taper-fed 240/30/400 μm wide FGCPW lines on a fused silica substrate. (HFSS’ curve corresponds to the HFSS calculated values. The surface impedance formulation for a 4 μm thick gold conductor was used in the simulations).

### 5.4. Characteristic impedance de-embedding for CBCPW lines

In many practical situations, microwave circuits have a backside ground plane, creating leakage from the CPW line to the parallel-plate waveguide modes. Furthermore, box-type resonances occur due to a finite substrate size. A practical method of avoiding the resonances can be a reduction of the top ground plane widths, leading to a Finite-Width CBCPW (Conductor-Backed CPW). It supports, however, zero cut-off microstrip-like (MSL), or coplanar microstrip (CPM) [103–106], and coupled slotline modes (see Appendix B). Connecting the top and bottom ground planes suppresses both modes but it can lead to parasitic waveguide modes. If the widths of the top ground planes are appropriately small, the resulting waveguide modes are cut-off. Though the leakage mechanism for this line configuration was recognised, only the propagation characteristics were thoroughly analysed. The CBCPW characteristic impedance de-embedding was only reported in [107], where the propagation constant and characteristic impedance were not smooth functions of frequency and showed anomalous behaviour. The measurements were based on a single line only and a probe-tip discontinuity was not taken into account, limiting de-embedding precision. The authors in [108, 109] noticed that a
waveguide mode with magnetic wall symmetry, which can be viewed as a perturbed $TE_{10}$ mode of the rectangular waveguide (see Fig. 5.15), starts to propagate at some frequency and that is responsible for the anomalies observed in [107].

![Figure 5.15: The dominant CPW (CBCPW) mode (top figure) and the perturbed $TE_{10}$ waveguide mode with magnetic wall symmetry [108, 109] (bottom figure) in an overmoded FW-CBCPW line with shorted top and bottom ground-planes. (With respect to a standard CPW without conductor-backing, the dominant CPW, or rather CBCPW mode, in a conductor-backed substrate shows the increased electric field lines passing through the substrate. For very thin substrates, its characteristics resemble more those of classical microstrip lines than the classical CPW lines).](image)

5.4.1. Experimental results

The de-embedding procedure of the complex propagation constant and characteristic impedance with an automatic detection of the equivalent reference plane position from Sec. 5.3.2 was applied for the FW-CBCPW line configuration [110].

The FW-CBCPW lines on three different build-ups were designed:

- thin-film BCB (left drawing in Fig. 5.16) with $\epsilon_r = 2.64$, $h = 44$ µm, $t_{Au} = 4.5$ µm
- 2-layer mixed laminate Speedboard C/BIAC LCP (right drawing in Fig. 5.16) with $\epsilon_{r1(2)} = 2.57$ (3), $h_{1(2)} = 39.5$ (24.5) µm, $t_{Cu} = 11$ µm
- 2-layer mixed laminate Speedboard C/Espanex NSC (right drawing in Fig. 5.16) with $\epsilon_{r1(2)} = 2.57$ (3.95), $h_{1(2)} = 37$ (24.5) µm, $t_{Cu} = 12$ µm
The line strip and slot widths, \( w \) and \( s \), are: 102/72 \( \mu m \), 118/62 \( \mu m \) and 120/58 \( \mu m \) for the three build-ups, respectively. The top GND widths, \( g \), are 300 \( \mu m \) and the lengths of line standards are 1, 1.9, 4.6 mm for the all considered build-ups. Vias \( (w_v = 60 \mu m) \) shorting the top and bottom GND were applied along the lines and at their both ends. For a 3-layer thin-film BCB build-up, only staircased grounding vias could be applied.

During measurements, the probe tips (150 \( \mu m \) pitch) were positioned behind the shorting vias at the inputs (see Fig. 5.17). Full-wave modal 2D HFSS simulations (at the excitation port) were performed to find the cut-off frequencies of the first 2 meaningful waveguide modes. The waveguide is modelled as a shielded structure with a large separation to the top and side walls of the shield. The first waveguide mode is the mentioned perturbed \( TE_{10} \) (see Fig. 5.15) and it can be seen as the counterpart of the MSL (CPM) mode (see Appendix B for the mode definition) in the line configuration with floating top ground planes. The second one with electric wall symmetry \[109\] resembles the coupled slotline mode in the same configuration. 2D HFSS simulations show that both modes are evanescent below 115 GHz, 102 GHz and 99 GHz for the considered BCB and laminate lines, respectively. The coupling between the dominant CPW mode (see Fig. 5.15) and the \( TE_{10} \)-like waveguide mode is of importance because both show the magnetic wall symmetry and field overlap. The coupling to the other can be neglected due to its electric wall symmetry.

The de-embedded parameters: \( \varepsilon_{ref} \), line loss, \( Z_0 \), \( d_1 \) and \( d_2 \), transformed onto the equivalent shunt capacitance at the probe-tips, are shown in Figs. 5.18 and 5.19. A smooth behaviour of \( \varepsilon_{ref} \), line loss and \( d_1 \) up to 100 GHz can be observed, with one exception at 90 GHz for the BCB lines. This is a result of the standing wave created between too sparsely located vias on a 1.9 mm long line (see Fig. 5.17(a)). The de-embedded shunt capacitance values cover the range of 3–10 \( fF \). The physical reference plane positions (counted from the middle of a 1 mm long \( THRU \) standard) for the three

![Figure 5.16: Cross-sectional view of the FW-CBCPW lines on a thin-film BCB (left figure) and on a 2-layer mixed laminate build-up (right figure).](image)
configurations are 370, 345, 355 μm, respectively. The corresponding \( d_1 \) values are 395, 360 and 368 μm. The difference is due to the series inductance at the probe tips. The extracted and simulated \( Re(Z_0) \) correspond well up to 80 GHz. Beyond this frequency, anomalous behaviour is observed, which can be attributed to the sparsely located vias for the BCB lines. The laminate lines, however, show the same phenomenon above 80 GHz, although their de-embedded complex propagation constants are smooth up to 100 GHz and 2D HFSS simulations show that waveguide modes are evanescent.

To investigate this effect, 3D HFSS modal simulations were performed. The lines were excited by the dominant CPW mode field pattern at the port and the internal structure assumed absorbing boundary conditions. Fig. 5.20 presents the reflection coefficients associated with the CPW mode, \( S^{CPW}_{11} \), and the \( TE_{10} \) waveguide mode, \( S^{HM}_{11} \), at the input port of the 1.9 mm long BCB line from Fig. 5.17(a). The following configurations are shown: the one with lateral shorting metal wall along the line, ‘shorted wall’, with 2 shorting vias along the line (corresponding to the measured configuration), ‘2 shorting vias’, with 6 vias and with 9 vias along the line length, ‘6 shorting vias’ and ‘9 shorting vias’. A return loss associated with the dominant CPW mode is practically the same for all the configurations, excluding the case with 2 shorting
vias, wherein the too sparsely located vias cause the already mentioned standing wave effects at 90 GHz. In this case, the \( TE_{10} \) waveguide mode power seen at the input around this frequency is even higher (\( S_{11}^{HM} = -22 \, dB \)) than that for the dominant CPW mode. The line configuration with the shorting metal wall along the line length should result in an infinitely small waveguide mode power at the input port because the mode is evanescent and there are no discontinuities along the line. The simulations indicate a return loss of 55 dB at 100 GHz for this mode and its finite value is a result of an imperfect
5.4. Characteristic impedance de-embedding for CBCPW lines

Figure 5.19: De-embedded and HFSS calculated: (a) $\text{Re}(Z_0)$ (b) $\text{Im}(Z_0)$ of the BCB (‘BCB’), Speedboard C/BIAC LCP (‘Speed – Biac’) and Speedboard C/Espanex NSC (‘Speed – Esp’) FW-CBCPW lines. (‘Extr’ and ‘Simul’ stand for the de-embedded and simulated values, respectively. The surface impedance formulation for the metallisation layers was assumed in simulations.)

match between the field patterns at the port and within the internal structure. For the configurations with a finite number of vias along the line length, the $TE_{10}$ complex waveguide mode power seen at the input port is considerably higher and increases with frequency towards its cut-off frequency. The simulated line configuration with 9 vias along the line results in $S_{11}^{HM} = -45 \, \text{dB}$ at 100 GHz, substantially lower than for the line with 2 shorting vias (corresponding to the measured configuration). The periodically changing top GND geometry (by inserted vias) seems to provoke field distribution disturbances along the line length, resulting in an increased $TE_{10}$ complex waveg-
Figure 5.20: HFSS simulated reflection coefficients of a 1.9 mm long BCB FW-CBCPW line standard. (The simulated structure was excited by the dominant CPW mode field pattern. $S_{11}^{CPW}$ denote the reflection coefficient associated with the dominant mode power, whereas $S_{11}^{HM}$ correspond to the perturbed $TE_{10}$ mode power at the input ports. The simulation results for 4 different line configurations are shown: ‘shorted wall’ - with lateral shorting metal wall along the line, ‘2 shorting vias’ - with 2 shorting vias along the line (corresponding to the measured configuration), ‘6 shorting vias’ and ‘9 shorting vias’ - with 6 vias and with 9 vias along the line length.)

The designed FW-CBCPW lines represent very critical case for the parasitic influence of the waveguide modes as the ratio of line width (ground-ground spacing) to line height is very high (3.8–5.6). For the lower ratio, the field overlap between the dominant CPW and the $TE_{10}$ waveguide mode is mini-
5.5. Characteristic impedance de-embedding for microstrip lines

A technique for de-embedding the microstrip line characteristic impedance is presented in this section [100, 111]. It is based on the measurement technique of two on-wafer microstrip line standards, similarly to the other de-embedding procedures from previous sections. The feed structure for the microstrip line standards (see Fig. 5.21(a)) consists of a coplanar pad configuration suited for the GSG probe-tip contact and of a via-based transition to the microstrip configuration. The procedure consists of two steps, similarly to that applied for the taper-fed CPW lines (see Sec. 5.3.3). In the first step, the probe-tip discontinuity is de-embedded by means of the technique with an automatic detection of the equivalent reference plane position from Sec. 5.3.2. For this purpose, an additional FW-CBCPW line pair with the same geometry as the feeding pads for the microstrip lines is required. If more microstrip line geometries are measured, they can be fed by the same probe-tip contact pad geometry and, thus, share the same model for the probe-tip discontinuity. De-embedding the influence of a FW-CBCPW-microstrip
line transition and determination of the microstrip characteristic impedance is performed in the second step using the chain matrices of the two measured microstrip line standards, THRU and LINE. The lengths of the intrinsic microstrip lines embedded between both FW-CBCPW-microstrip transitions should be taken in the second de-embedding step for THRU and LINE. Similarly, $A_TB_T C_T D_T$, $A_L B_L C_L D_L$ and $A_r B_r C_r D_r$ matrices should represent these intrinsic lengths and the FW-CBCPW-microstrip transition, respectively.

Three different modelling approaches were verified for the via-based FW-CBCPW-microstrip transition: lumped CGLR model from Sec. 5.3.2 (cascade of a shunt admittance and a series impedance), LRCG model (cascade of a series impedance and a shunt admittance) and symmetric error box model from Sec. 5.3.3. A comparison between different models reveals essential differences in the de-embedded characteristic impedance values and shows that the latter model outperforms the others at mm-wave frequencies.

### 5.5.1. FW-CBCPW-microstrip transition modelling

The accuracy of the de-embedding procedure for different models of a FW-CBCPW-microstrip transition was tested using the simulation data from HFSS for microstrip lines on a 100 μm thick GaAs substrate, a 60 μm and a 15 μm thick BCB film on a 250 μm thick alumina substrate (MCM-D). THRU and LINE standards embedded between FW-CBCPW-microstrip transitions only were simulated (Fig. 5.21(b)), being equivalent to the second de-embedding step. The simulated structures were excited by the CPW dominant mode at the ports (see Fig. 5.15 for mode definition). The FW-CBCPW feed pad dimensions (strip width, slot width and ground plane width), microstrip line geometries and other features of the simulated structures are collected in Table 5.3. The THRU and LINE standard lengths are 1 mm and 11 mm, and 1 mm and 6 mm, for the BCB and GaAs substrates, respectively. Two grounding vias (30 μm in diameter) per top finite ground plane were used. The feed pad geometries correspond approximately to 50 Ω impedance lines.

The de-embedded equivalent capacitances and inductances of the lumped error box model (see Fig. 5.5 for model definition) of the FW-CBCPW-microstrip line transition for different simulated microstrip line standards from Table 5.3 are depicted in Fig. 5.22. Fig. 5.23(a) shows $Z_0$ of the 50 μm and 30 μm wide microstrip lines on a 100 μm thick GaAs substrate de-embedded by means of the lumped (‘GCRL’) and symmetric (‘SYMM’) models. It can be noticed that the frequencies at which the equivalent capacitance in the lumped model and the corresponding de-embedded $Z_0$ start decreasing
Table 5.3: Line and feed geometries of the HFSS simulated microstrip line standards on a 100 μm thick GaAs substrate, a 60 μm and a 15 μm thick BCB film on a 250 μm thick alumina substrate (MCM-D). (The names of the structures listed in the table correspond to the names used in Figs. 5.22 and 5.23.)

<table>
<thead>
<tr>
<th>Structure name</th>
<th>Substrate</th>
<th>Feed geometry [μm] (strip width/slot width/ground width)</th>
<th>Microstrip width [μm]</th>
<th>Structure description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs-50μm</td>
<td>GaAs</td>
<td>54/53/200</td>
<td>50</td>
<td>FW-CBCPW feed</td>
</tr>
<tr>
<td>GaAs-30μm</td>
<td>GaAs</td>
<td>54/53/200</td>
<td>30</td>
<td>FW-CBCPW feed</td>
</tr>
<tr>
<td>GaAs-76μm</td>
<td>GaAs</td>
<td>54/53/200</td>
<td>76</td>
<td>FW-CBCPW feed</td>
</tr>
<tr>
<td>GaAs-120μm</td>
<td>GaAs</td>
<td>54/53/200</td>
<td>120</td>
<td>FW-CBCPW feed</td>
</tr>
<tr>
<td>BCB-t-60μm</td>
<td>BCB</td>
<td>140/50/230</td>
<td>140</td>
<td>60 μm thick BCB, FW-CBCPW feed</td>
</tr>
<tr>
<td>BCB-t-15μm</td>
<td>BCB</td>
<td>44/18/230</td>
<td>44</td>
<td>15 μm thick BCB, FW-CBCPW feed</td>
</tr>
</tbody>
</table>

Figure 5.22: De-embedded equivalent (a) capacitance and (b) inductance of the lumped error box model of the FW-CBCPW-microstrip line transition for different microstrip line standards from Table 5.3.

their values are in a very good agreement. $Z_0$ extracted using the symmetric model of the FW-CBCPW-microstrip transition, contrary to the previous case, performs very well in the entire frequency range. The de-embedding errors associated with the lumped model increase for longer transitions and for high permittivity substrates. Fig. 5.23(b) presents a set of characteristic impedances of different line geometries from Table 5.3 de-embedded using the symmetric feed error box model.

In the MCM-D technology, a microstrip ground metallisation (buried be-
Figure 5.23: (a) $Z_0$ of the 50 $\mu$m and 30 $\mu$m wide microstrip lines on a 100 $\mu$m thick GaAs substrate de-embedded by means of the lumped (‘GCRL’) and symmetric (‘SYMM’) models. (b) $Z_0$ of different microstrip lines from Table 5.3 de-embedded using the symmetric model. (‘direct’ denotes $Z_0$ directly calculated with the 2D HFSS port simulations.)

tween an alumina substrate and a BCB film) can be patterned. In this case, different possible feeding topologies for a 140 $\mu$m wide microstrip line standard on a 60 $\mu$m thick BCB were considered, reflecting different measurement configurations (see Table 5.4):

1. ‘BCB-t-60$\mu$m’ - microstrip line fed by a FW-CBCPW line, similarly to the previously considered GaAs and BCB microstrip lines

2. ‘CPW’ - finite-ground CPW feed (FGCPW). A 60 $\mu$m thick BCB is located on an infinitely thick alumina substrate

3. ‘Subst.GND’ - finite-ground CPW feed (FGCPW). A 60 $\mu$m thick BCB is located on a backside metallised 250 $\mu$m thick alumina (typical measurement setup)

4. ‘Subst.air’ - finite-ground CPW feed (FGCPW). A 60 $\mu$m thick BCB is located on an air-suspended 250 $\mu$m thick alumina (measurement setup suspended in the air).

The all listed configurations were modelled in the HFSS solver by applying the appropriate boundary conditions. Some results of these investigations are gathered in Fig. 5.24. It can be noticed that only $Re(Z_0)$ de-embedded applying the symmetric feed error-box model to the FW-CBCPW-microstrip
Table 5.4: Different feed topologies of the HFSS simulated 140 μm wide microstrip line standard on a 60 μm thick BCB film. The BCB film is span on a 250 μm thick alumina substrate (MCM-D). A microstrip ground plane is buried between the BCB film and the alumina substrate. (The names of the structures listed in the table correspond to the names used in Fig. 5.24.)

<table>
<thead>
<tr>
<th>Structure name</th>
<th>Substrate</th>
<th>Feed geometry [μm]</th>
<th>Microstrip width [μm]</th>
<th>Structure description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCB-t-60μm</td>
<td>BCB</td>
<td>140/50/230</td>
<td>140</td>
<td>60 μm thick BCB, FW-CBCPW feed</td>
</tr>
<tr>
<td>CPW</td>
<td>BCB</td>
<td>200/20/300</td>
<td>140</td>
<td>60 μm thick BCB, FGCPW feed, infinitely thick alumina substrate</td>
</tr>
<tr>
<td>Subst_GND</td>
<td>BCB</td>
<td>200/20/230</td>
<td>140</td>
<td>60 μm thick BCB, FGCPW feed, 250 μm thick alumina substrate backside metallised</td>
</tr>
<tr>
<td>Subst_air</td>
<td>BCB</td>
<td>200/20/230</td>
<td>140</td>
<td>60 μm thick BCB, FGCPW feed, 250 μm thick air-suspended alumina substrate</td>
</tr>
</tbody>
</table>

5.5. Characteristic impedance de-embedding for microstrip lines

Figure 5.24: De-embedded characteristic impedance of the HFSS simulated 140 μm wide microstrip line standards on a 60 μm thick BCB film for different feed configurations: (a) Re(Z₀) (b) Im(Z₀). (‘SYMMA’ and ‘GCRL’ correspond to the Z₀ values de-embedded applying the lumped and symmetric feed error-box models to the FW-CBCPW-microstrip line transition (BCB-t-60μm in Table 5.4). ‘CPW’, ‘Subst GND’ and ‘Subst Air’ stand for Z₀ de-embedded using the symmetric error box model for different FGCPW feed structures (see Table 5.4). ‘direct’ denotes Z₀ directly calculated with the 2D HFSS port simulations.)
5.5.2. Experimental results

The implemented 2-step feed structure for the measured microstrip line standards on a 45 μm thick BCB film is shown in Fig. 5.21(a). In this feed transition, a probe-tip-FW-CBCPW line discontinuity is separated from a FW-CBCPW-microstrip transition by a 170 μm long FW-CBCPW line section considered in Sec. 5.4.1. The grounding via paths are realised by means of a 3-layer staircased configuration (see Fig. 5.25(a)) because stacked vias are impossible for the considered MCM-D technology (see Sec. 3.2). The THRU standard is 1 mm long. Two different 1.8 mm and 4.2 mm long LINE standards are used, depending on the frequency range. The parasitics of the probe-tip-FW-CBCPW feed and transmission parameters, $Z_0$ and $\gamma$, of the reference FW-CBCPW line are de-embedded in the first step (see Figs. 5.16 and 5.19 for the line cross-section and its de-embedded $Z_0$ and $\gamma$).

![Figure 5.25: (a) A 3-layer staircased via grounding path of the FW-CBCPW-microstrip transition for the measured microstrip line standards on a 45 μm BCB film (via diameter is 60 μm). (b) Two- and single-step probe-tip-microstrip feed transition for the BCB microstrip lines.](image)

Characteristic impedances of different microstrip lines on a 45 μm BCB film de-embedded using the lumped and symmetric models of the FW-CBCPW-microstrip transition are presented in Fig. 5.26. It can be noticed that both models result in the similar $Re(Z_0)$ values up to 30 GHz. Beyond this frequency, the real parts of $Z_0$ extracted using the lumped model start falling down. They are apart by a few Ω at 80 GHz from the corresponding values for the symmetric model. Above 80 GHz, the de-embedded characteristic impedances should not be considered because of deteriorating influence of the too sparsely located grounding vias along the reference FW-CBCPW
5.5. Characteristic impedance de-embedding for microstrip lines

Figure 5.26: $Z_0$ of the 295 μm (25 Ω), 111 μm (50 Ω) and 67 μm (75 Ω) wide microstrip lines on a 45 μm BCB film de-embedded using the lumped ('Lmp') and symmetric ('Sym') models of the FW-CBCPW-microstrip transition: (a) $Re(Z_0)$ (b) $Im(Z_0)$ (symmetric error box model only). (The in-house extracted BCB dielectric permittivity is found to be in the range of 2.635–265 up to 100 GHz (see Sec. 6.6). The lines are covered with a 5 μm thick BCB passivation and a copper strip is 1 μm thick).

The de-embedded equivalent capacitance and inductance of the lumped error box model of the FW-CBCPW-microstrip line transition for the BCB microstrip line standards from Fig. 5.26 are shown in Fig. 5.27. Although, as shown before, the model is not well suited for mm-wave frequencies, it gives an impression about the order of parasitics introduced by the transition. It can be noticed that both inductance and capacitance is high and frequency dependent because of a long and complicated 3-vias grounding path (Fig. 5.25(b)). The highest values are for a 25 Ω line as a result of an additional considerable step-in-width discontinuity at the feed transition created by a 300 μm wide microstrip line and a 102 μm wide centre strip of the feeding FW-CBCPW line. The corresponding parasitic element values of the lumped error box model for the previously simulated line standards (see Fig. 5.22) with the four stacked grounding vias per transition are substantially lower and show
Figure 5.27: De-embedded equivalent (a) capacitance and (b) inductance of the lumped error box model of the FW-CBCPW-microstrip line transition for the BCB microstrip line standards from Fig. 5.26.

weaker frequency dependence.

The symmetric model performs well in the entire measured frequency range even for the implemented transition with long grounding paths because its distributed nature can be caught properly without any modelling effort.

Fig. 5.28 presents the characteristic impedances of the 50 Ω and 35 Ω BCB microstrip lines de-embedded using the lumped and symmetric models applied to the classical single- and the proposed two-step probe-tip-microstrip feed transitions from Fig. 5.25(b). The former forces the use of a single step de-embedding procedure as it does not allow a separation between the probe-tip-FW-CBCPW and the FW-CBCPW-microstrip line transitions. None of the models applied to this feed topology results in the required accuracy at mm-wave frequencies. Furthermore, the lumped model performs substantially worse than the symmetric for this single-step transition.

5.6. Multi-port measurements

In this work, several multi-port structures were measured. Multi-ports are conventionally characterised by measuring between 2 ports while the unused ports are terminated with 50 Ω loads. When only one DUT is available, several orthogonal probe pair measurements occur. The conventional calibration techniques available in the VNA (SOLT, LRM and TRL) assume that the THRU standard is a short straight transmission line. It has been shown [112]
5.6. Multi-port measurements

Figure 5.28: Characteristic impedance of the 111 μm (50 Ω) and 193 μm (35 Ω) wide microstrip line standards from Fig. 5.26 de-embedded using the lumped (‘Lmp’) and symmetric (‘Sym’) models applied to the classical single- (‘One step’) and the proposed two-step (‘Two steps’) probe-tip-microstrip feed transitions from Fig. 5.25(b).

that the orthogonal behaviour should be taken into account if accurate calibration is required. The SOLR technique [113] can be used in this case as it only makes use of the reciprocal property of the thru. The main drawback of this technique is that extra software is required and that the short, open and load standards have to be accurately known, which is difficult at high mm-wave frequencies.

When additional space is available, the measurement problem of multi-port elements can be solved by repeating the structure several times on-wafer. Two in-line probes are obtained by placing an additional bend at the orthogonal port. The influence of this bend can be afterwards removed from the measurements. In this approach, one assumes that all on-wafer standards are identical. This assumption, however, requires very precise manufacturing technology and it can be fulfilled for the MCM technologies considered in this work. Additionally, to minimise the influence of the in-panel process tolerances, the measured structures are places next to one another. This measurement technique was applied in this work. The frequency compensated terminations were realised on-wafer.

Power reflected from mismatched loads on the auxiliary ports can result in significant measurement errors. These errors will become larger with an increase of the mismatch errors and a number of ports. As a result, all
the terminations have to be characterised individually and their influence removed using a matrix renormalisation process. Such a procedure allowing a de-embedding of the influence of any kind of termination was also developed within this work.

5.6.1. Characterisation of the reciprocal 3- and 4-ports

For characterisation of reciprocal 3- and 4-ports, a method similar to that in [114] was developed. For the text space reasons, only a detailed formulation for a 3-port is presented. The DUT is measured 3 times with the orthogonal port terminated with 3 different reflects (in our case: load, open, short). The reflects are also measured using the same calibration. As only in-line measurements are required, the system needs to be calibrated only once, an orthogonal calibration technique is not required and the compensation for the non-ideal terminations is directly included.

The general formulation of a 3-port passive S-parameter matrix is:

\[
\begin{bmatrix}
S_{11} & S_{12} & S_{13} \\
S_{12} & S_{22} & S_{23} \\
S_{13} & S_{23} & S_{33}
\end{bmatrix}
\]  \hspace{1cm} (5.26)

When the third port is terminated with 3 different reflects, \(\Gamma_l\) \((l = 1 – 3)\), the resulting 2-port S-parameters are given by

\[
S_{11}^{\Gamma_l} = S_{11} + \frac{S_{13}^2}{\Gamma_l - S_{33}}
\]  \hspace{1cm} (5.27)

\[
S_{12}^{\Gamma_l} = S_{12} + \frac{S_{13} \cdot S_{23}}{\Gamma_l - S_{33}}
\]  \hspace{1cm} (5.28)

\[
S_{22}^{\Gamma_l} = S_{22} + \frac{S_{23}^2}{\Gamma_l - S_{33}}
\]  \hspace{1cm} (5.29)

for \(l = 1 – 3\). \(S_{ij}^{\Gamma_l}\) is the measured \(S_{ij}\) with the third port terminated by \(\Gamma_l\).

The set of the measured \(S_{11}^{\Gamma_l}\) can be solved for \(S_{11}, S_{33}\) and \(S_{13}\)

\[
S_{33} = \frac{(S_{11}^{\Gamma_1} - S_{11}^{\Gamma_2})(\Gamma_3 - \Gamma_2) - (S_{11}^{\Gamma_3} - S_{11}^{\Gamma_2})(\Gamma_1 - \Gamma_2)}{(S_{11}^{\Gamma_1} - S_{11}^{\Gamma_2})(\Gamma_3 - \Gamma_2) \cdot \Gamma_1 - (S_{11}^{\Gamma_3} - S_{11}^{\Gamma_2})(\Gamma_1 - \Gamma_2) \cdot \Gamma_3}
\]  \hspace{1cm} (5.30)

\[
S_{11} = \frac{\Gamma_2 S_{11}^{\Gamma_3}(1 - S_{33}\Gamma_1) - \Gamma_3 S_{11}^{\Gamma_2}(1 - S_{33}\Gamma_2)}{\Gamma_2(1 - S_{33}\Gamma_1) - \Gamma_3(1 - S_{33}\Gamma_2)}
\]  \hspace{1cm} (5.31)
5.7. Summary

The set of measured $S_{22}^\Gamma$ can be solved for $S_{22}$ and $S_{23}$

\[ S_{23} = \pm \sqrt{\frac{S_{22}^\Gamma - S_{33}^\Gamma}{1 - \Gamma_2 S_{33}}} \]

(5.33)

\[ S_{22} = S_{22}^\Gamma - \frac{\Gamma_2 S_{23}^2}{1 - \Gamma_2 S_{33}} \]

(5.34)

$S_{12}$ is finally calculated as

\[ S_{12} = S_{12}^\Gamma - \frac{S_{23} S_{13} \Gamma_2}{1 - \Gamma_2 S_{33}} \]

(5.35)

To make the correct choice of sign for $S_{13}$ and $S_{23}$, the corresponding phases should be known within $\pm 90^\circ$. The knowledge of the approximate phase suffices to make the correct choice of sign for all frequencies, e.g., for a T-junction the solution with the lowest phase shift is the right one.

5.7. Summary

In this chapter, a two-tier calibration technique for 2-port on-wafer measurements with probe-tips was implemented to accurately characterise the performance of the new developed MCM technologies. It performs a full TRL or LRRM off-wafer calibration and a second-tier on-wafer calibration based on the measurement technique of two transmission lines of different lengths, THRU and LINE [3, 4]. Using this technique, the line loss and line effective permittivity can be precisely de-embedded for the on-wafer line standards arbitrarily mismatched with a measurement system. The de-embedded values are also unaffected by the ill-conditioned S-parameter matrix equations at frequencies corresponding to the multiples of half a wavelength on a line. In practice, it means that LINE standards can be arbitrary long, thus, providing sufficient accuracy level for the de-embedded values of the line loss and line effective permittivity. Any modelling of the feed network error boxes is not required at this stage. The only parameter to be known is a length difference between both line standards.

Moreover, a detailed analysis of the limitations of the state-of-the-art methods for de-embedding the CPW line characteristic impedance was performed. As a result of this study, a variety of new de-embedding techniques was proposed:
- A de-embedding technique with an automatic detection of the reference plane position, valid for CPW lines on both lossless and lossy substrates was established. The proposed chain matrix formulation of the problem results in explicit analytical formulas relating the de-embedded line characteristic impedance and the elements of an error box model to the measured S-parameters of the calibration standards. It was shown that using chain matrix formulation, the shunt feed parasitics, practically representing the feed geometry behind the probe-tips, do not influence the de-embedding process. As a result, they do not need to be modelled and can be of any arbitrary complexity.

- It was also found that the symmetry of a reciprocal feed discontinuity allows to de-embed the line characteristic impedance from the chain matrices of the two measured line standards without modelling the internal structure of this discontinuity. This symmetry condition was applied to extend the de-embedding process to the taper-fed CPW lines.

- A characteristic impedance de-embedding process for Finite-Width CBCPW lines was presented. For this purpose, a previously developed technique with an automatic detection of the reference plane position was applied. The influence of parasitic waveguide modes on the de-embedded values was analysed in detail and validated by the full-wave simulation results.

- For the first time, a state-of-the-art two-step characteristic impedance de-embedding technique for microstrip lines, valid at mm-wave frequencies, was developed. The use of a symmetric error box model for the FW-CBCPW-microstrip mode conversion showed its potential to catch the distributed nature of this complex transition. The other known state-of-the-art lumped error box models failed at mm-wave frequencies. The choice of the proper feed topology was analysed and supported by full-wave 3D simulations.

Finally, different measurement results within the frequency range of 1-100 GHz for each of the considered line configurations were presented.
Extraction of dielectric properties for thin dielectric layers

In this chapter, a wide-band in-situ extraction procedure of material complex dielectric permittivities for thin dielectric layers at mm-wave frequencies is presented [115, 116]. As the considered interconnect technologies are supposed to work with printed lines, choosing them as a standard measurement cell allows to achieve full compatibility with the process flow and precise in-situ measurements. When using printed lines, the investigation of other process-related parameters such as the important influence of metallisation build-up and its quality on the line complex propagation constant and characteristic impedance is also possible.

The developed procedure is based on the probe-tip VNA measurements of a set of microstrip lines of different line cross-sections. It allows separation of complex permittivities of dielectric materials and metallisation related parameters (ohmic loss, slow-wave effects in a metal track) without an ex-
act modelling of the latter. Not only single-layer microstrip lines are analysed but also composite dielectric build-ups and substrates with passivation layer, often existing in hybrid interconnect technologies. In the first step of the procedure, complex propagation constants and characteristic impedances are de-embedded from the probe-tip measurements of different microstrip lines using the techniques developed in Chapter 5. In the second step, these parameters are converted into the equivalent elements $(C, G, L, R)$ of the corresponding distributed circuit model. $C$ and $G$ are related to the dielectric material properties $(\varepsilon_r, \tan\delta)$ by the use of a set of non-linear closed-form equation models which are then solved by a Gauss-Newton method. Hundreds of full-wave simulations have been performed to choose, test and modify different closed-form analytical formulas as they impose a limit on the maximum achievable accuracy of the extraction procedure. The accuracy of the procedure was tested up to 100 GHz for the microstrip line cross-sections and dielectric materials used within the frame of the EU project LIPS [117]. The technology set covers a BCB-based thin-film MCM-D and a variety of thin laminate MCM-L build-ups.

In the first section, a problem statement for determination of dielectric permittivities of thin dielectric layers is presented. The importance of in-situ extraction is underlined and the choice of a microstrip line as a measurement cell is explained. Section 6.1.1 gives a detailed analysis of different drawbacks of a classical printed-resonator measurement technique at mm-wave frequencies and justifies the decision of its rejection. The next section presents a general overview of a developed de-embedding technique, addressing some additional issues related to the microstrip lines in hybrid technologies that have to be taken into account in the development process of the extraction procedure. The accuracy measures for the tested closed-form expression models are defined in Sec. 6.3. The next two sections present the details of these models for a single dielectric layer and different multi-layer microstrip line configurations. Examples of the extraction results from the VNA measurements are given in the last section, indicating some other issues related to the accuracy of the extracted values such as the influence of calibration errors and its repeatability, and technology manufacturing tolerances.

### 6.1. Problem statement

The most widely used techniques for determination of complex permittivity of a dielectric material are: cavity resonators, free-space, open-ended coaxial probe and transmission/reflection. All these methods require a measurement cell made up of a section of coaxial line or rectangular waveguide filled with
the sample material to be characterised. We, on the contrary, aim at the extraction of complex permittivities for thin films and thin laminates with a fixed thickness and form. Building the samples based on a bulk material required by the above-mentioned characterisation techniques, essentially, is impossible in this case. The fact that these methods do not perform an in-situ extraction is also of importance for the confidence level in the extracted values. It is highly required that extraction procedures are based on the measurement cells that are created using exactly the same dielectric layer thicknesses and the same process flow as those supposed to be used in the standard technology build-up and design process. As the presented interconnect technologies are supposed to work with printed lines, choosing them as a standard measurement cell allows to achieve full compatibility with the process flow and precise in-situ measurements. When using printed lines, the investigation of other process-related parameters such as the important influence of a metallisation build-up and its quality on the transmission line parameters is also possible. However, for the extraction procedure based on printed lines measurements, many other issues have to be addressed:

1. The printed lines are inhomogeneous dielectric build-ups and do not guide pure TEM mode. As a result, simple procedures to find the relative permittivities of the materials used are not possible. Closed-form analytical equations relating the complex transmission parameters of the measured lines and the substrate relative dielectric permittivities and line geometry have to be used.

2. The high-frequency dispersion of the printed lines requires additional analytical equations modelling the dispersion level.

3. The low-frequency dispersion caused by slow-wave effects in the transmission line is also an issue. This effect is caused by noticeable field penetration in a metal track, rising the line internal inductance. This phenomenon considerably influences the frequency behaviour of thin microstrip lines, wherein the contribution of the internal inductance to the total line inductance is substantial. In this case, the measured line effective permittivity and line impedance can be noticeably different from those of the corresponding lossless line.

4. Different loss types exist on the printed lines: dielectric, ohmic, radiation to the space and surface waves. Extraction of the material dielectric loss tangent needs the separation of all these types of losses. This, in turn, calls for accurate analytical equations for every type of losses as
a function of the line geometry, substrate parameters ($\varepsilon_r$, $\tan\delta$) and operating frequency.

6.1.1. Printed line resonators

All the previously mentioned methods for determination of the complex dielectric permittivities, including cavity resonators, were rejected because of the very thin dielectrics used within this work. Although it is still possible to create resonator structures based on printed lines, this method was also eliminated because of some key disadvantages, which were found important for this work:

1. Narrow-band extraction at some frequency points only

2. Most of the $Q$-factor and resonant frequency de-embedding techniques were developed based on ideal model of the resonator system [118, 119]. The $S$-parameters of an ideal resonator measured near the resonance should form circles in the complex plane centred at the origin. However, due to the effects associated with the printed line dispersion and an external circuitry, the measured responses are distorted and often do not pass through the origin of the complex plane. The following phenomena affect the $S$-parameters:

- The basic error is the assumption of lack of line dispersion or constant dielectric permittivity around the resonance.

In this technique, the quality factor $Q$ is defined by the following relation $Q = \beta/2\alpha$ ($\beta$ - line propagation constant, $\alpha$ - line attenuation constant), where

$$\beta = \frac{\omega}{c}\sqrt{\varepsilon_{reff}} \quad (6.1)$$

This equation, however, does not include the effect of dispersion. For a dispersive line, $\varepsilon_{reff}$ becomes a function of frequency and the proper expression for $Q$ becomes:

$$Q = \omega(\partial\beta/\partial\omega)/(2\alpha) \quad (6.2)$$

where $\beta$ is defined by (6.1). As the typical quality factor $Q$ of the printed resonators is low, the measured bandwidth can be large and the assumption of the dispersion-free lines is not necessarily correct.
6.1. Problem statement

- The frequency-dependent loss and electrical delay introduced by dispersive feed transmission lines. The exact frequency-dependent characteristics of the feed lines have to be known to account for their influence.

- The resonators are gap-coupled for printed lines. This is a source of additional losses from the open-ends and of the frequency detuning caused by energy stored in a coupling structure. The coupling level is frequency dependent and only for high-\(Q\) systems (loaded \(Q > 1000\)) it may be justifiable to assume it constant in the narrow frequency band around the resonance. However, this is not necessarily true for printed line resonators [120].

- Impedance mismatch between the feed structure of a measured resonator and the reference impedance of a measurement system. A basic source of this mismatch are different values of both reference and feed line impedances. Another cause is not fully calibrated feed structure. Typically, the calibration procedure is performed using only an off-wafer calibration substrate with CPW line standards (assumed probe-tip measurements). Different substrate dielectric constants, feed geometries and line topologies for both off- and on-wafer structures cause that feed parasitics still remain influencing the measurements at mm-wave frequencies (see Fig. 5.3 in Chapter 5).

  In the presence of this mismatch, the magnitudes of reflection and transmission coefficients change periodically with frequency, except at the resonance peak. A nonlinear effect in the phase of reflection coefficients is also observed.

- Printed line resonators can show considerable radiation around the resonant frequencies, especially for thicker substrates and higher frequencies. This factor has to be taken into account in the extraction process of the line \(Q\)-factor in a precise manner. The radiation can also cause crosstalk between both coupling structures for transmission mode resonators.

Thin microstrip lines (TMSL) as a measurement cell

Microstrip lines (MSL) were chosen as a measurement cell since they allow good field concentration into the dielectric materials and, thus, seem to be well suited to their electromagnetic characterisation. The lines used within this work fall into the group of thin microstrip lines (TMSL) because of the
thin film and thin laminates MCM technologies used. For conventional MSLs, a variety of closed-form models is available in the literature. However, since dimensions of TMSL and conventional MSL differ considerably, applying the common MSL models to TMSL can yield significant errors. For TMSLs, line heights and widths are in the order of magnitude of the metallisation thickness, what is considerably different from common MSL. These differences in the geometrical dimensions between both configurations cause discrepancies in the electrical behaviour. In the TMSL case, small dimensions increase conductor losses. Due to the relatively large ratio of metal strip thickness to substrate height, $t/h_s$, the influence of a finite metal conductivity and an internal line inductance have to be taken into account. In the lower- and mid-frequency ranges, the physical behaviour of the internal inductance cannot be simply approximated because the line is outside of the DC and skin effect ranges [121]. Therefore, phase constant and characteristic impedance for TMSL can deviate considerably from the lossless case and show typical increase toward lower and mid-frequencies.

Classical approach for dielectric permittivity extraction

In the extraction process of dielectric permittivities, the two basic equations are routinely used:

$$\gamma = \alpha + j\beta \sqrt{(R_{dyn} + j\omega L_{dyn})(G_{dyn} + j\omega C_{dyn})}$$ (6.3)

$$\epsilon_{eff} = \left(\beta c_0/\omega\right)^2$$ (6.4)

where $\beta$ and $\alpha$ are the phase and attenuation constants, respectively. Using the correspondence between the complex propagation constant, $\gamma$, and the $C_{dyn}, G_{dyn}, L_{dyn}, R_{dyn}$ elements of an equivalent distributed circuit model, it can be noticed that the measured value of the line effective dielectric permittivity, $\epsilon_{eff}$, is a non-linear, in general, frequency-dependent function of all the model elements (the "dyn" index stands for frequency-dependence). As a result, dielectric permittivity extracted directly from the measured $\epsilon_{eff}$ (Eq. 6.4), using the known closed-form analytical formulas relating the line effective permittivity and the substrate dielectric constant, does not produce any errors for the lossless case only or it results in negligible errors for standard thick microstrip lines on low-loss substrates. However, using this approximation for the lines on lossy substrates such as a low-resistivity silicon can produce large deviations in the extracted values. It is also invalid for thin microstrip lines, wherein the internal line inductance, $L_{int}$, (modifying the phase constant of a microstrip line) associated with the magnetic fields inside
6.1. Problem statement

the conductors is comparable with the external line inductance, $L_{\text{ext}}$, covering the magnetic fields outside of the conductors.

To avoid the influence of a line loss, represented by $G_{\text{dyn}}$ and $R_{\text{dyn}}$, and of the slow-wave effects (caused by the internal line inductance) on the extracted dielectric permittivity values, $C_{\text{dyn}}$ should be used in the extraction process. In order to arrive at its value using only the measured line propagation constant, $\gamma$, (see Eq. 6.3), precise analytical equations for $G_{\text{dyn}}$, $L_{\text{dyn}}$ ($L_{\text{dyn}} = L_{\text{int}} + L_{\text{ext}}$), $R_{\text{dyn}}$ are necessary. These are difficult to find because of numerous factors analysed below.

As known from quasi-TEM theory, the line capacitance is related to the electrostatic case and, thus, is constant with frequency (except for high-frequency non-TEM contributions). The line inductance and resistance are determined by magneto-quasistatics. Therefore, in contrast to the line capacitance, they vary with the longitudinal current distribution changes in non-ideal conductors of finite conductivity. It results in a considerable frequency dependence due to the varying current penetration with frequency increase. This dependence can be subdivided into three different ranges [121, 122]:

1. DC range with homogeneous current density within a conductor
2. Skin-effect range with the current flowing only in a shallow area at the conductor surface
3. Transition range between the two above-mentioned. As the metallisation thickness is comparable with the skin depth, a simple approximation of the physical behaviour in this range is not possible.

For $L_{\text{dyn}}$ and $R_{\text{dyn}}$ in the thin microstrip lines, being under investigation, significant deviations between the conventional microstrip approximations and the actual values can be observed, particularly in the intermediate frequency range. The most extensive study of formulas modelling the frequency dependent behaviour of both elements for thin microstrip lines was reported in [121], wherein purely numerical non-linear functions, fitted to the full-wave simulation data, were used in the transition frequency range. For the investigated thin-film BCB microstrip lines ($w = 8 - 140 \ \mu\text{m}$, $h_{s} = 1.7 - 50 \ \mu\text{m}$, $t = 0.8 - 3.5 \ \mu\text{m}$, where $w$, $h_{s}$ and $t$ denote a strip width, a dielectric layer thickness and a metallisation thickness, respectively), the overall reported modelling accuracy was better than 3%, 2% and 8% for the line characteristic impedance, propagation constant and attenuation constant, respectively. The largest deviations occurred in the intermediate-frequency region between the DC and skin-effect ranges. Moreover, the formulas assumed the same
metallisation thickness for both the strip and the ground plane, ideal rectangular strip profile and homogeneous conductor material. Unfortunately, these assumptions are often violated for hybrid technologies. In this case, the following issues, potentially modifying the behaviour of $R_{dyn}$ and $L_{dyn}$, have to be addressed in the extraction procedure:

1. A strip profile can often deviate from the ideal rectangular as a result of non-ideal etching process, specifically for a thick metal strip. The acute angles, being a result of etching profile, cause considerable increase of the current density in these regions at mm-wave frequencies, substantially increasing the line attenuation constant and modifying the behaviour of $R_{dyn}$ and $L_{dyn}$.

2. The surface roughness of both metallisation and dielectric layers increase the equivalent surface resistance associated with a metal conductor and make it a more complex function of frequency. For many technologies, specifically laminate-based, the surface roughness can be considerable higher than the skin depth in typical high-conductivity materials at mm-wave frequencies.

3. A composite metal build-up is usually used. Typically, it consists of a main conductor layer sandwiched between adhesion or barrier materials such as Ti, TiW, Cr or Ni. It makes the current density distribution within conductor a complex function of frequency. A special care needs an intermediate layer of nickel, existing in some build-ups, because of its magnetic properties screening the field penetration. Analytical derivation of the line inductance can be difficult even in the DC range because of inhomogeneous current distribution within a complex conductor layer. Furthermore, the measured line DC resistance of a composite metal build-up is an effective value taking all conductor conductivities into account. As a result, it cannot be used as an input parameter for the approximation of $R_{dyn}$ and $L_{dyn}$ in the skin-effect and intermediate frequency ranges.

4. Different thicknesses and conductor materials of both ground and signal metallisations cause different frequency dependence of the field penetration in both metal layers. It results in a modified frequency behaviour of $R_{dyn}$ and $L_{dyn}$ if compared to the configuration with the consistent thickness and conductivity for both metal layers.

Summarising, the above analysed issues related to the complex frequency-dependent current distribution within a metal conductor make an analytical
prediction of $R_{dyn}$ and $L_{dyn}$ practically impossible. Their accurate calculation demands full-wave simulations with the fields solved inside metal layers. Even if some problem simplification could be made in order to arrive at approximate formulas, the uncertainty level of the extraction procedure would be high because of difficulties in prediction of the approximation errors.

6.2. Overview of the extraction procedure

Using the correspondence between both transmission line parameters, $\gamma$ and $Z_0$, and a distributed equivalent circuit model, given by equations Eq. 6.3 and that given below:

$$Z_0 = \sqrt{(R_{dyn} + j\omega L_{dyn})/(G_{dyn} + j\omega C_{dyn})} \quad (6.5)$$

allows to arrive at the corresponding $C_{dyn}$, $G_{dyn}$, $L_{dyn}$, $R_{dyn}$ model elements, thus, avoiding the above analysed complex influence of $R_{dyn}$ and $L_{dyn}$ on the accuracy of extracted dielectric permittivities. This powerful technique allows direct separation between the dielectric material properties and the metallisation-related parameters, without exact modelling of the latter. However, it demands an additional line parameter to be known, namely the line characteristic impedance. Finally, the material dielectric permittivities are extracted from $C_{dyn}$ only, using the following relation:

$$C_{dyn} = \varepsilon_{reff}^{\text{static}} F_C C_{air} \quad (6.6)$$

$C_{air}$ is a capacitance per unit length of the line without dielectric substrate, $\varepsilon_{reff}^{\text{static}}$ static value of the line effective dielectric constant and $F_C$ high-frequency dispersion factor.

Using the already known $C_{dyn}$ and $\varepsilon_r$ values, the material loss tangents can also be found without considering the influence of ohmic losses. For single dielectric microstrip lines, the de-embedded line conductance per unit length, $G_{dyn}$, is linearly related to the line partial capacitance filled with dielectric, $C_\varepsilon$, by the loss tangent, $\tan\delta$, [123]:

$$G_{dyn} = \tan(\delta) \cdot \omega \cdot C_\varepsilon = \tan(\delta) \cdot \omega \cdot C_{dyn} \cdot \frac{\varepsilon_r \cdot (\varepsilon_{reff}^{\text{static}} - 1)}{\frac{\varepsilon_{reff}^{\text{static}}}{\varepsilon_{reff}^{\text{static}}} \cdot (\varepsilon_r - 1)} \quad (6.7)$$

For composite dielectric microstrip line build-ups, such a simple formula does not exist. A general relation between $G_{dyn}$ and the contributing loss tangents of the composite dielectrics was developed (see Sec. 6.5.3). From the known
Chapter 6: Extraction of dielectric properties for thin dielectric layers

$R_{dyn}$, the frequency-dependent equivalent conductor surface resistance values can also be estimated, even for a composite conductor metallisation.

Taking the above into account, a transmission/reflection method for a wide-band extraction of complex material dielectric permittivities was established [115, 116]. A general block diagram of the developed method is shown in Fig. 6.1. It includes two blocks corresponding to the two distinct stages of the procedure. The input data are the S-parameters from the probe-tip VNA measurements of microstrip lines of different line cross-sections. In the first step, transmission line parameters, $\gamma$ and $Z_0$, are extracted from the input data. For this purpose, the de-embedding techniques from Secs. 5.2 and 5.5 (see also [98, 111]) for the line propagation constant and line characteristic impedance, respectively, were used. Due to the self-calibration property of these techniques, the influence of feed structures is fully eliminated. The problem of possibly considerable radiation from the printed resonators at the measured resonance frequencies is avoided, which is of importance for the accuracy of the extracted line loss attenuation. The open-end effects (among others radiation losses) associated with the gap-coupled printed resonators are also avoided.

The second step of the procedure (see Fig. 6.2) performs the extraction of complex dielectric permittivities using the transmission line parameters, $Z_0$ and $\gamma$, known from the previous phase. These are first converted to the equivalent elements of a distributed circuit model. Next, $C_{dyn}$ and $G_{dyn}$ are used to arrive at the appropriate dielectric permittivity and loss tangent val-

**Figure 6.1:** A block diagram of the extraction procedure of the complex dielectric material permittivities.
6.2. Overview of the extraction procedure

Figure 6.2: The 2nd step of the extraction procedure of the complex dielectric material permittivities ($C_{dyn}, C_{static}$ - static and dynamic values of the line capacitance per unit length, $C_{air}$ - capacitance per unit length of the line without dielectric substrate, $C_e$ - line partial capacitance filled with dielectric, $G_{dyn}, G_{static}$ - static and dynamic values of the line conductance per unit length, $\varepsilon_{reff}^{static}$ - static value of the line effective dielectric permittivity, $F_C$ - high-frequency dispersion factor of the line capacitance per unit length).

ues (see Eqs. 6.6 and 6.7). The kernel of the second stage of the procedure are the quasi-static closed-form models for the line effective dielectric permittivity, $\varepsilon_{reff}$, and line capacitance, $C_{dyn}$, (see Fig. 6.2). They are extended by the high-frequency dispersion correction factor, $F_C$. For the composite dielectric substrate and superstrate build-ups, an additional modelling step is needed, called single-layer reduction technique (SLR) [124, 125]. In this step, an equivalent single dielectric substrate permittivity, $\epsilon_{r,eq}$, is calculated, which is then used for the proper modelling of high-frequency dispersion and for the correct inclusion of a finite metal strip thickness into the quasi-static analysis.

As the closed-form models represent weak non-linearity, they are solved using a Gauss-Newton method due to its fast convergence. The minimum number of different microstrip line cross-sections needed in the extraction procedure is equal to the number of unknown dielectric permittivities in order to build a set of independent non-linear equations. For a single dielectric microstrip build-up, this number is equal to 1. In this work, composite dielectric substrate and superstrate configurations are also considered, requiring higher minimum number of different line cross-sections to be measured. In practice, a larger count of different line geometries is advisable in order to decrease the
uncertainty level of the extracted data.

In the next sections, the development of a set of closed-form analytical equations modelling the behaviour of different microstrip line configurations (single dielectric, composite dielectric and superstrate) is addressed.

### 6.3. Testing the accuracy of the closed-form equations

The accuracy of the closed-form models, being developed, needs to be determined for a variety of microstrip line cross-sections and dielectric materials using some reference data coming from the very accurate full-wave solvers. While testing the accuracy of different formulas, the highest attention was paid to the line configurations supposed to be used within the research project. The initially assumed values of dielectric constants and loss tangents for different thin-film and thin laminate materials investigated within this work are collected in Table 6.1. They are input parameters for the full-wave solvers used as reference data generators in the process of testing the accuracy of the closed-form analytical models being developed. The thicknesses of metallisation layers used for full-wave simulations are \( \{0,1,3\} \) \( \mu \text{m} \) for the BCB-based MCM-D and \( \{0,10,17\} \) \( \mu \text{m} \) for the MCM-L build-ups, respectively. The considered microstrip line widths are within 30-300\( \mu \text{m} \).

The accuracy of all closed-form models used in the extraction procedure (see Fig. 6.2), described in more detail in the next sections, was tested by comparison with the simulation data from two general full-wave solvers: Ensemble (SDA - Spectral Domain Analysis) and HFSS (FEM - Finite Element Method). The numerical accuracy of the transmission line parameters (complex \( Z_0 \) and complex propagation constant \( \gamma \)), calculated by means of these

<table>
<thead>
<tr>
<th>Material</th>
<th>( \varepsilon_r )</th>
<th>( \tan(\delta) )</th>
<th>Dielectric layer thickness [( \mu \text{m} )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCB</td>
<td>2.7</td>
<td>0.002</td>
<td>45</td>
</tr>
<tr>
<td>Microlam</td>
<td>3.4</td>
<td>0.008</td>
<td>38</td>
</tr>
<tr>
<td>Speedboard</td>
<td>2.67</td>
<td>0.0053</td>
<td>38</td>
</tr>
<tr>
<td>Espanex</td>
<td>3.5</td>
<td>0.007</td>
<td>25</td>
</tr>
<tr>
<td>Biac LCP</td>
<td>3</td>
<td>0.003</td>
<td>25</td>
</tr>
<tr>
<td>Arlon 85NT</td>
<td>3.8</td>
<td>0.015</td>
<td>47</td>
</tr>
</tbody>
</table>
6.4. Single dielectric configuration

s solvers, can be controlled by some error functions in the process of solution convergence. Another important issue is the influence of specific boundary conditions (needed for numerical problem truncation) on the \( Z_0 \) and \( \gamma \) parameters for the simulated line cross-sections. Perfect Electrical Conductor (PEC) boundary conditions are used for a 2D port definition in HFSS. As it influences the field pattern in its proximity, the port dimensions need to be made appropriately large. To define these dimensions, a reference problem with an exact analytical solution is needed. An air suspended lossless microstrip line with a 2D strip metallisation and maximal cross-sectional dimensions used in our technology set (85 \( \mu \)m thick and 300 \( \mu \)m wide microstrip line) was chosen. This problem has an exact analytical solution which can be calculated by means of a Schwarz-Christoffel conformal mapping procedure. The case of an air-suspended microstrip line is critical in view of the influence of PEC boundary conditions because the field spread for a line without dielectric substrate is the largest. The final port height and width were chosen to be 8 mm and 9 mm, respectively. It allowed to keep an \( \text{rms} \) error between the analytically and FEM calculated characteristic impedances of the air-suspended microstrip lines below 0.1\%. This \( \text{rms} \) error was taken over the maximal deviation values within the 1–100 GHz frequency range for every considered microstrip line and a set of 30–300 \( \mu \)m wide microstrip lines was used during its calculation. This error definition was also used for all further accuracy considerations in the next sections.

The proper port dimensioning allows to calibrate properly our numerical solver to be used later on as a reference for checking the accuracy of the closed-form equations for more complex, dielectric filled, microstrip line cross-sections without an exact analytical solution.

The differences between the characteristic impedances calculated by HFSS and Ensemble are in the range of 0.2\%, thus, bringing even higher level of confidence in the accuracy of the closed-form models being developed.

6.4. Single dielectric configuration

The procedure of choosing a basic set of closed-form analytical equations for a single dielectric configuration is presented in detail in the next three subsections. The following modelling aspects have to be considered: quasi-static analysis with consideration of a finite metal strip thickness and high-frequency dispersion.
6.4.1. Quasi-static analysis

Generally, the static value of the line effective permittivity for quasi-TEM lines can be calculated by means of a Schwarz-Christoffel conformal mapping. However, in contrast to CPW lines, this method is difficult to apply to a microstrip geometry because the interface between the dielectric layer and air does not coincide with an electric field line. In the literature, several other approximate solutions for the calculation of a microstrip line effective permittivity are available [123, 126]. Mostly, the functional approximation formulas of Hammerstad and Jensen [127] are used because they promise the highest accuracy for a broad range of dielectric constants and cross-sectional dimensions.

For the lossless air-suspended microstrip line with a zero metal strip thickness, $t$, the Hammerstad and Jensen formula [127] for the characteristic impedance reads:

$$Z_{0,air} = \frac{\eta_0}{2\pi} \cdot ln \left( \frac{F_1 \cdot h_s}{w} + \sqrt{1 + \left( \frac{2h_s}{w} \right)^2} \right)$$  \hspace{1cm} (6.8)

$$F_1 = 6 + (2\pi - 6) \cdot \exp \left( -\left( \frac{30.666 \cdot h_s}{w} \right)^{0.7528} \right)$$  \hspace{1cm} (6.9)

$$\eta_0 = \sqrt{\frac{\mu_0}{\epsilon_0}}$$  \hspace{1cm} (6.10)

where $w$ and $h_s$ denote the strip width and dielectric substrate thickness, respectively. We tested the accuracy of this expression for a wide range of air-suspended microstrip line cross sections. Differences between the results calculated using the above formula and an exact analytical solution, given by Schwarz-Christoffel conformal mapping, are within a few hundredths of a percent.

For a microstrip line on a dielectric substrate ($\epsilon_r > 1$), the line effective permittivity is:

$$\epsilon_{ref}(0) = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot \left( 1 + \frac{10h_s}{w} \right)^{-a \cdot b}$$  \hspace{1cm} (6.11)

$$a = 1 + \frac{1}{49} \cdot \ln \left( \frac{w}{h_s} \right)^4 + \left( \frac{w}{52h_s} \right)^4 + 0.432 + \frac{1}{18.7} \cdot \ln \left( 1 + \left( \frac{w}{181h_s} \right)^3 \right)$$  \hspace{1cm} (6.12)

$$b = 0.564 \cdot \left( \frac{\epsilon_r - 0.9}{\epsilon_r + 3} \right)^{0.053}$$  \hspace{1cm} (6.13)
In [124], it was pointed out that the accuracy of Eq. 6.11 shows some degradation for narrow lines. However, we did not experienced this effect for the narrowest considered line width of 30 μm and substrate heights of up to 85 μm. For comparison purposes, the line effective permittivities for a set of 30–300 μm wide microstrip lines on the dielectric substrates from Table 6.1 were calculated by means of a variational method. This analytical method is supposed to yield the highest accuracy for a very wide range of line geometries and dielectric substrate permittivities. Both variational analysis and the formulas by Hammerstad and Jensen [127] have shown similar accuracy for the tested line dimensions. As this technique has the potential for application to microstrip lines on multi-layer dielectrics, it will be analysed in detail in Sec. 6.5.1.

Regarding thin microstrip lines (TMSLs) considered in this work, a finite metallisation thickness of the signal conductor, \( t \), has to be taken into account, when using Eqs. 6.8 and 6.11. This is done by applying a concept of an equivalent increased conductor width, \( w_{eq} \) [123]. Two cases have to be distinguished. For an air-suspended microstrip line, \( w_{eq0} \) is to be used (Eq. 6.14), whereas for \( \varepsilon_r > 1 \), \( w_{eqZ} \) (Eq. 6.15) has to be applied:

\[
\begin{align*}
  w_{eq0} &= w + \frac{t}{\pi} \cdot \ln \left( 1 + \frac{4 \cdot \exp(1)}{t \cdot \coth^2 \left( \sqrt{6.517 \cdot \frac{w}{h_s}} \right)} \right) \quad (6.14) \\
  w_{eqZ} &= w + \frac{w_{eq0} - w}{2} \cdot \left( 1 + \frac{1}{\cosh \left( \sqrt{\varepsilon_r - 1} \right)} \right) \\ 
\end{align*}
\]

Using Eqs. 6.8–6.15, characteristic impedance and effective relative dielectric constant of the lossless microstrip in the case \( \varepsilon_r > 1 \) and \( t > 0 \) can be described by [127]:

\[
\begin{align*}
  Z_0^{\text{static}} &= \frac{Z_{0\text{air}}(weqZ)}{\sqrt{\epsilon_{\text{reff}(0)}(weqZ)}} \quad (6.16) \\
  \epsilon_0^{\text{static}} &= \epsilon_{\text{reff}(0)}(weqZ) \cdot \left( \frac{Z_{0\text{air}}(weq0)}{Z_{0\text{air}}(weqZ)} \right)^2 \\ 
\end{align*}
\]

It should be noticed that the line characteristic impedance for \( \varepsilon_r > 1 \) is obtained from the effective permittivity concept and the line impedance of a corresponding free-space microstrip line. In a result, any explicit closed-form equations for \( Z_0 \) are not needed.

The capacitance per unit length of the line without dielectric substrate (\( \varepsilon_r = 1 \)) is given by the characteristic impedance, \( Z_{0\text{air}} \), and free space light
velocity, \( c_0 \) [126]:

\[
C_{air} = \frac{1}{c_0 \cdot Z_{0air}(w_{eq0})}
\]  

(6.18)

Accordingly, the static capacitance per unit length of the line with dielectric substrate (\( \epsilon_r > 1 \)) is:

\[
C_{static} = \epsilon_{reff}^{static} \cdot C_{air}
\]  

(6.19)

6.4.2. Modelling of high-frequency dispersion

The closed-form equations presented thus far rely on a quasi-TEM description. Therefore, the transverse characteristic dimensions such as a signal conductor width, \( w \), and a substrate height, \( h_s \), have to be small enough compared to the wavelength. In order to expand the validity range of the models to high frequencies, dispersion formulas have to be included.

**Line effective permittivity dispersion**

Regarding dispersion of the effective dielectric constant, we refer to the formulas by Kirschning and Jansen [126], and Kobayashi [128]. For a detailed description of both dispersion models, refer to Appendix C.

Kirschning and Jansen [126] estimated the accuracy of their dispersion model as better than 0.6% in the range \( 0.1 < w/h_s \leq 100, 1 < \epsilon_r \leq 20, \) and \( 0 \leq h_s/\lambda_0 \leq 0.13 \). Whereas, the accuracy of the formula by Kobayashi was specified as better than 0.6% in the range \( 0.1 < w/h_s \leq 10, 1 < \epsilon_r \leq 128, \) and any \( h_s/\lambda_0 \) [128], thus considerably extending the frequency range of validity.

Both models were originally developed for microstrip lines with a zero metal strip thickness. We verified their validity for a finite strip conductor thickness, the influence of which could be accounted for by simple modifications. First, the corrected value of \( \epsilon_{reff}^{static} \) given by Eq. 6.17 was used as an input parameter in place of \( \epsilon_{reff}(0) \) (Eq. 6.11). Then \( w/h_s \) ratio was replaced by \( w_{eqZ}/h_s \) (see Eq. 6.15). We found out that both models give very similar accuracy for the considered microstrip lines set (see Table 6.2) with a zero strip thickness. However, the model by Kobayashi gives two times lower approximation error for thick metallisation thickness of \( \{10,17\} \mu m \) used in the MCM-L build-ups. The accuracy of the dispersion models also depends upon the accuracy of determination of static line permittivity values, or in other words the accuracy of the quasi-static closed-form equations from Sec. 6.4.1. The use of \( \epsilon_{reff}^{static} \) calculated by both the variational [129, 130] and Hammerstad and Jensen [127] expressions resulted in very similar model accuracies.
Characteristic impedance dispersion

Although the classical concept of characteristic impedance does not apply to microstrip lines in a rigorous sense, it can be considered to be an indispensable approximate means of microstrip circuit analysis. As shown by numerical solutions to the microstrip hybrid mode problem, different formulations of characteristic impedance in terms of suitable combinations of voltage, longitudinal current and average propagated power result in different numerical values at high frequencies. Only in the quasi-static limit microstrip characteristic impedance is a unique physical quantity. For this reason, several authors have contributed in the past to a discussion on the proper choice of the definition of microstrip characteristic impedance for frequencies where hybrid mode effects become noticeable.

The results of different considerations, among others performed in [91, 131], show that the net complex power as computed from the transverse electromagnetic field of the fundamental mode has to be part of any definition of microstrip network quantities, indispensably.

However, an additional very important criterion to be considered is which one of the possible power definitions is the better TEM-equivalent at high-frequencies. This TEM-equivalent is best represented by the power-current formulation. Numerical computations of the two power-related characteristic impedance formulations show that for a fixed propagated power on a microstrip, the longitudinal strip current has a much slower increase with frequency than the strip centre voltage. The reason for this is that the air-dielectric interface present in microstrip has a first-order effect on the electric field but only a second-order effect on the current and the associated transverse magnetic field. The near constancy of the function $I(f)$ for fixed values of the propagated power may itself be regarded as a measure of its suitability to serve as a TEM-equivalent. An inspection of systematic broad-band measurement results of a variety of microstrip lines, performed by different authors, clearly indicates good agreement between the measured values and those predicted by the power-current definition. The characteristic impedance values de-embedded from our measurements (see Sec. 5.5), showing very good agreement with the power-current defined characteristic impedances (calculated by means of the HFSS solver), support this observation.

Additionally, other practical and conceptual arguments in favour of the power-current definition have also been published. For example, Knorr and Tufekcioglu [132] point out that the numerical value of the power-current formulation is insensitive to the assumed surface current distribution, whereas that of the power-voltage definition is not. Moreover, the path integral defin-
ing a voltage in the power-voltage formula depends on the path between a given pair of endpoints for a dispersive frequency range. The loop integral defining a strip current does not show this ambivalence.

The most accurate explicit representation of high-frequency dispersion for the power current-definition of microstrip characteristic impedance was given by Kirschning and Jansen [133] (see Appendix C for a detailed model description). The method employed for the generation of the above model is a multi-dimensional curve-fitting. The authors in [133] estimate the accuracy of the model as better than 1% in the range $0.1 < w/h_s \leq 10$, $1 < \epsilon_r \leq 18$, and $0 \leq h_s/\lambda_0 \leq 0.1$ when compared with a rigorous fully converged numerical hybrid mode solution.

The static value of the line effective permittivity, $\varepsilon_{static}$, being one of the constituent model parameters (see Appendix C), for a line with a finite strip conductor thickness is calculated using Eq. 6.17. The $u = w/h_s$ ratio is replaced by $w_{eqZ}/h_s$ (see Eq. 6.15) from the same reason. The dynamic value of the line effective permittivity, $\varepsilon_{ref}(f_n)$, also required by the considered dispersion formula, is calculated by the model of Kobayashi (Eq. C.7).

**Line capacitance dispersion**

The high-frequency dispersion factor of the line capacitance, $F_C$, directly involved in the process of dielectric permittivity extraction from the measured $C_{dyn}$ (see Eq. 6.6) can be related to the appropriate dispersion factors of the line effective permittivity, $F_\varepsilon$, and characteristic impedance, $F_Z$, (modelled by dispersion formulas from Appendix C) as follows:

$$F_C = \sqrt{F_\varepsilon/F_Z} \quad (6.20)$$

The dispersion phenomenon in the line effective dielectric constant is substantially stronger that that in the line characteristic impedance (power-current definition assumed). As the dispersion factor of the line capacitance, $F_C$, is related to the square root of $F_\varepsilon$, the influence of errors introduced by the non-ideal dispersion models for $\varepsilon_{ref}$ will be minimised in the extraction process of material dielectric constants.

**6.4.3. Accuracy results**

The accuracy of the presented models for thin single-layer microstrip lines were calculated using the $rms$ measure taken over a set of 30–300 $\mu$m wide microstrip lines and a metallisation strip thickness of 0, 1, 3, 10 and 17 $\mu$m (see also Sec. 6.3). The reference data set for error calculations comes from
full-wave HFSS simulations. It should be noticed that the accuracy of the closed-form expressions for \( Z_0 \) and \( \varepsilon_{\text{reff}} \), separately, is not equal to the accuracy of the extracted dielectric constants, that are derived from the de-embedded line capacitance values, \( C_{\text{dyn}} \), (Eq. 6.6). Modelling the latter involves the use of the equations for both \( Z_0 \) and \( \varepsilon_{\text{reff}} \). Thus, determining the approximation errors for both the "calculation mode" and the "extraction mode" is of interest.

The \textit{rms} errors in the "calculation mode" for the lossless microstrip lines on three different dielectric build-ups used within this work are gathered in Table 6.2. For the line characteristic impedance, power-current definition with dispersion model by Kirchning and Jansen [133] (Eqs. C.13-C.32) is chosen, whereas for the line effective dielectric constant, the model of Kobayashi [128] (Eqs. C.7-C.12). Figs. 6.3 and 6.4 show the calculated and HFSS simulated frequency-dependent \( Z_0 \) and \( \varepsilon_{\text{reff}} \) for some representative lossless microstrip lines. Almost perfect match between both can be noticed. Fig. 6.5 shows the frequency-dependent approximation error for the same structures in a more detailed way.

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric layer thickness [( \mu \text{m} )]</th>
<th>( Z_{\text{pi}} ) rms error [%]</th>
<th>( \varepsilon_{\text{reff}} ) rms error [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCB</td>
<td>45</td>
<td>0.28</td>
<td>0.3</td>
</tr>
<tr>
<td>Microlam</td>
<td>76</td>
<td>0.36</td>
<td>0.39</td>
</tr>
<tr>
<td>Speedboard</td>
<td>76</td>
<td>0.43</td>
<td>0.45</td>
</tr>
</tbody>
</table>

In order to define the principal accuracy of the extraction procedure, the reference input data was taken from the full-wave HFSS simulation results. Thus, any measurement errors and manufacturing tolerances are excluded from the considerations at this stage. The calculated \textit{rms} accuracy of the extraction procedure in the "extraction mode" for the single dielectric lossless microstrip lines taken over the three analysed build-ups and lines geometries specified in Table 6.2 is equal to 0.45%.

In order to prove the effectiveness of the decoupling property between the material complex permittivity and the metallisation-related parameters, the extraction results for two different input data sets were compared. They consist of the propagation constants and characteristic impedances for both lossless and lossy lines (both ohmic and dielectric losses are included). The ex-
Figure 6.3: Comparison of the line effective permittivities calculated by the closed-form equation model and simulated by HFSS for different lossless single-layer microstrip lines (Parameters $t$ and $w$ denote metallisation thickness and strip width, respectively).

Figure 6.4: Comparison of the characteristic impedance calculated by the closed-form equation model and simulated by HFSS for different lossless single-layer microstrip lines (Parameters $t$ and $w$ denote metallisation thickness and strip width, respectively).

...tracted $\varepsilon_r$ values from both input data sets for some representative microstrip line geometries are shown in Fig. 6.6. As the theoretical dielectric constants and loss tangents, being input parameters for the reference full-wave simulations, are known and frequency independent, it is possible to check the extraction accuracy for every frequency point, separately. The frequency-dependent extraction error is depicted in Fig. 6.7 for the same line geometries as those in...
6.4. Single dielectric configuration

Figure 6.5: Frequency-dependent approximation error of the closed-form $\varepsilon_{\text{reff}}$ model for different lossless single-layer microstrip lines. The reference input data comes from the 2D HFSS simulations. (Parameters $t$ and $w$ denote metallisation thickness and strip width, respectively).

Figure 6.6: Dielectric permittivities extracted using the closed-form equation models. The input reference data comes from 2D HFSS simulations of both lossless and lossy lines (both ohmic and dielectric losses included). The dielectric permittivities of 2.7 and 3.4 for BCB and Microlam, respectively, were assumed in simulations (Parameters $t$ and $w$ denote metallisation thickness and strip width, respectively).

Fig. 6.6. The next figure, Fig. 6.8, shows the extracted dielectric loss tangents for the BCB and Microlam with the a priori assumed input values of 0.002 and 0.008, respectively.
6.5. Multi-layer dielectric configurations

A multi-layer microstrip line is filled with several layers of different dielectrics. In the following, the individual dielectric layers are assumed to be linear, homogeneous and isotropic. We focus our considerations on two rep-
representative configurations most often found in hybrid technologies. In the first one, the area between the strip and ground plane is composed of two different dielectrics (denoted as $\varepsilon_{r1}$ and $\varepsilon_{r2}$ in Fig. 6.9) while above the strip there is air of permittivity $\varepsilon_0$. Such a build-up exists in some cases of our laminate technologies. This is a result of some processing requirements, namely some prepreg materials need adhesion films. The second build-up is a superstrate dielectric configuration, created by the existence of a passivation layer of permittivity $\varepsilon_{r3}$ in some laminate and MCM-D build-ups.

6.5.1. Quasi-static analysis

A quasi-static effective permittivity of the generalised lossless multi-layer microstrip lines with a zero metal thickness can be investigated by two analytical methods. The first, by Svacina [134, 135] and its improved version by Wan [136], is based on an approximate analysis using the conformal mapping technique. The second, proposed by Verma et. al. [124, 125], is based on a combination of the transverse transmission line technique [137] (TTL) and variational method [129, 130].

Conformal mapping method for microstrip lines

The advantage of an approximate analytical method based on the conformal mapping technique is that it provides a clear analytic insight of the relations between the geometrical dimensions (strip width, dielectric thicknesses) and the line effective permittivity of a microstrip line. Assuming quasi-static wave propagation in the line, the existence of more layers of different dielectrics will only alter the effective permittivity of a multi-layer microstrip. The dimensional relations, given by the so-called filling factors obtained by the conformal transformation, will be independent of the constituent dielectric per-
mittivities in a multi-layer build-up.

Exact relations for the line effective permittivity for both superstrate and two-layer composite configurations, derived using conformal mapping [134], can be found in Appendix D.

**Variational analysis for microstrip lines**

The theoretical difficulty of a microstrip line is attributed to the dielectric boundary conditions crossing the electric field lines. The variational method applied to this problem treats these boundary conditions in a general way so that a single- and a multi-layer microstrip line can be analysed without difficulty. The analytical treatment of multiple boundaries is also easier than by the modified conformal mapping. However, it needs a numerical evaluation of some integral and, thus, does not provide an explicit closed-form analytical relation between the line effective permittivity and the line geometry.

In this approach, the static value of the line effective permittivity, $\varepsilon_{\text{reff}}^{\text{static}}$, is derived from the calculated capacitances per unit length for the line with and without dielectric:

$$
\varepsilon_{\text{reff}}^{\text{static}} = \frac{C_{\text{static}}}{C_{\text{air}}} \tag{6.21}
$$

The Fourier-transformed variational expression for the line capacitance can be written as [129]:

$$
\frac{1}{C} = \frac{1}{\pi\varepsilon_0} \int_0^\infty \frac{[\tilde{f}(\beta)/Q]^2}{\beta} \frac{1}{Y} d\beta \tag{6.22}
$$

The $\beta$ coordinate and $\tilde{f}(\beta)$ are the Fourier transforms of the spatial coordinate, $x$ (see Fig. 6.9), and charge density distribution on the conducting strip, respectively, whereas $Q$ is the total charge on the strip. $Y$ is a so-called characteristic admittance function appropriate to the considered multi-layer microstrip line. The admittance functions $Y_{\text{single}}$, $Y_{\text{comp}}$ and $Y_{\text{sup}}$ for the single dielectric, two-layer composite dielectric and superstrate configurations (see Fig. 6.9 for the build-up definition), respectively, take the following forms:

$$
Y_{\text{single}} = \varepsilon_{r1} \coth(\beta h_1) + 1 \tag{6.23}
$$

$$
Y_{\text{comp}} = \varepsilon_{r2} \left\{ \frac{\varepsilon_{r1} + \varepsilon_{r2} \tanh(\beta h_1) \cdot \tanh(\beta h_2)}{\varepsilon_{r1} \tanh(\beta h_2) + \varepsilon_{r2} \tanh(\beta h_1)} \right\} + 1 \tag{6.24}
$$

$$
Y_{\text{sup}} = \varepsilon_{r1} \coth(\beta h_1) + \varepsilon_{r3} \left\{ \frac{\varepsilon_{r3} + \coth(\beta h_3)}{1 + \varepsilon_{r3} \coth(\beta h_3)} \right\} \tag{6.25}
$$
For the charge density distribution on an infinitely thin conductor strip, the following trial function, suggested by Yamashita ([129]), was chosen:

\[
 f(x) = \begin{cases} 
 1 + \left|\frac{2x}{w}\right|^3 & \left(-\frac{w}{2} \leq x \leq \frac{w}{2}\right) \\
 0 & \text{(otherwise)} 
\end{cases} 
\] (6.26)

with its Fourier transform given by

\[
 \frac{\tilde{f}(\beta)}{Q} = 8 \left( \frac{\sin(\beta w/2)}{\beta w/2} \right)^2 + 12 \left( \frac{\sin(\beta w/2)}{\beta w/2} \right)^2 \times 
\left\{ \cos(\beta w/2) - \frac{2\sin(\beta w/2)}{\beta w/2} + \frac{\sin^2(\beta w/4)^2}{\beta w/4} \right\} 
\] (6.27)

This is a rapidly decreasing function of \(\beta w\), where \(w\) is a strip width. Consequently, the line capacitance integral converges fast.

Using the variational analysis, the characteristic impedance of the unloaded line (free-space) \(Z_{0_{air}}\) can also be calculated

\[
 Z_{0_{air}} = \frac{1}{C_{air}c_0} 
\] (6.28)

However, taking into account that the line capacitance obtained by this method is always smaller than the exact value, deviations of the variational characteristic impedance from the exact value can be observed. This deviation is small but it is a function of \(w/h_s\). Thus, the impedance calculated by the variational method should be corrected to get more accurate results. The formula by Hammerstad and Jensen [127] (see Eq. 6.8), based on functional approximation, gives very accurate results and it was used in this work.

**Influence of finite metal thickness**

The variational analysis presented in the previous section was based on the assumption that the strip thickness, \(t\), is infinitely thin. For a strip of finite thickness, Yamashita [129] proposed a modified variational formula for the line capacitance calculation:

\[
 \frac{1}{C} = \frac{1}{\pi\epsilon_0} \int_0^\infty \left( \frac{1 + e^{-\beta t}}{2} \right) \frac{\left[\tilde{f}(\beta)/Q\right]^2}{\beta} \frac{1}{Y} d\beta 
\] (6.29)

Nevertheless, the strip thickness, \(t\), is assumed to be thin (\(t \ll h\), \(t \lesssim w\)). We have found that this approximation does not give satisfactory results for
our MCM-L build-ups with a strip thickness up to 17μm. Better results could be achieved by applying the concept of an equivalent conductor width, \( w_{eqZ} \), (Eq. 6.15) directly to the variational or conformal analysis.

However, the calculation of the corrected line width, \( w_{eqZ} \), requiring the dielectric permittivity of a single-layer configuration to be known, presents some difficulty coming from the inhomogeneous dielectric substrate material. Thus, the conversion of a multi-layer build-up into an equivalent single-layer, represented by a new static equivalent relative permittivity, \( \varepsilon_{r,eq} \), is required.

For a multi-layer composite dielectric configuration, a simple formula, determining the equivalent dielectric permittivity, \( \varepsilon_{r,eq} \), from a series connection of parallel capacitances with their corresponding dielectric constants and heights, was used. Its version for the two-layer build-up, also used by Lee and Dahele [138], takes the form:

\[
\varepsilon_{r,eq}^{comp} = \frac{\varepsilon_{r1} \cdot \varepsilon_{r2} \cdot (h_1 + h_2)}{\varepsilon_{r1} \cdot h_2 + \varepsilon_{r2} \cdot h_1}
\]  

(6.30)

Taking into consideration the physics behind a concept of an equivalent conductor width, given by Eqs. 6.14 and 6.15 (field distribution considerations modified by the existing finite metal strip thickness), we modified the above-given series capacitance approximation to a superstrate configuration

\[
\varepsilon_{r,eq}^{sup} = \frac{\varepsilon_{r1} \cdot \varepsilon_{r3} \cdot (h_1 - h_3)}{\varepsilon_{r1} \cdot h_3 + \varepsilon_{r3} \cdot h_1}
\]  

(6.31)

The accuracy of this expression was verified for the thin passivation layers used within this work.

For comparison purposes, we also tested the accuracy of the approach based on conformal mapping, used by Verma [130] in modelling of high-frequency dispersion for multi-layer microstrip lines. Verma et. al. [130] assumed that multi-layers result in a modified single-layer microstrip line with the equivalent substrate dielectric permittivity, \( \varepsilon_{r,eq} \), given by

\[
\varepsilon_{r,eq} = \frac{(\varepsilon_{eff(0)} - 1)}{q} - 1
\]  

(6.32)

where \( q \) is the filling factor, known from the conformal mapping analysis:

\[
q = 0.5 \cdot (1 + p)
\]  

(6.33)

\[
p = \begin{cases} 
[1 + \frac{12h_1}{w}]^{-0.5} & \text{for } \frac{w}{h_1} > 1 \\
[1 + \frac{12h_1}{w}]^{-0.5} + 0.04 \left[ 1 - \frac{w}{h_1} \right]^2 & \text{for } \frac{w}{h_1} \leq 1
\end{cases}
\]  

(6.34)
$\epsilon_{eff(0)}$ is calculated by the variational method for the line with a zero metal strip thickness. Such calculated $\epsilon_{r,eq}$ needs some correction factor to be determined for the appropriate accuracy. It is an experimentally determined factor, different for every line geometry [130]. An iterative solution process is needed to find its value for every analysed line geometry, which does not fit well into the numerical procedure of extracting the dielectric material permittivities. Furthermore, the line effective permittivity predictions made with this approach for a superstrate configuration follow contrary direction to that required by the field distribution changes caused by a finite strip thickness. The use of Eqs. 6.30 and 6.31 allows direct calculation of the equivalent single-layer dielectric constant, $\epsilon_{r,eq}$, independently of any line width and metal strip thickness.

Knowing the new effective line width, $w_{eqZ}$, the previously described variational or conformal mapping analysis is used to calculate $\epsilon_{eff(0)}(w_{eqZ})$ (see Eq. 6.17). Next, we follow the standard procedure for a single-layer microstrip line configuration to calculate the final static values of line effective dielectric permittivity, $\epsilon_{reff}^{\text{static}}$, and characteristic impedance, $Z_0^{\text{static}}$, for the multi-layer microstrip line (see Eqs. 6.17 and 6.16).

### 6.5.2. Modelling of high-frequency dispersion

A validity range of the model for the considered multi-layer microstrip lines is extended to higher frequencies using the previously described dispersion formulas for single-layer substrates (see Sec. 6.4.2 and Appendix C). The above calculated quasi-static effective permittivity, $\epsilon_{reff}^{\text{static}}$, characteristic impedance, $Z_0^{\text{static}}$, and effective line width, $w_{eqZ}$, are the input parameters for these high-frequency dispersion formulas. The equivalent single-layer dielectric permittivity, $\epsilon_{r,eq}$, is an additional input parameter to be known. It is calculated using Eq. 6.30 for the composite dielectric substrate, the same as for the above considered influence of a finite strip thickness in the quasi-static analysis. For the superstrate build-up, Eq. 6.32 based on conformal mapping is used, which is different from the static calculations.

It should be noticed that the dispersion characteristics of a general multi-layer microstrip line can be, in general, more complicated than for a single-layer build-up. In [125], it was shown that with an increase in frequency, the effective relative permittivity of a multi-layer microstrip line does not move towards $\epsilon_{r,eq}$. This is a result of the field lines moving towards the dielectric layer of higher permittivity, bringing the gap between $\epsilon_{r,eq}$ and real relative permittivity of higher value. For some multi-layer microstrip line build-ups and appropriately high frequencies [125], it can lead to frequency-dependence
of dispersion characteristics \( \frac{\partial \varepsilon_{\text{ref}}(f)}{\partial f} \) modified to such an extent that cannot be modelled by the high-frequency dispersion formulas for a single-layer microstrip line. To address this issue, Verma [125] introduced the concept of a virtual relative permittivity. It is a line geometry- and frequency-dependent input parameter of the modified Kirschning and Jansen dispersion model, replacing the former \( \varepsilon_r \). For a two-layer composite dielectric build-up, a set of empirical equations, modelling the virtual relative permittivity as a combination of the quasi-static \( \varepsilon_{r,eq} \) and some frequency-dependent part, was also given. However, modifications of the dispersion models, according to [125], were not implemented because the above analysed effects were not observed within the considered frequency range of 1–100 GHz for the line build-ups and substrate dielectric permittivities used within this work.

### 6.5.3. Dielectric loss tangent

A general relation between the \( G_{\text{dyn}} \) element of a distributed equivalent transmission line model (see Sec. 6.2) and the contributing loss tangents of the composite dielectrics was developed [115]. The process of deriving this formula is given below.

It can be shown that the power accumulated by the electric field, \( \omega W_e \), and the power dissipated, \( P_v \), in a lossy dielectric can be related by [123]:

\[
\omega \cdot \frac{W_e}{P_v} = \frac{1}{\tan\delta} \quad (6.35)
\]

By the superposition method for a multi-layer configuration composed of the linear substrates, the above can be expressed as

\[
P_v = P_{v1} + P_{v2} + \cdots = \omega \cdot W_e \cdot \tan\delta_{eq} \quad (6.36)
\]

where \( P_{vj} \) are the dielectric losses associated with every of the dielectric layers used and \( \tan\delta_{eq} \) is an equivalent loss tangent of a virtual dielectric substrate dissipating the same power as in all the dielectric layers altogether. Substituting the results of Eq. 6.35 for every constituent \( P_{vj} \) into Eq. 6.36 one arrives at

\[
\frac{W_{e1}}{W_e} \cdot \tan\delta_1 + \frac{W_{e2}}{W_e} \cdot \tan\delta_2 + \cdots = \tan\delta_{eq} \quad (6.37)
\]

where \( W_{ej} \) denote the electric field accumulated power in every of the dielectric layers. From the perturbation method [139], the contributing unloaded dielectric quality factors for every dielectric layer can be approximated by

\[
\frac{1}{Q_{Dj}} = \frac{W_{ej}}{W_e} \cdot \tan\delta_j = \frac{\varepsilon_{rj}}{C_{\text{dyn}}} \frac{\partial C_{\text{dyn}}}{\partial \varepsilon_{rj}} \cdot \tan\delta_j \quad (6.38)
\]
6.5. Multi-layer dielectric configurations

\[ \frac{\varepsilon_{r1}}{C_{dyn}} \cdot \frac{\partial C_{dyn}}{\partial \varepsilon_{r1}} \cdot \tan \delta_1 + \frac{\varepsilon_{r2}}{C_{dyn}} \cdot \frac{\partial C_{dyn}}{\partial \varepsilon_{r2}} \cdot \tan \delta_2 + \cdots = \tan \delta_{eq} \]  \hspace{1cm} (6.39)

Taking into consideration that \( G_{dyn} \) and \( \tan \delta_{eq} \) are related by

\[ G_{dyn} = \omega \cdot C_{dyn} \cdot \tan \delta_{eq} \]  \hspace{1cm} (6.40)

the final expression for \( G_{dyn} \) takes the form:

\[ G_{dyn} = \omega \cdot \left( \varepsilon_{r1} \cdot \frac{\partial C_{dyn}}{\partial \varepsilon_{r1}} \cdot \tan \delta_1 + \varepsilon_{r2} \cdot \frac{\partial C_{dyn}}{\partial \varepsilon_{r2}} \cdot \tan \delta_2 + \cdots \right) \]  \hspace{1cm} (6.41)

\( C_{dyn} \) is a dynamic value of the line capacitance, known at the extraction stage of the dielectric loss tangents. The partial derivatives \( \partial C_{dyn}/\partial \varepsilon_{rj} \) are calculated by applying a gradient method to the previously derived closed-form expressions.

6.5.4. Accuracy results

The accuracy of the models for the thin multi-layer microstrip lines was calculated for the "calculation mode" (see Sec. 6.4.3 for definition) using the rms measure taken over a set of 30–300 \( \mu m \) wide microstrip lines and a metallisation strip thickness of 0, 1, 3, 10 and 17 \( \mu m \) (see also Sec. 6.3), similarly to the single dielectric case. The rms errors for six different two-layer composite dielectric and superstrate build-ups used within this work (see Table 6.3) are gathered in Table 6.4. The variational method is chosen for quasi-static calculations because the conformal formulas by Svacina

| Build-up 1 \( t \in \{0, 10, 17\} [\mu m] \) | Speedboard C | h1 = 38 \( \mu m \) \\ | | Espanex | h2 = 25 \( \mu m \) \\ | Build-up 2 \( t \in \{0, 10, 17\} [\mu m] \) | Speedboard C | h1 = 38 \( \mu m \) \\ | | Biac LCP | h2 = 25 \( \mu m \) \\ | Build-up 3 \( t \in \{0, 10, 17\} [\mu m] \) | Microlam 410 | h1 = 38 \( \mu m \) \\ | | Arlon 85NT | h2 = 47 \( \mu m \) \\ | Build-up 4 \( t \in \{0, 10, 17\} [\mu m] \) | Microlam 410 | h1 = 38 \( \mu m \) \\ | | Biac LCP | h2 = 25 \( \mu m \) \\ | Passivation \( t \in \{0, 1, 3\} [\mu m] \) | BCB | h1 + h2 = 45 \( \mu m \) \\ | | BCB | h3 \in \{3, 8\} [\mu m] \\ |
Table 6.4: Accuracy of the closed-form expressions for the composite and superstrate configurations (see Fig. 6.9 and Table 6.3 for the build-ups definition). The rms error is taken over a set of 30–300 µm wide microstrip lines and a metallisation strip thickness of 0, 1, 3, 10 and 17 µm. ($Z_{pi}$ - power-current defined microstrip characteristic impedance).

<table>
<thead>
<tr>
<th>Build-up</th>
<th>$\varepsilon_r$ rms error [%]</th>
<th>$Z_{pi}$ rms error [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Build-up 1</td>
<td>0.54</td>
<td>0.45</td>
</tr>
<tr>
<td>Build-up 2</td>
<td>0.31</td>
<td>0.52</td>
</tr>
<tr>
<td>Build-up 3</td>
<td>0.42</td>
<td>0.39</td>
</tr>
<tr>
<td>Build-up 4</td>
<td>0.24</td>
<td>0.5</td>
</tr>
<tr>
<td>Passivation ($h_3 = 3\mu m$)</td>
<td>0.76</td>
<td>0.4</td>
</tr>
<tr>
<td>Passivation ($h_3 = 8\mu m$)</td>
<td>0.87</td>
<td>0.45</td>
</tr>
</tbody>
</table>

[134, 135] (see Appendix D) result in a substantially higher approximation error, coming up to 3–4% for narrow lines (30–50 µm wide). The use of Eqs. 6.30 and 6.31 to account for a final metal strip thickness gives two times lower errors than Eq. 6.32 based on conformal mapping [130]. For the line characteristic impedance, the power-current definition with dispersion model by Jansen [133] (Eq. C.13) is chosen, whereas for the line effective dielectric constant, the model of Kobayashi [128] (Eq. C.7). Figs. 6.10 and 6.11 show frequency-dependent $Z_0$ and $\varepsilon_{reff}$ for some representative lossless multi-layer microstrip lines calculated by closed-form models and simulated with HFSS. Almost perfect match between both can be noticed. The frequency-dependent approximation error for the same line geometries is shown in Fig. 6.12 in a more detailed way.

The calculated rms accuracy of the extraction procedure in the "extraction mode" (see Sec. 6.4.3) is 0.68% and 0.95% for the two-layer composite dielectric and superstrate configurations, respectively. The analysed build-ups from Table 6.3 and lines geometries specified in Table 6.4 were taken into account in the calculations. The lower overall extraction accuracy for the lines with passivation is a result of higher approximation error of the quasi-static line effective permittivity for narrow lines calculated with variational analysis.

In principle, the extraction process for the multi-layer configurations can be formulated in terms of the lines of different widths that are laid on the same dielectric build-up. As the extraction problem in this case needs a multi-dimensional search of roots, some minimum differences between the dielectric permittivities of the constituent dielectric layers and between the line widths are required in order to avoid an ill-conditioned problem. The required minimum differences are dependent on the approximation errors of the used
Figure 6.10: Comparison of the line effective permittivities calculated by the closed-form equation models and simulated by HFSS for different lossless multi-layer microstrip lines (Parameters t and w denote a metal strip thickness and a line width, respectively; see Table 6.3 for the build-ups definition).

Figure 6.11: Comparison of the line characteristic impedance calculated by the closed-form equation models and simulated by HFSS for different lossless multi-layer microstrip lines (Parameters t and w denote a metal strip thickness and a line width, respectively; see Table 6.3 for the build-ups definition).

closed-form expressions and the measurement accuracy. The use of Eqs. D.3–D.12 in Appendix D, defining conformal filling factors for the multi-layer build-ups, could be a valuable help in checking how large spread in the line widths and dielectric constant values is needed for the acceptable extraction accuracy.

The extraction errors of dielectric material permittivities for the Speed-
Figure 6.12: Frequency-dependent approximation error of the closed-form $\varepsilon_{reff}$ models for different lossless multi-layer microstrip lines. The reference input data comes from the 2D HFSS simulations. (Parameters $t$ and $w$ denote a metal strip thickness and a line width, respectively; see Table 6.3 for the build-ups definition).

board C/Espanex composite build-up (denoted as "build-up 1" in Table 6.3), with the a priori assumed difference in both dielectric constant values of 0.83, are presented in Table 6.5. It can be noticed that the extraction error stays below 1% for both dielectrics if the lines as narrow as 70 $\mu$m combined with the lines wider than 200 $\mu$m are used in the extraction process. For the other two-layer composite build-ups analysed in this work (see Table 6.3) with differences between both dielectric permittivities below 0.4, the extraction errors are larger than 1% within the considered line widths of 30–300 $\mu$m. For these dielectric build-ups, a modified extraction process is defined. In this case, one line standard is built on a single dielectric layer (only adhesion film) and the second one is a two-layer microstrip line with the same bottom dielectric layer as that in the first line standard. This modification substantially simplifies the root searching process. In a result, any minimum spread in the line widths and dielectric permittivities is not needed. The previously given rms extraction error for the "extraction mode" is specified for this modified approach.

The $\varepsilon_r$ extraction results for some representative microstrip line geometries are shown in Fig. 6.13. The input data set comes from 2D HFSS simulations of both lossless and lossy microstrip lines. The shown results are defined for the modified extraction process, wherein the first line standard ($w_1$ in Fig. 6.13) is a single dielectric configuration based on the adhesion film (Speedboard C, Microlam 410) and the second one, ($w_2$ in Fig. 6.13), is a two-layer dielectric build-up with the same bottom dielectric layer. Per-
Table 6.5: Error [in %] of the extracted $\varepsilon_r$ values for the Speedboard C/Espanex composite build-up (“build-up 1” in Table 6.3). The input reference data comes from 2D HFSS simulations of lossy lines (both ohmic and dielectric losses included). The dielectric permittivities of 2.67 and 3.5 for Speedboard C and Espanex, respectively, and a copper strip thickness of 17 $\mu$m were assumed in simulations (Parameters $w_1$ and $w_2$ denote the strip widths of two microstrip line standards used in the extraction process).

<table>
<thead>
<tr>
<th>$w_1/w_2$ [(\mu\text{m})]</th>
<th>30</th>
<th>50</th>
<th>70</th>
<th>100</th>
<th>150</th>
<th>200</th>
<th>300</th>
</tr>
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<tbody>
<tr>
<td>30</td>
<td>x</td>
<td>2.25/1.22</td>
<td>1.55/0.76</td>
<td>1.57/0.75</td>
<td>1.28/0.55</td>
<td>0.53/0.15</td>
<td>0.49/0.24</td>
</tr>
<tr>
<td>50</td>
<td>x</td>
<td>1.44/0.65</td>
<td>1.68/0.74</td>
<td>1.26/0.43</td>
<td>0.35/0.54</td>
<td>0.33/0.67</td>
<td></td>
</tr>
<tr>
<td>70</td>
<td>x</td>
<td>2.40/1.47</td>
<td>1.40/0.59</td>
<td>0.32/0.97</td>
<td>0.44/1.09</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>x</td>
<td>0.80/1.35</td>
<td>0.99/2.05</td>
<td>0.94/1.91</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>150</td>
<td>x</td>
<td></td>
<td>3.48/5.84</td>
<td>2.12/3.88</td>
<td></td>
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<tr>
<td>200</td>
<td></td>
<td></td>
<td></td>
<td>1.02/2.10</td>
<td></td>
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<td>300</td>
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</table>

Figure 6.13: Dielectric permittivities extracted using the closed-form equation models. The input reference data comes from 2D HFSS simulations of both lossless and lossy lines (both ohmic and dielectric losses included). Two composite dielectric build-ups are shown: Speedboard C/Espanex (“bu-1”) and Microlam 410/Arlon 85NT (“bu-3”) (see Table 6.3). The dielectric permittivities of 2.67, 3.5, 3.4 and 3.8 for Speedboard, Espanex, Microlam and Arlon, respectively, were assumed in simulations (Parameters $t$, $w_1$ and $w_2$ denote a metal strip thickness and the line widths of two microstrip line standards used in the extraction process, respectively).

The perfect agreement between the extracted values for both data sets proves high accuracy of the decoupling property of the procedure between complex dielectric permittivities and metallisation-related parameters. As the theoretical dielectric constants and loss tangents, being the input parameters for the
Figure 6.14: Frequency-dependent approximation error of the closed-form $\varepsilon_{\text{reff}}$ models for different multi-layer microstrip lines. (For the symbol explanation and description of the drawing refer to Fig. 6.13).

Figure 6.15: Dielectric loss tangents of Speedboard C, Espanex, Microlam 410 and Arlon 85NT extracted from the line conductance per unit length, $G_{\text{dyn}}$ (see Eq. 6.41), using the closed-form equation models for the two-layer dielectric microstrip lines. The input reference data comes from 2D HFSS simulations of lossy lines (both ohmic and dielectric losses included). A copper conductor for metallisation layers and the loss tangents of 0.0053, 0.007, 0.008 and 0.015 for Speedboard C, Espanex, Microlam 410 and Arlon 85NT, respectively, were assumed in simulations (For the symbol explanation and description of the drawing refer to Fig. 6.13).

reference full-wave simulations, are known and frequency independent, it is possible to check the extraction accuracy independently for every frequency. This is shown in Fig. 6.14 for the same line geometries as those in Fig. 6.13.
Fig. 6.15 presents the extracted dielectric loss tangents for the two chosen two-layer build-ups, using Eq. 6.41. Comparing the extracted loss tangents with the a priori assumed values from Table 6.1, a very good agreement can be observed.

![Graph](image)

**Figure 6.16**: Comparison of the frequency-dependent extraction error of the BCB dielectric constant for a superstrate microstrip configuration, when considering and ignoring the presence of (a) a 3 µm thick and (b) an 8 µm thick BCB passivation layer. (Parameters t and w denote a metal strip thickness and a microstrip line width, respectively; see Table 6.3 for the build-ups definition).

The last figure, Fig. 6.16, shows the extraction errors of the BCB dielectric permittivity from the microstrip lines in a superstrate configuration, when
ignoring the presence of a passivation layer in the extraction process. Errors coming up to 7% and 15% can be generated for the neglected 3 μm and 8 μm thick BCB cover layers, respectively. This shows the necessity for the precise geometrical characterisation of line cross-sections (with reading accuracy down to 1 μm) for an accurate extraction of dielectric permittivities.

6.6. Extraction results

In this section, some representative extraction results will be presented, indicating some other related issues such as calibration inaccuracies, line length choice for the microstrip line standards or processing accuracy for the considered technology build-ups.

**Complex propagation constant de-embedding**

The complex propagation constants, $\gamma = \alpha + j\beta$, for different, previously considered, microstrip line build-ups were de-embedded using the technique from Sec. 5.2. The lengths for the measured line standards were chosen according to the accuracy considerations from Sec. 5.5.2 and they are 1 mm (THRU), 1.8 mm and 4.2 mm (LINE). Both 1–4.2 mm and 1.8–4.2 mm line combinations result in practically the same extracted $\varepsilon_{reff}$ values, within ± 0.005 margin, whereas those de-embedded from 1–1.8 mm line pairs show a deviation of 0.02–0.03 in comparison to the longer lines, indicating insufficient line length difference.

Additional factors determining the extraction accuracy are the manufacturing tolerances and the positioning errors of the probe-tips. The latter was observed to be within ± 5 μm. From the point of view of the process tolerances, a via misalignment (basic element of the feed transitions) is of special importance for asymmetry between feed error boxes on both sides of every line standard and for their repeatability between different line standards used in the extraction procedure. For the BCB thin-film technologies, this misalignment was observed to be below ± 2 μm, whereas for the composite dielectric laminate build-ups, ± 10–15 μm, thus, lowering the extraction accuracy for the MCM-L technologies.

Some examples of the extracted line effective permittivities for different microstrip line build-ups are presented in Fig. 6.17(a) (for definition of the single dielectric build-up, see Table 6.2 and for the composite dielectric and superstrate configurations, Table 6.3, and Fig. 6.9) The largest high-frequency dispersion level of a few % at 100 GHz can be observed for a 410 μm wide microstrip line on the Microlam / Biac LCP composite dielectric build-up, in-
6.6. Extraction results

directly indicating no or low material dispersion. The frequency behaviour of
the narrow lines (20 \( \mu \)m wide BCB microstrip line), contrary to the previous
case, is dominated by the slow-wave effects within the entire measured fre-
quency range. Some typical examples of the de-embedded line losses for the

![Graph](image)

**Figure 6.17:** Comparison of the extracted line effective permittivities and
line losses for the MCM-D and MCM-L technologies. "BCB" and "BCB-
PASS" denote single layer and superstrate BCB thin-film build-ups, respec-
tively. "SPD-ESP", "MICR-BIAC" and "SPD-BIAC" stand for the Speed-
board C/ Espanex, Microlam 410/ BIAC LCP and Speedboard C/ Biac LCP
two-layer dielectric build-ups from Table 6.3. (Parameters \( t \) and \( w \) denote a copper
strip thickness and a microstrip line width, respectively.)

microstrip line geometries corresponding to the characteristic impedance val-
ues of 45–55 Ω are depicted in Fig. 6.17(b). The thin-film BCB lines outperform any of the laminate counterparts, even if the thinner substrate (45 μm vs. 63 μm), narrower lines and substantially thinner metal strips are used. This is due to almost perfect surface roughness of only few nm, very precise line edge definition and lower dielectric loss tangent. The measured $rms$ surface roughness of 440-630 nm for the laminate build-ups results in practically doubled ohmic losses at 60–80 GHz, when compared to the perfect conductor surface, as it exceeds the skin depth in a copper conductor at these frequencies.

**Characteristic impedance de-embedding**

Microstrip line characteristic impedances are de-embedded using the two-step technique from Sec. 5.5. As the characteristic impedance extraction problem shows some accuracy deterioration for the frequency points, for which the line length difference between $THRU$ and $LINE$ standards is equal to the multiples of half a wavelength, the proper choice of the line standards for the required frequency range is of interest. For frequencies beyond 10–15 GHz, the two shortest line standards, 1 mm and 1.8 mm long, are used. They result in a resonance-free impedance extraction up to 100 GHz. For lower frequencies, the two other line combinations, 1–4.2 mm and 1.8–4.2 mm, are used in order to catch accurately the low-frequency dispersion.

**Figure 6.18:** Extracted characteristic impedances of the BCB microstrip lines in a superstrate configuration with a BCB passivation layer of 5 μm (see Table 6.3 for the build-up definition). (Parameters $t$ and $w$ denote a copper strip thickness and a microstrip line width, respectively.)

Examples of the extracted characteristic impedances are shown in
6.6. Extraction results

Fig. 6.18. The measured lines are built using the BCB thin film build-up with a 5 μm BCB passivation layer (superstrate configuration) and they cover the 25–110 Ω range. A very low high-frequency dispersion can be noticed, confirming the validity of the power-current impedance definition. A resonance-like effect between 85–100 GHz is not a physical behaviour of the microstrip line characteristic impedance but it is due to the extraction errors of the CBCPW line characteristic impedance in the first step of the de-embedding process (see Sec. 5.4). These errors are a result of the too sparsely located vias shorting top and bottom ground planes of the CBCPW lines, giving rise to the unintentional half a wavelength resonances between vias at about 90 GHz.

Dielectric constant de-embedding

Fig. 6.19 presents some examples of the BCB dielectric permittivity extracted by means of two approaches: the classical (using only the measured line propagation constant, γ), and the newly developed (using both line propagation constant, γ, and line characteristic impedance, Z₀). Values de-embedded from the measurements of different microstrip line widths for both single dielectric (see Table 6.2 for the build-up definition) and superstrate configurations with a BCB passivation layer of 5 μm (see Table 6.3 for the build-up definition) were used in the extraction process. The spread among all the de-embedded values is small, indicating high modelling accuracy for a wide range of microstrip line geometries.

The εᵣ values extracted using the developed technique indicate no material dispersion for the BCB film in the measured frequency range. The anomalous behaviour beyond 80 GHz is a result of the previously mentioned characteristic impedance de-embedding errors for the CBCPW lines (see Sec. 5.4). Some waviness in the de-embedded results comes mainly from the non-ideally determined characteristic impedances of both CBCPW and microstrip line standards, being sensitive to the probe-tip positioning errors and calibration imperfections. The εᵣ extraction results for the classical method prove that the BCB dielectric permittivity still shows a stable, frequency-independent, value at 80–100 GHz, the frequency range for which the previous technique failed due to errors in the de-embedded line characteristic impedances. However, this approach results in εᵣ extraction errors as high as a few % up to 40–50 GHz for the considered BCB microstrip lines due to the unaccounted for slow-wave effects (see Fig. 6.19(b)). The influence of these effects can be even more pronounced for thinner lines and for considerably higher frequencies. The higher noise level in the dielectric constant values extracted by means of the developed method is a result of the characteristic
impedance de-embedding inaccuracies.

Figure 6.19: BCB dielectric permittivity extracted by means of two approaches: the classical (using only the measured line propagation constant, $\gamma$), and the newly developed (using both line propagation constant, $\gamma$, and line characteristic impedance, $Z_0$): (a) single dielectric configuration (see Table 6.2 for the build-up definition) (b) superstrate configuration with a BCB passivation layer of 5 $\mu$m (see Table 6.3 for the build-up definition) (Parameters $t$ and $w$ denote a metal strip thickness and a microstrip line width, respectively).

Accurate extraction of the material dielectric constants required precise microstrip line geometries to be known. For this purpose, line cross-sections (Fig. 6.20) were used. It can be noticed that a metal strip profile for the all depicted build-ups can be assumed rectangular within a good approximation,
being advantageous for the accuracy of the used closed-form models.

![Microstrip line cross-sections of different laminate and thin-film technology build-ups.](image)

**Figure 6.20:** Microstrip line cross-sections of different laminate and thin-film technology build-ups. ("BCB", "Mlam/Biac", "Spd/Espanex" and "Spd/Biac" refer to the single dielectric thin-film BCB, Microlam 410/Biac LCP, Speedboard C/Espanex and Speedboard C/Biac LCP composite dielectric microstrip line configurations from Table 6.3).

The dielectric layers and metal strip thicknesses for the thin-film technologies showed small in-panel variations and could be determined in a precise way. In order to check the influence of uncertainty of the line dimensions reading (related to the manufacturing tolerances and cross-section quality) on the deviations in the extracted dielectric constant values, different tests were performed. The classical de-embedding method, based only on the measured line propagation constants, shows low sensitivity to the geometry reading errors because $\varepsilon_{ref}$ of a microstrip line is weakly dependent on the line width to substrate thickness ratio, $w/h_s$, (see Eq. 6.11). For a 112 $\mu$m wide BCB microstrip line ($50 \, \Omega$), the $\pm 1 \, \mu$m, $\pm 1 \, \mu$m and $\pm 2 \, \mu$m reading errors for a substrate height, a metal strip thickness and a line width, respectively, result in deviations of the extracted BCB dielectric permittivity below 0.005. However, the application of this method for the extraction problem of very thin microstrip lines can be substantially limited because of the mentioned slow-wave effects. The proposed method shows higher dependence on the reading errors because the line capacitance, being used in the extraction process, is proportional to the ratio of line width to substrate height ($C_{dyn} \propto w/h_s$).
Therefore, accurate geometry reading is indispensable in this case. The thickness uncertainty of ± 1 μm for a 45 μm thick BCB results in a ± 1% deviation in the extracted dielectric permittivity. In order to increase the confidence level of the extracted dielectric constants, a combination of both methods in the de-embedding process seems to be an ultimate approach. The dielectric constant values de-embedded using the classical method at the appropriately high frequencies, at which the influence of line internal inductance in a metal strip is of lesser importance, can be used as a sort of calibration for minimisation of errors induced in reading the cross-sectional dimensions.

![Graph](image)

**Figure 6.21**: Extracted dielectric permittivity of the Speedboard C laminate (composite dielectric configuration). (Indices 1–4 refer to different line width combinations used in the extraction procedure).

For the laminate microstrip lines, it is more difficult to achieve the same extraction accuracy because of a lower manufacturing accuracy than for the thin-film technologies. The factors determining this lower accuracy are mainly a line width variation of ± 2 μm within the same line standard and an increased difficulty in reading the thickness of the constituent dielectric layers. The latter issue is related to the substantially higher surface roughness of 0.44–0.63 μm and 2 μm for the rms and peak-to-peak values, respectively. Different sensitivity tests of the extracted dielectric constant values to the uncertainty of the line dimensions reading were performed, similarly to the thin-film build-ups. From this point of view, the two-layer composite Speedboard C/Espanex build-up is the most difficult because a small difference of 0.83 between dielectric permittivities of both constituent dielectric layers. The classical de-embedding method, applied to a 50 μm / 300 μm microstrip line pair, results in extraction errors of both dielectric permittivities below 1–
1.5% for every of the following dimensional uncertainties: \( \Delta w_1 = \pm 2\mu m \), \( \Delta w_2 = \pm 5\mu m \), \( \Delta h_1(h_2) = \pm 2\mu m \) and \( \Delta t = \pm 1\mu m \), separately, and for most of the combinations among them.

The extracted dielectric permittivity of the Speedboard C laminate up to 100 GHz is shown in Fig. 6.21. The artificial low-frequency dispersion, being a result of the too short line standards for this frequency range, is more pronounced than for the thin film technologies because of a substantially thicker metal strip of 10 \( \mu m \).

### 6.7. Summary

Finally, an in-situ technique for a wideband determination of complex dielectric permittivities was established. Although developed for thin dielectric layers, it could also be used for thicker dielectric materials. It is based on probe-tip measurements of microstrip lines of different line cross-sections.

As the microstrip lines are inhomogeneous dielectric build-ups and do not guide pure TEM mode, a high-frequency dispersion at mm-wave frequencies has to be considered with high accuracy. The lines used within this work fall into the group of thin microstrip lines (TMSL) with the relatively large ratio of metal strip thickness to substrate height. Therefore, phase constants and characteristic impedances of TMSL deviate considerably from the lossless case, showing typical increase toward lower and mid-frequencies as a result of the influence of the finite metal conductivity and internal line inductance. As the physical behaviour of internal line inductance in the lower- and mid-frequency ranges cannot be simply approximated, specifically for a composite metal build-up (typically used in hybrid technologies), a precise analytical prediction of the frequency behaviour of transmission line parameters, \( \gamma \) and \( Z_0 \), is practically impossible. As a result, \( \epsilon_r \) extracted directly from the measured \( \gamma \) results in large deviations. Similar extraction errors can be observed for the lines on lossy substrates such as a low-resistivity silicon.

Using a correspondence between both transmission line parameters, \( \gamma \) and \( Z_0 \), and a distributed equivalent circuit model allows to arrive at the corresponding \( C, G, L, R \) model elements, thus, avoiding the complex influence of the line loss and internal line inductance on the \( \epsilon_r \) extraction accuracy. However, it demands line characteristic impedance to be known. Finally, the material dielectric permittivities are extracted from \( C \) only. Using the already known \( C \) and \( \epsilon_r \) values, the material loss tangents could also be found from \( G \) without considering the influence of ohmic losses.

Taking the above into account, a transmission/reflection method for a wide-band extraction of material dielectric permittivities was established. It
consists of two distinct stages. The input data are the S-parameters from the probe-tip VNA measurements of microstrip lines of different line cross-sections. In the first step, transmission line parameters, $\gamma$ and $Z_0$, are extracted from the input data. For this purpose, the de-embedding techniques for the line propagation constant and line characteristic impedance from Secs. 5.2 and 5.5 are used. Due to the self-calibration property of these techniques, the influence of feed structures is fully eliminated. The open-end effects associated with the gap-coupled printed resonators are avoided and the problem of possibly considerable radiation at the measured resonance frequencies is also eliminated. The second step of the procedure performs the extraction of dielectric permittivities using the transmission line parameters, $Z_0$ and $\gamma$, known from the previous phase. These are first converted to the equivalent elements of a distributed circuit model. Next, $C$ is used to arrive at the appropriate dielectric permittivity. The kernel of the second stage of the procedure are the quasi-static closed-form analytical models for the line effective permittivity and line capacitance. They are extended by the high-frequency dispersion correction factors. For the composite dielectric substrate and superstrate build-ups, also considered within this work, an additional modelling step is needed, called single-layer reduction technique [124, 125]. In this step, an equivalent single dielectric substrate permittivity, $\epsilon_{r,eq}$, is calculated. It is used for the proper modelling of high-frequency dispersion and for the correct inclusion of a finite metal strip thickness into the quasi-static analysis.

Accuracy of the all closed-form analytical models was tested for a broad set of 30–300 $\mu$m wide single dielectric, 2-layer composite dielectric and superstrate microstrip lines realised in the considered thin-film BCB and thin laminate MCM technology build-ups. For this purpose, a reference data set from two full-wave solvers, Ensemble and HFSS, was used. An rms error of the extracted dielectric permittivities (calculated using the reference data set from the above-mentioned full-wave simulations) taken in the frequency range of 0.1–100 GHz over the mentioned set of microstrip lines is below 0.7%. Any measurement errors and manufacturing tolerances are excluded because they are technology and measurement method dependent. Some representative extraction results from the VNA measurements were presented, including the BCB dielectric constant up to 100 GHz, indicating some other issues related to the extraction accuracy such as the influence of technology manufacturing tolerances and calibration errors.
Conclusions

In this chapter, the main achieved results, being an outcome of the five basic objectives formulated in the introduction, will be summarised.

The main goal of the thesis was the development of a set of MCM integration technologies for 60–80 GHz applications. The other issues, related to the development process, were:

- to provide the precise characterisation methods of the process- and material-related parameters
- to design a comprehensive set of interconnect and functional elements for performance validation
- to develop a set of reliable calibration and de-embedding procedures for accurate measurements and modelling of the designed elements.

**MCM-D technology**

The first achievement is the development of a single substrate integration concept at 60–80 GHz using a modified multi-layer BCB-based MCM-D technology with a performance-oriented, optimally chosen dielectric thickness. The limitations of the CPW configuration usage in hybrid technologies above
50 GHz were discussed. They eventually supported the choice of the microstrip configuration, assuming that the appropriate BCB thickness can be achieved. The process of finding this optimal thickness was thoroughly analysed.

The final technology build-up is based on a 3-layer BCB dielectric with an overall thickness of 45 μm. It allows the realisation of ultra low-loss transmission lines without high-frequency dispersion up to 100 GHz and low parasitics at discontinuities. The potential of the developed process is verified by over 1000 measurement and simulation results. With the proposed MCM-D setup, the design of passive elements at 60–100 GHz is as simple as at lower microwave frequencies because most of the high-frequency effects are eliminated. The performance is highly repeatable due to the accurate metallisation definition and precise BCB thickness control.

For comparison purposes with the proposed microstrip-oriented dielectric build-up, an alternative BCB/Rogers 4003 MCM-D technology setup, allowing the use of the CPW configuration, was investigated. On the basis of different full-wave simulation and measurement results, a set of critical drawbacks of the CPW topology in hybrid technologies above 50 GHz was presented. It led to the proposal of the quasi-CPW and quasi-ACPS transmission line alternatives, taking advantage of the multi-layer build-up. Their use allows to alleviate the problem of the high line width to wavelength ratio, critical at mm-wave frequencies. This approach also results in a via-less realisation of bridges and tunnels, promoting further miniaturisation of transmission line discontinuities and, thus, easier realisation of distributed passives.

**MCM-L technology**

The other developed process is an MCM-L build-up. It is supposed to be used for the realisation of SMT compatible single die packages and standard functional mm-wave units in V-band. Such a solution will allow efficient implementation of a modular approach for the mm-wave system integration.

Active devices are positioned in cavities included in a common substrate, allowing wire-bonding suppression. The achieved relatively tight design rules should allow integration of many passive elements in V-band, however, structures demanding very narrow line width and spacing are still out of reach. Of special importance was the use of the recently developed liquid crystal polymer laminate Biac LCP from Gore with excellent thermo-mechanical and chemical properties. It was verified that Biac LCP shows outstanding dielectric properties up to 100 GHz. The line loss as low as 0.1 dB at 60 GHz was demonstrated for the microstrip lines on a 38 μm/25 μm thick Speed-
Chapter 7: Conclusions

board C/Biac LCP build-up.

Calibration and characteristic impedance de-embedding techniques

To characterise the performance of the developed MCM processes, reliable calibration techniques had to be developed. Relying on an off-wafer calibration only can lead to erroneous measurement results at mm-wave frequencies. An accurate on-wafer fabrication of calibration standards is, however, difficult if the goal is the characterisation of a newly established technology.

Therefore, a two-tier calibration technique for 2-port on-wafer measurements with probe-tips, accounting for the differences between off- and on-wafer feed structures, was implemented. It performs a full TRL or LRRM off-wafer calibration and a second-tier on-wafer calibration based on the measurement technique of two transmission lines of different lengths, THRU and LINE [3, 4]. Using this technique, the line loss and line effective permittivity can be precisely de-embedded for the on-wafer line standards arbitrarily mismatched with a measurement system.

A variety of new de-embedding techniques for the line characteristic impedance was proposed:

- A de-embedding procedure with an automatic detection of the reference plane position, valid for CPW lines on both lossless and lossy substrates. It was shown that using chain matrix formulation of the problem, the shunt feed parasitics, practically representing the feed geometry behind the probe-tips, do not influence the de-embedding process. As a result, they do not need to be modelled and can be of any arbitrary complexity.

- The symmetry of a reciprocal feed discontinuity allows to de-embed the line characteristic impedance without modelling the internal structure of this discontinuity. This symmetry condition was applied in the de-embedding process of the taper-fed CPW lines.

- The above-mentioned de-embedding process with an automatic detection of the reference plane position was applied for the characteristic impedance of Finite-Width CBCPW lines.

- A two-step characteristic impedance de-embedding technique for microstrip lines, valid at mm-wave frequencies, was developed. The use of a symmetric error box model for the FW-CBCPW-microstrip mode conversion showed its potential to catch the distributed nature of this complex transition.
An in-situ dielectric permittivity extraction for thin dielectric layers

Finally, an in-situ technique for a wideband determination of material dielectric permittivities was established. Although developed for thin dielectric layers, it could also be used for thicker dielectric materials.

It consists of two distinct stages. The input data are the S-parameters from the probe-tip VNA measurements of microstrip lines of different line cross-sections. In the first step, transmission line parameters, $\gamma$ and $Z_0$, are extracted from the input data. For this purpose, the de-embedding techniques for the line propagation constant and line characteristic impedance from Secs. 5.2 and 5.5 are used. Due to the self-calibration property of these techniques, the influence of feed structures is fully eliminated. The open-end effects associated with the gap-coupled printed resonators are avoided and the problem of possibly considerable radiation at the measured resonance frequencies is also eliminated. The second step of the procedure performs the extraction of dielectric permittivities using the transmission line parameters, $Z_0$ and $\gamma$, known from the previous phase. Using a correspondence between both transmission line parameters, and a distributed equivalent circuit model allows to arrive at the corresponding $C$, $G$, $L$ and $R$ model elements, thus, avoiding the complex influence of the line loss and internal line inductance on the $\varepsilon_r$ extraction accuracy. Next, $C$ is used to arrive at the appropriate dielectric permittivity. The kernel of the second stage of the procedure are the quasi-static closed-form analytical models for the line effective permittivity and line capacitance. They are extended by the high-frequency dispersion correction factors.

The accuracy of all closed-form analytical models was tested for a broad set of 30–300 $\mu$m wide single dielectric, 2-layer composite dielectric and superstrate microstrip lines realised in the considered thin-film BCB and thin laminate MCM technology build-ups. For this purpose, a reference data set from two full-wave solvers, Ensemble and HFSS, was used. An rms error of the extracted dielectric permittivities taken in the frequency range of 0.1–100 GHz over the mentioned set of microstrip lines is below 0.7%. Some representative extraction results from the VNA measurements were presented, including the BCB dielectric constant up to 100 GHz.
Reciprocity relations in waveguide junctions

If the waveguides are lossless, the forward and reverse transmission coefficients of a reciprocal junction are equal as a result of the Lorenz reciprocity theorem [206]. This well-known condition is especially useful if only the product of the forward and reverse transmission coefficients can be measured. This is the case for the TRL-like de-embedding algorithms, also used in this work.

With the increasing use of planar transmission lines, junctions between waveguides supporting lossy hybrid modes became common. Microwave wafer probes are good examples of such junctions. For these cases, the classical microwave circuit theories [206] fail. A general waveguide theory [91, 207] was developed that is applicable to lossy hybrid modes such as those found in CPW or microstrip lines. In this theory, the S-parameters are related to the true travelling waves in waveguides (referenced to the char-
characteristic impedance of the waveguide). As stated in Sec. 5.3, the classical TRL calibration as well as the second-tier on-wafer two-line calibration, applied within this work, result in a consistent calibration with identical reference impedances at each port equal to the characteristic impedance of the line standards. Thus, they calibrate the VNA measurements so as to measure the unique scattering matrix which relates the actual travelling waves, not some arbitrary S-matrix.

Applying the Lorentz reciprocity theorem and a general waveguide circuit theory [91] for determination of the relationship between the forward and reverse transmission coefficients of a reciprocal junction connected to uniform but otherwise arbitrary waveguides, 'n' and 'm', showed that the usual condition equating the forward and backward transmissions does not hold in general case [207]. The relation, given by Eq. A.1, involves two terms: the first one dependent on the phase angle of the characteristic impedances in the guides and the other related to the so-called reciprocity factors.

\[
\frac{S_{nm}}{S_{mn}} = \frac{K_m}{K_n} \frac{1 - \text{Im}(Z_{0m})/\text{Re}(Z_{0m})}{1 - \text{Im}(Z_{0n})/\text{Re}(Z_{0n})} \tag{A.1}
\]

The reciprocity factor \( K_n \) for the \( nth \) waveguide is given by:

\[
K_n = \frac{Z_{0n}}{|\nu_{on}|^2} \int_{\sigma_n} e_n \times h_n \cdot \tilde{n} dS = \frac{\overline{p}_{on}}{p^*_{on}} \tag{A.2}
\]

\[
p_{on} = \int_{\sigma_n} e_n \times h_n^* \cdot \tilde{n} dS \tag{A.3}
\]

\[
\overline{p}_{on} = \int_{\sigma_n} e_n \times h_n \cdot \tilde{n} dS \tag{A.4}
\]

\[
\nu_{on} = -\int_{\text{path}} e_n \cdot dl \tag{A.5}
\]

\[
Z_{0n} = \frac{|\nu_{on}|^2}{p^*_{on}} \tag{A.6}
\]

\( Z_{0n} \) is a characteristic impedance of the mode (in general complex) in every waveguide connecting the junction (see Sec. 6.4.2 for considerations on the characteristic impedance dispersion at mm-wave frequencies). It is defined from the modal transverse electric field, \( e_n \), and magnetic field, \( h_n \), of the forward propagating mode. The integration surface \( \sigma_n \) is coincident with the reference plane in the \( nth \) waveguide port, chosen far enough from the junction so that higher-order modes are insignificant. \( p_{on} \) is the complex power...
Appendix A: Reciprocity relations in waveguide junctions

Carried across the surface $\sigma_n$. The constant $\nu_{on}$ is defined by Eq. A.5 and $\vec{n}$ is the unit vector normal to the surface $\sigma_n$ directed into the junction. The integration path in Eq. A.5 lies in $\sigma_n$ and time dependence $e^{j\omega t}$ is assumed. The phase of $Z_{0n}$ is independent of the normalisation imposed by the choice of this integration path. It is fixed by the phase relation between $\epsilon_n$ and $h_n$, being an inherent property of the mode.

The condition on the $Z_{nm}$ impedance matrix elements, corresponding to that given by Eq. A.1, takes the form:

\[
\frac{Z_{nm}}{Z_{mn}} = \frac{K_m \nu_{on} \nu_{om}^*}{K_n \nu_{on}^* \nu_{om}} \tag{A.7}
\]

In general, TEM, quasi-TEM and most of the TM guides satisfy the conditions that allow the assumption $K_n = 1$ or nearly 1, specifically coplanar lines [207]. However, the influence of complex characteristic impedances of the lossy lines on the S-matrix symmetry can be of importance even for $K_n = 1$. According to Eq. A.1, the impedance or chain matrix symmetry, contrary to the S-matrix, is not influenced by normalising line characteristic impedances.

Applying above considerations to the two-tier de-embedding procedure used within this work, it can be shown that the relationship between the forward and reverse transmission coefficients of the trans-wafer error boxes is described in terms of two ratios [208]: the first between characteristic impedances and the other between reciprocity factors of off- and on-wafer line standards. When using the S-matrix formulation for the characteristic impedance de-embedding procedure, the models of trans-wafer error boxes have to reflect a change between both on- and off-wafer reference impedances. This, in turn, is typically modelled by a presence of a classical impedance transformer represented by the following cascade matrix:

\[
\begin{bmatrix}
1 & -\Gamma_{nm} \\
\Gamma_{nm} & 1
\end{bmatrix}
\]

where the following definition for $\Gamma_{nm}$ is used

\[
\Gamma_{nm} = \frac{Z_{0m} - Z_{0n}}{Z_{0m} + Z_{0n}} \tag{A.8}
\]

However, the results determined from a general waveguide theory [91] indicate that the above-given cascade matrix should be replaced by a more general formula for the complex impedance transform:

\[
\frac{1}{\sqrt{1 - \Gamma_{nm}^2}} \begin{bmatrix}
1 & \Gamma_{nm} \\
\Gamma_{nm} & 1
\end{bmatrix} \tag{A.10}
\]
Using the chain matrix formulation for the characteristic impedance deembedding problem (instead of S-matrix), it is possible to avoid the influence of a difference between complex characteristic impedances of both off- and on-wafer line standards on the S-matrix asymmetry of a feed error box.
Higher-order effects in wafer probing environment

When moving into the millimetre-wave range, accurate on-wafer testing becomes more difficult because of more significant substrate modes. In order to validate the quality of the measurements and de-embedding procedures, the influence of mode coupling and energy leaking effects has to be investigated.

The general criteria for coupling between modes are that electromagnetic fields of the two modes should not be orthogonal and that the parasitic mode should have a phase velocity equal to, or lower than the propagating mode. At mm-wave frequencies, the substrate modes can show lower velocities than that of a CPW mode (mode of interest in the measurement environment with GSG probe-tips). The frequency at which both velocities become equal is called the critical frequency. For a CPW transmission line on a dielectric substrate suspended in air, the critical frequency for $TE$ and $TM$ modes is
Appendix B: Higher-order effects in wafer probing environment

given by [209]:

\[
f_c = \sqrt{\frac{2}{\varepsilon_r - 1}} \frac{c}{\pi h} \left( \arctan A + \frac{n\pi}{2} \right)
\]  

(B.1)

where \( h \) is a substrate thickness and \( A \) is equal to \( \varepsilon_r \) for TM modes or 1 for TE modes. For a substrate covered with conductor on one side, all the even values of \( n \) for TE modes and all the odd values of \( n \) for TM modes are eliminated. At the same time, the conductor plane forms a mirror which effectively doubles the substrate thickness and lowers the critical frequencies by two for all other TE and TM modes.

![Figure B.1: Coupling effects between the CPW and TM surface wave modes (left figure) and between the CPW and TE surface wave modes (right figure) in an air-suspended dielectric substrate. (The solid lines denote the electric field lines of the CPW mode, whereas the dashed are associated with the electric field lines of the surface wave modes).](image)

The field pattern of a single slot in the probe effectively creates an electric dipole. The dipole generates a transverse electric field pattern in a dielectric slab when the probe tip is brought into contact with the slab surface. The GSG probe has two opposed dipoles that tend to cancel the transverse electric field of each other but can generate a net transverse magnetic field if the electric fields are bent into the dielectric slab. It result in coupling to the TM modes (see Fig. B.1). This observation is supported by field overlap integral calculations which predict greater coupling to the \( TM_0 \) mode than to the \( TE_0 \) mode for a coplanar waveguide on a dielectric slab [149]. From Eq. B.1, it can be noticed that the \( TE_0 \) shows the lowest critical frequency for a CPW line on an air-suspended dielectric substrate, whereas for a conductor-backed slab it is the \( TM_0 \) mode that first couples to the CPW mode. As a result, a lower leakage rate can be preserved for the finite-ground CPW lines (FGCPW) with a finite ground-plane width than for the classical configuration with the entire dielectric surface covered with ground metallisation. However, prediction of the coupling phenomena for the FGCPW topology is more complex because of different boundary conditions between and beyond the edges of the
finite ground planes, leading to interactions between $TE_0$ and $TM_0$ modes [151, 210].

Reducing the substrate height, increases the cut-off frequencies of higher-order surface waves modes. By picking it small enough these modes can be pushed above the frequency range of interest. The $TE_0$ and $TM_0$ have no cut-off frequency, hence they must be dealt with in an other manner. In order to minimise the interactions with these surface waves, the overall ground-ground spacing for a CPW line should be kept low relative to the substrate height and dielectric wavelength at the frequency range of interest [149]. The separation between the ground planes may be thought of as an antenna aperture, hence reducing this quantity reduces the radiated power (into the substrate) available for coupling to surface waves [103, 151, 210, 211].

Conductor backing of a CPW line, as is common in most of the wafer probing situations, gives rise to the parallel-plate waveguide modes. Particularly important is the presence of the zero cut-off TEM mode. The phase velocity of this mode is always smaller than that of the CPW mode. In a result, it is a source of power loss or, due to the geometrical circuit truncation, it can cause resonance phenomena in the transmission [103–105, 160]. The leakage rate to this mode increases considerably with the overall line width [149], whereas the use of a thicker substrate will lower this leakage [212]. As rule of thumb, the ratio of the line width to the substrate thickness should be kept below one, isolating the fields of the CPW mode from the backside metal plane [156].

Several methods have been proposed to eliminate the leakage and resonance problems from the measured conductor-backed CPW lines over a certain frequency range. These include the use of vias [213], absorbing materials [214] or multiple dielectric layers [215]. A practical approach can be a reduction of the ground plane width, leading to a modified CPW line configuration known as Finite-Width Conductor-Backed CPW (FW-CBCPW). A disadvantage of this configuration is that it can guide a zero cut-off microstrip-like (MSL) mode, also called coplanar microstrip mode (CPM) [103–106] (see Fig. B.2). As this mode always shows a lower phase velocity than the CPW on a single dielectric substrate, the power conversion between both modes does not occur on an infinitely long FW-CBCPW line. At discontinuities, however, energy can be transferred from one mode to the other. The coupling level depends on the details of a particular discontinuity and not only on an infinitely long line geometry. This conversion is important since the microstrip modes will not couple to the GSG coplanar probe-tips and, thus, render a measurement setup inoperable. In [103], it was shown that open-ended structures can be very good converters between the CPW and microstrip-like modes, specif-
Figure B.2: The two fundamental symmetric modes of an overmoded FW-CBCPW line: CPW (CBCPW) mode (top figure) and MSL (CPM - Coplanar Microstrip) mode (bottom figure) [103–106]. (With respect to a standard CPW without conductor-backing, the CPW, or rather CBCPW mode, in a conductor-backed substrate shows the increased electric field lines passing through the substrate. For very thin substrates, its characteristics resemble more those of classical microstrip lines that the classical CPW lines).

ically if the substrate is very thin. As a result, their application to the calibration procedures should be avoided for the conductor-backed substrates. The presence of a backside ground plane has no practical effects on the propagation characteristics of a CPW line if the ratio of a substrate thickness to a line ground-ground spacing is appropriately high in order to isolate the CPW fields from those of the MSL (CPM) mode [106, 149]. However, the use of thicker substrates may launch surface waves. Thus, an optimum thickness has to be found for the frequency range of interest, taking into consideration both coupling mechanisms.

Additionally, the overall width of a FW-CBCPW line (including the widths of both finite ground planes) should be less than half a wavelength in the dielectric substrate at the highest operating frequency in order to avoid the parasitic resonative behaviour across the line geometry [158, 159].

All the factors above outlined should be carefully analysed when performing an on-wafer calibration at mm-wave frequencies.
High-frequency dispersion of microstrip lines

In order to expand the validity range of the quasi-static closed-form expression models to higher-frequencies, the dispersion formulas by Kirschning and Jansen [126], and by Kobayashi [128] for the line effective permittivity, and by Kirschning and Jansen [133] for characteristic impedance were considered.

The parameters $\epsilon_r$, $\epsilon_{\text{reff}}$, $\epsilon_{\text{static}}$, $Z_0$, $Z_{0\text{static}}$, $w$ and $h_s$, used in the following equations, denote dielectric substrate permittivity, frequency-dependent and static values of the line effective dielectric permittivity, frequency-dependent and static values of the line characteristic impedance, strip width and substrate thickness, respectively. $F_e$ and $F_Z$ are the high-frequency dispersion factors for the line effective permittivity and line characteristic impedance, respectively.
Dispersion model of the line effective permittivity by Kirschning and Jansen [126]

\[ F_\varepsilon = \frac{\varepsilon_{\text{reff}}}{\varepsilon_{\text{reff}}^{\text{static}}} = \frac{\varepsilon_r}{\varepsilon_{\text{reff}}^{\text{static}}} - \left( \frac{\varepsilon_r}{\varepsilon_{\text{reff}}^{\text{static}}} - 1 \right) / (1 + P) \]  
\[ P = P_1 \cdot P_2 \cdot \left( 0.1844 + P_3 \cdot P_4 \right) \cdot 10 \cdot \frac{f \cdot h_s}{GHz \cdot cm} \]  
\[ P_1 = 0.27488 + \frac{w}{h_s} \cdot \left( 0.6315 + \frac{0.525}{\left( 1 + 0.157 \cdot \frac{f \cdot h_s}{GHz \cdot cm} \right)^{20}} \right) - 0.065683 \cdot \exp \left( -8.7513 \cdot \frac{w}{h_s} \right) \]  
\[ P_2 = 0.33622 \cdot (1 - \exp(-0.03442 \cdot \varepsilon_r)) \]  
\[ P_3 = 0.0363 \cdot \exp(-4.6 \cdot \frac{w}{h_s}) \cdot \left\{ 1 - \exp \left[ - \left( \frac{f \cdot h_s}{3.87 \cdot GHz \cdot cm} \right) \right] \right\} \]  
\[ P_4 = 1 + 2.751 \cdot \left\{ 1 - \exp \left[ - \left( \frac{\varepsilon_r}{15.916} \right)^8 \right] \right\} \]  

Dispersion model of the line effective permittivity by Kobayashi [128]

\[ F_\varepsilon = \frac{\varepsilon_{\text{reff}}}{\varepsilon_{\text{reff}}^{\text{static}}} = \frac{\varepsilon_r}{\varepsilon_{\text{reff}}^{\text{static}}} - \left( \frac{\varepsilon_r}{\varepsilon_{\text{reff}}^{\text{static}}} - 1 \right) / (1 + (f/f_{50})^m) \]  
\[ f_{50} = \frac{f_{K,TM_0}}{0.75 + \left( 0.75 - \frac{0.332 \cdot \varepsilon_1^{0.73}}{\varepsilon_r} \right) \frac{w}{h_s}} \]  
\[ f_{K,TM_0} = c_0 \cdot \tan^{-1} \left( \frac{\varepsilon_r \cdot \sqrt{\frac{\varepsilon_{\text{reff}}^{\text{static}} - 1}{\varepsilon_r - \varepsilon_{\text{reff}}^{\text{static}}}}} {2\pi \cdot h_s \sqrt{\varepsilon_r - \varepsilon_{\text{reff}}^{\text{static}}}} \right) \]  
\[ m = m_0 \cdot m_c \quad (\leq 2.32) \]
\[ m_0 = 1 + \frac{1}{1 + \sqrt{\frac{w}{h_s}}} + 0.32 \cdot \left( \frac{1}{1 + \sqrt{\frac{w}{h_s}}} \right)^3 \]  \hspace{1cm} (C.11)

\[ m_c = \begin{cases} 
= 1 + \frac{1.4}{1 + \frac{w}{h_s}} 
\cdot \left( 0.15 - 0.235 \cdot \exp \left( \frac{-0.45}{f_{50}} \right) \right) & (w/h_s \leq 0.7) \\
= 1 & (w/h_s \geq 0.7)
\end{cases} \]

The frequency point \( f_{50} \) is the point at which:

\[ \varepsilon_{reff} = (\varepsilon_r + \varepsilon_{static})/2 \]  \hspace{1cm} (C.12)

For the curve of \( \varepsilon_{reff} \), a horizontal line \( \varepsilon_{reff} = \varepsilon_{static} \) is a lower bound at low frequencies and the dispersion curve for \( TM_0 \) surface wave mode is a higher bound at high frequencies. The quantity \( f_{K, TM_0} \) is the frequency at the intersection point of this horizontal line and the \( TM_0 \) curve.

**Dispersion model of the power-current defined characteristic impedance by Kirschning and Jansen [133]**

\[ F_Z = \frac{Z_0(f_n)/Z_0^{static}}{(R_{13}/R_{14})^{R_{17}}} \]  \hspace{1cm} (C.13)

\[ R_{17} = R_7 \cdot (1 - 1.1241 \cdot \frac{R_{12}}{R_{16}} \cdot \exp(-0.026 \cdot f_n^{1.15656} - R_{15})) \]  \hspace{1cm} (C.14)

\[ R_{16} = 1 + 0.0503 \cdot \varepsilon_r^2 \cdot R_{11} \cdot (1 - \exp(-(\varepsilon_r^{1.36})^6)) \]  \hspace{1cm} (C.15)

\[ R_{15} = 0.707 \cdot R_{10} (f_n/12.3)^{1.097} \]  \hspace{1cm} (C.16)

\[ R_{14} = (0.9408 - R_9) \cdot (\varepsilon_{reff} f_n)^{R_8} - 0.9603 \]  \hspace{1cm} (C.17)

\[ R_{13} = 0.9408 \cdot (\varepsilon_{reff} f_n) R_8 - 0.9603 \]  \hspace{1cm} (C.18)

\[ R_{12} = 1/(1 + 0.00245 \cdot u^2) \]  \hspace{1cm} (C.19)

\[ R_{11} = (f_n/19.47)^6 / (1 + 0.0962 \cdot (f_n/19.47)^6) \]  \hspace{1cm} (C.20)

\[ R_{10} = 0.00044 \cdot \varepsilon_r^{2.136} + 0.0184 \]  \hspace{1cm} (C.21)

\[ R_9 = 5.086 \cdot R_4 \cdot \frac{R_5}{0.3838 + 0.386 \cdot R_4} \cdot \frac{\exp(-R_6)}{(\varepsilon_r - 1)^6} \]  \hspace{1cm} (C.22)

\[ R_8 (f_n/19.47)^6 \]  \hspace{1cm} (C.23)

\[ R_7 = \frac{R_5}{\varepsilon_r} \]  \hspace{1cm} (C.24)

\[ R_6 = \frac{\varepsilon_r - 1}{\varepsilon_r} \]  \hspace{1cm} (C.25)

\[ R_5 = \frac{\varepsilon_r - 1}{\varepsilon_r} \]  \hspace{1cm} (C.26)

\[ R_4 = \frac{\varepsilon_r - 1}{\varepsilon_r} \]  \hspace{1cm} (C.27)

\[ R_3 = \frac{\varepsilon_r - 1}{\varepsilon_r} \]  \hspace{1cm} (C.28)

\[ R_2 = \frac{\varepsilon_r - 1}{\varepsilon_r} \]  \hspace{1cm} (C.29)

\[ R_1 = \frac{\varepsilon_r - 1}{\varepsilon_r} \]  \hspace{1cm} (C.30)
\[R_8 = 1 + 1.275(1 - \exp(-0.004625 \cdot R_3 \cdot \\ \cdot \epsilon_r^{1.674} \cdot (f_n/18.386)^{2.745}))\] (C.23)

\[R_7 = 1.206 - 0.3144 \cdot \exp(-R_1) \cdot (1 - \exp(-R_2))\] (C.24)

\[R_6 = 22.2 \cdot u^{1.92}\] (C.25)

\[R_5 = (f_n/28.843)^{12}\] (C.26)

\[R_4 = 0.016 + (0.0514 \cdot \epsilon_r)^{4.524}\] (C.27)

\[R_3 = 4.766 \cdot \exp(-3.228 \cdot u^{0.64})\] (C.28)

\[R_2 = 0.267 \cdot u^7\] (C.29)

\[R_1 = 0.03891 \cdot \epsilon_r^{1.4}\] (C.30)

\[f_n = (f/\text{GHz}) \cdot (h_s/\text{mm})\] (C.31)

\[u = w/h_s\] (C.32)
The two representative multi-layer microstrip configurations, most often found in hybrid technologies, are considered: superstrate and two-layer composite dielectric build-ups. In the first one, the area between the strip and ground plane is composed of two different dielectrics (denoted as $\epsilon_{r1}$ and $\epsilon_{r2}$ in Fig. D.1) while above the strip there is air of permittivity $\epsilon_0$. The second build-up is a superstrate dielectric configuration, created by the existence of a passivation layer of permittivity $\epsilon_{r3}$ in some technologies.

Using the conformal mapping analysis, the approximate relations for the line effective permittivity for both considered configurations can be derived [134]:

$$
\epsilon_{reff(0)}^{sup} = \epsilon_{r1} \cdot q_{1}^{sup} + \epsilon_{r3} \cdot \frac{(1-q_{1}^{sup})^2}{\epsilon_{r3} \cdot (1-q_{1}^{sup} - q_{3}^{sup}) + q_{3}^{sup}}
$$

(D.1)
Appendix D: Conformal mapping for multi-layer microstrip lines

206

Figure D.1: A general 3-layer microstrip line build-up.

\[
\epsilon_{\text{comp}}^{\text{eff}(0)} = 1 - q_1^{\text{comp}} - q_2^{\text{comp}} + \epsilon_{r1} \cdot \epsilon_{r2} \cdot \frac{(q_1^{\text{comp}} + q_2^{\text{comp}})^2}{\epsilon_{r1} \cdot q_2^{\text{comp}} + \epsilon_{r2} \cdot q_1^{\text{comp}}} \quad (D.2)
\]

Indices 1, 2 and 3 related to different dielectric layers in multi-layer build-ups are given according to Fig. D.1. Indices sup and comp correspond to the superstrate and two-layer composite build-ups, respectively. \( q_j \) factors denote the degree of filling the cross-section of a microstrip line in a conformally mapped plane by individual dielectrics \( \epsilon_{rj} \).

Using Wheeler’s transformation [216] for a wide microstrip line (\( w/h_1 \geq 1 \) for a superstrate configuration and \( w/(h_1 + h_2) \geq 1 \) for a two-layer composite build-up), one can arrive at the above used filling factors [134] for both the superstrate and two-layer composite configurations, respectively:

\[
q_1^{\text{sup}} = 1 - 0.5 \cdot \frac{\ln \left( \frac{\pi \cdot w_{ef}}{h_1} \cdot \frac{\epsilon_{r1} \cdot \epsilon_{r2}}{\epsilon_{r3}} \right)}{w_{ef}} \quad (D.3)
\]

\[
q_3^{\text{sup}} = 1 - q_1^{\text{sup}} - 0.5 \cdot \frac{h_1 - v_e}{w_{ef}} \cdot \ln \left( \frac{w_{ef}}{h_1} \right) \cdot \frac{\cos \left( \frac{v_e \cdot \pi}{h_1} \right)}{\sin \left( \frac{v_e \cdot \pi}{h_1} \right)} + \sin \left( \frac{v_e \cdot \pi}{h_1} \right) \quad (D.4)
\]

\[
w_{ef} = w + \frac{2h_1}{\pi} \cdot \ln \left( 17.08 \cdot \left( \frac{w}{2h_1} + 0.92 \right) \right) \quad (D.5)
\]

\[
v_e = 2 \cdot \frac{h_1}{\pi} \cdot \arctan \left( \frac{\pi \cdot \frac{w_{ef}}{h_1} - 2 \left( \frac{h_1 + h_3}{h_1} - 1 \right)}{2} \right) \quad (D.6)
\]
\[ q_{comp}^1 = 0.5 \cdot \frac{h_1}{h_1 + h_2} \cdot \left\{ 1 + \frac{\pi}{4} - \frac{h_1 + h_2}{w_{ef}} \right\} \cdot \ln \left( \frac{\pi}{h_1 + h_2} \cdot w_{ef} \cdot \sin \left( \frac{\pi}{2} \cdot \frac{h_1}{h_1 + h_2} \right) + \cos \left( \frac{\pi}{2} \cdot \frac{h_1}{h_1 + h_2} \right) \right\} \]

\[ q_{comp}^2 = 1 - q_{comp}^1 - 0.5 \cdot \ln \left( \frac{\pi}{h_1 + h_2} \cdot w_{ef} - 1 \right) \frac{w_{ef}}{h_1 + h_2} \]

For narrow microstrip lines \((w/h_1 \leq 1\) for a superstrate build-up and \(w/(h_1 + h_2) \leq 1\) for a two-layer composite configuration), we get the following filling factors after [134]:

\[ q_{sup}^1 = 0.5 + \frac{0.9}{\pi \cdot \ln \left( \frac{h_1}{w} \right)} \]

\[ q_{sup}^3 = 0.5 - \frac{0.9 + \frac{\pi}{4} \cdot \ln \left( \frac{(h_1 + h_3)/h_1 + 1}{(h_1 + h_3)/h_1 + w/4h_1 - 1} \right)}{\pi \cdot \ln \left( \frac{8h_1}{w} \right)} \]

\[ q_{comp}^1 = \ln \left( \frac{1 + h_1/(h_1 + h_2)}{1 - h_1/(h_1 + h_2) + w/4(h_1 + h_2)} \right) \frac{1 + \pi}{4} - 0.5 \cdot \arccos \left\{ \frac{h_1 + h_2}{h_1} \cdot \frac{w}{8(h_1 + h_2)} \sqrt{\frac{1 + \frac{h_1}{h_1 + h_2}}{1 - \frac{h_1}{h_1 + h_2} + \frac{w}{4(h_1 + h_2)}}} \right\} \]

\[ q_{comp}^2 = 0.5 + \frac{0.9}{\pi \cdot \ln \left( \frac{(h_1 + h_2)}{w} \right)} - q_{comp}^1 \]
Appendix D: Conformal mapping for multi-layer microstrip lines
Glossary

Scalars

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q$</td>
<td>Quality factor</td>
</tr>
<tr>
<td>$R_q$</td>
<td>Surface roughness (RMS)</td>
</tr>
<tr>
<td>$R_s$</td>
<td>Surface resistance</td>
</tr>
<tr>
<td>$R_{DC}$</td>
<td>DC resistance</td>
</tr>
<tr>
<td>$R_{sheet}$</td>
<td>Sheet resistance</td>
</tr>
<tr>
<td>$Z_0$</td>
<td>Characteristic impedance</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>Loss attenuation constant</td>
</tr>
<tr>
<td>$\alpha_c$</td>
<td>Conductor loss</td>
</tr>
<tr>
<td>$\alpha_d$</td>
<td>Dielectric loss</td>
</tr>
<tr>
<td>$\beta$</td>
<td>Propagation constant</td>
</tr>
<tr>
<td>$\delta$</td>
<td>Skin depth</td>
</tr>
<tr>
<td>$\epsilon_0$</td>
<td>Free space permittivity ($= 8.85419 \cdot 10^{-12}$ F/m)</td>
</tr>
<tr>
<td>$\epsilon_r$</td>
<td>Relative dielectric permittivity</td>
</tr>
<tr>
<td>$\epsilon_{reff}$</td>
<td>Effective relative dielectric permittivity</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>Complex propagation constant</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>Wavelength</td>
</tr>
<tr>
<td>$\lambda_0$</td>
<td>Free-space wavelength</td>
</tr>
<tr>
<td>$\mu$</td>
<td>Distribution mean value</td>
</tr>
<tr>
<td>$\mu_0$</td>
<td>Free space permeability ($= 1.25663 \cdot 10^{-6}$ H/m)</td>
</tr>
<tr>
<td>$\mu_r$</td>
<td>Relative permeability</td>
</tr>
<tr>
<td>$\sigma$</td>
<td>Metal conductivity</td>
</tr>
<tr>
<td>$\omega$</td>
<td>Angular frequency</td>
</tr>
<tr>
<td>$c_0$</td>
<td>Light speed ($= 2.99792 \cdot 10^8$ m/s)</td>
</tr>
<tr>
<td>$t$</td>
<td>Metal thickness</td>
</tr>
<tr>
<td>$\tan \delta$</td>
<td>Dielectric loss tangent</td>
</tr>
<tr>
<td>$w$</td>
<td>Strip width</td>
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Abbreviations
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>3D</td>
<td>3 Dimensional</td>
</tr>
<tr>
<td>ABC</td>
<td>Absorbing Boundary Conditions</td>
</tr>
<tr>
<td>ACC</td>
<td>Adaptive Cruise Control</td>
</tr>
<tr>
<td>ACPS</td>
<td>Asymmetric Coplanar Stripline</td>
</tr>
<tr>
<td>AFM</td>
<td>Atomic Force Microscope</td>
</tr>
<tr>
<td>Ag</td>
<td>Silver</td>
</tr>
<tr>
<td>Al</td>
<td>Aluminium</td>
</tr>
<tr>
<td>Au</td>
<td>Gold</td>
</tr>
<tr>
<td>BCB</td>
<td>Benzocyclobutene</td>
</tr>
<tr>
<td>BPF</td>
<td>Band Pass Filter</td>
</tr>
<tr>
<td>CBCPW</td>
<td>Conductor-Backed Coplanar Waveguide</td>
</tr>
<tr>
<td>CPW</td>
<td>Coplanar Waveguide</td>
</tr>
<tr>
<td>CTE</td>
<td>Coefficient of Thermal Expansion</td>
</tr>
<tr>
<td>Cr</td>
<td>Chromium</td>
</tr>
<tr>
<td>Cu</td>
<td>Copper</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DOP</td>
<td>Degree Of Planarisation</td>
</tr>
<tr>
<td>DRIE</td>
<td>Deep Reactive Ion Etching</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>EDP</td>
<td>Ethylene Diamine Pyrocatechol</td>
</tr>
<tr>
<td>FEM</td>
<td>Finite Element Method</td>
</tr>
<tr>
<td>FGCPW</td>
<td>Finite-Ground Coplanar Waveguide</td>
</tr>
<tr>
<td>FW-CBCPW</td>
<td>Finite-Width Conductor-Backed Coplanar Waveguide</td>
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<tr>
<td>GCPW</td>
<td>Grounded Coplanar Waveguide</td>
</tr>
<tr>
<td>GaAs</td>
<td>Gallium Arsenide</td>
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<tr>
<td>HF</td>
<td>High Frequency</td>
</tr>
<tr>
<td>HDP</td>
<td>High Density Packaging</td>
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<tr>
<td>HFSS</td>
<td>High Frequency Structure Simulator</td>
</tr>
<tr>
<td>HTCC</td>
<td>High Temperature Co-fired Ceramics</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>IP</td>
<td>Integrated Passives</td>
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<tr>
<td>MVDS</td>
<td>Microwave Video Distribution System</td>
</tr>
<tr>
<td>LAP</td>
<td>Large Area Processing</td>
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<tr>
<td>Abbreviation</td>
<td>Description</td>
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<td>--------------</td>
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</tr>
<tr>
<td>LCP</td>
<td>Liquid Crystal Polymer</td>
</tr>
<tr>
<td>LMDS</td>
<td>Local Multipoint Distribution Systems</td>
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<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LPF</td>
<td>Low Pass Filter</td>
</tr>
<tr>
<td>LRL</td>
<td>Line-Reflect-Line</td>
</tr>
<tr>
<td>LRM</td>
<td>Line-Reflect-Match</td>
</tr>
<tr>
<td>LRRM</td>
<td>Line-Reflect-Reflect-Match</td>
</tr>
<tr>
<td>LTCC</td>
<td>Low Temperature Co-fired Ceramics</td>
</tr>
<tr>
<td>LTCC-M</td>
<td>Low Temperature Co-fired Ceramics on Metal</td>
</tr>
<tr>
<td>MCM</td>
<td>Multi Chip Module</td>
</tr>
<tr>
<td>MCM-L</td>
<td>Multi Chip Module with laminated interconnect</td>
</tr>
<tr>
<td>MCM-D</td>
<td>Multi Chip Module with deposited interconnect</td>
</tr>
<tr>
<td>M-HDI</td>
<td>Microwave High Density Interconnect</td>
</tr>
<tr>
<td>MM</td>
<td>Millimetre-Wave</td>
</tr>
<tr>
<td>MMIC</td>
<td>Monolithic Microwave Integrated Circuit</td>
</tr>
<tr>
<td>MPA</td>
<td>Medium Power Amplifier</td>
</tr>
<tr>
<td>MPRW</td>
<td>Metal Pipe Rectangular Waveguide</td>
</tr>
<tr>
<td>MSL</td>
<td>Microstrip</td>
</tr>
<tr>
<td>MVDS</td>
<td>Microwave Video Distribution System</td>
</tr>
<tr>
<td>MoM</td>
<td>Method of Moments</td>
</tr>
<tr>
<td>NIST</td>
<td>National Institute of Standards and Technology</td>
</tr>
<tr>
<td>Ni</td>
<td>Nickel</td>
</tr>
<tr>
<td>PCB/PWB</td>
<td>Printed Circuit Board/Printed Wiring Board</td>
</tr>
<tr>
<td>PEC</td>
<td>Perfect Electrical Conductor</td>
</tr>
<tr>
<td>PI</td>
<td>Polyimide</td>
</tr>
<tr>
<td>ppm</td>
<td>Parts per million ($= 10^{-6}$)</td>
</tr>
<tr>
<td>PTFE</td>
<td>Polytetrafluoroethylene</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>RMS</td>
<td>Root-Mean-Square</td>
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<tr>
<td>SBU</td>
<td>Sequential Build-Up</td>
</tr>
<tr>
<td>SDA</td>
<td>Spectral Domain Analysis</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscope</td>
</tr>
<tr>
<td>SLR</td>
<td>Single Layer Reduction</td>
</tr>
<tr>
<td>SMD</td>
<td>Surface Mount Devices</td>
</tr>
<tr>
<td>Acronym</td>
<td>Definition</td>
</tr>
<tr>
<td>---------</td>
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</tr>
<tr>
<td>SMT</td>
<td>Surface Mount Technology</td>
</tr>
<tr>
<td>SMM</td>
<td>Shielded Membrane Microstrip</td>
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<tr>
<td>SOC</td>
<td>System-on-a-Chip</td>
</tr>
<tr>
<td>SOP/SIP</td>
<td>System-on/in-a-Package</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
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<tr>
<td>SOLT</td>
<td>Short-Open-Line-Thru</td>
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<tr>
<td>SOLR</td>
<td>Short-Open-Line-Reflect</td>
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<tr>
<td>TAB</td>
<td>Tape Automated Bonding</td>
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<tr>
<td>TEM</td>
<td>Transverse Electromagnetic</td>
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<tr>
<td>Ti</td>
<td>Titanium</td>
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<tr>
<td>TL</td>
<td>Transmission Line</td>
</tr>
<tr>
<td>TMSL</td>
<td>Thin Microstrip Line</td>
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<tr>
<td>TOS</td>
<td>Tape on Substrate</td>
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<tr>
<td>TRL</td>
<td>SThru-Reflect-Line</td>
</tr>
<tr>
<td>TTL</td>
<td>Transverse Transmission Line</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
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<td>VNA</td>
<td>Vector Network Analyser</td>
</tr>
<tr>
<td>W</td>
<td>Tungsten</td>
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</tbody>
</table>
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Curriculum Vitae

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