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BiCMOS Radio-Frequency Front-Ends for Wireless-LAN Receivers

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One ought to be ashamed to make use of the wonders of science embodied in a radio set, while appreciating them as little as a cow appreciates the botanical marvels in the plant she munches.

Albert Einstein

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Contents

Abstract

This work presents the study of the design of the RF front-end for monolithic receivers, which are compliant with the wireless LAN standards at $5\,\mathrm{GHz}$, and the modifications needed for dual-band extension to the $2\,\mathrm{GHz}$ band. In particular, the implementation in BiCMOS technologies has been considered, since these are well suited for the large-scale fabrication of low-cost system-on-chip.

An important dimension of the receiver design is the choice of the architecture of the RF front-end. Among the alternatives suitable for monolithic integration, the low-IF receiver is chosen. The main issue in integrating this architecture comes from the tight requirements for the symmetry of the I and Q signals, necessary to provide sufficient rejection of the image signal. Several fabricated prototypes are presented, and demonstrate that sufficient image-rejection can be achieved with monolithic implementations at $5\,\mathrm{GHz}$ and $2\,\mathrm{GHz}$.

The design of low-noise amplifiers, microwave mixers and polyphase filters is studied in detail. Several design examples are given for individual building blocks suitable for monolithic integration.
The cascode amplifier is best suited for pre-amplification in low-power receivers. The approach chosen for input and output matching of such a cell is described extensively. Several variants are presented, including a technique for broadband tuning of the output matching and dual-band extensions of input and output matching networks.
In describing downconversion-mixer design, the focus is on active mixers, both singly- and doubly-balanced. Due to the low substrate conductivity, passive mixers are less attractive in silicon-based technologies, because it

is very difficult to limit their conversion losses: the difference in conversion gain between active and passive mixers is often in the $25-30\,\mathrm{dB}$ range. The design of several low-power monolithic active mixers is presented. In addition, one example of passive mixer is given, since these can be useful for the second downconversion step of double-downconversion receivers and reconfigurable front-ends derived from those.

The choices made for the various building blocks and architectures are validated experimentally by presenting several integrated RF front-ends. Two low-IF receivers meet the specifications for $5-6\,\mathrm{GHz}$, and a dual-band version allows operation also at $2.4\,\mathrm{GHz}$. All the circuits operate with very low power consumption.

The work presented demonstrates that monolithic low-IF receivers can be implemented with the available BiCMOS technologies at competitive power levels. State-of-the-art performances have been reached with several of the fabricated circuits.

Sommario

Questo lavoro presenta lo studio del progetto del *front-end* a radio-frequenza di ricevitori monolitici, conformi agli standard per le wireless LAN a $5\,\mathrm{GHz}$, e le modifiche richieste per le estensioni *dual-band* alla banda a $2\,\mathrm{GHz}$. In particolare, è stata considerata la realizzazione con tecnologie BiCMOS, perché queste si adattano bene alla fabbricazione su larga scala di *system-on-chip* a basso costo.

Un aspetto importante del progetto di un ricevitore è la scelta dell'architettura del *front-end* a radio-frequenza. Tra le varie alternative adatte alla integrazione monolitica è stato scelto il ricevitore *low-IF*. Il problema principale nell'integrazione di questa architettura deriva dalle stringenti esigenze di simmetria dei segnali I e Q, necessaria per fornire sufficiente reiezione del segnale immagine. Si presentano vari prototipi fabbricati, e questo dimostra che una sufficiente reiezione d'immagine può essere ottenuta con realizzazioni monolitiche a $5\,\mathrm{GHz}$ e $2\,\mathrm{GHz}$.

Il progetto di amplificatori a basso rumore, *mixer* a microonde e filtri polifase è studiato in dettaglio. Si presentano vari esempi di progetto per i singoli componenti adatti all'integrazione monolitica.
L'amplificatore *cascode* è il più adatto per la pre-amplificazione in ricevitori a basso consumo di potenza. L'approccio scelto per l'adattamento dell'ingresso e dell'uscita di questo componente è descritto per esteso. Si presentano diverse varianti, compresa una tecnica per la sintonizzazione a larga banda dell'adattamento di uscita, ed estensioni *dual-band* per le reti di adattamento di ingresso e uscita.
Nel descrivere il progetto di *mixer* per ricezione, l'attenzione è rivolta ai *mixer* attivi, sia a singolo che a doppio bilanciamento. A causa della

bassa conduttività di substrato, i *mixer* passivi sono meno promettenti in tecnologie su silicio, perché risulta molto più difficile limitare le perdite di conversione: la differenza in termini di guadagno di conversione tra *mixer* attivi e passivi è spesso nell'ordine dei $25-30\,\mathrm{dB}$. Si presenta il progetto di diversi *mixer* monolitici attivi a basso consumo di potenza. Inoltre, si descrive un esempio di *mixer* passivo, perché questi possono essere impiegati nella seconda fase di ricezione dei ricevitori *double-downconversion*, e nelle architetture riconfigurabili derivabili da questi.

Al fine di validare sperimentalmente le scelte fatte per i diversi componenti del ricevitore e la sua architettura, si presenta la caratterizzazione di diversi *front-end* integrati a radio frequenza. Due ricevitori *low-IF* soddisfano le specifiche per $5-6\,\mathrm{GHz}$, e una versione *dual-band* estende l'utilizzo anche a $2.4\,\mathrm{GHz}$. Tutti i circuiti, per il loro funzionamento, richiedono potenze di alimentazione molto basse.

Il lavoro presentato dimostra che ricevitori *low-IF* monolitici possono essere fabbricati con le tecnologie BiCMOS disponibili a valori di potenza competitivi. Prestazioni allo stato dell'arte sono state raggiunte con vari circuiti fabbricati.

Chapter 1

Introduction

The growing demand of wireless connectivity has motivated the industry to evolve beyond voice-based cellular networks. This is testified by the large availability of services for GPRS/UMTS handsets, and the number of $2\,\mathrm{GHz}$ public access-points and devices for wireless local area networks (WLANs). Recently-defined standards for WLANs operating in the $5-6\,\mathrm{GHz}$ band seek to provide substantially higher data rates to supplement, and occasionally replace, wired networks.

The IEEE 802.11b standard for the $2.4\,\mathrm{GHz}$ band is the first that actually enjoyed a noteworthy penetration in the consumer market. However, it suffers of two major problems: the relatively poor spectral efficiency and the over-crowding of its allocated band. The first problem has been solved with the definition of the backward-compatible 802.11g standard, which introduces the OFDM modulation at $2\,\mathrm{GHz}$, and the latter with the use of the $5-6\,\mathrm{GHz}$ band in 802.11a. This provides far more channels, and bandwidth with little interference from other devices. As the proliferation of wireless-enabled devices and users continues, the multi-channel advantage of $5\,\mathrm{GHz}$ systems over $2\,\mathrm{GHz}$ counterparts grows in importance.
Although the use of higher frequencies is convenient, it is complicated by the large diffusion of $2\,\mathrm{GHz}$ infrastructures: initially, $5\,\mathrm{GHz}$-only devices would be unattractive on the consumer market, due to the lack of access points. A dual-band approach combines the benefits of the availability of large additional spectrum, with the ease of covering different market seg-

ments with a single product. In addition, compatibility with different bands and standards allows to exploit spectral diversity and increase the efficiency in channel use: for example, the traffic not especially sensitive to latency issues, such as web browsing or low-volume data transfer, can be routed via the busier $2.4\,\mathrm{GHz}$, while streaming traffic, such as voice-over-IP or high-definition TV (HDTV), can benefit from the low-interference $5\,\mathrm{GHz}$ bands.

The huge potential market for wireless applications and devices feeds the competition among manufacturers and leads to the need of ever higher integration levels, lower production cost and power consumption. As a consequence, the integration level increases towards single-chip radio transceivers, which ease large-scale production and reduces costs. At the same time, the development of BiCMOS technologies, which provide fast HBTs on sub-micron CMOS, makes possible the integration of monolithic radios in a technology better suited for large-scale and low-cost fabrication than the III-V competitors.

A typical wireless device contains a number of transistors in the order of millions, but only a small fraction operates in the RF range and the rest performs low-frequency base-band analog- or digital-signal processing. In terms of number of devices, the baseband section is more complex than the RF front-end, but the latter is still the design bottleneck of the entire system. This is due to several reasons:

- RF design is a multidisciplinary field. The design of RF systems demands a good understanding of many areas that are not directly related to IC design: communication theory for the choice of modulation, RF system-level design for the transceiver architecture, IC design for the individual building blocks, microwave electronics and electromagnetic-field theory for the interaction between IC and package. The need for a higher integration level demands increasingly more *concurrent engineering*.
- RF circuits must process analog signals at high frequency with large dynamic range. Trade-offs involve noise, power consumption, linearity, gain and operating frequency. While digital circuits benefit from advances in IC technology, RF circuits do not as much: using a more advanced technology, the redesign of digital circuits for operation at higher frequencies can be trivial, but this does not hold true for RF

analog circuits. In addition, RF circuits often require components, e.g. inductors, that are difficult to integrate on chip.

- CAD environments for analysis and synthesis of RFICs have improved, but still force the designer to rely on experience and inefficient simulation techniques to predict the performance of building blocks and complete systems.

For those reasons, an important aspect of the receiver design is the choice of the system architecture for the RF front-end. Radio communication is mainly dominated by the superheterodyne receiver. Although it is the most sensitive and selective, the monolithic integration is difficult, as it requires high-quality filters at radio and intermediate frequencies. The intensive research of the past decade has rediscovered architectures, such as direct conversion and low-IF, whose inventions date back to the sixties.

The target devices for WLAN connections are in nearly all cases portable and battery operated. This includes laptops, but also mobile phones and palm-tops, since multimedia-streaming services make WLAN attractive also for handsets. In order to extend the battery lifetime, the reduction of power consumption is always an important design goal for the electronic part of the system. The circuits and building blocks operating in the selected architecture must be designed for low power consumption, by carefully selecting topology, operating point and interstage impedance levels.

This scenario motivated the work presented in this thesis, which is a contribution to the research on the integration of $5-6\,\mathrm{GHz}$ transceivers, and their multi-band extensions, in silicon-based technologies.

1.1 Organization of the Thesis

The material in this thesis is organized as follows:

Chapter 2 summarizes the main features of the WLAN standards, with particular emphasis on the requirements for the RF front-end of the receiver.

Chapter 3, after a brief introduction to BiCMOS technology, resumes the main features of the two commercially available IBM BiCMOS RF technologies, the IBM BiCMOS 6HP and IBM BiCMOS 7HP , used for the fabrication of the circuits presented in the rest of the thesis.

Chapter 4 reviews the receiver architectures suitable for monolithic integration, and discusses their advantages and disadvantages.

Chapter 5, in the first part, describes the design methodology adopted for the design of the low-noise amplifiers (LNAs), and the alternatives that have been considered for the input and output matching network of common-emitter and cascode amplifiers. In the second part, the design and implementation of some prototype is presented, together with measurement results.

Chapter 6 describes and discusses the principle exploited in most RF mixers, active and passive. The chapter presents the design and characterization of several mixers tailored for WLAN integrated receivers.

Chapter 7 summarizes the properties of the RC passive polyphase filters, their use with symmetrical signals for image rejection, the degenerate case of two-phase system for quadrature generation, and the design guidelines.

Chapter 8 presents the integration of several receiver RF front-ends: the circuits described in the previous chapters are employed for low-power monolithic implementations of front-ends operating at $5\,\mathrm{GHz}$ and $2\,\mathrm{GHz}$, complying with WLAN specifications.

Chapter 2

Wireless LAN Standards

In 1985 the Federal Communication Commission (FCC) of the United States authorized the use of the Industrial, Scientific and Medical (ISM) frequency bands. The availability of these ISM bands accelerated the development of WLANs, because vendors no longer needed to apply and pay for licences to operate their products.
In 1987 the IEEE 802.11 Working Group began elaborating on the Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications. The final draft was ratified in 1997. In 1999 the IEEE 802.11 standard was officially revised: the IEEE ratified two wireless networking communication standards, named 802.11a (for operation at $5\,\mathrm{GHz}$) [4,5] and 802.11b (at $2.4\,\mathrm{GHz}$) [6].
Later, other standards have been ratified: in order to enhance the $2.4\,\mathrm{GHz}$ technology, in 2001 the IEEE proposed the 802.11g standard [7]; the band allocation in the $5\,\mathrm{GHz}$ band was improved in 2003 with the 802.11h [8].
Meanwhile, other organizations, mostly in Europe and Japan, defined and ratified other standards, such as the ETSI HiPeRLAN/1-2 [9] (Europe) and the MMAC HiSWANa (Japan). However, the market is largely dominated by products compliant with the IEEE standards.

This chapter summarizes the main features of the mentioned standards, with particular emphasis on the requirements for the RF front-end of the receiver.

2.1 IEEE 802.11a

Although the IEEE 802.11b (§2.4) products have successfully diffused in the WLAN market, the resulting interference within the $2.4\,\mathrm{GHz}$ ISM band is a major issue. These problems motivated the definition of a standard in a less crowded band: the IEEE 802.11a standard, which uses the $5\,\mathrm{GHz}$ band, was approved in the same year as the 802.11b.

The IEEE 802.11a standard specifies operation over a $300\,\mathrm{MHz}$ allocation of spectrum, making use of the three Unlicensed National Information Infrastructure (U-NII) bands, all $100\,\mathrm{MHz}$ wide, from $5.15\,\mathrm{GHz}$ to $5.35\,\mathrm{GHz}$ and from $5.725\,\mathrm{GHz}$ to $5.825\,\mathrm{GHz}$. The bottom $100\,\mathrm{MHz}$ domain is restricted to a maximum power output of $50\,\mathrm{mW}$, the next $100\,\mathrm{MHz}$ to $250\,\mathrm{mW}$, and the top $100\,\mathrm{MHz}$ to a maximum of $1\,\mathrm{W}$. This last domain is intended to support mostly outdoor communications.

The $300\,\mathrm{MHz}$ aggregate spectrum for 802.11a nearly quadruples the band available for 802.11b/g. This is enhanced by the radically different occupancy rates of the two allocations, as the 802.11b spectrum has become increasingly crowded by various wireless technologies, such as cordless telephones and Bluetooth, but also suffers interference from microwave ovens.

The 802.11a exploits the Orthogonal Frequency Division Multiplexing (OFDM) modulation, which helps compensating the higher indoor attenuation of $5\,\mathrm{GHz}$ signals with respect to $2.4\,\mathrm{GHz}$, and supports higher data rates at the same time. OFDM subdivides a carrier into several individually modulated orthogonal subcarriers, transmitted in parallel. In 802.11a, each carrier is $20\,\mathrm{MHz}$ wide and subdivided in 52 subchannels, each about $300\,\mathrm{kHz}$ wide. Four of those channels are used for error correction. The subcarrier at the center of the channel, is not used, in order to ease the implementation of direct conversion receivers (§4.2).
The standard accommodates a variety of data rates, adapting the modulation in use to the propagation conditions. At the lowest data rate, binary phase-shift keying (BPSK) encodes $125\,\mathrm{kbit/s}$ per subchannel, resulting in a $6\,\mathrm{Mbit/s}$ data rate. Using quadrature phase-shift keying (QPSK), the data rate doubles to $250\,\mathrm{kbit/s}$ per subchannel, yielding a $12\,\mathrm{Mbit/s}$ data rate. With 16-level quadrature amplitude modulation (16-QAM), the rate increases to $24\,\mathrm{Mbit/s}$. All devices compliant with the 802.11a must support at least those three data rates, but the standard allows rates beyond

$24\,\mathrm{Mbit/s}$: using a 64-QAM permits an increase to $54\,\mathrm{Mbit/s}$. Multiple channels can also be combined to provide data rates in the same order as wired Ethernet.

2.1.1 RF Receiver Specifications

Band The standard allocates $300\,\mathrm{MHz}$ in three non-contiguous $100\,\mathrm{MHz}$ bands. In many open-literature examples it is chosen to cover only the lower $200\,\mathrm{MHz}$ [10–15], from $5.15\,\mathrm{GHz}$ to $5.35\,\mathrm{GHz}$ or the upper $100\,\mathrm{MHz}$ [16, 17], from $5.725\,\mathrm{GHz}$ to $5.825\,\mathrm{GHz}$. However, full compliance with the standard requires the input bandwidth to span $5.15-5.825\,\mathrm{GHz}$.

Gain The typical gain from the antenna to the input of the analog-to-digital converter is around $100\,\mathrm{dB}$, in order to amplify the microvolt input signal to a level that can be digitalized by a low-cost low-power ADC. Of this gain, typically $25-30\,\mathrm{dB}$ is contributed by the LNA-mixer combination [13–16, 18–21].

Sensitivity and Noise Figure The most stringent requirements are set in the $54\,\mathrm{Mbit/s}$ mode. In this case the sensitivity level is $-65\,\mathrm{dBm}$, and a SNR of $20.5\,\mathrm{dB}$ [22] has to be guaranteed at the ADC output in order to meet the specified packet error rate ($<10\%$). Under this assumption, the noise figure would be

$$NF = -65\mathrm{dBm} - [-173.8\mathrm{dBm} + 10\log(20\mathrm{MHz})] - 20.5\mathrm{dB} = 15.3\mathrm{dB} \tag{2.1}$$

Due to the very high SNR requirement, even at the minimum signal level, interference plays a significant role. For a $50\,\mathrm{ns}$ delay spread radio channel, the SNR requirement grows to approximately $26\,\mathrm{dB}$ [22], leading to a NF of about $10\,\mathrm{dB}$. However, the standard specification is independent from the characteristics of the available channel, because it requires explicitly a NF of $10\,\mathrm{dB}$ with $5\,\mathrm{dB}$ of implementation margin.

Linearity For a 10% packet error rate, the 802.11a specifies a maximum input signal of $-30\,\mathrm{dBm}$. Converting this requirement into precise iIP_3 and $\mathrm{P}_{1\,\mathrm{dB}}$ is nontrivial. As a conservative rule of thumb, the $\mathrm{P}_{1\,\mathrm{dB}}$ of the receiver should be $4\,\mathrm{dB}$ above the maximum input signal power level that must be

Table 2.1: *Transmit power levels and frequency bands in United States and Europe for the IEEE 802.11h standard.*

Frequency band (GHz)	USA	EU
$5.15-5.25$	$40\,\mathrm{mW}$	$200\,\mathrm{mW}$
$5.25-5.35$	$200\,\mathrm{mW}$	$200\,\mathrm{mW}$
$5.470-5.725$	===	$1\,\mathrm{W}$
$5.725-5.825$	$800\,\mathrm{mW}$	===

received successfully [14]. Based on this approximation, the target $P_{1\,\mathrm{dB}}$ for an 802.11a-compliant receiver is $-26\,\mathrm{dBm}$.

Image Rejection Ratio (IRR) The standard explicitly specifies adjacent-channel rejection (ACR) and alternate-adjacent-channel rejection (AACR) for all possible data rates. The more stringent requirements are given for the lowest data rate ($6\,\mathrm{Mbit/s}$): ACR is $16\,\mathrm{dB}$ and AACR $32\,\mathrm{dB}$. This implies that the receiver must provide a IRR of at least $32\,\mathrm{dB}$, if the frequency plan of the receiver makes the image frequency fall onto the alternate-adjacent channel.

2.2 IEEE 802.11h

The 802.11h specification is an addition to the 802.11 family of standards, intended to resolve interference issues introduced by the use of 802.11a in some locations, particularly with military radar systems and medical devices. The 802.11h is a spectrum-managed 802.11a, which addresses also the requirements of the European regulatory bodies. By means of a dynamic channel selection (DCS) and transmit power control (TPC) the devices operating in the $5\,\mathrm{GHz}$ band will avoid interference with techniques similar to those implemented in HiPeRLAN2 (§2.3).

From the point of view of the RF receiver requirements, the only significant change affects the frequency band allocation and transmit power, resumed in Table 2.1. With respect to 802.11a, an extra $255\,\mathrm{MHz}$ band is allocated for use in Europe in the gap left by the US regulation.

2.3 ETSI HiPeRLAN, HiPeRLAN2

The ETSI **Hi**gh **Pe**rformance **R**adio **L**ocal **A**ccess **N**etwork (HiPeRLAN) is a wireless LAN standard ratified by the European Telecommunications Standards Institute (ETSI), with adherents in Europe and recognized by the European Commission. It operates in the $5.15-5.35\,\mathrm{GHz}$ band, dividing the spectrum allocation in $24\,\mathrm{MHz}$-wide channels. Each channel nominally provides a maximum data rate of $24\,\mathrm{Mbit/s}$, using Gaussian Minimum shift keying (GMSK). In addition, a low-bit-rate mode uses frequency shift keying (FSK) to provide $1.5\,\mathrm{Mbit/s}$. In the latter mode, HiPeRLAN terminals can tolerate with ease large delay spreads in indoor environments.

HiPeRLAN2 is an evolutionary step beyond HiPeRLAN. It operates in the same three bands specified for IEEE 802.11h in Europe, with the same power levels, as resumed in Table 2.1. In addition, HiPeRLAN2 specifies the use of OFDM for the high-data-rate mode ($54\,\mathrm{Mbit/s}$) and is, for this reason, close to IEEE 802.11a/h standards.

2.3.1 RF Receiver Specifications

Band The $5.15-5.35\,\mathrm{GHz}$ frequency range is allocated for both standards and the $5.470-5.725\,\mathrm{GHz}$ for the HiPeRLAN2 only: the RF front-end must span the $5.15-5.725\,\mathrm{GHz}$ range.

Gain Under the same assumptions valid for the 802.11a, the RF gain provided by the LNA-mixer combination is about $25-30\,\mathrm{dB}$.

Sensitivity and Noise Figure At the highest data rate, the receiver must exhibit a $-70\,\mathrm{dBm}$ sensitivity over a channel bandwidth of $24\,\mathrm{MHz}$. Assuming a SNR of $12\,\mathrm{dB}$ [14], the noise figure can be estimated as follows:

$$NF = -70\mathrm{dBm} - [-173.8\mathrm{dBm} + 10\log(24\mathrm{MHz})] - 12\mathrm{dB} = 18.0\mathrm{dB} \tag{2.2}$$

Linearity The standard specifies a maximum input signal of $-25\,\mathrm{dBm}$. As in §2.1.1 for 802.11a, this sets the $\mathrm{P}_{1\,\mathrm{dB}}$ to $-21\,\mathrm{dBm}$.

Image Rejection Ratio (IRR) The standard specifies the power ratio of desired signal and non-adjacent channel at a PDU[1]-error rate of $10\,\%$, which makes nontrivial the derivation of a IRR specification for the RF front-end. Since HiPeRLAN2 uses the same modulation as 802.11a for the highest data rate with a much lower SNR, the same $32\,\mathrm{dB}$ IRR was set as target.

2.4 IEEE 802.11 and 802.11b

The IEEE 802.11 standard specifies two radio transmission schemes for wireless networking in the $2.4-2.4835\,\mathrm{GHz}$ ISM band, with data rates up to $2\,\mathrm{Mbit/s}$ based on frequency hopping spread spectrum (FHSS) and direct sequence spread spectrum (DSSS) in a radio channel of approximately $22\,\mathrm{MHz}$.

The 802.11b extended the DSSS transmission scheme: employing the same signal bandwidth, it adopted the complementary code keying (CCK), and enabled operation at $5.5\,\mathrm{Mbit/s}$ and $11\,\mathrm{Mbit/s}$. The 802.11a at $5\,\mathrm{GHz}$ does not use DSSS, but OFDM: the different physical layers makes it difficult to implement a low-cost dual-band transceiver capable of complying with both 802.11a and 802.11b standards. This problem, however, has been solved with the ratification of the 802.11g standard, which uses OFDM modulation at $2.4\,\mathrm{GHz}$.

2.4.1 RF Receiver Specifications

Band The frequency allocation is simpler than that of the $5\,\mathrm{GHz}$ standards: the 802.11b uses the $2.4-2.4835\,\mathrm{GHz}$ ISM frequency range.

Gain Under the same assumptions valid for the 802.11a, the RF gain provided by the LNA-mixer combination is about $25-30\,\mathrm{dB}$.

Sensitivity and Noise Figure The $11\,\mathrm{Mbit/s}$ operation mode is the most demanding for the receiver of the 802.11b terminal. At the maximum frame error rate of $8\,\%$, the adopted modulation scheme requires an SNR of $9.5-11.5\,\mathrm{dB}$, where the extra $2\,\mathrm{dB}$ can be added to take into account

[1] **P**rotocol **D**ata **U**nit

the effect of the multi-path channel and finite accuracy of the transmitted signal [22]. Since the channel bandwidth is $22\,\mathrm{MHz}$ and the specified sensitivity is $-76\,\mathrm{dBm}$, the noise figure can be calculated as follows:

$$NF = -76\mathrm{dBm} - [-173.8\mathrm{dBm} + 10\log(22\mathrm{MHz})] - 11.5\mathrm{dB} = 12.9\mathrm{dB} \tag{2.3}$$

Linearity The standard does not specify an intermodulation test: the linearity requirement of the receiver can only be expressed in terms of $\mathrm{P}_{1\,\mathrm{dB}}$. The standard specifies an adjacent channel rejection of $40\,\mathrm{dB}$ when the desired channel is at $-74\,\mathrm{dBm}$.
This translates to a $\mathrm{P}_{1\,\mathrm{dB}}$ of about $-30\,\mathrm{dBm}$ [22, 23][2].

Image Rejection Ratio (IRR) The standard specifies a test for the adjacent channel rejection, having $\geq 25\,\mathrm{MHz}$ separation from the wanted channel frequency. The adjacent channel rejection shall be equal or better than $35\,\mathrm{dB}$, with a frame error rate no worse than $8 \cdot 10^{-2}$ using $11\,\mathrm{Mbit/s}$ CCK modulation.

2.5 IEEE 802.11g

The 802.11g standard is backward compatible with the 802.11b, and operates in the same spectrum. The main improvement lies in the modulations used: the $1, 2, 5.5$ and $11\,\mathrm{Mbit/s}$ data rates are achieved using the same modulation techniques, allowing compliance with the older standard; OFDM is used to reach the $54\,\mathrm{Mbit/s}$. This affects the SNR ratio and the noise figure, which has to be roughly the same required for 802.11a for the highest data rate. The other specifications for the RF front-end are as for 802.11b.

[2] Actually [22] sets the $\mathrm{P}_{1\,\mathrm{dB}}$ to $-26\,\mathrm{dB}$, taking into account a $4\,\mathrm{dB}$ safety margin.

Table 2.2: *Summary of the specifications for the RF front-end of a multi-standard, multi-band receiver.*

	802.11b/g	802.11a/h, HiPeRLAN2
Band	$2.4-2.4835\,\mathrm{GHz}$	$5.15-5.825\,\mathrm{GHz}$
Gain	$25-30\,\mathrm{dB}$	$25-30\,\mathrm{dB}$
NF	$10\,\mathrm{dB}$	$10\,\mathrm{dB}$
$P_{1\,\mathrm{dB}}$	$-30\,\mathrm{dBm}$	$-21\,\mathrm{dBm}$
IRR	$35\,\mathrm{dB}$	$32\,\mathrm{dB}$
In-band emission	$<-47\,\mathrm{dBm}$	$<-47\,\mathrm{dBm}$

2.6 Multi-Band, Multi-Standard Receiver RF Front-End

Although some of the modulations used and the MAC strategies are different for the 802.11a and 802.11b standards, this has little effect on the RF front-end, as the channel bandwidth allocated to each user is always about $20\,\mathrm{MHz}$ and the power levels at the antenna are similar. It is possible to define a set of specifications for the RF front-end of a receiver, which complies with all the main standards. Table 2.2 resumes the specification for the RF performance of the receiver in the two bands of interest.

Chapter 3

BiCMOS RF Technologies

The great majority of today's global semiconductor market exploits the semiconductor silicon (Si) to realize a host for integrated circuits. This dominance relies on a number of practical advantages that Si has over the other semiconductors:

- Si can be grown in large and almost defect-free single crystals, yielding many low-cost ICs per wafer
- Si can be controllably doped with both n- and p-type impurities in a large density range
- silicon dioxide (SiO_2) is a high-quality dielectric and can be easily grown on Si, for use in isolation and passivation
- Si has excellent mechanical strength, facilitating handling and fabrication
- Si is an abundant and easily purified material

From an electronic point of view, Si is not an ideal semiconductor: the carrier mobility for both electrons and holes is rather low, and Si can be regarded as a slow semiconductor. Many of the III-V compound semiconductors (e.g. GaAs and InP) enjoy higher mobility and saturation velocities. This results in a large performance advantage for III-V technologies. The main issues related to the III-V compounds are associated with the practical

problems in making highly integrated low-cost ICs: there is no grown oxide available, wafers are smaller with much higher defect densities and less resistent mechanically. This results in lower integration levels, lower yield and higher cost. For those reasons, Si ICs are better suited to the high-volume fabrication of low-cost microprocessors and memories. RF and microwave applications, which operate at definitely higher frequencies, are typically more demanding in terms of device performances, and the poorer intrinsic speed of Si devices becomes problematic. In addition, the Si substrate, which plays a more important role at higher frequencies by means of parasitic coupling, is much more lossy than that of III-V compounds. This results in larger signal attenuation and substrate-noise coupling.

The use of SiGe alloys to bandgap-engineer Si devices makes possible to improve the performance of Si transistors to a level competitive with III-V devices for RF and microwave applications, while preserving most of the yield, cost and manufacturing advantages of conventional Si fabrication [24]. The first functional SiGe heterojunction bipolar transistor (HBT) was demonstrated by the IBM Research Division in 1987 [25, 26] and the interest of the community was directed to the technology in 1990, by the demonstration of a SiGe HBT with a cut-off frequency of $75\,\mathrm{GHz}$ [27]. At that time, this was about twice the performance of state-of-the-art Si bipolar transistors (BJT).
The BiCMOS technology, which achieved its first manufacturing qualification in 1996 [28], integrates the high-performance SiGe HBT with a CMOS technology, and is compatible with the associated CMOS process in devices, metallizations and interconnects, ASIC design system. In terms of device performance, the availability of fast HBT fills the gap with III-V technologies; at the same time, the compatibility with standard CMOS processes allows to exploit all the advantages of large-scale integration of systems and high-volume production in large wafers.

Passive components The development of BiCMOS technologies has been focused largely on the integration of high-performance SiGe HBT in a base CMOS technology. In general, passive devices can be developed from existing process steps used for transistors: resistors can be formed from CMOS FET source-drain implants; MOS capacitors from the oxide-polysilicon of

the FET gate; inductors using the last-metal option of the technology. The need for high-quality passive devices in RF applications has motivated a change in the direction of passive-component development in the last several years: in RF technologies, passive devices utilize process steps not used before by digital-IC manufactures, allowing higher performances. Examples are the thick analog metal used as last metal option for high-Q inductors, TaN resistors integrated in the back-end-of-line (BEOL) metallization for low parasitic capacitance and tolerance, high-capacitance nitride metal-insulator-metal (MIM) capacitors.

IBM RF technologies This chapter summarizes the main features of the two commercially available IBM BiCMOS RF technologies, the IBM BiCMOS 6HP [29] and IBM BiCMOS 7HP [30], used for the fabrication of the circuits presented in the following chapters. Both technologies are the result of a process flow built on a preexisting CMOS process with the addition of several extra steps, which allow the integration of bipolar SiGe devices and analog elements tailored for analog and RF applications.

3.1 IBM BiCMOS 6HP

The IBM BiCMOS 6HP technology is a process which integrates a $47\,\mathrm{GHz}$-f_t SiGe HBT with a $2.5\,\mathrm{V}$, $0.25\,\mu\mathrm{m}$ CMOS base. To improve the RF passive components, the process has thick dielectric and thick last metal level.

Figure 3.1 shows a SEM picture of the cross section of a single-base-contact HBT. It is possible to identify the emitter, base and collector tungsten contacts to the aluminum wiring. At the sides of the device, the $6\,\mu\mathrm{m}$ deep-trench isolation is visible. The deep trenches are used throughout the technology to isolate bipolar transistors, n-wells, isolate sensitive circuits from noisy circuits, and lower the parasitic capacitance of passive components.

Figure 3.1: *A SEM picture of a SiGe npn HBT of the IBM BiCMOS 6HP technology. This transistor has a minimum* $0.30\,\mu\mathrm{m}$*-wide emitter and deep trench isolation.*

Transistors Two types of HBTs are available: standard high-f_t and high breakdown. Table 3.1 resumes their electrical characteristics.
IBM BiCMOS 6HP supports two nFETs, optimized for $2.5\,\mathrm{V}$ and $3.3\,\mathrm{V}$ operation. Table 3.2 resumes the FET electrical characteristics, comparing the typical values from the parent CMOS technology with typical values obtained on BiCMOS [29]. The additional steps introduced for the fabrication of HBT and analog components have little effect on the corresponding standard CMOS, ensuring compatibility of designs.

Capacitors The technology provides both silicon-based MOS capacitors and MIM capacitors. The MOS capacitors provide capacity per unit-area of $3.1\,\mathrm{fF}/\mu\mathrm{m}^2$, but they are silicon based and exhibit a voltage dependent characteristic. The MIM capacitors are essentially voltage independent and provide a capacity per unit-area of $0.7\,\mathrm{fF}/\mu\mathrm{m}^2$ with SiO_2 dielectric and $1.5\,\mathrm{fF}/\mu\mathrm{m}^2$ with nitride dielectric. The process allows the fabrication of two-layer stacked MIM capacitors, for area saving.

Varactor The varactor diode uses the base and collector regions of the high-f_t npn HBT as a p-n diode. The diode is used in the reverse biased mode as a variable capacitor. The varactor has a capacity per unit-area of $1.225\,\mathrm{fF}/\mu\mathrm{m}^2$ when biased at $0\,\mathrm{V}$, and $2.175\,\mathrm{fF}/\mu\mathrm{m}^2$ at $2.5\,\mathrm{V}$.

Inductors On-chip spiral inductors can be implemented by means of a $4\,\mu\mathrm{m}$-thick analog metal (AM). If all the six metal layers are fabricated, the total dielectric stack is $10.15\,\mu\mathrm{m}$ thick: this is achieved by means of a last dielectric growth of $3\,\mu\mathrm{m}$ and reduces substrate losses due to eddy currents and capacitive coupling, with respect to the standard CMOS process.
A minor improvement of the Q can be obtained by placing a polysilicon patterned ground shield below the spiral. This prevents capacitive coupling to the lossy substrate and, simultaneously, suppresses eddy currents. Another advantage is that the shielding greatly reduces the coupling of noise from the substrate to the inductor. Figure 3.2(a) shows a photograph of a spiral inductor with the polysilicon patterned shield: the polysilicon is split in four quarters with slits (not all visible due to photograph resolution) in each to reduce eddy currents.
Alternatively, as shown in Figure 3.2(b), the substrate below the inductor

Table 3.1: *Characteristics of the HBTs available in the IBM BiCMOS 6HP technology [28,29].*

	High f_t	High BV
β	100	80
Peak f_t	47 GHz	27 GHz
Peak f_{max}	65 GHz	55 GHz
f_t at 30 µA (min. area)	19 GHz	–
I_C at peak f_t (min. area)	0.5 mA	–
BV_{CEO}	3.3 V	5.0 V
BV_{CBO}	10.5 V	14.0 V

can be filled with a grid of the $6\,\mu\mathrm{m}$-deep trench: this increases the resistivity of the substrate, reducing its effects, and avoids the increased capacity to ground introduced by the polysilicon shield.
At $5\,\mathrm{GHz}$, the quality factor of a $1\,\mathrm{nH}$ spiral inductor over deep-trench grid is about 16, and 18 over polysilicon shield.

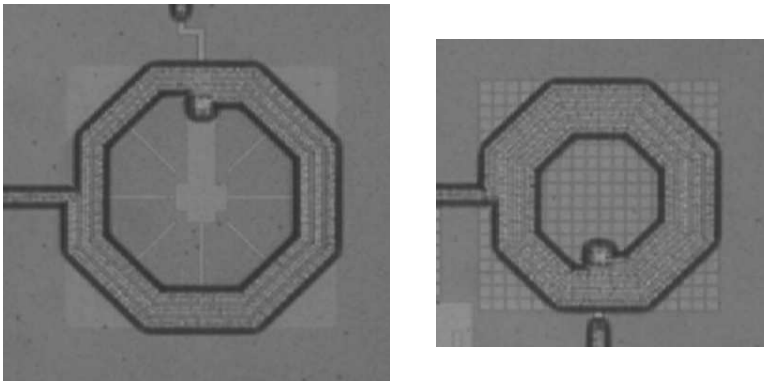
Resistors The technology allows the fabrication of four type of resistors: two p-doped polysilicon resistors and two diffusion resistors.
Polysilicon resistors are often preferred over silicon resistors, because of their low voltage and temperature sensitivity, and their low voltage-independent capacitance to the underlying ground plane. The polysilicon resistor can be placed over n+ substrate wells, for noise shielding, or over deep-trench grids, for capacitance reduction.
If a low value of sheet resistance is required, the silicon diffusion resistor are a better choice, due to the tighter tolerance. Table 3.3 summarize the characteristics of the resistors available in IBM BiCMOS 6HP .

Table 3.2: *Electrical characteristics of the FETs available in the IBM BiCMOS 6HP technology. The table compares typical values from the parent CMOS technology with typical values obtained on corresponding BiCMOS [28,29].*

Parameter	Unit	nFET		pFET		Thick ox. nFET		Thick ox. pFET	
		CMOS	BiCMOS	CMOS	BiCMOS	CMOS	BiCMOS	CMOS	BiCMOS
Gate t_{ox}	nm	6.1	6.1	6.1	6.1	8.2	8.2	8.05	8.06
Min. L *Drawn*	µm	0.240	0.240	0.240	0.240	0.400	0.400	0.340	0.340
Effective	µm	0.172	0.172	0.163	0.173	0.260	0.260	0.265	0.265
$V_{T,lin}$	V	0.500	0.503	−0.488	−0.490	0.525	0.536	−0.525	−0.539
$I_{D,sat}$ min.	µA/µm	630	642	310	305	580	568	285	278
$g_{m,sat}$	µS/µm	300	300	200	200				
f_T	GHz	35	35	20	20				
f_{max}	GHz	22	22	22	22				

Table 3.3: *Resistors available in the IBM BiCMOS 6HP technology [28,29].*

Device	Resistance	Tolerance
p– polysilicon	$3.6\,\mathrm{k}\Omega/\square$	$\pm 25\,\%$
p+ polysilicon	$210\,\Omega/\square$	$\pm 20\,\%$
Si p+	$100\,\Omega/\square$	$\pm 10\,\%$
Si n+	$63\,\Omega/\square$	$\pm 10\,\%$



(a) (b)

Figure 3.2: *Photographs of integrated spiral inductors. The quality factor can be improved by means of a polysilicon patterned shield (a) or a deep-trench grid (b).*

Table 3.4: *Characteristics of the HBTs available in the IBM BiCMOS 7HP technology [28,30].*

	High f_t	High BV
β	500	350
Peak f_t	120 GHz	27 GHz
Peak f_{max}	100 GHz	57 GHz
C_{eb}	9.5 fF/µm^2	8.5 fF/µm^2
C_{cb}	4.6 fF/µm^2	2.8 fF/µm^2
BV_{CEO}	1.8 V	4.25 V
BV_{CBO}	6.4 V	12.5 V

3.2 IBM BiCMOS 7HP

The IBM BiCMOS 7HP technology is a process integrating 120 GHz-f_t SiGe HBTs on a 1.8 V, 180 nm CMOS technology. It uses low-resistance copper wiring at the first four metal levels and aluminum for two additional thick levels, added to enable high-Q inductors and transmission lines. The process provides deep-trench isolation and high quality passive devices in the same fashion as IBM BiCMOS 6HP .

Transistors Two type of HBT are available, optimized for high f_t and high beak-down voltage. Both devices are fabricated with buried subcollector and self-aligned emitter. Table 3.4 resumes their electrical characteristics.
The FETs compare well with those of the base-CMOS technology, allowing ASIC-library compatibility [30]. In addition to the thin-oxide FET, a thicker oxide CMOS is also offered for 2.5 V and 3.3 V applications. The electrical characteristic of the FETs are summarized in Table 3.5.

Passive devices A full suite of passive devices is also supported in the technology.
Various diffusion resistors and polysilicon resistors are included, without additional process masks. As optional devices for additional masks, a high-value polysilicon resistor and a low parasitic TaN resistor can be included.

Table 3.5: *CMOS specifications, common to IBM* $180\,\mathrm{nm}$ *technology family, including IBM BiCMOS 7HP [28,30].*

	Standard		Thick oxide	
	nFET	pFET	nFET	pFET
L_{min}	$0.18\,\mu\mathrm{m}$	$0.18\,\mu\mathrm{m}$	$0.4\,\mu\mathrm{m}$	$0.4\,\mu\mathrm{m}$
L_{eff}	$0.11\,\mu\mathrm{m}$	$0.14\,\mu\mathrm{m}$	$0.29\,\mu\mathrm{m}$	$0.29\,\mu\mathrm{m}$
V_t	$0.43\,\mathrm{V}$	$-0.38\,\mathrm{V}$	$0.64\,\mathrm{V}$	$-0.67\,\mathrm{V}$
$I_{D,sat}$	$600\,\mathrm{mA}$	$260\,\mathrm{mA}$	$550\,\mathrm{mA}$	$235\,\mathrm{mA}$
T_{ox}	$3.5\,\mathrm{nm}$		$7\,\mathrm{nm}$	

Table 3.6: *Resistors available in the IBM BiCMOS 7HP technology [28,30].*

Device	Resistance	Tolerance
p– polysilicon	$1.6\,\mathrm{k}\Omega/\square$	$\pm 25\,\%$
p+ polysilicon	$260\,\Omega/\square$	$\pm 15\,\%$
Si p+	$105\,\Omega/\square$	$\pm 15\,\%$
Si n+	$72\,\Omega/\square$	$\pm 10\,\%$
Si n+ subcoll.	$8.1\,\Omega/\square$	$\pm 15\,\%$
TaN on M1	$142\,\Omega/\square$	$\pm 10\,\%$

Table 3.6 summarizes the resistor characteristics.
Both MOS ($1.0\,\mathrm{fF}/\mu\mathrm{m}^2 \pm 15\,\%$) and MIM ($2.5\,\mathrm{fF}/\mu\mathrm{m}^2 \pm 15\,\%$) capacitors are integrated. The nitride dielectric is used for MIM capacitors, allowing a higher capacitance per area and alleviating reliability concerns associated with the use of thin oxide dielectrics. Varactors are available as collector-base junctions and MOS diodes.
Inductors are built using the top thick aluminum metallization, that is separated from the substrate by over $10\,\mu\mathrm{m}$ of dielectric stack, for a typical five-metal-level run. The quality factor of a $1.6\,\mathrm{nH}$ spiral inductor over deep-trench grid is about 16 at $5\,\mathrm{GHz}$. The polysilicon patterned shield versions can be fabricated as for IBM BiCMOS 6HP, but no models are available.

Chapter 4

Receiver Architectures

Most of the commonly used receiver architectures are based on the conventional superheterodyne receiver. This receiver, in its standard version, is typically not suitable for monolithic integration, because it requires expensive and non-integrable RF and IF filters. All the other architectures of interest can be described as degenerated or enhanced variants of the superheterodyne. For this reason the superheterodyne receiver is shortly described. The rest of this chapter reviews the receiver architectures suitable for integration, and discusses their advantages and disadvantages.

4.1 Superheterodyne Receiver

The operation of the superheterodyne receiver is based on the idea of converting all the input RF channels to the same fixed lower intermediate frequency f_{IF}, in order to ease the design of the following stages, i.e. the channel selection filter and the high-gain IF amplifiers. Figure 4.1 shows the architecture of the receiver. The RF signal feeds the antenna and is filtered by a pre-selection filter (antenna filter), whose purpose is the suppression of all the out-of-band signals. The signal is then amplified by a low-noise amplifier and multiplied by a sine wave of frequency f_{LO}. This translates the desired input channel to a determined intermediate frequency (IF). The IF signal is then processed by a demodulator, whose characteristics depend on the operation frequency and type of modulation. For WLAN applications,

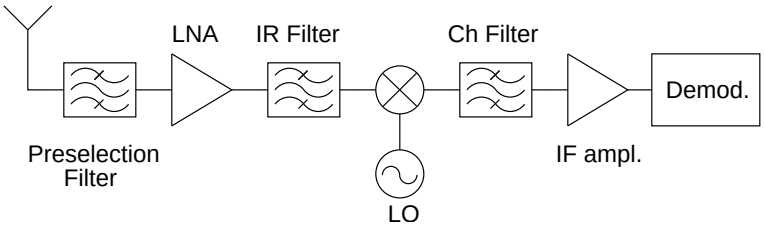


Figure 4.1: *Block diagram of a superheterodyne receiver.*

which make use of I-Q digital modulations, a second multiplication with a fixed frequency is required, in order to generate the I and Q components and further lower the frequency before digitalization [31].
By effect of the first multiplication, both the RF signals at $f_{RF,1} = f_{LO} + f_{IF}$ and $f_{RF,2} = f_{LO} - f_{IF}$ are converted to the same intermediate frequency f_{IF}. While one of the two is the desired signal, the other, called *image (signal)* is unwanted and must be suppressed. This suppression is performed by the image-reject (IR) filter and, depending on the frequency plan, the preselection filter, both shown in Figure 4.1 after and before the LNA.
The received frequency is tuned by setting the LO frequency, in order to downconvert the desired channel to the fixed IF, where most of the channel selectivity and amplification takes place. IF blocks do not need tuning.
The choice of IF is crucial. On one hand it is desirable to keep IF as low as possible, in order to simplify the design of channel filter and high gain stages of the IF amplifier; on the other hand a low IF requires a high frequency selectivity in the image-reject filter. This particular makes the standard superheterodyne receiver hardly suitable for monolithic integration: the required high-quality IF and image-reject filters cannot be integrated in modern microelectronic technologies. This architecture is used in hybrid solutions, where all parts of the receiver are monolithically integrated, excluding an external passive high-Q image-reject filter.
Besides the need for discrete external components, another major drawback of the superheterodyne receiver is that the off-chip IR filter has low input impedance. This requires high drive capabilities for the preceding LNA, leading to more severe trade-offs between gain and power dissipation in the amplifier.

4.2 Direct-Conversion Receiver

The direct-conversion receiver can be described as a degeneration of the superheterodyne receiver: the problem of image rejection is circumvented by setting the IF to zero[1], and the frequency conversion is performed by setting the LO sine wave at the same received RF frequency[2]. The RF signal is downconverted directly to baseband.
Figure 4.2 shows the block diagram of a direct conversion receiver. After preselection and low-noise amplification, the center frequency of the RF channel is downconverted to baseband. This conversion has no image frequency, thus no image rejection is needed with this architecture. However the lower-side band of the spectrum is folded on the upper side and, in order to properly receive the desired channel, a vector I-Q demodulation is necessary. Mixing with a single sinusoid would result in irreversible corruption of the transmitted information.
The IF filter and high gain amplifier do not need anymore to be bandpass blocks, but can be replaced with low-pass filters and baseband amplifiers, more suitable for monolithic integration. Furthermore, the absence of the bulky off-chip IR filter removes the LNA requirement to drive a low-impedance load. The low-frequency spectrum of the downconverted signal allows direct digitalization, so the remaining demodulation steps can be performed by the digital-signal processing (DSP) unit.
Besides all the advantages coming from block simplification, the direct-conversion receiver suffers of a number of problems that are not as serious in a heterodyne receiver or other of its variations.

DC offset The DC offsets arise from self-mixing phenomena of the LO signal or in-band large interferer. These unwanted offset voltages can corrupt the desired signal and/or saturate the stages following the mixers. The isolation between the LO and RF port of the mixers is not perfect, especially in monolithic implementation of the receiver, and a finite amount of feedthrough exists. The LO leakage signal at the RF port is mixed with the original LO and produces a DC component at the IF port. A similar effect occurs if a large interferer in the passband of the RF preselection filter leaks from the RF port to the LO port of the mixer. Those leakages, which arise

[1] For this reason, the direct conversion receiver is often called zero-IF receiver.
[2] For this reason, the direct conversion receiver is often called homodyne receiver.

from capacitive and substrate coupling, can be reduced by means of layout techniques, but cannot be entirely eliminated.
A method to eliminate the effect of the offsets is the use of AC-coupling in the signal path. Many of the spectral efficient modulation schemes currently in use exhibit significant power at DC, and such signals are corrupted by AC-coupling. However, the OFDM modulation, which subdivides a main carrier in several subcarriers, is very well suited to DC elimination: the OFDM schemes in use for IEEE802.11a/g (§2.1) (§2.5) and HiPeRLAN2 (§2.3) make no use of the center-frequency subchannel, thus eliminating the DC component of the baseband signal.

1/f noise If FETs are used for baseband stages, the signal has to deal with the 1/f noise introduced by FET.

LO leakage In addition to introducing the DC offset, the leakage of the LO signal to the RF port can reach the antenna, and radiation from there creates interference for other receivers using the same band. The use of differential LOs can reduce the coupling to the antenna [18]. The total in-band spurious radiation that can be tolerated during operation is set by international regulations: in the WLAN bands, $2.4-2.5\,\mathrm{GHz}$ and $5-6\,\mathrm{GHz}$, the maximal emission must be smaller than $-47\,\mathrm{dBm}$.

I/Q mismatch For most currently used modulation schemes, a direct conversion receiver must incorporate quadrature downconversion. This is typically done by shifting the LO signal by 90°, as shown in Figure 4.2. The errors in the nominal 90° phase-shift and the amplitude mismatch between the I and Q signals corrupt the downconverted signal constellation, increasing the bit error rate. For example, a 5° phase imbalance degrades the SNR by about $1\,\mathrm{dB}$ [18]: this level of accuracy can be reached with integrated circuits, but requires careful layouting.

Even-order distortion Even-order distortions in the LNA or the RF stage of active mixers result in near-DC components of the signal, when the amplifier is fed with two signals close in frequency. In fact, an LNA exhibiting a non-linear response such as $y(t)=\alpha_1\cdot x(t)+\alpha_2\cdot x^2(t)+\ldots$, when fed with an input $x(t)=A_1\cdot\cos\omega_1 t+A_2\cdot\cos\omega_2 t$, will show at the output a component proportional to $\alpha_2 A_1 A_2\cos(\omega_1-\omega_2)t$. This component is near DC

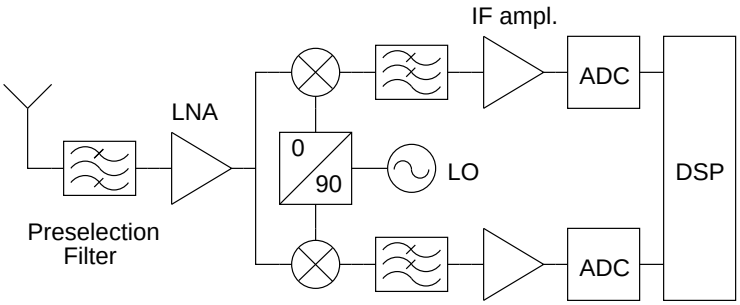


Figure 4.2: *Block diagram of a direct conversion receiver.*

when the two tones are close in frequency, and reaches the IF port of the mixer via the RF-to-IF feedthrough, present in mixers due to the asymmetries in the LO differential switches. This near DC component corrupts the downconverted signal in direct conversion receivers.
One common solution to this problem is the use of fully differential structures in the signal path. This reduces the second-order distortions to those arising from asymmetries in the differential pairs.

Despite all these problems, direct-conversion receivers are in full production for many wireless applications, such as GSM, pagers and WLAN. In many of these receivers, in order to handle the problems associated with static and dynamic offsets, DSP algorithms are used. However, these techniques add a significant amount of complexity and do not solve other problems, such as the 1/f noise or the sensitivity to even-order distortion.

4.3 Image-Rejecting Receivers

The image-reject receivers are variants of the superheterodyne, based on the use of image-reject mixers. In practice, the mixer and IR filter in Figure 4.1 are replaced with one single block, i.e. an image-rejecting mixer. Two examples, based on the Hartley [32] and Weaver [33] topologies, are given in Figure 4.3. In both the cases, it can be shown that the spectra of the signals at the input of the adders contain the desired signal with the same polar-

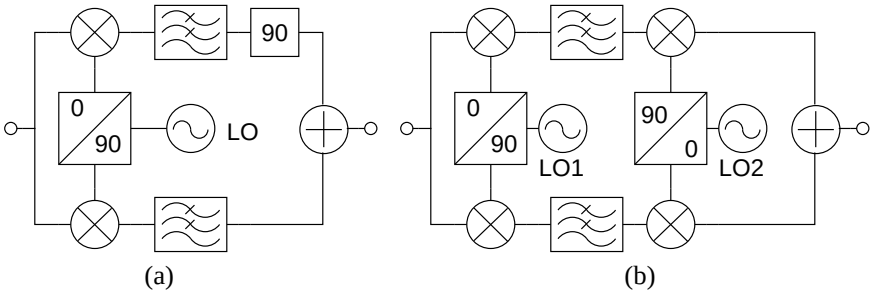


Figure 4.3: *Block diagram of two image-reject mixers: Hartley [32] (a) and Weaver [33] (b) architectures.*

ity and the image with opposite polarity [34]. Thus, in the ideal case, the summed output is free from the image.
The main issue in those architectures is the imperfect image rejection resulting from gain and phase mismatches in the two signal paths. For example, in the Hartley receiver, an amplitude mismatch of $0.3\,\mathrm{dB}$ and a phase mismatch of 3° result in an IRR of $30\,\mathrm{dB}$ [35]. From this point of view, the Weaver architecture is less demanding, since the rejection is achieved by combining LO and RF signals which are both in quadrature when applied to the second pair of mixers. It is prooven in [36] that in such a case the image rejection depends only on the second order of quadrature inaccuracy in the LO and RF signal. A quadrature inaccuracy of 2.7°, in both RF and LO signals, leads to an image rejection ratio of $60\,\mathrm{dB}$.
The advantage of this class of receivers is the suppression of the IR filter, whose required quality factor is too high for monolithic integration. Moreover, the intermediate frequency can be chosen sufficiently low to integrate the channel filter and perform most of the demodulation in the digital domain.

4.3.1 Low-IF Receiver

The low-IF receiver is a variant of the superheterodyne, where the IR filter and mixer are replaced by an image-reject mixer. This makes possible the

use of an intermediate frequency in the low-frequency range and exploit all the advantages of the heterodyne downconversion, while avoiding some of the crucial issues of the homodyne receivers (§4.2). The IF frequency is typically chosen beetween one and two times the channel bandwidth.
Practical implementations may differ significantly, depending on the IR mixer architecture chosen. If the Hartley IR mixer is chosen, then the $90°$ phase shift and the IF-signal combination can be provided by a polyphase filter, as described in §7 and demonstrated in §8.
Low-IF receivers are suitable for monolithic integration, and are often an alternative to direct conversion receivers. The two architectures have some typical issues in common, and behave differently with respect to others.

DC offset Setting the IF frequency to one or two times the channel bandwidth, the low-IF receiver can easily filter the DC offsets by means of on-chip AC coupling. Monolithic capacitors can be used, since the IF blocks have typically high input impedance.

1/f noise In CMOS implementations of the IF blocks, the 1/f noise figure does not degrade the SNR.

LO leakage The low-IF receiver suffers of LO-leakage problems to the same extent as DiCon receivers.

I/Q mismatch The low-IF receiver bases its operation on the IR mixers. Those needs very accurate quadrature to provide sufficient image rejection. The requirements are typically tighter than those for DiCon receivers.

Even-order distortion The low-IF receivers are less sensitive to the near-DC components generated by the even-order distortions in the RF gain path. In fact, the IF can be set in a band above those interferers. The reduced sensitivity to those distortions allows the use of single-ended circuits in the RF front-end of the receiver.

In comparison with the DiCon receivers, the requirements for low-IF receivers are more demanding only for the I/Q mismatch. For the other aspects, the requirements are the same, or more relaxed.

The receivers presented in §8 demonstrate that the I/Q quadrature precision necessary for WLAN can be achieved in monolithic implementations.

4.3.2 Wide-Band IF Receiver with Double Downconversion

A special kind of image-reject receiver is the wide-band IF receiver with double downconversion, which can be obtained from a superheterodyne receiver, replacing IR filter and mixer with a Weaver IR mixer. The architecture of the resulting receiver is shown in Figure 4.4. After preselection filtering and amplification, all potential RF channels are quadrature-mixed and downconverted to a broad IF band. A second quadrature-mixing rejects the image of the first downconversion. The image of the second downconversion is filtered by the low-pass filter before the mixers, if possible in the available technology and frequency plan. Alternatively the second downconversion can be a direct conversion to baseband. The schematic in Figure 4.4 has four mixers and two adders, in order to make both I and Q signals available at the DSP input. The IR mixer in Figure 4.3(b) downconverts only the I signal.
The channel selection, as in the DiCon receiver, can be performed at base band, allowing the possibility of a programmable integrated channel select filter for multi-standard applications. However, the wide-band IF receiver has some advantages over the homodyne counterpart: since there is no LO operating at the same frequency of the incoming RF signal, the problems associated with the time-varying DC offset and LO leakage are minimized. If the second downconversion translated the channel to baseband, the second LO is at the same frequency as the desired first IF: the DC offset resulting form self mixing can lead to the same problems of DiCon receivers. To avoid this, the second downconversion can be done to a low IF, using the same techniques described in §4.3.1.

4.4 Dual-Band Variants

The presented receiver architectures operate in a single band, meaning that all the blocks involved in the RF front-end are tuned to the center frequency of the band of interest and the input bandwidth is set by the resonator quality factors.

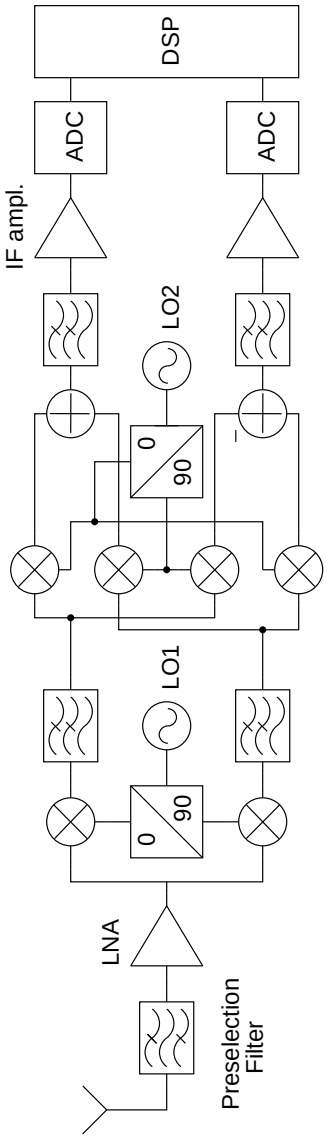


Figure 4.4: *Block diagram of a wide-band IF receiver with double down-conversion.*

In order to extend the operation of a receiver to more than one band, there are two possible strategies. Using the same static architecture for both bands, the building blocks can be implemented for operation in multiple bands. Alternatively, the system architecture can be reconfigured, and the operation in different bands requires some of the building blocks to change their function at a system level. The following paragraph introduces the system architectures considered in this work for dual-band receivers, using those two strategies.

4.4.1 Dual-Band Low-IF Receiver

A standard low-IF architecture can be used for dual-band operation, if the building blocks are all designed accordingly. An example is given in §8.2: a dual-band LNA (§5.5.4) feds the RF signal to a pair of broad band active mixers (§6.2); dual-band quadrature generation and IF signal recombination are both preformed by means of polyphase filters (§7.3).
The main drawback of this approach is that the LO signal needs to sweep over a very broad frequency range or, alternatively, to sweep over two non-contiguous bands.

4.4.2 Reconfigurable Low-IF/Wide-Band-IF Receiver

A dual-band receiver can be implemented by modifying the architecture in Figure 4.4, and by reconfiguring the system for hi- and low-frequency operation.
Many microwave mixers are based on switches driven by the LO signal: this makes them inherently capable of operating in mixer or *through* mode (§6.4.1). Exploiting this feature, a wide-band IF receiver can be modified to work as a single-downconversion or double downconversion-receiver, depending on the operation state of the second mixer array. If the mixers are in *through* mode, the low-frequency band can be downconverted to a low-IF with a single downconversion step. If the second mixer array is in mixer mode, then the high-frequency band can be downconverted to the same IF with a double-quadrature downconversion. This require a dual-band LNA (§5.5.4), broadband singly-balanced mixers (§6.2) for the first downconversion, reconfigurable mixers for the second downconversion (§6.4.1) and single-band quadrature generation (§7.3). All these blocks are suitable for monolithic integration, as demonstrated in the following chapters.

Chapter 5

Low-Noise Amplifiers

As shown in chapter 4 the LNA is the first block of the receiver front end. While terminating the antenna filter with a standard $50\,\Omega$, it has to amplify the signal adding a minimum of noise.
The first part of this chapter describes the design alternatives that have been considered for the input and output matching network of common emitter and cascode amplifiers. In the second part, the design and implementation of several prototypes are presented, together with measurement results.

5.1 Input Design

The design of the input matching network of an LNA has to meet several different constraints. It must offer a $50\,\Omega$ impedance to the antenna filter, but simultaneously affects significantly gain and noise performance of the whole amplifier.

Figure 5.1 shows the three most used configurations in open-literature examples. The topology in Figure 5.1(a) uses the emitter of a common-base stage as input termination: the input impedance is $1/g_m$ and the bias current can be set to meet the $50\,\Omega$ requirement. A simplified analysis of this topology [37] shows that the minimum achievable noise figure for bipolar transistors is about $2\,\mathrm{dB}$ and in the $2-3\,\mathrm{dB}$ range for modern CMOS processes. These values are well above the minimum noise figure NF_{min} achievable with common emitter configurations in the available BiCMOS technolo-

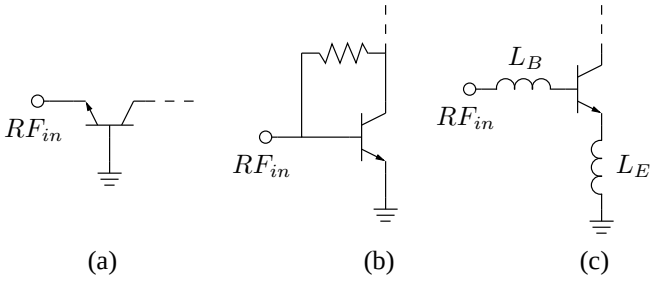


Figure 5.1: *Schematics of the LNA input matching topologies: (a) $1/g_m$ termination, (b) shunt-shunt feedback, (c) inductive degeneration. Inductive degeneration is the prevalent method used for integrated amplifiers.*

gies (§3). Moreover the topology does not allow the use of techniques for simultaneous noise and power matching: when a good $50\,\Omega$ matching is necessary, the noise figure would suffer further degradation.
Figure 5.1(b) shows another topology, which uses a resistive feedback to realize a broadband input matching. This type of matching is intrinsically broadband and highly linear, but it has the drawback of requiring a high power consumption to achieve gain in the range of $10-15\,\mathrm{dB}$, as specified in §4 for WLAN applications. The few open-literature examples [38–40] of this kind of amplifiers exhibit power consumptions 10 to 50 times larger than those presented in §5.5. This is mostly due to the fact that this topology is not suited for LC-tuning techniques, which can reduce the power consumption in narrow bands.
The third alternative, which is the one chosen in all the designs presented in this chapter, is shown in Figure 5.1(c) and employs an inductive emitter degeneration to introduce a real term in the input impedance. In order to suppress the remaining reactive term, tuning becomes necessary, making this topology narrow-band. This is not a severe limitation for the target WLAN applications.

The common-emitter amplifier with emitter degeneration is the most used topology for integrated LNAs, since it offers the best noise performance among the presented topologies. This is possible as the amplifier can be simultaneously noise and power matched, by properly choosing the two

inductors, transistor size and bias. As it will be shown in §5.4.1 the same topology can be easily modified for the use in dual-band applications.

5.1.1 Inductive Emitter Degeneration for Simultaneous Input Noise and Power Matching

For any given transistor, it exists an impedance $Z_{opt}=1/Y_{opt}$, such that the amplifier noise figure can be expressed as

$$NF=NF_{min}+\frac{R_N}{G_S}|Y_S-Y_{opt}|^2, \tag{5.1}$$

where

Y_S	signal-source admittance presented to the amplifier,
Y_{opt}	optimum noise admittance that results in minimum noise figure,
NF_{min}	minimum noise figure of transistor,
R_N	equivalent noise resistance of transistor,
G_S	real part of signal-source admittance

are all parameters dependent on the available technology [41]. An amplifier is noise matched if its signal-source impedance is Z_{opt}. The aim of this paragraph is to show that, with the topology shown in Figure 5.1(c), it is possible to make $Z_{opt}\simeq Z_0=50\,\Omega$, thus achieving simultaneous noise and power matching on an impedance suitable to terminate commercial antenna filters [42].
As shown in [43], the minimum noise figure and the optimum noise current density are practically independent of emitter length. Figure 5.2 shows the simulation of the minimum noise figure of a dual-base-contact HBT in IBM BiCMOS 6HP technology, as function of collector current I_{cc} and emitter length. For emitter lengths above $20\,\mu\mathrm{m}$ it is apparent that the minimum noise figure is very little affected by the chosen values of both collector current and emitter length. This allows to set independently power consumption and emitter size to meet other requirements.

The emitter degenerated input stage benefits from an important property: as shown in Figure 5.3 the degenerating inductance affects the maximum

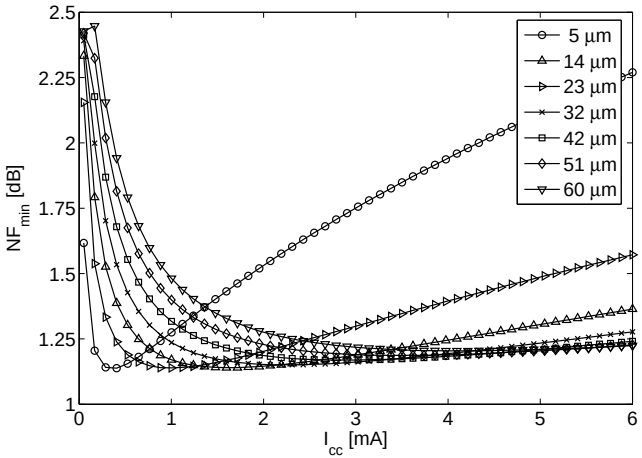


Figure 5.2: *Simulation at* $5.5\,\mathrm{GHz}$ *of the minimum noise figure of a dual-base-contact HBT in a* $0.25\,\mu\mathrm{m}$ *BiCMOS technology, as function of collector current* I_{cc} *and emitter length.*

available gain, but the real part of Z_{opt} and the minimum noise figure are nearly independent of the chosen value of L_E. This gives a useful degree of freedom in the design, since it allows to match R_{opt} by setting the transistor size only. Figure 5.4 shows the dependence of Z_{opt} and the complex conjugate of the input impedance on the emitter size: the HBT size can be chosen to set $R_{opt} = 50\,\Omega$.
According to [43], for both bipolar and field effect transistors it should always be

$$X_{opt} = X_{in}^{*}; \tag{5.2}$$

as shown again in Figure 5.4 this does not hold exactly true for the HBT transistors in the available technologies. However, the two values are reasonably close, and this property can still be exploited.
After setting the emitter size to match R_{opt}, the analysis of the circuit in Figure 5.1(c) with a simplified model allows to express the input impedance

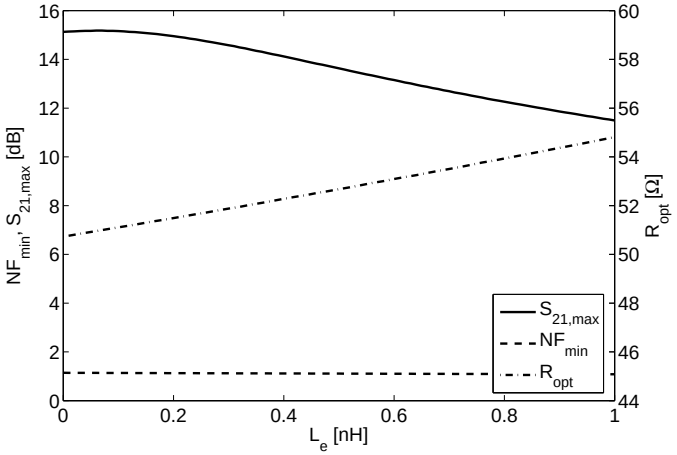


Figure 5.3: *Simulation at* $5.5\,\mathrm{GHz}$ *of the real part of* Z_{opt}*, the maximum stable gain and the minimum noise figure as function of the degenerating inductance* L_E*.*

seen at the base of the degenerated HBT as

$$Z_{in} = \frac{g_m}{C_\pi} L_E + j\omega L_E - j\frac{1}{\omega C_\pi}. \tag{5.3}$$

It is apparent that a proper choice of L_E can match the real part to $Z_0 = 50\,\Omega$, while the reactive component will be compensated with the series L_B inductance. Choosing

$$L_E = \frac{C_\pi}{g_m} Z_0 = \frac{Z_0}{\omega_t} \tag{5.4}$$

$$L_B = \frac{1}{\omega^2 C_\pi} - L_E \tag{5.5}$$

ensures power matching and, due to the approximated equation (5.2), simultaneous noise matching to the $Z_0 = 50\,\Omega$ source. Those choices do not affect the value of R_{opt}.
Figure 5.5 shows Z_{in} and Z_{opt} as function of possible values of L_E: apparent are the negligible dependence of R_{opt} on this parameter, the possibility

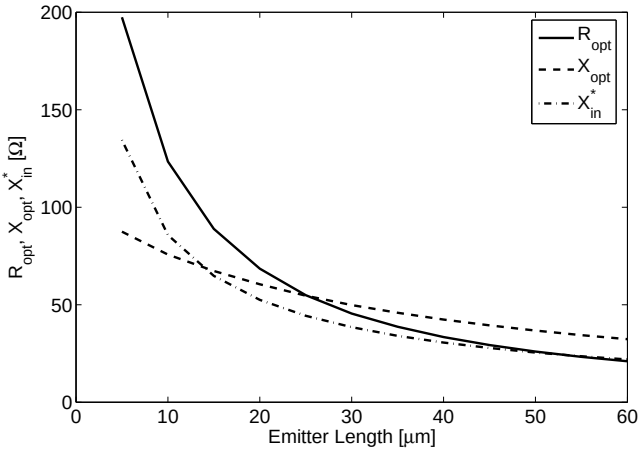


Figure 5.4: *Simulation at $5.5\,\mathrm{GHz}$ of real and imaginary part of Z_{opt}, and conjugate of input reactance of a dual-base-contact HBT in $0.25\mu m$ Bi-CMOS technology, as function of the emitter length. X_{opt} and X_{in}^* are not identical, as stated in [43], but values are close enough to exploit this feature.*

of matching R_{in} to $50\,\Omega$, the corresponding close values of X_{opt} and X_{in}^*. With the design approach depicted above, all the parameters of the emitter degenerated input stage are determined. The simulated result of those choices is shown in Figure 5.6: the ideal power matching is centered at $5.5\,\mathrm{GHz}$ and, at the same time, the noise figure reaches its minimum.
Summarizing, the parameters of the emitter-degenerated input stage in Figure 5.1(c) can be determined as follows:

- set emitter length to match R_{opt} to $50\,\Omega$, see Figure 5.4
- set L_E, i.e. the inductive emitter degeneration, to match R_{in} to $50\,\Omega$, see Figure 5.5 and equation (5.3)
- set series inductor L_B to match simultaneously X_{in} and X_{opt}^*, see Figure 5.4 and equation (5.5)

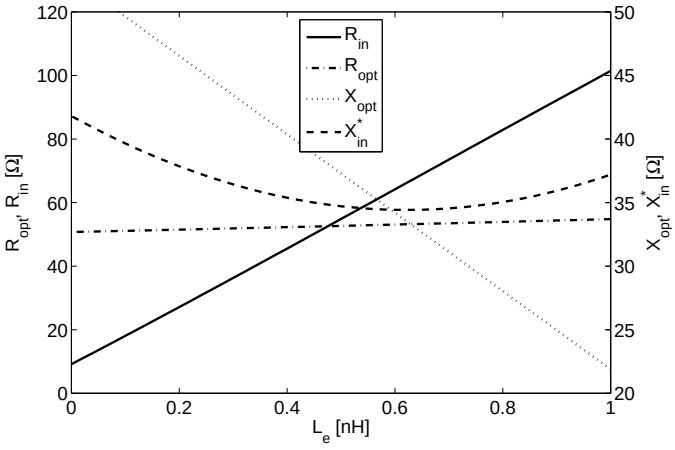


Figure 5.5: *Simulation of Z_{in} and Z_{opt} at $5.5\,\mathrm{GHz}$ as function of the emitter inductor L_E. Transistor dimension is already set to meet $R_{opt}=50\,\Omega$.*

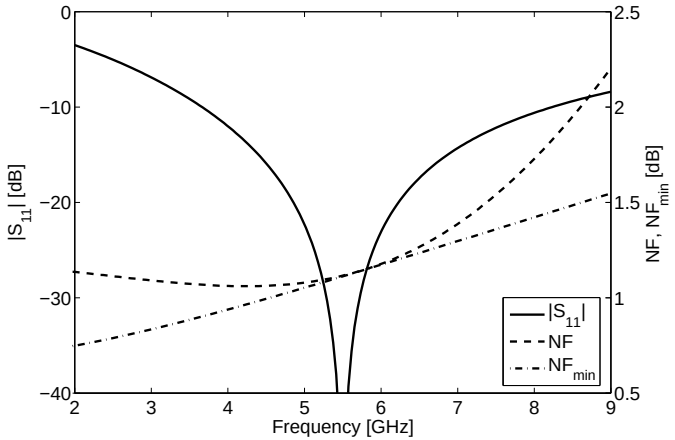


Figure 5.6: *Simulation of $|S_{11}|$, NF and NF_{min} of the inductive degenerated input stage designed as depicted in §5.1.1. Power and noise matching are achieved at the same frequency.*

5.2 Amplifier Gain Cell: Common Emitter and Cascode

The common-emitter amplifier shown in Figure 5.1(c) can be directly matched to the load using one of the techniques described in §5.3. This choice typically leads to practical issues in designing the input matching as described in §5.1.1. In fact, due to the very poor collector-to-base isolation of typical HBTs, the input and output matching networks cannot be designed independently and influence each other in a non-negligible way. If the available circuit simulator (CAD) is powerful enough to allow this approach, then the output of the amplifier can be loaded with its own complex conjugate impedance, i.e. the input design can be completed *assuming* the output already ideally matched [42]. Alternatively, the design can be completed by successive iterations of input and output redesigns or re-tuning: practical experience shows that the solution converges to acceptable values in few iterations.

Gain and bandwidth of the resulting amplifier depend significantly on the real part of the output impedance of the transistor, because of the effect described in §5.3. The bipolar cascode amplifier has an output impedance β times larger than a common emitter with the same current consumption [44], thus allows to achieve higher gains in narrower bands. Moreover it offers a better output-to-input isolation, thus simplifying the design of the matching networks and improving the LO-to-RF leakage of the receiver front-end. If needed, the large output impedance of cascode amplifiers can be reduced by means of a shunt resistor, in order to set gain and bandwidth to the values specified.

A further possibility would have been the use of cascaded common-emitter stages. This solution has been discarded, because the second stage would have required inductive or resistive emitter degeneration in order to meet the linearity specification, leading to larger circuit footprint or power consumption respectively.

5.3 Output Design

The output matching network is the part of the circuit responsible of feeding the amplified signal into the following stage. Although this part of the

amplifier does not affect significantly its noise performance, it determines gain, bandwidth and output impedance which, in turn, restricts the set of loads that can be properly driven.

5.3.1 Power Matching versus Voltage Matching

Power matching a load to a signal source means maximizing the power transfer from the source to the load. Extending this idea, voltage matching can be intended as maximization of voltage-signal amplitude from source to load.
In microwave design, being of paramount importance the use of transmission lines between different blocks of a system, most of the circuits must match in power the low resistive loads achievable with transmission lines, with $50\,\Omega$ being a standard.
In RFIC design, however, on-chip dimensions are so small that, even at frequencies in the low-GHz range, building blocks of a system might not need to be connected by transmission lines: a careful layout often allows the use of interconnects of lengths that are not a significant fraction of the wavelength. In those cases, the signal can be handled, ideally, as voltage- or current-only. Typical analog-electronic practice, mostly due to intrinsic features of common transistors, has favored voltage-mode circuits. For similar reasons, i.e. the features of active RF mixers (§6) and polyphase filters (§7), voltage matching is an alternative to power matching in some of the systems presented in §8.

5.3.2 Power Matching Alternatives

When designing the output power-matching network, both amplifier topologies that have been considered can be modelled as a transconductance, in parallel with a resistor and a capacitor. This is always an acceptable approximation in a relatively narrow band and for small input signals. Figure 5.7 shows the simple network that will be used to describe the matching networks considered and their properties. The values reported refer to a cascode amplifier in IBM BiCMOS 7HP technology, input noise and power matched by means of ideal components.

Figure 5.8 shows four topologies that can be used to match the amplifier modelled in Figure 5.7 to an impedance Z_0. Figure 5.9 and Table 5.1 show the simulation of power gain and output matching achievable with the four topologies, using ideal components and aiming at underling the main features of each choice.

The plain LC matching in Figure 5.8(a) can match capacitive-output amplifiers to real impedances, but might suffer of some limitations if cascode gain cells are used. In fact, those always have a large real part of the output impedance, which sets the quality factor of the resonator to relatively high values. This has the desirable effect of allowing higher gain with respect to single stage common-emitter versions, but at the same time tightens the relative bandwidth. Another drawback of the LC matching is that it requires high shunt inductances with respect to other alternatives.

The topology in Figure 5.8(b) is a possible solution for matching cascode amplifiers over a larger bandwidth. A shunt resistor R_q has been added, in order to lower the resonator quality factor. This simultaneously lowers the gain and broaden the bandwidth. Due to the same effect, the lower output impedance of common emitter amplifiers typically results in lower gain and larger bandwidth, when compared with cascode amplifiers biased with the same collector current and having the same transconductance. From a design point of view, the interesting property of this topology is that the value of the shunt resistance can be chosen in order to meet the bandwidth specification. A positive side effect is the reduction of shunt inductance needed for the matching; this results in a smaller spiral inductor and circuit footprint.

Another way to reduce the large shunt inductance needed with the LC matching is shown in Figure 5.8(c): a shunt capacitor is added in parallel to the inductor, and values are determined to provide the same reactance at center frequency. This approach allows to preserve the peak gain, but the drawback is the increase of quality factor and corresponding reduction of bandwidth. Values reported in Table 5.1 shows an emphasized example of the frequency response changes introduced by the shunt capacitor, but are unrealistic due to the absence of losses in all the reactive components and the very high quality factor of the resulting resonator. In practical cases, the inductance reduction will be possible, but the bandwidth will be larger.

An example of this is given by the matching topology shown in Figure 5.8(d), where a shunt resistor is added to lower the quality factor and results in a wider bandwidth.

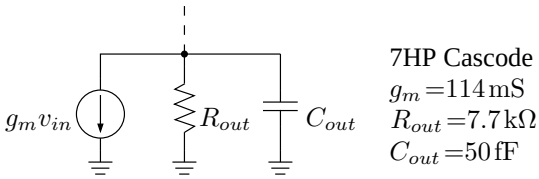


Figure 5.7: *The simplest model of the output of a common-emitter or cascode amplifier. Values reported in figure are those used in the following examples, corresponding to a noise and power matched cascode in BiCMOS7HP technology.*

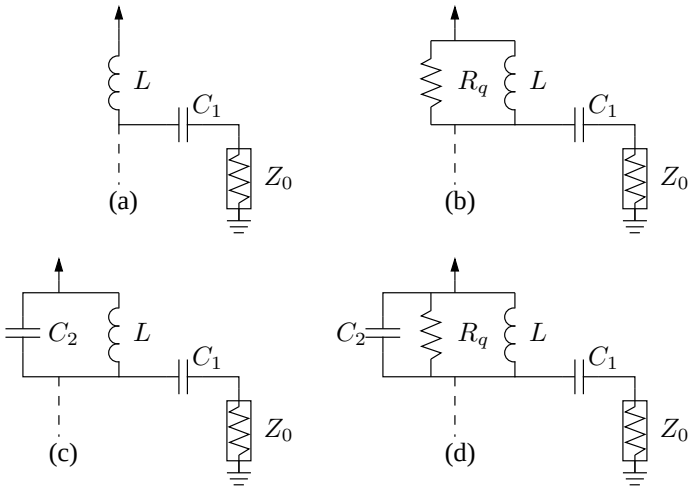


Figure 5.8: *Topologies for output power matching of low-noise amplifiers.*

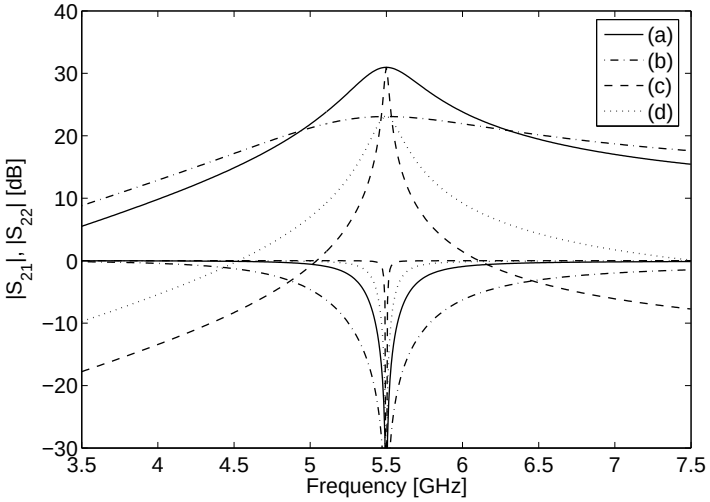


Figure 5.9: *Power gain $|S_{21}|$ and output return loss $|S_{22}|$ of the four matching topologies in Figure 5.8, when used to match the simplified output model in Figure 5.7. Design values are compared in Table 5.1.*

Table 5.1: *Design values and simulated band widths for the four output matching network in Figure 5.8.*

	L	C_1	C_2	R_q	S_{21} band	S_{22} band
(a)	8.8 nH	—	50 fF	—	432 MHz	324 MHz
(b)	5.17 nH	—	50 fF	1.5 kΩ	1.67 GHz	530 MHz
(c)	600 pH	1.3 pF	50 fF	—	30 MHz	14 MHz
(d)	600 pH	1.3 pF	50 fF	1.5 kΩ	180 MHz	70 MHz

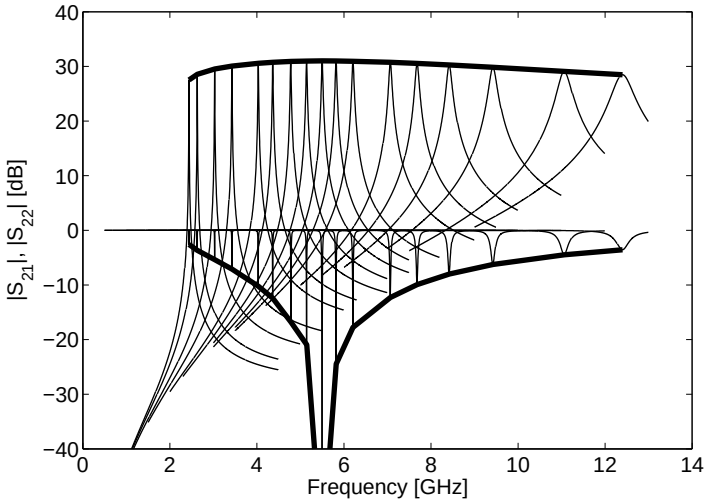


Figure 5.10: *Effect of the output matching tuning on $|S_{21}|$ and $|S_{22}|$. The shunt capacity sweeps from $150\,\mathrm{fF}$ to $7\,\mathrm{pF}$.*

Frequency tuning

The matching topologies in Figure 5.8(c)-(d) are attractive because of the lower inductance required, but cannot be easily used: the center frequency has a strong dependance on the shunt capacitor value. Typical process tolerances of $\pm 25\%$ on MIM capacitors can significantly shift the gain of the amplifier. This feature can be exploited replacing capacitor C_2 with a varactor, and offering the possibility of tuning the amplifier center frequency. Figure 5.10 shows the effect of the capacity variation in the simplified case in exam: the capacity of C_2 varies from $150\,\mathrm{fF}$ to $7\,\mathrm{pF}$ and the corresponding peaks of S_{21} and S_{22} sweep from $2\,\mathrm{GHz}$ to $12\,\mathrm{GHz}$, covering a very broad band. This output matching technique is particularly suited for applications with broad allocated bands, but narrow single-user bands, such as the $20\,\mathrm{MHz}$ channel of the WLAN standards at $5-6\,\mathrm{GHz}$.

5.3.3 Voltage Matching Alternatives

The idea behind voltage matching is that it is not necessary to optimize power transfer from the LNA to the following mixers, but in most of the cases it is sufficient to handle the signal as voltage and maximize the signal voltage amplitude at the mixer RF port. This is particularly true with nFET active mixers, presented in §6.2. In that case, the input impedance can be modelled as the shunt of a large resistor and a capacitor without excessive approximation: typical values are, e.g., in the $\mathrm{k}\Omega$ and tenths-of-pF ranges for IBM BiCMOS 6HP technology. The load of the amplifier can be a simple shunt inductor, which resonates with the mixer input capacity at center frequency: the voltage transfer function will depend only on the real part of the interface impedances.
Modifications to this main topology are possible, in quite similar ways as depicted in Figure 5.8: a shunt resistor lowers the quality factor and the peak gain, while broadening the bandwidth; an extra shunt capacitor allows the use of smaller inductors, but tightens the bandwidth; tuning of the center frequency is possible by adding a shunt varactor.

5.4 Dual-Band Matching

Some of the ideas presented in §5.1 and §5.3 can be extended for multi-band operation. This section presents the topologies and design techniques exploited for dual-band LNAs and receivers presented in §5.5.4 and §8.2.1. As in previous sections, the cascode amplifier is assumed to be the basic gain cell: input and output can be designed independently.
Section §5.4.1 presents two alternatives for the input matching, and section §5.4.2 two for output matching.

5.4.1 Input

Depending on system-level specifications, it can be convenient for a dual-band receiver to have a single input port or two, one for each band. It is apparent that this choice affects directly the design of the input stage of the LNA, as first stage of the receiver.
Having one input port per band allows the use of independent antenna filters:

the unwanted band can be filtered quite easily, but the number of external components increases.
Multi-band antenna filters are commercially available, and can be used to reduce the system complexity: in this case it is necessary to use one single input port for both the input bands, and the suppression of the unwanted band must be handled on-chip, leading unavoidably to worse rejection ratios.
This section presents two topologies suitable for the two cases and employed for receivers in §8.

Switched input

The schematic in Figure 5.11 shows a modification of the emitter-degenerated input matching, presented in §5.1.1, which allows to receive multiple-inputs and feed them to a single output port, through a shared common-base stage. The example in Figure 5.11 has two independent inputs for a dual-band receiver.
The emitter current of T_3 flows completely in T_1 or T_2, according to the selection of a control voltage, which sets the position of the bias switch. When active, both the inputs are power and noise matched to a $50\,\Omega$ source. The two parts do not influence each other up to frequencies dependant on the technology in use: the off branch introduces only parasitic capacities at the collector of the active input transistor, and those must be negligible with respect to the emitter impedance of T_3 at the highest frequency of interest.
This input matching topology has been used for the receiver presented in §8.2.1.

Dual-band input matching

The minimum noise figure NF_{min} of HBTs increases monotonically with frequency [43]. In a dual-band amplifier, a small noise mismatch can be tolerated for the lower band, since the NF does not have to be minimum in order to be sufficient for the system requirements. Exploiting this, it is possible to merge two single-band emitter-degenerated input stages into one, by replacing the series base inductors with the impedance shown as Z_b in Figure 5.12.
With this topology, the transistor size and emitter degeneration are determined to achieve noise matching in the highest band; then the two series

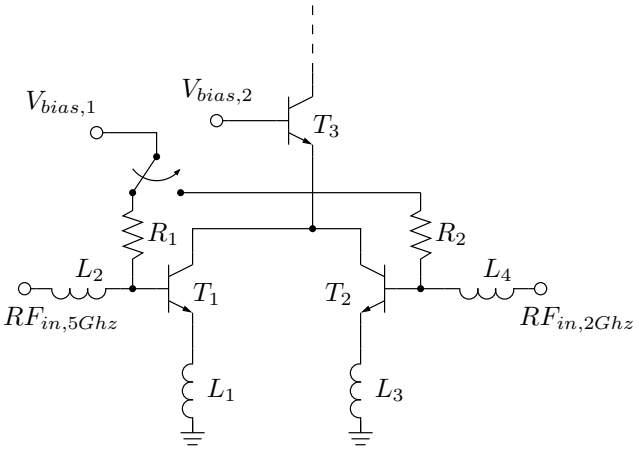


Figure 5.11: *Schematic of the switched dual-band LNA input.*

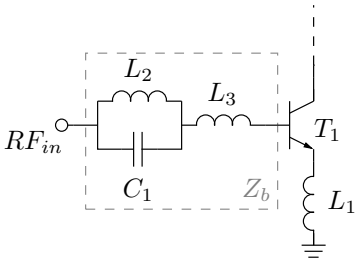


Figure 5.12: *A topology suitable for dual band power matching, which allows noise matching in one of the two bands and sub-optimal performance in the second.*

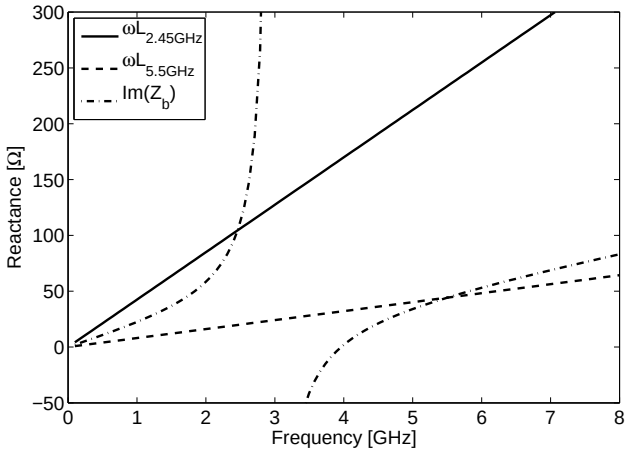


Figure 5.13: *Simulation of the reactance of the* dual-band *base inductance Z_b, compared with the reactance of inductors that would be required for single-band matching.*

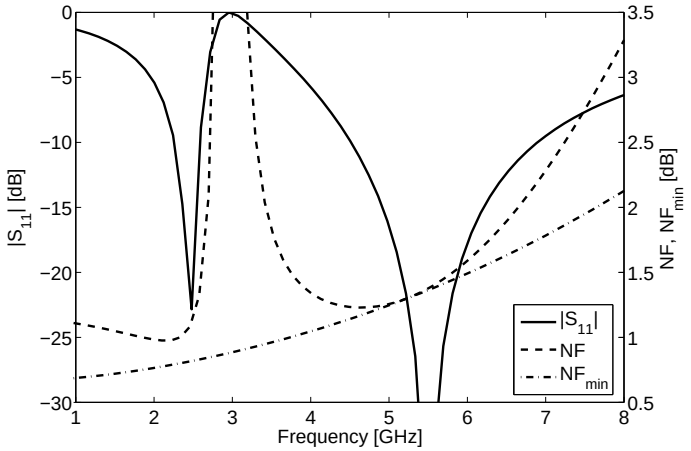


Figure 5.14: *Simulation of $|S_{11}|$, NF and NF_{nim} of the inductive degenerated dual-band input stage.*

inductors necessary for power matching can be determined, achieving noise matching only in the highest band. The two inductors are different, and can be replaced with Z_b: Figure 5.13 shows the simulation of the reactance of Z_b compared with those corresponding to the simple series inductances needed for single band matching. It is apparent that Z_b can replace different inductors in two narrow bands: in this example the bands are centered at $2.45\,\mathrm{GHz}$ and $5.5\,\mathrm{GHz}$. Figure 5.14 shows the dual-band matching: power matching is achieved in both the bands, while the noise figure is optimal in the upper band only. The values in the lower band remain acceptable, due to the better noise behavior of the transistor at lower frequencies. This input topology has been used for the amplifier presented in §5.5.4.

5.4.2 Output

As described in §4.4.1 and §4.4.2, the broadband frequency response of the downconversion mixers (§6) makes possible sharing the downconversion stage of a receiver for two or more bands. With this architecture, it is necessary to employ dual-band LNAs having one single output port, in order to avoid the use of series switches in the RF-signal path.
This section presents the solutions chosen for single-port voltage and power matching.

Dual-band load resonator

The topology shown in Figure 5.15 is suitable for dual-band voltage matching, because it can resonate with the shunt capacity at the input of the RF port of mixers. Figure 5.16 shows a simulation of the magnitude of the series impedance of the load Z_{load}, which is proportional to the voltage gain for a cascode or a common-emitter amplifier. In this example, the values of components are chosen to provide gain in the $2.45\,\mathrm{GHz}$ and $5.5\,\mathrm{GHz}$ bands. The two resistors R_1 and R_2 can be used to set gain and bandwidth in the two bands: for simplicity the graph in Figure 5.16 was plotted for $R_1 = R_2 = R$, but the values of the two resistors have effects on each of the band independently.
This active load has been used for the LNA of the receiver presented in §8.2.1.

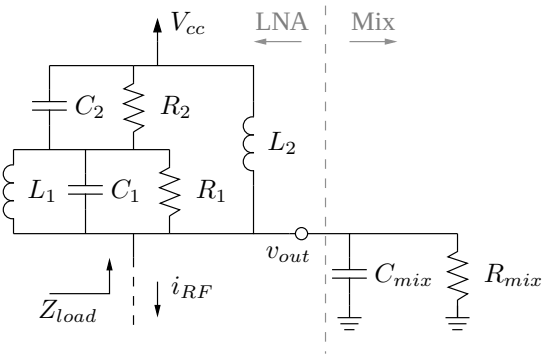


Figure 5.15: *Dual-band shunt resonator for voltage matching of the LNA. The shunt capacitor C_{mix} accounts for the mixers, and is part of the resonator.*

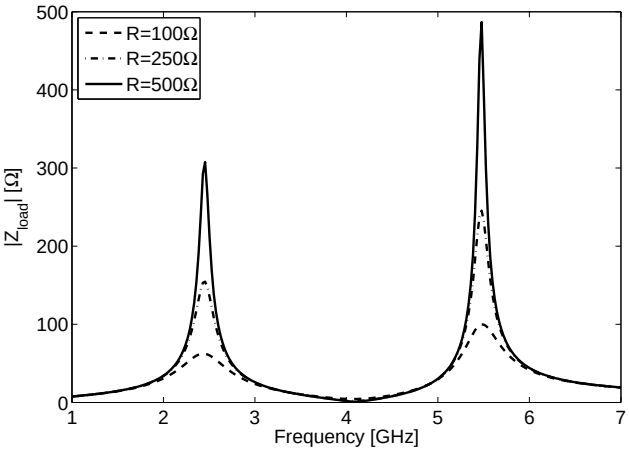


Figure 5.16: *Simulation of the frequency behavior of the dual-band load used for on-chip voltage matching.*

Switched power matching

The power matching equivalent of the load in Figure 5.15 could not be found. This is due to complexity of the problem. In fact, voltage matching imposes only one inequality on the magnitude of the output impedance, while power matching imposes two equalities on real and imaginary part of the output impedance.
If the receiver is designed for the downconversion of one band at a time, then the circuit in Figure 5.17 is a possible solution: two simple LC power-matching networks, one for each input band, are connected face-to-face, and only one branch is biased at a time. The unbiased branch has very little influence on the active part, so the two matching can be designed independently. Figure 5.18 shows the simulation of the achievable S_{21} and S_{22} for the two bands.
The off network loads the active side with a series LC resonator, which resonates at a frequency close to that of the power matching it is designed for. As a result the off network introduces a notch in the S_{21} transfer function of the wanted band. This behavior can be exploited to increase the rejection of the unwanted band, which would be amplified by the LNA in case a single input port is chosen for the receiver. In Figure 5.18 the rejection of the $2.45\,\mathrm{GHz}$ is about $30\,\mathrm{dB}$, and $10-15\,\mathrm{dB}$ for the $5.5\,\mathrm{GHz}$.
This matching network has been used for the dual-band LNA presented in §5.5.4.

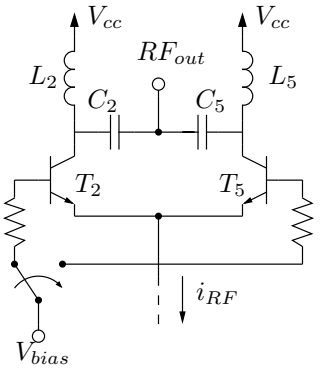


Figure 5.17: *The dual-band power-matching network. The switch drives the bias current to one branch at a time.*

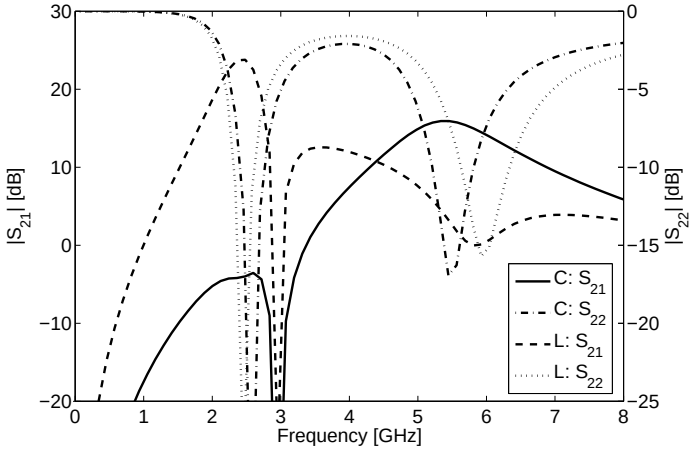


Figure 5.18: *Simulation of output return loss $|S_{22}|$ and power gain $|S_{21}|$ for the two operating mode of the power matching network.*

5.5 Experimental Results

This paragraph presents the design and characterization of the LNAs that have been fabricated as test structure for the validation of the ideas presented above, and the available device models.
Several other LNAs have been designed to be used in integrated receivers presented in §8, but their output matching networks do not allow direct $50\,\Omega$ characterization.

5.5.1 Single-Stage Common Emitter

The simplest topology that allows to employ the input matching network described in §5.1.1 is the single-stage common emitter amplifier, which matches the input stage directly to the output.
Figure 5.19 shows the simplified schematic of an amplifier of this kind, that was designed and fabricated in IBM BiCMOS 6HP technology. The emitter-degenerated input stage is directly power matched to a $50\,\Omega$ load by means of an LC transformer. Input and output matching network have been designed simultaneously, because of the poor input-to-output isolation of the common-emitter amplifier. As mentioned in §5.2, this can be done in few re-design iterations of each matching network, while the amplifier is loaded by an estimated input impedance of the following stage.
Table 5.2 resumes the design values referring to the schematic in Figure 5.19. All the components shown are integrated on chip: T_1 is a dual base-contact HBT; L_i are octagonal spiral inductors over deep trench grid ($L_{1,2}$) or polysilicon patterned shield (L_3); C_1 is a MIM capacitor over deep-trench grid.
Figure 5.20 shows a photograph of the common-emitter LNA. Total area shown measures $0.97\,\mathrm{mm}^2$, while active area is $0.38\,\mathrm{mm}^2$.

The circuit has been characterized on wafer. Figure 5.21 shows the measured and simulated input and output $50\,\Omega$ return losses $|S_{11}|$ and $|S_{22}|$ at a bias current of $2\,\mathrm{mA}$ from a power supply of $1\,\mathrm{V}$. Figure 5.22 shows power gain S_{21} and noise figure for the same operating point; $\mathrm{P}_{1\,\mathrm{dB}}$ and iIP_3 are $-8.7\,\mathrm{dBm}$ and $-1.5\,\mathrm{dBm}$ respectively. The measured performances are summarized in Table 5.3.
The measured results match the simulations in terms of frequency behavior. However power gain and noise figure suffer of some degradation. This is

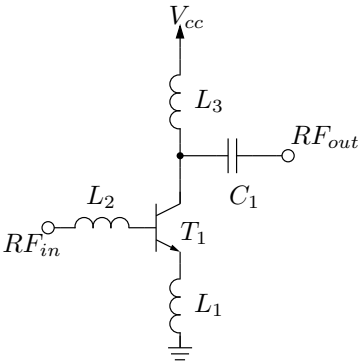


Figure 5.19: *Schematic of the common emitter LNA. Bias network is not shown; all components are integrated.*

Table 5.2: *Design values for the common-emitter LNA.*

T_1	$2 \times 27\,\mu\text{m} \times 320\,\text{nm}$
L_1	$0.8\,\text{nH}$
L_2	$0.9\,\text{nH}$
L_3	$2.2\,\text{nH}$
C_1	$530\,\text{fF}$
V_{cc}	$1\,\text{V}$
I_{cc}	$2\,\text{mA}$

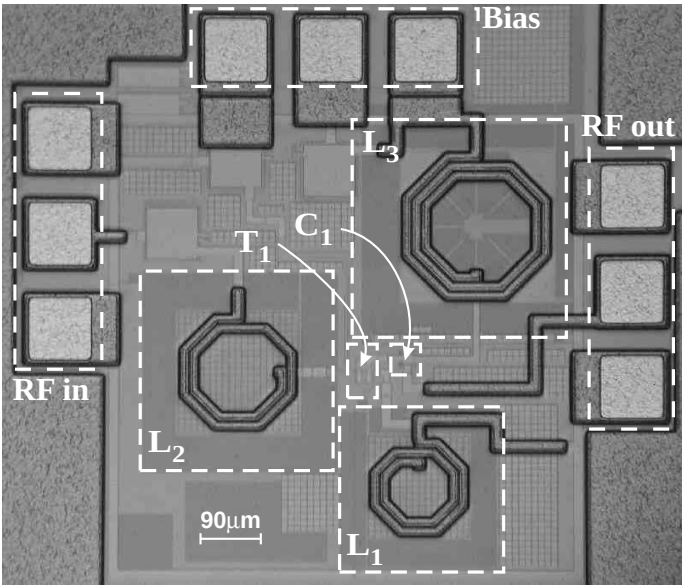


Figure 5.20: *Photograph of the common emitter LNA. Area shown measures* $1040\,\mu\mathrm{m}\times930\,\mu\mathrm{m}$*, total active area is* $0.38\,\mathrm{mm}^2$.

due to the losses in the metal connection among devices, which are not included in simulations, arising from the series resistance of the metal strips and the coupling of those to the substrate. The same parasitic lowers the quality factor of the input and output resonators, which results in slightly larger measured bandwidths.

This amplifier exhibits a noise figure sufficient for WLAN applications, and has a good gain-to-power-consumption ratio, which makes it attractive for low-power applications. However, the power gain is not sufficient for systems which make use of active downconversion mixers, because of the very high noise figure they typically exhibit. The low gain, as explained in §5.3.2, is mostly due to the low quality factor of the output resonator, set by the common-emitter output impedance. This is confirmed as well by the relatively large bandwidth of the output matching.

At a system level, a solution to the lack of gain of this kind of amplifier

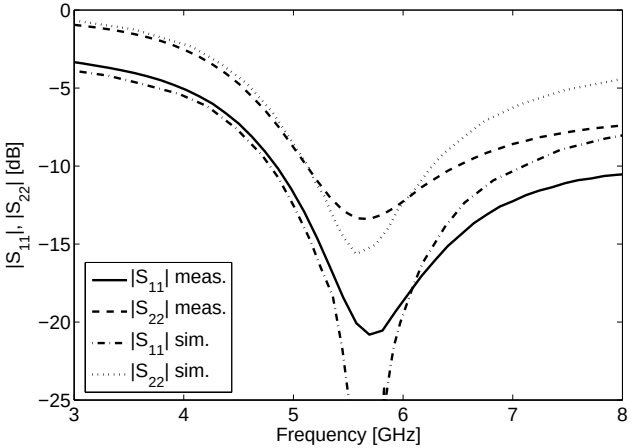


Figure 5.21: *Measurement and simulation of $|S_{11}|$ and $|S_{22}|$ for the common-emitter LNA.*

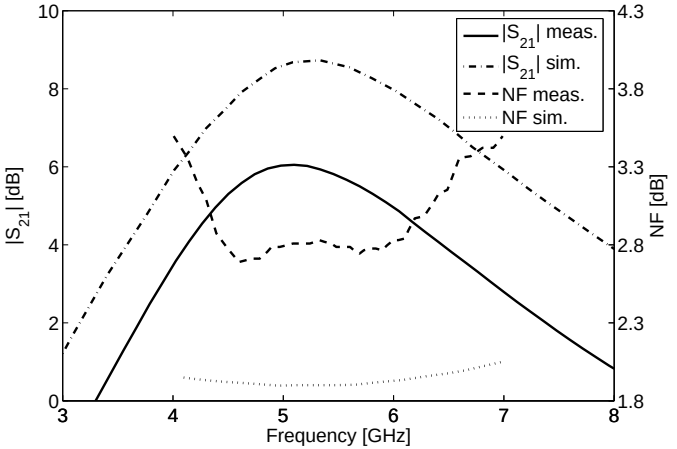


Figure 5.22: *Measurement and simulation of $|S_{21}|$ and NF for the common-emitter LNA.*

Table 5.3: *Measurement results for the common emitter amplifier.*

$S_{11} < -10\,\mathrm{dB}$	$4.9 - 8.9\,\mathrm{GHz}$
$S_{22} < -10\,\mathrm{dB}$	$5.1 - 6.5\,\mathrm{GHz}$
$S_{21,max}$	$6.1\,\mathrm{dB}$ @ $5.1\,\mathrm{GHz}$
S_{21} 3 dB-band	$3.9 - 6.9\,\mathrm{GHz}$
NF	$2.8\,\mathrm{dB}$
$\mathrm{P}_{1\,\mathrm{dB}}$	$-8.7\,\mathrm{dBm}$
iIP_3	$-1.5\,\mathrm{dBm}$
V_{cc}	$1\,\mathrm{V}$
I_{cc}	$2\,\mathrm{mA}$

could be the use of a second common-emitter stage. This choice implies the use of at least one more inductor and higher power consumption. A valid alternative is the use of a common-base amplifier for the second stage, i.e. a cascode amplifier.

5.5.2 Power Matched Cascode

The use of a cascode amplifier as gain cell of the LNA for integrated receivers is a quite common choice in the GHz bands [13–18, 23, 45–49]. This is apparent to such an extent that is rather difficult to find, in open literature, examples of different approaches [10, 50, 51]. This is mostly due to the possibility of achieving a higher gain for the same current consumption of a common emitter, because of the effect described in detail in §5.3.2. In fact, the output resistance of the cascode is β times larger than that of a common emitter biased with the same DC current. As a consequence, the gain peak is higher and its bandwidth narrower, but often sufficient for WLAN applications. If not, a shunt resistor can be added to the load.
Another positive feature of this gain cell is the higher output-to-input isolation, important to control the unwanted LO-to-RF leakage, which for direct

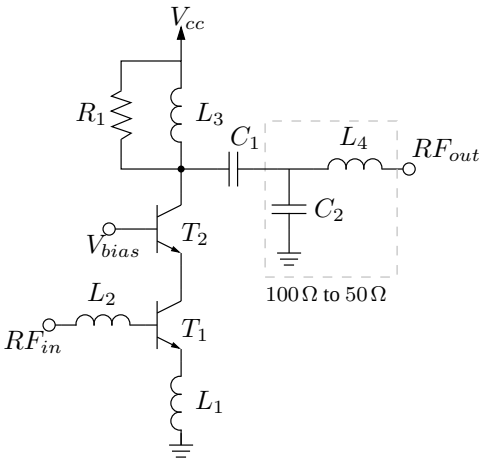


Figure 5.23: *Schematic of the cascode LNA. The bias network is not shown.*

Table 5.4: *Design values for the cascode LNA.*

T_1	$2 \times 29.3\,\mu\text{m} \times 320\,\text{nm}$
T_2	$2 \times 50\,\mu\text{m} \times 320\,\text{nm}$
L_1	422 pH
L_2	1.46 nH
L_3	2.77 nH
C_1	123.2 fF
L_4	2.44 nH
C_2	578.5 fF
V_{cc}	2 V
V_{bias}	1.6 V
I_{cc}	2 mA

conversion and low-IF receivers might fall in-band and cannot be suppressed by the antenna filter. However, experiments on silicon have shown that the isolation of a common emitter amplifier is close to that of a cascode, because in both cases the substrate coupling can be dominant over the device-to-device path. The circuit presented in this section, and the common emitter in §5.5.1 exhibit similar values of S_{12}.
Apart from the narrower bandwidth, the main drawback of using a cascode gain cell is the higher bias voltage needed for its operation: the current consumption is usually the same as a single-stage common emitter, but the voltage headroom needed for the common-base stage of a cascode is roughly the same as for a common emitter. Therefore, the total voltage needed for a cascode has to be increased according to the requirements of the input common-emitter stage, which depends on the technology. The very small voltage gain of the cascode first stage, however, allows to bias it at a minimum voltage, without sacrificing the amplifier overall linearity. Typically, amplifiers in IBM BiCMOS 6HP and IBM BiCMOS 7HP technologies require a $0.6-0.8\,\mathrm{V}$ increase of the voltage supply.

Figure 5.23 shows a simplified schematic of a cascode amplifier designed and fabricated in IBM BiCMOS 6HP technology. This circuit has been conceived as test structure for the receiver presented in §8.1.1 and [52]: due to the system requirements the amplifier has to drive a $100\,\Omega$ load, and an LC transformer to $50\,\Omega$ has been added for ease of characterization. Special attention has been paid in order to avoid the effects of this additional transformer on gain, linearity and bandwidth of the amplifier. Therefore, the results presented in this paragraph are direct measurements on a $50\,\Omega$ environment, but are expected to be very close to what would be measured at the inner $100\,\Omega$ node.
Table 5.4 resumes the design values referring to the schematic in Figure 5.23. All the components shown are integrated on chip: T_1 and T_2 are dual-base contact HBTs; L_i are octagonal spiral inductors over deep trench grid (L_1 and L_3) or polysilicon patterned shield (L_2 and L_4); C_1 and C_2 are MIM capacitors over deep-trench grid.
Figure 5.24 shows a photograph of the cascode amplifier: total area shown measures $1.22\,\mathrm{mm}^2$, while active area is $0.26\,\mathrm{mm}^2$ for the LNA output-matched to $100\,\Omega$, excluding the LC matching to $50\,\Omega$.

The circuit has been characterized on wafer, using $50\,\Omega$ RF wafer probes.

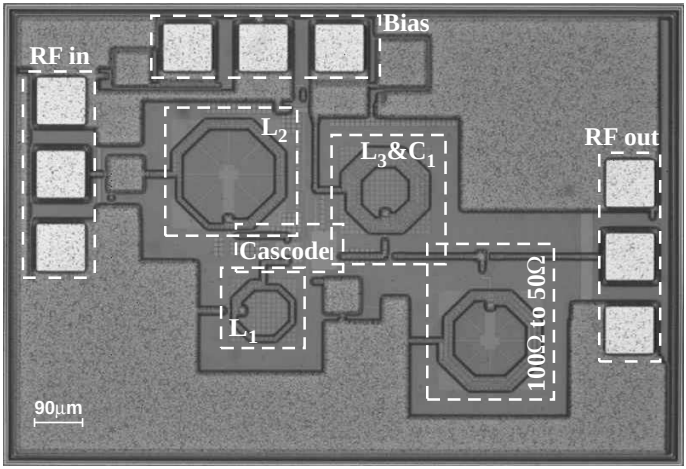


Figure 5.24: *Photograph of the cascode LNA. Area shown measures* $1323\,\mu\mathrm{m}\times923\,\mu\mathrm{m}$*, total active area for the amplifier output-matched to* $100\,\Omega$ *is* $0.26\,\mathrm{mm}^2$.

All the results shown are direct measurements of the amplifier, including the test LC matching from $100\,\Omega$ to $50\,\Omega$. For both small and large signal tests, simulations have shown that the additional matching network does not affect the performance of the amplifier on a $100\,\Omega$ load. The circuit have been biased with $2\,\mathrm{mA}$ from a $2\,\mathrm{V}$ power supply. Figure 5.25 shows input and output return loss. The simulation of $|S_{11}|$ and $|S_{22}|$ are included, in order to account of a slight mismatch with the input impedance measurements. Figure 5.26 shows power gain and noise figure. $\mathrm{P}_{1\,\mathrm{dB}}$ and iIP_3 are $-16.2\,\mathrm{dBm}$ and $-8.2\,\mathrm{dBm}$ respectively. The measured performances are summarized in Table 5.5.

As for the amplifier in §5.5.1, the performance of this LNA is affected by the losses of the metal connections among devices, which cannot be entirely taken into account in simulation. This results in lower power gain and noise figure higher than predicted in the design phase.
The input stage of this amplifier was designed according to the procedure described in §5.1.1. The effect of actual device parasitics shifts the optimal

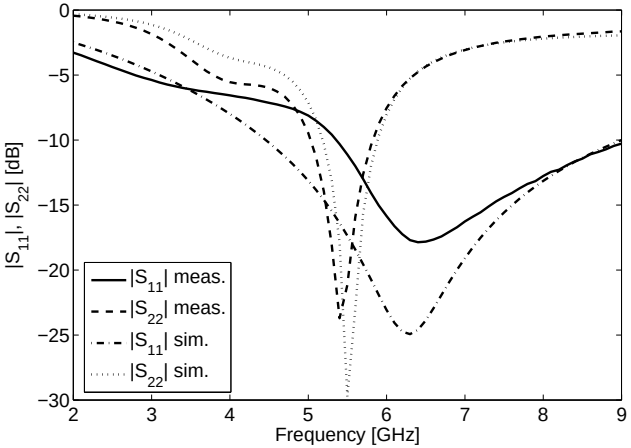


Figure 5.25: *Measurement and simulation of $|S_{11}|$ and $|S_{22}|$ for the cascode LNA.*

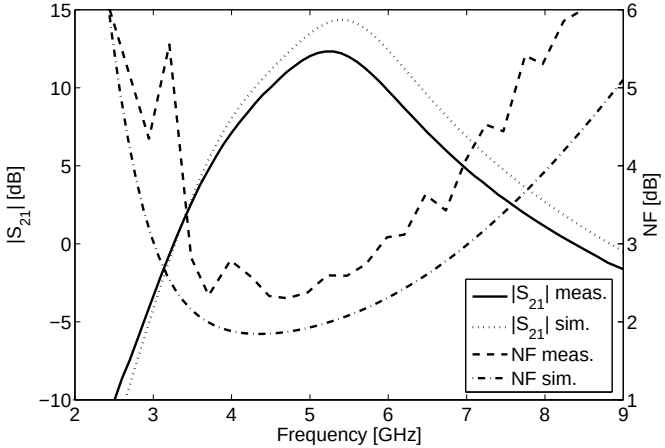


Figure 5.26: *Measurement and simulation of $|S_{21}|$ and NF for the cascode LNA.*

Table 5.5: *Measurement results for the cascode amplifier.*

$S_{11} < -10\,\mathrm{dB}$	$5.3 - 9.1\,\mathrm{GHz}$
$S_{22} < -10\,\mathrm{dB}$	$5.0 - 5.9\,\mathrm{GHz}$
$S_{21,max}$	$12.3\,\mathrm{dB}$ @ $5.3\,\mathrm{GHz}$
S_{21} 3dB-band	$4.3 - 6.1\,\mathrm{GHz}$
NF	$2.9\,\mathrm{dB}$ @ $5.9\,\mathrm{GHz}$
$\mathrm{P}_{1\,\mathrm{dB}}$	$-16.2\,\mathrm{dBm}$
iIP_3	$-8.2\,\mathrm{dBm}$
V_{cc}	$2\,\mathrm{V}$
I_{cc}	$2\,\mathrm{mA}$

band for both power and noise matching significantly. Some of those effects, as can be seen in Figure 5.25, could already be foreseen at a simulation stage, when the parasitics of the spiral inductors are included. The actual effect of parasitics and device-to-device coupling is larger that expected. In both the cases, the measured input return loss and noise figure are still sufficient for covering the three U-NII bands and provide pre-amplification in an integrated receiver. This has been demonstrated integrating this LNA in a low-IF receiver, as described in §8.1.1 and [52].

5.5.3 Tunable Cascode

In order to validate the tunable output matching described in §5.3.2, a power matched tunable cascode amplifier was designed and fabricated in IBM BiCMOS 7HP technology [1]. The advantages of using a cascode amplifier are reported and discussed in §5.5.2.
Although the tuning capabilities of this output matching network might allow very broadband tuning ranges, this would require the use of several varactor in parallel, possibly connected with switches. For example, in order to achieve an equivalent bandwidth as shown in Figure 5.10, the varactor would have to sweep from $150\,\mathrm{fF}$ to $7\,\mathrm{pF}$. In this particular case, in order to

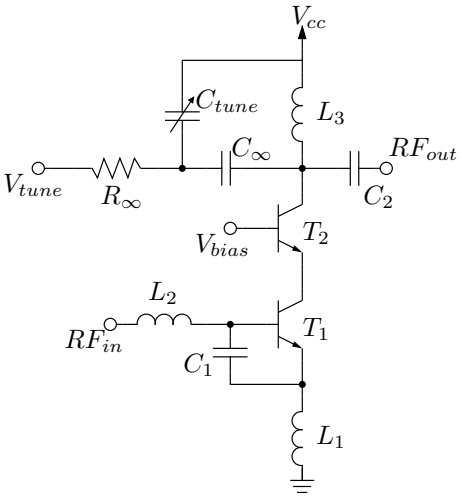


Figure 5.27: *Schematic of the fabricated tunable low-noise amplifier. Bias network is not shown.*

keep the circuit complexity to a minimum, the amplifier was designed targeting only the $5-6\,\mathrm{GHz}$ band, sufficient to cover all the three U-NII bands of the WLAN standards.

Figure 5.27 shows a simplified schematic of the fabricated circuit. The input matching network was designed as described in §5.1.1, but a capacitor C_1 is used to avoid resizing the transistor T_1: this allows to match the real part of the noise impedance, without increasing the emitter length and reducing the series base resistance. The output matching network was designed as in §5.3.2. The shunt capacitor is replaced with a varactor; the capacity-control network consist of a large resistor R_∞, a large capacitor C_∞ and a control voltage source V_{tune}. For ease of characterization, both input and output are power matched to $50\,\Omega$, but the same concept for the output matching can be easily adapted to the higher impedance levels typical of on-chip circuits.
Table 5.6 reports in detail the design values for the amplifier. All the components are integrated on the same chip: T_1 and T_2 are dual-base contact

Table 5.6: *Design values for the cascode tunable LNA in IBM BiCMOS 7HP technology.*

Tech.	IBM BiCMOS 7HP
T_1	$2 \times 6.08\,\mu\mathrm{m} \times 200\,\mathrm{nm}$
T_2	$2 \times 6.08\,\mu\mathrm{m} \times 200\,\mathrm{nm}$
L_1	$257\,\mathrm{pH}$
L_2	$2.41\,\mathrm{nH}$
L_3	$546\,\mathrm{pH}$
C_{tune}	$356\,\mathrm{fF} - 1.04\,\mathrm{pF}$
C_1	$193\,\mathrm{fF}$
C_2	$419\,\mathrm{fF}$
V_{cc}	$2\,\mathrm{V}$
V_{bias}	$1.6\,\mathrm{V}$
I_{cc}	$3\,\mathrm{mA}$

HBTs; C_1 and C_2 are MIM capacitors over deep-trench grid; C_{tune} is an nMOS varactor; L_i are octagonal spiral inductors over deep trench grid. Polysilicon shields have not been used for the integrated inductors, because models were not available for this technology at the time of fabrication. Figure 5.28 shows a photograph of the amplifier: total area shown measures $1.08\,\mathrm{mm}^2$, while active area is $0.3\,\mathrm{mm}^2$.

This circuit has been characterized on wafer, using $50\,\Omega$ probes. Biased with a collector current of $3\,\mathrm{mA}$, it showed similar performances for V_{cc} ranging from $1.5\,\mathrm{V}$ to $2.4\,\mathrm{V}$. Results presented here are those observed for V_{cc}=$2\,\mathrm{V}$. Figure 5.29 shows the effect of C_{tune} variations on gain and output matching. The capacity value is controlled by $V_{cc} - V_{tune}$, which sweeps from $-0.4\,\mathrm{V}$ to $0.3\,\mathrm{V}$. The tuning capability allows to extend the $-10\,\mathrm{dB}$ bandwidth of S_{22} from $700\,\mathrm{MHz}$ to $1.4\,\mathrm{GHz}$, and to sweep the peak gain of $13.2\,\mathrm{dB}$ over a $1.1\,\mathrm{GHz}$ band. Due to the good isolation of

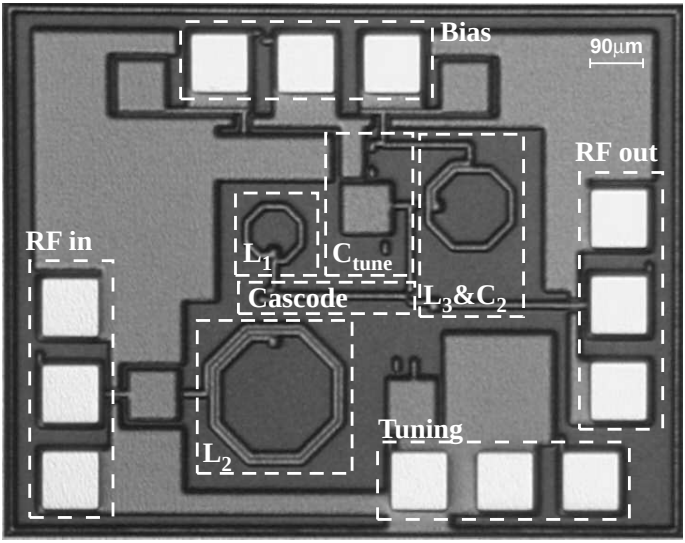


Figure 5.28: *Chip photograph of the tunable LNA. Area shown measures* $1.18\,\mathrm{mm}\times 0.92\,\mathrm{mm}$

the cascode gain cell, input matching and noise figure are not significantly affected by output matching variations. Figure 5.30 shows the measured S-parameters and NF, as function of frequency, at the V_{tune} corresponding to the best value of $|S_{22}|$. In the usable band, the NF is smaller than $2.3\,\mathrm{dB}$. Figure 5.31 presents an example of linearity tests performed on the LNA at $5.5\,\mathrm{GHz}$: in this case, $\mathrm{P}_{1\,\mathrm{dB}}$ is $-20.5\,\mathrm{dBm}$ and iIP_3 is $-9\,\mathrm{dBm}$ at the corresponding optimum V_{tune} value. Extrapolations of iIP_3 at other frequencies have confirmed that it is independent of C_{tune} variations, within measurement uncertainty.

The measurement results are summarized in Table 5.7. These performances are sufficient to meet the specifications for an RF front-end compliant with the main WLAN standard in the $5\,\mathrm{GHz}$ band (§2.1), [52]. In particular, the flat frequency response of the gain can significantly improve the noise performance of the whole receiver, or ease the use of noise-critical active mixers (§6).

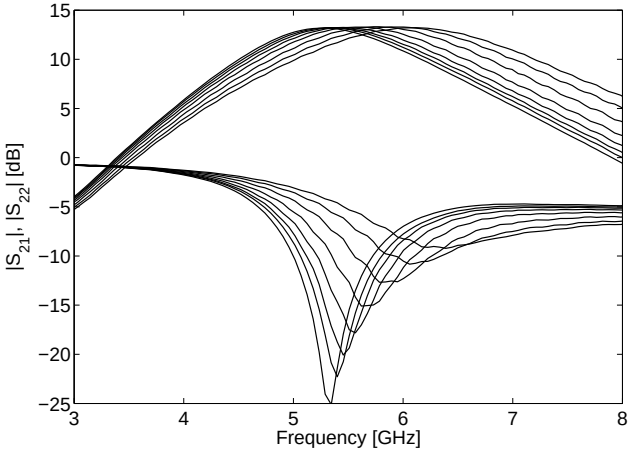


Figure 5.29: *Effects of the output-matching tuning on $|S_{21}|$ and $|S_{22}|$: $V_{cc} - V_{tune}$ sweeps from $-0.4\,\mathrm{V}$ to $0.3\,\mathrm{V}$*

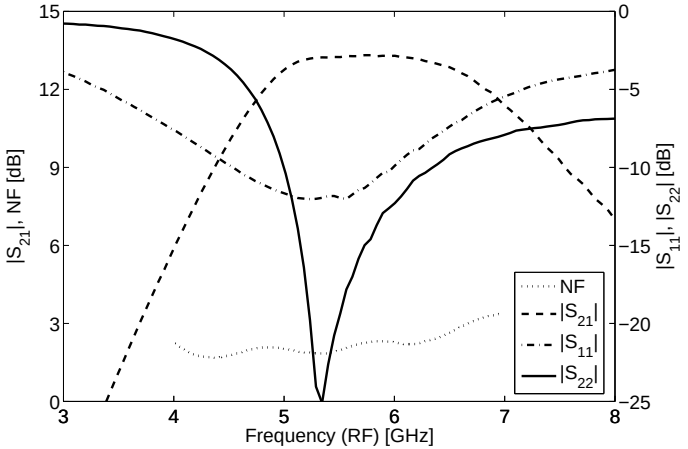


Figure 5.30: *Optimum S-parameters and noise figure of the tunable LNA: for each frequency V_{tune} is set for best $|S_{22}|$ value.*

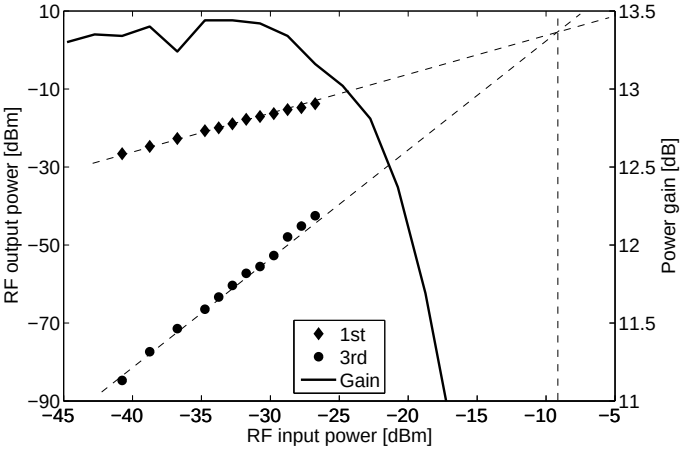


Figure 5.31: *Linearity tests preformed on the LNA at* $5.5\,\mathrm{GHz}$*.* V_{tune} *is set for best* $|S_{22}|$ *value.*

Table 5.7: *Summary of experimental results for the tunable LNA.*

Technology	$120\,\mathrm{GHz}$-f_t BiCMOS
$\lvert S_{21}\rvert_{max}$	$13.2\,\mathrm{dB}$
$\lvert S_{21}\rvert_{max} \pm 0.1\,\mathrm{dB}$	$5.1-6.2\,\mathrm{GHz}$
$\lvert S_{11}\rvert < -10\,\mathrm{dB}$	$4.6-6.0\,\mathrm{GHz}$
$\lvert S_{22}\rvert < -10\,\mathrm{dB}$	$5.0-6.4\,\mathrm{GHz}$
NF	$2.3\,\mathrm{dB}$
$\mathrm{P}_{1\,\mathrm{dB}}$	$-20.5\,\mathrm{dBm}$
iIP_3	$-9\,\mathrm{dBm}$
V_{cc}	$2\,\mathrm{V}$
I_{cc}	$3\,\mathrm{mA}$
$V_{cc}-V_{tune}$	$-0.4 \div 0.3\,\mathrm{V}$

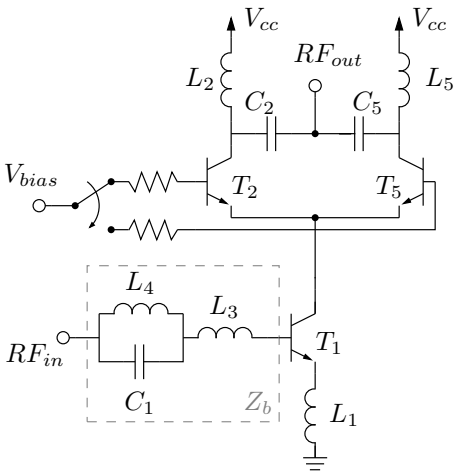


Figure 5.32: *Schematic of the power-matched dual-band cascode amplifier.*

5.5.4 Dual-Band LNA

The amplifier presented in this section is a dual-band LNA, designed using the input and output power-matching topologies presented in §5.4.
Figure 5.32 shows the schematic of the circuit. The input stage is dual-band power matched to a $50\,\Omega$ signal source, optimized for simultaneous noise matching in the upper band. On the output side, a switched power matching is used: assuming that the two bands are not received at the same time, the switch on the bias network directs the signal current to T_2 or T_5, each of which is matched to one of the input bands by means of a simple LC network. The design values of the schematic in Figure 5.32 are summarized in Table 5.8.

The circuit was fabricated in the IBM BiCMOS 6HP technology, on a $1323\,\mu\mathrm{m} \times 1185\,\mu\mathrm{m}$ chip, shown in Figure 5.33. Active area is $0.44\,\mathrm{mm}^2$. The chip includes an LC transformer, not shown in the schematic, to match the $50\,\Omega$ output impedance to $10\,\Omega$, since the amplifier was designed to drive a pair of low-input-impedance Micromixers (§6.3.2). The results shown here have been de-embedded from the effects of this adapter.

Table 5.8: *Design values for the dual-band cascode LNA in IBM BiCMOS 6HP technology.*

T_1	$2 \times 29.3\,\mu\text{m} \times 320\,\text{nm}$
L_1	$406\,\text{pH}$
L_3	$2.25\,\text{nH}$
L_4	$1.46\,\text{nH}$
C_1	$1.93\,\text{fF}$
T_2	$2 \times 29.3\,\mu\text{m} \times 320\,\text{nm}$
L_2	$5.31\,\text{nH}$
C_2	$605\,\text{fF}$
T_3	$2 \times 29.3\,\mu\text{m} \times 320\,\text{nm}$
L_3	$3.06\,\text{nH}$
C_3	$176\,\text{fF}$
V_{cc}	$2.4\,\text{V}$
V_{bias}	$1.8\,\text{V}$
I_{cc}	$2\,\text{mA}$

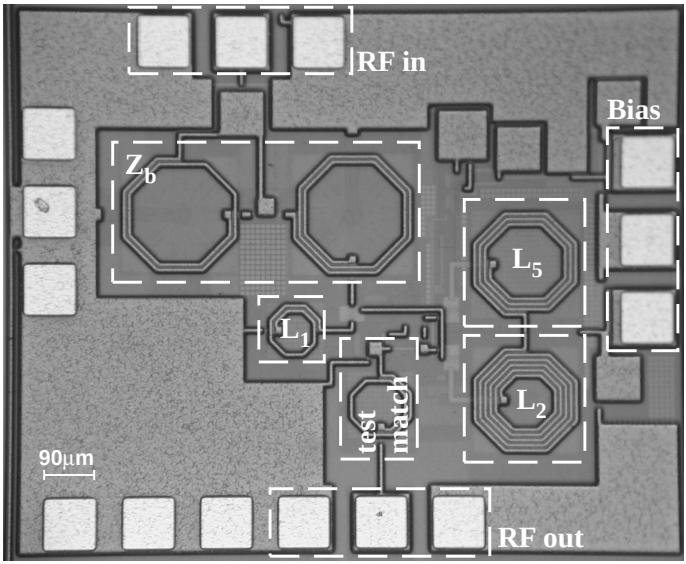


Figure 5.33: *Chip photograph of the dual-band LNA. Area shown measures* $1.323\,\mathrm{mm} \times 1.185\,\mathrm{mm}$

Figure 5.34 shows the measured input return loss $|S_{11}|$ and NF of the dual-band amplifier. Due to the good isolation of the cascode amplifier, the position of the bias switch, which selects the $2.45\,\mathrm{GHz}$ band (L) or the $5.5\,\mathrm{GHz}$ band (C), has little effect on the input matching. The noise figure is affected more, because of the change in power gain introduced by the change of bias. The input port offers a good matching to the source in the two bands of interest, confirming the validity of the matching topology presented in §5.4.1. Figure 5.35 shows the output matching and power gain. The effect of the bias switching is much larger, in particular on the power gain. The measured results for the output matching and power gain differ significantly from the simulations. This is probably due to inaccuracies in modeling the collector capacity of the transistor in the *off* branch, which loads the other significantly. Besides the poor performance, the gain reshaping is apparent in the comparison of the two operating modes.

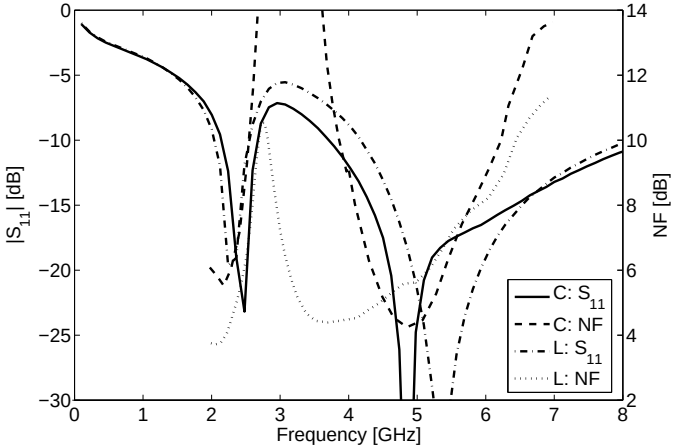


Figure 5.34: *Measured input return loss $|S_{11}|$ and NF for the two operating modes of the dual-band amplifier.*

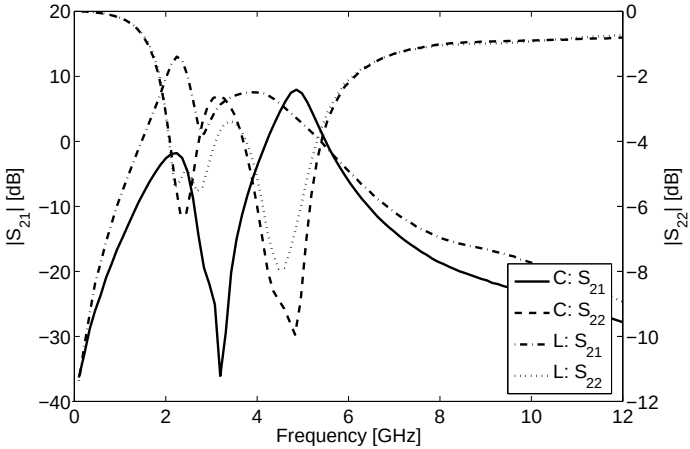


Figure 5.35: *Measured values of output return loss $|S_{22}|$ and power gain $|S_{21}|$ in the $5\,\mathrm{GHz}$ (C) and $2\,\mathrm{GHz}$ (L) mode.*

5.6 Summary

In this chapter, the design of low-noise amplifiers for wireless LAN applications has been studied. Several solutions are presented for receiver front-ends operating at $5-6\,\mathrm{GHz}$ and dual-band extensions, for operation also at $2.4\,\mathrm{GHz}$.

The design strategies adopted for input and output matching of single-stage common-emitter and cascode amplifier are described. The emitter degeneration is argued to be the most convenient input matching topology for the target application. The choice for the output matching depends on the system requirements: the design strategy presented allows both voltage and power matching to the following mixers. The prototypes presented in §5.5 are all power matched, since this enables the RF characterization. Examples of voltage matched LNAs are given in §8 as part of larger circuits.

In the design of the integrated front-end (§8), the cascode configuration has always been preferred over the common-emitter. This is motivated by the higher output impedance of the cascode, which for the same current consumption offers higher gain. The higher voltage required is compatible with the system requirements, as the active mixers would not be able to operate at the same lower voltage of common emitter amplifiers. Another advantage of cascode amplifiers is the higher input-to-output isolation. At a system level, for Si-based implementation, the increased isolation is nearly nullified by the substrate coupling. However, the isolation is still an advantage, since it reduces the interaction between the input- and output-matching networks, simplifying their design. This is experimentally shown in §5.5.3, where the changes in the output matching do not affect the input impedance.

The possibility of improving and extend the presented techniques are explored as well. A tunable output matching is presented and exploited to enlarge the usable bandwidth. Dual-band versions are proposed for input and output matching, covering several possible configuration of the receiver: single or multiple input port, voltage or power output matching.

Chapter 6

Downconversion Mixers

All the receiver architectures presented in §4 are variants of the superheterodyne receiver and use one or more mixers to perform the frequency translation of the input signals. Since a linear and time-invariant system cannot produce outputs with spectral components not present at the input, mixers must be either non-linear or time-varying elements in order to provide the necessary frequency translation.
Virtually any non-linear device or circuit can be used as mixer, but some non-linear circuits are better suited for the realization of mixers in monolithic and RF systems. The first paragraph of this chapter describes the principle exploited in a large majority of RF mixers, active and passive. The rest of the chapter presents the design and characterization of several mixers suitable for WLAN integrated receivers.

6.1 Principle of Operation

All the mixers presented in this chapter are based on the same principle of operation described in this paragraph and represented in the block diagram in Figure 6.1.
An input RF signal is amplified and fed into a switch, which connects it alternatively to an inverting and a non-inverting buffer. The switching is driven by the LO signal and the IF signal is the combination of the output of the two buffers. This operation is equivalent to multiplying the RF input

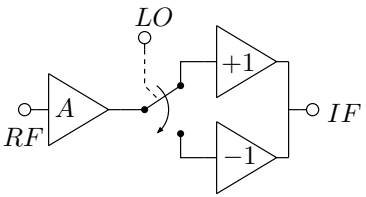


Figure 6.1: *Basic elements of an ideal switching mixer.*

signal for a zero-average square wave, having the same periodicity of the LO signal. The Fourier-series expansion of such a wave is

$$h(t) = \frac{4}{\pi} \sum_{i=0}^{+\infty} \frac{(-1)^n}{2n+1} \cdot \sin[(2n+1)\pi f_{LO} t] = \frac{2}{\pi} \cdot \sin(2\pi f_{LO} t) + \ldots, \quad (6.1)$$

which results in a conversion gain

$$G_c = \frac{2}{\pi} \cdot A \quad (6.2)$$

for the mixer in Figure 6.1. Therefore, even assuming that the switching is ideal, the maximum achievable conversion gain G_c is smaller than the RF gain A. As it will be shown in the rest of this chapter, the unideality of the switch will affect the conversion gain, specially when low LO powers are used, while the linearity will mostly depend on the implementation of the RF amplification.
In practical cases, the RF amplifier and the switch are not implemented separately. In particular, for active mixers, the amplifier is in cascode configuration, and the switch is implemented simply by replicating the common base stage and driving the amplified signal alternatively to one of two symmetric loads. On the other hand, for passive mixers, there is no RF gain stage and the switch is implemented by one or more *cold* FETs or diodes.

6.1.1 Cascode Amplifier and Active Mixers

Monolithic mixers are often based on the use of a current-mode *mixer core*, which is a differential pair voltage-driven by the LO signal. The RF input

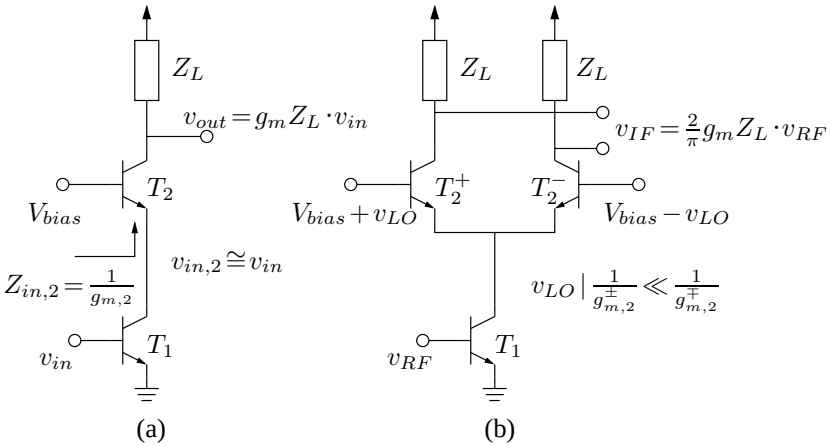


Figure 6.2: *Schematic and simplified analysis of a cascode amplifier (a) and a singly-balanced mixer (b). The singly-balanced mixer inherits gain and linearity from the corresponding cascode amplifier.*

section provides amplification; it operates in voltage-to-current (transconductance) mode and delivers the current signal to the core. The mixer core acts as part of the cascode for the RF input cell: for this reason, the design of the most common active mixers can be based on the design of the corresponding cascode amplifier, which shares with the mixer important features, such as gain and linearity.

Conversion gain

The schematic and simplified analysis of a cascode amplifier and the corresponding singly-balanced mixer are shown in Figure 6.2: a cascode amplifier operating at the RF frequency is transformed in a mixer by replicating its common base stage and passive load. The operating principle depicted in Figure 6.1 is implemented by superimposing a differential LO signal on the bias of the common-base transistors T_2^+ and T_2^-. As shown in Figure 6.2(a), the input impedance of the common-base transistor is approxi-

mately $Z_{in,2}=1/g_{m,2}$, and depends directly on the base bias voltage V_{bias}. In Figure 6.2(b), this bias is modified with the superimposition of the differential LO signal, which indirectly changes the base impedances of the two transistors $T_2^{\pm}$. If the LO signal is large enough to ensure that

$$\frac{1}{g_{m,2}^{\pm}} \ll \frac{1}{g_{m,2}^{\mp}}, \tag{6.3}$$

then the RF current-mode signal is alternatively redirected to one of the two symmetric loads.
With these considerations, together with the equations in Figure 6.2, the mixer conversion gain can be determined. Equation (6.3) gives a clear guideline in finding the minimum amplitude of the LO signal.

Linearity

Although the mixer-core switching is large-signal driven and intrinsically non-linear, the linearity of the mixer conversion gain is mostly dependant on effects similar to those limiting the linearity of a cascode amplifier, such as RF cell non-linearity and signal clipping in some part of the circuit. If the condition in equation (6.3) is satisfied with ideal commutation, the conversion gain defined in equation (6.2) is a linear function of the RF gain, and inherits its linearity features.
For this reason, in designing active mixers, it is useful to investigate the linearity of HBT cascode amplifiers and its variants, such as the inductively-degenerated cascode and the BiCMOS cascode, which replaces the common-emitter stage with a common-source FET amplifier. The study of the linearity behavior of a mixer, based on the equivalent cascode amplifier, brings an important practical advantage: the large-signal simulation of the gain of an amplifier is a single-frequency simulation, while for a mixer it involves the beat frequency $f_{LO}-f_{RF}$ and all its harmonics up to the RF and LO frequencies. This does not make a difference for harmonic-balance simulations, but for time-domain-based simulations it can reduce the simulation time by orders of magnitude.
Figure 6.3 shows simulation results as example of this correspondence of behavior for an emitter degenerated HBT cascode and the mixer equivalent: the input referred $P_{1\,\mathrm{dB}}$ is the same for both the circuits, while the gains are related according to equation (6.2). The simulated circuits are those of

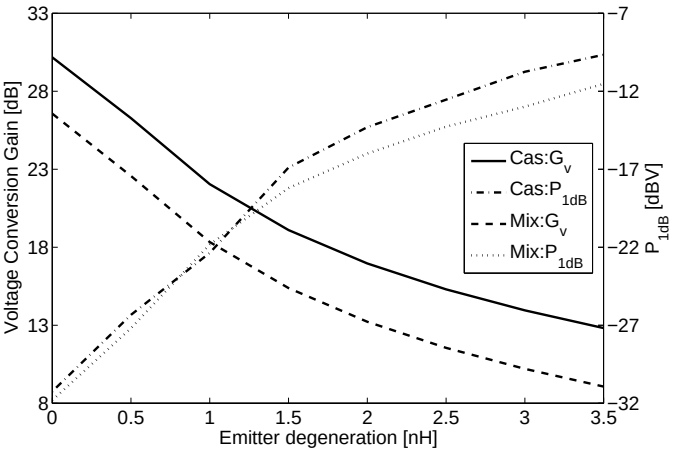


Figure 6.3: *Comparison of conversion gain and input referred $P_{1\,\mathrm{dB}}$ for a cascode amplifier and the corresponding singly-balanced mixer, as function of the emitter degeneration. RF is $5.5\,\mathrm{GHz}$ for both circuits and IF is $100\,\mathrm{MHz}$ for the mixer.*

Figure 6.2, with the addition of an inductive emitter degeneration and a real load $R_L = 1\,\mathrm{k}\Omega$; the RF frequency is $5.5\,\mathrm{GHz}$ for both circuits, and the IF frequency is $100\,\mathrm{MHz}$ for the mixer, driven by a $0.15\,\mathrm{V}$ LO signal.
The results in Figure 6.3 also show the effectiveness of inductive degeneration as linearization technique: for a given DC power consumption, conversion gain can be traded for linearity by increasing the degenerating inductance. A non-degenerated FET, being more linear, is an alternative to the degenerated HBT as first stage of the cascode amplifier: this allows to achieve similar performances, avoiding the use of large inductive degeneration, and saving chip area. Examples are in §8.1.2 and §8.2.

Noise

The time variance and frequency translation in mixers make it difficult to calculate accurately the noise figure. However, qualitative considerations

can help to draw some design guideline. In a mixer, the noise sources of interest lie in the RF stages, before downconversion, and in the LO and IF stage after downconversion.
In order to minimize the noise of the RF stage, it is useful to noise and power match the RF transconductance, following the procedure described in §5.1.1 for the input stage of LNAs. This reduces the noise contributed by the RF transconductance and, at the same time, provides frequency selectivity at the RF port. In this way, the thermal noise at higher frequencies, which would be downconverted by the the LO harmonics, are rejected and do not contribute to the noise at the IF frequency [2, 53, 54]. Example of this approach are given in §6.2.3 and §6.3.1.
Other noise sources are related to the switching pair: the emitter area of the switching HBTs has to be selected carefully in order to optimize the noise performance. Imperfect switching leads both transistors of the pair to be simultaneously on for a non-negligible fraction of the LO period. During this time both transistors see a low impedance ($\approx 1/g_m$) to ground; acting as common-emitter stages, amplify the thermal noise of their base resistance and inject their collector shot noise to the output. This increases the mixer noise figure [34]. For this reason, small and fast transistors are desirable. On the other hand, very small transistors have higher series base resistances, and the corresponding thermal noise, amplified to the IF output, is larger. This trade-off requires a careful choice of the device size. For the designs presented in this chapter the compromise was found by simulation of the noise behavior.

6.2 Singly-Balanced Active Mixers

Based on the idea depicted in Figure 6.2, three variants of singly-balanced mixers have been design and fabricated. In order to meet the linearity specification of the RF front-end, the mixers in §6.2.1 and §6.2.2 exploit modifications of the RF transconductance, i.e. inductive degeneration of an HBT and non-degenerated nFET. The mixer in §6.2.3 is based on a modification of the mixer core, which allows to share one RF transconductance between the two matched mixer of a receiver.

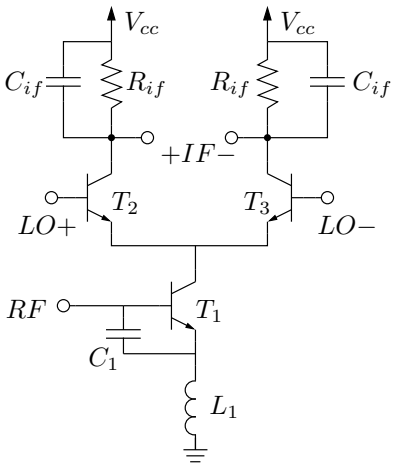


Figure 6.4: *Schematic of the HBT singly-balanced mixer. Bias network is not shown.*

6.2.1 HBT RF Transconductance

In systems like those described in §4 and §8, the intrinsic linearity of a non-degenerated HBT mixer is not sufficient to handle the input signal fed to the RF port by the LNA at the receiver compression point: for an LNA with $15\,\mathrm{dB}$ of gain, the mixer receives at the RF port up to $-6\,\mathrm{dBm}$ if matched to $50\,\Omega$, equivalent to $-13\,\mathrm{dBV}$ on a large input impedance.
The graph in Figure 6.3 shows the effect of inductive degeneration on gain and linearity of a singly-balanced mixer: the emitter degeneration can be determined to meet the linearity specification of the system, whereas the gain can be adjusted with the collector current of the RF transconductance.
The circuit presented in this paragraph has been designed with this approach as downconversion stage of the low-IF receiver in §8.1.1 and [52]. Figure 6.4 shows the schematic of the circuit. A common-emitter HBT T_1 is strongly degenerated with a large spiral inductor L_1: the resulting input impedance has a small reactive component, compensated by a small capacitor C_1, which eases the design and characterization of the previous stage (LNA). The resulting input impedance is $200\,\Omega$. The load is the shunt of

Table 6.1: *Design values for the schematic in Figure 6.4.*

T_1	$2 \times 15\,\mu\mathrm{m} \times 320\,\mathrm{nm}$
$T_{2,3}$	$2 \times 10\,\mu\mathrm{m} \times 320\,\mathrm{nm}$
L_1	$3\,\mathrm{nH}$
C_1	$990\,\mathrm{fF}$
R_{if}	$1\,\mathrm{k}\Omega$
C_{if}	$1.5\,\mathrm{pF}$
V_{cc}	$3\,\mathrm{V}$
I_{cc}	$2.3\,\mathrm{mA}$

a resistor and a capacitor: the resistors determine the gain and the quiescent voltage the mixer core collectors, in order to allow sufficient voltage headroom at the input compression point; the capacitors suppress the large LO-to-IF feedtrough and has no effect at the IF frequencies.
Table 6.1 reports the design values for the circuit in Figure 6.4, chosen for fabrication in IBM BiCMOS 6HP technology. Figure 6.5 shows a detail of the chip where two mixers are implemented, as part of a receiver. The pair of mixers occupies $0.185\,\mathrm{mm}^2$ of active area.
An independent test structure for this mixer was not fabricated, but an estimation of its performances can be extrapolated by comparison of the measurements of the LNA (§5.5.2) and the complete receiver (§8.1.1). The results of this indirect characterization are reported in Table 6.2.

6.2.2 nFET RF Transconductance

As an alternative to the inductive degeneration, the linearity of a singly-balanced active mixer can be improved implementing the RF transconductance with a FET. This allows to save active area, because no source degeneration is needed. The main drawback of this approach comes from the difficulties in matching the RF port to $50\,\Omega$, direct consequence of the lack of inductive degeneration. For this reason, this kind of mixer is particularly suitable for single-chip systems, as those presented in §8.1.2 (page 132)

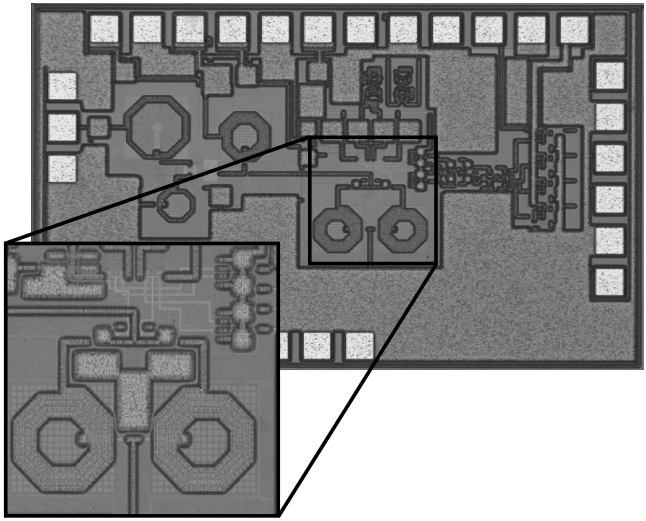


Figure 6.5: *Photograph of two HBT singly-balanced mixers, integrated in a low-IF receiver front-end (§8.1.1), [52]. The two mixers shown occupy a chip area of* $430\,\mu\mathrm{m} \times 430\,\mu\mathrm{m}$.

Table 6.2: *Summary of extrapolated performance of the HBT singly-balanced mixer in Figure 6.4. RF is* $5.3\,\mathrm{GHz}$ *and IF* $40\,\mathrm{MHz}$.

Conv. Gain	12.7	dB
$P_{1\,\mathrm{dB}}$	-6.7	dBm
iIP_3	-0.2	dBm
LO amplitude	~ 0.15	V
Active area	0.185	mm^2

and §8.2.1 (page 142), where power matching to real impedances is not necessary. On the other hand, the characterization of test structures in a $50\,\Omega$ test environment becomes difficult.
The circuit presented in this paragraph has been designed and fabricated as test structure, with the purpose of verifying the performances of this kind of mixer when employed in lager systems.
Figure 6.6 shows the schematic of the test chip. Transistors T_{1-3}, together with the resistive loads R_{if}, constitute the singly-balanced active mixer. Inductor L_1 and capacitor C_1 resonates with the input capacity of the nFET at $5.5\,\mathrm{GHz}$. This allows to test the voltage matching used on-chip for the receivers in §8.1.2 and §8.2.1, and simplifies the estimation of the voltage conversion gain. In fact, at resonance, the input impedance of the RF port is dominated by the real part of the nFET input impedance, which is in the order of $2-3\,\mathrm{k}\Omega$.
No tuning was implemented at the LO port, because this would limit the LO band available for testing. A precise control of the LO amplitude is not necessary in measuring the main RF figures of merit.
The first column of Table 6.3 resumes the design values for the BiCMOS singly-balanced mixer. A photograph of the fabricated chip is in Figure 6.7: the total area measures $1323\,\mu\mathrm{m}\times 923\,\mu\mathrm{m}$, but the active area of the mixer, without RF input resonator, is only $0.12\,\mathrm{mm}^2$, making this solution attractive for compact systems.

For characterization, the chip was mounted on a microstrip test board. The differential LO signal was generated by means of a microwave hybrid, and the results presented have been de-embedded from its attenuation. The IF signal was sensed single-ended, with the second IF port terminated by the same $50\,\Omega$ impedance of the cable, in order to ensure a symmetric differential load. The results in Figure 6.8 and 6.9 have been corrected to represent the behavior with differential output.
Due to the absence of resonant matching at the LO and IF port, the mixer exhibits a similar behavior over a broad range of IF frequencies, from near DC to $1\,\mathrm{GHz}$. The results presented here have been measured for RF at $5.5\,\mathrm{GHz}$ and IF $500\,\mathrm{MHz}$. Figure 6.8 shows the measurement of voltage conversion gain and iIP$_3$ as function of the LO amplitude. The conversion gain reaches its peak already at relatively small LO amplitudes, and has a small dependance on it.
Figure 6.9 presents an example of extrapolation of $\mathrm{P}_{1\,\mathrm{dB}}$ and iIP$_3$. A similar behavior has been observed for a broad range of LO and IF frequencies,

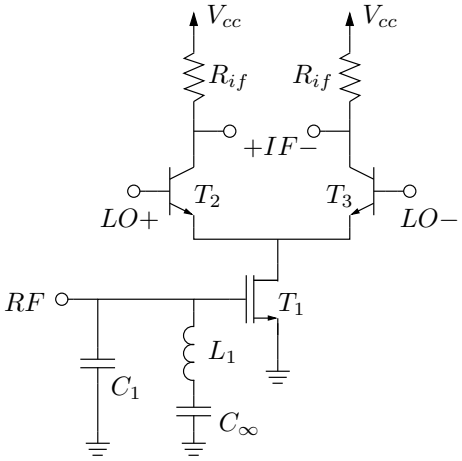


Figure 6.6: *Schematic of the BiCMOS singly-balanced mixer. Bias network in not shown.*

Table 6.3: *Design values for the schematic in Figure 6.6 and the modified version used for the receiver in §8.1.2.*

	test chip	§8.1.2
T_1	$20 \times 5\,\mu\text{m} \times 240\,\text{nm}$	$20 \times 11.5\,\mu\text{m} \times 240\,\text{nm}$
$T_{2,3}$	$2 \times 15\,\mu\text{m} \times 320\,\text{nm}$	$2 \times 10\,\mu\text{m} \times 320\,\text{nm}$
L_1	$1.36\,\text{nH}$	—
C_1	$390\,\text{fF}$	—
Z_{if}	$750\,\Omega$	$850\,\Omega \| 1.46\,\text{pF}$
V_{cc}	$3\,\text{V}$	$2.4\,\text{V}$
I_{cc}	$3.2\,\text{mA}$	$2\,\text{mA}$

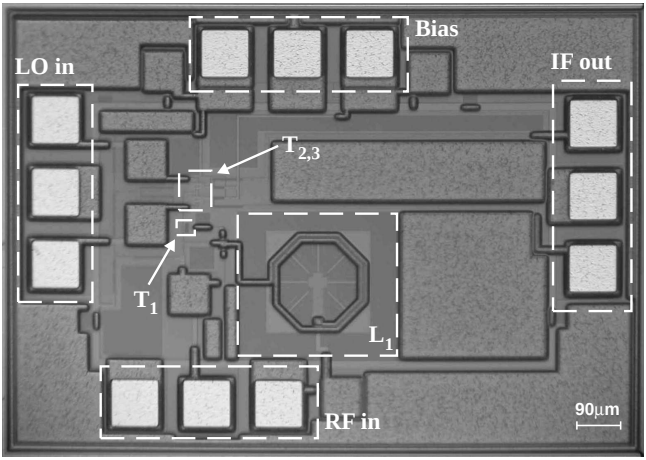


Figure 6.7: *Photograph of the test chip for a BiCMOS singly-balanced mixer. Area shown measures* $1323\,\mu\mathrm{m}\times 923\,\mu\mathrm{m}$*; active area is* $0.12\,\mathrm{mm}^2$*, including two large LO coupling capacitors.*

when the RF band corresponds to the input resonator frequency.
A comparison with the simulated performance of the mixer is presented in Figure 6.8 and Figure 6.9. The behavior of the mixer is predicted with acceptable accuracy, being the deviation for gain and linearity in the order of $3-4\,\mathrm{dB}$.
The linearity of this test structure would not be sufficient to meet the specifications for the receiver in §8.1.2: the circuit has been redesigned, using the same topology, but resizing the FET transconductance. The values for the modified mixer used for the BiCMOS low-IF receiver are in the second column of Table 6.3. Since the circuits in §8.1.2 does not allow to measure the LNA and mixer separately, only the performance of the complete circuit can presented.

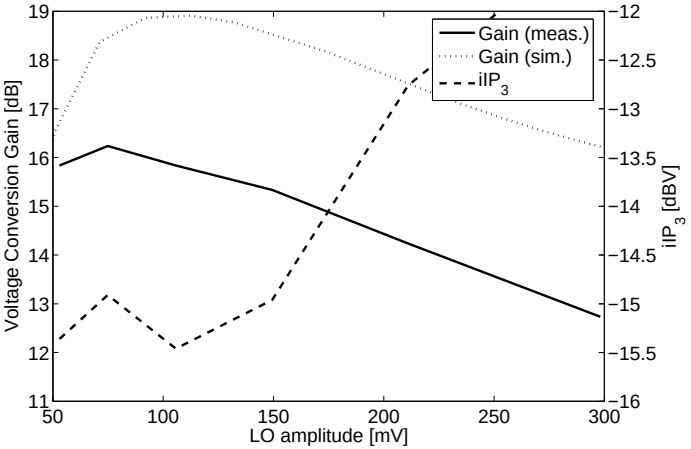


Figure 6.8: *Voltage conversion gain and iIP_3 as function of the LO amplitude. RF is* $5.5\,\mathrm{GHz}$ *and IF* $500\,\mathrm{MHz}$*.*

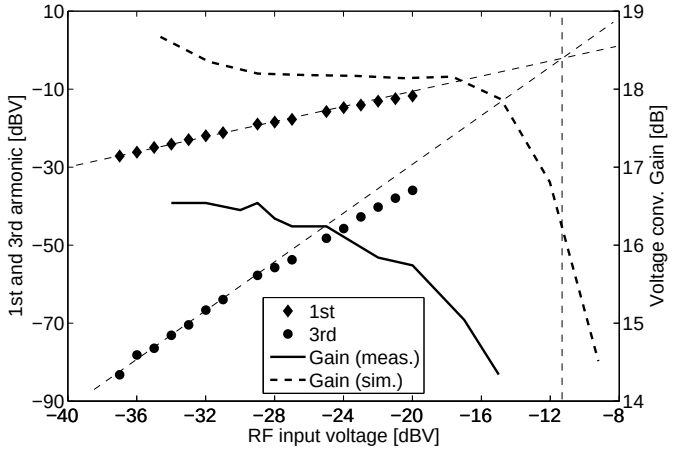


Figure 6.9: *Input-referred third-order intercept point extrapolation. IF is* $500\,\mathrm{MHz}$ *and RF* $5.5\,\mathrm{GHz}$*.*

6.2.3 Image-Rejecting Merged LNA and Mixer

Table 2.2 resumes the main specifications for an RF front-end compliant with the main $5\,\mathrm{GHz}$ standards. Promising results achieved at lower frequencies [53] suggest that the RF front-end might not need pre-amplification to meet the noise-figure requirements. Such a simplification of the receiver architecture would bring benefits in terms of power-consumption and linearity.
This paragraph presents design and implementation of an image-rejecting mixer, which fulfills the given specifications for the whole RF front-end. The circuit is an evolution of simpler singly-balanced active mixers [34]. In order to achieve image rejection and/or IF I and Q signals, two mixers are necessary with the standard system architectures and building blocks: this requires two independent RF transconductances. However, the two RF current signals fed into the switching pairs must be equal, and this makes possible to use a single transconductance. If this transconductance is designed for optimun RF noise behavior, the topology, mostly used in its differential version, is referred to as *merged LNA and mixer* [53, 55].
The schematic in Figure 6.10 shows the detail of the circuit. It consists of

- one common-emitter HBT transconductance T_1, which is noise and power matched to $50\,\Omega$ by means of two inductors $L_1 - L_2$ and one capacitor C_1;
- two switching pairs $T_2 - T_5$, driven by I and Q differential LO signals;
- resistive IF loads R_{if} in parallel with capacitors C_{if}, which suppress LO feed-through;
- one LO polyphase filter for the generation of quadrature differential LO;
- one IF polyphase filter to provide image rejection.

The RF transconductance was designed by applying the same considerations that usually lead the design of low-noise amplifiers (§5.1). This requires a good estimation of the load at the collector of T_1, because it affects significantly the input impedance. The input matching network was designed assuming that the four transistor $T_2 - T_5$ are biased at the same DC operating point, and share the same bias current. Even if this situation does not

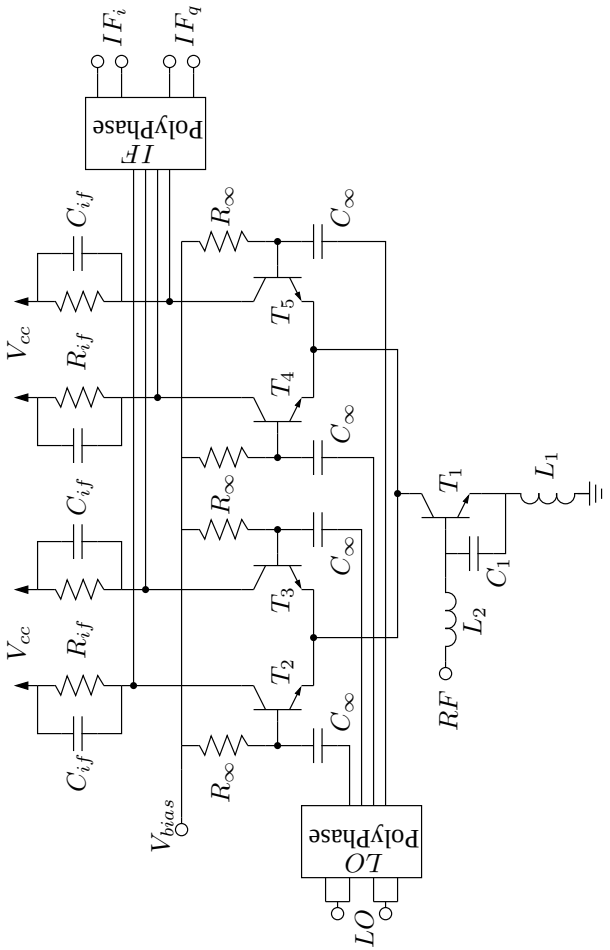


Figure 6.10: *Schematic of the merged LNA and mixer. Bias network is shown only partially at the LO input ports. The two polyphase filters are both based on two-stage RC standard topologies.*

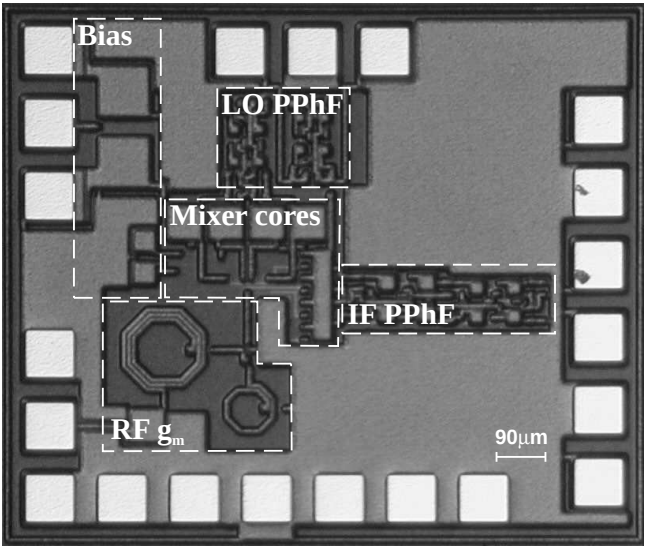


Figure 6.11: *Photograph of the merged LNA and mixer. Area shown measures* $1.33\,\mathrm{mm}\times1.12\,\mathrm{mm}$*, total active area is* $0.34\,\mathrm{mm}^2$.

occur in normal circuit operation, simulations have shown that the average impedance seen by the collector of T_1 is approximated with sufficient precision.

As described in §6.1.1, the emitter area of the switching HBTs has to be selected carefully in order to optimize the noise performance. For this design the compromise was found by simulation of the noise behavior.

The resistive loads R_{if} determine the conversion gain, which is limited by linearity constrains. The resistance is chosen to leave sufficient output voltage headroom at the compression point. The shunt capacitors C_{if} lower the load-impedance at LO frequencies and suppress the large LO feed-through at the IF output, which could easily saturate the following stages and the mixer itself.

The LO polyphase filter is used for quadrature signal generation. In order to broaden its bandwidth and allow the down-conversion of the $5-6\,\mathrm{GHz}$ band, this filter has been designed as a cascade of two stages. In order to

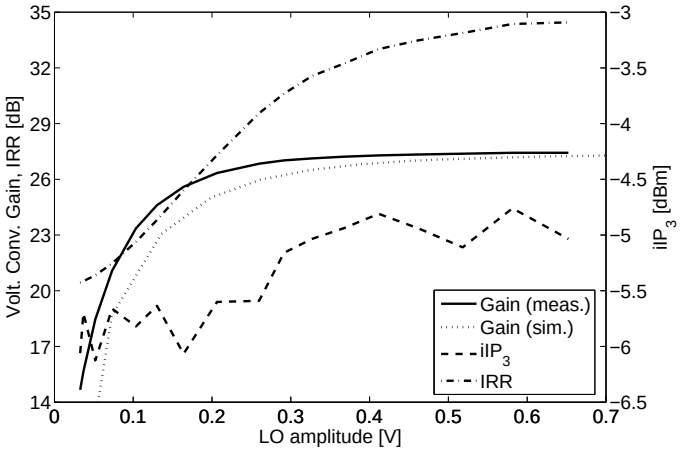


Figure 6.12: *Voltage conversion gain, image rejection ratio and iIP$_3$ as function of the LO amplitude.*

simplify the interface to $50\,\Omega$ RF measurement instrumentation, the impedance level has been kept low, leading to a voltage attenuation of about $4\,\mathrm{dB}$. The IF polyphase filter is used to provide image rejection over the $20\,\mathrm{MHz}$ channel bandwidth of the main $5-6\,\mathrm{GHz}$ WLAN standards. Center frequency is set at $40\,\mathrm{MHz}$. The impedance level is higher than the IF mixer output to avoid voltage signal losses. Both polyphase filters have been designed as resumed in §7 (page 117).
The circuit consumes $3\,\mathrm{mA}$ from a $2.4\,\mathrm{V}$ supply.

Experimental results

The circuit was fabricated with the commercial IBM BiCMOS 7HP process, on a $0.34\,\mathrm{mm}^2$ active area, as shown in Figure 6.11. Total chip area measures $1.33\,\mathrm{mm}\times\ 1.12\,\mathrm{mm}$ [2].
For characterization the chip was mounted and bonded on a microstrip test substrate. Differential LO and IF signals have been generated and combined by means of microwave hybrids and results de-embedded from their attenuations.

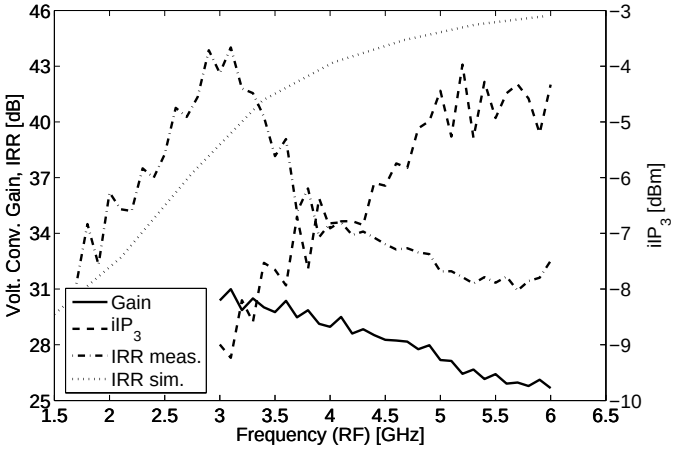


Figure 6.13: *Voltage conversion gain, image rejection ratio and iIP_3 as function of the RF frequency. IF is fixed at $40\,\mathrm{MHz}$, the LO frequency is adjusted accordingly.*

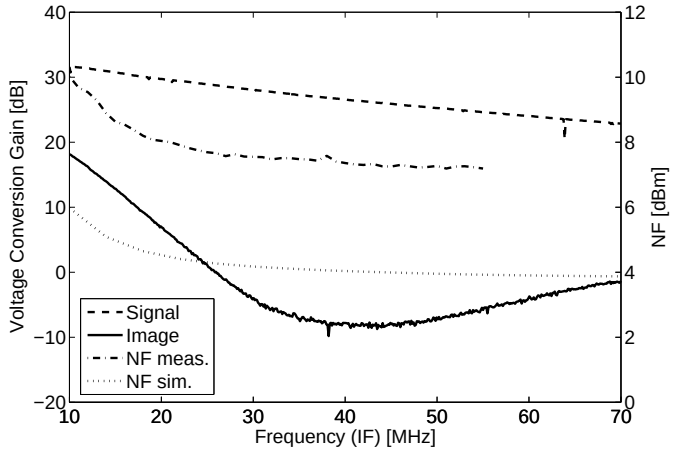


Figure 6.14: *Noise figure and voltage conversion gain for signal and image, as a function of the IF frequency for U-NII band at $5.3\,\mathrm{GHz}$.*

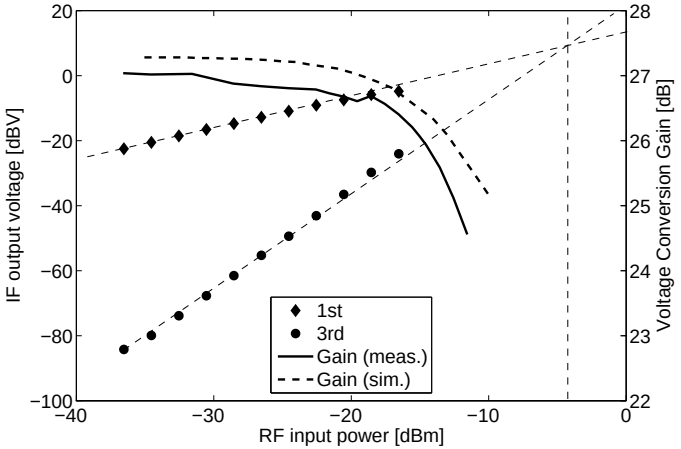


Figure 6.15: *iIP$_3$ and $P_{1\,\mathrm{dB}}$ extrapolation for U-NII band at* $5.3\,\mathrm{GHz}$.

The graph in Figure 6.12 shows the behavior, at nominal bias ($\mathrm{I}_{cc}=3\,\mathrm{mA}$, $\mathrm{V}_{cc}=2.4\,\mathrm{V}$), of voltage conversion gain, iIP$_3$ and IRR as function of the LO voltage swing for a test RF frequency of $5.3\,\mathrm{GHz}$, corresponding to the center of the second U-NII band, and an IF of $40\,\mathrm{MHz}$. A similar behavior has been observed over the whole $5-6\,\mathrm{GHz}$ RF range. The mixer performance improves at larger LO driving voltage: gain and linearity saturate at a relatively small LO amplitude, while IRR increases monotonically with higher values. This can be explained as follows: since the IRR depends on I-Q amplitude and phase balance, a higher LO voltage amplitude drives the mixing pairs into deeper saturation and compensates the possible LO amplitude unbalances. Depending on the target application and receiver architecture, the LO voltage amplitude can be set according to the IRR requirements. The $5-6\,\mathrm{GHz}$ IEEE WLAN standards require an IRR of $32\,\mathrm{dB}$ (§2.1): for this reason the rest of the characterization has been performed at the corresponding LO amplitude of $0.35\,\mathrm{V}$.
Also the simulation of the voltage conversion gain as function of the LO voltage amplitude is presented in Figure 6.12: both the conversion gain and dependance on LO signal are predicted with good accuracy.

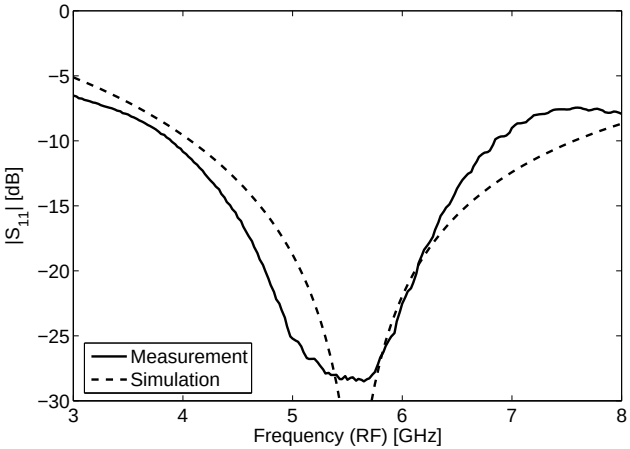


Figure 6.16: *Simulated and measured matching to* $50\,\Omega$ *for the RF port of the merged LNA and mixer.*

Table 6.4: *Summary of experimental results for the merged LNA and mixer.*

RF band ($-10\,\mathrm{dB}$)	$3.8-6.9$	GHz
Conv. Gain	27	dB
IRR	32	dB
NF	7	dB
$\mathrm{P}_{1\,\mathrm{dB}}$	-15.5	dBm
iIP_3	-5.2	dBm
LO amplitude	0.35	V
In-band emission	<-49.1	dBm
Supply	2.4	V
Bias current	3	mA
Active area	0.31	mm^2

Figure 6.13 shows the mixer frequency response for an IF of $40\,\mathrm{MHz}$ at the chosen LO amplitude: the highest values of IRR are achieved out of the target band. This can be explained by inaccuracy in modelling the small capacitors of the LO polyphase filter and their parasitics. Still the IRR achieved on the $5-6\,\mathrm{GHz}$ band is sufficient for WLAN applications. For comparison, the simulation of the frequency behavior of IRR is shown.
Figure 6.14 shows the signal- and image-frequency voltage conversion gain versus IF, together with the corresponding noise figure: the highest NF value in the $30-50\,\mathrm{MHz}$ band is $7\,\mathrm{dB}$. The NF measurement is compared with the corresponding simulation: the frequency dependance meets the expectation, whereas the actual value is about $2\,\mathrm{dB}$ higher. This can be explained by considerations similar to those in §5.5.1 and §5.5.2 for the LNAs, but also by the difficulties in modelling accurately the noise of mixers (§6.1.1).
Figure 6.15 shows $\mathrm{iIP_3}$ extrapolation and $\mathrm{P_{1\,dB}}$ measurement. The input matching as a function of the frequency represented is in Figure 6.16.
Table 6.4 resumes the measured results: input matching, conversion gain, linearity, noise figure and isolation meet the specifications for the implementation of a RF WLAN front-end without preamplification.

Conclusion

The circuit performances and, in particular, the low noise figure allow the use of this mixer as RF front-end of receiviers compliant with IEEE WLAN standards at $5\,\mathrm{GHz}$ without a preamplifier.
A remarkable feature of the presented circuit is the high conversion-gain to power-consumption ratio: Figure 6.17 compares this work with a selection of high-performance receivers and mixers. The presented G_v/P_{DC} ratio is the highest reported for this kind of circuit at any frequency, as well as the highest reported for the $5-6\,\mathrm{GHz}$ band. In comparison to the traditional LNA-mixer cascade, this approach is attractive, in particular for low-power applications.

6.3 Doubly-Balanced Active Mixers

To prevent the LO signal from reaching the IF output port, two singly-balanced mixers can be combined in a doubly-balanced mixer. The classic Gilbert switching-quad topology, shown in Figure 6.18 and 6.25 with

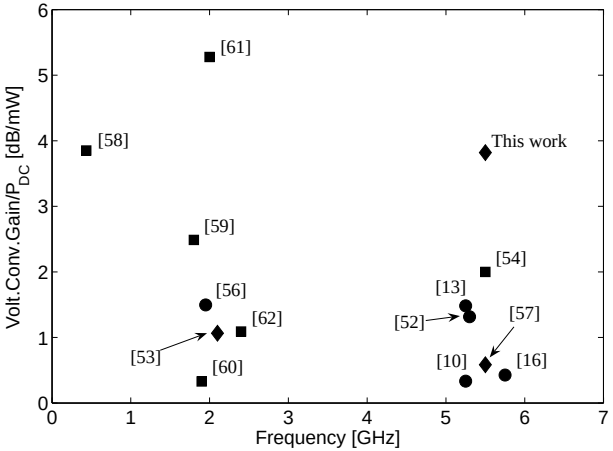


Figure 6.17: *Comparison of recently published receiver and mixer performances. Different topologies are compared: merged LNA and mixer (diamonds), cascade LNA-mixer (circles) and active mixers (squares).*

transistors T_{3-6}, exploits the fact that the gain of a common-emitter voltage amplifier is inverting, while the gain of a common-base current amplifier is not: the two-single balanced mixers are connected in parallel for the RF signal and in antiparallel for the LO signal. Therefore the RF signal components sum in-phase at the IF output, and the LO components in anti-phase. This paragraph presents the design and characterization of two variants of doubly-balanced active mixers.

6.3.1 Gilbert Mixer

The circuit presented in this paragraph is the combination of a Gilbert switching quad and a noise- and power-matched HBT differential pair, which acts as RF transconductance [63].
The mixer schematic is shown in Figure 6.18. The active part of the circuit consists of a transconductance pair $T_1 - T_2$, noise and power matched by means of inductors $L_1 - L_2$; a mixing quad $T_3 - T_6$; resistive loads R_{if}. A

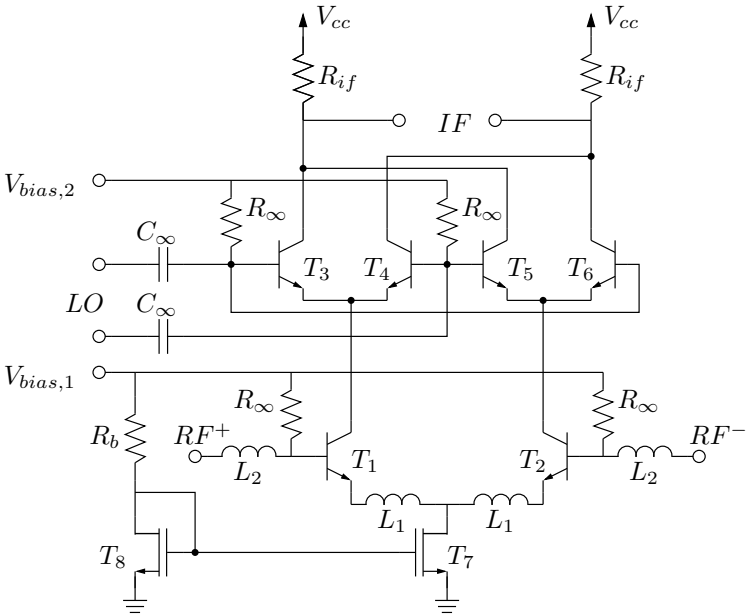


Figure 6.18: *Schematic of the Gilbert mixer. A simplified bias network is shown; the circuit is operated with a* $3.3\,\mathrm{V}$ *voltage supply, provided with two contact pads for test purposes.*

resistive bias network, not entirely shown in the schematic, together with a FET current mirror, were chosen in order to allow simultaneous control of the current operating point of all the active devices [54].
The differential RF input is fed into the circuit through the bases of the transconductance pair. In order to reduce the noise contribution of this circuit block, the transistors and the matching network have been designed for simultaneous noise and power matching to $50\,\Omega$, as described in §5.1.1.
Since the mixing quad has also a significant impact on the overall mixer noise figure, for this circuit, quad transistors where set to half the transconductance transistor size: as described in §6.1.1, the size reduction improves the switching time, but is limited by the effects of parasitic base resistance on the noise figure.

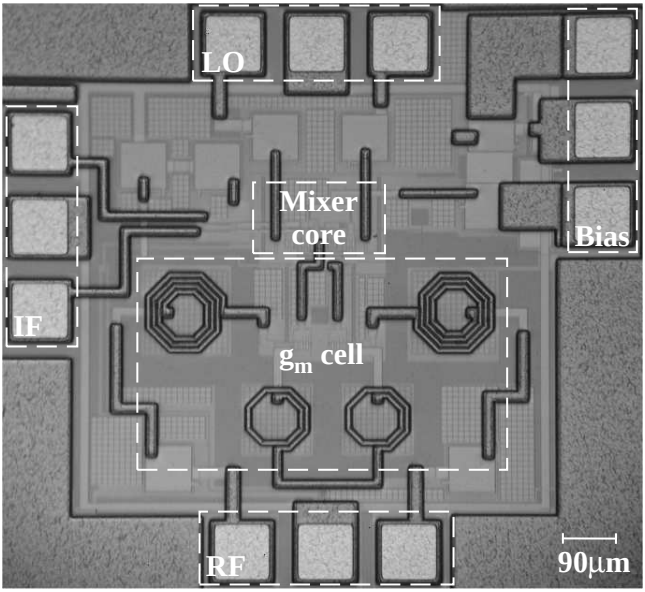


Figure 6.19: *Photograph of the Gilbert mixer. Area shown measures* $988\,\mathrm{mm} \times 900\,\mathrm{mm}$*; active area is* $0.53\,\mathrm{mm}^2$.

The IF load resistors where determined to provide the highest gain while allowing, at the compression point, sufficient voltage headroom for the signal at the IF port.

Both IF and LO ports are not power matched to any specific impedance. For the LO port, a power match is not necessary, because at this port the circuit behavior is mainly voltage-driven, and this class of circuits is often integrated with on-chip low-impedance buffers. For the IF port, a power match would be quite impractical, because the IF frequency is typically below a few hundreds of MHz and the IF receiver blocks can be easily designed to offer a high input impedance.

In order to allow an unloaded characterization of the circuit in a $50\,\Omega$ measurement environment, two large resistors, not shown in Figure 6.18, have been integrated in series to the IF port.

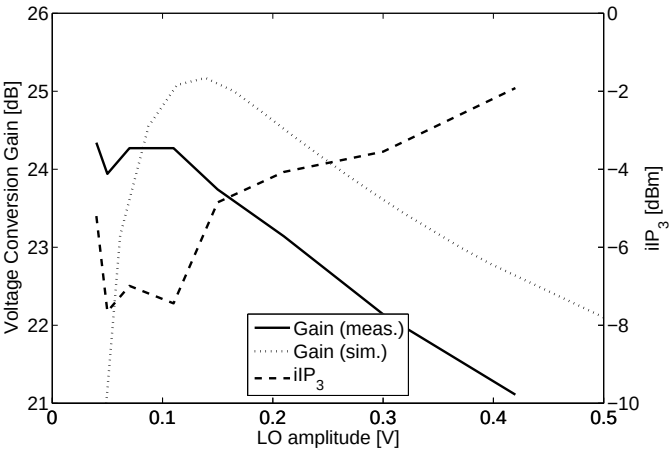


Figure 6.20: *Voltage conversion gain and iIP$_3$ versus LO voltage amplitude. IF is at* $500\,\mathrm{MHz}$.

Experimental results

The circuit was fabricated with the IBM BiCMOS 6HP technology, on a $760\,\mu\mathrm{m}\times 700\,\mu\mathrm{m}$ active area, as shown in the photograph in Figure 6.19. In order to prevent magnetic coupling, the inductors are provided with a guard distance of $60\,\mu\mathrm{m}$. Further experiences with this technology have shown that this precaution is very conservative.

For its characterization, the chip has been mounted on a microstrip test board. The presented measured results have been de-embedded from the effects of the power dividers and combiners, as well as the integrated large resistors in series to the IF port.

As mentioned above, the LO and IF ports do not have any frequency dependent matching. The circuit has been tested for the IF range $50-500\,\mathrm{MHz}$ and shows, as expected, variations of at most $1-2\,\mathrm{dB}$ in its main figures of merit.

The measured input RF reflection coefficient is well below $-10\,\mathrm{dB}$ over the whole $5-6\,\mathrm{GHz}$ target band. Figure 6.20 shows an example of the behavior of voltage conversion gain and iIP$_3$ as a function of the LO voltage. The

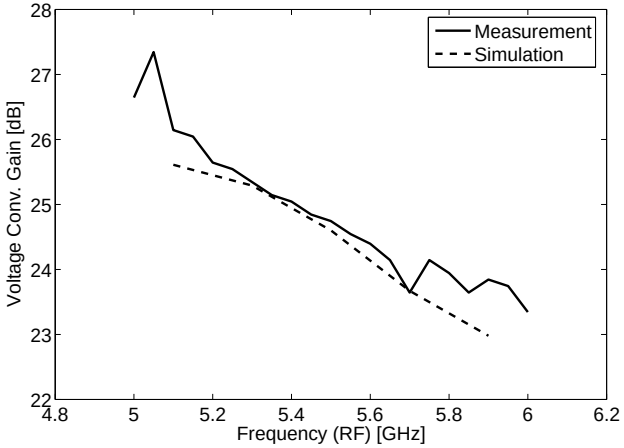


Figure 6.21: *Down-conversion gain versus of RF frequency. IF is fixed at* $50\,\mathrm{MHz}$*, LO frequency swept with* $0.15\,\mathrm{V}$ *amplitude.*

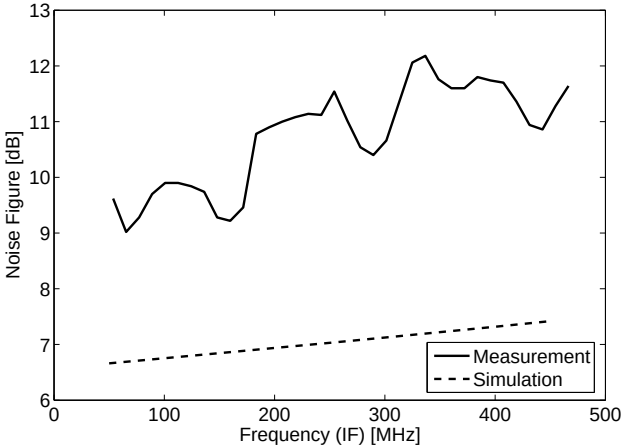


Figure 6.22: *Double-side-band noise figure versus IF. LO is at* $5.5\,\mathrm{GHz}$*.*

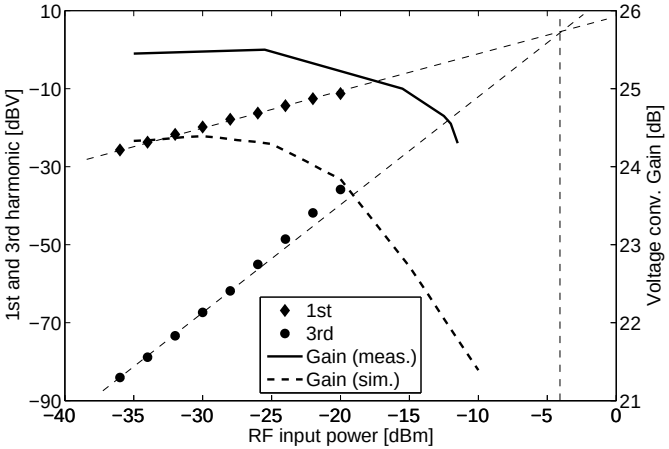


Figure 6.23: *Input-referred third-order intercept point extrapolation. IF is* $500\,\mathrm{MHz}$ *and RF* $5.5\,\mathrm{GHz}$.

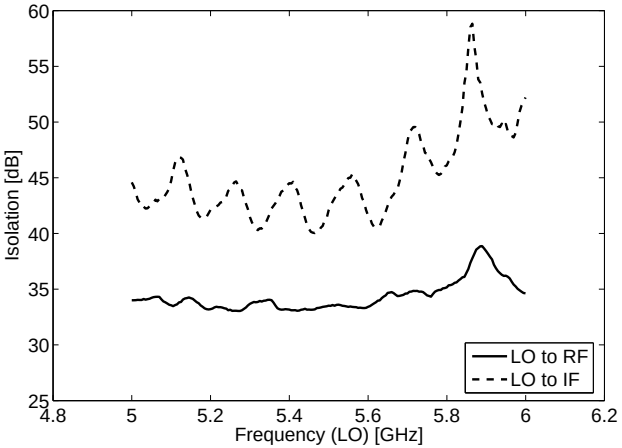


Figure 6.24: *Isolation of the LO signal at the IF and RF ports. The test was performed on a chip mounted on a microstrip test board.*

Table 6.5: *Summary of experimental results for the Gilbert mixer.*

RF band	$5-6\,\mathrm{GHz}$
LO frequency	up to $6.5\,\mathrm{GHz}$
LO amplitude	$0.15\,\mathrm{V}$
S_{11} $50\,\Omega$	$<-10\,\mathrm{dB}$
Conv. Gain	$23-25\,\mathrm{dB}$
NF_{DSB}	$9-12\,\mathrm{dB}$
P_{1dB}	$-12\,\mathrm{dBm}$
iIP_3	$-4\,\mathrm{dBm}$
LO - RF isolation	$>33\,\mathrm{dB}$
Supply	$3\,\mathrm{V}$
Bias current	$4\,\mathrm{mA}$
Active area	$0.53\,\mathrm{mm}^2$

measurement was performed at an RF center frequency of $5.5\,\mathrm{GHz}$; similar results have been observed at $5.2\,\mathrm{GHz}$ and $5.9\,\mathrm{GHz}$. For this circuit and its application, the range V_{LO}=$0.15 \div 0.20\,\mathrm{V}$ was judged as optimum and the rest of the characterization has been performed at this LO level. Figure 6.21 shows the conversion gain with a fixed IF frequency of $50\,\mathrm{MHz}$, as a function of the RF frequency. Figure 6.22 shows the measured double side band noise figure. For an IF of $50-60\,\mathrm{MHz}$, the NF is below $9.5\,\mathrm{dB}$. Figure 6.23 shows the results of two-tone and large-signal tests: the extrapolated iIP_3 is about $-4\,\mathrm{dBm}$ and the $\mathrm{P}_{1\,\mathrm{dB}}$ is around $-12\,\mathrm{dBm}$. Figure 6.24 shows the isolation of the LO signal at the IF and RF port in the $5-6\,\mathrm{GHz}$ band.

In addition, Figures 6.20, 6.21, 6.22, 6.23 present an example of comparison between measurements and simulations. The available models allow the prediction of the voltage conversion gain with a $1-2\,\mathrm{dB}$ uncertainty. For other mixers presented in this paragraph the gap enlarged up to $5-6\,\mathrm{dB}$, possibly due to process tolerances on transconductance and resistors. Ac-

ceptable accuracy is possible also in simulating the $P_{1\,dB}$ and LO signal amplitude. The measured noise is always higher than simulated. This is due to the many noise sources that are not taken into account in simulation, such as the losses in the metal connection and their interaction with the substrate.

Conclusion

Table 6.5 resumes the main experimental results for the Gilbert mixer. For $5\,GHz$ WLANs, isolation and noise figure require the use of this mixer in combination with a LNA, but the good overall performance can relax significantly the noise figure and preamplification required to meet the standard specifications presented in §4.

6.3.2 Micromixer

The Micromixer is a variant of the standard Gilbert cell [64], which extends the linear range replacing the RF differential pair with a *bisymmetric* class-AB topology. This allows to avoid the use of inductive emitter degeneration.
Figure 6.25 shows a schematic of the circuit: the mixer core is the same used for the Gilbert mixer and the important differences lie in the RF input transconductance. Transistor T_2 is a common-base amplifier, which delivers its non-inverted current-signal to the pair T_{3-4}. Transistor T_1 is a common-emitter amplifier, which delivers its inverted current-signal to the pair T_{5-6}. Since the two stages have similar gains, the transistors T_{1-2} convert a single-ended input voltage to a differential current.
This input stage is much more linear than a differential pair biased with the same current. Transistor T_1 can handle a large positive excursion of the input voltage. Similarly, transistor T_2 can handle a large negative excursion. The difference of those two non-linear currents provides a symmetric differential transfer characteristic, which is linear and independent of the bias current. The large signal behavior of the pair can be satisfactory for many application. The avoidance of inductive degeneration makes this topology attractive in monolithic implementations.
The input impedance is dominated by the low input impedance of the common-base stage T_2, which depends directly on the the inverse of the bias current. As a result, the input impedance is almost real and frequency inde-

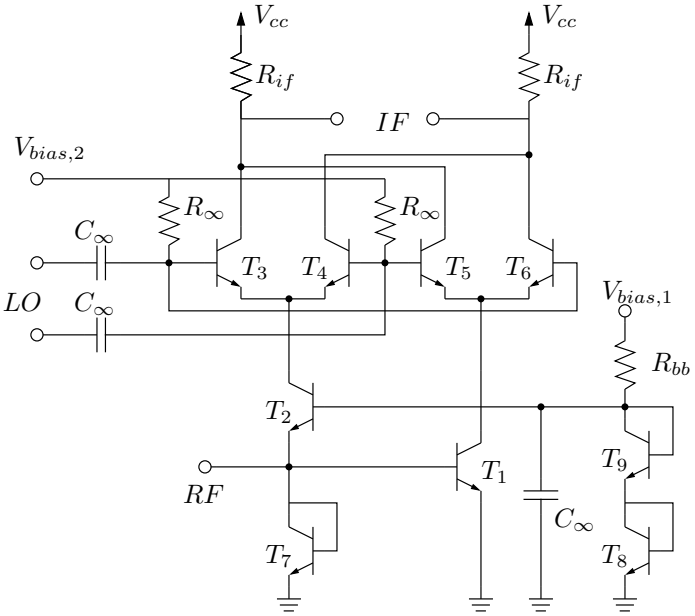


Figure 6.25: *Schematic of the Micromixer. A simplified bias network is shown. The circuit is operated with a* $3.3\,\mathrm{V}$ *voltage supply, provided with two contact pads for test purposes.*

Table 6.6: *Design values for the Micromixer.*

T_{1-9}	$20 \times 10\,\mu\mathrm{m} \times 320\,\mathrm{nm}$
R_{if}	$600\,\Omega$
V_{cc}	$3.3\,\mathrm{V}$
I_{cc}	$2.1\,\mathrm{mA}$
Z_{in}	$\sim 19\,\Omega$

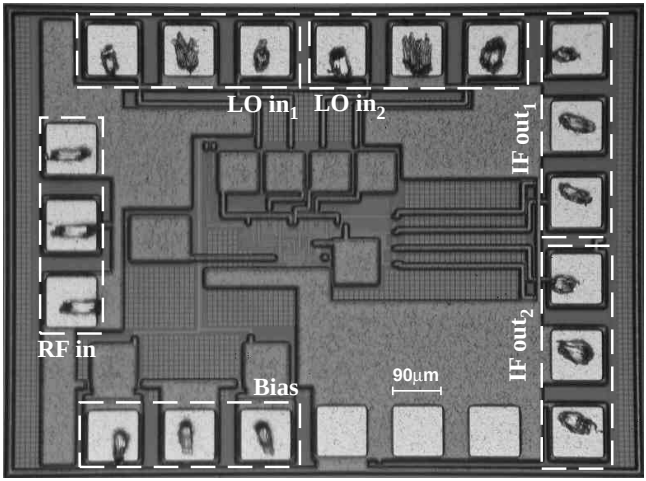


Figure 6.26: *Photograph of the test chip for the Micromixer. The size of the chip is* $1249\,\mu\mathrm{m} \times 923\,\mu\mathrm{m}$*; the active area occupied by the two matched Micromixers is* $0.048\,\mathrm{mm}^2$.

pendent from low-frequencies up to the limits given by parasitic capacitances. This allows a broadband power matching for the RF port. For very large RF-signal excursions, the incremental input impedance drops to low values. This is due to the fact that for large negative RF signals the emitter impedance of transistor T_2 lowers, while for positive signals the diode-connected transistor T_7 dominates similarly. As a consequence, this input stage does not show gain compression, but rather expansion in the main-carrier output at high input-signal levels. This effect, however, is not due to a reduction of the third order harmonic component. In fact, this mixer typically exhibits iIP_3 in the same range as the other active-mixer alternatives.
The bias current affects the linearity and the gain, and cannot be set independently to match the RF port: if the voltage headroom at the IF port is determined by the system specifications, then the current must be set according to the transconductance needed in the RF stage, in order to provide sufficient conversion gain. This is often a serious drawback for the micromixer: since the current depends on other constraints, the input impedance can be rather

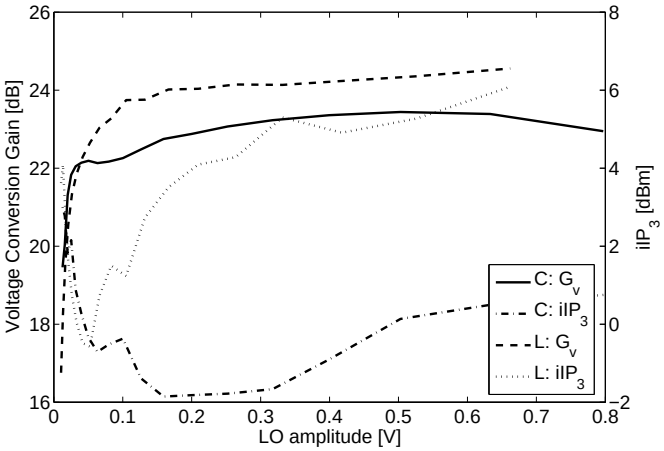


Figure 6.27: *Voltage conversion gain and iIP$_3$ versus LO voltage amplitude. IF is at* $40\,\mathrm{MHz}$ *and RF test signals are fed at C band (*$5.5\,\mathrm{GHz}$*) and L band (*$2.45\,\mathrm{GHz}$*).*

low for monolithic systems. For example, in the reconfigurable receiver presented in §4.4.2, the required gain for the mixer is the $25-30\,\mathrm{dB}$ range and forces the RF input impedance down to $19\,\Omega$ for each of the two mixers. Another significant drawback of this topology is the large bias voltage needed for its operation: if the forward bias of *p-n* (or *base-emitter*) junctions in the available technology is V_{fw}, then the collector of transistor T_2 has to be biased at $2V_{fw}$, or slightly below that. This is by V_{fw} higher than the bias voltage of the corresponding node in a Gilbert mixer and in similar single-ended versions. In IBM BiCMOS 6HP technology, V_{fw} is about $0.8\,\mathrm{V}$: for this reason the circuit presented in this paragraph had to be biased at $3.3\,\mathrm{V}$, which is higher than the typical bias of other active mixers exhibiting similar performances (e.g. $2.4\,\mathrm{V}$ is used for the mixer presented in §6.2).

Experimental results

The mixer in the schematic in Figure 6.25 was fabricated with the IBM BiCMOS 6HP technology. Figure 6.26 shows a photograph of the chip, where

two matched micromixers have been integrated as test structure for a receiver of the type presented in §4.4.2. The chip measures $1249\,\mu\mathrm{m} \times 923\,\mu\mathrm{m}$, and the active area occupied by the two matched micromixers is $0.048\,\mathrm{mm}^2$, including a large capacitor necessary for a proper bias of the RF stage.
As mentioned above, the mixer does not have any resonant matching at the input RF port. Similarly to other mixers presented in this chapter, no matching is present at the other ports. This makes the mixer inherently broadband. For this reason, the LO amplitude required for operation was tested on two bands of interest, as shown in Figure 6.27: RF frequencies at $2.45\,\mathrm{GHz}$ (labelled L in the graph) and $5.5\,\mathrm{GHz}$ (labelled C) are both downconverted to $40\,\mathrm{MHz}$. It is apparent that the mixer can be operated at very low LO amplitudes, and exhibits similar performances in both bands.
The frequency behavior can be further investigated with the graph in Figure 6.28: the RF frequency is swept at a constant LO amplitude of $0.15\,\mathrm{V}$ and downconverted to $40\,\mathrm{MHz}$. The conversion gain is reduced at higher frequencies, because of the effect of the capacitances at the LO port, but the circuit provides sufficient gain and linearity up to the maximum test frequency of $6.5\,\mathrm{GHz}$.
The graph in Figure 6.29 gives an example of the two-tone and large-signal tests performed: iIP_3 extrapolation is performed with a test RF frequency of $5.5\,\mathrm{GHz}$, whereas the large signal conversion gains for $\mathrm{P}_{1\,\mathrm{dB}}$ extrapolation correspond to $2.45\,\mathrm{GHz}$ and $5.5\,\mathrm{GHz}$ RF input signals.
An important advantage of the micromixer is that it is a doubly-balanced mixer with single-ended RF input: it suppresses both LO-to-IF and LO-to-RF feed-throughs. Figure 6.30 presents the on-wafer measurements of the two isolations. The most critical of the two is the LO-to-IF, because the LO signal can be amplified by the mixer-quad transistor, which act as common-emitter amplifiers. The measured isolation is sufficient, since the input LO signal is always around few hundreds of mV.

Conclusion

Table 6.7 resumes the experimental results. This mixer has been designed as first downconversion stage of the reconfigurable system described in §4.4.2. Although the low input impedance is difficult to drive with an LNA, the measured results confirm that this topology can provide the necessary broadband frequency response, conversion gain and linearity, with sufficient suppression of the unwanted LO feed-trough at the IF port.

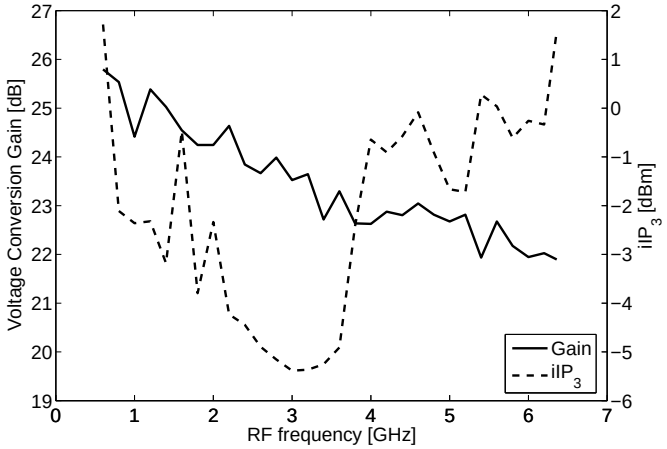


Figure 6.28: *Voltage conversion gain and iIP$_3$ as function of the RF frequency. IF is fixed at* $40\,\mathrm{MHz}$*, while an LO of* $0.15\,\mathrm{V}$ *sweeps frequency.*

Table 6.7: *Summary of experimental results for the Micromixer.*

RF band	$>1.5-6.5\,\mathrm{GHz}$
LO amplitude	$0.15\,\mathrm{V}$
Conv.Gain	$22-26\,\mathrm{dB}$
P_{1dB}	$>0\,\mathrm{dBm}$
iIP_3	$0\,\mathrm{dBm}$
LO - RF isolation	$>45\,\mathrm{dB}$
LO - IF isolation	$>15\,\mathrm{dB}$
Supply	$3.3\,\mathrm{V}$
Bias current	$2.1\,\mathrm{mA}$
Active area	$0.048\,\mathrm{mm}^2$

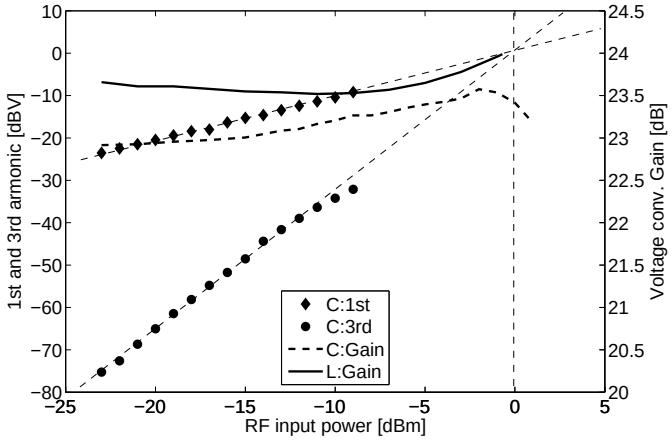


Figure 6.29: *iIP$_3$ extrapolation for an RF frequency at* $5.5\,\mathrm{GHz}$ *downconverted to* $40\,\mathrm{MHz}$ *with an LO amplitude of* $0.15\,\mathrm{V}$*. The large signal voltage conversion gain is shown for input frequencies at* $2.45\,\mathrm{GHz}$ *and* $5.5\,\mathrm{GHz}$*.*

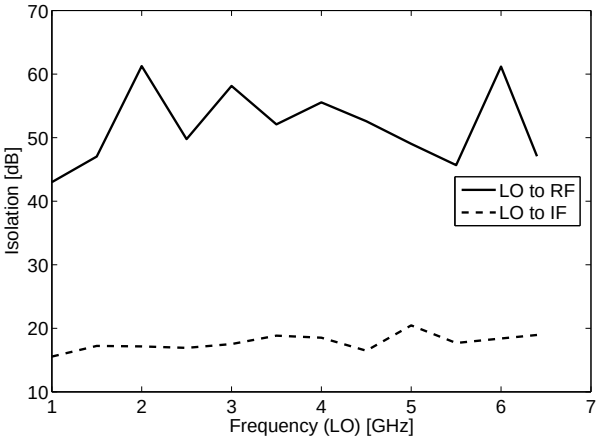


Figure 6.30: *Isolation of the LO signal at the IF and RF ports. The test was performed on wafer.*

6.4 Passive Mixers

An alternative approach for the implementation of the mixing principle depicted in Figure 6.1 in integrated circuit technologies is the use of actual switches. In many microwave applications, specially for very high frequencies, the switches can be implemented with diodes, which can provide the fastest switching performance. The diodes act as change-over switches, alternating the polarity of a differential RF signal on the IF load, while driven by a very large LO signal. The LO signal must significantly exceed the applied RF signal, as it can de-bias the diodes. This leads to very large currents flowing from the LO driver into the diodes, which are driven into deep forward bias.
In modern realizations of passive ring mixers, each diode can be replaced by a FET. This has as major advantage the reduction of LO current needed to drive the switches.

6.4.1 FET Ring Mixer

An array of four FET ring mixers was designed and fabricated in IBM BiCMOS 6HP technology, as part of a larger system presented in §8.1.3. The simple system architecture allows to de-embed the mixer RF figures of merit from the measurements, and they are presented in this paragraph.
Figure 6.31 shows the schematic of one of the mixers: four FET are connected in a ring configuration and are controlled as switches driven by a LO differential voltage at their gates. The differential RF signal is redirected to the IF load with the polarity alternated at the LO frequency. The gate DC voltage $V_b^{\pm}$ is controlled independently. This allows to reconfigure the circuit as *through* connection from RF to IF without frequency translation and negligible attenuation. This can be useful, as in the dual-band reconfigurable receiver presented in §4.4.2.
Figure 6.32 shows a detail of a chip where four FET-ring mixers are implemented. Each mixer occupies $7.7 \cdot 10^{-3}\,\mathrm{mm}^2$ of active area.
Figure 6.33 shows the behavior of conversion gain and linearity as function of the LO voltage amplitude at the test frequencies $2.75\,\mathrm{GHz}$ for RF input and $40\,\mathrm{MHz}$ for IF. The conversion gain reaches usable values only at LO amplitudes much larger than in active mixers presented in previous paragraphs of this chapter, including those with lossy polyphase filters at the LO port.

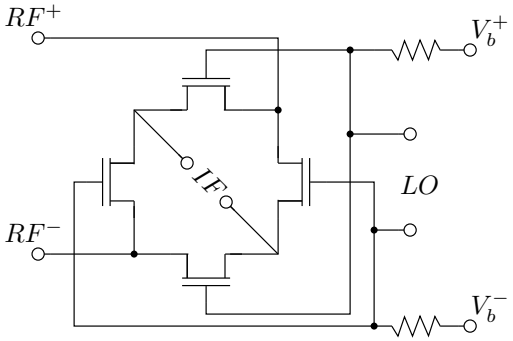


Figure 6.31: *Schematic of the doubly-balanced FET-ring passive mixer. Gate size is* $10 \times 5\,\mu\text{m} \times 240\,\text{nm}$.

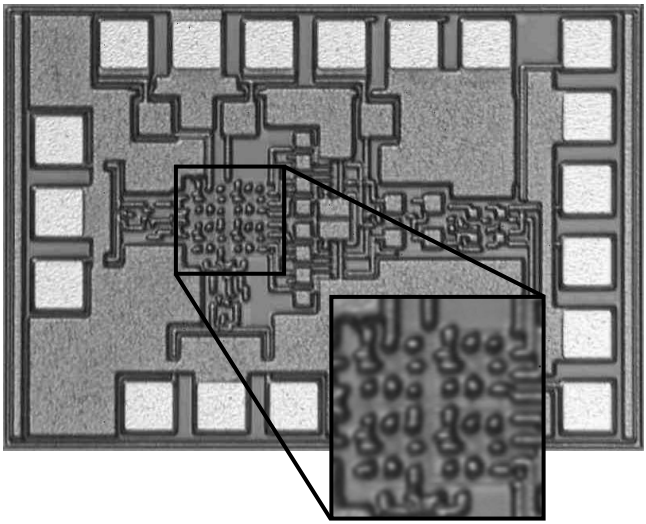


Figure 6.32: *Photograph of the passive FET ring mixer, integrated with three polyphase filters for test purposes. The four mixers shown occupy a chip area of* $180\,\mu\text{m} \times 170\,\mu\text{m}$.

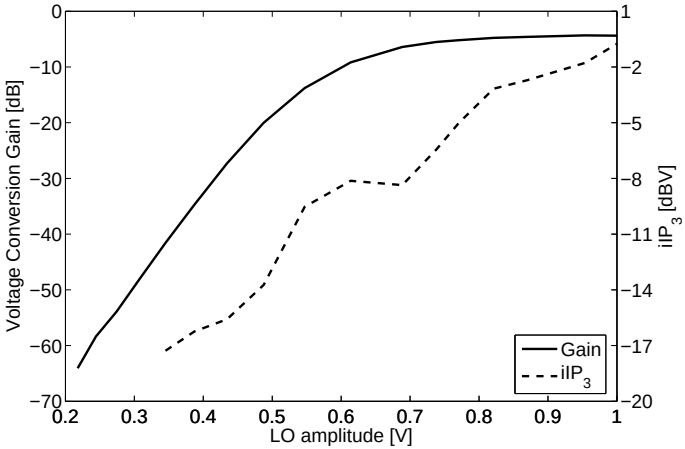


Figure 6.33: *Voltage conversion gain and iIP_3 versus LO voltage amplitude. IF is at* $40\,\mathrm{MHz}$ *and RF at* $2.75\,\mathrm{GHz}$*.*

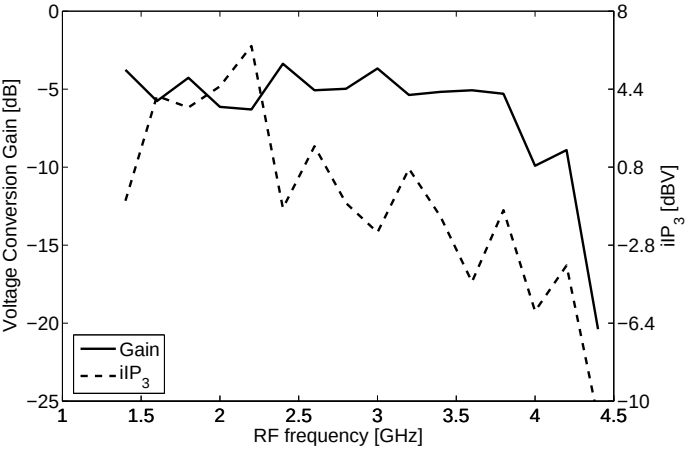


Figure 6.34: *Voltage conversion gain and iIP_3 versus RF frequency. IF is at* $40\,\mathrm{MHz}$ *and RF at* $2.75\,\mathrm{GHz}$*.*

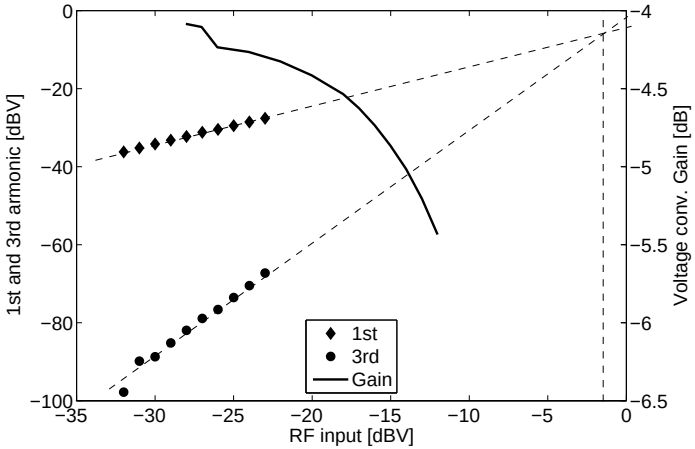


Figure 6.35: *Input-referred third-order intercept point extrapolation and large signal conversion gain. IF is* $40\,\mathrm{MHz}$ *and RF* $2.75\,\mathrm{GHz}$

The performance of this type of mixer depends on the gate DC bias: typical choice in CMOS implementations ($V_t \neq 0$) is to set the quiescent voltage of all the four gates to half of the FET threshold voltage V_t, as this allows to maximize the conversion gain.
This FET ring mixer does not have any resonant matching at its ports. This allows the mixer to operate in a broad frequency range, and reduces the area needed for circuit fabrication. The measured frequency response of this mixer is shown in Figure 6.34 at a fixed LO amplitude of $0.8\,\mathrm{V}$. For frequencies up to $4\,\mathrm{GHz}$ the mixer behavior does not show a significant frequency dependance. At higher frequencies the response could not be investigated, because limited by the low-pass response of the IF output stage integrated on the same chip, as presented in §8.1.3.
An example of the linearity behavior of the mixer is given in Figure 6.35, where $\mathrm{iIP_3}$ and $\mathrm{P_{1\,dB}}$ are extrapolated for an RF signal at $2.75\,\mathrm{GHz}$ and an IF of $40\,\mathrm{MHz}$.
The conversion loss of passive this mixer makes it unpractical as first down-conversion stage in RF front-ends: several active topologies can offer gain

up to $30\,\mathrm{dB}$ higher at lower LO amplitudes. The main advantage of the FET-ring mixer is its good linearity, which makes it particularly attractive as second mixing stage in double-downconversion receivers [13, 65, 66]. In this case, sufficient RF gain can already be provided by an LNA and a pair of active mixers, and the conversion loss of passive mixers becomes less critical for the system.

6.5 Summary

In this chapter, the design of downconversion mixers for integrated receivers has been presented. The mixers presented are divided in three categories: active singly-balanced, active doubly-balanced and passive. All mixers base their operation on the same principle, which is shortly described.

The design strategy adopted for the design of active mixers is described, underlining the correspondence between cascode amplifiers and active mixers.

Active mixers are suitable for single-downconversion monolithic receivers, both zero- and low-IF. The main advantage over passive alternatives is the capability of providing RF gain. The intrinsic conversion loss of passive mixers, typically worse than $5\,\mathrm{dB}$ in silicon technologies, makes them unsuited to follow directly the LNAs presented in §5. In fact, this would result in a total RF conversion gain of only $5-7\,\mathrm{dB}$. The use of active mixers allows to meet the conversion gain requirements presented in §2.

The main advantage of doubly-balanced active mixers over the singly-balanced ones is the rejection of the LO signal at the IF port. In some particular cases, e.g. the double-downconversion receivers (§4.4.1), the rejection of the large LO signal cannot be achieved by means of integrated capacitors. In the degenerated case of downconversion to baseband by means of two multiplications by the same LO signal [13], the first IF signal falls at the same LO frequency used for the first downconversion, and separation by filtering would be impossible. Two versions of doubly-balanced active mixers are presented, both based on the Gilbert mixer quad. The first offers a differential power- and noise-matched RF input, for noise optimization, whereas the latter, known as Micromixer, employs a bysimmetric class-AB

topology, which meets linearity requirements without inductors.

In simpler single-downconversion receivers, such as zero- and low-IF, the LO signal at the IF port can be rejected with integrated capacitors. In this case, the singly-balanced mixers allow to achieve the same conversion gain and linearity, consuming half of the bias current, from practically the same voltage supply. For this reason, singly balanced mixers have always been preferred in the integrated low-IF receivers presented in §8. Three examples of singly-balanced mixers are presented: two are designed for the receiver front-ends presented in §8.1.1 and §8.1.2, one is designed to meet the receiver front-end specification without pre-amplification.

Passive mixers offer higher linearity, combined with much lower conversion gains. The combination of these two features makes this type of mixer suitable for the second downconversion of double-downconversion architectures, such as the wideband-IF (§4.3.2). In fact, the combination of LNA and first downconversion mixers can provide $30\,\mathrm{dB}$ of gain, which make possible to tolerate the conversion loss and, on the other hand, tightens significantly the linearity requirements. A passive FET-ring mixer is presented, designed to be used in combination with the Micromixer in the system architecture presented in §4.4.2.

Chapter 7

Polyphase Filters

A polyphase signal is a set of N voltages (or currents) of the same frequency. Such voltages may be represented as vectors in the complex plane (phasors). In a symmetrical polyphase signal the vectors are equal in magnitude and spaced equally in phase. If, for example, a four-phase system is considered which has voltages of $V, +jV, -V, -jV$ applied to its four input terminals, then the input signal can be called symmetrical and of positive sequence.

This chapter summarizes the properties of the classic RC passive polyphase filters, their use with symmetrical signals for image rejection, the degenerate case of two-phase system for quadrature generation, and the design guidelines.
Polyphase filters are important building blocks of the monolithic receivers described in chapter 8. In fact, both the low-IF and direct conversion architectures described in chapter 4 need quadrature LO signals, and those are preferably generated on-chip. The low-IF architecture needs also appropriate combination of the IF quadrature signals, in order to provide image rejection.
Polyphase filters are networks able to provide both the mentioned functions and are suitable for low-cost monolithic integration, if the passive RC topology is chosen.

7.1 Principle of Operation

The amplitude attenuation and phase shift of a signal of frequency $f_{3\,\mathrm{dB}} = 1/2\pi RC$ fed into a low- or high-pass filter are indicated respectively in Figure 7.1(a) and Figure 7.1(b): at the cut-off frequency the two filters have equal amplitude response, but the phase is shifted by -45° and $+45^\circ$. This results in a total 90° phase difference, which could be, in principle, exploited for the generation of quadrature signals. In fact, assuming perfect match of the two resistors and capacitors, the phase shift is independent of the frequency. On the other hand, the amplitude is the same only at the $3\,\mathrm{dB}$ frequency, which can vary largely due to process tolerances. The issues on the amplitude can be partly solved using two limiting amplifiers: this can make the band larger and the sensitivity to tolerances more relaxed.
The RC passive polyphase filter [67] can be described as combination of singles stage RC low- and high-pass filters, and offers an alternative to the use of limiting amplifiers for quadrature generation. Figure 7.1(c) shows the schematic of a single stage filter. Each of the four input, when the remaining three are grounded, is connected to a low-pass and a high-pass RC filter. When a signal is fed to each of the input, it results in a $\pm 45^\circ$ phase shift to the corresponding output, according to the schematic of the connections. Since the circuit is linear, the response of each output can be described as the sum of the responses of each individual input, applied grounding the others. If a symmetric polyphase signal of frequency $f_{3\,\mathrm{dB}}$ is applied to the four input nodes, the amplitude of the four inputs is the same, and only the phase needs to be considered to describe the filter response. This is done in Table 7.1 for three typical polyphase signals: differential counterclockwise (positive) quadrature (2), differential clockwise (negative) quadrature (3), degenerated two-phase (1). It is apparent that the same RC network can generate quadrature differential signals from a single-phase differential signal (1) and reject the image of quadrature IF signals (2)-(3).

7.2 Input and Output Impedance

The input impedance of each of the four input nodes is, in principle, a function of the signal-source and load impedance. However, assuming them ideal, the impedance seen into each of the four input nodes is the shunt of

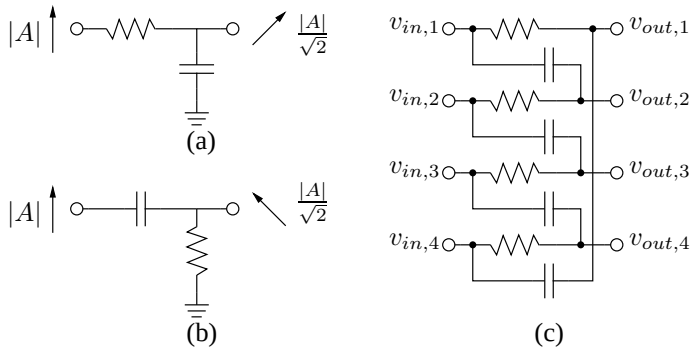


Figure 7.1: *An RC polyphase filter can be described as combination of RC high- and low-pass single-stage filters: (a) amplitude and phase response at cut-off frequency of a RC low-pass, (b) of a high-pass and (c) the schematic of a single stage polyphase filter.*

Table 7.1: *Input and output phases for three typical uses of a polyphase filter: (1) quadrature signal generation from a single-phase differential input; (2) pass-transfer of a pair of differential signals in counterclockwise quadrature (signal); (3) reject-transfer of a pair of differential signals in clockwise quadrature (image).*

input				*output*			
	(1)	(2)	(3)		(1)	(2)	(3)
$\angle v_{in,1}$	$\rightarrow$	$\uparrow$	$\uparrow$	$\angle v_{out,1}$	$\searrow\oplus\swarrow\equiv\downarrow$	$\nearrow\oplus\nearrow$	$\nearrow\oplus\swarrow$
$\angle v_{in,2}$	$\rightarrow$	$\leftarrow$	$\rightarrow$	$\angle v_{out,2}$	$\searrow\oplus\nearrow\equiv\rightarrow$	$\nwarrow\oplus\nwarrow$	$\nwarrow\oplus\searrow$
$\angle v_{in,3}$	$\leftarrow$	$\downarrow$	$\downarrow$	$\angle v_{out,3}$	$\nwarrow\oplus\nearrow\equiv\uparrow$	$\swarrow\oplus\swarrow$	$\swarrow\oplus\nearrow$
$\angle v_{in,4}$	$\leftarrow$	$\rightarrow$	$\leftarrow$	$\angle v_{out,4}$	$\nwarrow\oplus\swarrow\equiv\leftarrow$	$\searrow\oplus\searrow$	$\searrow\oplus\nwarrow$

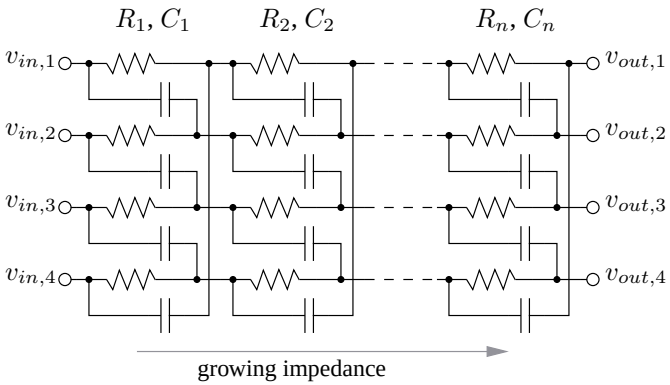


Figure 7.2: *Cascade of stages in a polyphase filter. Tapering the impedance in a multi-stage filter results in lower attenuation of the wanted signal.*

the impedances seen into a low- and a high-pass RC filter.
Similarly, the output impedance of each of the four output ports is the shunt of a resistor R and a capacitor C.
Those considerations are important when designing cascaded multi-stage polyphase filters: Figure 7.2 shows the typical connection of cascaded multi-stage filters. In order to achieve good voltage transfer from stage to stage it is sufficient to rise the value of the resistor. In the same way, the impedance level has to be lowered to drive properly the filter load [36].

7.3 Bandwidth

An ideal polyphase filter provides the phase combinations in Table 7.1 only at the $1/2\pi RC$ frequency. Away from this frequency the image rejection is weaker and the quadrature generation degrades. For the same reasons, quadrature generation is limited on a relatively narrow band.
If the filter has to operate over a wide band, then several stages in cascade must be used, as shown in Figure 7.2.
Figure 7.3 shows the effects of a cascade of stages on the quadrature generation as a function of frequency. As figure of merit for the quality of the

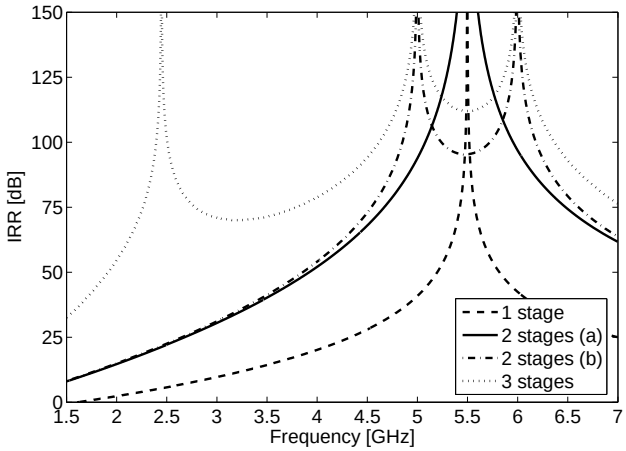


Figure 7.3: *Frequency response of multi-stage polyphase filters for broad- and multi-band quadrature generation. The behavior of an ideal single stage is compared with two dual-stage filters and one three-stage. In all of the cases, the first stage only is fed as in Table 7.1, column (1).*

quadrature, the achievable image rejection ratio was chosen, defined as

$$IRR \cong \frac{4}{\Delta^2 A + \Delta^2 \Phi} \tag{7.1}$$

where ΔA and $\Delta\Phi$ are the amplitude and phase deviation from perfect quadrature. The filter is employed as shown in Table 7.1, column (1), i.e. the input signal is single-phase differential and the two differential quadrature outputs are $v_I = v_{out,1} - v_{out,3}$ and $v_Q = v_{out,2} - v_{out,4}$. The bandwidth of the filter depends on the specifications on the tolerable amplitude and phase mismatch, and will correspond to a particular value of achievable IRR. Regardless the precise value required, it is apparent from visual inspection of Figure 7.3 that the band of a single stage polyphase filter is intrinsically narrow. Cascading two polyphase filters with the same $1/RC$ constants, case (a) in Figure 7.3, can lead to a significant improvement. The filter can be optimized by placing the $1/RC$ constants, according to the minimum rejection required at center band. In both cases the quadrature matching peaks

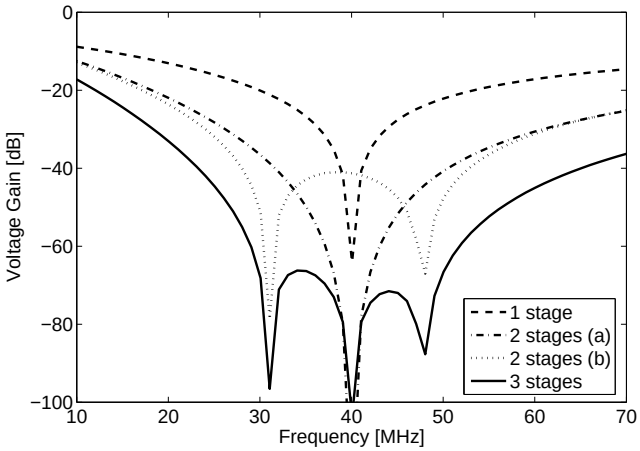


Figure 7.4: *Frequency response to the image frequency of multi-stage polyphase filters. The behavior of an ideal single stage is compared with two dual-stage filters and one three-stage.*

correspond exactly to the frequencies $f_i = 1/2\pi R_i C_i$. This characteristic can be exploited also for generating quadrature in discontinuous frequency intervals, as could be needed in multi-band applications. Figure 7.3 shows an example of three-stage filter, for the bands at $2.45\,\mathrm{GHz}$ and from $5\,\mathrm{GHz}$ to $6\,\mathrm{GHz}$. An example of the use of a similar filter for multi-band receivers is given in §8.2.

Cascading stages allows such bandwidth enhancement also on the IF side of the receiver, when using the polyphase filter for the combination of the I and Q signals, in order to provide image rejection. Figure 7.4 shows the image-frequency response of four filters, ranging from one to three stages. In this simulation, the input of the filter is always a quadrature differential signal as in Table 7.1, column (3), and the impedance level is increased using resistors $R_i = \{1\,\mathrm{k}\Omega,\ 3\,\mathrm{k}\Omega,\ 9\,\mathrm{k}\Omega\}$. This choice is necessary in order to minimize the voltage-signal loss for the positive quadrature (wanted signal), which is not attenuated by the filter. The number of stages and position of the notches can be determined according to the IF bandwidth and the required image-rejection ratio.

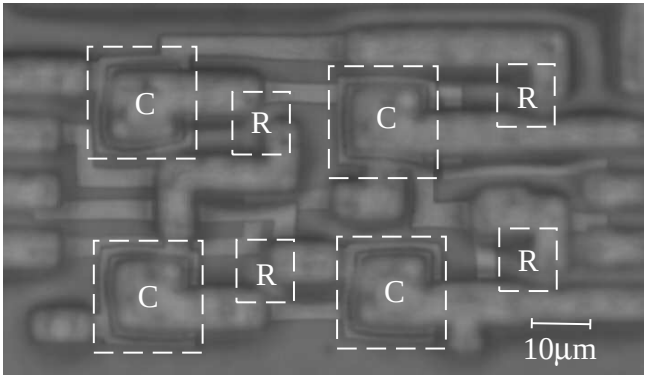


Figure 7.5: *Photograph of one stage of the polyphase filter used for LO quadrature generation for the receiver in §8.1.1. Area shown measures* $140\,\mu\text{m} \times 80\,\mu\text{m}$.

7.4 Process Tolerances and Layout Considerations

Polyphase filters are sensitive to process tolerances of the resistors and capacitors employed: mismatch in the transfer function of each branch of the polyphase filter means that the phasors representing the image signal will no longer cancel exactly. The use of components with large surface area [68] is a possible technique to minimize the variance of adjacent on-chip resistors and capacitors. While this can be easily done with resistors, it leads to large capacitances. Unfortunately, the range of usable values of capacitance and resistance is limited by other constrains, mostly related to the interaction among stages and with the other blocks of a system (§7.2). The strategy adopted for the filters in §8 is different: the values of capacitors and resistors are chosen to optimize the voltage transfer between system blocks, and the layout of each stage has been designed using a chessboard topology, with minimum distances between components of the same kind. Figure 7.5 shows the photograph of one stage of a polyphase filter used for quadrature generation in the receiver presented in §8.1.1. Although the circuit makes use of very small-area devices, it has proven to provide quadrature sufficient

for the IRR of $32\,\mathrm{dB}$ requested by the $5-6\,\mathrm{GHz}$ WLAN standards.
An other important effect related to the process tolerances is that the RC time constant may vary from run to run by $\pm 25\%$. Apparently, this cannot be compensated by any layout technique: the filter must be designed to null over the bandwidth of one channel with $\pm 25\%$ added as margin.

7.5 Summary

In this chapter the operating principle and design of passive RC polyphase filters have been presented.
A simple representation is used to explain the quadrature-generation and image-rejection capabilities of this type of network. Several simulations are used to describe the frequency behavior of the filter with respect to these two main functions. These results lead to practical design guidelines. In addition, the issues related to process tolerances are considered, and a layout strategy is proposed. This is validated by all the filters employed in the low-IF front-ends presented in §8.

Chapter 8

Monolithic Integrated Receivers

This chapter presents the integration of several receiver RF front-ends. The circuits described in the previous chapters are employed for low-power monolithic implementations of front-ends operating at $5\,\mathrm{GHz}$ and $2\,\mathrm{GHz}$, complying with WLAN specifications.
Two low-IF receivers meet the specifications for $5-6\,\mathrm{GHz}$, and a dual-band version allow operation also at $2.4\,\mathrm{GHz}$. All the circuits operate with very low power consumptions.
The results achieved validate experimentally the choices made for building blocks and architectures.

8.1 Single-Band Receivers

This first section of the chapter presents three single-band low-IF receivers. The first two are for the $5\,\mathrm{GHz}$ band and the second is designed for an RF band centered at $2.75\,\mathrm{GHz}$. This receiver was intended as second downconversion stage of the more complex dual-band system in §4.4.2.

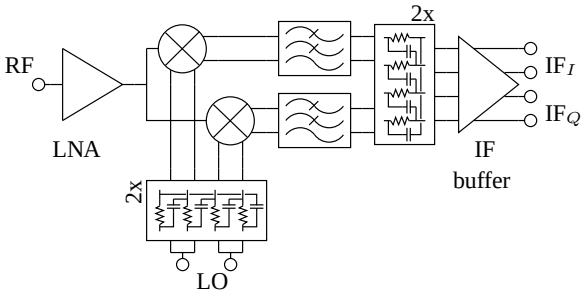


Figure 8.1: *Block diagram of the architecture of the implemented HBT low-IF receiver.*

8.1.1 HBT Low-IF Receiver

This paragraph presents a low-IF receiver [3,52] built by combining a power matched cascode amplifier (§5.5.2), two inductively degenerated singly-balanced mixers (§6.2.1) and two polyphase filters for LO quadrature generation and image rejection (§7). The system architecture is the same as described in §4.3.1, completed with an IF buffer (line driver) which simplifies the characterization in a $50\,\Omega$ environment. Figure 8.1 shows the system-level schematic of the circuit, fabricated in IBM BiCMOS 6HP technology.
For the LNA, a cascode was chosen due to its better output-to-input isolation and higher output impedance, which yields higher gain for a power consumption similar to the single-stage common emitter. The pre-amplifier was designed to provide about $14\,\mathrm{dB}$ of power gain and a NF of $2.6\,\mathrm{dB}$, with a current consumption of $2\,\mathrm{mA}$ from a $2\,\mathrm{V}$ supply. Direct on-wafer measurements of a test structure fabricated for this LNA are presented in §5.5.2 (page 58).
The topology chosen for the mixers is the active single-balanced mixer, described in §6.2.1, and shown in Figure 6.4 (page 81). The single-ended topology was preferred over the differential (§6.3), because it provides the same conversion gain for half the current consumption. The main drawback is the lack of isolation from the LO to the IF port: the large LO signal could saturate the following stage, but can be easily filtered by means of non-critical capacitors, shown in Figure 6.4 as C_{if}.
The mixer core consists of a pair of matched HBTs, whose bias current de-

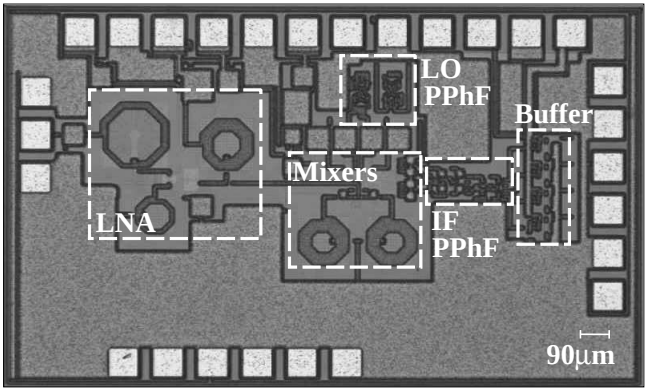


Figure 8.2: *Chip photograph of the HBT low-IF receiver. Area shown is* $2.14\,\mathrm{mm}\times1.32\,\mathrm{mm}$*; total active area, including the IF buffer, is* $1.05\,\mathrm{mm}^2$

termines the dynamic range of the whole mixer. In fact, for very low-power implementations, the transistors T_2 and T_3 limit the linearity of this circuit well before T_1. Transistor T_1 has to be inductively degenerated in order to reduce its transconductance and not to overdrive the mixer core. This does not necessarily imply a reduction of voltage gain, because low signal and bias currents allow the use of larger IF load impedances, which yield a high voltage conversion gain. As a consequence of the degeneration, the real part of the RF input impedance falls in the range of few hundreds of Ohms. Under this condition, the capacitor C is sufficient to provide power matching from the LNA output to the mixer input. The circuit was designed to provide $14\,\mathrm{dB}$ of voltage conversion gain, $P_{1\,\mathrm{dB}}$ of $-4\,\mathrm{dBm}$, with a current consumption of $2.5\,\mathrm{mA}$ from a $3\,\mathrm{V}$ supply.

Both IF and LO polyphase filters were designed with a cascade of two stages, exploiting the frequency behavior described in §7.3. For the IF filter, two stages are necessary to achieve sufficient IRR over the $20\,\mathrm{MHz}$ of IF bandwidth. In order to reduce signal voltage loss, the resistances increase toward the output [36]: from the mixer output impedance to the IF buffer input, each stage drives a higher impedance. The two stages of the LO filter are identical and ensure amplitude and phase balance of the quadrature sig-

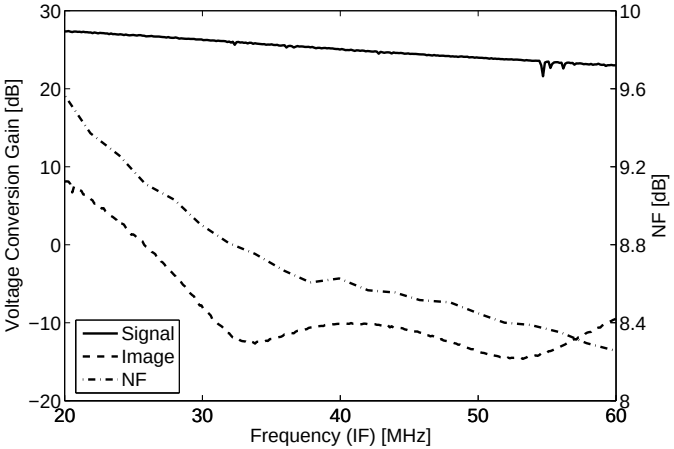


Figure 8.3: *Signal and image conversion gain for the downconverted second U-NII band, and corresponding noise figure, as a function of IF.*

nals over the $1\,\mathrm{GHz}$ LO tuning band.

Experimental results

The circuit was fabricated with the IBM BiCMOS 6HP technology, on a $1.05\,\mathrm{mm}^2$ active area, as show in the photograph in Figure 8.2. Total area measures $2.14\,\mathrm{mm}\times 1.32\,\mathrm{mm}$.
For characterization, the chip was mounted on a microstrip test board. The LO differential signal has been generated by means of a 180° microwave hybrid, IF differential output was converted to single ended using a power combiner. The presented results have been de-embedded from the effect of the chip test environment and the integrated IF buffer, which was characterized independently.
Table 8.1 summarizes the measured performance of the prototype over the three U-NII bands; DC power consumption is $19\,\mathrm{mW}$, and LO power is set to $2\,\mathrm{dBm}$. Figure 8.3 shows the measurement results of conversion gain, IRR and NF of the down-converted intermediate band. Figure 8.4 shows the

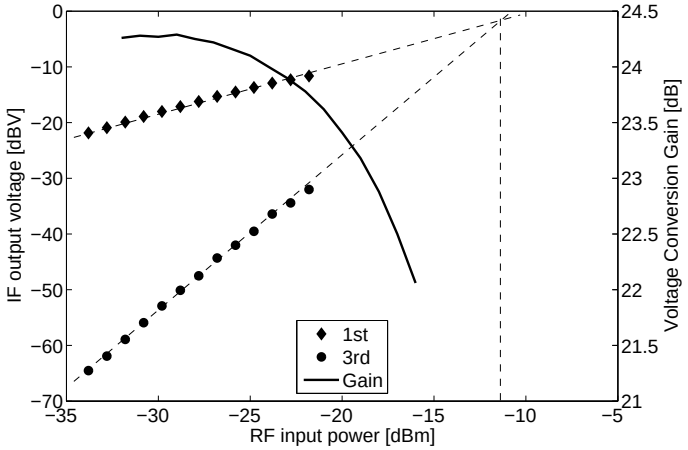


Figure 8.4: *Gain compression and iIP$_3$ for the downconversion of the second U-NII band.*

Table 8.1: *Summary of measured results for the HBT low-IF receiver.*

U-NII band	[GHz]	$5.15-5.25$	$5.25-5.35$	$5.725-5.875$
Conv. Gain	[dB]	25	25	22.5
IRR	[dB]	33	35	36.5
NF	[dB]	8.2	8.9	10.2
$P_{1\,dB}$	[dBm]	-19.1	-19	-18
iIP$_3$	[dBm]	-12.2	-12.5	-11.25
S_{11}	[dB]	<-9	<-10	<-14
LO to RF	[dB]	-64	-62	-57

large-signal gain ($P_{1\,\mathrm{dB}}$) and an iIP_3 extrapolation for the same band. Conversion gain, linearity, IRR and LO-to-RF isolation meets the WLAN specifications for $5\,\mathrm{GHz}$. The value of S_{11} in the lower band is higher than expected, but still acceptable. The NF is about $4\,\mathrm{dB}$ higher with respect to simulations; in particular, in the upper band, NF is $0.2\,\mathrm{dB}$ higher than specified for IEEE802.11a. This value still falls within the $5\,\mathrm{dB}$ implementation margin given by the standard definition (§2.1) [4, 5].

Conclusion

The measured results meet the specifications for the main two C-band standards, with the exception of the NF in the upper U-NII band, which is higher than requested, but still within an allowed implementation margin. Table 8.2 compares this work with the main C-band receivers published: in [52], this circuit has been presented as the first low-IF implementation reported with sufficient IRR values over all the three U-NII bands without external components. In the comparison of the power consumption it has to be taken into account that many works include an on chip LO generation: the current consumption of a local oscillator and a buffer suitable for this chip is estimated to be about $10\,\mathrm{mA}$.

Table 8.2: *Silicon C-band receiver state of the art, as published in [52].*

Process	Architecture	Bands	Gain [dB]	NF [dB]	iIP$_3$ [dBm]	Current/Voltage	IRR [dB]	Year	Ref.
Si Bipolar 25 GHz	Low-IF (75 MHz)	1-2-3	17	5.1	-4.5	23 mA/2.2 V (LO and quad)	Off chip	2000	[69]
BiCMOS 22 GHz	Superhet., two external filters	1-2	18	7 (DSB)	-17	18 mA/3 V	—	2000	[10]
CMOS 0.25 µm	DiCon (but IF @ 10 MHz)	1-2	18	3 (DSB)	-11.3	38 mA/3 V (LO and quad)	—	2000	[11]
Si Bipolar 47 GHz	Superhet. with external filter	1-2-3	14	6.9	-5.8	10 mA/1.8 V (LO and buff.)	36	2000	[50]
CMOS 0.24 µm	Low-IF or DiCon	2	12	5.2 (∼DSB)	-2	3.6 mA/2.5 V(?) (passive mix.)	12	2000	[12]
CMOS 0.25 µm	2×Superhet. (no ext. filters)	1-2	43	6.4	-15	11.6 mA/2.5 V	62	2001	[13]
CMOS 0.25 µm	Low-IF (Weaver)	1-2	26	7.2	-18	32.7 mA/1.8 V (LO and quad.)	50	2002	[14]
Si Bipolar 46 GHz	Superhet. several ext. comp.	∼1	24	3.2	-13	18 mA/3 V (LO and quad.)	35	2003	[15]
BiCMOS 45 GHz	DiCon	3	26.5	5.2	-17.4	23 mA/2.7 V	—	2003	[16]
BiCMOS6HP 47 GHz	DiCon	3	20.2	7.1 (DSB)	-3	31.2 mA/3.75 V	—	2003	[17]
BiCMOS6HP 47 GHz	Low-IF	1-2(-3)	25 (22.5)	8.9 (10.2)	-12	7 mA/3 V	33	—	This work

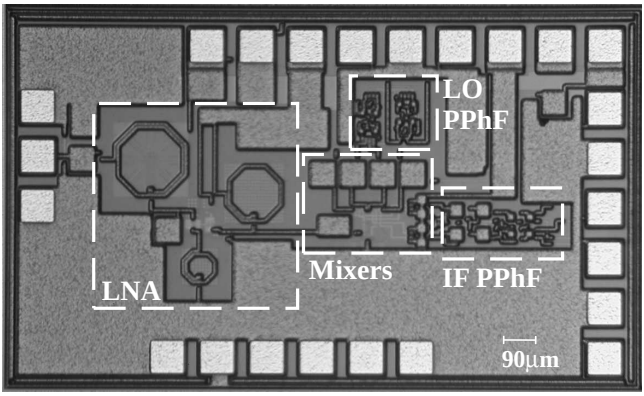


Figure 8.5: *Chip photograph of the BiCMOS low-IF receiver. Area shown measures* $1.916\,\mathrm{mm} \times 1.146\,\mathrm{mm}$*; the active area occupied by the circuit is* $0.48\,\mathrm{mm}^2$.

8.1.2 BiCMOS Low-IF Receiver

In order to further improve the power consumption and reduce the number of on-chip inductors, a second receiver based on the same system architecture of Figure 8.1 has been designed and fabricated. Targeting minimum power consumption, this second receiver comply with the IEEE802.11a standard only: this relaxes by $4\,\mathrm{dB}$ the gain-compression requirements with respect to the HiPerLAN2 standard (§2.3), and allows to save current in the active mixers.

As shown in §6.2.2, for a given bias current in the RF transconductance, the linearity performance of the singly-balanced mixer can be improved by implementing the transconductance with an nFET, which requires no inductive degeneration to accommodate the signal amplified by the LNA. The resulting input impedance of the RF port of this mixer is more suited for voltage matching with the LNA output port: the LNA load is a shunt inductor, which resonates at $5.5\,\mathrm{GHz}$ with the input capacities of the two mixers. The bandwidth of this resonator is determined by a shunt resistor, as described in in §5.3.2 for the power-matching equivalent. The input stage of the cascode LNA was designed for simultaneous noise and power matching to a $50\,\Omega$

Table 8.3: *Summary of measured results for the BiCMOS low-IF receiver.*

U-NII band	[GHz]	$5.15-5.25$	$5.25-5.35$	$5.725-5.875$
Conv. Gain	[dB]	31.4	31.4	28.7
IRR	[dB]	38.3	33.0	32.7
NF	[dB]	7.9	8.2	10.0
$P_{1\,dB}$	[dBm]	-24.1	-23.8	-21.6
iIP_3	[dBm]	-15.0	-14.1	-12.5
$\lvert S_{11}\rvert$	[dB]	-23	-24	-21

source (§5.1.1). This pre-amplifier was designed to provide about $15\,\mathrm{dB}$ of voltage gain on a high-impedance tuned load, a NF of $2.4\,\mathrm{dB}$, with a current consumption of $2\,\mathrm{mA}$ from the $2.4\,\mathrm{V}$ system supply.
The two BiCMOS mixers were designed to reach compression simultaneously with three main linearity limits on the corresponding BiCMOS cascode amplifier (§6.1.1): when the HBT common-base amplifier is fed with its maximum current signal, the common-source nFET receives the maximum voltage input, and the output peak-to-peak voltage at the HBT collector uses the full headroom. With this design strategy, a bias current of only $2\,\mathrm{mA}$ is sufficient to provide $18\,\mathrm{dB}$ of conversion gain and linearity. The IF load is the shunt of a resistor and a capacitor, which provides a sufficient reduction of the LO feedtrough. Details on the design values of the mixers are given in Table 6.3 (page 85).
The system is completed by two two-stage polyphase filters for LO generation and image suppression, similar to those in §8.1.1.
This version of the receiver does not include an on-chip IF buffer.

Experimental results

The receiver was implemented with the IBM BiCMOS 6HP technology on a $1.916\,\mathrm{mm}\times 1.146\,\mathrm{mm}$ chip: a photograph of the circuit is in Figure 8.5. The total active area is $0.48\,\mathrm{mm}^2$.
As for the other receiver presented, this chip was mounted on a microstrip

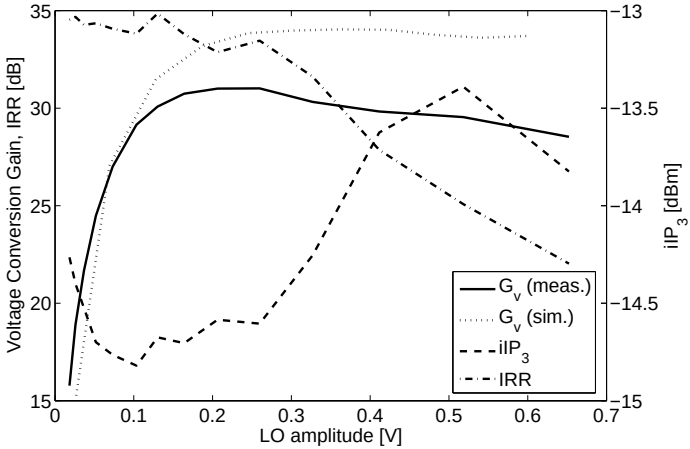


Figure 8.6: *Voltage conversion gain, image rejection ratio and iIP$_3$ as function of the LO amplitude.*

test board for characterization on a $50\,\Omega$ single-ended environment. Differential LO signal and single ended IF signal where generated by means of microwave hybrids, and the results presented here have been de-embedded from the effects of the test embodiment.
Figure 8.6 and Figure 8.7 show the behavior, at nominal bias point (I_{cc}=6 mA, V_{cc}=2.4 V), of voltage conversion gain, iIP$_3$, IRR and NF as a function of the LO voltage for a test RF frequency of $5.3\,\mathrm{GHz}$, corresponding to the center of the second U-NII band, and for an IF of $40\,\mathrm{MHz}$. Based on this test, and on similar results observed at the other two U-NII bands, an LO amplitude of $0.2\,\mathrm{V}$ has been chosen for the rest of characterization.
It is interesting to notice the behavior of the NF: at very low LO amplitudes, e.g. below $50-70\,\mathrm{mV}$, the noise figure is high due to the low conversion gain; for LO amplitudes above $0.1\,\mathrm{V}$ the conversion gain is sufficient and the NF improves significantly at larger LO levels. This confirms experimentally the qualitative considerations reported in §6.1.1: at low LO amplitudes the switching is imperfect, leading to both transistors of the pair simultaneously on for a non-negligible fraction of the LO period, and this increases

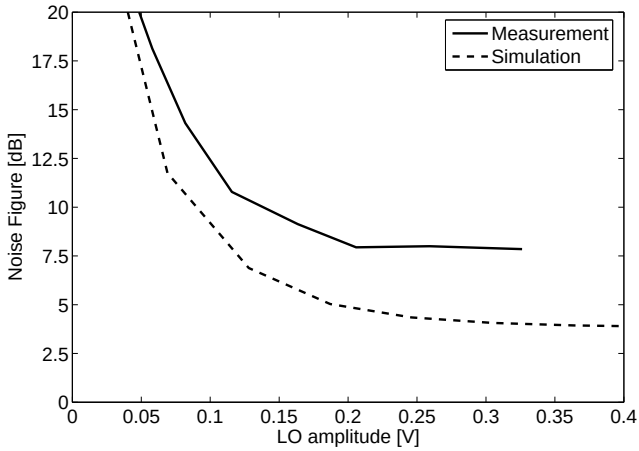


Figure 8.7: *Noise figure of the BiCMOS receiver vs. LO amplitudes.*

the mixer noise figure [34]. This effect is significant: it easily leads to an increase of NF of several dB, and it can be predicted with good accuracy employing the the available device models.
Figure 8.8 and Figure 8.9 display in detail the frequency response of the receiver: an RF signal is swept in frequency and downconverted to a fixed $40\,\mathrm{MHz}$ IF. The IRR is well centered on the $5-6\,\mathrm{GHz}$ target RF band; the conversion gain peaks at a lower frequency, with respect to the simulated values. This is due to some inaccuracy in the LNA load modelling, as indirectly confirmed by the behavior of the noise figure, which reaches its minimum exactly at the frequency of the conversion-gain peak. Still both gain and noise figure meet the specifications for the IEEE802.11a standard.
Figure 8.10 shows a detail of the voltage conversion gain versus IF for signal and image frequencies, together with the corresponding noise figure and its simulation. In Figure 8.11 the two-tone and large-signal tests allow the direct extrapolation of $\mathrm{iIP_3}$ and $\mathrm{P_{1\,dB}}$ for the $5.3\,\mathrm{GHz}$ U-NII band.
Finally, Table 8.3 resumes the performances of the receiver in the three bands of interest for the IEEE802.11a standard. Besides the underlined problems of the LNA load, which leads unavoidably to a larger NF, the receiver meets the specifications given in §2.1.

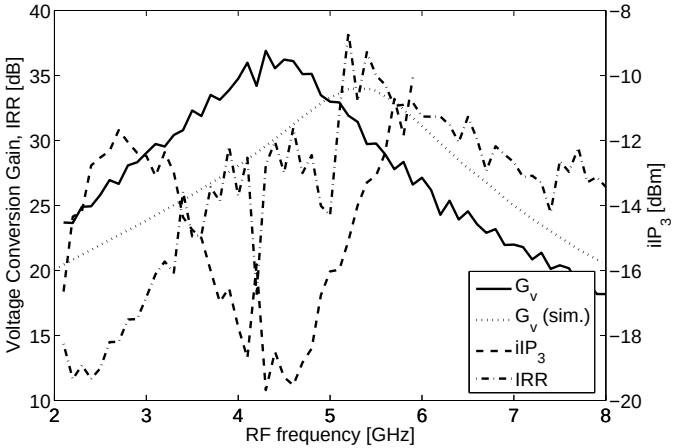


Figure 8.8: *Conversion gain, image rejection ratio and iIP_3 of the receiver for a RF input swept in frequency and downconverted to a fixed* $40\,\mathrm{MHz}$ *IF.*

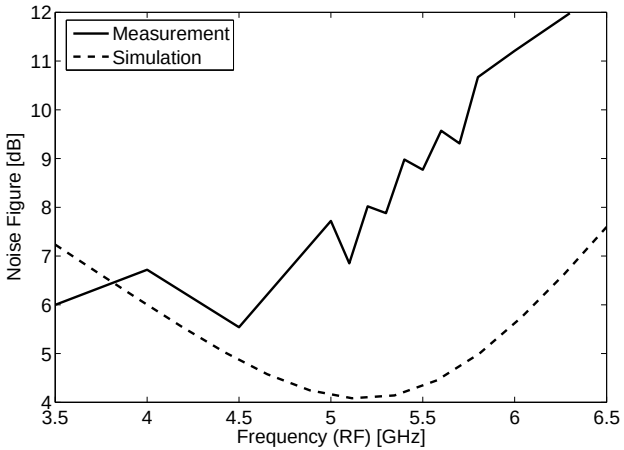


Figure 8.9: *Receiver NF as function of the RF frequency. The lowest values are reached at the same frequency as the LNA-gain maximum.*

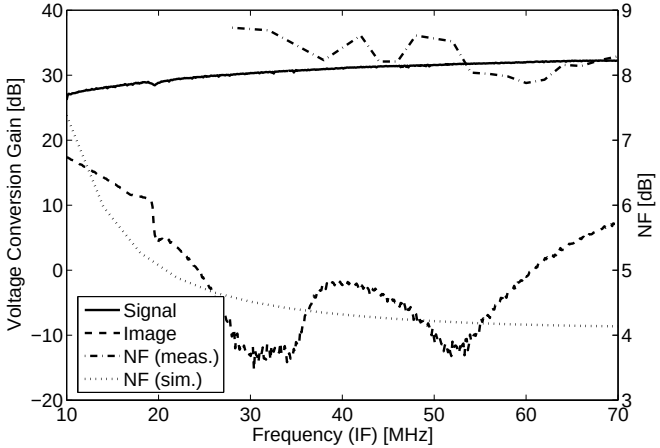


Figure 8.10: *Image rejection ratio of the downconverted second U-NII band, and corresponding noise figure.*

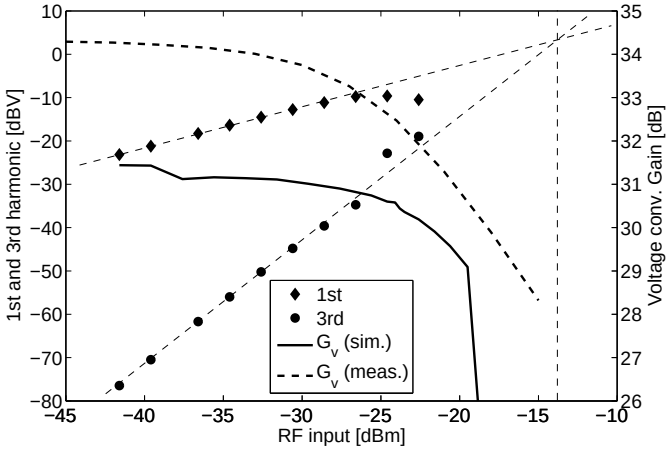


Figure 8.11: *Linearity test on the BiCMOS receiver for the RF input at* $5.3\,\mathrm{GHz}$.

Conclusion

The circuit presented in this paragraph is a second implementation of the architecture in Figure 8.1: the use of non-degenerated nFET as RF transconductance in the active mixers allows to reduce the circuit footprint. In comparison with the first version (§8.1.1), it has to be taken into account that the linearity specifications are $4\,\mathrm{dB}$ higher in that case: this explains the lower current consumption, which is not directly related to the mixer topology. Besides the reduced linearity, this circuit represents an improvement with respect to the first version in terms of active area, power consumption and overall RF performance.

8.1.3 Double Quadrature Low-IF Receiver

The second downconversion stage of the reconfigurable receiver described in §4.4.2 has been fabricated as a test structure. As part of the larger system, following a pair of matched Micromixers, its function is to perform the second downconversion of the $2.5-3\,\mathrm{GHz}$ when the $5-6\,\mathrm{GHz}$ band is received, or act as a through for the band at $2.45\,\mathrm{GHz}$. In the high-frequency mode, the sub-system is a double-quadrature receiver [36], because it combines RF and LO signals which are both already in quadrature. The main advantage of this downconversion architecture is that the image rejection depends only on the second-order components of the quadrature inaccuracy in the LO and RF signals, as the first-order errors are, ideally, cancelled by the recombination at IF [36, 70].

The architecture of the test chip is shown in Figure 8.12. It consist of three polyphase filters, four passive mixers (§4.4.2) and two IF adders. The single-stage LO and RF filters generate quadrature signals at about $2.75\,\mathrm{GHz}$. The IF filter is the same used for the other low-IF receivers of this chapter, and provides image rejection in the $30-50\,\mathrm{MHz}$ band.
The two differential IF adders have been implemented using the topology in Figure 8.13: the two input differential signals are converted to current-mode signals by means of two differential pairs, which act as transconductance. The current signals add linearly on the load resistors. This adder provides the same voltage gain as the corresponding single-input differential pair. For the purpose of this test, the performance of the adder is not of interest and the gain has been kept low: therefore, the adder does not limit the linearity of the whole system and allows indirect measurements of the linearity of the

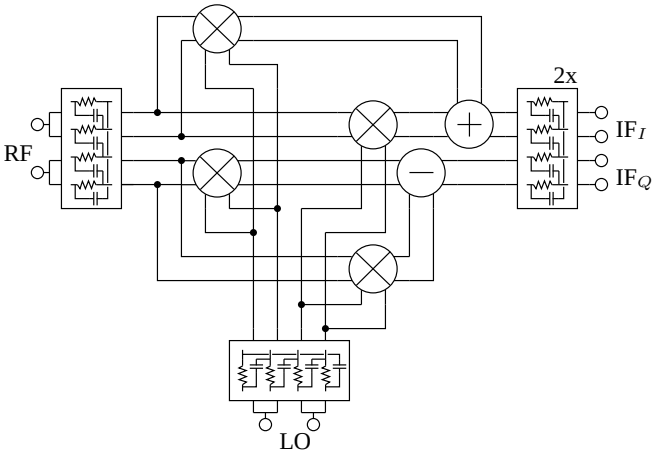


Figure 8.12: *Block diagram of the architecture of the implemented double-quadrature low-IF receiver.*

FET ring mixers, presented in §6.4.1. The nFET differential pairs are commonly the first stage of the IF circuits that follow the RF front-end and, as shown here, they are suited for adding or subtracting differential IF signals. The circuit was fabricated with IBM BiCMOS 6HP technology, on a $1323\,\mu\mathrm{m} \times 923\,\mu\mathrm{m}$ area, shown in Figure 6.32 (page 111). For characterization, the chip was mounted on a microstrip test board; differential signals have been generated by means of microwave hybrids and the results presented have been de-embedded from their effects.

Figure 8.14 shows the frequency response of the receiver for a fixed IF frequency of $40\,\mathrm{MHz}$. The absence of resonant structures in the RF and LO port allow the conversion gain and iIP$_3$ to be almost frequency independent in a large band. The gain observed is entirely due to the voltage gain of the IF adders. The adders set the upper limit of the operation frequency as well: the values of gain drop at about $4\,\mathrm{GHz}$, because of the frequency response of the differential pair, as measured directly when biasing the mixers in *through* mode. As shown by the simulation, the IRR is set at $40\,\mathrm{dB}$ by design, centered at $2.75\,\mathrm{GHz}$: the measured IRR values are higher than the specified $32\,\mathrm{dB}$ (§2) on a relative bandwidth larger than that of single-

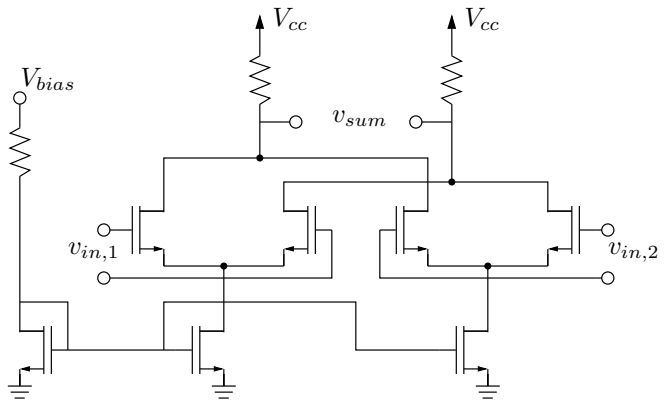


Figure 8.13: *Schematic of the IF differential adders used for the double quadrature receiver.*

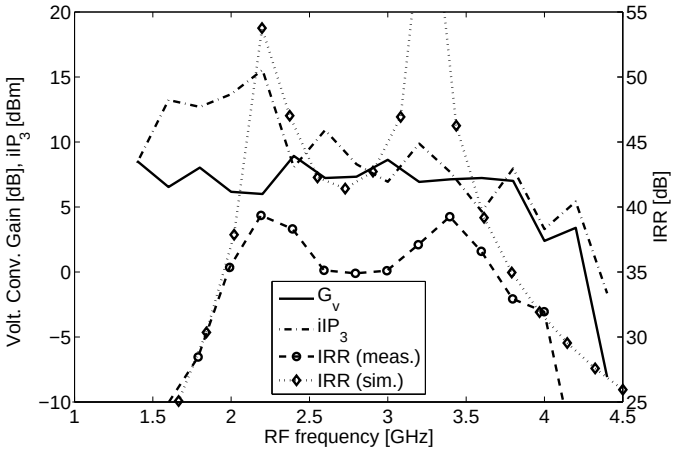


Figure 8.14: *Conversion gain, image rejection ratio and iIP_3 of the double quadrature receiver for a RF input swept in frequency and downconverted to a fixed* $40\,\mathrm{MHz}$ *IF.*

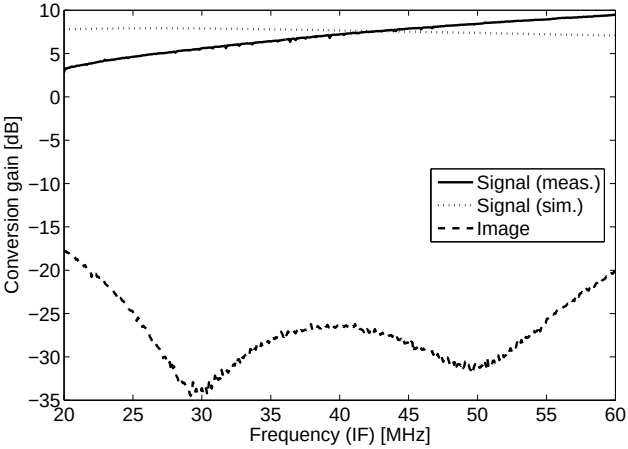


Figure 8.15: *Signal and image conversion gain of the double quadrature receiver as function of IF frequency: the RF input bands are centered at* $2.75\,\mathrm{GHz}$ *(signal) and at* $2.83\,\mathrm{GHz}$ *(image).*

quadrature receivers, shown in Figure 8.8 and Figure 8.19. This is due to the mentioned robustness of the double-quadrature architecture on quadrature imperfections.
Figure 8.15 shows a detail of the IF signals downconverted from the bands centered at $2.75\,\mathrm{GHz}$ (signal, measured and simulated) and at $2.83\,\mathrm{GHz}$ (image).
An extrapolation of iIP_3 and $\mathrm{P}_{1\,\mathrm{dB}}$ is shown in Figure 6.35 (page 113).

8.2 Dual-Band Receivers

The $2.45\,\mathrm{GHz}$ industrial scientific medical (ISM) band is presently the most used for wireless LAN applications, as a large number of access points are already installed and accessible. The migration to the $5-6\,\mathrm{GHz}$ unlicensed-national-information-infrastructure (U-NII) bands is desirable, because it would allow higher data rates, but it will necessarily result in a coexistence. This makes multi-band and multi-standard devices more attractive.

The issues of the design of such devices are often addressed by integrating several independent sets of RF front-ends [71, 72]. However, some of the blocks needed are inherently broadband and this feature can be exploited to reduce the overall number of components, dice area and cost [20, 73]. An example of this approach is given in §8.2.1.
An alternative architecture exploits the reconfigurability of switching mixers, as summarized in §4.4.2. Such a receiver could be implemented integrating the dual-band LNA in §5.5.4, the active mixers in §6.3.2 and the reconfigurable double-quadrature receiver in §8.1.3.

8.2.1 Single Downconversion Low-IF Dual-Band Receiver

This paragraph presents the low-power implementation of an architecture which makes use of the broadband frequency response of singly-balanced active mixers (§6.2.2) and multi-stage polyphase filters (§7) in low-IF multiband receivers [3, 74].
Figure 8.16 shows the block diagram of the receiver. It consists of a dual-input LNA and an image-rejecting mixer, which is in turn constituted of a pair of matched mixers and two polyphase filters. The LNA has two inputs: the one in use must be selected with an external control voltage. The amplified signal is fed through a switchless connection to the mixer pair and downconverted to a $40\,\mathrm{MHz}$ IF. The LO polyphase filter generates quadrature signals needed for both input bands, and image rejection over the $30-50\,\mathrm{MHz}$ band is provided by the IF polyphase filter.
Fig. 8.17 shows the schematic of the HBT cascode dual-band LNA. The two-input switched stage is designed as described in §5.4.1, and the load is a dual-band shunt resonator (§5.4.2). The emitter current of T_3 flows completely in T_1 or T_2, according to the position of the switch. When active, the two inputs are power and noise matched to a $50\,\Omega$ source. The collector load of T_3 is designed to provide, together with the mixer input capacities, a high impedance at both input bands, thus allowing a switchless connection to the following stage. The shunt resistor R_3 lowers the resonator quality factor to fulfill the bandwidth specifications. The LNA provides $20\,\mathrm{dB}$ and $18\,\mathrm{dB}$ of voltage gain for the $2\,\mathrm{GHz}$ and $5\,\mathrm{GHz}$ band respectively, with $1.6\,\mathrm{dB}$ and $2.1\,\mathrm{dB}$ noise figures, at current consumptions of $2.2\,\mathrm{mA}$ and $3.9\,\mathrm{mA}$ from a $2.4\,\mathrm{V}$ power supply.
The matched mixers are the same BiCMOS active singly-balanced used for the receiver in §8.1.2. The RF transconductance is implemented with a non-

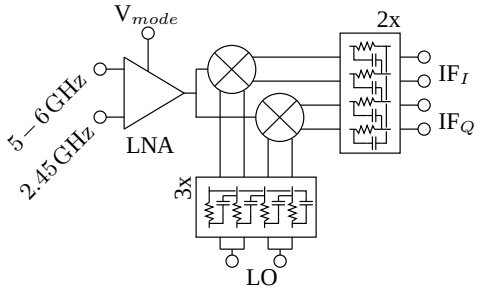


Figure 8.16: *Block diagram of the architecture of the dual-band low-IF receiver.*

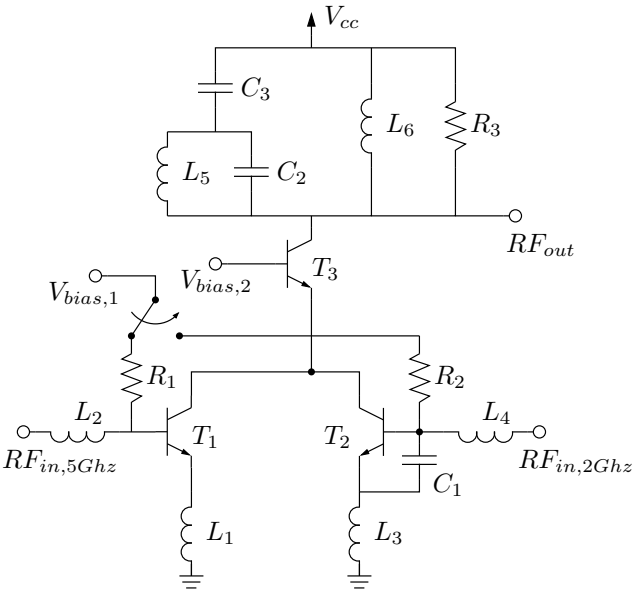


Figure 8.17: *Schematic of the dual-band LNA.*

degenerated common source nFET, whose input capacity resonates with the LNA load in the two operating bands, in order to offer a high impedance to the preamplifier. The mixer core is an HBT differential pair driven by the differential LO voltage; the LO port is not matched to any particular frequency, allowing the exploited broadband operating range. The IF load is a resistor in parallel with a capacitor. The resistor sets the conversion gain, the capacitor reduces the IF output bandwidth and the LO feed-through. Each mixer was designed to provide $16\,\mathrm{dB}$ of voltage conversion gain with a current consumption of $2\,\mathrm{mA}$ from the $2.4\,\mathrm{V}$ power supply.
The LO polyphase filter is the cascade of three passive RC stages. In order to provide amplitude balance and phase quadrature for both operation modes, the first stage has its cut-off frequency in the $2\,\mathrm{GHz}$ band, and the last two in the $5\,\mathrm{GHz}$ band: the frequency response of the series of the three stages can offer sufficient amplitude and phase balance in both operating bands (§7.3). The IF polyphase filter is the cascade of two stages, in order to achieve IRR over the $20\,\mathrm{MHz}$ bandwidth required for the main WLAN standards.

Experimental results

The circuit was fabricated in the IBM BiCMOS 6HP technology. A photograph of the circuit, implemented on a $0.73\,\mathrm{mm}^2$ active area, is shown in Figure 8.18. Total chip area measures $1.79\,\mathrm{mm}\times 1.29\,\mathrm{mm}$.
Figure 8.19 shows the measured frequency behavior of conversion gain, image-rejection ratio and iIP_3 for a swept RF and a fixed IF of $40\,\mathrm{MHz}$: the circuit is operated in low-frequency mode for frequencies up to $3.4\,\mathrm{GHz}$, in high-frequency mode otherwise. Both conversion gain and IRR show dual-band response: the two conversion gain peaks are due to the double resonance of the LNA load, and the IRR values are the result of the quadrature LO signals generated on chip by the LO polyphase filter. The comparison of the measured conversion gain with the simulation shows that, for both operation modes, the gain peaks are slightly out of band and lower than expected.
Figure 8.20 shows the frequency behavior, measured and simulated, of the input matching for the two input ports in the corresponding operating mode. Figure 8.21 and Figure 8.22 show in greater detail the measurement results for the $2.45\,\mathrm{GHz}$ band: in Figure 8.21 NF, signal and image conversion gain,

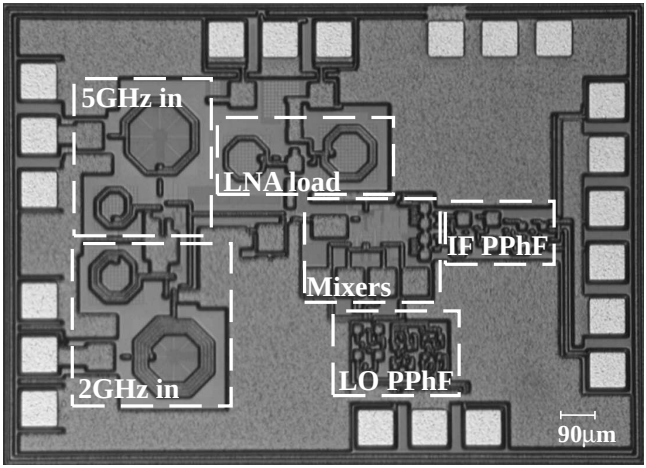


Figure 8.18: *Chip microphotograph of the dual-band image-reject receiver. Area shown measures* $1.79\,\mathrm{mm} \times 1.29\,\mathrm{mm}$.

Table 8.4: *Summary of measured results for the dual-band low-IF receiver*

RF band	[GHz]	2.45	5.2	5.3	5.775
Conv. Gain	[dB]	33.4	27.0	26.5	24.5
IRR	[dB]	43.3	31.9	36.7	30.8
NF	[dB]	4.1	8.6	8.6	10.1
$P_{1\,dB}$	[dBm]	-26.0	-19.0	-19.3	-16.7
iIP_3	[dBm]	-16.6	-11.6	-11.0	-9.3
S_{11}	[dB]	<-17.5	<-18.0	<-16.0	<-18.0
LO	[dBm]	0.8	2.5	2.4	2.4
LO to RF	[dB]	62.8	63.5	67.4	54.4

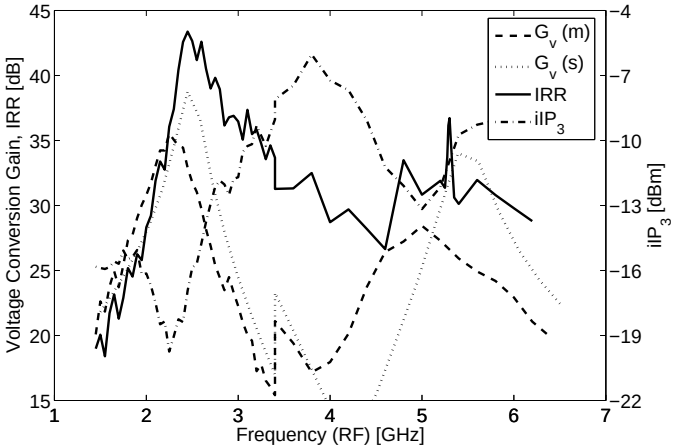


Figure 8.19: *Conversion gain, image rejection ratio and iIP_3 of the receiver. The circuit is operated in mode "low" below* $3.4\,\mathrm{GHz}$ *and mode "high" above that. LO power levels are* $0.8\,\mathrm{dBm}$ *and* $2.4\,\mathrm{dBm}$ *respectivley.*

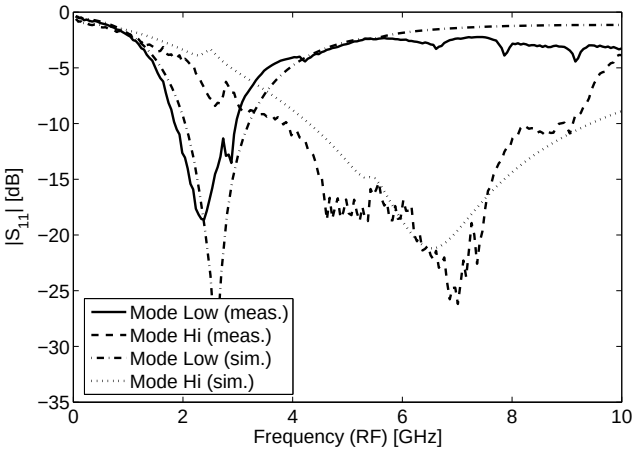


Figure 8.20: *Input matching of the two RF ports.*

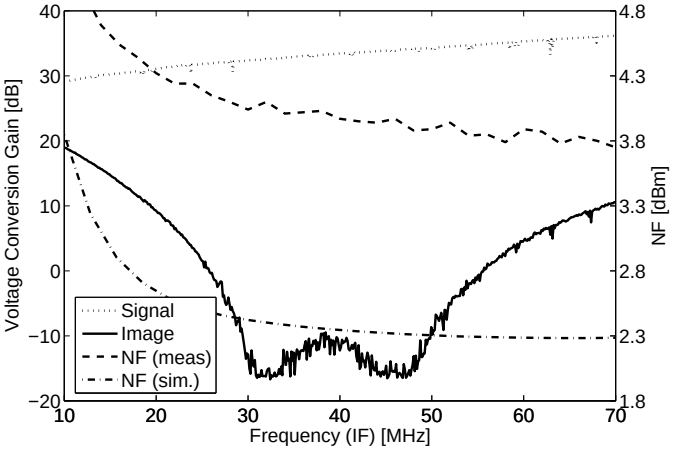


Figure 8.21: *Voltage conversion gain and NF for the* $2\,\mathrm{GHz}$ *band.*

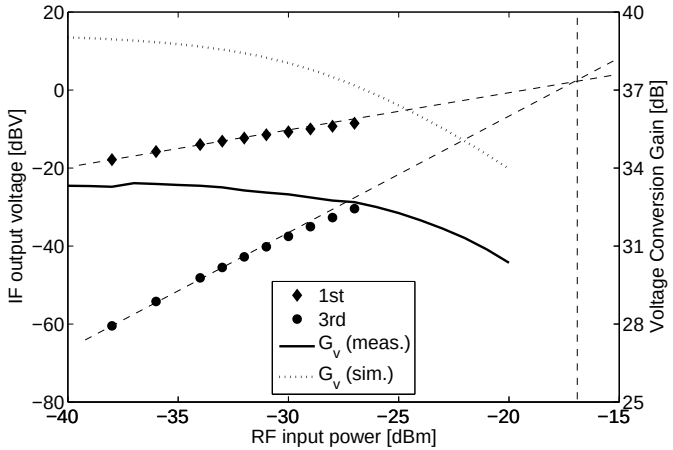


Figure 8.22: *iIP*$_3$ *and* $P_{1\,\mathrm{dB}}$ *in the* $2\,\mathrm{GHz}$ *band.*

and in Figure 8.22 $P_{1\,\mathrm{dB}}$ and iIP_3 extrapolation are shown.
Table 8.4 summarizes the measured performances of the prototype over the $2\,\mathrm{GHz}$ ISM band and the three $5\,\mathrm{GHz}$ U-NII bands. Power consumption is $14.9\,\mathrm{mW}$ for the low frequency mode and $18.7\,\mathrm{mW}$ for the high frequency mode. Performances are satisfactory in the $2\,\mathrm{GHz}$ mode, but suffer of some degradation of NF in the $5\,\mathrm{GHz}$ mode. This is partly due to an inaccuracy in the LNA double-band load modelling, which peaks at $5\,\mathrm{GHz}$ instead of $5.5\,\mathrm{GHz}$ as simulated, and test-board inductive parasitics on the ground connections, which are more critical in the high-frequency operation.
The IRR measurements in the high-frequency range are probably affected by test board parasitics as well. These result in unwanted coupling and worsen the observed results. The values shown in Fig. 8.19 and Table 8.4 can be considered as worst-case estimations.

Conclusion

The BiCMOS low-power dual-band RF front-end shows multi-band functionalities, confirming the validity of the chosen architecture. The measured performances are close to the specifications for the RF front-end of receivers compliant with IEEE WLAN standards at $2\,\mathrm{GHz}$ [23] and $5\,\mathrm{GHz}$ [52]. Without external components and very low DC power, this chip provides a good basis for the realization of WLAN low-cost receivers for dual-band operation.

8.3 Summary

This chapter presented fabrication and characterization of several monolithic receiver RF front-ends. The design of those circuits was based on the considerations and results described in all the previous chapters.

Two single-band low-IF receivers are presented in §8.1.1 and §8.1.2, both integrating a cascode LNA with two singly-balanced mixers and two polyphase filters. The front-ends meet the specifications for the $5\,\mathrm{GHz}$ standards. The two circuits show similar performances, but the BiCMOS version, which uses non-degenerated nFETs as transconductance for the active mixers, employs less integrated inductors, thus allowing a significant reduction of chip area. Power and voltage matching are used at the RF mixer port of, respectively, the HBT and BiCMOS versions. As anticipated in §5.3.1, this choice does not lead to a significant difference in terms of RF performance of the monolithic front-end.

A dual-band receiver extends the idea used for the single-band BiCMOS version. A dual-band load for the LNA is used in combination with broadband singly-balanced mixers and a dual-band LO polyphase filter. Without external components, this front-end meets the specifications for IEEE wireless LAN standards at in the $2\,\mathrm{GHz}$ and $5\,\mathrm{GHz}$ bands. The front-end operates in the same DC-power range as the single-ended versions, and achieve similar performances in the high-frequency operation.

Those circuits demonstrate that sufficient IRR can be achieved without external components at $5\,\mathrm{GHz}$, even in more complex dual-band architectures.

In addition, a double-downconversion low-IF receiver was fabricated. This circuit can serve as reconfigurable *downconversion-through* stage of the front-end described in §4.4.2. The operation frequency was selected to allow receiving the $5\,\mathrm{GHz}$ band with two successive multiplication by the same LO signal. The circuit exhibit a large IRR relative bandwidth, resulting from the good tolerance of double-quadrature receivers for I- and Q-signal asymmetries.

Chapter 9

Conclusion

A study of the design of the RF front-ends for receivers compliant with the WLAN standards has been presented in this thesis. As motivated in §1, the focus is on low-power monolithic BiCMOS implementations, compliant with the IEEE standards at $5-6\,\mathrm{GHz}$, and dual-band extensions to $2.4\,\mathrm{GHz}$.

The characteristics of the main standards ratified in both bands are reviewed in §2. For each standard, the specifications for the RF front-end are derived, since typically those are not explicit in the system-level specifications. The resulting requirements for the RF front-end, resumed in Table 2.2, have been used as target for the design of the receivers and the building blocks.

An overview of receiver architectures is given in §4. Since the superheterodyne receiver is not suitable for integration, the advantages and disadvantages of two alternatives, direct-conversion and low-IF receiver, are discussed. It is underlined that the two architectures are both suitable for monolithic integration, similar in many aspects, and share several issues. The main difficulty in integrating low-IF receivers comes from the tight requirements for the symmetry of I and Q signals, necessary to provide sufficient rejection of the image signal. The circuits in §6.2.3, §8.1.1, §8.1.2 and §8.2.1 demonstrates that sufficient IRR can be achieved at $5-6\,\mathrm{GHz}$. With respect to other aspects, low-IF receivers are less sensitive to some of the typical problems affecting DiCon receivers. For example, the lower sensi-

tivity to second-order distortions simplify the use of single-ended building blocks. Concerning the design of individual building blocks of the system, the differences between the two architectures are minimal, since all the major issues need to be handled at a system level.

The study of the design of the receiver, including prototype fabrication and characterization, has been conducted using two commercial RF BiCMOS technologies from IBM, and the corresponding design kits. The main features of those two technologies are summarized in §3.

The design approach for the low-noise amplifier is described in §5. Several possibilities are presented and discussed for the amplifier topology and the matching of input and output ports. The cascode configuration is argued as most convenient for monolithic low-power receivers, since, for a given current consumption, it provides higher gain than single stage common-emitter amplifiers. For the input matching, a design procedure is described in detail, which allows simultaneous noise and power matching to real impedances, such as the $50\,\Omega$ of commercial antenna filters. Several possibilities are presented for the output matching, including a tunable power matching, which allows to extend the usable bandwidth of the amplifier. In addition, several modifications of the presented matching schemes are presented, in order to allow dual-band operation in different configurations, such as single or double input ports, voltage or power matching to the following stage.

Downconversion mixers are presented in §6. The focus is on active mixers, since passive mixers usually suffer of strong conversion attenuations in silicon-based implementations. This makes them unsuited as first downconversion stage of simple receiver front-ends. The design approach chosen for active mixers is described, and several design examples are given. Exploiting the advanced performance offered by the IBM BiCMOS 7HP technology, and combining the design approaches described in §5.1.1 and §6.1.1 a merged LNA and mixer demonstrates that the RF front-end of a WLAN receiver compliant with the IEEE802.11a/h standards can consume as little power as $7\,\mathrm{mW}$.

Polyphase filters have been used extensively for LO quadrature generation and recombination of the I and Q IF signals. The operating principles

of these networks are summarized in §7, together with the adopted design approach.

The monolithic RF front-ends are presented in §8. In this chapter, the choices made for the various building blocks and architectures are validated experimentally. Two low-IF receivers meet the specifications for $5-6\,\mathrm{GHz}$, and a dual-band version allow operation also at $2.4\,\mathrm{GHz}$. All the circuits operate with very low power consumptions. In addition, a $2\,\mathrm{GHz}$ receiver is presented as second downconversion stage of a reconfigurable dual-band receiver.

The work presented demonstrates that monolithic low-IF receivers can be implemented with the available BiCMOS technologies at competitive power levels. State-of-the-art performances have been reached with several of the fabricated circuits:

- the merged LNA and mixer in §6.2.3 [2] offers a remarkably high gain-to-power-consumption ratio and, at the same time, can serve as RF front-end of a $5\,\mathrm{GHz}$ receiver without preamplification
- the receiver in §8.1.1 has been presented as the first monolithic low-IF receiver covering all the three U-NII bands at $5\,\mathrm{GHz}$ [52]; it compares favorably also with similar implementations in narrower bands
- the receiver in §8.1.2 further reduces the power consumption of the latter, employing nFETs for the RF transconductance of active mixers, and relaxing the linearity specification
- the dual-band receiver in §8.2.1 [74] demonstrates that, with a minimum increase of power consumption, the receiver operation can be extended to a second band

9.1 Outlook

The circuits presented are examples of monolithic receiver front-ends in BiCMOS technologies. The first step in completing this work would be the integration of an adequate VCO on the same chip as the presented front-ends.

From a more general point of view, the need for a high level of integration motivates the design effort for monolithic implementations of much larger systems. The entire transceiver, i.e. receiver, transmitter and digital circuitry, can be fabricated on the same chip. In some cases, due to the large losses of silicon substrates and low breakdown voltage of available devices, only the power amplifier is realized on a separate chip. However, it has been recently demonstrated [75] that switched-mode power amplifiers are a highly efficient solution for the integration of power amplifiers in compact silicon chips at $5\,\mathrm{GHz}$, and are able to deliver power at levels close to the maximum allowed in the wireless LAN bands (Table 2.1). This is an important result, as it shows that a complete WLAN system-on-chip can be integrated in BiCMOS technologies. In this context, the antenna switch, which directs the input and output signals to the LNA or the PA, is a critical component to integrate. A distributed switch is one of the possible solutions, compatible with the available technologies [76].

Another major issue that arises from the integration of a complete system on a single chip is the interaction of the RF front-end with the noisy digital circuits. This is particularly troublesome on a silicon substrate, due to its limited isolation capabilities. The mixed-signal technologies, including the IBM BiCMOS 6HP and IBM BiCMOS 7HP , offer means to improve the poor isolation of silicon substrates. Deep trench barriers can be used to increase the resistance between critical points, or substrate-contact rings around particularly sensitive devices, in order to ground the noise carriers travelling on the substrate. These effects are, however, extremely difficult to simulate or predict, and require experimental investigations.

Several possibilities can be explored for improvements in the dual-band version of the receiver. For example, the size of the circuit presented in §8.2.1 can be reduced modifying the input and output matching of the the LNA. At the input, a dual-band matching (§5.4.1) can be used to save one inductor and significantly reduce the size of the $2\,\mathrm{GHz}$ series inductor. At the output, a tunable voltage matching (§5.3.2) can be designed to cover the broadband range $2.4 - 6\,\mathrm{GHz}$; this requires an array of varactors, but allows to use only one small inductor.

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Curriculum Vitæ

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