A radio frequency source for the preparation of quantum states

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A Radio Frequency Source for the Preparation of Quantum States

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Abstract

The present Diploma thesis was motivated by the need for a versatile radio frequency source to be used in experiments with cold atoms. The working principles and the design of said source are presented including its characterization and an example of its evaluation in an experiment.

The desired experimental uses impose a set of strict requirements on the design such as highly stable output phase and frequency as well as reproducible and precisely controllable profiles of phase, frequency and output power. The device developed in this thesis features output frequencies from 5 MHz up to 500 MHz, phase-continuous operation, fast linear frequency sweeps with very small frequency jumps, phase synchronized output of two frequencies and arbitrary sweep profiles with update rates of up to 8 kHz. All parameter and profile controls can be accessed and adjusted using a graphical user interface that is integrated into the experiment control framework.

Validating the features experimentally, Rubidium Bose-Einstein condensates were transported over distances of a few centimeters in a moving interference pattern of two counterpropagating laser beams. The frequency difference of the laser beams was controlled by the device, permitting precise and reproducible positioning of the atoms. Further possible applications include generation of radio frequency sweeps to drive Landau-Zener transitions or generation of Ramsey type pulses. The required precise control of timing and phase of multiple pulses is achievable with the present design approach.
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Chapter 1

Introduction and Overview

Atom physics has been approaching regimes of ever increasing control over quantum mechanical states of matter. The ability to prepare and probe samples close to the absolute zero of temperature as well as to control quantum mechanical processes permits testing physical models in the extreme parameter ranges where effects and behavior become relevant that are not apparent under normal conditions.

A prime example for a state that can be realized at low temperatures is the motional ground state of neutral bosonic atoms which form a Bose-Einstein condensate (BEC) [1, 2]. At the extremely low temperatures reached with a BEC the behavior of the atoms is strongly non-classical and governed by the effects of quantum mechanics.

Cold atoms are a very suitable system to test phenomena seen in solid state physics. When subjected to periodic potentials the atoms form crystal-like structures. Those periodic potentials are realized by light waves forming lattices of spatially varying light intensity which induce a dipole potential. The atoms are captured in the lattice and can then be brought into regimes such as the Mott insulating phase [3] by varying the potential. Lattices also serve well to study cold fermions [4].

In recent years novel regimes have been realized such as molecular states of fermionic atoms [5, 6] which form a superfluid phase under certain conditions [7]. For those molecules the preparation and understanding of the internal state of the molecules is of great interest.

In order to reach the low temperatures necessary to obtain cold atoms, transitions between certain quantum mechanical states such as hyperfine states or Zeeman sublevels are induced. The transitions are used to evaporatively cool down to Bose-Einstein condensation or to bring the condensate into states that differ in their interaction with magnetostatic, electrostatic or electromagnetic fields.

Some of these transition processes become very selective in energy—and equivalently in the associated frequency—requiring precise frequency sources to drive them on one hand but on the other allowing to determine the involved frequencies up to an extremely high degree of precision. Spectroscopy with cold atoms provides frequency and time standards of unprecedented accuracy [8].
Radio frequencies (RF) play a key role as a manipulative tool in the techniques mentioned above. Their use is not limited to processes that directly involve an electromagnetic wave in the radio frequency range. RF can also be used in combination with other electromagnetic radiation in the microwave or optical frequency range to drive multi-photon processes. Another common technique is to send laser light through a modulator in which a radio frequency modulates optical parameters. The modulation creates sidebands on the laser's frequency or diffraction orders that have the sum or the difference of the light frequency and the RF frequency. Those sidebands or diffraction orders can then easily be tuned without having to detune the laser source itself. Light of precisely adjustable frequency or two beams with controllable difference frequency are obtainable this way. Examples of these manipulative techniques are given in the following chapter (chapter 2).

Using radio frequencies to prepare quantum states implies a set of requirements that a frequency source has to fulfill in order to be experimentally useful and versatile.

- Keeping in mind the possibly very narrow lines of the transitions between states, the frequency has to be locked onto a suitably stable reference source. A very good reference is obtainable from the global positioning system’s (GPS) satellites. Professional GPS receivers provide a 10 MHz reference clock output which is long-term stabilized onto the GPS system and short-term stabilized by a voltage controlled and temperature regulated crystal oscillator. The locking onto the reference clock has to be not only on a frequency level but also deterministic on the phase level since precise control of the phase of the output of the frequency source relative to the reference (and thus relative to the rest of the experiment) may be necessary.

- If short RF pulses, so-called $\pi$ or $\pi/2$ pulses, are employed for state preparation, not only the frequency but also the length of the pulse determines the final state. This makes precise timing—in start and duration—of the pulses a requirement.

- Many spectroscopic methods involve multiple short pulses with characteristic timings and relative phases. To generate these, a frequency source with a phase that is continuous in time and has an adjustable phase offset is needed.

- When used in the generation of a moving optical lattice holding and transporting atoms, the frequency output has to be changed over a few Megahertz in a few milliseconds but with a smooth and precisely shapable frequency profile. Quick sweeps of high resolution have to be performed.

- Frequency and phase offset switches need to be very agile, nearly instantaneous and can not require time to “tune in”, that is to reach their final state.
With analog frequency sources (all types of “oscillators”) most of these requirements cannot be fulfilled. The sources are either limited in their tuning range, are slow when tuning in and cannot be phase locked to a reference frequency throughout their frequency range. A few of the requirements can be accomplished by using an array of frequency sources and subsequently multiplying and switching between them. That approach, however, leads to a complex, large and expensive design with many possible sources of errors.

If one could devise a device that is fast enough to directly output the appropriate instantaneous signal values that in time synthesize a sinusoidal frequency, the requirements could be fulfilled given suitable mechanisms to control the way the signal is generated over time. This method is most easily implemented in digital circuits and thus called direct digital synthesis or DDS. The telecommunication industry with its broadband data transmissions and high frequency digital circuits had the need for agile frequency sources of large tuning range and generated enough demand to foster the development of DDS chips that produce the aforementioned signals at a rate of up to 1 GHz. Those chips are commercially available. The principles and limitations of direct digital synthesizers are explained in detail in chapter 3.

Centered around such a fast DDS chip a device has been designed which is specifically suited for experiments with cold atoms. A control software allows the user to specify the pulse sequence and the profiles of phase, frequency and power in a graphical way. From the user’s input a descriptive format, a recipe, is distilled and sent over a standard computer network to the device. On the device the recipe is then interpreted and executed synchronously to the rest of the experiment. The design is detailed in chapter 4.

In chapter 5 the first revision of the device is characterized under different aspects and realistic circumstances and with respect to its specifications and desired applications.

Following the characterization, in chapter 6 the device has been integrated into an experimental apparatus that produces a BEC of $^{87}$Rb atoms. The frequencies generated by the device control the transport of the BEC in a standing light wave into an optical cavity where the atoms are detected. The characterization and the effectiveness of the transport in the experiments demonstrate the properties of the radio frequency source.\(^1\)

\(^1\) Throughout the text explanatory footnotes have been added where terms are used the casual reader might not be familiar with. The footnotes give a brief but hopefully sufficient definition and explanation of the respective term as well as a link to further literature.
Chapter 2

Manipulating Atoms with Radio Frequencies

Present experiments with ultra-cold atoms rely heavily on manipulation of quantum states with radio frequencies (RF). In this chapter some cases of manipulative techniques will be explained. The experimental techniques range from direct interaction of the quantum states and radio frequency electromagnetic fields that induce transitions between states to indirect methods where a light field’s frequency is shifted by an RF signal and used to create a spatially varying potential for the atoms.

The electromagnetic fields used to drive the transitions generally can be of a wide frequency range from lower radio frequency bands up to the optical frequencies. But radio frequencies are regularly employed even if the actual transition is accessed by such a high frequency: Microwave radiation is combined with RF by multi-photon or Raman processes. For optical frequencies it is common practice to shift the frequency of the light emitted by a laser whose frequency is locked onto a narrow atomic transition. This is accomplished with the help of an acousto-optic (AOM) or electro-optic modulator (EOM). The amount of the frequency shift is determined by the frequency that drives the modulator.

2.1 Hyperfine and Zeeman Levels

In Figure 2.1 a typical level scheme of the hyperfine structure and the Zeeman sublevels of an atom is shown. The scheme consists of the two hyperfine levels $F = 1$ and $F = 2$ whose $(2F + 1)$-fold degeneracy splits up in a magnetic field into the Zeeman sublevels $m_F \in \{-F, \ldots, 0, \ldots, F\}$. The Zeeman levels have a different energy depending on the external magnetic field.

In the following sections the level scheme and the indicated transitions will be used as a generic example to explain the different methods employed to prepare quantum states.

2.2 The Bloch Sphere

For the interpretation of the interaction of electromagnetic radiation with quantum mechanical states an introduction to the Bloch sphere is useful.\(^1\)

\(^1\)An extensive treatment is given, for example, in [9].
Chapter 2. Manipulating Atoms with Radio Frequencies

\[ F = 1 \quad m_F \in \{-1, 0, 1\} \]

\[ F = 2 \quad m_F \in \{-2, -1, 0, 1, 2\} \]

Figure 2.1: Hyperfine and Zeeman level structure of the $5^2S_{1/2}$ ground state of $^{87}$Rb. The vertical position of the levels indicates their energy (not to scale). Transitions mentioned in the text are indicated by arrows. The $F = 1$ and $F = 2$ hyperfine levels’ degeneracy is removed when a magnetic field is applied. Each hyperfine level then splits up into $2F + 1$ Zeeman sublevels where the separation of the Zeeman sublevels increases with the magnetic field.

Given a two-level system with unperturbed and uncoupled eigenstates $|1\rangle$ and $|2\rangle$—describing for example a particle with spin $1/2$ or an idealized two-level atom—and subjecting it to a oscillating electric field, the system’s trajectory through phase space is a time-dependent linear combination of the two eigenstates [9]:

\[ |\psi(t)\rangle = a(t)|1\rangle + b(t)|2\rangle. \tag{2.1} \]

One defines the three real quantities

\[ u = ab^* + a^*b, \tag{2.2a} \]
\[ v = -i(ab^* - a^*b), \tag{2.2b} \]
\[ w = a^*a - b^*b, \tag{2.2c} \]

and identifies them as a vector $s(t) = u\mathbf{e}_1 + v\mathbf{e}_2 + w\mathbf{e}_3$. Here, $w$ is the population inversion between $|2\rangle$ and $|1\rangle$. It is required by population conservation that that vector lies on the unity sphere since $s^2 = u^2 + v^2 + w^2 = |a|^2 + |b|^2 = 1$. This sphere is the so-called the Bloch sphere, Figure 2.2(a).

The electromagnetic field that interacts with the two-level system is represented by a vector $f$ in the plane of $\mathbf{e}_1$ and $\mathbf{e}_3$ [9]:

\[ f = \Omega\mathbf{e}_1 + \delta\mathbf{e}_3. \tag{2.3} \]

$\Omega$ is the Rabi frequency determined by the dipole moment of the transition and the electromagnetic field strength. $\delta = \omega - \omega_0$ is the detuning of the radiation $\omega$ from the atomic resonance $\omega_0$. The length of the vector $f$ is then $|f| = \sqrt{\Omega^2 + \delta^2}$. When exposed to the electromagnetic radiation, the Bloch vector $s$ precesses around the radiation vector $f$ similar to a spin in a magnetic field:

\[ \dot{s} = s \times f. \tag{2.4} \]
2.2. The Bloch Sphere

Figure 2.2: The Bloch sphere. The unperturbed and uncoupled eigenstates $|1\rangle$ and $|2\rangle$ are located at the poles of the sphere. The equator consists of the equal mixtures $|\psi\rangle = a|1\rangle + b|2\rangle$ where $|a| = |b|$. The normalization constants have been suppressed for brevity. The electromagnetic field is represented by the red vector $f$ in the plane of $\hat{e}_1$, $\hat{e}_3$ and the resulting trajectory of the Bloch vector by the green line.
2.3 \( \pi \) Pulses

Transfer between different states can now be accomplished for example by short pulses. The pulse frequency is chosen to be on resonance, \( f = |\hat{f}| \), and thus the Bloch vector rotates in the plane of \( \hat{e}_2 \) and \( \hat{e}_3 \), with the speed of the effective Rabi frequency \( \Omega' = |\hat{f}| = \sqrt{\Omega^2 + \delta^2} \). After a quarter period the state mixture \( \frac{1}{\sqrt{2}}(|1\rangle - i|2\rangle) \) is reached, Figure 2.2(c). The pulse duration \( \tau = \pi/(2\Omega') \) determines the population ratio of the two states after the transfer to be \( 1/2 \) for each state. After half a period \( \tau = \pi/\Omega' \) the entire population is transferred into the state \( |2\rangle \), see Figure 2.2(b) and Figure 2.1 transition \( \beta \).

Originally this method was applied to molecular beams to perform precision spectroscopy [10]. The method serves to determine with high precision whether the detuning is zero or not: the final state after performing two consecutive \( \pi/2 \) pulses with temporal evolution in between, sensitively depends on the value of the detuning and on the duration of the temporal evolution. The resulting Ramsey fringes are used to determine with high precision the resonance frequency of the transition.

The technique of \( \pi \) and \( \pi/2 \) pulses has also been used in the case of \( ^{87}\text{Rb} \) BECs [11, 12, 13, 14] to prepare condensates in different hyperfine states. Starting from an initial condensate cloud, a microwave pulse at 6.8 GHz (Figure 2.1 transition \( \gamma_1 \)) along with a RF pulse in the order a few MHz (Figure 2.1 transition \( \gamma_2 \)) induces a two-photon process. This process connects the two hyperfine states and permits accurate preparation of state mixtures. \( \Omega' \) is in the order of \( 2\pi \times 600 \) Hz for a \( ^{87}\text{Rb} \) \( |F = 1, m_F = -1\rangle \rightarrow |F = 2, m_F = 1\rangle \) two-photon process and a realistic strength of the electromagnetic field [13]. Typically the pulses are a few 100 \( \mu \)s short and require precise timing in the \( \mu \)s range.

2.4 Landau-Zener Adiabatic Transfer

Instead of using radiation with a frequency exactly on resonance, it is also possible to start with a large detuning \( \delta \) far above the resonance and with all atoms in state \( |1\rangle \) and then slowly decrease the frequency [15]. Initially \( f \parallel s \parallel \hat{e}_3 \) and the Bloch vector does not move at all, Figure 2.2(d). When the detuning gets smaller, \( f \) starts moving towards \( \hat{e}_2 \) and \( s \) precesses around \( f \) but follows its movement closely. They remain almost parallel throughout the frequency sweep. When ending the sweep in a large negative detuning \( f \parallel s \parallel -\hat{e}_3 \) and the entire population is in state \( |2\rangle \). In terms of the energy \( E \) and the detuning \( \delta \) that is adiabatically varied, the process can also be understood as in Figure 2.3.

This Landau-Zener transfer [16, 17, 18] is adiabatic in the sense that the atom remains in the state of lowest energy. Landau and Zener found the adiabatic conversion probability \( P \) during such a transfer to be

\[
P = 1 - e^{-\frac{2\pi\gamma}{4|\delta|}} \quad \gamma = \frac{\Omega^2}{4|\delta| (\epsilon_1 - \epsilon_2)} = \frac{\Omega^2}{4|\delta|}\]

(2.5)

The transfer process as described above can be driven by slow collisions, sweeping of electric or magnetic fields or by sweeping the detuning of a RF or microwave
2.5. Evaporative Cooling

Evaporative Cooling has been a keystone on the way to Bose-Einstein condensation. After having collected atoms in a magneto-optical trap (MOT), the attainable temperatures are still not sufficiently low to achieve condensation. At this stage radio frequency (RF) evaporation is used to remove the hottest atoms from the cloud.

This process is explained in Figure 2.4. The Zeeman levels are split up in a magnetic field. The split depends on the field strength which varies spatially. The $|F = 1, m_F = -1\rangle$ state's energy increases with the field making it a trapped state with atoms in this state seeking low fields. $|F = 1, m_F = 0\rangle$ is untrapped since its energy does not—in the first order—depend on the magnetic field and $|F = 1, m_F = 1\rangle$ is anti-trapped. Atoms in this state seek high fields where their energy is lower.

The transition (also indicated by the green arrow $\alpha$ in Figure 2.1) is induced by a microwave frequency electromagnetic field. Hot and thus fast atoms have a higher probability of being found in regions of high magnetic field since their energy is higher. Cold and slow atoms are found in the trap’s center. The frequency of the microwave radiation determines which atoms are susceptible to being transferred from the trapped to the untrapped state since the energy of the level relative to the final untrapped state changes with the magnetic field. One starts with a frequency corresponding to high magnetic fields that selects hot atoms and removes them from the trap. While lowering the frequency continuously colder atoms are being selected but all the hotter atoms have already been removed. The cloud becomes overall colder.
Figure 2.4: Evaporative cooling. The energies $E(x)$ of the three Zeeman sublevels of the $F = 1$ hyperfine ground state of $^{87}\text{Rb}$ depend on the position $x$ in a spatially varying magnetic field. The atoms are initially all trapped in the low-field seeking $|m_F = -1\rangle$ state. Hot atoms have a high probability of being found at high potential energies and thus at high magnetic fields. There, they also have a different resonance frequency for the transfer into the $|m_F = 0\rangle$ state. By irradiating a microwave into the sample whose frequency corresponds to the resonance of the hottest atoms, only they will be transferred into the untrapped $|m_F = 0\rangle$ state. The rest of the cloud then thermalizes. By decreasing the microwave frequency further the temperature of the cloud is decreased as well.

The sweep is done slowly enough so that the atoms can thermalize and temperature in the cloud is always near the equilibrium. For this method it is desirable to produce a smooth sweep and a phase-continuous signal since spurious frequency components and phase jumps evaporate the wrong atoms out of the cloud.

2.6 Atoms in Standing Light Waves

The last example for the application of a versatile RF frequency source in experiments with cold atoms is of indirect nature. In this case, the radio frequency does not interact with the atoms directly but controls the motion of a standing light wave that is used as a conveyor belt for a BEC of cold atoms.

Strong light fields are known [9] to create a potential for atoms due to the interaction with the atom’s dipole moment which polarizes them and exerts a force. Depending on the detuning with respect to an atomic resonance light fields are attractive if the light is red-detuned and repulsive if the light is blue detuned. The focus of a red-detuned laser beam radially and axially confines the atoms since the intensity is the highest in the focus. The atoms can then be moved by simply moving the focus. These optical tweezers can be employed to move, transport or fixate not only single atoms but even macroscopic objects such as bacteria [19, 20].

A variation of this scheme removes the need for moving the focus and thus mechanically moving optical parts. Two counterpropagating red-detuned laser beams with the wavelength $\lambda$ create a periodic and tightly confining potential in axial direction due to their interference pattern. The pattern has a periodicity of $\lambda/2$ and
2.6. Atoms in Standing Light Waves

Figure 2.5: Transport in a standing light wave. Two laser beams obtained from a diode laser are amplified in tapered amplifiers (TA 1 and 2). The light's frequency is then shifted by two acousto-optical modulators (AOM 1 and 2) by different amounts and subsequently coupled into single-mode fibers. The two beams are brought to counterpropagating interference creating a vertical pattern that acts as a conveyor belt spanning from the place of the BEC cloud to the optical cavity. The interference pattern can be moved in a controlled way by changing one of the two frequencies that drive the AOMs.

ranges from zero intensity to four times the intensity of one beam if both beams are of the same power and geometry. It is then possible to move the atoms without any mechanical movement of optical parts by only shifting the frequencies of the two laser beams relative to each other. A possible experimental setup that achieves this is shown in Figure 2.5.

The light from a suitable diode laser whose frequency is red-detuned from the atomic resonance is split and the two parts are amplified in tapered amplifier chips. The two beams of wavelength $\lambda$ are then sent through two separate acousto-optical modulators (AOM).

The principle of such an acousto-optical modulator is shown in Figure 2.6. A piezo-electric transducer (PZT) injects a running acoustic wave into the crystal that creates a density modulation of the crystal whose periodicity changes with the frequency. Incident light is diffracted by this grating-like pattern into different diffraction orders that separate spatially. By adjusting the angle of incidence it can be achieved that most of the light is transferred into the first order diffracted beam. The different orders are not only spatially separated but also possess different frequencies due to the diffraction by the moving wave. When a RF acoustic wave with a frequency $f$ and momentum $\hbar|K| = \hbar f/(2\pi c_{\text{sound}})$ diffracts the laser light of frequency $\nu$ and momentum $\hbar|k| = \hbar \nu/(2\pi c_{\text{light}})$, the $n$th order diffracted beam has the
Figure 2.6: Acousto-optical modulator. An acoustic wave with momentum $\hbar K$ is generated by a piezoelectric transducer at the lower edge of the crystal and propagates through it. The acoustic wave is a pressure and density pattern that diffracts an incident laser beam of momentum $\hbar k$. The first-order diffracted beam $\hbar k'$ has a different direction and frequency since it has absorbed a phonon from the acoustic wave: $\hbar k' = \hbar k + \hbar K$.

In the experiment sketched in Figure 2.5 the two laser beams are passed through two AOMs that are driven with different frequencies $f_1$ and $f_2$. Only the two first-order diffracted beams with frequencies $\nu + f_1$ and $\nu + f_2$ are coupled into single-mode fibers and brought to counterpropagating interference. The interference pattern has a periodicity of $\lambda/2$. Shifting the two beams by frequencies differing by $f_2 - f_1 = \Delta f$ results in a movement of the standing wave with a speed of $v = \Delta f \lambda / 2$ in the axial direction. In the experiment a BEC is created in a magnetic trap above a high-finesse optical cavity serving to detect the atoms [21]. The standing wave dipole trap is ramped up and the magnetic trap is ramped down to transfer the atoms from the magnetic trap into the optical trap. Then the frequencies $f_{1,2}$ are detuned increasing the speed of the standing wave and the atoms. A description of the frequency profile that is used is given in section 5.7. Experimental results for these transports can be found in section 6.1.
Chapter 3

Direct Digital Synthesizer

Electronic generation of periodic electrical signals has seen numerous different approaches [22]. The oldest and simplest is the resistor, capacitor and coil circuit. These circuits show a resonant behavior at a certain frequency that depends on the electrical properties of the parts involved. The circuit is normally excited by feedback via transformers, vacuum tubes or semiconductor switches. A more elaborate version of this oscillator principle uses a crystal oscillator as the resonant element. The advantage of this simple design is the rapid implementation requiring only a handful of electrical parts. But for all these approaches the tunability is rather limited since in order to change the resonance frequency the electrical properties of the resonant element have to be changed in-place. If a quartz crystal oscillator is employed whose resonance frequency can not be easily changed, it has to be pulled off resonance. When a large tuning range is required, Yttrium iron garnet (YIG) tuned oscillators come into play. A YIG oscillator contains a sphere with ferrite properties that is resonant and whose resonance frequency can be quickly tuned by applying an external magnetic field. The tuning range can span some octaves making a YIG oscillator interesting for use in spectrum analyzers.

To reach other frequencies the output of an oscillator can be divided by integer numbers using digital elements and then filtered again to obtain a more or less pure sinusoidal signal. Up-converting the signal to higher frequencies is accomplished by phase locked loops (PLL) where the output of a tunable oscillator that is resonant at the final frequency is divided by an integer and the phase of the divided signal is compared with the reference signal. This phase difference is then used to tune the oscillator until both phases match. Almost arbitrary fractional ratios $M/N$ of frequencies can be obtained by first down-converting the reference frequency with division by $N$ and then multiplying it by $M$ using a PLL. Each new PLL oscillator limits the performance of the frequency source and increases the complexity of the setup. The reachable tuning ranges are again limited by the tunability of the oscillators involved.

For any of the above frequency sources locking them to a reference frequency gets more difficult with increasing tuning range. A way around this limitation is to combine multiple oscillators’ outputs with electronic mixing. The oscillators can be separately locked onto the reference. Starting from such a bank of many oscillators
Chapter 3. Direct Digital Synthesizer

Figure 3.1: High-level building blocks of a frequency source based on a direct digital synthesizer (DDS). The DDS chip generates the desired output signal from the reference clock. The signal has to be filtered to suppress digital artifacts and is then amplified to the desired power level.

with no or only a small tuning range, the desired output frequency is then combined by sequential electronic multiplication and subsequent filtering. Multiplying two frequencies in a non-linear electronic mixer generates the sum and the difference frequency of the two initial frequencies. To obtain one of these non-linear components the other has to be filtered out. Repeated application of this principle permits generation of frequencies in a wide tuning range. There are drawbacks though: complexity increases with the number of oscillators, desired tuning range and precision of the generated frequency.

With the advent of fast semiconductor electronics with speeds of up to 1 GHz fostered by the demand in telecommunications, a different method to create frequencies from a reference has become feasible. In a high-speed digital chip the output signal values are generated directly in a time-sampled manner and their evolution in time resembles the the desired frequency signal. This method is called direct digital synthesis, DDS. The digital nature of the generation scheme allows for a wide range of interesting features such as fast and complex sweeps, high frequency and phase agility and extremely wide tuning ranges from DC up to 500 MHz. The principles and the features of such a chip will be described in the following section. Since a digital time-sampled system always introduced digital noise as well as artifacts like harmonics and distortion, special attention is given to these effects in section 3.2.

3.1 Principles

Generating frequency signals by direct digital synthesis requires just a few parts which are shown in Figure 3.1. Two inputs, namely a way to control the DDS chip and a reference clock frequency are needed. The controlling part sends parameters such as frequency, phase and sweep rate to the DDS chip and activates them at the desired time. The reference clock serves as a time basis and clocks all processes and actions inside the DDS chip. After the output of the DDS, a filtering element is required that removes digital artifacts. The signal is then amplified by a controllable amplifier and available at the output.

The functional blocks that make up the DDS chip fall into two classes, namely generation of the output signal and communication and synchronization. The two
classes are described in the following sections.

3.1. Principles

The set of equations constituting the processes that determine the output signal generation in the DDS is explained below. A decomposition of a DDS chip into its fundamental building blocks is shown in Figure 3.2. In that figure the flow of the register values and associated variables as well as their effects on the signal is also shown.

Capital variables denote unit-less integer register values implemented in the DDS chip. Lower-case variables denote the scaled physical quantities that bear units. \( \lfloor x \rfloor \) is the floor-function returning the nearest integer smaller than or equal to \( x \).

The DDS’ signal-determining heart is a phase word \( P \) implemented as an accumulator\(^1\) holding an integer phase value in the range \([0, 2^\alpha - 1]\), \( \alpha = 32 \). The phase word \( P \) is periodically incremented by a frequency word \( F \), an integer in the same range as the phase word. The phase word \( P \) represents the phase \( \phi \) of the output signal at a given point in time, \( t \):

\[
P = F \lfloor \nu_0 t \rfloor \mod 2^\alpha, \quad \alpha = 32, \quad \phi = 2\pi \frac{P}{2^\alpha},\tag{3.1}
\]

while the frequency word \( F \) represents the frequency \( f \),

\[
f = \nu_0 \frac{F}{2^\alpha}.	ag{3.2}
\]

The increments happen at the rate set by the reference clock \( \nu_0 \),

\[
\nu_0 = 10 \text{ MHz} \times \frac{2^{20}}{10^4} = 1.048576 \text{ GHz},\tag{3.3}
\]

which is supplied to the DDS chip. A synchronization clock \( \nu_{\text{sync}} \) that runs at \( \nu_0 / 8 \) is deduced from the reference clock by simple integer division. \( \nu_{\text{sync}} \) is the clock that determines the communication process and the synchronization of the register updates as will be seen later.

The phase accumulator is cyclic in the sense that it overflows periodically when the maximum value is reached. The overflows happen at a rate of \( f = \nu_0 F / 2^\alpha \) which is the output frequency. Due to these overflows, the phase word register’s value is a saw-tooth shaped curve in time.

In some frequency generation schemes the different frequencies run in parallel and a switch between output frequencies consists of physically switching between the sources. This is fundamentally different in the DDS scheme. Since the phase is always incremented by the current frequency, there is no equivalent of switching between frequencies in a DDS chip. The difference between different frequencies that

\*An accumulator is a register holding an integer value. The value range spans from zero two a power of two. Frequently used accumulator widths \( \alpha \) are 16 and 32 allowing value ranges from zero to \( 2^{16} - 1 \) respectively \( 2^{32} - 1 \). An accumulator accumulates its value by being incremented. Accumulation is understood as the operation \( A' = (A + \delta A) \mod 2^\alpha \) where \( A \) and \( A' \) are the accumulator values before and after the increment \( \delta A \).
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Figure 3.2: DDS block diagram. Arrows denote signal paths that can be either a clock, a digital or an analog signal. Arrows with a diagonal line are a digital signals of a certain bit-width. The insets at the right side give a rough example of how the value at that specific stage in the signal generation process looks like. The formulas are shortened to aid readability. A detailed explanation of the diagram is given in the text.
are generated subsequently is just the rate at which the phase changes. A DDS is thus inherently phase continuous.

After truncation of the instantaneous value of the phase accumulator,

\[ P' = \lfloor P/2^{a-b} \rfloor, \quad b = 14, \quad (3.4) \]

it is fed as an address pointer into a sine look-up table (LUT)\(^3\) implemented as a read-only memory. This way, a time dependent digital amplitude value \( U \) is obtained from the phase value:

\[ U = \lfloor 2^c \sin(2\pi P'/2^b) \rfloor, \quad c = 10. \quad (3.5) \]

The output from the sine LUT is \( c = 10 \) bit wide and in time resembles a digitally sampled (at the rate \( \nu_0 \)) representation of the frequency \( f = \nu_0 F/2^a \).

To obtain an analog signal, the output value from the sine LUT is passed to a digital to analog converter (DAC)\(^4\) on every reference clock cycle yielding the output signal:

\[ u = u_0 \frac{U}{2^c}. \quad (3.6) \]

The signal is yet to be filtered appropriately to get rid of the distortions due to the discrete sampling (see section 3.2):

\[ u'(f) = \alpha(f)u(f). \quad (3.7) \]

The various implementations of DDS chips add further features to this trivial behavior. A simple but powerful change is the implementation of the frequency word \( F \) as another accumulator holding the constant frequency tuning word FTW and adding to it a differential frequency tuning word DFTW at a rate set by the synchro-

---

\(^2\)“Phase continuity” is not the same as “phase coherence”. The former refers to a continuous variation of the phase over the entire frequency sweep or switch including periods of “zero” frequency. Phase coherence on the other hand refers to the case where all frequencies generated during a sweep or switch once have the same relative phase when extrapolated to a chosen initial point in time. Phase coherent operation is typically non-continuous.

\(^3\)A look-up table is a list of return values generated from a function \( f(x) \) such as for example \( f(x) = \sin x \). It is easily implemented as an area of contiguous memory. The return value \( f(x_i) \) for a given discretized input value \( x_i \) is then obtained by suitably mapping the \( x_i \) to the range of indices of input values and returning the value at the memory address corresponding to the \( i \)th input value. A table of \( 2^b \) possible input values \( x_i \) and a return value \( f(x_i) \) that is \( c \) bits wide, is \( 2^{b+c} \) bits large.

\(^4\)A digital to analog converter transforms an integer number that is digitally represented as a set of binary bits into an appropriate voltage or current signal proportional to the digital number. A DAC can be easily implemented as a set of switchable resistors forming a \( R2R \) network, [http://en.wikipedia.org/wiki/Resistor_Ladder](http://en.wikipedia.org/wiki/Resistor_Ladder).
nization clock divided by a *differential ramp rate word* (DFRRW).

\[
\nu_{\text{sweep}} = \frac{\nu_{\text{sync}}}{\text{DFRRW}} = \frac{\nu_0}{8 \times \text{DFRRW}},
\]

(3.8)

\[
\delta f = \frac{\nu_0}{2^a}, \quad a = 32,
\]

(3.9)

\[
\nu_{\text{sweep}} \delta f = \frac{\delta f}{\delta t_{\text{sweep}}} = \frac{\nu_0^2}{2^{a+1}} \times \text{DFTW}. \quad \text{(3.10)}
\]

With the frequency word now changing linearly in time,

\[
F = \text{FTW} + \text{DFTW} \lfloor \nu_{\text{sweep}} t \rfloor \mod 2^a,
\]

(3.11)

a linear frequency sweep with a speed proportional to \(\text{DFTW}/\text{DFRRW}\) is the result. By changing \(\text{DFTW}\) and \(\text{DFRRW}\) registers quickly, arbitrary sweeps can be approximated by piecewise linear segments.

Another easily implemented feature is an adjustable *phase offset word* \(\text{POW}\) which is added as an offset to the phase accumulator:

\[
P = \text{POW} + F \lfloor \nu_0 t \rfloor \mod 2^a.
\]

(3.12)

Phase modulation of the output can then be implemented by simply changing the phase offset word register.

Analog Devices\(^5\) offers a variety of DDS chips. They differ in speed and added features such as on-chip PLL or mixer circuitry. Some chips combine multiple DDS cores synchronized to each other yielding different output frequencies with a well-defined phase relation that is given by their phase offset words. Others include means to rapidly switch the frequency and phase offset words not by repeatedly writing to registers (which is much slower than the reference clock) but by switching between different pre-programmable register value sets via external signal lines. That enables fast digital modulation techniques such as phase shift keying\(^6\).

### 3.1.2 Communication and synchronization

The DDS receives a *reference clock* frequency \(\nu_0\) (1.048576 GHz in the current implementation) against which all operations including the communication bus and the output are synchronized. This reference clock serves as a global time base for every operation that is time or frequency related. The DDS chip itself is totally agnostic with respect to the actual value of the frequency. That means that by changing the reference clock, the output of the DDS is changed in time by the same relative amount. All parameters that adjust the operation of the DDS chip are thus given in fractions of the reference frequency. How the reference clock is generated exactly is of little

\(^5\)http://www.analog.com/

\(^6\)Phase shift keying is a modulation technique that encodes the digital value that is to be transmitted in the phase shift of the carrier signal. http://en.wikipedia.org/wiki/Phase-shift_keying
3.1. Principles

![Diagram of DDS register transfer and synchronization mechanism.]

**Figure 3.3:** DDS register transfer and synchronization mechanism. The port used to write registers can be either the serial or the parallel port. The write operation targets the buffer registers while the active register values are only updated with the values from these buffer registers if the frequency update (FUD) signal is asserted. The update then happens synchronously to the synchronization clock. The sampling of the FUD signal at the synchronization clock cycles is performed by a D flip.

interest, except that since in most applications it is a fixed frequency, it can easily be locked onto a reference frequency such as the 10 MHz obtained from the Global Positioning System (GPS).

The DDS is controlled via an electronic bus\(^7\) (either serial\(^8\) or parallel\(^9\)) over which DDS register values can be written (and for debugging purposes also read) as depicted in Figure 3.3. The control mechanisms includes activating and deactivating functional blocks as well as changing registers that determine the output frequency and the behaviour of the chip with respect to other external signals. Setting any of the registers over the communication bus does not immediately affect the operation of the chip upon completion of the write operation. The values first get buffered in a set of buffer registers. Another register set, the working registers, determines the operation of the DDS chip. The transfer from the buffer registers into the working registers is done synchronously by a pulse on a frequency update (FUD) line. The FUD signal is sampled at the synchronization clock cycles and if the signal is asserted during a

---

\(^7\)A bus is an interface between two or more electrical devices. It consists of a group of electrical signals each having a specific function. A bus can be unidirectional or bidirectional, adhere to a complex digital communication protocol or just distribute analog values or supply voltages. [http://en.wikipedia.org/wiki/Electrical_bus](http://en.wikipedia.org/wiki/Electrical_bus)

\(^8\)A serial bus transports the data bit by bit on a single wire. In the majority of cases an additional clock signal is needed to determine the times at which the data wire has certainly reached the desired value and the data is to be sampled by the receiving device. [http://en.wikipedia.org/wiki/Serial_bus](http://en.wikipedia.org/wiki/Serial_bus)

\(^9\)Parallel busses transport the data in larger sets than a single bit. The set can be of any size ranging from a handful up to several hundreds bits transmitted on equally many electrical wires. Since many data bits are transferred at the same time, parallel busses generally provide higher data rates at the price of a more complex wiring schemes and more electrical signals.
Chapter 3. Direct Digital Synthesizer

rising edge of the synchronization clock, the update takes place. Synchronous activation of a possibly complex set of parameter changes permits a quick and synchronous switch between largely different modes of operation.

A few sections of the DDS chip are not directly synchronized to the full resolution reference clock but only to a pre-scaled clock, the synchronization clock (sync clock) which is derived from the reference clock by division by 8. The generation of this clock is done internally by the DDS chip but the clock is externally available on the chip for synchronization purposes. Since the synchronization clock is the highest rate at which the communication with the DDS chip and register updates can be performed it is desirable to also synchronize the device controlling the DDS chip to this clock. In order to obtain two frequencies that have a controllable phase relation to each other two DDS chips have to be synchronized not only with respect to their reference clocks but also with respect to their synchronization clocks. The necessary synchronous reset of the divide-by-8 counter that generates the synchronization clock can be triggered over an externally accessible reset pin.

3.2 Noise and Spurious Frequencies

The output of a DDS always contains noise and spurious frequencies. These artifacts are due to different reasons and have been subject of thorough analysis [23, 24, 25].

For a given and fixed application it may be possible to select reference and output frequencies in such a relation that either all spurious frequencies are outside the region of interest or fall together with the desired output frequency. But restricting the output to certain frequencies only is not an option keeping in mind the desired applications in experiments. It is thus advisable to design a good filter that suitably attenuates the spurious frequencies that lie above the highest frequency that can be generated. Additionally an understanding of the sources of noise and spurious frequencies in the region that is not attenuated by the filter lets one estimate possible limitations and predict problems.

In the following sections the main reasons for noise and spurious output frequencies will be described. For an exemplary spectrum see the wide-band and narrow-band spectra of the output of the DDS device in Figure 5.3(a) and Figure 5.3(b) respectively.

3.2.1 Reference Clock

All operation of of the DDS is directly deduced from the reference clock. Frequency, phase and amplitude errors there feed through to the output signal. Since the output is essentially the divided reference frequency, a relative error in the reference clock frequency induces the same relative error in the output frequency. The same is true for phase jitter and noise, inducing jitter and noise in the output which is attenuated (relative to the input jitter and noise) by \( \log N \times 20 \text{ dB} \) where \( N \) is the ratio between reference clock and output frequency: \( N = 2^a/F \), \( a = 32 \) for the given DDS chip at a given frequency word \( F \) [23]. Amplitude modulation of the reference clock on the other hand can only feed through to the output if it survives the input squaring
3.2. Noise and Spurious Frequencies

circuit of the DDS which converts a possibly sinusoidal signal to a square wave in order to obtain well-defined and stable clocking edges. The input limiter typically converts the amplitude modulation of the reference clock into a phase modulation which is about 6 dB smaller [23]. The phase modulation can pass the DDS circuitry and is attenuated by \( \log N \times 20 \) dB as described above.

### 3.2.2 Phase Truncation

In order to provide fine-grained frequency resolution in the order of \( 2^{-32} \) of the reference clock (about 0.25 Hz in the current setup) only the frequency word and the phase word have to be \( a = 32 \) bits wide. But using a 32 bits wide input value to the sine look-up table (LUT) and a 32 bit deep digital to analog converter (DAC) is impractical due to the necessary size and memory consumption in the order of \( 2^{32} \times 32 \) bits or \( 10^{11} \) bytes (hundreds of Gigabytes). Also, a realistic 32 bit DAC that could convert the 32 bit sine value obtained from the lookup-table loses probably a third of its bits to noise.

Realistic DDS chip designs have to truncate the phase fed to the sine LUT and also truncate the digital value of the sine fed to the DAC to reduce the size of the LUT. It is also advisable to exploit the quarter wave symmetry of the sine or use other techniques of phase to sine conversion like those suggested in [24]. The techniques mentioned there employ a reduced sine LUT or generate the value in an entirely algorithmic way and without a LUT.

The AD9858 DDS has a \( b = 14 \) bit wide and 10 bit deep sine LUT and a 10 bit DAC and thus truncates the phase word by \( a - b = 18 \) bits. Those discarded lower bits induce a modulation in the phase value sent to the sine LUT with respect to the ideal phase. The phase modulation is determined by the discarded bits in the phase word. They have a periodicity of \( \nu_0 \times m/2^{a-b} \) where \( m \) is the decimal value of the discarded bits in the frequency word. This can be easily understood since the \( a - b \) bits that are truncated from the phase word overflow into the remaining \( b \) bits that form the input to the sine LUT. The rate at which they cause this additional increment is just \( \nu_0 \times m/2^{a-b} \). The mechanism is analogous to the effect of the full frequency word on the full phase accumulator. The amplitude of the spurious frequency created by phase truncation is estimated to amount to \( -b \times 6 \) dBc (dB relative to the carrier) [23]. A 14 bit sine LUT is thus expected to produce phase truncation spurs at \(-84\) dBc.

### 3.2.3 Quantization Noise and Non-Linearities

The DAC (or equally the sine LUT) rounds the amplitude output value to the nearest \( c = 10 \) bit value. This quantization results in a total noise power of \(-1.67 - 6 \times c \) dBc = \(-62\) dBc [23]. The location of the predominant spurs depends on the sine LUT and DAC architecture, the frequency word and the reference frequency. A method to determine these frequencies is given in [23].
Chapter 3. Direct Digital Synthesizer

Figure 3.4: Creation of alias frequencies in digital signals. The green line is the fundamental frequency $f$ that is to be reconstructed by the blue digital signal with a sample rate of $\nu_0 = 3f$. The digital signal samples the green one at every sampling point (black) $n/\nu_0$ and holds that value up to the next sampling point. The red curve with $f' = \nu_0 + f = 4f$ is an alias and represented equally well by the digital signal.

3.2.4 Digital Aliases

The highest possible frequency $f_{\text{max}}$ that can be digitally generated with a sampling rate of $\nu_0$ is $f_{\text{max}} = \nu_0/2$ since at least two samples are needed to form a period. This relation is known as the Nyquist–Shannon sampling theorem. The interval $[0, \nu_0/2]$ is called the first Nyquist zone. It is to be expected that a digital reconstruction of the frequency $f$ is only injective in this first Nyquist zone: The frequency $f$ has one of its aliases at $\nu_0 + f$. That frequency would be represented by the same digital signal as demonstrated in Figure 3.4.

The aliases appear in the output of the DDS as integer linear combinations of the carrier and the sampling rate (reference clock) $k\nu_0 + lf$ with integer $k$ and $l$. These combinations are also folded back into the first Nyquist zone $[0, \nu_0/2]$ by the aliasing process described above. The aliases can also be created by non-linear processes in the DAC and the amplifier that produce sum and difference frequencies.

Predicting the power contained in the alias frequencies of a digitally sampled signal is not easily done analytically. However, it is true that the power in these harmonics generally decreases with increasing $|k|$ and $|l|$. Increasing the reference clock $\nu_0$ and maintaining the same output frequency $f$ thus shifts the harmonics out of the region of interest. Choosing the highest possible frequency as a reference clock does not only enlarge the output frequency range but also the decreases the amount of spurious frequencies close to $f$.

As seen above, the range of useful output frequencies is the first Nyquist zone $[0, \nu_0/2]$. To suppress aliases and harmonic combinations outside that zone, a reconstruction filter is required. If only a small interval of output frequencies is of interest, the filter can be a band-pass. Otherwise it has to be a low-pass with a cutoff at the Nyquist frequency $\nu_0/2$. The ideal characteristic of such a filter is a low-pass with a rectangular transfer characteristic suppressing all frequencies above $\nu_0/2$. A rect-

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11 The situation is similar to that of the quantum mechanical wave function of an atom in a periodic potential. Wave functions with momenta above the inverse lattice constant in the higher Brillouin zones alias back into the first zone.
3.2. Noise and Spurious Frequencies

Figure 3.5: The function $\text{sinc}(t) = \frac{\sin(t)}{t}$ (blue) is the Fourier transform of the rectangular low-pass. Its square (red) corresponds to the sinc-filter transfer function in terms of attenuation of the power. A time-sampled digital signal has to be convoluted with this filter to free it from aliases.

angle in the frequency domain is the $\text{sinc}$ function $\frac{\sin(t)}{t}$, Figure 3.5, in the time domain. While this function is the ideal filter, it has a non-compact support making its delay infinitely large and thus unsuitable for realistic filtering. A sinc of reduced size can be implemented though. Some DDS chips integrate such a filter that has a finite window size and can be applied to the output.
Chapter 4

Design of the Frequency Source

The frequency source device was designed in a top-down\footnote{http://en.wikipedia.org/wiki/Top-down} process. Starting from the specifications that were dictated by the desired experimental applications, modular parts that are self-contained and can be exchanged and improved separately were designed. The blocks described in this chapter are the reference clock, the DDS board and the controller. Other blocks are yet to be finished and are only mentioned briefly.

4.1 Specifications

The specifications for the device to be designed were the following:

- A frequency output range from 0.5 MHz to 400 MHz in steps of 10 Hz is needed to cover different application ranges. The resolution is chosen to be high enough to enable tunability even in applications where the suitable frequencies are only from a narrow range such as the different transfer mechanisms described in chapter 2.

- To address power dependent processes or peripherals like acousto-optical modulators and RF amplifiers that have an optimal input power, the output power of the device should be adjustable from $-25$ dBm to $15$ dBm in steps of 0.1 dBm.

- With regard to experimental reproducibility and ease of testing alternative frequency ranges without the need for complex calibration measurements, the power output shall be calibrated to an uncertainty of less than 3 dBm over the entire frequency range.

- A controllable phase offset between two frequency sources and between different pulses from the same frequency source is desirable. Adjustable phase becomes a necessity when generating Ramsey pulses and when fine grained control over the transport in standing light waves is needed.

- Being able to play frequency and amplitude profiles consisting of at least $10^5$ points at a rate of at least 1 kHz guarantees good resolution of the pro-
files and at the same time long profiles. Both are needed for RF evaporation and controlled transport in the standing light wave.

- In order to lock the frequency source’s operation to the other devices involved in the experiment one needs to be able to externally trigger the pulse or sweep produced by the device. The delay with respect to the trigger is required to be as constant as possible while its absolute value is of no importance.

- Spurious frequencies, harmonics and aliases in the output are to be suppressed by at least $-40$ dBc with respect to the carrier for a given output power level. Otherwise the erratic signals could cause heating or evaporation of the wrong atoms.

- Spikes larger than 15 dBm when powering on or off have to be suppressed in order to not endanger connected equipment such as amplifiers.

- Some applications require that the output frequency be as precise and constant as possible. For these purposes the output should be deduced from a 10 MHz reference frequency provided externally by a GPS disciplined oscillator. Simpler applications where frequency precision and stability are not strictly required are to be served in a stand-alone mode where a quartz oscillator generates the reference clock.

- Connection to external systems such as mixer or amplifiers is to be done with a standard SMA type jack output at the front panel of the device.

- Physical integration into the experimental hardware shall be done by fitting the device into a short 19 inch wide standard electronics rack.

- The device is required to be network controllable with a simple text-based protocol that is transferred over a standard computer network and the communication layer TCP/IP.

- The controlling driver generating the recipe that describes the sweeps and pulses and afterwards uploads the recipe to the device is to be integrated as an extension to the existing ExperimentWizard software that runs the entire experiment.

All those specifications have been fulfilled or surpassed by the design. The critical ones are analyzed in chapter 5 using the first revision of the device.

4.2 Hardware

In order to keep electromagnetic interference and crosstalk between the different modular subsections of the device to a minimum, a design where each building block is given its own shielded box was chosen. A photo can be seen in Figure 4.1(c). The boxes are made of thick and specially coated aluminum providing excellent RF
shielding. All modules have the same width and height but different lengths depending on whether they need access to the front panel or not. Given the height of a 4-unit 19 inch rack, a maximum of 4 modules can vertically fit into a device’s box. The modules are interconnected via SMA plugs and coaxial cables on the rear and via the 20-wire communication bus on the front. Available and planned modules are the following:

- The reference clock board receives a 10 MHz input from an external frequency reference such as a GPS frequency standard. On the controller board there is also space for a standard 10 MHz oscillator which can be connected to the reference clock and enables stand-alone operation of the entire device. The reference clock output can be obtained at the rear panel and fed into the DDS board that houses the DDS chip. It is described in the following section.

- The DDS board is the core module containing the DDS chip, anti-aliasing filter, amplifier and controllable attenuator. The board has a SMA input for the reference clock and a SMA output for the output frequency on the rear panel. On the front it connects to the 20-wire communication bus. The board is described in detail in subsection 4.2.2.

- In order to reach into the frequency range of 6.8 GHz (the ground state hyperfine splitting of $^{87}$Rb), a PLL/VCO module for that frequency is being designed. The module features a mixer that adds the DDS output frequency to the local oscillator’s frequency of 6.8 GHz This way it shifts the 500 MHz output frequency range of the DDS into the 6 – 7 GHz band.

- To have a simple fixed-frequency source, a small control panel for the DDS board has been designed which allows manual control of frequency and power at the front panel.

- The embedded computer controlling the DDS for complex operations has been given its own board in the stack. It provides network connectivity and a TTL trigger input as well as an informative LCD output at the front panel. The computer directly controls all hardware in the device. The design and properties of the controller board are described in detail in subsection 4.2.3.

### 4.2.1 Reference Clock Board

The reference clock board uses a two-stage phase locked loop (PLL) setup to up-convert the 10 MHz reference to 1048.576 MHz. The first PLL’s voltage controlled oscillator (VCO) runs at 8.192 MHz. It is tuned in a feedback loop that compares the 10 MHz reference divided by $5^4$ with the VCO after division by $2^9$,

$$8.192 \text{ MHz} = 10 \text{ MHz} \times \frac{2^9}{5^4}. \quad (4.1)$$
Chapter 4. Design of the Frequency Source

(a) The controller board.

(b) The DDS board.

(c) The stack of boards.

Figure 4.1: Photos of a controller board, a DDS board and the entire stack consisting of two shielded DDS boards and the controller board as well as an empty box at the bottom that is used as a spacer.
The second stage oscillates at the final frequency of 1048.576 MHz and its signal divided by $2^7$ is phase locked to the output of the first oscillator,

$$1048.576 \text{ MHz} = 8.192 \text{ MHz} \times 2^7 = 10 \text{ MHz} \times \frac{2^{16}}{5^3}. \tag{4.2}$$

The design achieves sufficiently fast locking of the PLLs and low phase noise at the output. Without the external reference connected the board still provides a usable output signal. The precision and stability are degraded though. Circuit schematic and board layout are reproduced in Figure A.2 and Figure A.1.

### 4.2.2 DDS Board

The DDS board is systematically divided into two parts. The digital signal path contains the busses and the DDS chip up to the DAC output. Its schematic diagram is reproduced in Figure A.4. The analog part includes the transformer after the DAC output, the anti-aliasing low-pass and the amplification and attenuation stages and is shown in Figure A.5.

The layout of the DDS board is reproduced in Figure A.3. For a photo of the fully assembled first version of the DDS board see Figure 4.1(b). Giving the digital and the analog part spatially and electrically separated tracks reduces digital noise on the analog signals. Special care has been taken to provide good thermal and electric ground to power-dissipating and noisy digital parts.

#### Digital Signal Path

Starting from the reference clock input the input signal is impedance matched\(^2\) to 50 $\Omega$, capacitively decoupled\(^3\) and fed into the DDS chip using its input in single-ended\(^4\) mode. Some parts of the DDS chip are unused (PLL and mixer circuitry, parallel input) and are decoupled capacitively.

The DDS chip provides two different busses that can be used to communicate with it. The chip can be either controlled via a standard parallel bus consisting of 8 data lines and one strobe line providing high speed (100 MHz) data transfer but requiring many pins and many signals on the board. The serial bus on the other hand allows sufficient data rates (up to 10 MHz) and requires only three wires. Due to the restricted number of pins on the bus connecting the DDS board and the controller board, the serial bus has been chosen.

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\(^{2}\)Matching output impedance—usually 50 $\Omega$—of a high-frequency signal source with the input impedance of the signal sink is required to maximize the amount of power transferred from source to sink and minimize the power reflected by the sink back to the source. [http://en.wikipedia.org/wiki/Impedance_matching](http://en.wikipedia.org/wiki/Impedance_matching)

\(^{3}\)Decoupling serves to restrict the kind of signal transferred from source to sink to a certain frequency range. Here the DC and low-frequency parts of the signal are blocked. [http://en.wikipedia.org/wiki/Decoupling_capacitor](http://en.wikipedia.org/wiki/Decoupling_capacitor)

Figure 4.2: SPI serial port timing diagram. Time increases horizontally. Double vertical bars denote that a possibly longer time interval has been skipped. Drawn are the serial clock signal (CLK), the serial data signal line (DTA), the chip select line (CS) and the frequency update signal (FUD). X means that the signal X has inverted logic. It is active (asserted) when the signal is low and inactive (not asserted) when the signal is high. The process of setting a register value such as the frequency tuning word is as follows: The controller asserts (pulls low) the CS signal of a specific DDS board on the bus signalling to the DDS chip that the data following now is destined to be interpreted by it. Keeping the CS signal low throughout the process of setting the register’s new value, the serial clock CLK is started and kept running at a rate chosen by the controller. Setting a register value consists of first transmitting the address of the register, an 8-bit integer, and then the new content. Since the registers are of different length depending on their function—some are 16 bits, long others are 32 bits long—the number of data bits transferred after the address has to match the size of the register. Otherwise synchronization of the communication will be lost. Before each rising edge of the clock the data line has to be stable and bear the value of the bit that is to be transferred. After the rising edge of CLK the data line is driven to the value of the next bit. If all bits have been transferred the clock is stopped and the chip select signal CS is unasserted. The value is stored in the buffer register at this points. When the new register values are to be activated, a short pulse on the frequency update line is given that transfers the values from the buffer registers to the active registers.
The protocol that the serial bus adheres to, is the Serial Peripheral Interface bus, SPI, whose timing is illustrated and explained in Figure 4.2. The serial bus lines, FUD and RESET signals are CMOS logic voltage level matched with resistive voltage dividers.

For applications that require synchronized output of two frequencies, two DDS boards have to be placed on the communications bus to the controller. To distinguish the two DDS boards the following scheme is employed: The DDS chip ignores all action and data transmitted on the DTA and CLK lines when its CS line is not asserted. That makes it possible to connect multiple DDS chips and boards to the same serial bus. In order to distinguish for example two of them, it is sufficient to use two separate chip select signals CS<sub>1,2</sub>. The DDS boards can be equipped in two different ways such that the two boards listen on different chip select lines.

**Analog Signal Path**

The analog signal path begins with the digital to analog converter in the DDS. The output of the chip is differential and current sinking. It has a rather high impedance of 100 kΩ making resistive or inductive impedance matching with a resistor network or a transformer necessary. The transformer has been chosen over the resistor due to the low losses of the former and the inherent galvanic isolation. The two complementary signals are led through the transformer which has a 1:1 ratio of turns. It removes the DC bias and matches the DDS DAC output impedance to a 50 Ω load before it is passed to the low-pass anti-aliasing filter.

The filter is made of two commercially available integrated low-pass filter blocks that suppress frequencies above 560 MHz and 460 MHz respectively. The attenuation quickly increases with increasing frequency. The two filters surround a T-shaped set of transmission lines<sup>6</sup> acting as another frequency selective element. The transmission lines together with a capacitor form a notch filter that has a resonance frequency between the characteristic cutoff frequencies of the two low-pass filters at about 520 MHz. The notch-filter short-circuits signals with its resonance frequency to ground. It is thus a narrow-band blocking filter. Due to the narrow resonance of the notch filter the onset of strong attenuation of the entire anti-aliasing filter can be tuned by modifying just this notch filter. By cutting traces on the board, the length of the transmission line is changed and with it the resonance frequency. The filter is analyzed in section 5.2.

To provide the necessary range of output power, a combination of two fixed amplifiers and two digitally switchable attenuator sets completes the DDS board. The amplifiers provide a fixed amplification of up to 14.4 dB each while the attenuators

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<sup>5</sup>http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus

<sup>6</sup>A transmission line is a strip of copper on a printed circuit board having definite length and distance to the surrounding grounded planes. It can serve as an impedance converter that is selective for certain frequency depending on its length. For a signal of this frequency, the transmission line can then, for example, function as an effective short-circuit. http://en.wikipedia.org/wiki/Transmission_line
provide up to 31.5 dB attenuation in 0.5 dB steps each. They are cascaded and controlled digitally over the same serial bus as the DDS chip. To distinguish them as separate listeners on the bus they have a separate chip select line. The amplifiers receive their supply current as a DC bias on their output. Crosstalk from the amplifiers’ output to the supply has to be inhibited by inductors that block high frequency components.

Also included on the DDS board is a digitally controlled potentiometer to fine-tune the resistor that serves the DDS as a reference current source for the DAC. The potentiometer is operated over another serial bus which is different from the SPI bus that is used to connect the DDS and the attenuators with the controller. The bus protocol of the potentiometer is called Inter-Integrated Circuit\( ^7 \), I\( ^2 \)C, and is used as an additional handle to control and calibrate output power. The calibration profile is obtained for each device individually by measuring the output power at various output frequencies and attenuation values. The measured profile is inverted and sampled into a look-up table that returns a control value for a given pair of desired output frequency and output power. The profile can be stored on the DDS board in a 512 kBit large EEPROM\( ^8 \) that is addressed via the I\( ^2 \)C bus which is also used for the digital potentiometer.

The first revision of the DDS board employed a self-regulating power control. A logarithmic detector detecting the output power was used in a control loop. The voltage proportional to the logarithmic output power was compared with a voltage proportional to the desired logarithmic power. The attenuator was then adjusted accordingly forming a feedback loop. Severe ringing was observed making strong damping of the control circuitry necessary. The additionally observed non-linearities of the attenuator and power control are shown and discussed in section 5.4 and Figure 5.4. This first revision of the power control in the prototype was subsequently bypassed and replaced by only one uncontrolled amplifier with constant amplification showing no visible ringing and small non-linearities. The prototype with its uncontrolled and uncalibrated output power served for most of the characterization (chapter 5) and the experiments (chapter 6) that were conducted.

4.2.3 Controller Board

The controller board houses the embedded computer that serves as an interface between the computer network and the busses to the DDS board. It also includes the necessary logic to address a liquid crystal display, LCD, that displays the state of the device as well as the current output frequency and power. A TTL level trigger input is

\( ^7 \)The I\( ^2 \)C bus is another incarnation of the serial bus principle. As opposed to SPI, I\( ^2 \)C does not distinguish the connected participants by a special chip select signal but by device addresses sent at the beginning of a communications sequence. As opposed to the SPI bus the I\( ^2 \)C bus also provides hand-shaking mechanisms to ensure successful and error-free transmission. \url{http://en.wikipedia.org/wiki/I2C}

\( ^8 \)Electrically Erasable Programmable Read-Only Memory is a non-volatile semi-permanent storage mechanism to store small amounts of data for a long time in a solid-state memory without the need for a power supply to refresh the data. \url{http://en.wikipedia.org/wiki/EEPROM}
4.2. Hardware

A small embedded computer running the GNU/Linux operating system has been chosen to perform the task of controlling the entire device. Its form factor is only a standard DIL48 socket (about 2 times 6 centimeters) which makes it easily embeddable in printed circuit boards (PCBs). The computer—a UNC90 module from FS-Forth\textsuperscript{9}—features a AT91RM9200 CPU\textsuperscript{10} with an ARM\textsuperscript{11} architecture\textsuperscript{12}. The module is clocked at 180 MHz, has a 32 MB sized flash memory where the operating system and programs are stored permanently, a 32 MB sized RAM, an Ethernet Media Access Controller, MAC\textsuperscript{13}, and physical layer transciever, PHY\textsuperscript{14} providing connectivity to standard Ethernet networks. On the 48 pins of the UNC90 module, access to the parallel bus lines of the CPU, 16 general purpose input/output (GPIO) lines, USB signals and Ethernet signals is available. Each of the 16 GPIO lines shares the same pin with special function signals such as interrupt lines, I\textsuperscript{2}C (also called two wire interface, TWI) bus and RS232 serial busses. The function of the pin can be switched between the different uses by software routines. The module can obtain its operating system code and the programs to run from different media. During development the device is mainly booted from the network over protocols that allow the transfer of programs and data such as TFTP and NFS. This allows for quick tests with new software compiled on the development host which is then directly available on the UNC module. The module can be operated the same way a personal computer is controlled over the keyboard. Possible means of control are via a serial console available on the GPIO pins or via the network. When the software has been finalized, the module can be configured to boot from its flash memory without the need for other computers that have to provide the software images.

The board's power supply provides a 3.3 V rail for the CMOS logic parts including the UNC module and a 5 V rail for the TTL logic parts. ±12 V as well as 5 V are also generated on the controller board to supply the DDS board via the bus cable. The supply rails on the bus cable power the amplification control logic on the DDS board. To make stand-alone operation of the entire device possible, an integrated 10 MHz oscillator can be placed on the controller board providing the reference clock board with the necessary frequency as an alternative to the external 10 MHz reference source.

\textsuperscript{9}http://www.digi.com/products/embeddedsolutions/connectcore9u.jsp
\textsuperscript{10}http://www.atmel.com/dyn/products/product_card.asp?part_id=2983
\textsuperscript{11}http://en.wikipedia.org/wiki/ARM_architecture
\textsuperscript{12}The architecture of a computer denotes its design class. Common architectures are for example Intel x86, PowerPC and ARM. Programs compiled for a specific architecture generally run without modification or recompilation on most processors that adhere to the architecture design.
\textsuperscript{13}The Media Access Controller, MAC, is the functional block that handles events and most of the lower level of the communication protocol on an Ethernet node. http://en.wikipedia.org/wiki/Media_Access_Control
\textsuperscript{14}The PHYceiver, or PHY, handles modulation and demodulation according to the electrical requirements of the Ethernet standard. It is at the lowest level, the physical layer, of the Ethernet protocol stack. http://en.wikipedia.org/wiki/PHYceiver
Interfacing to the LCD is accomplished directly with the parallel bus and a bus driver that converts the 3.3 V CMOS levels to 5 V TTL level signals. The LCD is mounted on the front panel and connected to the controller board with a 16-pin ribbon cable. The RJ45 Ethernet connector is accessible at the front panel. Since the Ethernet PHY of the UNC module can directly interface with the RJ45 connector no additional parts are necessary on the controller PCB.

To precisely time the FUD pulses that activate those register values which have been previously loaded via the serial bus into the DDS chip, a logic circuitry has been designed. As described in subsection 4.3.1 there are two different possible timings of an event. One is synchronization to the external trigger pulse that is generated by other hardware. The other is relative synchronization, delayed in time, with respect to the preceding event. That means that the frequency update (FUD) signal must be triggered in a switchable way by either a countdown timer (called TICK) or by the externally delivered trigger pulse.

The countdown clock source $\nu_{\text{TICK}} = 8$ kHz that provides the ticks for the relative timing of events is derived from the DDS’ internal synchronization clock which runs at $\nu_0/8 = 131.072$ MHz. That clock is pre-scaled on the DDS board by division by 128 and then on the controller board divided by a variable divisor of $2^j$, $j \in \{5, \ldots, 10\}$, $\nu_{\text{TICK}} = \nu_0/2^{3+j}$ which correspond to countdown timer frequencies from $\nu_{\text{TICK}} = 32$ kHz down to $\nu_{\text{TICK}} = 1$ kHz. The divisor exponent $j$ can be chosen at build-time of the controller board.

The external TTL trigger input on the other hand, that is used for events that are synchronized externally, is transient-filtered and equipped with protection diodes to prevent damage. Both, the TTL trigger and the TICK timer pulses are shaped by monostable multivibrators\(^\text{15}\) to pulse lengths of approximately 2 $\mu$s. The distinction of the two pulses is accomplished by gating them with GPIO lines of the controller module. The controller can thus decide whether it and the DDS are performing the next action based on a trigger signal or based on the countdown timer. Both gated signals are logically OR-ed, then gated again by another GPIO line and passed to the DDS board over a bus line. The controller module reacts based on the signal before the last gate. That allows the controller to count the ticks of the countdown without passing a tick pulse as a FUD signal to the DDS board prematurely. Before the last countdown tick the signal is then gated through to the DDS board. The timing of the FUD signal and how it causes buffer registers to become active registers is demonstrated and explained in Figure 4.3.

The layout of the board is reproduced in Figure A.6. See Figure 4.1(a) for a photo of the first version of the fully assembled controller board. Later versions will be produced professionally and also have the “green look” stemming from the solder stop mask.

\(^{15}\text{A monostable multivibrator converts every rising edge on its input signal into a pulse of specific length. http://en.wikipedia.org/wiki/Multivibrator}\)
4.3 Software

The software can be broken into three functionally separable parts which communicate with each other over well-defined interfaces. The parts are the kernel module, the server and the ExperimentWizard driver. The split approach was chosen since a modular design generally lets one exchange a software module against another without having to redesign, recompile or even restart the other modules. It was also enforced by the fact that the front-end to the user—the ExperimentWizard—software was already written and thus already functionally separate.

The software parts will be described in detail in the following sections.

4.3.1 Timing and Recipe Format Definition

Operation of the device can be classified into two modes: In the first mode single settings and parameters of the DDS board are one-by-one changed and subsequently activated. The changing of the parameters in this mode is not expected to be performed with restrictions on the timing and necessary minimum rate at which the changes can happen. This type of operation is invoked when the device is operated manually by single commands either via direct access to the embedded computer’s console, via the network protocol or via a web interface. Possible parameters that can be changed by commands are the mask of listening DDS boards (a bit-field of chip...
select signals to set), the frequency, the sweep speed, the phase offset and the output power. The interface and protocol to set the parameters in this slow mode via either commands executed on the console of the device (subsection 4.3.2) or the network protocol (subsection 4.3.3, Figure 4.5(a)) is demonstrated later.

The other mode is active when a predefined list of parameters and their respective timings is being interpreted and executed. That list is called a recipe and consists of concatenated recipe events. The recipe can be up to a few $10^6$ bytes large. At this size it can describe sweeps of all parameters at the full sampling rate over a few minutes. Since the list has a binary format, a byte order for values made of multiple bytes (endianness) has to be well-defined. The DDS chip, the ARM CPU and the default
network byte order are all big-endian\textsuperscript{16} and that endianess has been chosen for the recipe format as well. When executing a recipe, there is not much time to perform time consuming calculation on the controller board since the ARM CPU is limited in computing power in comparison with the computer running the ExperimentWizard software that controls the device. Thus, the recipe is required to consist exclusively of precomputed and sampled events where most parameter values have already been converted into the raw DDS chip format beforehand by the creator of the recipe. After the recipe has been generated it is transferred to the frequency source device over the network. How this transfer takes place is shown and explained in Figure 4.5(b) and subsection 4.3.3.

Each recipe event consists of a header byte and a variable number of body bytes. The header is always one byte large and interpreted as a bit-field of eight bits. The header byte uniquely defines the length of the body and which parameters are to be set at the event's time. The bits all have different meanings. Their exact positions and values are well-defined but qualitatively irrelevant.

- The \textit{event timing bit} defines the event's synchronization in time. An event is either synchronized to the external trigger pulse or relative to the preceding event with the help of the countdown timer.

If the event is a trigger (TRG) event, the trigger signal is gated (TRG_EN) through to the DDS and a trigger pulse is awaited. If the trigger arrives the parameters of the event that have been previously written into the buffer registers of the DDS chip during the waiting phase are activated. The output power value, which is the only value not written to the DDS chip, is sent to the digitally controlled attenuators and to the digitally controlled potentiometer upon reception of the trigger pulse.

If the event is a countdown (TICK) event, a 16-bit unsigned integer is read from the body of the event defining the delay with respect to the preceding one in units of the countdown frequency. The other parameters are then written, a countdown counting the TICKs is instantiated, the TICK signal is enabled (TICK_EN) and at the last TICK pulse also gated through (FUD_EN) to the DDS board activating the previously written settings.

- The \textit{extended commands bit} in the recipe header indicates that a 32-bit unsigned integer is to be read from the event's body and interpreted as a bit-field of 32 different actions to perform. The actions include clearing and resetting all connected DDS boards, immediately synthesizing a FUD signal and setting or clearing various configuration bits in the DDS configuration register.

\textsuperscript{16}The endianess of a byte-wise representation of a multi-byte value is either little-endian or big-endian. In the latter the most significant byte is the first. It has the lowest memory address and is transferred first over a bus. The endianess of a personal computer with an Intel chip is little-endian. \url{http://en.wikipedia.org/wiki/Endianness}
• The select bit causes a 8-bit value to be read from the body and interpreted as a mask describing the DDS boards that are to be selected for this and all following events. The corresponding chip select lines are activated or deactivated causing only the DDS boards to listen whose chip select line is active. At most 8 DDS boards can be distinguished this way. Since multiple DDS boards can be selected at the same time it is possible to set multiple DDS boards to the same parameter values at the same time saving bus time and recipe size.

• If the frequency bit is set, a 32-bit frequency tuning word is read from the body of the event and written to the DDS board. All listening DDS chips then write the frequency tuning word into their buffer register and activate it upon reception of the FUD signal.

• The differential frequency tuning and the differential ramp rate word bits cause signed 32-bit and unsigned 16-bit values to be read from the body and passed on to the listening DDS boards. The instantaneous linear sweep rate is determined by them.

• The phase offset bit signifies that a 16-bit unsigned integer is to be read and passed on to the DDS boards.

• The output power bit triggers the read of a 16-bit unsigned integer, which is looked up in the calibration table. The resulting parameters for the switchable attenuator sets and the digital potentiometer are saved and activated upon reception of the respective synchronization pulse.

4.3.2 Kernel Module

Most higher operating systems have a notion of kernel space versus user space. Program code is executed in either. In operating systems where the driving of the various hardware devices is not done in user space, direct communication with the hardware is only allowed from within kernel space. That paradigm enforces clear distinction between trusted low-level hardware code in the kernel on one side and untrusted arbitrary user-space code on the other. The user-space code may only exercise well-defined interfaces to the kernel but is portable across operating systems. Code running in kernel space has to obey rules to not endanger the stability of the system such as not blocking the CPU for too long. Kernel space has the advantage of all freedom with respect to what is done with the hardware. The implication is that tasks that are time-critical and cannot afford to go through an interface to the kernel mandate their implementation in kernel space.

The interfacing with the DDS board and the FUD logic as well as the time-critical recipe playing parts have been implemented in a kernel module. The module then provides a stack of abstraction layers around those operations ranging from single GPIO setting and clearing functions to higher level functions such as register writes over the bus and handling of the recipe buffer. Only the highest level of abstraction is
directly visible to user space in the form of a device file that interprets all data written to it as a recipe stream. Additionally a set of file-like attributes that each interpret the data written to them as a single value for a parameter (such as frequency, sweep speed and power) is offered. The device file interface is used when a recipe consisting of complex pulses and sweeps is interpreted. The attributes interface is used when single parameters are set. Streaming a recipe to the device and writing values to the attribute file can be done directly via commands executed at the command line of the embedded computer.

4.3.3 Protocol Server

The commonly used way of passing a recipe or single parameters to the device is via a network protocol that is exercised by a server process. It runs as a program in user space on the device and connects the kernel module interface to the network. It also serves as a means of enforcing exclusive access to the device. Concurrent access would cause in unpredictable results. The communication with the server is a simple text-based protocol which is transferred over TCP/IP. The protocol is based on the File Transfer Protocol, FTP. A session of setting simple attributes can look like in Figure 4.5(a). The possibility to use common general-purpose tools and simple textual commands to access and control the device demonstrates the simplicity of the protocol. The available commands have self-explaining names and are FREQ: SET, AMP: SET, PHASE: SET, SWEEP: SET, RECIPE: SET, RECIPE: START, RECIPE: STATUS, RECIPE: STOP and QUIT. The server answers every command with a status code. In the examples the status codes 200 means successful execution, and 221 means terminating state. Following the return code, a line describing the result of the executed command in a textual form is transmitted. The commands expect either zero, one or two numerical arguments. SET: SWEEP expects two arguments, while QUIT, RECIPE: START, RECIPE: STOP and RECIPE: STATUS expect zero. The RECIPE: SET command is special in the sense that reads as many bytes as specified by the argument after having received the command, Figure 4.5(b). The data is only checked for the correct length but not for correct or valid content. The recipe gets buffered in memory after having been set and is written to the recipe device upon reception of a RECIPE: START command.

4.3.4 Python Recipe Generator

Owing to the need for a rapidly extensible and modifiable tool that can be used during development of the kernel module recipe parser and during characterization and benchmarking of the device, a script written in the programming language Python has been designed. Python is an interpreted high-level programming language that has a rich set object-oriented programming tools and is well-equipped for rapid ap-
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# nc qo-cdds1-transport 4711
> FREQ:SET 80000000
< 200 freq set to 80000000.
> PHASE:SET 8192
< 200 phase set to 8192.
> QUIT
< 221 goodbye.

(a) Setting parameters.

Figure 4.5: Two examples of communication with the device using the text-based network protocol. Lines starting with # are commands executed on the development host. The nc command is used to connect to the device. nc is short for netcat, a tool to quickly explore services on a network that are exposed over TCP/IP ports. qo-cdds1-transport is the host name of the device and 4711 is the TCP/IP port number taken from a region of free/reserved ports assigned by the IANA, http://www.iana.org/assignments/port-numbers. Those lines starting with > denote data sent to the frequency source and lines with < are responses that are received from it. Text in parentheses is an abstract description of what happens at a given point.

plication development and prototyping. Due to Python’s slowness when it comes to long iterative calculations the script is not suitable for the generation of minute-long recipes at full sampling rate. But for evaluating new ideas and fine-tuning the definition of the recipe its flexibility has proved to be extremely worthy. The first implementation of the sweeping algorithm (described in detail in subsection 4.3.6) and the first recipe parser were incarnated in the Python recipe generator and later ported to the ExperimentWizard and to the kernel module respectively.

4.3.5 ExperimentWizard Driver

When operated in the final experimental environment, the frequency source device will receive its commands from the software controlling the entire experiment. That software was written by Thilo Stößerle in Borland C++ [26] and has been modified and extended to be able to operate the DDS device.
Figure 4.6: The upper screenshot shows the DDS related channels in the Experiment-Wizard software. The DDS device with two DDS boards on the bus appears as a set of six channels. Two for the frequencies, two power levels and two phase offset channels. DDS device parameters such as the resolution of the sweeps and the location of the device in the network are adjusted in the device parameters dialogue which is accessed through the hardware menu as shown in the screenshot in the lower left. The sweep dialogue is accessed by clicking on the desired channel at the desired timing edge. The formula that describes the sweep can then be edited and previewed.
The ExperimentControl software’s appearance is a matrix-like grid that contains in the horizontal direction timing edges describing the timing of actions of the devices and in the vertical direction the different channels that are provided by the devices. The user interface to the device as part of the ExperimentControl software is shown and described in Figure 4.6. Upon queueing a new experimental run description for execution, the recipe is generated by sampling the channels. For the frequency channels sweeps are generated as described in the following section. This way the sampled frequency values are connected by linear sweeps. The recipe is then sent to the DDS device and the latter is started by a trigger pulse together with the other devices.

### 4.3.6 Sweep Algorithm

The frequency channel of the recipe consists of sampled frequency events with linear sweeps in between. Such a possible linear frequency sweep may be to sweep by $\Delta f$ in the time interval $\Delta t$. The sweep speed is then $\Sigma = \Delta f / \Delta t$. For the present applications there is requirement for sweeps anywhere in the interval $|\Sigma| \in [1 \text{ Hz}/1 \text{s}, 500 \text{ MHz}/100 \mu\text{s}]$. The interval corresponds to a dynamic range of more than 13 decimal or 42 binary orders of magnitude. While all those sweeps have to be realized as smoothly as possible, the DDS chip can only sweep in a stair-stepped way. The quantization is due to the digital nature of the chip. The presently used DDS chip can sweep in units of $\sigma_0 = \nu_0^2 / 2^{32+3}$ which amounts—in the current configuration—to $\sigma_0 = 64 \text{ MHz}/\text{s}$.

The ratio between differential frequency tuning word DFTW and differential frequency ramp rate word DFRRW determines the sweep. The two registers’ values are bounded integers with the ranges $\text{DFTW} \in [-2^{31}, 2^{31} - 1]$ and $\text{DFRRW} \in [0, 2^{16} - 1]$. The sweep speed is then $\sigma = \text{DFTW} / \text{DFRRW} \sigma_0$.

“Smooth” as used above needs to be defined more precisely: A sweep can be considered smooth if there are no frequency jumps $\delta f$ during the sweep larger than a given maximum $\delta f_{\text{max}}$. An additional requirement is that the accurate but rough sweep $\Sigma$ which would consist of only one frequency jump $\Delta f$ after the time $\Delta t$ is represented as precisely as possible by the smooth sweep $\sigma = \text{DFTW} / \text{DFRRW} \sigma_0$. The smooth sweep consists of $\Delta f / \delta f$ small frequency jumps of size $\delta f$.

\[
\delta f = \nu_0 \frac{\text{DFTW}}{2^{32}}, \quad \Delta f / \delta f = 2^{32} \Delta f / \nu_0 \text{DFTW}. \tag{4.3}
\]

The jumps are separated by $\delta t$:

\[
\delta t = \frac{\text{DFRRW}}{2^{31} \nu_0}, \quad \Delta t / \delta t = 2^{31} \Delta t \nu_0 / \text{DFRRW}. \tag{4.4}
\]

The maximum tolerance be $\varepsilon_{\Sigma}$. The smoothness and precision conditions are then:

\[
\delta f < \delta f_{\text{max}} \quad \text{and} \quad \frac{\Sigma - \frac{\text{DFTW}}{\text{DFRRW}} \sigma_0}{\Sigma} < \varepsilon_{\Sigma}. \tag{4.5}
\]
4.3. Software

Figure 4.7: A graphical visualization of how the convergents for \( e - 2 \approx 0.718281 \) approach the precise value. The first five convergents are 0/1, 1/1, 2/3, 3/4, 5/7. The space of integer fractions is shown in the figure as circles. The solid blue line denotes the place of precise representations of \( e - 2 \), namely the ray \( p = (e - 2)q \), the green one is the path that is taken by the convergents while approximating the precise value. The corridor between the dotted red lines visualizes the decreasing error of the convergents. [27]

A beautiful mathematical tool that can be used to approximate the positive real number \( x \) using rational fractions \( n/d \) is readily available: the continued fraction representation of \( x \) which is defined as

\[
x = a_0 + \cfrac{1}{a_1 + \cfrac{1}{a_2 + \cfrac{1}{\ddots}}}.
\]  

(4.7)

The \( a_i \) are all positive integers called the partial quotients. In an abbreviated notation we can write

\[
x = [a_0, a_1, a_2, \ldots].
\]  

(4.8)

The partial quotients \( a_i \) for the continued fraction representation of the real number \( x \) are easily found iteratively using their recurrence relation:

\[
r_0 = x, \quad i \geq 0,
\]  

(4.9)

\[
r_i = \frac{1}{r_{i-1} - a_{i-1}}, \quad i > 0,
\]  

(4.10)

\[
a_i = \lfloor r_i \rfloor.
\]  

(4.11)

\( \lfloor \cdots \rfloor \) denotes the floor function.
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The fully reduced fraction $p_k/q_k$ that is obtained from the first $k$ terms of a continued fraction for $x$, $p_k/q_k = [a_0, a_1, a_2, \ldots, a_k]$ is called the $k$th convergent.\footnote{Continued fractions and convergents have many uses. One—see [27] for more—is finding near commensurabilities of events with different periods such as the metonic cycle. This cycle has been discovered by the Greeks and is used in the Hebrew calendar and in the calculation of the date of Easter. It consists of 235 lunar periods ("months") which almost coincide with 19 solar periods ("years"): $235/19$ is the sixth convergent of the precise ratio of the lunar month and solar year $365.2425/29.53059$. With a year spanning 12 months, 7 leap months have to be inserted in 19 years: $235 = 19 \times 12 + 7$.} The convergents $x_i = p_i/q_i$ for a given real number $x$ can be found in the following iterative way [27] which is especially useful for computers. How this scheme works can also be demonstrated visually as in Figure 4.7. First define the starting values

$$
p_{-2} = 0, \quad q_{-2} = 1, \tag{4.12}
$$
$$
p_{-1} = 1, \quad q_{-1} = 0, \tag{4.13}
$$
$$
p_0 = a_0, \quad q_0 = 1. \tag{4.14}
$$

Then iteratively all other convergents are obtained from the continued fraction $[a_0, a_1, \ldots]$ by the recurrence relations

$$
p_i = a_ip_{i-1} + p_{i-2}, \tag{4.15}
$$
$$
q_i = a_iq_{i-1} + q_{i-2}. \tag{4.16}
$$

To judge the quality of a convergent, the following two assertions have been proved by Serge Lang [28]: The $p_i/q_i$ are the best approximations for $x$ in the following sense:

1. $p_i/q_i$ is the best approximating fraction of all $p'/q'$ with $q' \leq q_i$. For any $q' \leq q_i$ and any integer $p'$ it holds that $|x - p_i/q_i| < |x - p'/q'|$.

2. $p_i/q_i$ is the first fraction after $p_{i-1}/q_{i-1}$, that is a better approximation for $x$. $q_i$ is the smallest of the integers $q' > q_{i-1}$ such that $|x - p'/q'| < |x - p_{i-1}/q_{i-1}|$ for any $p'$.

The iterations for the partial quotients $a_i$ and for the convergents $p_i/q_i$ can be interleaved and aborted when the precision is sufficient without having to calculate superfluous terms. This algorithm is used in the Python recipe generator and in the ExperimentWizard driver for the frequency source to find the pair DFTW/DFRRW for a given sweep.
Chapter 5

Characterization of the Device

During the design and while finalizing the first prototype of the devices several tests and measurements were performed. The parts that were analyzed range from single elements such as the low-pass anti-aliasing filter to the entire device for measurements of the beat between two outputs. The functional blocks of the frequency source were tested one by one at a component level or as a part of the entire device where appropriate. In this chapter the most important of these tests and their results are presented. The tests show that the frequency source fulfills the specifications and even exceeds many of them.

5.1 Interrupt Latency

The performance of the embedded computer controller module has two different aspects. One is its raw speed which is important when big amounts of data have to be handled quickly. The overall maximum speed of the controller module is not very critical and has been seen to be sufficient for handling long frequency and amplitude sweeps at high resolution. The other aspect is how quickly it reacts to external stimuli and how well it manages to adhere to the timing restrictions of the individual recipe events. The delay between the stimulus of the embedded computer—for example an interrupt—and the first reaction to it is the latency. In the present case the interrupt can be caused by the countdown tick timer or by the trigger as described in the definition of the recipe in subsection 4.3.1. This timing, however, does not determine the timing precision of the output signal. Changes of the output signal are synchronized directly to the frequency update signal without any involvement of the embedded computer. The FUD timing latency relevant for the synchronization of the output signal will later be shown to amount $318 \pm 4$ ns in section 5.5. It is important, however, that an interrupt caused by the FUD pulse is handled before the next one arrives. Otherwise synchronization with the rest of the experiment is lost and all future events that are time-based will be delayed. The latency varies depending on whether at the time of the stimulus another part of the kernel blocks and prevents interrupts from being handled. It also depends on the load placed onto the device. Factors increasing the load can be high network traffic or many active processes running on the computer.
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Figure 5.1: Latency measurement. The picture is a visually superimposed sum of many traces and results from interrupting the UNC at a frequency of 10 kHz which can be seen on channel 2 (red). The figure shows an accumulation of more than 800,000 traces of a burst of 100 hypothetical SPI clock cycles (blue) as a response to the interrupt. The minimum—and also most frequently occurring—delay to the interrupt is 1.8 $\mu$s. The maximum delay observed over 800,000 interrupts is 50 $\mu$s. A number of recipe events correspond to 100 seconds of full-resolution recipe data that are handled without a glitch. Note that none of the responses to the first interrupt reaches into the next interrupt.

Figure 5.1 shows a typical measurement of the interrupt latency. The UNC module is interrupted roughly every 100 $\mu$s and its goal is to respond to the interrupt with a characteristic sequence of pulses. The response consists of 100 pulses on a GPIO line and simulates a real communication with the DDS board. Such communication bursts occur when streaming a recipe to the DDS board. Sufficiently quick handling of the interrupts is given when the response happens before the next interrupt arrives. As can be seen in the figure even for a large number and high rate of interrupts it is ensured that the entire communication cycle always finishes before the respective FUD signal and time synchronization is not lost. In further measurements, it has also been confirmed that the latency is still sufficiently low even if an additional synthetically generated network load increases the interrupt pressure on the device.

Assertions about the speed of the serial bus can also be made on the basis of the trace. Transferring 100 bits over the serial bus needs 32 $\mu$s. A single bit can then be
5.2. Properties of the Anti-Aliasing Filter

The anti-aliasing filter determines the suppression of images of the desired carrier frequency that lie above the Nyquist frequency. It is desirable that its transfer function is as flat as possible in for all frequencies from zero up to the Nyquist frequency and then falls as steeply as possible in order to suppress aliases. A measurement of the transfer function is reproduced in Figure 5.2. The filter properties ensure low distortion of the carrier frequency and at the same time few spurious components and aliases. The effect of the filter on a realistic output frequency spectrum is described in the following section.

Figure 5.2: Low-pass characteristic of the anti-aliasing filter. The figure shows the attenuation (on the vertical axis) of a range of frequencies passing through the filter. Frequency components of the output signal that lie above the Nyquist frequency at 524 MHz are attenuated by at least $-20$ dB while frequency components in the usable frequency range up to the 470 MHz do not suffer a loss of more than $-5.1$ dB. The markers show a $-2.3$ dB loss at 400 MHz and the said $-5.1$ dB loss at 470 MHz. The attenuation above the Nyquist frequency at 524 MHz is better than 500 dB/octave.
Figure 5.3: Spectra of a 80 MHz output signal with a 12 dBm carrier power at different window widths and resolution bandwidths. The most predominant spurious frequencies are the fundamental harmonics \( n \times 80 \text{ MHz} \) where \( 2 \times 80 \text{ MHz} = 160 \text{ MHz} \) is the largest component at about \(-40 \text{ dBc}\). In the narrow bandwidth plots the peaks at 80 MHz \( \pm n \times 50 \text{ Hz} \) hint to an amplitude or phase modulation pertaining to the mains frequency.

5.3 Characterization of the Output Spectrum

In this measurement the spectra of the output from the device are analyzed. Special attention has to be given to spurious frequencies and spectral purity of the signal. In Figure 5.3 spectra of different resolutions of an output frequency of 80 MHz are shown. The frequency has been chosen as a single example since it is the frequency that is used in the cavity experiment to drive the acousto-optical modulators for the standing-wave transport.

The upper spectrum in Figure 5.3(a) shows a wide frequency range from 0 Hz to 3 GHz. Apart from the desired component at \( f = 80 \text{ MHz} \) a few spurious frequencies can be observed. The most prominent are the harmonics at \( n f = n \times 80 \text{ MHz} \), especially the second and third harmonic at 160 MHz and 240 MHz respectively. The most powerful is 160 MHz with a power level of \(-28 \text{ dBm}\) corresponding to \(-40 \text{ dBc}\) (relative to the carrier). Other components that can be identified are \( v_o/2 = 524 \text{ MHz} \),
\[ \nu_0/8 = 131 \text{ MHz}, \ \nu_0/2 - f = 444 \text{ MHz and } \nu_0 + 3f = 1.29 \text{ GHz}. \]

The power in each of these spurious components is always sufficiently below the carrier power.

The second spectrum in Figure 5.3(a) demonstrates the narrow-band components of ±1 kHz around the carrier. The most visible parts of the spectrum are a background of phase noise at −75 dBC and spurious components at 80 MHz ± n × 50 Hz. Especially the third harmonic at 80 MHz ± 150 Hz is visible. These frequencies stem most probably from amplitude modulation by the mains power frequency crosstalk through the power supply. That amplitude modulation can either happen at the reference clock source or at the amplification stage on the DDS board.

5.4 Amplifier Calibration

As was already mentioned before, the DDS board initially contained a regulated amplification stage that involved a logarithmic detector to compare the output power with a desired logarithmic power level. The first revision of this power control circuit showed some severe ringing of the power level. As a work-around the circuit had to be heavily damped making its response to changes in the desired output level slower than 500 ms. That speed is not sufficient to play a well-resolved power profile since steep edges in the profile would be washed out. The circuit was then modified to not regulate the power logarithmically but only control it linearly. In order to compensate for the non-flat frequency response of the amplifier and attenuation circuit calibration profiles have been recorded as shown in Figure 5.4. Converting this data into a power correction factor \( \gamma \) that depends on the output frequency \( f \) and on the desired output level \( p \), a two-dimensional look-up table \( \gamma(f, p) \) has been created and integrated into the device. This calibration look-up table returns the required control voltage for the desired output power \( p \) at a given frequency \( f \).

At high attenuations (low power levels) an undesirably strong dependence of output power on the frequency around 20 MHz is clearly seen. Apart from this artifact there is another problematic behaviour at low frequencies which is not seen in the plot. At around 20 MHz the harmonics of the output frequency become very strong. Some amount to −10 dBC hinting to a severely non-linear transfer function of either the amplifier or the attenuator.

Although a calibration table was successfully generated and implemented from the given data, the entire power control circuit has been deactivated after further measurements since the final application of the prototype device was the control of the acousto-optical modulators. In that setup another method of power regulation was already implemented making the one implemented on the DDS boards superfluous. It was thus decided to bypass the device's own power control. The output power characteristic of the version without power control is shown in the black curve in Figure 5.4.

In the following sections it will be noted whether the measurements were performed with a device where the power control was active or not.
Figure 5.4: DDS output power in dependence of the attenuator control voltage. Each of the colored lines shows the output power depending on the output frequency for a given control voltage of the attenuator. The output power in dBm shows an approximately logarithmic dependency on the control voltage and the latter an offset of 0.9 V. The version of the DDS board with the voltage controlled attenuator includes two amplifiers (14.4 dB each) and one attenuator (−55 dB to −3 dB). The uncontrolled version includes just one amplifier and no attenuator. Its output power is shown as the black line.
5.5 Frequency Profile and Timing

A big advantage of the present frequency source is its ability to play long and complex frequency profiles. A very critical point in this context is what happens at the times when the frequency is turned on or off. At those times the generated frequency switches from zero to the desired value or back.

Figure 5.5 shows the case of the dual DDS device switching on a frequency of 400 MHz. The difference in symmetry and behaviour is caused by different designs of the two DDS boards. The blue signal originates from the DDS board with the attenuation circuit and the second amplifier still intact while the red signal originates from the other DDS board whose amplification stage only consists of one amplifier and no attenuator. It is clearly visible that the overshoot is caused before the amplifiers since its polarity changes with the number of amplifiers present. Each amplifier inverts the signal once.

The source of the overshoot can most probably be found in the current sinking DAC and transformer combination. With the default values of the configuration registers of the DDS chip, the output signal shape signal is a cosine. A cosine has maximum amplitude at zero time. Since the transformer and the circuit behind the DAC—such as the filter and the capacitors used to decouple the amplifiers—are not yet loaded by the signal the DAC has to produce a very high voltage to drive the desired current through the transformer’s primary coil at the time of switching on. On the secondary side of the transformer the high voltage during the loading phase of the transformer is visible as an overshoot. The overshoot decays according to the cutoff frequency of subsequent elements which is around 1 to 10 MHz depending on the amplifier configuration.

This transient behaviour would make the device unusable for the direct generation of short pulses. A workaround is having the device start generating the signal long before it is gated on by an additional radio frequency switch. The transient behaviour can indeed be fully avoided if the beginning of the signal lies on a zero-
crossing of the output signal. The result is shown in Figure 5.6(a) for the case of switching on a sinusoidal output frequency of 80 MHz and in Figure 5.6(b) for the case of switching off the signal. Starting with the signal at a zero crossing clearly avoids the transient effects that are observed in the cosine shaped case.

Figure 5.6 also serves well to demonstrate the quality of the timing of the recipe events. The time axis in the figures is relative to the rising edge of a TTL level trigger pulse. The traces show a delay with respect to the trigger of 317 ns and 320 ns respectively. The difference is to be attributed to the frequency updates being synchronized to the synchronization clock ticking at time intervals of $8/\nu_0 = 7.6 \text{ ns}$ as previously shown in Figure 4.3. Since the TTL trigger can happen at an arbitrary time with respect to the phase of the synchronization clock, the delay to the rising edge of the TTL pulse jitters by the length of such a clock cycle. The minimum delay to the trigger pulse is caused by the sum of all propagation delays through the TTL filtering, shaping and gating logic. It can easily be compensated for by triggering earlier. The jitter can be controlled and compensated for by enforcing a synchronization of the trigger to the synchronization clock and by resetting the synchronization clock divider at the begin of the experiment.

### 5.6 Phase Calibration

Having two DDS board in one frequency source device permits generation of two frequencies with a given phase relation. But manufacturing tolerances or different
5.6. Phase Calibration

Revisions of the DDS boards may result in different output phases \( \phi_1(f_1) \) and \( \phi_2(f_2) \) of the two boards that may also depend on the output frequency. In order to be able to produce two signals with a known phase relation it is necessary to know the difference between the output phases of the two DDS board. Using the dual-DDS board device with one board having the simplified uncontrolled amplifier and the other using the controlled combination of attenuator and two amplifiers, the following measurements have been performed:

The two DDS boards’ output two frequencies \( f_1 \) and \( f_2 \). The boards’ signals \( U_1 \) and \( U_2 \) include the respective output phase shifts \( \phi_1(f_1) \) and \( \phi_2(f_2) \). The first board may additionally have a variable but known phase offset \( \Delta \phi \). Both signals,

\[
U_1 = \cos \left[ 2\pi f_1 t + \phi_1(f_1) + \Delta \phi \right], \quad U_2 = \cos \left[ 2\pi f_2 t + \phi_2(f_2) \right],
\]

were multiplied in an electronic mixer yielding a product signal of

\[
U_1 U_2 = \frac{1}{2} \left\{ \cos \left[ 2\pi (f_1 - f_2) t + \phi_1(f_1) + \Delta \phi - \phi_2(f_2) \right] + \cos \left[ 2\pi (f_1 + f_2) t + \phi_1(f_1) + \Delta \phi + \phi_2(f_2) \right] \right\}.
\]

With the difference frequency set to zero, \( f_1 = f_2 = f \), and after filtering out the high frequency component \( \cos(4\pi ft + \cdots) \) with the help of a low-pass filter, only the phase part due to the phase difference remains:

\[
U' = \frac{1}{2} \cos \left[ \phi_1(f) - \phi_2(f) + \Delta \phi \right].
\]

In Figure 5.7 such a measurement of the beat voltage \( U' \) is shown. Both DDS boards provide a \( f_1 = f_2 = f = 40 \text{ MHz} \) output signal and the phase offset of one board was incremented in time by steps of \( 2\pi/2^3 \), \( \Delta \phi = n2\pi/2^3 \). To visually mark the point where the phase offset word difference \( \Delta \phi \) between the two boards was zero, a marker was generated that can be seen at the left and right side of the graph. In order to obtain a phase offset value \( \phi_1 - \phi_2 \) for a given frequency \( f \), the beat voltage must be averaged over each step and a cosine fitted to the points yielding the phase offset. The value should be around \( \phi_1 - \phi_2 = \pi \) due to the one board having one inverting amplifier more than the other.

The phase difference \( \phi_1 - \phi_2 \) is not expected to be the same for all frequencies \( f = f_1 = f_2 \) since the parts involved may have different frequency dependencies in their phase shifts. This is especially true for the present case of two different amplifier and attenuator configurations: the additional amplifier and attenuator pair on one board causes an frequency dependant phase shift. It is thus necessary that the phase offset calibration be performed for multiple frequencies.

This measurement demonstrates that the relative phase between two DDS outputs can be precisely determined and calibrated. It also shows that the DDS boards’s frequencies are very stable. Each unwanted phase jump would be visible in the phase difference signal.
Figure 5.7: Phase difference signal obtained from the DC component of the mixed output of two synchronized DDS boards providing 40 MHz each. The steps are phase offset increments of $2\pi/2^5$. Due to one DDS board being equipped with the power control circuitry while the other one was not, the first board contains one amplifier more which inverts the signal.

5.7 Frequency Sweep and Beat

In the context of atoms transport in a standing light wave a more thorough analysis of the beat between two DDS boards during a frequency sweep is indicated. As already seen in section 2.6, the transport distance is directly proportional to the phase shift that is accumulated between the two frequencies during the transport. To guarantee a positioning precision on the sub-wavelength scale, the accumulated phase shift between the two frequencies must be controllable with an accuracy of better than $2\pi$. Not only this integral phase error but also the differential phase error has to be kept small. Phase jumps correspond to a wide frequency spectrum that causes unwanted heating.

Figure 5.8 shows a frequency sweep similar to those that will be used in the transport of $^{87}$Rb in a standing light wave in section 6.1. The two DDS boards provide frequencies that are amplified and fed into an AOM shifting the frequency of the light in the first-order beam by the radio frequency. A standing wave is created by superimposing the two beams. The interference pattern and with it the dipole potential are only static if both DDS outputs are of the same frequency. If they produce different frequencies $f_1(t)$ and $f_2(t)$, the speed $v(t)$ of the interference pattern is directly proportional to the difference frequency $\Delta f(t)$ between the two DDS. The speed $v(t)$ and
5.7. Frequency Sweep and Beat

(a) The phase error $|\phi_{\text{err}}(t)| = |\arcsin(U_{\text{data}}(t)/U_0) - \arcsin(U_{\text{fit}}(t)/U_0)|$ between the measured phase and the phase as obtained from the fit is shown in green. A frequency measurement obtained from the 150 point Fourier transform and the instantaneous frequency of the fit are shown in red and blue respectively.

(b) Beat phase and fit at the beginning of the sweep.

(c) The point of highest difference frequency $\Delta f_{\text{max}} = 200$ kHz.

(d) End of the sweep where the difference frequency returns to zero.

Figure 5.8: Analysis of the beat signal between two DDS boards. One DDS produces a constant 80 MHz output while the other performs a cosine-shaped sweep in 20 ms from 80 MHz to 80.2 MHz and back to 80 MHz. Shown in the graphs are the measured values of phase (lower row) and difference frequency (upper graph) in red as well as the fit in blue. The upper graph also shows the phase error relative to a fit.
distance $x(t)$ realized during a transport that started at $t_0$ are

$$\nu(t) = \Delta f(t) \frac{\lambda}{2}, \quad (5.4)$$

$$x(t) = \int_{t_0}^{t} \nu(t') \, dt' = \frac{\lambda}{2} \int_{t_0}^{t} \Delta f(t') \, dt'. \quad (5.5)$$

The last integral is the number of beats between the two DDS. The time evolution of the two frequencies as used in the transport are

$$f_1(t) = f_0, \quad (5.6)$$

$$f_2(t) = f_0 + \frac{1}{2} \Delta f_{\text{max}} \left( 1 - \cos \frac{2\pi(t - t_0)}{T} \right), \quad (5.7)$$

$$\Delta f(t) = f_2(t) - f_1(t). \quad (5.8)$$

With (5.5) the transport distance for a transport of length $T$ is

$$x(t_0 + T) = \frac{\lambda}{2} \int_{t_0}^{t_0 + T} \Delta f(t') \, dt' = \frac{1}{4} \lambda \Delta f_{\text{max}} T. \quad (5.9)$$

To analyze such a transport, one could overlap the two laser beams on a photo diode and observe the signal on an oscilloscope. This corresponds to a measurement of the potential of the standing wave at a certain place. An alternative is to mix the two DDS boards’ frequencies electronically and observe the low-frequency component as was already done in section 5.6 to calibrate the phase difference. The equations (5.2) and (5.3) were obtained for the beat signal of static frequencies. For the case of two frequencies $f_1(t)$ and $f_2(t)$ that vary in time one obtains for the beat voltage:

$$U(t) = U_0 \cos \left\{ \int_{t_0}^{t} \Delta f(t') \, dt' + \phi_0 \right\}$$

$$= U_0 \cos \left\{ \pi \Delta f_{\text{max}} \left[ (t - t_0) - \frac{T}{2\pi} \sin \frac{2\pi(t - t_0)}{T} \right] + \phi_0 \right\}. \quad (5.10)$$

The parameters for the sinusoidal frequency sweep used as an example here are:

$$T = 20 \, \text{ms}, \quad (5.11)$$

$$\Delta f_{\text{max}} = 200 \, \text{kHz}. \quad (5.12)$$

$U_0$, $\phi_0$, $f_0$ and $t_0$ are arbitrary. In Figure 5.8 (b)—(d) the measured beat voltage is shown as well as the results of a non-linear least-squares fit. The following parameters
were obtained from the fit with (5.10):

\[
U_0 = 1.220(3) \, \text{V}, \\
T = 20.0000(1) \, \text{ms}, \\
t_0 = 5.96615(4) \, \text{ms}, \\
\Delta f_{\text{max}} = 199.999(1) \, \text{kHz}, \\
\phi_0 = -0.295(3) \, \text{rad}.
\] (5.13-5.17)

The phase difference between measured sweep phase and the curve obtained from the fit is presented in Figure 5.8(a). The mean phase error is 0.058 rad and its maximum is 0.45 rad. That shows that the fit is really at the global residual minimum of parameter space. Since the phase error does not grow above 2\pi, the claim of sub-wavelength precision can be held.

The reduced $\chi^2$,

\[
\frac{\chi^2}{\nu} = \frac{1}{N_{\text{data}} - N_{\text{fit}}} \sum_i \frac{(U_{\text{data}}(t_i) - U_{\text{fit}}(t_i))^2}{\sigma_i^2}.
\] (5.18)

is a useful measure for the quality of such a fit. $U_{\text{data}}(t_i)$ and $U_{\text{fit}}(t_i)$ are the beat voltage values of the measurement and the fit respectively. $\sigma_i = 10 \, \text{mV}$ is the error of the beat voltage measurements, $\nu = N_{\text{data}} - N_{\text{fit}}$ denotes the number of degrees of freedom, $N_{\text{data}} = 10 000$ the number of data points and $N_{\text{fit}} = 5$ the number of free parameters of the fit. The fit is characterized by

\[
\frac{\chi^2}{\nu} = 116 \gg 1. 
\] (5.19)

Such a large reduced $\chi^2$ hints to an insufficient model. But that can be explained: The linear sweeps of which the cosine shaped sweep consists, have a structure that is can not be represented in the smooth model.

A second method to characterize the transport sweep is to determine its instantaneous frequency. The instantaneous frequency of the beat voltage is just the difference frequency between the two DDS boards as has been shown in (5.3). One can obtain this instantaneous frequency by calculating the Fourier transform of a moving window of the beat voltage data. The frequency value associated with the component of maximum amplitude of the Fourier transform is the instantaneous frequency. The Fourier transform is the limiting factor of this type of measurement. The resolution of the frequency grows with the window size but the time resolution of that frequency gets lower. A $n$ point Fourier transform resolves $n$ distinct frequency values. At 500 000 samples per second, the $n$th frequency corresponds to 500 kHz. In the range from zero to $f_{\text{max}} = 200$ kHz only 60 distinct frequencies can be resolved with a 150 point transform. Higher resolution has been obtained by calculating the weighted average of adjacent frequency values in the Fourier transform. Figure 5.8(a) shows the result of such a measurement. The curve is the weighted average frequency.
of the Fourier transform of a Hamming window of $n = 150$ points around a given time point.

The third way to analyze the sweep is to simply count the number of beats $p$ corresponding to the number of pulses or zero crossings in the plot of the beat voltage. For the given two frequency profiles the number is 2000 which coincides with the calculated value:

$$p = \int_{t_0}^{T} \Delta f(t') \, dt' = \frac{1}{2} \Delta f_{\text{max}} T = 2000. \quad (5.20)$$
Chapter 6

Experimental Evaluation

6.1 Transport of Atoms in a Standing Light Wave

The first experimental application of the frequency source proved to be a very demanding one that exercised all critical features of the device. Parallel to the design of the DDS frequency source, an optical conveyor belt was in the process of being implemented in one of the two experimental setups of the quantumoptics group. The conveyor belt transports atoms from the place of the BEC into the high-finesse optical cavity that is used detect and interact with the atoms. The experimental apparatus as well the cavity are described in detail in [21]. The apparatus is especially interesting since it combines cavity quantum electrodynamics (QED) and BECs. This combination has given rise to a series of interesting new experiments with coherent matter waves [29], counting statistics [30, 31] and matter and light in the strong coupling regime [31, 29]. The standing wave transport that has been built will add new possibilities to the apparatus such as repeated interaction of the same atoms with the cavity or interaction over longer periods of time.

During the design and construction of the lasers and optics for the standing light wave conveyor belt, the conclusion has been drawn that the commercial frequency sources that were planned to be employed are incapable of generating sweeps of sufficient smoothness and resolution. After the characterization of the first prototype of the DDS frequency source it became clear that this device could accomplish the task of generating the desired frequencies. The first prototype was then equipped with a second DDS board and integrated into the BEC transport experiment to control the standing light wave. While currently the experimental setup is still in a state of flux, the first measurement are already available and permit a preliminary presentation of the properties of the transport.

The experimental procedure begins with the creation of a BEC of some $2 \times 10^6$ atoms of $^{87}\text{Rb}$ by standard means. The BEC is held in a Ioffe-Pritchard magnetic trap in the $|F = 1, m_F = -1\rangle$ hyperfine ground state 36 mm above the high-finesse optical cavity. The trapping frequencies of the magnetic trap are $(\omega_x, \omega_y, \omega_z) = 2\pi \times (39, 7, 29)$ Hz where $z$ denotes the vertical axis.

In order to transport the atoms, a pair of counterpropagating laser beams creates an interference pattern that acts as a potential. Since the frequencies of the two
Chapter 6. Experimental Evaluation

Figure 6.1: Absorption pictures of an atom cloud after a different transport distances. The initial position of the atoms in the magnetic trap is at the left while gravity points to the right. The black bar in the lower right serves as a scale of 200 µm length. All transports were performed in 200 ms. Then the cloud was held in the standing wave trap for 365 ms before the absorption picture was taken. The picture shows condensates transported by different distances of $\Delta z = n \times -0.625 \text{ mm}, n \in \{0, \ldots, 6\}$ into the direction of the optical cavity (to the right side of the picture).

Beams can be controlled precisely, the potential can be accelerated in the axial direction. The principles of transport in the standing light wave are depicted in Figure 2.5 and described in section 2.6. The two counterpropagating transport beams have a wavelength of $\lambda = 850 \text{ nm}$ and a power of approximately 90 mW. They are optically shaped in such a way that their common focus is located in the cavity and has beam waists of $(w_x, w_y) = (30, 60) \mu m$.

By ramping up the beam power to their full intensity, the BEC is transferred from the magnetic trap—which is later ramped down—into the standing wave trap. After loading the atoms into the standing wave, the difference frequency between the two laser beams is increased resulting in a movement of the interference pattern downwards in the direction of the cavity with a speed proportional to the difference frequency. At half the final transport distance the difference frequency is lowered and the atoms are decelerated until they come to a stand-still at the desired position. The difference frequency profile between the two laser beams has the cosine shape that has been analyzed in the characterization of the beat between two DDS frequency sources in section 5.7. After the transport, detection of the atoms is achieved by illumination with resonant light that is strongly absorbed. The cloud appears dark in the picture. For transport distances larger than 5 mm the final position of the cloud can not be viewed by the camera anymore. In order to obtain an image of the cloud in these cases, the entire process is repeated in reverse and the atoms are transported back up to their original position into the field of view of the camera where an absorption image is taken.

First experimental results are shown in Figure 6.1. It can be seen that a large fraction of the atoms can successfully be transferred into the standing wave and transported a few millimeters. The positioning accuracy is mainly determine by the DDS. The accuracy is seen to be better than the size of the cloud which is approximately 50 µm. This is true even for transports of 144 mm round-trip distance and corresponds to a relative positioning accuracy of better than $10^{-4}$. It is believed that the actual accuracy is in the range of the wavelength of the transport beams or even better. This estimate is strongly supported by the characterization of the frequency
6.1. Transport of Atoms in a Standing Light Wave

Figure 6.2: Transport efficiency for transport distances from 0 mm to −72 mm. The cavity is situated at −36 mm. For the transport the atom cloud is first loaded into the standing wave. Then during 200 ms the frequencies of the two laser beams perform a cosine shaped sweep transporting the cloud the respective distance $\Delta z$ downwards. The atoms are held at this position during 150 ms and subsequently transported upwards again by the same distance in 200 ms. The number of atoms that remains after the transport is obtained from absorption pictures taken after 15 ms free expansion. For these measurements a relative error of 10% is assumed.

sweep performed in section 5.6 and section 5.7.

In order to obtain a quantitative measurement of the transport quality, the number of atoms that still remain trapped in the standing wave trap beam is determined from absorption pictures taken after the transport and subsequent free expansion of the cloud, Figure 6.2. It is observed that the largest losses happen during transport through the regions where the beam is narrow, namely the proximity of the optical cavity.

The measurements show that the transport in the optical standing wave basically works but has to be improved. It is for example desirable to lock the 850 nm laser to an atomic transition since its wavelength is the distance scale for the transport. Drifts in the laser wavelength cause relative scaling in the transport distances.

A second problem is the significant heating of the atoms that is observed. Due to the heating, no visible condensate fraction is present after the transport. The causes for the heating are not to be sought at the frequency source’s side, though. Noisy laser beams, unstable interference patterns and especially dynamical instabilities during Bloch oscillations contribute most to the heating and losses. This can for example be seen when holding the atoms in the standing wave without moving it. In this case
the heating is observed to be just as intense.

The aforementioned relative positioning accuracy limit of \(10^{-4}\) has to be attributed to the measurement process. A more precise determination of the positioning error can be obtained by RF spectroscopy of a narrow pancake-shaped disk of atoms. It is possible to evaporate most of the atoms out of the cloud in such a way that only a small spatially confined portion of the cloud is retained and transferred into the beam. The position of the pancake before and after the transport can be precisely determined since the frequency of the evaporation transition depends on the magnetic field and thus on position. These measurements will be performed in the future.

A fundamental limitation to the possible transport speeds lies in the acousto-optic modulation. Typical transport times are \(T = 200\) ms per way. From equations (5.5) and (5.8) one obtains a required maximum difference frequency \(\Delta f\) between the two DDS boards for a transport distance of \(\Delta z = -36\) mm of

\[
\Delta f = \frac{4\Delta z}{\lambda T} = -0.85 \text{ MHz.} \tag{6.1}
\]

Since the diffraction angle of the first order beam after the acousto-optical modulator increases with the modulation frequency it is clear that with a large difference frequency the two beams start to not couple into the fiber anymore and the power in the beams decreases. A frequency shift of 0.85 MHz is already high enough to lose a significant amount of light intensity during the phases of highest speed. The possible maximum frequency difference can be increased by a factor of two by asymmetrically shifting the two DDS boards’ frequencies.

If these hurdles can be taken, the transport will help to perform further interesting experiments: the preparation of entangled states and quantum computing in optical cavities can be achieved by measurement induced entanglement [32]. Sympathetic cooling during detection [33] and experiments with optical lattices in high-finesse cavities can also be employed.

The DDS frequency source proved to be easily integrable into the experimental environment. Based upon the data available so-far it is also well-equipped for the task of generating the needed signals.
Chapter 7

Conclusion and Outlook

In the present thesis a frequency generator is presented which is specifically suited to be used in experiments with cold atoms. The various measurements that were performed during design and characterization provide a quantitative determination of the properties. The device was shown to be an essential part in the control of the standing wave conveyor belt while evaluation in the context of evaporative cooling, generation of Ramsey pulses and Landau-Zener adiabatic transfers will be performed soon. The modular design is very flexible and may well be extended to other applications of computer controlled generation of signals.

The signal that can be generated by the source has guaranteed properties that fit well into experimental applications. Tailored high-resolution sweeps of frequency, power and phase can be easily specified in a way compatible with pre-existent control software. Stability and deterministic control of all parameters are supported by the largely digital nature of the design.

Although the device fulfills all specifications and exceeds most, some limitations remain to be overcome. The frequency sweep, phase and power level sampling rate of 8 kHz impose a limit on the obtain modulation frequencies. Higher resolutions and rates make Ramsey pulses without external gating of the signal feasible. This rate is imposed by the choice of the serial bus to the DDS chip and by the embedded computer and its operating system. The latter not strictly a real-time operating system but a multipurpose commodity one.

With these limitations in mind, a series of possible improvements is proposed:

- Reimplementing the kernel module and the server on a field programmable gate array (FPGA, a massively parallel logic device), similar to the approach presented in [34], would increase the sampling rate to approximately 10 MHz and thus permit modulation frequencies of up to 5 MHz. The inherent synchronization of the FPGA to the DDS should permit pulses as short as 50 ns with a timing resolution of 7 ns.

- It might also be advantageous to build on top of the GNURadio framework [35] and its Universal Software Radio Platform, USRP [36]. The USRP architecture features a computer controlled FPGA and a set of fast ADCs and DACs. Uti-
lizing this architecture permits a wide range of extensions and other already existing and freely available boards to be easily integrated.

- To realize more synchronized frequency outputs in one device, other chips\textsuperscript{1} can be employed providing two or four synchronized, separately controllable DDS cores. Since communication between the embedded controller and the DDS chip is performed over a single shared bus, the sampling rate will have to be shared between the outputs. To alleviate that limitation the parallel bus would have to be used.

- Generation of arbitrary waveforms could be accomplished by a pure digital to analog converter setup. An arbitrary waveform corresponds to an arbitrarily large set of output frequencies. To supply the DAC with data, a high-bandwidth data stream of samples would then be written to it. The output can be any digital time-sampled signal with a sampling rate only limited by the DAC chip. DAC chips with sampling rates of up to 1.2 GHz are available commercially.\textsuperscript{2} If supplied with data at a sufficiently high rate, those chips can then generate a nearly arbitrary spectrum in the range of 0 Hz to 600 MHz. Such a wide arbitrary spectrum can be used to generate tailored potentials for cold atoms in magnetic traps. The frequency components in the spectrum cause localized shifts of the energy levels similar to those seen in the Landau-Zener adiabatic transfer in section 2.4. These localized deformations can trap atoms [37]. A different approach is supplying the spectrum to a broad-band acousto-optical modulator. The incident laser beam is diffracted into a controllable and possibly complex pattern of output beams. Those output beams can be used to design a specifically formed dipole potential for cold atoms. Double-well or other complex structures can be created by these means.

- With a more powerful computer embedded in the device it may become feasible to generate and optimize the recipe in real-time on the device. The data transferred to the embedded computer would then be an abstract description of the sweeps and not consist of precomputed raw values. This would simplify and shorten the recipe and also reduce the amount of computation time that has to be spent on the user’s computer. If the device performs most of the calculation, stand-alone operation with a web interface where the user can enter and preview the functions defining the desired profile is possible. No special driver software is needed in this case.

\textsuperscript{2}AD9735, http://www.analog.com/en/prod/0,AD9735,00.html
Bibliography


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