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Ultra-Compact and Ultra-Efficient Three-Phase PWM Rectifier Systems for More Electric Aircraft

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Für meinen Vater Anton
For my father Anton

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Abstract

In order to improve the efficiency and to reduce the environmental impact of aircraft, global efforts for reducing the aircraft weight are under way. One of the key issues thereto is the wide application of electric systems instead of heavy mechanical, pneumatic and hydraulic driven equipment. This change in the power supply structure of an aircraft is known as More Electric Aircraft (MEA). In the course of this concept unidirectional active three-phase rectifiers in the power range of several kW are required, mainly for electrically driven actuators for flight control. In modern civil aircraft a three-phase AC mains with a voltage level of either 115 V or 230 V and a variable mains frequency of 360 Hz ... 800 Hz exists.

In this work unidirectional three-phase rectifiers are evaluated which are able to meet the enhanced requirements of aircraft application. Starting with a brief survey on the power supply structure and the demanding requirements to be met such as the power factor or input current quality, a survey on three-phase rectifier topologies suited for aircraft applications is given. There, also passive and hybrid (active/passive) systems are considered. Based on this evaluation, the two-level three-phase Δ-switch rectifier is found to be an ideal solution for a mains voltage of 115 V and the three-phase three-level Vienna Rectifier topology optimally fits the requirements for a 230 V mains.

Initially, the specific characteristics and control approaches of the well known Vienna Rectifier topology are summarized. The MEA concept calls for a minimization of volume and weight and hence a single-objective optimization of the three-phase Vienna Rectifier

topology regarding maximum possible power density is performed which finally results in a 10 kW rectifier system with a power density of 14.1 kW/dm^3. Several limitations of the power density optimizations are addressed. A magnetically coupled damping layer is proposed for reducing the switching transients oscillations caused by the high-speed switching. It is shown how the turn-off delay of power MOSFETs degrades the input current quality and how the switching losses can be minimized. These effects can clearly be illustrated with a η-THD$_\mathrm{I}$-Pareto Curve.
Furthermore, a purely digital implementation of a high-speed controller using an FPGA is developed which achieves a total control cycle time of 490 ns. Also substantial improvements of the current controller, mainly for operation at the high mains frequencies of 360 Hz ... 800 Hz, are shown which finally results in a THD$_\mathrm{I}$ of the input current below 2 %. A considerably improved noise model of the Vienna Rectifier system is derived considering parasitic capacitances to the heat sink and to earth. Also a novel concept for eliminating the CM voltage of the output is proposed and analyzed in detail. Measurements taken from the implemented prototype finally confirm the proper operation of the rectifier circuit and the effectiveness of the discussed improvements.

Next to the Vienna Rectifier topology, a two-level Δ-switch rectifier system is analyzed. Basic operation of the topology is discussed, detailed loss models are derived and a digital PWM current controller/modulation concept is developed where all three phases are controlled simultaneously. The proposed, phase related controller concept is able to handle a single phase loss without any changes in the controller structure. A detailed study on reactive power capability is performed and it is analyzed to what extend this feature can be used to compensate capacitive currents drawn by the EMI filter capacitors. The discussion is accompanied by measurements taken from the implemented 5 kW laboratory prototype.

In the course of this thesis, several Vienna Rectifier systems with different switching frequencies have been built. Using the data of the constructed rectifier systems permits to derive a Pareto Curve regarding efficiency and power density of this topology. Also the actually achievable volume reduction due to an increase in switching frequency can clearly be illustrated.

Kurzfassung

Die Erhöhung des Wirkungsgrads und die Reduzierung der Schadstoffemission sind Ziele in der Flugzeugindustrie die gegenwärtig mit großem Hochdruck verfolgt werden um den Flugverkehr wirtschaftlicher zu gestalten. Vor allem die Reduzierung des Gesamtgewichts des Flugzeugs spielt dabei eine entscheidende Rolle. Dies soll in erster Linie dadurch erreicht werden, dass bestehende hydraulisch, mechanisch oder pneumatisch angetriebene Geräte durch elektrische Systeme ersetzt werden. Dieser strukturelle Umbruch in der Energieversorgung ist unter dem treffenden Namen "More Electric Aircraft" (MEA) bekannt. Im Zuge dieses Umbruchs werden massiv unidirektionale aktive dreiphasige Gleichrichtersysteme in einem Leistungsbereich von mehreren kW benötigt, vor allem für elektrisch betriebene Aktuatoren zur Steuerung und Stabilisierung der Flugbahn des Flugzeugs. Moderne zivile Flugzeuge besitzen ein AC-Stromnetz mit einer Spannung von entweder 115 V oder 230 V und einer Netzfrequenz von 360 Hz . . . 800 Hz.

Im Rahmen dieser Arbeit werden unidirektionale Gleichrichterstrukturen hinsichtlich der erhöhten Anforderungen in Flugzeuganwendungen untersucht. Nach einem Überblick über geeignete Gleichrichterstrukturen, der neben aktiven Gleichrichtersystemen auch passive und hybride Topologien beinhaltet, werden zwei vielversprechende Gleichrichterstrukturen unter der Berücksichtigung von Anforderungen wie Leistungsfaktor und Eingangsstromverzerrungen für weitere Untersuchungen ausgewählt. Während der dreiphasige 2-Level Δ-Switch Rectifier für eine Netzspannung von 115 V vorteilhaft ist, erfüllt die dreiphasige 3-Level Vienna Rectifier Topologie die Anforderungen für das höhere Nezspannungsniveau von 230 V optimal.

Ein Hauptpunkt des MEA-Konzepts stellt die Reduzierung der Baugröße und des Gewichts der eingesetzten Aktuatoren dar. Im Hinblick auf diese zentralen Anforderungen wird eine detaillierte Optimierung der Vienna Rectifier Struktur hinsichtlich Leistungsdichte vorgenommen, welche in einem 10 kW Gleichrichtersystem mit einer Leistungsdichte von 14.1 kW/dm^3 resultiert. Im Zuge dieser Optimierung werden verschiedenste limitierende Faktoren für eine Erhöhung der Leistungsdichte diskutiert. Ein neuartiges, magnetisch gekoppeltes PCB-integriertes Snubber-Konzept zur Reduktion der transienten Schaltüberspannungen bei MOSFETs mit sehr hoher Schaltgeschwindigkeit wird vorgestellt. Es wird weiters gezeigt, dass die nichtlineare Ausgangskapazität der eingesetzten MOSFETs die Stromqualität signifikant verschlechtert und diskutiert wie Schaltverluste bei hohen Schalfrequenzen in Grenzen gehalten werden können. Der Zusammenhang zwischen Wirkungsgrad und Verzerrung der Eingangsströme kann hier sehr anschaulich in einer η-$\mathrm{THD_I}$-Pareto Front dargstellt werden.

Im Zuge der Realisierung des optimierten Gleichrichtersystems wird die Implementierung eines voll-digitalen dreiphasigen Stromreglers mit einer Berechnungszeit von nur 490 ns unter Verwendung eines modernen FPGAs behandelt. Zusätzlich werden effektive Verbesserungen der bestehenden Regelansätze implementiert, wodurch letztendlich ein $\mathrm{THD_I}$ der Netzströme von unter 2 % erzielt werden kann.
Aufgrund der hohen Schaltfrequenzen muss zudem ein verbessertes EMV Modell der Vienna Rectifier Gleichrichterstruktur erarbeitet werden welches auch parasitäre Kapazitäten der Halbleiter zum Kühler und gegen Erde berücksichtigt. Es wird eine EMV-Filterstruktur vorgeschlagen und im Detail analysiert, welche die störende hochfrequente Gleichtaktspannung am Ausgang des Gleichrichters unterdrückt. Die diskutierten und vorgeschlagenen Verbesserungen werden durch Messungen am realisierten Gleichrichtersystem bestätigt.

Darauf folgend wird eine dreiphasige 2-Level Δ-Switch Gleichrichterstruktur im Detail analysiert. Neben einer Diskussion der grundlegenden Funktion des Systems und einer Ableitung von detaillierten Verlustmodellen wird ein neuartiges phasenorientiertes Regelungskonzept entwickelt, bei dem stets alle drei Phasenströme geregelt werden. Die vorgeschlagene Regelungsstruktur ermöglicht im Falle eines Phase-

nausfalls den fortlaufenden Betrieb mit reduzierter Ausgangsleistung ohne Änderungen in der Regelungsstruktur vornehmen zu müssen. Das Δ-Switch Gleichrichtersystem ermöglicht ausserdem den Betrieb mit eingeschränkter Phasenverschiebung zwischen Phasenspannung und Phasenstrom und es wird gezeigt, dass diese Eigenschaft zur Kompensation der Blindleistung der Filterkondensatoren am Eingang und somit zur Verbesserung des Leistungsfaktors verwendet werden kann. Die diskutierten Punkte werden jeweils durch Messungen an einem realisierten 5 kW Gleichrichtersystem bestätigt.

Im Zuge dieser Dissertation wurden mehrere Vienna Rectifier Prototypen mit unterschiedlichen Schaltfrequenzen realisiert. Die Daten und Performance-Indizes dieser Systeme werden verwendet um eine Pareto Front hinsichtlich Wirkungsgrad und Leistungsdichte zu erstellen. Darauf basierend wird auch die effektiv über Erhöhung der Schaltfrequenz erzielbare Reduktion des Volumens kritisch diskutiert.

Contents

Chapter 1

Introduction

1.1 The More Electric Aircraft

In the last years the passenger air traffic has grown at an average rate of 9 %/year and is predicted to further grow with a rate of approximately 5 %/year in the near future [1]. One reason for this remarkable growth can be found in the technological improvement of the aircraft which increased the efficiency and reduced the cost of traveling by air. An increase of the fuel economy, achieved on the one hand by more efficient propulsive energy generation and on the other hand by reducing the take-off weight of the aircraft, is a major point of concern. The improvement can also be measured by reduced life cycle costs of modern aircraft which can for instance be achieved by technologies offering reduced periodical maintenance. Reliability is of high importance in aerospace applications and any new technology must not lead to reduced reliability.

The use of electronic equipment emerged to be a key technology to further improve the efficiency and reduce the fuel-costs and CO_2 emissions of aircraft and is commonly known as *More Electric Aircraft (MEA)* concept [2]. The intention with introducing this concept is to reduce the weight of the aircraft by substantial use of electronic equipment instead of heavy mechanical, pneumatic or hydraulic driven elements. Technology studies for military aircraft carried out in the

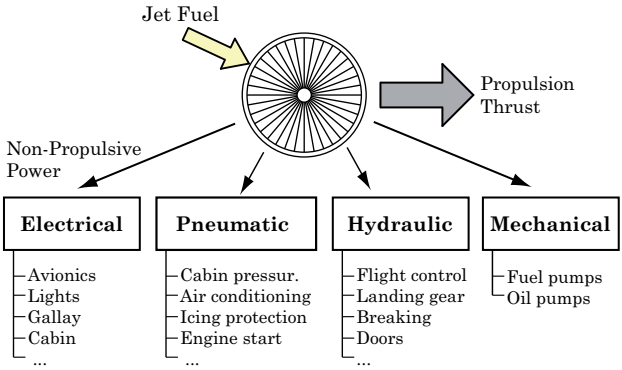


Fig. 1.1: Power distribution of non-propulsive power of a conventional aircraft using electrical, pneumatic, hydraulic and mechanical power.

late 1990s expect a reduction of the take-off weight of 6.5 % and an increase of mean flying hours between failures of 5.4 % by application of MEA technologies [3].

The power generation of an aircraft is performed by its turbines where the power can be separated in a propulsive part and in a non-propulsive part. The non-propulsive part is used to drive several elements on the aircraft and in an conventional aircraft such as the A330 from Airbus Inc. it can be separated in electrical, pneumatic, hydraulic and mechanical power (cf. **Fig. 1.1**). The mechanical power of the turbine is used to drive the fuel and oil pumps. Due to the high power density of hydraulically powered actuators and their ability to generate large forces, the hydraulic power is used to move the flight control surfaces in order to control the flight path of the aircraft. It is further used for the landing gears, braking, doors and other actuators.
Some bleed air of the turbine is used for pressurization and air conditioning of the cabin and for icing protection of the wings.
An electrical generator is connected to a shaft of the gas turbine and the electrical power is used for lighting, avionics, galley, flight entertainment and other electrical loads.

In the course of the MEA concept all non-electric power take-off possibilities (mechanical, hydraulic and pneumatic) shall be replaced by

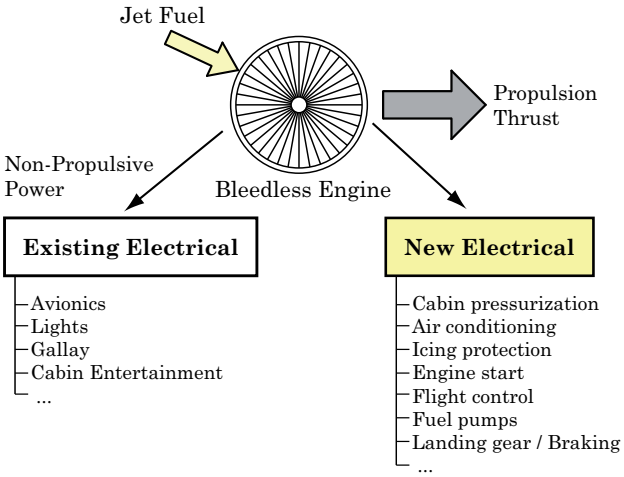


Fig. 1.2: Non-propulsive power distribution of a "More Electric Aircraft".

electrical systems (cf. **Fig. 1.2**) [4]. The bleed air taken from the engine, e.g. for heating and pressurization of the cabin, considerably reduces the efficiency of the engine and a total elimination of bleed air is preferable. This, however, requires new electrical systems for cabin pressurization, air conditioning, icing protection or electric engine start-up as in a conventional aircraft the pneumatic system is also used for engine start-up. The hydraulic power, which is mainly used for primary and secondary flight control, offers the advantage of a very robust actuator system showing a high power density. The hydraulic infrastructure, however, is heavy, inflexible and requires regular maintenance. A high reliability of the primary flight control elements is required and typically a redundant hydraulic architecture (3H) is used in conventional aircraft which finally results in a high weight [5]. In addition, the dangerous fluids are a problem in case of a leakage. A replacement of the hydraulic actuators by electrically powered actuators is therefore highly desirable and one of the biggest parts of the MEA concept. Further details will be discussed below.
Due to the elimination of the mechanical power sources electrically driven fuel pumps and oil pumps with very high reliability are required.

The replacement of the non-electric systems by electrical equipment

results in a considerably increased electrical power demand. Whereas in a conventional aircraft, such as the Airbus A330, the installed capacity is about 300 kVA the installed capacity of the recently released MEA aircraft Airbus A380 is 600 kVA [6] and according to [7] the Boeing Dreamliner 787 will have an installed capacity of 1 MVA.
In a conventional aircraft the electrical generators are connected with the turbine via a mechanical gear box which transfers the variable speed of the engine shaft to a constant speed shaft used for generation of a three-phase on-board power net with a constant mains frequency of 400 Hz and a voltage of 115 V (cf. **Fig. 1.3(a)**). A three-stage permanent magnet excited wound field synchronous machine is typically used for civil aircraft [8][1]. The engine start is normally provided by the pneumatic system of the aircraft and due to the elimination of the bleed air and the pneumatic system, new solutions have to be found. Instead of using an additional element for engine start the generator is also used as starter motor which reduces the weight of the aircraft advantageously [9, 10].

In a MEA the mechanical gearbox is eliminated and the electrical power generator is directly connected to the variable engine shaft which results in a variable on-board mains frequency of 360 Hz–800 Hz (cf. **Fig. 1.3(b)**). Either Permanent Magnet Synchronous Machines (PMSM) or Switched Reluctance Machines (SRM) are promising motor/generator technologies due to their high power density, robustness and temperature tolerance [1, 11, 12]. Due to the increased electrical power demand, the mains voltage of the Boeing B787 will be increased to 230 V which reduces the conduction losses caused by the large current levels for $V_{\mathrm{N}} = 115\,\mathrm{V}$ [8]. By increasing the mains voltage from 115 V to 230 V, however, and a simultaneous possible increase of the mains frequency up to 800 Hz the reactive power of the system in case of capacitive load

$$Q = 2\pi f_{\mathrm{N},800} C V_{\mathrm{N},230}^2 = 8\left(2\pi f_{\mathrm{N},400} C V_{\mathrm{N},115}^2\right) \ , \tag{1.1}$$

as caused e.g. by the EMI filter capacitors or the parasitic capacitance of the cables, is increased by a factor of eight. This huge reactive power demand may be a problem for the intended electrical generators.

[1] A permanent magnet exciter stage produces energy which is used to induce a magnetic field on the rotor. The main rotor field strength is controlled by field control applied in the wounded main exciter stage. More details can be found in [8]

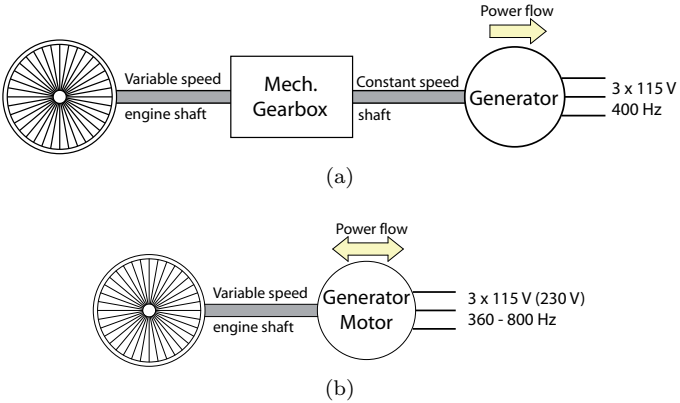


Fig. 1.3: (a) Conventional electrical power generation using a mechanical gearbox to transfer the variable speed of the engine shaft to a shaft with constant speed and (b) electrical power generation omitting the mechanical gearbox resulting in a variable generator frequency of 360 Hz–800 Hz. The generator is also used as starter motor for the engine.

Whereas some AC loads, such as heaters, lights and passive rectifier systems, are not or only slightly influenced by the variable mains frequency, some of the existing AC loads such as induction motors for pumps and fans are significantly affected. The work given in [13] addresses the impact of the variable mains frequency on the different load types. As a result, power electronic systems are heavily required to interface the different load types to the on-board mains. According to [5], more than 70 motors for fans, pumps or actuators with a power of less than 10 kW are installed in the Airbus A380 .
Due to the large mains frequency and constant power loads, which result in a negative input impedance of active rectifier systems, stability problems may occur [14] which will be further discussed in section 7.3.

Fig. 1.4 shows one half of the symmetrical electrical power system architecture (e.g. left side) of the civil MEA Boeing Dreamliner 787. The possible application areas of active rectifiers are highlighted. The gas turbines drive two starter/generators which generate an AC mains bus with a frequency of 360 Hz–800 Hz and a voltage of 230 V/400 V. An Auxiliary Power Unit (APU) is connected to the AC bus as well which would be activated in case of an emergency. The APU is also used for power supply on ground while the engines are not running.

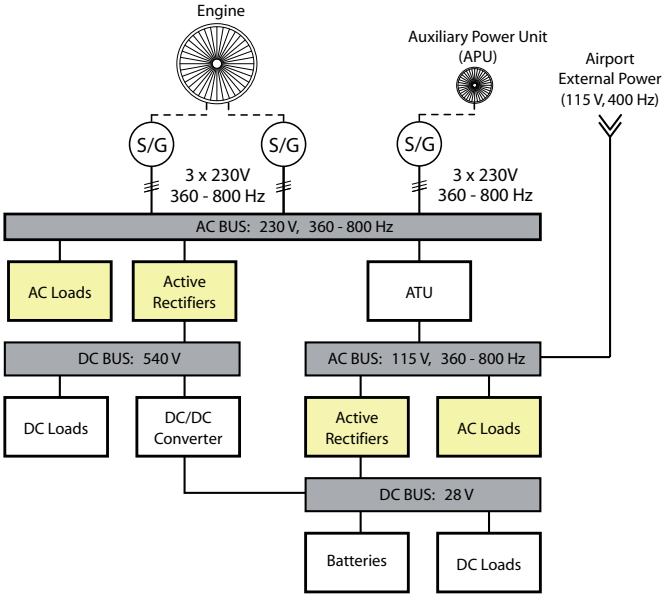


Fig. 1.4: Electric power system architecture of a modern More Electric Aircraft (Boeing 787) according to [15].

Some AC loads are directly connected to this bus and depending on the load type an active rectifier circuit is needed. By application of active rectifiers a 540 V DC bus ($\pm$270 V) is generated. On the other hand an Auto Transformer Unit (ATU) is used to build the 115 V AC bus with variable frequency. AC loads designed for the former AC bus with a voltage of 115 V can directly be connected. Also the external power connectors of the airports can be connected to this bus.
The widely used 28 V DC bus (e.g. avionics) is either generated by active rectifiers from the 115 V AC bus or by use of DC/DC converters from the high-voltage DC bus.

In the course of the MEA power electronic systems are also needed for ground power supplies [17, 18], for landing gears [19], breaking [20], and many other subsystems.

Some research on the next generation More Electric Aircraft deals

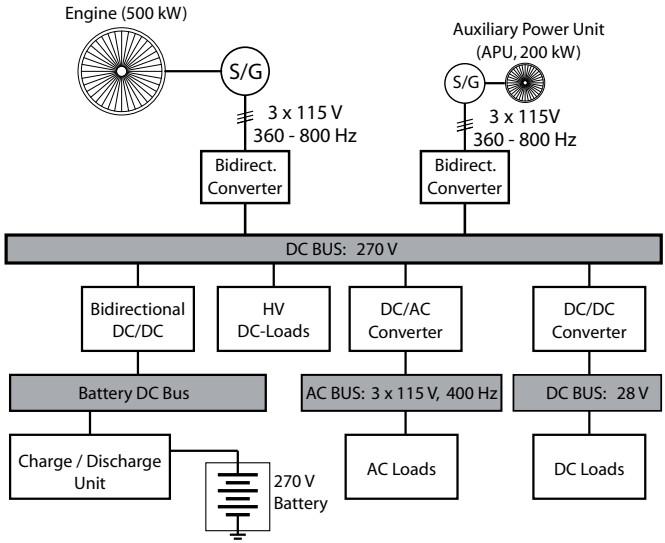


Fig. 1.5: Possible future electric power system architecture using DC primary power supply [16].

with electrical propulsion by use of Superconductors [21] in order to implement the true All Electric Aircraft. There it is stated that liquid hydrogen LH_2 may be used as fuel which shows only one-third of the weight of common jet fuel if the same energy amount is compared. However, due to safety and reliability reasons these topologies are not expected to be in service in the next 20-30 years.

Fig. 1.5 shows a possible future electric power system architecture using a 270 V DC bus [16]. The stability problems coming along with the AC bus can be solved if the DC bus is used as primary power system. In addition a battery for energy storage with a corresponding battery DC bus can easily be installed. Also the 115 V AC bus and the low voltage DC bus (28 V) are still present. Military aircraft already use this power system architecture.

1.1.1 Actuators for Flight Control

In order to control and stabilize the airplane's flight trajectory the aircraft exhibits special surfaces which can be activated by the pilot. These flight control surfaces can be separated into two groups: the primary flight control and the secondary flight control surfaces. The primary flight control elements, such as *aileron, rudder* and *elevator* are absolutely essential to control the flight path whereas the secondary flight control elements, such as *spoiler, flaps, slats* or *horizontal stabilizer* are basically not required but mainly help to increase the lift during starting and landing [1].

The state-of-the-art technology for flight control is called *Fly By Wire (FBW)* and uses a centralized hydraulic pump, a hydraulic line system to the actuator and an electronically controlled actuator. This technology was first introduced in a civil aircraft by Airbus in the 1980s [22]. In order to guarantee a high safety, three independent hydraulic lines are used for the primary control systems which is known as the 3H architecture. Although the actuator is electronically controlled, a connection to the redundant hydraulic system with a centralized pump exists. These hydraulic systems and actuators show a very high reliability but the heavy piping needs periodic maintenance and shows the problem of leakage.

One major point of the MEA concept is to replace these heavy hydraulic actuator system by electrically driven actuators in order to get rid of the heavy centralized powered hydraulic lines [23, 24]. Two types of actuators emerged as alternative - the Electro Hydrostatic Actuator (EHA) [25] (cf. **Fig. 1.6(a)**) and the Electro Mechanical Actuator (EMA) [26, 27] which is shown in **Fig. 1.6(b)**.
The control surface for an EHA is still moved using hydraulic power. The required hydraulic system is yet locally generated in the actuator where the local hydraulic pump is powered by a motor. Due to their robustness and reliability the SRM or the PMSM are suited as electrical motor [1]. The interface to the grid can either be performed by direct AC/AC matrix conversion or by a voltage source back-to-back conversion consisting of a rectifier system and an inverter system which is shown in **Fig. 1.6(a)**. As the power grid of the aircraft typically does not offer any energy storage element, energy regeneration into

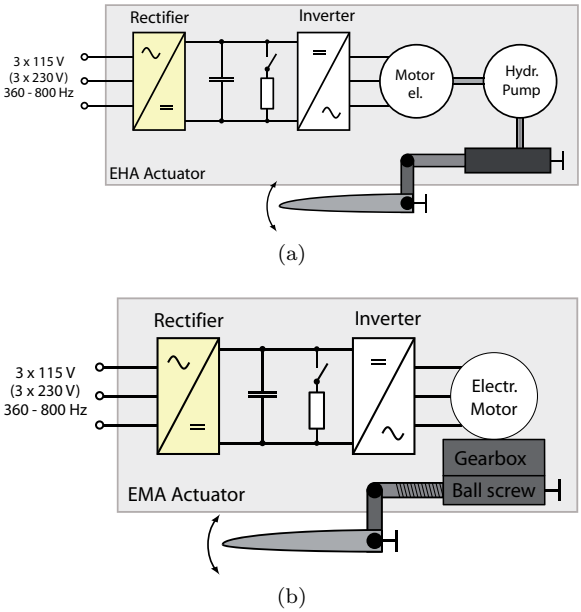


Fig. 1.6: Basic schematic of (a) an Electro Hydraulic Actuator (EHA) and (b) an Electro Mechanical Actuator (EMA) for application in the More Electric Aircraft.

the mains is not allowed. The energy has to be dissipated in the DC voltage link which is illustrated by a braking resistor in **Fig. 1.6**. In case of power distribution on the aircraft using a DC bus, the rectifier system is not needed and the inverter can directly be connected to the high voltage DC bus. If additionally to the AC mains also a DC bus is available (e.g. 115 V_{AC}, 270 V_{DC}), it is conceivable that the DC bus is connected with the DC link of the rectifier/inverter system in case of an outage of the rectifier system in order to increase the reliability of the actuator system.

The biggest advantage of the EHA type is that it can be combined with the existing hydraulic line where either the locally (electrically) generated hydraulic power or the existing centralized powered hydraulic source drives the actuator. This type of actuator is called Backup Electro Hydraulic Actuator (BEHA) and results in a very high reliability. The local weight of the EHA is higher than a classical FBW operated hydraulic actuator but due to the missing hydraulic lines the

global weight is reduced [5].

In contrast to the EHA the EMA waives the hydraulic system and the flight control surface is directly moved by the EMA as illustrated in **Fig. 1.6(b)**. The interface to the grid is similar to the EHA solution. Up to now, the EMA shows reduced reliability due to possible jamming and this type of actuator is currently not allowed to be used on civil aircraft [28].

The power required for the different actuators varies from a few kW for the edge slats to 50 kW for the horizontal stabilizers and the rudder [29] and also the mission profile of the various actuators is very different. Whereas during starting and landing huge movements have to be performed only small or no variations are required during the flight. Due to safety reasons and the high reliability of existing classical hydraulic actuators the presented actuators are currently only used for secondary flight control on civil aircraft [28]. The sole use of EMA and EHA is reserved for military aircraft, such as the F18 [30] or Unmanned Aerial Vehicles (UVA). Due to the use of hydraulic actuators in combination with electrically driven actuators the reliability of the resulting system is improved. The recently developed Airbus A380 for instance employs two independent hydraulic systems (2H) and and two independent electrical systems (2E) which is a safety improvement with respect to the former used 3H architecture.

1.1.2 Requirements for Equipment Connected to the Aircraft Mains

The MEA concept in general calls for a reduction in size and weight in order to reduce the take-off weight of the aircraft which finally results in cost reduction due to reduced fuel consumption. A high power density (expressed in kW/dm^3) and preferably low power to weight ratio of the electrical power systems are desirable.

As for mains interfaces in industrial environment, rectifier systems applied in aircraft have to comply with (aircraft) standards. Primarily the airborne standard DO160F [31] and the military standard MIL-STD704F [32] have to be fulfilled. As reported in [33] aircraft companies

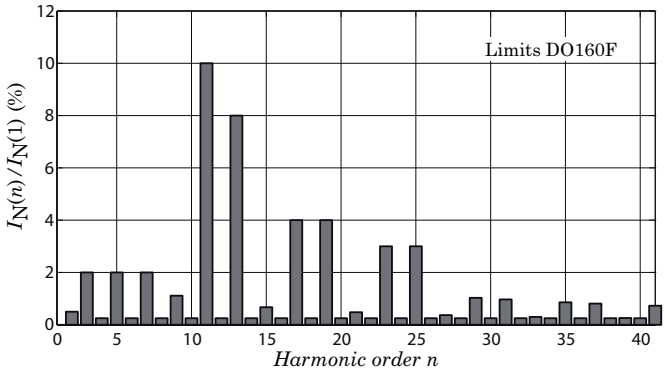


Fig. 1.7: Individual current harmonic limits listed in the standard DO160F [31].

create their own standard with partly more stringent limitations than the ones listed in the mentioned airborne standard. In the following the main requirements will be discussed briefly.

Due to the missing energy storing elements in an aircraft the active rectifiers are not allowed to regenerate energy back into the mains. Strictly speaking only unidirectional rectifier systems are permitted where an energy regeneration into the mains is inherently prohibited by the basic structure. Bidirectional rectifier systems are able to prohibit a power flow into the mains only by control logic. In case of a failure, where for instance the rectifier system is disabled, however, an energy feed-back could occur.
According to [31] the rectifier system must be able to handle a voltage unbalance of 10 % and an outage of one or more phases must not lead to unsafe operation modes. It is rather requested that the rectifier system should be able to further operate at a reduced power level if a single phase loss occurs.
The individual input current harmonic limits are listed in **TABLE 1.1** and illustrated in **Fig. 1.7** where $I_{N(1)}$ is the fundamental and n is the order of the harmonics.

The harmonic limits are specified in such a way, that passive 12-pulse rectifier systems, with their characteristic harmonics at $n \cdot 12 \pm 1$, can be applied. Boeing, however, defined more stringent harmonic limits for the 11^{th} and 13^{th} so that the limits can not be fulfilled with passive

TABLE 1.1: Current harmonics limits of three-phase equipment according to DO160F [31].

Harmonic Order	**Limits (I_n)**
3^{rd}, 5^{th}, 7^{th}	$0.02I_1$
Odd Triplen Harmonics (9^{th}, 15^{th}, $21^{th} \dots 39^{th}$)	$0.1I_1/n$
Odd Non-Triplen Harmonics (11^{th}, 13^{th})	$0.03I_1$
Odd Non-Triplen Harmonics (17^{th}, 19^{th})	$0.04I_1$
Odd Non-Triplen Harmonics (23^{th}, 25^{th})	$0.03I_1$
Odd Non-Triplen Harmonics (29^{th}, 31^{th}, 35^{th}, 37^{th})	$0.3I_1/n$
Even Harmonics, 2^{nd}, 4^{th}	$0.01I_1/n$
Even Harmonics > 4 (6^{th}, 8^{th}, $10^{th} \dots 40^{th}$)	$0.0025I_1$

12-pulse rectifiers and that either active rectifiers or passive 18-pulse rectifiers must be used instead.

The power factor of AC interface systems is limited between 0.85 lagging and unity for power levels greater than 50 % of the rated output power. In the standard MIL-STD407F [32] it is stated that a leading power factor is not allowed for equipment with output power levels greater than 500 VA in order to prevent self-excitation of synchronous generation sources [33]. No information is, however, given whether this limitation is only valid for steady state operation or also during transients. This limitation has to be considered for an evaluation of the applicability of active rectifier systems. Active rectifier circuits require a specifically designed EMI filter, including filter capacitors connected to the rectifier input, in order to limit the conducted emissions gener-

ated by the high-frequency switching actions. Bidirectional active rectifier systems, such as the two-level six-switch rectifier circuit or the three-level NPC rectifier, are actively able to compensate the capacitive reactive power also at no load condition. Unidirectional rectifier systems, which are discussed in this work, are partly able to compensate the capacitive currents but require thereto a specific amount of load current and a compensation at no-load condition is therefore not possible. Bidirectional rectifier circuits on the other hand may allow energy regeneration into the mains which is also not permitted. In addition the existing filter capacitance may be a problem if the rectifier control is turned off, e.g., in case of a failure or during start up. As a result only 12-pulse or higher order passive rectifier systems would remain. It therefore has to be clarified if active (bidirectional) rectifier systems can be used for such applications.
Compensation of the capacitive current by use of inductors at the input is possible but sensible due to their large volume and weight. This can be demonstrated if an input capacitance of $C = 3\,\mu\text{F}$ per phase is assumed. The corresponding reactive power generated by the filter capacitors can be calculated to

$$Q = 2\pi f_\text{N} C V_\text{N}^2 = 797\,\text{VAr} \tag{1.2}$$

if a mains frequency of 800 Hz and a mains voltage of 230 V is assumed. The required inductor to compensate this reactive power, compensation inductors placed in parallel to the star-connected filter capacitors, would be $L = 13\,\text{mH}$. Using this compensation approach the reactive power is only compensated for one mains frequency and cannot be applied for aircraft showing a variable mains frequency. The compensation is, however, independent of the applied load.
The compensation inductors could alternatively be connected to the rectifier input (in series to the impedance of the mains) and an inductor value of $L = 750\,\mu\text{H}$ would be required for the case at hand. Beneath the fact that compensation is only possible for one mains frequency the compensation is dependent on the applied load, i.e. only a $\cos(\varphi_1)$ of $\cos(\varphi_1)_{5\text{kW}} = 0.94$ can be achieved at 50 % of nominal load and is further reduced to $\cos(\varphi_1)_{2.5\text{kW}} = 0.75$ at $P_\text{o} = 2.5\,\text{kW}$ ($V_\text{N} = 230\,\text{V}$, $f_\text{N} = 800\,\text{Hz}$, $P_\text{o} = 10\,\text{kW}$). A compensation only by connecting inductors to the system is therefore not very promising.

In addition to the limitations of the low-frequency input current

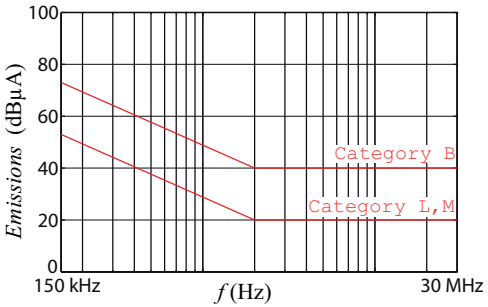


Fig. 1.8: Conducted input current emission limits for equipment connected to the AC mains of an aircraft according to the standard DO160F [31].

TABLE 1.2: Requirements for three-phase rectifier circuits connected either to the 115 V or to the 230 V mains.

Mains voltage 115 V	
Input voltage	$V_N = 115\,V \pm 10\,\%$
Output power	$P_o = 5\,kW$
Output voltage	$V_o = 400\,V$ $(\Delta V_o < 0.1 V_o)$
Mains voltage 230 V	
Input voltage	$V_N = 230\,V \pm 10\,\%$
Output power	$P_o = 10\,kW$
Output voltage	$V_o = 2 \times 400\,V$ $(\Delta V_o < 0.1 V_o)$
Mains frequency	$f_N = 360\,Hz \ldots 800\,Hz$
Power factor	$\lambda > 0.85$ (lagging) for $P_o > 0.5 P_{o,nom}$
Input current quality	$THD_I < 5\,\%$
	Indiv. harm. according to **TABLE 1.1**
EMI	Compliance with DO160F

harmonics the rectifier system has to comply with high-frequency conducted emission standards. The EMI limits are of high importance as the volume of the EMI filter takes about 30 % of an active rectifier system which will be discussed in section 5.8. The corresponding conducted emission limits for the input currents of the airborne standard DO160F are given in **Fig. 1.8**. Note that limitations of the noise

currents (dBμA) are given which can be translated into equivalent noise emissions (dBμV) using the frequency dependent impedance of the Line Impedance Stabilization Network (LISN). The standard covers the frequency range [150 kHz...30 MHz] and several categories are defined for the equipment. Category L and category M are defined for equipment which is located in the bay or in the passenger cabin of the aircraft but far from radio receiver antennas. Equipment of the category B is intended for equipment where interference should be controlled to tolerable levels (cf. [31]).

The requirements for three-phase rectifier circuits treated in this work are summarized in **TABLE 1.2** for a mains voltage of 115 V and 230 V respectively.

1.2 Objective and New Contributions of this Work

The objective of this work is to select and analyze unidirectional three-phase rectifier topologies which are suitable to fulfill the requirements for aerospace applications (cf. **TABLE 1.2**). The three-level three-phase Vienna Rectifier circuit and the three-phase two-level Δ-switch rectifier circuit are selected and their control and performance are discussed particularly with regard to the high mains frequency of 360 Hz–800 Hz. In addition the highest possible power density of the Vienna Rectifier topology is evaluated as power density and weight are of high concern in aerospace applications.

The main new contributions of this work are:

- Evaluation and selection of three-phase rectifier circuits suitable for aerospace applications (chapter 2).
- Development of detailed loss models for the Vienna Rectifier topology and calculation of the efficiency as a function of chip area and switching frequency (section 5.3).
- Analysis and optimization of the high-speed switching behavior of superjunction MOSFET devices and analysis of the input current quality as a function of chip area and switching frequency (section 5.1) which finally results in the η-$\mathrm{THD_I}$-Pareto Front (section 5.5).
- Analysis of the reactive power capability of the Vienna Rectifier topology (section 3.2.6).
- Development and detailed analysis of a magnetically coupled damping layer for switching transient shaping (section 5.2).
- Design and implementation of a purely digital three-phase current controller for the Vienna Rectifier circuit using an FPGA with a cycle time of only 490 ns.
- Derivation of an enhanced common mode model of the Vienna Rectifier topology and analysis of a novel common mode filter concept where the rectifier output shows no high-frequency common mode voltage (section 5.7).

- Successful design and construction of a 10 kW Vienna Rectifier prototype system operating at a switching frequency of 1 MHz and featuring a power density of 14.1 kW/dm^3 (section 5.8).
- Detailed analysis of the Δ-switch rectifier topology including derivation of a detailed loss model (chapter 6).
- Proposal and design of a novel phase-oriented PWM controller concept which is able to handle several error conditions (section 6.2).
- Illustration of the relation between efficiency and power density (η-ρ-Pareto Front) based on data taken from actually implemented rectifier systems (chapter 7).

In the course of this dissertation the following conference and journal papers have been published:

Conference Papers

- M. Hartmann, A. Muesing, J. W. Kolar, "Switching Transient Shaping of RF Power MOSFETs for a 2.5 MHz, Three-Phase PFC," *Proc. of the 7th Int. Conf. on Power Electronics (ICPE '07),* Daegu, South Korea, Oct. 22 - 26, 2007, pp. 1160-1166, PDF, IEEE.
- M. Hartmann, S. D. Round, J. W. Kolar, "High-Frequency, Three-Phase Current Controller Implementation in an FPGA," *Proc. of the 11th Workshop on Control and Modeling for Power Electronics (COMPEL 2008),* Aug. 17-20, 2008, pp. 1-8, PDF, IEEE.
- M. Hartmann, J. Miniboeck, J. W. Kolar, "A Three-Phase Delta Switch Rectifier for More Electric Aircraft Applications Employing a Novel PWM Current Control Concept," *Proc. of the APEC 2009,* Washington DC, USA, February 15 -19, 2009, pp. 1633 - 1640, PDF, IEEE.
- M. Hartmann, H. Ertl, J. W. Kolar, "EMI Filter Design for High Switching Frequency Three-Phase/Level PWM Rectifier Systems," *Proc. of the APEC 2010,* Palm Springs, California, February 21-25, 2010, pp. 986-993, PDF, IEEE.

- M. Hartmann, J. W. Kolar, "Analysis of the Trade-Off between Input Current Quality and Efficiency of High Switching Frequency PWM Rectifiers," *Proc. of the Int. Power Electronics Conf. (ECCE 2010)*, Sapporo, Japan, June 21-24, 2010, pp. 534-541, PDF, IEEE.

Journal Papers

- M. Hartmann, J. Biela, H. Ertl, J. W. Kolar, "Wideband Current Transducer for Measuring AC Signals with Limited DC Offset," *IEEE Transactions on Power Electronics,* vol.24, no.7, pp. 1776-1787, July 2009, IEEE.
- M. Hartmann, A. Muesing, J. W. Kolar, "Switching Transient Shaping by Application of a Magnetically Coupled PCB Damping Layer," *Korean Journal of Power Electronics,* vol. 9, no. 2, pp. 308-319, July 2009, PDF.
- M. Hartmann, S. Round, H. Ertl, J. W. Kolar, "Digital Current Controller for a 1 MHz, 10 kW Three-Phase VIENNA Rectifier," *IEEE Transactions on Power Electronics,* vol.24, no.11, pp. 2496-2508, Nov. 2009, PDF, IEEE.
- M. Hartmann, H. Ertl, J.W. Kolar, "EMI Filter Design for a 1 MHz, 10 kW Three-Phase/Level PWM Rectifier," *IEEE Transactions on Power Electronics,* Early Access, 2011, IEEE.

Conference Tutorials

- J. W. Kolar, M. Hartmann, T. Friedli, "Three-Phase PFC Rectifier and AC-AC Converter Systems," *Tutorial at the APEC 2011,* Fort Worth, TX, USA, March 6-10, 2011.

Patents

- J. W. Kolar, M. Hartmann, and T. Friedli, "Hybrider dreiphasiger AC/DC-Konverter und Verfahren zu dessen Steuerung," *Swiss Patent, Appl. No. CH 00298/11, Switzerland,* filed Feb. 21, 2011.

1.3 Outline of the Thesis

In **Chapter 2** a survey on unidirectional three-phase rectifier circuits suited for the intended aerospace application is given. Next to active rectifier systems also passive and hybrid rectifier systems are considered. Based on the findings of chapter 2, the two-level Δ-switch rectifier and the three-level Vienna Rectifier are chosen for further investigations.

The basic operating principle of the Vienna Rectifier topology including PWM control concept is summarized in **Chapter 3**. There, also the reactive power capability of the Vienna Rectifier topology is discussed and a novel concept for operation with considerable phase displacement using a phase-oriented PWM controller is proposed.

In **Chapter 4** a basic introduction in multi-objective optimization of power electronic systems is given.

Chapter 5 discusses the power density optimization of the Vienna Rectifier topology. Several issues such as the high-speed switching behavior of the semiconductors, turn-off delay of the applied MOSFETs and switching losses are addressed and a novel magnetically coupled damping layer is introduced to attenuate occurring switching transient oscillations. A detailed loss model of the rectifier is derived which is used to calculate the possible efficiency of the rectifier circuit. Based on the calculated results a η-$\mathrm{THD_I}$-Pareto Front is finally sketched, illustrating the existing basic relation between efficiency and input current quality.
In addition, the implementation of the digital current controller using an FPGA is given. Also an improved CM noise model of the Vienna Rectifier system is derived and a novel concept for eliminating the CM voltage of the rectifiers output is analyzed.
Finally, the construction of the rectifier prototype is shown and measurements taken from the implemented rectifier are given which verify the proper operation of the system.

The two-level Δ-switch rectifier system is the scope of **Chapter 6**. After discussion of the basic operating principle including the appearing DM and CM voltages a novel phase-oriented current control concept using pulse-width modulation is proposed.

Next to a derivation of a detailed loss model also the reactive power capability of the Δ-switch rectifier topology is treated and it is shown how this feature can be used to improve the power factor of the rectifier circuit. Experimental results taken from the implemented hardware prototype confirm the calculated results. Finally, a comparison of the Δ-switch rectifier topology with the Vienna Rectifier topology is given.

In **Chapter 7** the data of actually constructed Vienna Rectifier circuits with different switching frequencies are used to derive a Pareto Front regarding efficiency and power density (η-ρ-Pareto Front). Also the actually achieved volume reduction due to an increase in switching frequency is discussed.

Chapter 2

Comparison of Unidirectional Rectifier Topologies

Many possibilities are conceivable for implementing a mains interface for electrical driven actuators. The interface can either be implemented using a direct AC-AC conversion (cf. **Fig. 2.1(a)**) such as the Matrix Converter (MC) or the Indirect Matrix Converter (IMC) or by two-stage solutions based on an "inner" storage element. The two-stage solutions can either be classified into DC Voltage Link Back-to-Back connected Converters (VLBBC) using a capacitor in the DC link (cf. **Fig. 2.1(b)**) yielding to an impressed voltage in the DC link or, alternatively into a DC Current Link Back-to-Back connected converters (CLBBC) using an inductor as storage element (cf. **Fig. 2.1(c)**) which is characterized by an impressed current in the DC link. In a broader sense, also passive rectifier topologies can be included to the VLBBC category. The stringent requirements on power factor and input current quality in aircraft (cf. section 1.1.2), however, inhibit the application of a simple diode rectifier bridge.

As shown in **Fig. 2.1(d)**, the low-frequency harmonics generated by the diode bridge can be compensated by an active filter connected to the grid. Such active filter structures are analyzed in [34] and [35] for

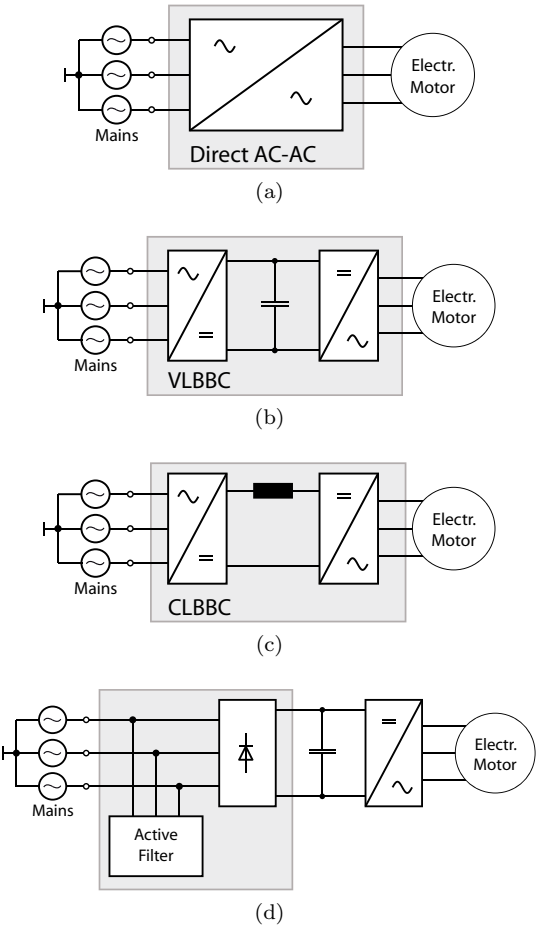


Fig. 2.1: Possible solutions for three-phase AC-AC converters; (a) Direct AC-AC conversion (e.g., Matrix Converter, Indirect Matrix Converter, etc.); (b) Two-stage conversion using back-to-back connected voltage source converters and (c) using current source converters. (d) Mains interface using a standard diode bridge in combination with an active filter compensating the harmonics generated by the diode bridge.

aerospace applications. Further contributions on active power filters and examples can be found in [36, 37, 38].

Direct AC-AC conversion using a MC in MEA applications is discussed extensively in [18, 39, 40, 41, 42]. An overview on matrix converters can be found in [43] and a detailed discussion of direct AC-AC converters can be found in [44]. It seems to be a good approach to implement these converter systems for MEA requiring high power density as an energy storage element such as the DC-link capacitor is omitted. Matrix converters have therefore been subject of topology evaluations and comparisons where the structure is benchmarked relative to a VLBBC [45, 46, 47]. According to the evaluations, the MC shows a slightly better efficiency and a volume reduction of the passive components including heat sink can be achieved. A volume reduction by a factor of 1.5 is for instance reported for the system given in [45] with a switching frequency of 32 kHz.

Despite the advantages of a slightly higher efficiency and smaller total volume, the MC shows also some serious drawbacks. The main drawbacks are the limited maximum output voltage of 86.6 % of the mains voltage, and the need of an active clamping circuit for mains failures. The system can, furthermore, not handle an outage of a single phase. In addition, a more complex and more powerful controller is required as an easy PWM control of the input currents is not possible. Also the statement, that a MC does not have "any" energy storage element, has to be revised as the MC requires input capacitors for proper operation and it can be argued that the intermediate storage element of a VLBBC is somehow shifted to the input.

According to [45], the MC does not provide the best solution for applications requiring high-load dynamics or single-phase operation due to the lack of a main energy storage element and shows good results only for loads where low dynamic performance is required or achievable due to high inertia. Due to this set of disadvantages, the MC is not an ideal solution for the application in MEA and is therefore not further discussed in this work.

The topology evaluation given in [47] is performed for switching frequencies between 40 kHz and 140 kHz. This evaluation also includes a CLBBC converter which, unfortunately, shows higher weight compared to the MC and the VLBBC. The classical VLBBC is therefore an ideal candidate for an implementation showing high power density and low weight. Due to the missing on-board storage element in MEA applications energy feedback into the mains is not allowed and hence only unidirectional front ends are considered.

In the following an overview of unidirectional rectifier circuits is given where the focus is laid on rectifier systems with low weight and high power density as those are the main requirements for MEA applications. Comparisons and reviews of rectifier topologies can be found in [49, 50, 51] and a more comprehensive comparison is presented in [48] which is the basis of the following discussion.

Unidirectional rectifier systems can basically be divided into passive systems, hybrid systems and active systems. Passive systems use either a line commutated diode or thyristor bridge without any active current control. This results in low-frequency harmonics in the input currents and basically in an uncontrolled output voltage. Hybrid systems on the contrary exhibit either partly controlled input currents or output voltages. They therefore employ low-frequency as well as high-frequency passive components. Active rectifier systems show a controlled output voltage and controlled, sinusoidally shaped mains currents.

2.1 Passive Systems

Passive systems using a three-phase diode bridge usually exhibit high input current peaks which results in a very poor input current quality and power factor. The conduction interval can, however, be enlarged if either three inductors are inserted on the AC-side or a single inductor is inserted on the DC-side of the rectifier bridge. This considerably improves system performance but still a $\mathrm{THD_I}$ above 30 % and a power factor below 0.952 exists. In addition, the concept of passive third harmonic injection can be used to improve the input current quality as shown in [52] and a $\mathrm{THD_I}$ of 5 % at full load can be achieved using this method.

The input current quality can be enhanced considerably if two or more phase-shifted rectifier bridges are connected in parallel which results in passive multi-pulse rectifier systems. Transformers are either used for phase-shifting and isolation and such systems are called Transformer Rectifier Units (TRU) or Auto Transformers in combination with Rectifiers (ATRU) are applied if isolation is not

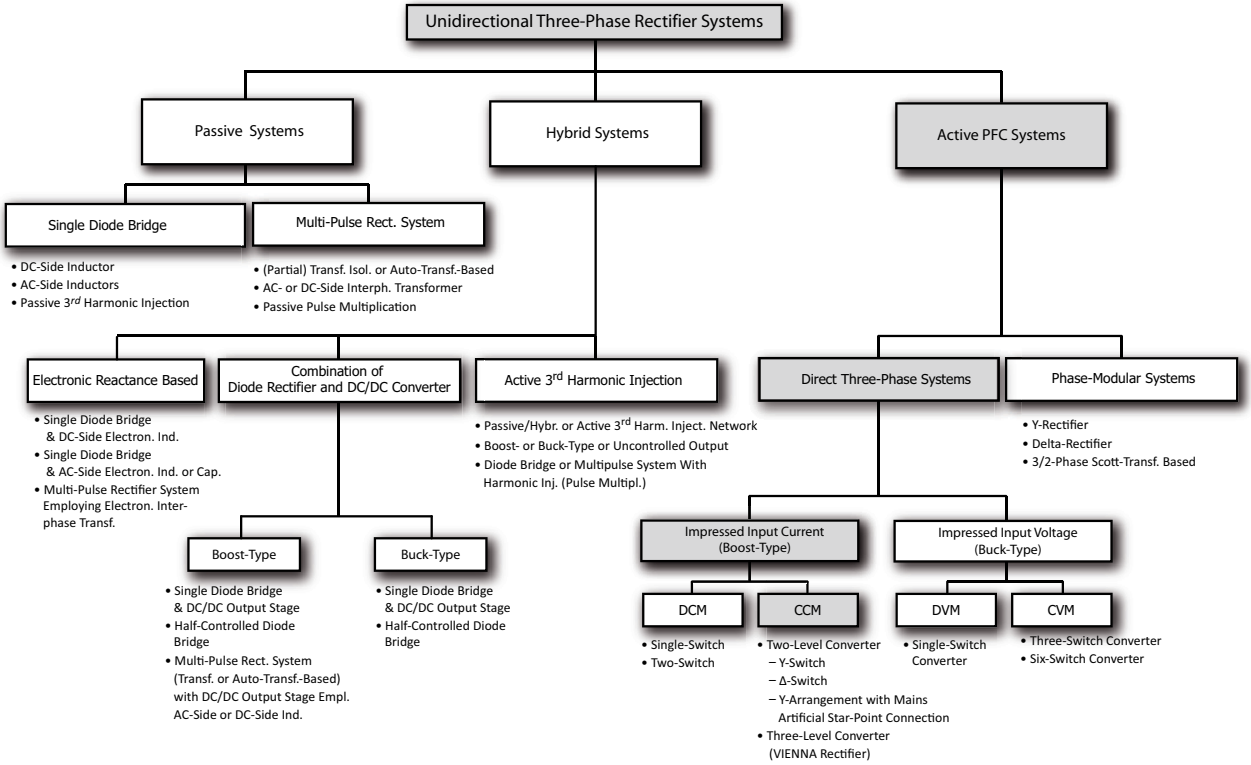


Fig. 2.2: Overview of unidirectional rectifier systems according to [48].

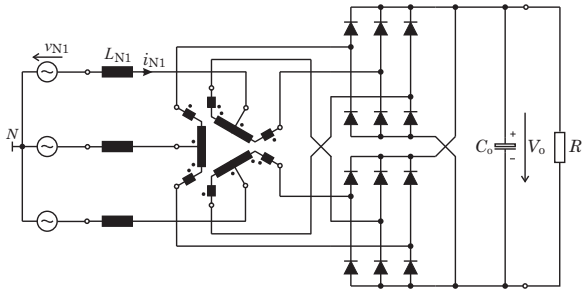


Fig. 2.3: Passive 12-pulse rectifier system with interphase transformer located on the AC-side [53].

needed. The interphase transformer can be placed on the AC-side as shown in **Fig. 2.3** for a 12-pulse rectifier system [53] which results in an impressed DC voltage. Alternatively the interphase transformer could be inserted on the DC-side as demonstrated in [54].
Multi-pulse rectifier circuits, usually 18-pulse rectifier circuits, are common rectifier topologies in MEA [55, 56, 57, 58, 59]. The 12-pulse rectifier circuits can comply with the harmonic limits of the airborne standard DO160F (cf. **TABLE 1.1**), however, in order to comply with the more stringent harmonic limits of major OEMs such as Boeing or Airbus, 18-pulse rectifier system are required. Multi-pulse rectifier systems are very robust and due to their relatively large mass, high short-term overloads can be handled. On the other hand, such rectifier systems offer no dedicated control of the DC voltage, show limited input current quality (e.g. $\mathrm{THD_I} = 6 - 9\,\%$ for 18-pulse rectifier systems) and exhibit a high weight due to the low-frequency transformer or auto-transformer. Enhanced rectifier topologies are therefore required to overcome this drawbacks.

2.2 Hybrid Systems

In order to improve the input current quality the concept of third harmonic injection can be applied. A specific amount of current is injected either into one phase or in all three phases resulting in the effect that zero mains current periods are avoided. The most famous

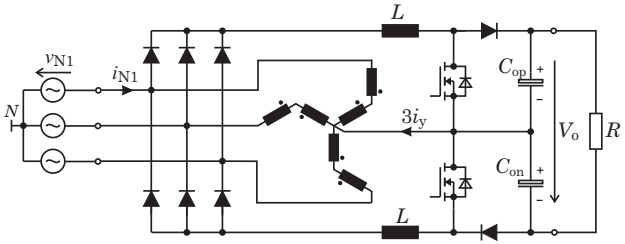


Fig. 2.4: Minnesota rectifier using third harmonic injection into all three-phases to achieve sinusoidal main currents.

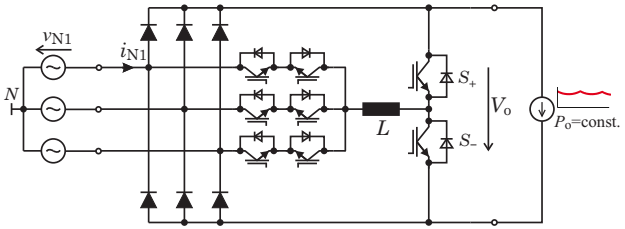


Fig. 2.5: Three-phase rectifier circuit using third harmonic injection always into only one phase (Korea Rectifier [62]).

topology has been proposed by Prof. N. Mohan in 1995 and is known as Minnesota rectifier [60, 61] (cf. **Fig. 2.4**). It uses two cascaded boost converters at the output and a third harmonic current injection transformer. The rectifier system shows a controlled output voltage and purely sinusoidal mains currents. The main drawback of the topology is the bulky, low-frequency current injection transformer which shows a high weight. This inhibits the application of this promising approach in aircraft applications.

The bulky and heavy third harmonic injection network can be omitted if the current is injected always into only one phase. An interesting approach has been proposed in [62, 63] and the basic structure of the rectifier system is given in **Fig. 2.5**. The system uses only a single inductor and three bidirectional, bipolar switches for injection of the current into one phase. The current in the inductor L is modulated by the transistors S_+ and S_-. The three bidirectional switches connect always the phase with smallest (absolute) voltage value to the inductor

and only one switching action is therefore required every 60 ° of the mains period. Only S_+ and S_- are hence modulated with switching frequency. Due to the small current level injected into the third phase, low conduction losses occur in the bidirectional switches, in the inductor and in the two high-frequency modulated transistors. This finally results in a very high efficiency. A rough estimation yields to an achievable efficiency of almost 99 %. Sinusoidal input currents are, however, only achieved for constant power loads as indicated in **Fig. 2.5**. The output voltage of the rectifier system is uncontrolled and the output capacitor must be small so that a 6-th harmonic voltage shape on the DC side can occur. Application of electrolytic capacitors is therefore omitted. In addition, the system cannot deal with an outage of a single phase. Due to its high efficiency and due to the low complexity it is, however, an interesting approach where a controlled output voltage is not needed and for applications where a constant power load is connected to the output of the rectifier circuit.
Output voltage control could, however, be achieved by inserting an "electronic inductor" [64] on the positive DC rail which produces the required current shape.

A topology using third harmonic injection only into one phase in combination with boost circuits for output voltage control is presented in Fig. 5(e) of [51]. This topology would show sinusoidal input currents and a controlled output voltage with a voltage level near to the rectifier AC voltage but suffers from the high voltage stress of the semiconductors.

The performance of multi-pulse rectifier systems can also be improved if the diode bridge rectifiers are combined with DC/DC boost-type output stages. The required inductors can be located either on the DC side [65, 66] or on the AC side [67]. These rectifier types are member of the hybrid rectifiers category as passive low-frequency elements are combined with high-frequency elements for current shaping or output voltage control or both. A 12-pulse hybrid rectifier system with inductors located on the AC side is given in **Fig. 2.6**. Two boost-type output stages are there used for modulation of the diode bridge output voltage. A detailed analysis of the the rectifier is given in [68] where it is also compared to an implementation using only one switch. A more comprehensive closed-loop control implementation is furthermore

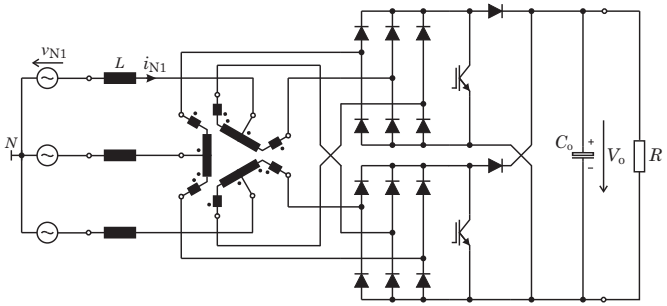


Fig. 2.6: Schematic of a hybrid 12-pulse ATRU using two boost stages at the output impressing/modulating the diode bridge current.

discussed in [69].
Using this hybrid approach a THD_I below 2 % at full load can be achieved and an efficiency of 95 % can be measured for $f_N = 400\,Hz$, $V_N = 115\,V$ and $P_o = 10\,kW$. The power factor is, however, below 0.96. This method allows to control the output voltage at almost sinusoidal input current shape and is a good approach to improve the behavior of the passive rectifier circuit. Due to the large size of the constructed prototype it shows, however, only a power density of $1.55\,kW/dm^3$. In addition a power to weight ratio of only 122 W/kg is achieved because of the low frequency magnetic components. Also the low power factor below 0.96 does not ideally fit the needs for aerospace applications.

2.3 Active Systems

Active PFC rectifier circuits are well suited for implementing a rectifier system with high power density, low weight and high input current quality. According to **Fig. 2.2**, the active rectifier topologies can be divided into phase-modular systems and direct three-phase rectifier systems. Phase-modular systems use a single-phase rectifier stage for each phase. The individual rectifier systems can either be connected in star, called Y-Rectifier [70, 71] (cf. **Fig. 2.7(a)**), or between the phases which is called Δ-Rectifier [72] (cf. **Fig. 2.7(b)**). The phase units show individual output voltages and according to **Fig. 2.7** isolated DC/DC converter stages are required if a single DC output voltage should be

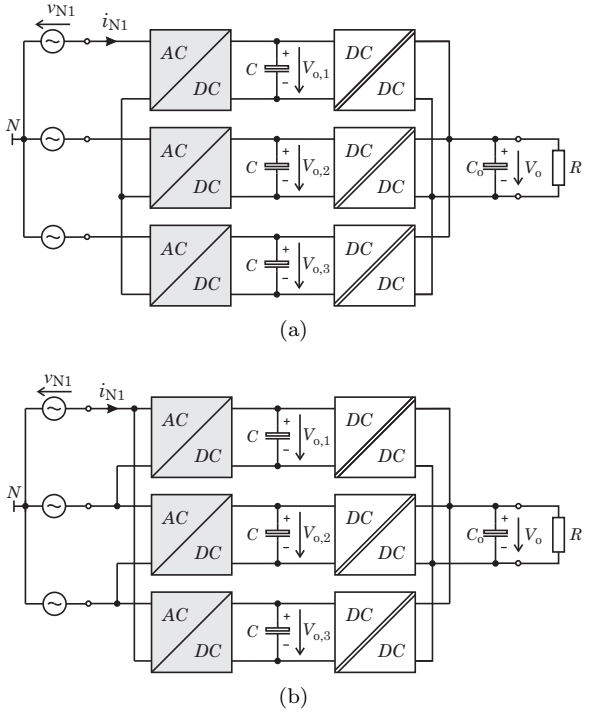


Fig. 2.7: Basic structures of phase-modular rectifier systems. On the AC-side the systems can (a) either be connected in star (Y-Rectifier) or (b) between the phases (Δ-Rectifier). Isolated DC/DC converter stages are required if a common DC output voltage should be generated.

built. Compared to a direct three-phase rectifier system large capacitors must be applied in the individual DC links of the modular systems as a pulsating power flow, being typical for single-phase systems, occurs. Also balancing issues of the three independent outputs have to be addressed. On the other hand, in particular the Δ-Rectifier shows the advantage that the system can further operate with full output power in case of a single phase loss if the diode bridges are replaced by three-phase thyristor bridges. Overall, the modular systems show good results but as typically a DC/DC converter is required for each phase these systems are not the first choice to achieve highest power density.

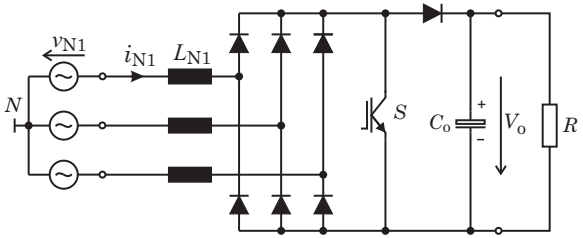


Fig. 2.8: Single-switch three-phase rectifier system operating in discontinuous operation mode.

Direct three-phase rectifier circuits perform a direct energy conversion from the three-phase AC-mains to a single DC-bus. In a symmetrical three-phase mains a continuous power flow exists which results in a reduced current stress of the rectifiers output capacitor. Direct three-phase rectifier systems can generally be classified into boost-type and buck-type rectifier systems. Buck-type rectifier systems, such as the Three-Switch Buck Rectifier System [73] or the Six-Switch Buck Rectifier System [74], exhibit an output DC voltage which is below $V_o = \frac{3}{2}\hat{V}_N$ if they are not combined with a boost-type DC/DC converter. They show discontinuous input phase currents and therefore a relatively high filtering effort using capacitors must be accepted. The large amount of input capacitors, however, is in contradiction to the required power factor at mains frequencies of 360 Hz - 800 Hz. Buck-type rectifier systems are therefore not very well suited for aerospace applications and not further discussed in this work. The same is true for Matrix Converters which exhibit a similar input current behavior and filter requirement or both.

A very simple direct three-phase rectifier circuit is the single-switch three-phase boost rectifier [75,76] shown in **Fig. 2.8**. The system operates in DCM mode and the switch is modulated with a constant duty cycle which means that no PWM as well as no current measurement is required. The system shows, however, discontinuous input currents and high current peak values which results in a large EMI filter demand. The performance can be improved by three-level arrangement or by interleaved operation of two systems as discussed in [77] but similar to buck-type rectifier systems this topology is not suited for aerospace applications and hence not further discussed here.

Three-phase rectifier systems can furthermore be divided into two-level and three-level topologies utilizing either two or three voltages levels for PWM voltage formation. Three-level rectifiers show a smaller current ripple which allows to reduce the size of the boost inductor compared to two-level systems. Dependent on the rectifier topology, either all or only some of the semiconductors are stressed with half of the output voltage which results in reduced switching losses and reduced DM filtering effort. The reduced voltage stress also allows to employ today's SJ MOSFETs which enable switching frequencies beyond 50 kHz. The possibility of using such high switching frequencies is the main reason why three-level three-phase rectifier systems are very well suited to implement very high power densities. This statement may, however, loose its generality as recently SiC-MOSFETs have been developed [78]. They show a low on-state resistance, a high break down voltage and they allow high switching frequencies even for devices with a breakdown voltage of 1200 V.
Three-level rectifier systems also show some drawbacks. On one hand a higher complexity of the system is present and on the other hand an additional controller for balancing the two output voltages is required. The advantages, however, overrule the drawbacks for applications where high power density is required at a mains voltage level of 230 V.

The most famous representative of a unidirectional three-phase three-level rectifier system is the Vienna Rectifier topology shown in **Fig. 2.9(a)** [79, 80]. This is the "original" VR topology although the name is often used in literature for unidirectional implementations where all three phases can be connected to the output voltage midpoint. The VR system requires only three switches and all semiconductors (diodes and MOSFETs) are only stressed with half of the output voltage. The system shows a high reliability as a short circuit of the DC bus is not possible. In the original implementation always two diodes are conducting current. The linked conduction losses can be reduced if six switches are used instead (cf. **Fig. 2.9(b)** [81]).

The recent development of reliable SiC Schottky diodes with a blocking voltage of 1200 V and ideally no reverse recovery current support an implementation shown in **Fig. 2.10**. The diodes are there stressed with full output voltage whereas the switches are only stressed with $V_o/2$. The main advantage of this topology is its very high efficiency and a

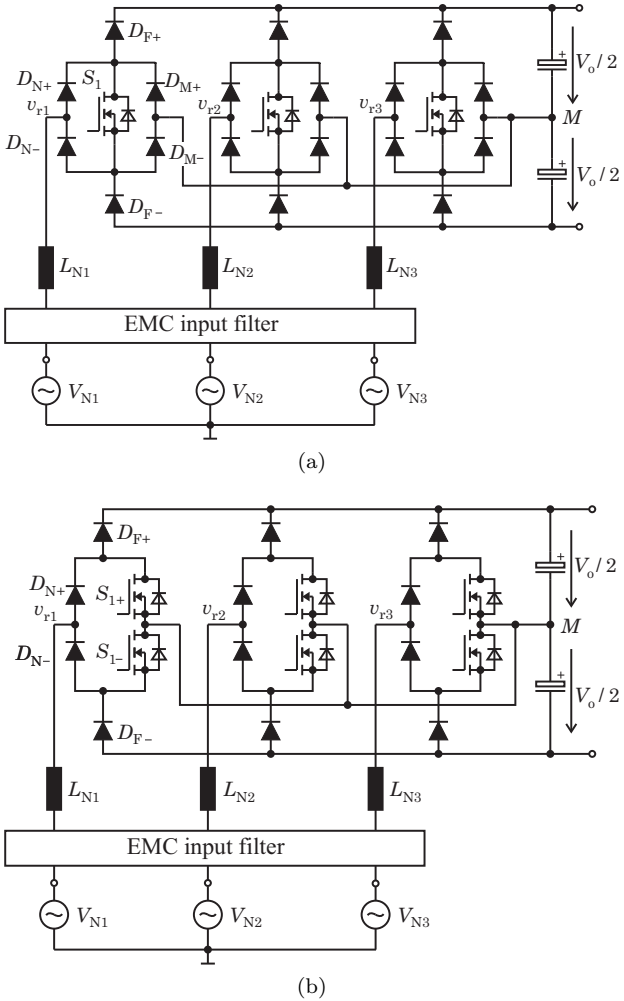


Fig. 2.9: (a) Power circuit of the three-phase three-level Vienna Rectifier topology [79, 80] and (b) of the three-phase three-level six-switch Vienna-type rectifier [81] system showing reduced conduction losses at higher power levels.

rough estimation of power losses reveals that an efficiency of nearly 99 % is possible for a 10 kW rectifier system operating at $f_N = 50$ Hz.

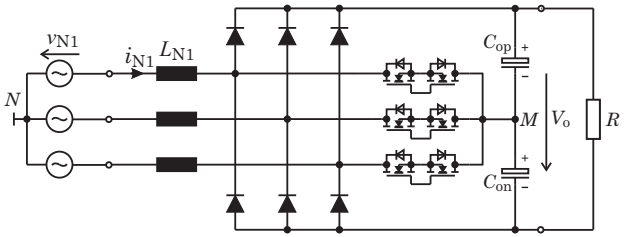


Fig. 2.10: Three-level Vienna-type rectifier circuit showing very high efficiency if SiC-diodes are applied.

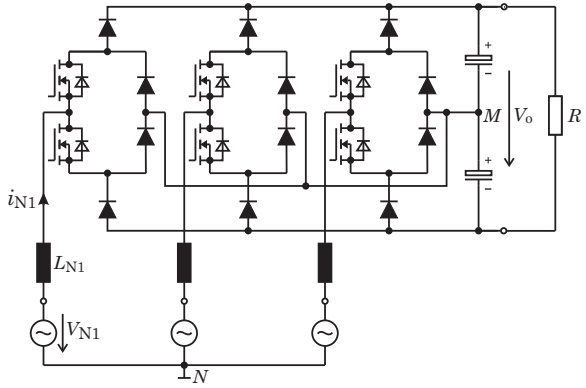


Fig. 2.11: Unidirectional three-phase rectifier circuit based on the NPC converter [82].

A derivation of unidirectional three-phase rectifier circuits based on conventional bidirectional rectifier topologies such as the Neutral Point Clamped (NPC), the Flying Capacitor and the converter employing symmetric Cascaded H-Bridges is discussed in [82]. A unidirectional rectifier topology based on the NPC converter (cf. **Fig. 2.11**) is there proposed and an improved efficiency is predicted if synchronous rectification is used. The topology is an interesting solution, however, a more detailed analysis and experiences taken from a practical implemented prototype are still needed.

In order to further reduce the voltage stress of the semiconductors or increase the operating voltages of the rectifier systems the number

of levels can be increased. In [83], unidirectional multi-level rectifier systems based on the topology shown in **Fig. 2.10** are proposed and carrier-based PWM strategies are derived. A five-level three-phase rectifier system for aircraft applications is proposed in [84], which is a combination of a NPC rectifier and a flying capacitor rectifier. Those systems suffer from the large amount of required switches; furthermore, multiple output capacitors have to be balanced. They show, however, no significant advantages for the intended voltage and power range ($V_N = 115/230\,V$, $P_o = 10\,kW$) and are therefore not further discussed here.

Altogether, the three-phase VR topology is an ideal candidate for implementing a rectifier system for aerospace applications showing a high power density, a low weight and a high performance regarding power factor and input current quality. This is also confirmed by the comparative evaluation given in [85] where the VR topology is compared with a 12-pulse passive rectifier system (cf. **Fig. 2.3**) and a conventional six-switch rectifier circuit (cf. **Fig. 2.14**) and where the VR topology scores well. The VR topology using six switches as shown in **Fig. 2.9(b)** is therefore an ideal candidate for an implementation for the voltage range of 230 V.

In todays commercially used aircraft, a mains voltage of 115 V and a fixed frequency of 400 Hz exists (see also section 1.1). Also in future aircraft the AC bus with 115 V will be available so that existing equipment, including equipment on the ground, can still be used. The voltage stress on the semiconductors employed in three-level topologies is only 200 V for a total DC bus voltage of 400 V and semiconductors with a blocking voltage around 350 V would be required. Such semiconductors are, unfortunately, not commercially available and 600 V devices must be used instead which show an increased on-state resistance. The three-level VR system can therefore not show its strength and two-level rectifier systems are the preferred solution.

A survey on (unidirectional) two-level rectifier systems can be found in [50, 86]. In [87], a topology using either Y-connected (Y-switch rectifier, cf. **Fig. 2.12(a)**) or Δ-connected (Δ-switch rectifier, cf. **Fig. 2.12(b)**) bidirectional switches on the AC side is presented and the operation analysis of the Δ-version using SVM in combination

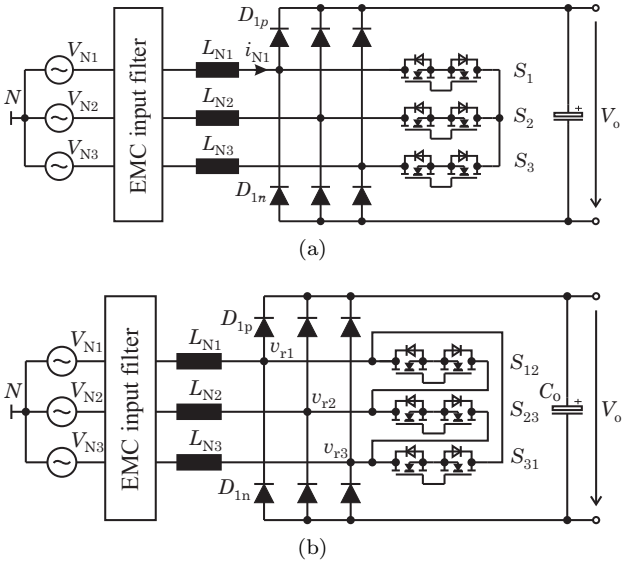


Fig. 2.12: Active three-phase two-level rectifier systems using (a) Y-connection (Y-switch rectifier) and (b) Δ-connection (Δ-switch rectifier) of the bidirectional switches.

with hysteresis control is discussed in [88]. In general, the Y-connected implementation shows higher conduction losses as compared to the Δ-connected alternative, as there are always two (bidirectional) switches connected in series. A short-circuit of the DC-voltage is not possible with either topology. In both implementations the semiconductors are stressed with the full output voltage which inhibits the application of MOSFETs for $V_N = 230\,V$. SJ devices with a blocking voltage of 650 V can, however, be applied for a mains voltage of 115 V and $V_o = 400\,V$. As shown in [86], also a single three-phase rectifier power module with low current rating can be used for implementation.

Two possibilities of implementing the bidirectional (current), bipolar (voltage) switches using MOSFETs are given in **Fig. 2.13**. The original VR topology (cf. **Fig. 2.9(a)**) uses the bidirectional switch shown in **Fig. 2.13(b)** instead of the two MOSFETs per phase-leg shown in **Fig. 2.12(b)**. An elegant topology, which integrates the bidirectional switch of **Fig. 2.13(b)** into the diode bridge, is shown in [89, 90]. The

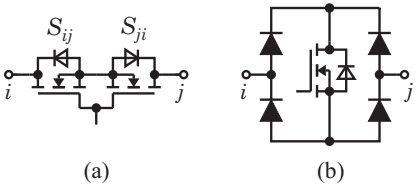


Fig. 2.13: Possible implementations of a bidirectional (current), bipolar (voltage) switch using (a) two MOSFETs and (b) a MOSFET and a diode bridge.

conduction losses of this version are, however, higher than those when two MOSFETs (cf. **Fig. 2.12(b)**) are used.
In addition, some topologies using quasi tri-directional switches [91] or topologies operating in discontinuous conduction mode are shown in [92, 93]. The topology using tri-directional switches increases the system complexity and DCM topologies cannot meet the requirements for the total harmonic distortion. Due to its low complexity, low conduction losses and high reliability the Δ-switch rectifier topology seems to be an optimal choice for implementation of a rectifier for aerospace applications with a mains voltage of 115 V and a DC bus voltage of 400 V. The Δ-switch rectifier circuit will therefore be analyzed in detail in section 6 where also a novel current control concept is proposed. The proper operation of the rectifier circuit is verified by measurements taken from the constructed hardware prototype.

2.4 Bidirectional Rectifier Circuits

In future aircraft, feedback of energy into the mains might be allowed and therefore a short discussion of two- and three-level bidirectional rectifier circuits is given in the following.

The most common direct three-phase boost-type rectifier system is the two-level six-switch PWM rectifier bridge as shown in **Fig. 2.14**. The rectifier structure is simple, robust and power modules as well as auxiliary components are available from several manufacturers. Drawbacks are reduced reliability due to possible shoot-through of a bridge leg resulting in a short circuit of the DC-voltage, the high

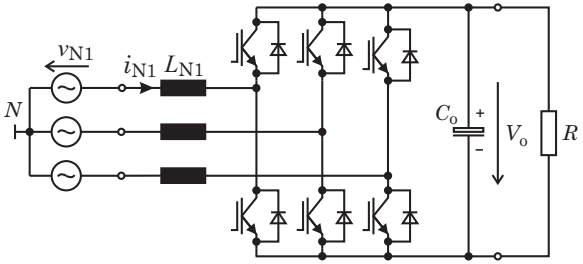


Fig. 2.14: Commonly used bidirectional three-phase two-level PWM rectifier system.

current stress on the semiconductors, and the involvement of the MOSFET body diode causing a substantial limitation of the switching frequency. Also the boost inductors show a large volume due to the two-level nature.

The three-level bidirectional T-type neutral point clamped (NPC) rectifier system shown in **Fig. 2.15(b)** can be derived by replacing the diodes of the VR structure given in **Fig. 2.10** with transistors. A three-level bidirectional I-type NPC converter can similarly be derived by replacing the diodes in **Fig. 2.11** by transistors (cf. **Fig. 2.15(b)**). According to [94], the three-level rectifier circuits show a higher efficiency than the six-switch rectifier circuit for higher switching frequencies. Similar to the unidirectional rectifier system the semiconductors of three-level rectifiers are stressed with lower level voltages which lowers switching losses. Furthermore, the volume of the passive components can be reduced. They show, however, increased conduction losses and a considerably increased complexity and implementation effort.
Bidirectional rectifier systems show a better input current quality than unidirectional rectifier systems as they avoid intervals with zero current in the vicinity of the zero crossing. Bidirectional systems can also compensate a large amount of reactive power which is only possible to a limited extend for unidirectional rectifier systems.

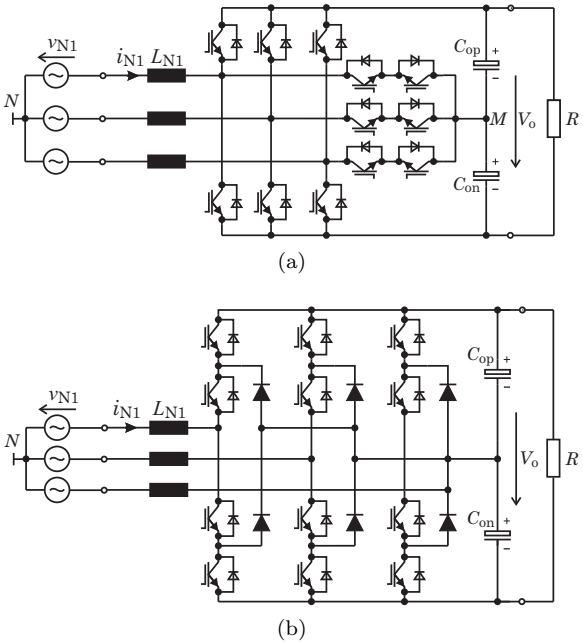


Fig. 2.15: Bidirectional three-phase three-level rectifier circuits. (a) Three-level T-type NPC rectifier and (b) three-level I-type NPC rectifier.

Chapter 3

Three-Phase Vienna Rectifier

In this chapter the basic operation of the three-phase three-level Vienna Rectifier topology will be discussed. Some of the material has already be discussed in previous publications. The widespread informations will be summarized here and considerably extended at specific points. Based on a short description of the basic operation of the rectifier system design guidelines for the power circuitry will be given. Corresponding models for the design of an appropriate controller structure, consisting of a three-phase current controller, an output voltage controller and an output voltage symmetry controller will be derived. It will be demonstrated again that the three-level VR topology shows redundant switching states which can be used advantageously to balance the output voltages of the three-level topology. The information given in this chapter can be used to design a proper VR system and are the base for the optimization of the power density discussed in section 5.

3.1 Basic Operation

The power circuit of the original VR topology as published in [79], [80] is given in **Fig. 3.1(a)**. The topology consists of three bidirectional switches, implemented using a single unidirectional switch S_i in

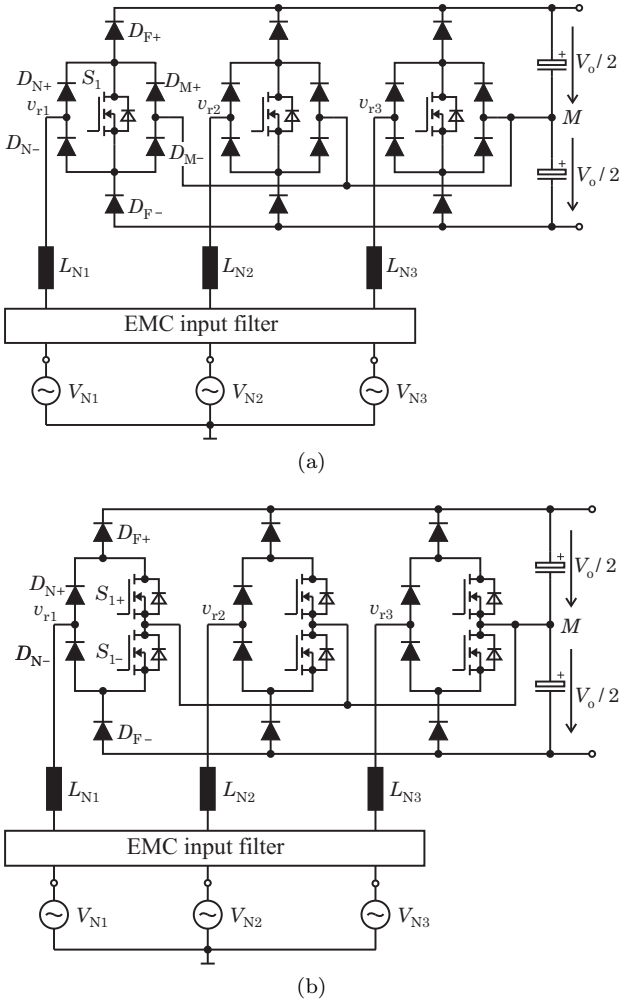


Fig. 3.1: (a) Power circuit of the three-phase three-level Vienna Rectifier topology [79, 80] and (b) of the three-phase three-level six-switch Vienna-type rectifier [95] system showing reduced conduction losses at higher power levels.

combination with a diode bridge, which are advantageously integrated in the diode bridge D_{F+}, D_{F-} of the rectifier system. The output capacitors are split and the bidirectional switches are connected to the

output voltage midpoint M. Two diodes of the bidirectional switch implementation are connected to the mains ($D_{\mathrm{N}+}$ and $D_{\mathrm{N}-}$) and two diodes are connected to the output voltage midpoint M ($D_{\mathrm{M}+}$ and $D_{\mathrm{M}-}$). The input of the rectifier system, which is connected to the boost inductor $L_{\mathrm{N}i}$, can now either be switched to M (0) by closing S_i or, depending on the current direction, switched to the positive voltage rail ($+V_{\mathrm{o}}/2$) or to the negative voltage rail ($-V_{\mathrm{o}}/2$) by the free-wheeling diodes $D_{\mathrm{F}+}$ and $D_{\mathrm{F}-}$ which finally results in the three-level system behavior.
The mains side diodes $D_{\mathrm{N}+}$ and $D_{\mathrm{N}-}$ are only commutated with mains frequency, $D_{\mathrm{N}+}$ conducts during the whole positive half-wave and $D_{\mathrm{N}-}$ conducts during the negative half-wave. The input currents commutate with switching frequency between the free-wheeling diodes $D_{\mathrm{F}+}$ or $D_{\mathrm{F}-}$ and the switches S_i. Fast-recovery diodes must therefore be used for $D_{\mathrm{F}+}$ and $D_{\mathrm{F}-}$ in order to limit switching losses, whereas for all other diodes standard rectifier diodes can be applied.

The current flows through two diodes in every switching state which results in considerable conduction losses. In order to reduce the conduction losses, the diodes $D_{\mathrm{M}+}$ and $D_{\mathrm{M}-}$ can be removed if two switches are used instead of a single switch which is shown in **Fig. 3.1(b)**. This configuration is a six-switch version of the three-level Vienna Rectifier and was first published in 1993 [95]. The two switches show a low utilization compared with the original VR topology which employs only a single switch but better cooling can be performed as the power losses are distributed to two devices. In addition the commutation path can be optimized easier as the switch S_{i+} only commutates with the diode $D_{\mathrm{F}+}$ and the switch S_{i-} with $D_{\mathrm{F}-}$. The fundamental operation of the six-switch version given in **Fig. 3.1(b)** is equal to the original VR topology and therefore in the following only the six-switch version will be discussed. It will be denominated as Vienna Rectifier even if it is not exactly the original VR topology.

Dependent on the state s_i of the corresponding switch ($s_i = 1$ denotes that the switch S_i is conducting) and the input current direction ($\mathrm{sign}(\mathrm{i}_{\mathrm{N}i})$), the rectifier voltage of each phase is given by

$$v_{\mathrm{r}i} = \begin{cases} \frac{V_{\mathrm{o}}}{2}\mathrm{sign}(i_{\mathrm{N}i}) & \text{for } s_i = 0 \\ 0 & \text{for } s_i = 1 \end{cases} . \tag{3.1}$$

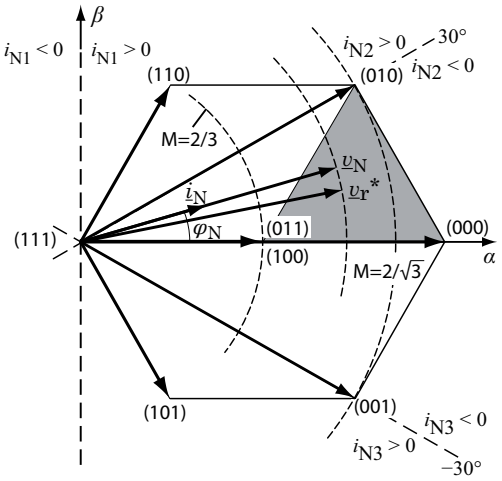


Fig. 3.2: Space vector diagram of the three-phase three-level VR topology for the sector $\varphi_N \in [-30°, 30°]$ ($i_{N1} > 0$, i_{N2}, $i_{N3} < 0$).

Using space vector calculus the corresponding voltage space vector

$$\underline{v}_r = \frac{2}{3}(v_{r1} + \underline{a}v_{r2} + \underline{a}^2 v_{r3}) \text{ with } \underline{a} = e^{j\frac{2\pi}{3}} \tag{3.2}$$

can be calculated. With the VR topology in total eight different discrete voltage space vectors can be generated which are shown in **Fig. 3.2** for $\varphi_N \in [-30°, +30°]$ ($i_{N1} > 0$, i_{N2}, $i_{N3} < 0$). There, (s_1, s_2, s_3) describe the different switching states where e.g. (010) denotes that S_2 is turned on and S_1 and S_3 are turned off. In addition the boundary of areas with equal input current directions is shown, e.g. i_{N1} shows a positive direction in the whole right half plane. It is obvious that the switching states (011) and (100) result in equal voltage space vectors and are therefore equivalent for generation of the input currents. As will be discussed below these two redundant switching states, however, lead to different current directions in the connection to the output voltage midpoint M which can be used for balancing of the two output voltages. The modulation index

$$M = \frac{\hat{V}_N}{\frac{V_o}{2}} \tag{3.3}$$

describes the modulation index of the system and according to **Fig. 3.2** a maximal value of of $M = \frac{2}{\sqrt{3}}$ is possible. A higher rectifier or mains

voltage or both would result in significant input current distortions due to over-modulation.
Using the voltage space vector of the mains

$$\underline{v}_{\mathrm{N}} = \hat{V}_{\mathrm{N}}\ e^{j\varphi_{\mathrm{N}}}\ ,\ \ \varphi_{\mathrm{N}} = \omega_{\mathrm{N}} t \tag{3.4}$$

the input current space vector

$$\underline{i}_{\mathrm{N}} = \hat{I}_{\mathrm{N}}\ e^{j\varphi_{\mathrm{i_N}}} \tag{3.5}$$

is given by

$$\underline{v}_{\mathrm{N}} - \underline{v}_{\mathrm{r}} = L_{\mathrm{N}} \frac{d\underline{i}_{\mathrm{N}}}{dt}\ . \tag{3.6}$$

As only discrete voltage space vectors can be generated by the rectifier system the desired voltage space vector $\underline{v}_{\mathrm{r}}^{*}$ has to be approximated by the time average over one switching period using the surrounding discrete voltage space vectors. The approximation for the desired voltage space vector $\underline{v}_{\mathrm{r}}^{*}$ given in **Fig. 3.2** (and for all other voltage space vectors in the gray shaded area) can be performed by the switching states (000), (010), (011) and (100),

$$\underline{v}_{\mathrm{r}}^{*} = \delta_{(100)}\underline{v}_{\mathrm{r},(100)} + \delta_{(000)}\underline{v}_{\mathrm{r},(000)} + \delta_{(010)}\underline{v}_{\mathrm{r},(010)} + \delta_{(011)}\underline{v}_{\mathrm{r},(011)}\ , \tag{3.7}$$

where

$$\delta_{(100)} + \delta_{(000)} + \delta_{(010)} + \delta_{(011)} = 1\ . \tag{3.8}$$

The on-times $\delta_{(\mathrm{xxx})} \in [0 \ldots 1]$ of the particular voltage space vectors $\underline{v}_{\mathrm{r},(\mathrm{xxx})}$ can be calculated using simple geometrical relations and a detailed calculation can be found in [96]. The on-times can be used to implement a space vector control of the rectifier system and examples for such a space vector control can be found in [97, 98, 99].
The sequence of the switching states is essential for obtaining minimal switching losses which can be achieved by a minimizing the number of switching actions. The optimal switching sequence for the voltage space vector given in $\underline{v}_{\mathrm{r}}^{*}$ is

$$\Big|_{0}(100) - (000) - (010) - (011) - \Big|_{\frac{T_{\mathrm{s}}}{2}} - (011) - (010) - (000) - (100)\Big|_{T_{\mathrm{s}}}\ . \tag{3.9}$$

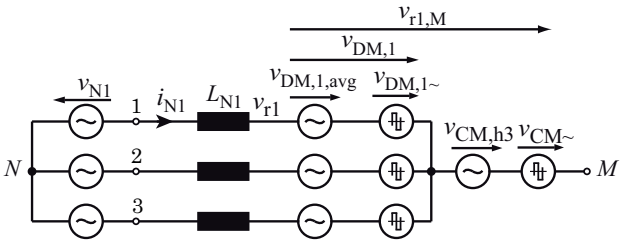


Fig. 3.3: Equivalent circuit of the Vienna Rectifier system where the rectifier voltage $v_{\mathrm{r1,M}}$ is split into a DM voltage components $v_{\mathrm{DM,1}}$ and in a CM voltage component V_{CM}.

Any following switching state can be reached by a single switching action i.e. by changing the state of only one switch and the switching states at the end and at the beginning of the switching sequence are equal. In addition the switching sequence is symmetrical to half of the pulse period $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$.

In **Fig. 3.3** the equivalent circuit of the VR is shown where the voltage formation is represented by voltage sources. The corresponding waveforms are plotted in **Fig. 3.4**. The rectifier voltage $v_{\mathrm{r1,M}}$ (measured from v_{r1} to M)

$$v_{\mathrm{r1,M}} = v_{\mathrm{DM,1}} + v_{\mathrm{CM}} \tag{3.10}$$

can be split into a DM voltage component $v_{\mathrm{DM,1}}$ and in a voltage component common to all three phases (CM voltage component v_{CM}).

The average (low-frequency) components of the voltages, e.g., $v_{\mathrm{r1,M,avg}}$ or $v_{\mathrm{DM,1,avg}}$, can be calculated by averaging over one switching cycle

$$v_{\mathrm{r1,M,avg}} = \frac{1}{T_{\mathrm{s}}} \int_0^{T_{\mathrm{s}}} v_{\mathrm{r1,M}}(t)dt \ . \tag{3.11}$$

The voltage $v_{\mathrm{r1,M}}$ is generated by chopping either the output voltage v_{op} (positive input current direction) or v_{on} (negative input current direction) and its low-frequency component is equivalent to the modulation function, i.e. a sinusoidal and an added third harmonic signal. Details on the modulation function and the third harmonic signal will be given later. The characteristic three voltage levels (V_{op}, V_{on} and 0) are clearly visible in the voltage shape of $v_{\mathrm{r1,M}}$.

The DM voltage

$$v_{\mathrm{DM,1}} = v_{\mathrm{DM,1,avg}} + v_{\mathrm{DM,1}\sim} \tag{3.12}$$

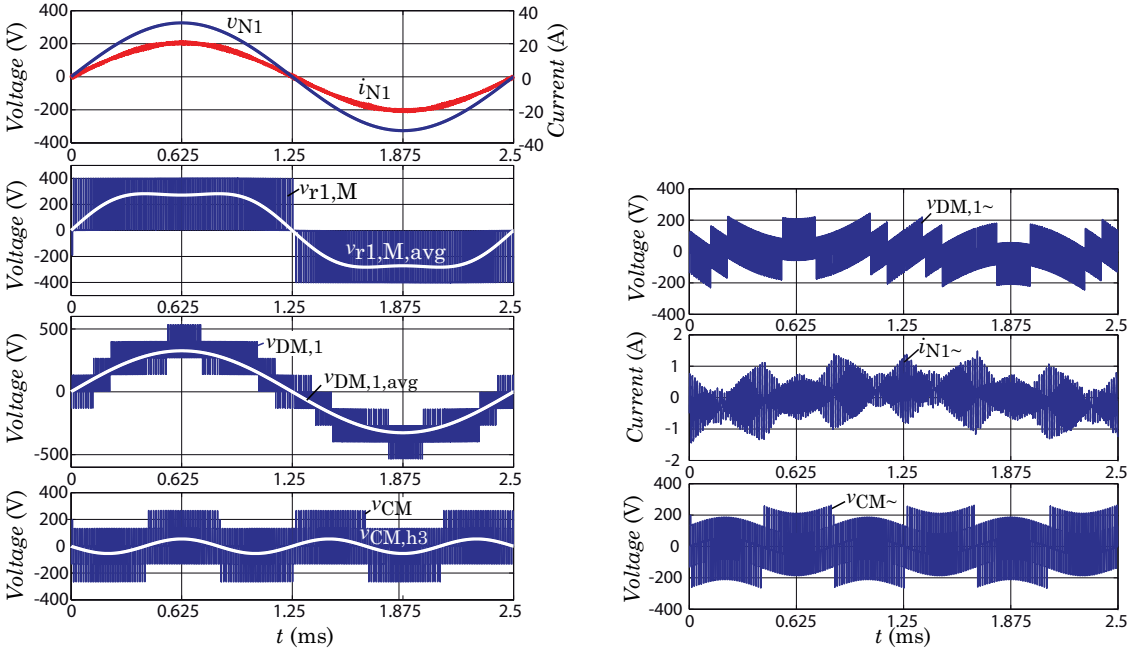


Fig. 3.4: (a) Splitting of the rectifier input voltage $v_{r1,M}$ (v_{r1} to M) in a DM component $v_{DM,1}$ and a CM component v_{CM}; (b) high-frequency component of the DM voltage $v_{DM,1\sim}$, of the CM voltage $v_{CM\sim}$ and high-frequency input current ripple $i_{N1\sim}$.

can further be split into a low-frequency component $v_{\mathrm{DM,1,avg}}$ and in a high-frequency noise component $v_{\mathrm{DM,1}\sim}$.
Only this DM voltage $v_{\mathrm{DM,1}}$ is available for input current formation and its low-frequency component shows purely sinusoidal shape.

Also the CM voltage can be split into a low-frequency component $v_{\mathrm{CM,h3}}$, representing the added third harmonic signal, and a high-frequency component $v_{\mathrm{CM}\sim}$. The output voltage midpoint M therefore shows a low-frequency variation with $3f_{\mathrm{N}}$ and a considerably large high-frequency component. The voltages $v_{\mathrm{DM,1}}$ and v_{CM} are relevant for EMI filtering and will be used in section 5.7 for EMI filter design.

The high-frequency DM and CM voltages are responsible for the high-frequency ripple $i_{\mathrm{N1}\sim}$ of the input current and the voltages are given in **Fig. 3.4(b)** together with the high-frequency current ripple. The CM voltage only contributes to the current ripple for capacitive connection of M to the input (see also section 5.7).

3.1.1 Modulator

A space vector modulation can be applied to implement the optimal switching sequence, but requires a high computational effort and is therefore no option for systems with very high switching frequencies as intended in this work. As shown in [100], a pulse width modulation using a proper carrier signal intrinsically implements the optimal switching sequence. This allows to use phase-oriented average mode current control which reduces the processing demand considerably. The use of simple average mode single-phase PWM controllers would be possible but due to the coupling of the three input currents non-synchronized PWM patterns would result in non-optimal switching sequences and increased input current distortion.

Under consideration of the balance of the mains phase voltages and the rectifier input voltages within each switching period the modulator has to implement the modulation function

$$m_i(t) = M\left(\cos\left(\varphi_{\mathrm{N}} - \frac{2\pi}{3}(i-1)\right)\right)\mathrm{sign}(i_{\mathrm{N}}) \quad i \in [1,2,3] \qquad (3.13)$$

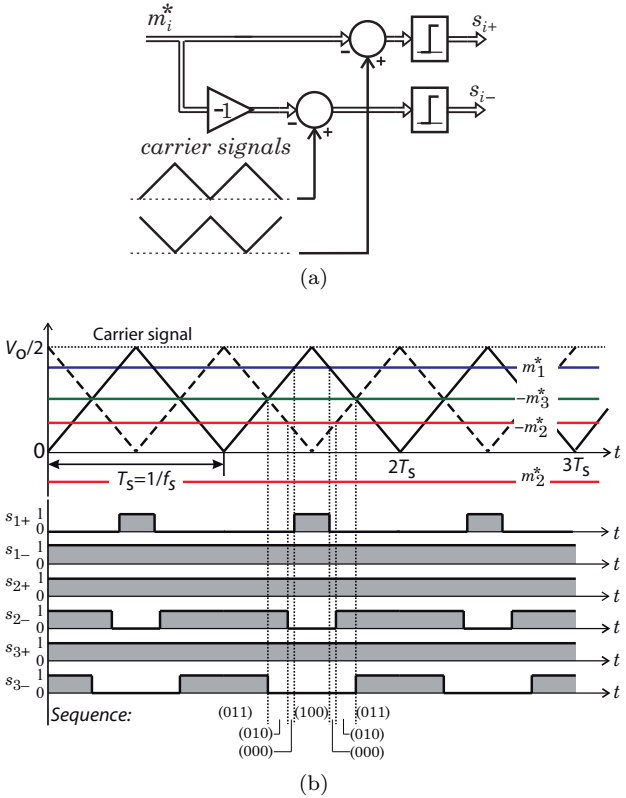


Fig. 3.5: (a) Architecture of the pulse-width modulator for the VR system and (b) pulse-width modulation at $\varphi_N = 10\,°$ using two 180 °-phase shifted triangular carrier signals. The optimal switching sequence (011)-(010)-(000)-(100)-(000)-(010)-(011) can be observed.

where the corresponding duty cycle is

$$\delta_i(t) = 1 - m_i(t) \ . \tag{3.14}$$

The proposed three-phase modulator using two unipolar, 180 °-phase shifted triangular carrier signals is shown in **Fig. 3.5(a)**. Dependent on the input current direction either the switch S_{i+} or S_{i-} has to be operated. According to **Fig. 3.5(a)** the modulation signal generated by the current controller is directly used for pulse-width modulation of S_{i+} and the inverted modulation signal is used for switch S_{i-}.

The modulator output of each phase is high if the triangular carrier signal exceeds the modulator input signal m_i^* (cf. **Fig. 3.5(b)**). As the carrier signal for the PWM of the switches S_{i+} and S_{i-} is 180 ° out of phase inverse pulse-patterns are generated inherently. Symmetrical pulse patterns are generated by the triangular shaped carrier signals and as will be discussed in detail in section 5.6, the peaks of the carrier signals can be used advantageously to derive the sampling instants for the AD-converter.
Unlike the unipolar carrier signal the modulation signals m_i^* are bipolar and hence a duty cycle of 100 % is automatically generated for negative modulation voltages. This means that e.g., the switch S_{1+} is permanently on during $m_1^* < 0$ which does not matter as the input diode D_{N+} blocks. Using this modulation strategy the gate-drive losses of the corresponding switch can be reduced during the inactive half-wave. In addition the direction of the input currents $\mathrm{sign}(i_{\mathrm{N}i})$ must not be considered in the modulation function as negative duty cycles automatically are handled by the opposing switch (i.e. S_{i-} for $i_{\mathrm{N}i} < 0$). **Fig. 3.5(b)** shows the operation of the PWM for $\varphi_{\mathrm{N}} = 10\,^\circ$ ($i_{\mathrm{N}1} > 0$, $i_{\mathrm{N}2} < 0$, $i_{\mathrm{N}3} < 0$) and the optimal switching sequence (011)-(010)-(000)-(100)-(000)-(010)-(011) can be observed (see also **Fig. 3.2**).

3.1.2 Third Harmonic Injection

In the previous section it was discussed that the voltage space vector of the rectifier system $\underline{v}_{\mathrm{r}}$ is decisive for the generation of the input current in combination with the mains voltage. It is well known that a common mode signal added to all three phases has no influence on the fundamental component of the differential mode input current (only the ripple component is influenced). The three-level VR topology offers an output voltage midpoint M which is not connected to the neutral N of the mains. During normal operation, as will be discussed in section 5.7, the output voltage midpoint M itself shows a considerable high-frequency CM voltage (see also [101]).
A low-frequency CM signal can therefore be added to the modulation signal without changing the DM voltage required for input current generation. This circumstance can be used to optimize a specific behavior of the rectifier system [96]. In the following the two major optimization goals will be discussed briefly:

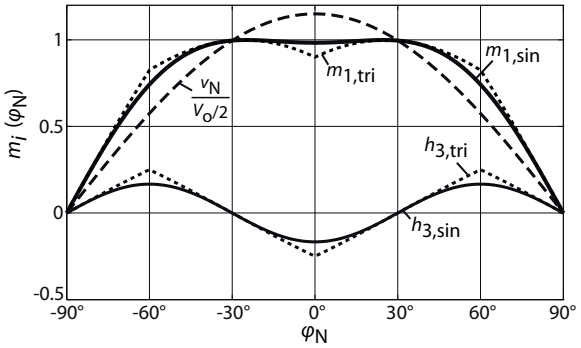


Fig. 3.6: Modulation signal waveforms of phase v_{N1} if the rectifier system is operated at the modulation limit ($M = 2/\sqrt{3}$) if either an ideal sinusoidal third harmonic injection signal $h_{3,\sin}$ or a triangular shaped injection signal $h_{3,\mathrm{tri}}$ is added to the basic sinusoidal modulation function.

A) Increased modulation range M;
B) Minimized current stress of the output capacitor C_o.

Both optimization goals are related to the output behavior (DC side) of the rectifier system. The degree of freedom can alternatively be used to optimize the input behavior (AC side) of the rectifier system, e.g. to minimize the input ripple current and details can be found in [102].

A) Increasing the Modulation Range M

A detailed analysis of the modulation signal given in (3.13) shows that the modulation index is limited to $M = 1$. According to **Fig. 3.2**, however, a maximal modulation index of $M = 2/\sqrt{3}$ can be determined which could be achieved if SVM is applied. The reason for the reduced modulation range can be found in a missing low-frequency CM signal in (3.13).

The modulation range of the phase-oriented control of the input currents in combination with the discussed pulse-width modulator can be extended to $M = 2/\sqrt{3}$ if a proper third harmonic CM signal

$$m_{i,\sin}(\varphi_\mathrm{N}) = M \left| \left(\cos\left(\varphi_\mathrm{N} - \frac{2\pi}{3}(i-1) \right) - \frac{1}{6}\cos\left(3\varphi_\mathrm{N}\right) \right) \right| \qquad (3.15)$$

is added to the modulation function. Note, that a factor 1/6 has to be used for the third harmonic injection thereto.

Fig. 3.6 shows the resulting modulation function $m_{1,\sin}(\varphi_\mathrm{N})$ at the modulation limit ($M = 2/\sqrt{3}$) if the sinusoidal third harmonic signal $h_{3,\sin}(\varphi_\mathrm{N})$ is added. Whereas for $-90\,^\circ < \varphi_\mathrm{N} < -30\,^\circ$ and $30\,^\circ < \varphi_\mathrm{N} < 90\,^\circ$ the modulation signal is increased, it is reduced below 1 for $-30\,^\circ < \varphi_\mathrm{N} < 30\,^\circ$ and pulse-width modulation is therefore possible. As the third harmonic signal is equal in all three phases the same reduction is given for the other two phases. The addition of a third harmonic CM signal in fact moves the output voltage midpoint M in such a way that the peak rectifier input voltage $\hat{V}_\mathrm{N}$ stays below $V_\mathrm{o}/2$ but due to the potential shift can balance a mains voltage amplitude up to $2/\sqrt{3}V_\mathrm{o}/2$. Besides the high-frequency CM voltage generated by the PWM also a low-frequency CM voltage ($3f_\mathrm{N}$) is now present.

Instead of using a purely sinusoidal third harmonic injection, which is in practice not easy to generate, especially in aerospace applications where a variable mains frequency exists, a triangular shaped third harmonic signal $\mathrm{tri}(\varphi_\mathrm{N})$

$$\mathrm{tri}(\varphi_\mathrm{N}) = \begin{cases} -1 + \frac{2}{\pi}\varphi_\mathrm{N} & \text{for } \; 0 < \varphi_\mathrm{N} \leq \pi \\ 3 - \frac{2}{\pi}\varphi_\mathrm{N} & \text{for } \; \pi < \varphi_\mathrm{N} \leq 2\pi \end{cases} \tag{3.16}$$

(see also **Fig. 3.6**) can be used as published in [103]. The modulation signal

$$m_{i,\mathrm{tri}}(\varphi_\mathrm{N}) = M \left| \left(\cos\left(\varphi_\mathrm{N} - \frac{2\pi}{3}(i-1) \right) + \frac{1}{4}\mathrm{tri}\,(3\varphi_\mathrm{N}) \right) \right| \tag{3.17}$$

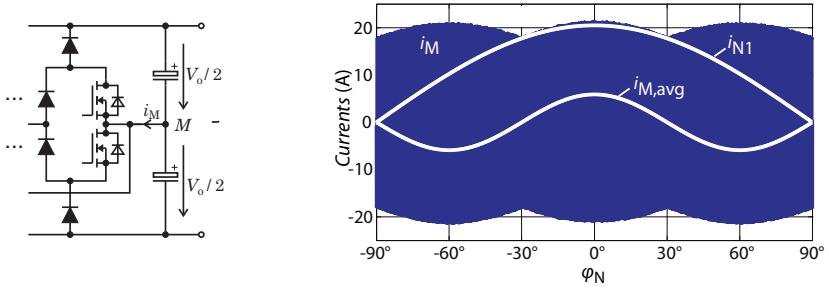
for such a triangular CM function is plotted in **Fig. 3.6** as well.
The corresponding triangular modulation signal can easily be approximated using the phase-to-neutral voltages of the mains

$$h_{3,\mathrm{tri}}(\varphi_\mathrm{N}) \approx \max\{v_{\mathrm{N}1}, v_{\mathrm{N}2}, v_{\mathrm{N}3}\} + \min\{v_{\mathrm{N}1}, v_{\mathrm{N}2}, v_{\mathrm{N}3}\} \tag{3.18}$$

as $v_{\mathrm{N}i} \approx v_{\mathrm{v},i}$ is valid in the stationary case for low boost inductance values or high switching frequencies or both.

B) Minimizing the Midpoint Current

Fig. 3.7(b) shows the simulated current i_M flowing from the connection of the (bidirectional) switches into the midpoint M of the output capacitors (cf. **Fig. 3.7(a)**) for $P_\mathrm{o} = 10\,\mathrm{kW}$, $f_\mathrm{N} = 400\,\mathrm{Hz}$ and



(a) (b)

Fig. 3.7: (a) Schematic of one phase-leg of the VR system illustrating the midpoint current i_M and (b) simulated midpoint current i_M for $P_o = 10\,\text{kW}$, $f_N = 400\,\text{Hz}$, $V_N = 230V$ and $f_s = 250\,\text{kHz}$.

$V_N = 230V$ if the modulation function according to (3.13) is used. The current shows pulsed shape and averaging over one switching period results in the current $i_{M,avg}$. This approximately sinusoidal current shows the amplitude $\hat{I}_N M/2$ and a frequency of $3f_N$. Next to the high-frequency current therefore also a low-frequency, third harmonic current is present which has to be considered for the design of the output capacitors. This current also results in (locally) unbalanced output voltages with $3f_N$ but its average over one mains period is zero. It has to be stated here that i_M shows next to the third harmonic component also components with $k3f_N$ where $k = 1, 3, 5\ldots$ which are very small and can therefore be neglected.

Also here a proper CM signal can be used to minimize this unwanted third harmonic midpoint current and will be derived in the following. The local average of the midpoint current

$$i_{M,avg}(\varphi_N) = \delta_1(\varphi_N) i_{N1}(\varphi_N) + \delta_2(\varphi_N) i_{N2}(\varphi_N) + \delta_3(\varphi_N) i_{N3}(\varphi_N) \quad (3.19)$$

can be calculated using the input currents $i_{Ni}(\varphi_N)$ and the corresponding duty cycles $\delta_i(\varphi_N) = 1 - m_i(\varphi_N)$

$$\delta_i(\varphi_N) = 1 - M\left|\cos\left(\varphi_N - \frac{2\pi}{3}(i-1)\right) - M_3\cos\left(3\varphi_N\right)\right| . \quad (3.20)$$

In the following the the factor M_3 for minimum rms-value of the low

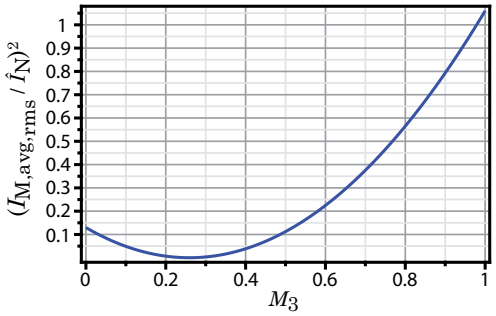


Fig. 3.8: Value of the local average, i.e. low frequency component of the midpoint rms current as a function of the amplitude M_3 of the third harmonic modulation signal. A minimum rms value results for $M_3 \approx 1/4$.

frequency component of the midpoint current i_{M} will be determined. As the midpoint current shows a frequency of $3f_{\mathrm{N}}$ only a $60\,^\circ$ interval has to be considered. The interval $\varphi_{\mathrm{N}} \in [-30\,^\circ \ldots 30\,^\circ]$ is used here for the calculation of $i_{\mathrm{M,avg}}$ which allows to replace the the abs-function by the corresponding signs of the input currents.

$$
\begin{aligned}
I^2_{\mathrm{M,avg_{rms}}} &= \frac{1}{\frac{\pi}{3}} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} i^2_{\mathrm{M}}(\varphi_{\mathrm{N}}) d\varphi_{\mathrm{N}} = \\
&= \frac{3}{\pi} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} \Big(\delta_1 i_{\mathrm{N1}} + \delta_2 i_{\mathrm{N2}} + \delta_3 i_{\mathrm{N3}}\Big)^2 d\varphi_{\mathrm{N}} = \\
&= \frac{3}{\pi} \hat{I}^2_{\mathrm{N}} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} \Bigg(\Big(1 - M\Big(\cos\big(\varphi_{\mathrm{N}}\big) - M_3 \cos\big(3\varphi_{\mathrm{N}}\big)\Big)\Big) \cos\big(\varphi_{\mathrm{N}}\big) + \\
&\quad + \Big(1 - (-1) M\Big(\cos\Big(\varphi_{\mathrm{N}} - \frac{2\pi}{3}\Big) - M_3 \cos\Big(3\varphi_{\mathrm{N}}\Big)\Big)\Big) \cos\Big(\varphi_{\mathrm{N}} - \frac{2\pi}{3}\Big) + \\
&\quad + \Big(1 - (-1) M\Big(\cos\Big(\varphi_{\mathrm{N}} + \frac{2\pi}{3}\Big) - M_3 \cos\Big(3\varphi_{\mathrm{N}}\Big)\Big)\Big) \\
&\qquad \cos\Big(\varphi_{\mathrm{N}} + \frac{2\pi}{3}\Big)\Bigg)^2 d\varphi_{\mathrm{N}} = \\
&= I^2_{\mathrm{N}} M^2 \left(\frac{\big(16\,\pi + 27\,\sqrt{3}\big)}{16\pi} M_3^2 - M_3 + \frac{12\pi - 18\sqrt{3}}{16\pi} \right) .
\end{aligned}
\tag{3.21}
$$

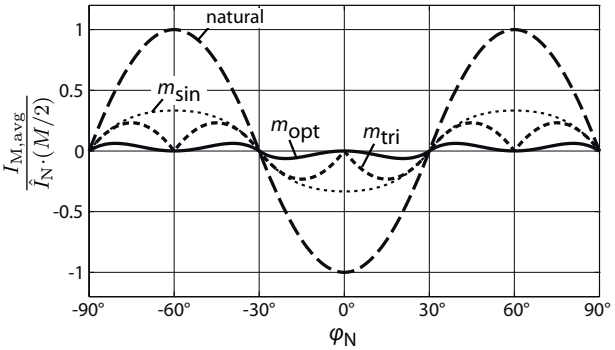


Fig. 3.9: Low frequency component of the midpoint current for the modulation function given in (3.13) (natural) compared to to a modulation including different third harmonic injection signals where for $m_{\sin}(\varphi_{\text{N}})$ the modulation function given in (3.15), for $m_{\text{tri}}(\varphi_{\text{N}})$ the modulation function (3.17) and for $m_{\text{opt}}(\varphi_{\text{N}})$ the optimized modulation function given in (3.20) is applied.

The minimum rms current as a function of M_3 can be found by

$$\begin{aligned} \frac{di^2_{\text{M,avg}_{\text{rms}}}}{dM_3} &= 0 \\ \frac{16\pi + 27\sqrt{3}}{8\pi} M_3 - 1 &= 0 \end{aligned} \tag{3.22}$$

which results in an optimal amplitude of the third harmonic modulation signal of

$$M_3 = \frac{8\pi}{16\pi + 27\sqrt{3}} \approx \frac{1}{4} \ . \tag{3.23}$$

Fig. 3.8 shows the resulting low frequency midpoint rms current value as a function of M_3 where the derived minimum of $M_3 \approx \frac{1}{4}$ can be verified. Similar results were found in [96] where SVM is used to derive the optimal third harmonic function.

In **Fig. 3.9** the resulting waveforms of the midpoint current local average values of several modulation functions are plotted with respect to the midpoint current without any added third harmonic modulation signal. The optimum modulation function using (3.20) with $M_3 = 1/4$ results in the current $i_{\text{M,avg,opt}}$ which is a reduction of the peak value by 95 %.

A reduced midpoint current $i_{\mathrm{M,avg,sin}}$ can be observed as well if the modulation function given in (3.15) is applied which is optimized to maximize the modulation index M of the rectifier system. In **Fig. 3.9** also the resulting local average midpoint current for a triangular shaped third harmonic signal is given ($i_{\mathrm{M,avg,tri}}$). The triangular shaped third harmonic signal results in a considerably reduced neutral point current with respect to $i_{\mathrm{M,avg,sin}}$. As this injection signal also maximizes the input voltage range and considerably reduces the local average of the midpoint current which finally reduces the capacitive requirement of the output capacitors, this third harmonic signal is recommended.
It has to be noted, that the derived results are only valid for symmetrical load of the two output voltages.

3.1.3 Guidelines for Power Circuit Design

The on-state losses are essential for the design of the rectifier system. Simple analytical approximations have been derived in [104] for the VR topology and in [105] for the six-switch VR. The results are summarized in **TABLE 3.1** where the following assumptions have been made for the calculations:

- purely sinusoidal phase current shape;
- input current in phase with mains voltage;
- no low-frequency voltage drop across the boost inductor for the sinusoidal shaping of the input currents;
- constant switching frequency;
- linear behavior of the boost inductors (inductance is not dependent on the current level).

The detailed calculation of the semiconductor power losses will be given in section 5.3. The rms current stress on the output capacitors $I_{\mathrm{C_o,rms}}$ is the total rms current including the high-frequency pulse current and the low-frequency third-harmonic current according to **Fig. 3.9**. Please note that the total current rms-value of the output capacitor C_{o} is independent of the modulation function.

TABLE 3.1: Analytically calculated current stresses of the main components of the original VR and the 6-switch VR topology.

Device	**Six-Switch VR** (cf. **Fig. 3.1(b)**)	**Vienna Rectifier** (cf. **Fig. 3.1(a)**)
S_{i+}, S_{i-}	$I_{\mathrm{S,avg}} = \left(\frac{1}{\pi} - \frac{M}{4}\right)\hat{I}_{\mathrm{N}}$ $I_{\mathrm{S,rms}} = \sqrt{\frac{1}{4} - \frac{2M}{3\pi}}\,\hat{I}_{\mathrm{N}}$	$I_{\mathrm{S,avg}} = \left(\frac{2}{\pi} - \frac{M}{2}\right)\hat{I}_{\mathrm{N}}$ $I_{\mathrm{S,rms}} = \sqrt{\frac{1}{2} - \frac{4M}{3\pi}}\,\hat{I}_{\mathrm{N}}$
$D_{\mathrm{F}i+}$, $D_{\mathrm{F}i-}$	$I_{\mathrm{D_F,avg}} = \frac{M}{4}\hat{I}_{\mathrm{N}}$ $I_{\mathrm{D_F,rms}} = \sqrt{\frac{2M}{3\pi}}\,\hat{I}_{\mathrm{N}}$	
$D_{\mathrm{N}i+}$, $D_{\mathrm{N}i-}$	$I_{\mathrm{D_N,avg}} = \frac{1}{\pi}\hat{I}_{\mathrm{N}}$ $I_{\mathrm{D_N,rms}} = \frac{1}{2}\hat{I}_{\mathrm{N}}$	
$D_{\mathrm{M}i+}$, $D_{\mathrm{M}i-}$	— —	$I_{\mathrm{D_M,avg}} = \left(\frac{1}{\pi} - \frac{M}{4}\right)\hat{I}_{\mathrm{N}}$ $I_{\mathrm{D_M,rms}} = \sqrt{\left(\frac{1}{4} - \frac{2M}{3\pi}\right)}\hat{I}_{\mathrm{N}}$
C_{o}	$I_{\mathrm{C_o,rms}} = \sqrt{\frac{5\sqrt{3}M}{4\pi} - \frac{9M^2}{16}}\,\hat{I}_{\mathrm{N}}$	

Inductor Current Ripple

The boost inductor current ripple of the VR system, which is heavily affected by the control and modulation strategy, is already discussed in [96, 106]. There, the total rms value of the boost inductor current ripple is derived using space vector control and is useful to calculate the inductor power losses caused by the current ripple. A clear statement on the required boost inductor value in order not to exceed a specified peak-to-peak current ripple value, as often used for the design of the boost inductors, is however missing and will be derived in the following.

Fig. 3.10 shows the simulated current waveform and boost inductor current ripple for a VR system operating at $P_{\mathrm{o}} = 10\,\mathrm{kW}$, $f_{\mathrm{s}} = 250\,\mathrm{kHz}$, $L_{\mathrm{N}} = 100\,\mu\mathrm{H}$ and a modulation index of $M = 0.813$ using a triangular shaped third harmonic injection signal with $M_3 = 1/4$ ($V_{\mathrm{N}} = 230\,\mathrm{V}$, $V_{\mathrm{o}} = 800\,\mathrm{V}$). It can be verified that the maximum amplitude of the

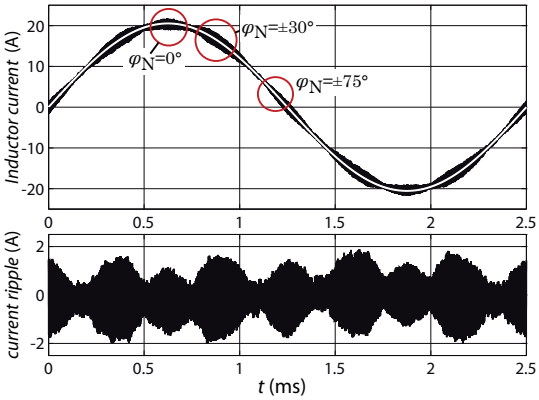


Fig. 3.10: Simulated current waveform i_{N1} and current ripple of the boost inductor L_{N1} for $P_o = 10\,\text{kW}$, $f_s = 250\,\text{kHz}$, $L_N = 100\,\mu\text{H}$ and a modulation index of $M = 0.813$ ($V_N = 230\,\text{V}$, $Vo = 800\,\text{V}$).

ripple current occurs at $\varphi_N = \pm 30\,^\circ$ and $\varphi_N = 270\,^\circ \pm 30\,^\circ$.[1] Unfortunately, the phase angle where the maximum ripple current occurs is heavily dependent on the modulation index M and as a detailed analysis shows the maximum peak-to-peak ripple current occurs either at $\varphi_N = 0\,^\circ$, at $\varphi_N = \pm 30\,^\circ$ or at $\varphi_N = 75\,^\circ$. This can also easily be verified by simulation of the rectifier system. A sinusoidal shaped third harmonic injection with the amplitude M_3 (cf. section 3.1.2) is assumed for the following calculations.

Ripple current at $\varphi_N = 0\,^\circ$

The inductor voltages can be calculated using the difference voltages of the particular voltage space vectors to the phase voltage space vector $\underline{v}_N$ (cf. **Fig. 3.12**). The projections of these voltages on the corresponding phase results in the desired inductor voltages. The ripple itself is a function of the switching sequence, of the voltage space vectors turn-on times and of the particular inductor voltages. **Fig. 3.11** shows the corresponding switching sequence at $\varphi_N = 0\,^\circ$ for $M = 1$ (cf. section 3.1.1). It is obvious that only the switching states (000), (011) and (100) are used as the switching state (010) would yield to a phase shift. According to **Fig. 3.12** switching states (011) and (100) increase and the switching state (000) decreases the inductor current i_{N1}. The corresponding peak-

[1] Consider that cos-waveforms are assumed.

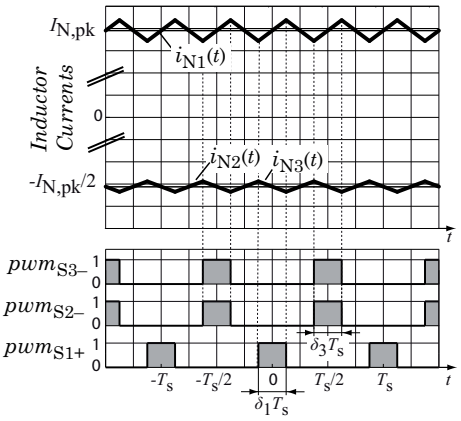


Fig. 3.11: Schematic inductor currents i_{Ni} and corresponding pwm-signals for $\varphi_N = 0\,°$; $M = 1$, $M_3 = 1/4$.

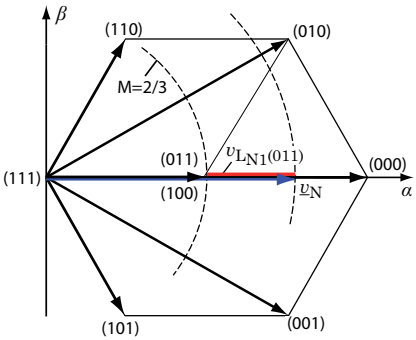


Fig. 3.12: Space vector diagram for determining the peak-to-peak current ripple at $\varphi_N = 0\,°$.

to-peak current ripple at $\varphi_N = 0\,°$ can be calculated using the switching state (011) and which is dependent of the duty cycle of switch S_{3-}.

According to (3.20) the duty cycle $\delta_3(\varphi_N)$ is given by

$$\begin{aligned}\delta_3(\varphi_N = 0) &= 1 - M\left|\cos\left(\varphi_N - \frac{4\pi}{3}\right) - M_3\cos(3\varphi_N)\right| = \\ &= 1 - M\left(\frac{1}{2} + M_3\right)\end{aligned} \tag{3.24}$$

for $0 < M_3$. The corresponding inductor voltage of L_{N1} is the difference of the phase voltage v_{N1} and the voltage space vector (011)

$$\begin{aligned} v_{\mathrm{L_{N1}}}(\varphi_{\mathrm{N}} = 0) &= \hat{V}_{\mathrm{N}} - v_{\mathrm{r,(011)}} = \hat{V}_{\mathrm{N}} - \frac{V_{\mathrm{o}}}{3} = \\ &= \frac{V_{\mathrm{o}}}{2}\left(M - \frac{2}{3}\right) \end{aligned} \tag{3.25}$$

which can easily be derived for the case at hand as the inductor voltages are in/out out phase with v_{N1}. Using the turn-on time $\delta_3(\varphi_{\mathrm{N}} = 0\,^\circ)$ and the derived voltage $v_{\mathrm{L_{N1}}}(\varphi_{\mathrm{N}} = 0\,^\circ)$ the peak-to-peak current ripple at $\varphi_{\mathrm{N}} = 0\,^\circ$ can be calculated to

$$\begin{aligned} \Delta i_{\mathrm{N,pp},0^\circ} &= \frac{v_{\mathrm{L_{N1}}}(0^\circ)\delta_3(0^\circ)}{L_{\mathrm{N1}} f_{\mathrm{s}}} = \\ &= \frac{V_{\mathrm{o}}}{2 f_{\mathrm{s}} L_{\mathrm{N}}}\left(M - \frac{2}{3}\right)\left(1 - M\left(\frac{1}{2} + M_3\right)\right)\ . \end{aligned} \tag{3.26}$$

Similar calculations can be performed at $\varphi_{\mathrm{N}} = \pm 30\,^\circ$

$$\Delta i_{\mathrm{L,pp,max},\pm 30^\circ} = \frac{V_{\mathrm{o}}}{2 f_{\mathrm{s}} L_{\mathrm{N}}}\left(1 - M\frac{\sqrt{3}}{2}\right)\left(M\frac{\sqrt{3}}{2} - \frac{1}{3}\right) \tag{3.27}$$

and $\varphi_{\mathrm{N}} = \pm 75\,^\circ$

$$\begin{aligned} \Delta i_{\mathrm{L,pp,max},\pm 75^\circ} =& \frac{V_{\mathrm{o}}}{2 f_{\mathrm{s}} L_{\mathrm{N}}}\left(\left(\frac{2}{3} - M\cos\left(\frac{5\pi}{12}\right)\right)\right. \\ & \left(M\left(\cos\left(\frac{5\pi}{12}\right) + \sin\left(\frac{5\pi}{12}\right) - 1\right)\right) + \\ & \left. + \left(\frac{1}{3} - M\cos\left(\frac{5\pi}{12}\right)\right)\left(1 - M\left(\cos\left(\frac{5\pi}{12}\right) - \frac{M_3}{\sqrt{2}}\right)\right)\right) \end{aligned} \tag{3.28}$$

which can be approximated by

$$\begin{aligned} \Delta i_{\mathrm{L,pp,max},\pm 75^\circ} \approx& \frac{V_{\mathrm{o}}}{2 f_{\mathrm{s}} L_{\mathrm{N}}}\left(\left(\frac{2}{3} - \frac{M}{4}\right)\left(1.22M - 1\right) + \right. \\ & \left. + \left(\frac{1}{3} - \frac{M}{4}\right)\left(1 - M\left(1 - \frac{M_3}{\sqrt{2}}\right)\right)\right)\ . \end{aligned} \tag{3.29}$$

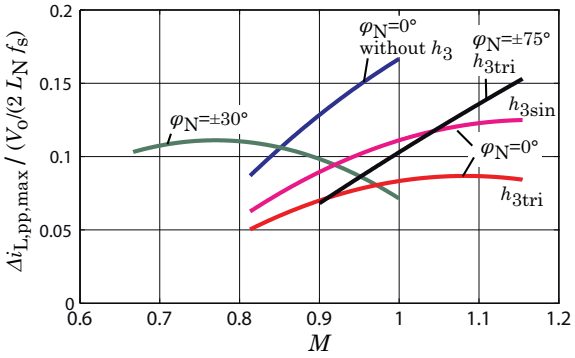


Fig. 3.13: Calculated peak-to-peak inductor current ripples as a function of M and for different third harmonic injection signals (triangular and sinusoidal shaped).

The calculated normalized peak-to-peak current ripples are depicted in **Fig. 3.13** as a function of M for different third harmonic injection signals (triangular or sinusoidal shaped) with amplitudes M_3. The amplitude of the third harmonic signal at $\varphi_N = \pm 30\,^\circ$ is zero and the current ripple at $30\,^\circ$ is therefore independent of M_3. It is obvious that a triangular shaped carrier signal results in smaller current ripples compared to the purely sinusoidal third harmonic injection signal. The maximum peak-to-peak current ripple occurs either at $\varphi_N = \pm 30\,^\circ$ or at $\varphi_N = \pm 75\,^\circ$. The corresponding formula for calculating the inductance value of the boost inductor has to be selected according to the application. A reasonable design criterion for the boost inductor current would be the ripple current at $\varphi_N = \pm 30\,^\circ$ and $M = 0.813$ ($V_N = 230\,\mathrm{V}$, $V_o = 800\,\mathrm{V}$) unless the Vienna Rectifier system is not operated in a nominal point of $M > 1.05$.

3.2 Control of the Rectifier System

To design a controller for the active three-phase rectifier an appropriate model of the rectifier system is required. As the switching ripple (input current ripple) is small in comparison to the low frequency input currents, averaging over one switching period can be applied. The pulsed voltages are thereto replaced by an equivalent value averaged over one switching period. Neglecting the input filter, the rectifier

system exhibits five energy storage elements (three boost inductors and two output capacitors) and a fifth order model is therefore expected. However, as the sum of the input currents is forced to zero, only two inductors represent independent energy storage elements and therefore the model is actual of fourth order.
In [107] a detailed nonlinear time varying model including all five elements for control of the three-phase three-level rectifier system is derived using state space averaging. It is shown that the nonlinearity can be eliminated using a proper input signal transformation and the time-variant behavior is avoided by application of the Park transformation which transfers the state variables into the *dq0*-space. Based on this model a linear controller [108] as well as a quasi linear controller [109] is designed and also large signal modeling and steady state analysis [110] is performed.
The model itself is unfortunately not as general as it promises as for instance cross-couplings of the *d*- and *q*-quantities of the model are neglected. An additional drawback is that the model relies on the Park transformation. This means that some information on the mains frequency and the mains voltage phase angle are required. Such a controller might not operate as intended in case of a single phase loss.

In [111] it shown that the model of the three-phase VR is flat.[2] Based on this model an overview of nonlinear control methods suited for control of the rectifier system including several linearisation techniques and two passivity based approaches is given in [112]. The main conclusion of this work is that the system responses of the nonlinear control methods to load steps are similar to the ones of a linear controller and that the nonlinear methods only show advantages for trajectory planning which is typically not required in the rectifier system as the output voltage is normally kept at a fixed value.

An explicit design of a passivity based controller using parallel damping injection for the three-phase VR system is given in [113]. The

[2] A linear or nonlinear system is called *flat* if a (virtual) output y exists where all system variables can be expressed by this output and time derivatives of the output. In addition y must be differentially independent, i.e. there must not exist a differential relation only in the this output y and its derivatives. The definition of a *flat* system is the extension of controllability from linear systems to nonlinear systems. A *flat* system can be controlled by a combination of a special designed feedforward signal and a linear controller.

controller design is based on the model of [107], requires therefore the Park and inverse Park transformation and does not show notably good results.

In [80], beside the basic operation of the rectifier system also a controller structure has been proposed. In contrast to the approach given in [107] more or less decoupled models for the AC-side of the rectifier system (current control) and DC-side of the rectifier system (output voltage control and output voltage symmetry control) are intended. The decoupling of the output voltage controller from the input current controller is justifiable by the different dynamic behaviors of both sides. The time behavior of the input current control loop is related to the switching frequency f_s where the output voltage control is related to the mains frequency f_N which is considerably lower than f_s. The typically relative large output capacitor C_o is the decoupling element of the two control loops and a cascade control structure can therefore be used.

The basic controller structure used in this approach is shown in **Fig. 3.14** where a phase-oriented modulation strategy is assumed in combination with superimposed output voltage and output voltage symmetry controllers. A three-phase current controller $K_\mathrm{I}(s)$ is required to ensure sinusoidal input currents which are in phase with the mains phase voltages or leading/lagging the mains voltages by a limited amount. In order to achieve a constant output voltage an output voltage controller $K_\mathrm{V}(s)$ must be employed. The output signal of the voltage controller is equivalent to the required output power P_o^*. Using the rms values of the mains voltages a conductance

$$G_\mathrm{e}^* = \frac{P_\mathrm{o}^*}{V_\mathrm{N1}^2 + V_\mathrm{N2}^2 + V_\mathrm{N3}^2} \tag{3.30}$$

can be calculated which is used for generating the reference currents $i_{\mathrm{N}i}^* = v_{\mathrm{N}i}\, G_\mathrm{e}^*$.

As the output capacitor is split into two parts an output voltage symmetry controller $K_\mathrm{S}(s)$ is required for balancing of the corresponding output voltages v_op and v_on.
As will be discussed in section 3.2.3, a common signal i_0 added to the corresponding modulation functions can be used to balance the two

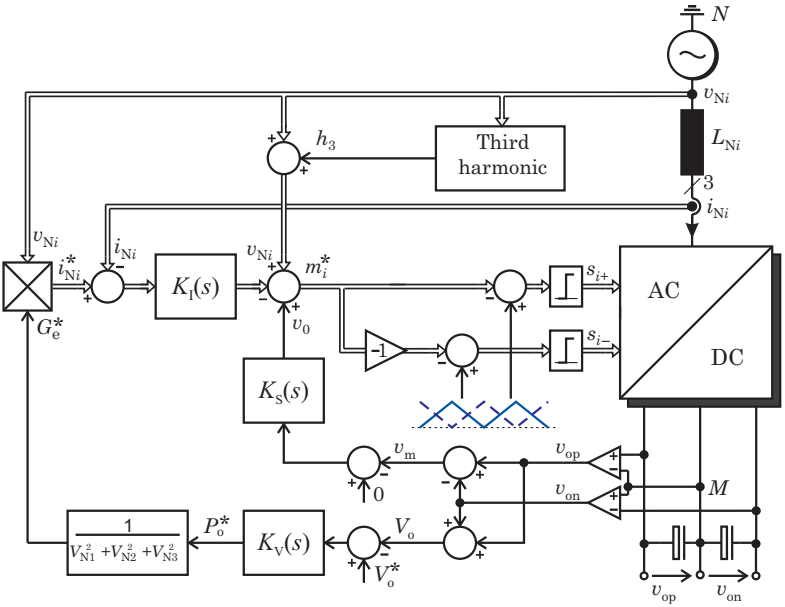


Fig. 3.14: Basic controller structure of the three-phase three-level rectifier system. Signal paths being equal for all phases are shown by double lines.

output voltages. It is well known that a common DC offset does not influence the DM current generation and therefore also this control is not directly coupled with the current control.
The models of the rectifier system and the design of the corresponding controllers are summarized in the following.

3.2.1 Current Controller

Several approaches have been reported in literature for implementation of a proper three-phase current controller. A hysteresis controller, as shown in [80], is an easy way for current control but shows on one hand variable switching frequency and on the other hand an increased current ripple due to the cross-couplings of the three phases. A Decoupled Hysteresis Controller (DHC) [114] has therefore been proposed which results in a more regular switching of the power transistors and the possibility to control the output voltage balance and characteristic of the

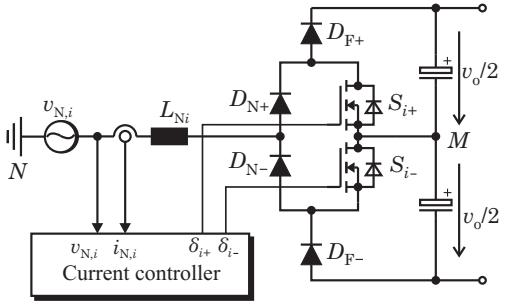


Fig. 3.15: One phase leg of the three-level six-switch Vienna-type rectifier.

center point current [115].

Alternatively, three commercially available analog single-phase PFC control chips (e.g. UC3854), could be applied for current control. This would be an easy and cheap approach but these chips typically use a sawtooth-shaped carrier signal and usually cannot be synchronized in an easy manner. A sawtooth-shaped carrier signal results in non-optimal switching sequences and the three phases are not correlated due to the missing synchronization. Altogether, this leads to higher current ripple in the boost inductances and to significantly higher input current distortion [100].

Average mode current control using a triangular shaped carrier signal for PWM has emerged to be a good approach. The multiplier required to generate the reference currents i^*_{Ni} is not very suited for an analog implementation and therefore a multiplier-free implementation has been developed [116]. In a digital implementation of the current controller, as intended in this work, the implementation of a multiplier is easy and a control architecture as shown in **Fig. 3.14** is used.

Controller Design

In the following a very simple linear model for current controller design is derived which describes the main behavior of the rectifier system. As already mentioned average mode control is used which means that all signals are averaged over one switching period. A phase leg of the rectifier topology is shown in **Fig. 3.15**.

Using the duty cycle $\delta_i(t)$, one can write

$$v_{\mathrm{N}i}(t) - L_{\mathrm{N}i}\frac{di_{\mathrm{N}i}(t)}{dt} = \frac{v_{\mathrm{o}}(t)}{2}\Big(1 - \delta_i(t)\Big) \tag{3.31}$$

if ideal balanced output voltages are assumed and the CM voltage v_{MN} is neglected, i.e. a decoupled operation of the phases is assumed in a first step. The design of a current controller considering the coupling of the three-phases is discussed in section 6.3.1. This equation is nonlinear as the output voltage is multiplied by the duty cycle and time varying as the sinusoidal mains voltage $v_{\mathrm{N}i}$ is included. The output voltage $v_{\mathrm{o}}(t)$ is controlled to a constant value by the output voltage controller and as the dynamic of the voltage control loop is much slower than the dynamic of the current control loop a constant output voltage $v_{\mathrm{o}}(t) = V_{\mathrm{o}}$ can be assumed. This eliminates the nonlinearity in (3.31).
Instead of using the Park transformation to eliminate the time variance of (3.31) a proper feedforward signal is applied in this work. Using the feedforward function

$$\delta_{\mathrm{res},i}(t) = \delta_{\mathrm{ff},i}(t) + \delta_i(t) \quad \delta_{\mathrm{ff},i}(t) = 1 - \frac{v_{\mathrm{N}i}(t)}{V_{\mathrm{o}}/2} \tag{3.32}$$

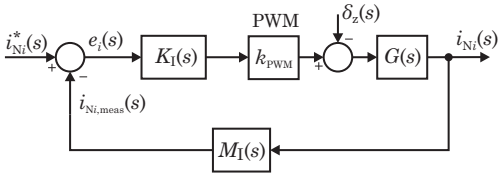
also the time variance is eliminated and the Laplace transform can be applied resulting in the very simple model

$$G(s) = \frac{i_{\mathrm{N}i}(s)}{\delta_i(s)} = \frac{V_{\mathrm{o}}}{2L_{\mathrm{N}}s} \tag{3.33}$$

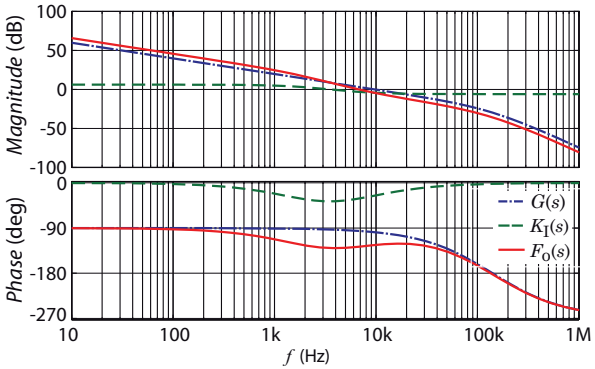
for the rectifier system. Note that an ideal input voltage feedforward signal is assumed which generates the duty cycle according the sinusoidal mains voltages and that the current controller only has to deal with the deviations from the reference current. The influence of an error in the input voltage feedforward signal is discussed below.
In this model some details, such as the impedance of the mains, the characteristics of the EMI-filter or the delay times of the switches are not considered for sake of simplicity.

Previous work on a 400 kHz VR system [117] showed that a simple P + Lag controller

$$K_{\mathrm{I}}(s) = K_{\mathrm{p}}\frac{1 + sT_{\mathrm{D}}}{1 + sT_1} \tag{3.34}$$



(a)



(b)

Fig. 3.16: Design of the analog current controller; (a) simplified control loop and (b) Bode plot of the digital current controller for the VR250 rectifier system (cf. section 7.2). A crossover frequency of 7 kHz and a phase margin of 53 ° can be read.

in conjunction with the voltage feed-forward function of (3.32) is an adequate solution. Using the P + Lag controller, the controller gain is reduced for frequencies above the intended maximum mains frequency (i.e. 800 Hz). This considerably improves input current quality but reduces on the other hand the phase margin of the control loop. A better performance of the current controller is therefore paid by a slightly reduced phase margin.

Fig. 3.16(a) shows the analog current control loop where $G(s)$ is the derived simple model of the VR system, $K_I(s)$ is the P + Lag current controller and $M_I(s)$ is the transfer function of the current measurement considering the bandwidth limitation of the current sensor. The digital control implementation including a detailed discussion on sampling effects and calculation delays is treated in section 5.6.

A Bode plot of the analog control loop of the implemented VR250 rectifier system (cf. section 7.2, system parameters: $V_\mathrm{N} = 230\,\mathrm{V}$, $f_\mathrm{s} = 250\,\mathrm{kHz}$, $P_\mathrm{o} = 10\,\mathrm{kW}$, $V_\mathrm{o} = 800\,\mathrm{V}$ and $L_\mathrm{N} = 100\,\mu\mathrm{H}$) is depicted in **Fig. 3.16(b)** where $F_\mathrm{o}(s)$ is the open loop transfer function of the control loop. With the controller parameters $K_\mathrm{p} = 2$, $T_\mathrm{D} = 23\,\mu\mathrm{s}$ and $T_1 = 90\,\mu\mathrm{s}$ a crossover frequency of 7 kHz and a phase margin of 53 ° is achieved.

Improved Feedforward Signal

Initial measurements taken from the constructed prototypes showed only moderate results regarding input current quality for mains frequencies of 360 Hz-800 Hz. One reason has been found in the measurement delay of the phase voltages which are used for the input voltage feedforward. This delay, e.g. caused by a filter stage of the measurement should be as small as possible in order to achieve good input current quality. The voltage drop across the boost inductor has been determined as the main reason for the rather large input current distortion. This voltage drop is negligible for a mains frequency of 50 Hz, whereas the limited gain of the current controller is not able to fully compensate the increased voltage drop at higher mains frequencies which causes the increased input current distortion. As shown in [118] and analyzed in more detail in [119] also the boost inductor's voltage drop can be added as an additional feedforward signal

$$\delta_{\mathrm{ff},i}(t) = 1 - \frac{v_{\mathrm{N}i}(t) - L_\mathrm{N}\frac{di^*_{\mathrm{N}i}(t)}{dt}}{V_\mathrm{o}/2} \tag{3.35}$$

which considerably improves the input current quality. The inductor voltage drop can be estimated by

$$L_\mathrm{N}\frac{di^*_\mathrm{N}(t)}{dt} \approx L_\mathrm{N}\frac{\Delta i^*_\mathrm{N}(t)}{\Delta T} = L_\mathrm{N}\frac{i^*_\mathrm{N}[n-1] - i^*_\mathrm{N}[n]}{T_\mathrm{s}} \tag{3.36}$$

in the digital controller where i^*_N is the reference current generated using the measured input voltages. The two components of the feedforward signal are plotted in **Fig. 3.17** where a modulation index of $M = 0.813$ is assumed. A boost inductor value of $100\,\mu\mathrm{H}$ and an output power of $P_\mathrm{o} = 10\,\mathrm{kW}$ ($f_\mathrm{N} = 800\,\mathrm{Hz}$, $V_\mathrm{N} = 230\,\mathrm{V}$) is assumed in this plot which corresponds to the VR250 rectifier system (cf. section 7.2). The

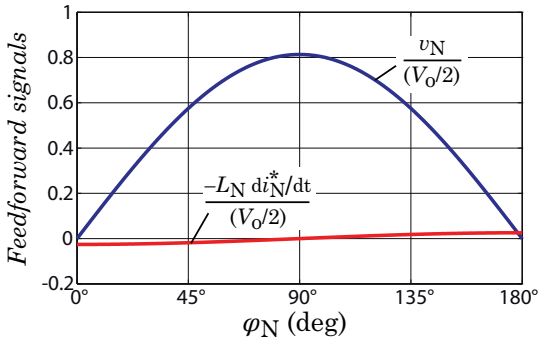


Fig. 3.17: Components of the feedforward signal including the voltage drop over the boost inductor used to improve input current quality.

voltage drop shows a maximum of 2.5 % of the mains voltage at the zero-crossings. Despite this low value, the feedforward signal considerably improves the input current quality as will be further discussed in section 5.1.2 using measurement results.

Influence of EMI filter

The discussed control loop relies on an ideally sinusoidal voltage source connected to the AC-side of the boost inductors L_N. Actually, however, an EMI filter has to be connected to the rectifier input for a practically implemented rectifier system in order to comply with EMI standards. A simplified single-phase schematic of the VR input is given in **Fig. 3.18(a)**.

This filter, together with the impedance of the mains L_M take influence on the input current quality on the mains interface. The work given in [120] includes the total filter impedance the impedance of the mains in the model of the rectifier system which is a good way to get a basic idea of the system behavior. It describes, however, the implemented system not exactly as for instance the mains voltages v_{Ni} used to derive the reference currents are measured on the ac side of the boost inductors and not at the (ideal) voltage sources of the mains (cf. **Fig. 3.18(a)**). The same applies for the current measurement which is performed at the boost inductors and not at the rectifier input.
If the input filter is considered in the dynamic behavior of the rectifier

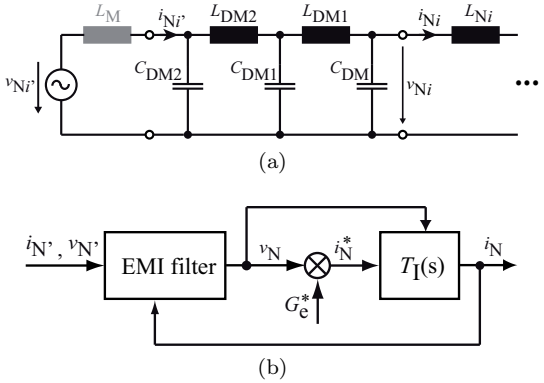


Fig. 3.18: (a) Equivalent single-phase schematic of the VR input if an EMI filter and mains impedance L_M is considered and (b) corresponding block diagram.

system the transfer function

$$G'(s) = \frac{i'_N(s)}{v'_N(s)} \tag{3.37}$$

characterizes the rectifiers input current i'_N as a function of the mains voltage v'_N. The corresponding model is depicted in **Fig. 3.18(b)**. The input of the EMI filter (including the mains impedance L_M) are the mains voltage v'_N and input current i'_N. The rectifier input voltage voltage v_N is dependent on the controlled boost inductor current i_N and the EMI filter characteristic and the reference current i^*_N is calculated by the use of the conductance G^*_e. According to (3.32) the rectifier input voltage is used as feedforward signal for the current controller and an ideal feedforward signal is assumed.

Fig. 3.19 shows the calculated Bode plot of the transfer function $G'(j\omega)$ for different grid impedances L_M for the VR250 rectifier system (cf. section 7.2) operating at an output power of $P_o = 10\,kW$. The conductance G^*_e is $0.063\,A/V$ which is -24 dB. It is obvious that the rectifier input shows ohmic behavior up to about 1 kHz but in contrast to the results of the current controller design slight differences in the phase and magnitude of $G'(j\omega)$ already occur at $f_N = 800\,Hz$. An RC-damping circuit is implemented to damp the filter resonances but for grid impedances below 20 µH still a relatively large magnitude of $G'(j\omega)$

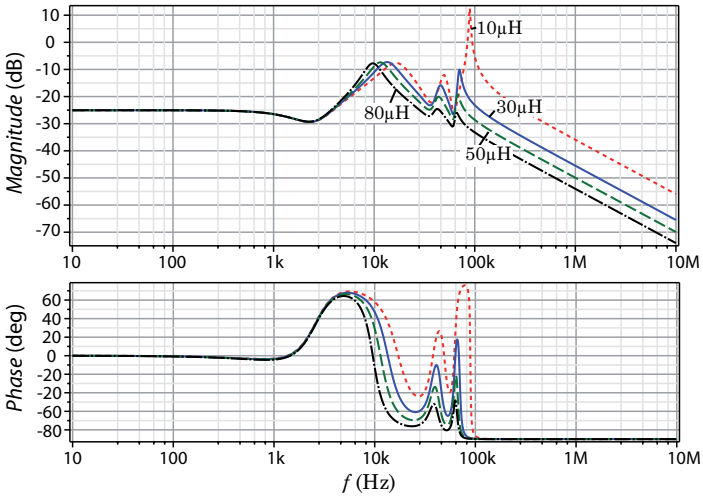


Fig. 3.19: Bode plot of the transfer function $G'(j\omega) = \frac{i'_{\mathrm{N}}(\mathrm{j}\omega)}{v'_{\mathrm{N}}(\mathrm{j}\omega)}$ for different grid impedances L_{M}.

at the resonance frequency appears and an additional damping circuit may be required.
According to **Fig. 3.19** no filter resonance occurs in the frequency range of the grid $f_{\mathrm{N}} = 360\,\mathrm{Hz} \ldots 800\,\mathrm{Hz}$ as well at the switching frequency of $f_{\mathrm{s}} = 250\,\mathrm{kHz}$.

The ohmic behavior of the rectifier circuit could also be used advantageously to damp the filter resonance in case the resonance falls into current controller bandwidth. This may occur for higher power levels but note that in order to achieve the corresponding conductance a considerably increased rectifier power level would be required.

Nonideal Voltage Feedforward

An ideal input voltage feedforward signal has been assumed for derivation of (3.33). In this section the influence of a disturbed feedforward signal $v_{\mathrm{N}i,\mathrm{ff}} = v_{\mathrm{N}i} + \Delta v_{\mathrm{N}i}$, e.g. evoked by an error or delay in the input voltage measurement, is analyzed. If $v_{\mathrm{N,ff}}$ is used in the feedforward signal (3.32) in conjunction with (3.31) the input current can be expressed

by

$$i_{\mathrm{N}i}(s) = \frac{V_{\mathrm{o}}}{2L_{\mathrm{N}}s}\delta_i(s) - \frac{1}{L_{\mathrm{N}}s}\Delta v_{\mathrm{N}i}(s) \tag{3.38}$$

and an additional part occurs besides the dependence on the duty cycle. This part in fact can be expressed by an error term in the duty cycle $\delta_{\mathrm{z}i}(s) = \frac{\Delta v_{\mathrm{N}i}(s)}{V_{\mathrm{o}}/2}$ which finally results in

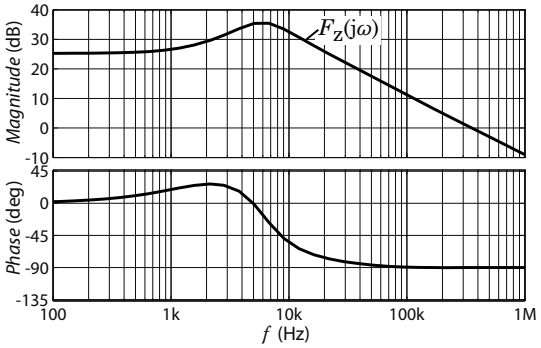
$$i_{\mathrm{N}i}(s) = \frac{V_{\mathrm{o}}}{2L_{\mathrm{N}}s}\Big(\delta_i(s) - \delta_{\mathrm{z}i}(s)\Big) \ . \tag{3.39}$$

An error in the input voltage feedforward signal is therefore equal to an error in the duty cycle and can be treated as disturbance input $\delta_{\mathrm{z}i}(s)$ of the control loop (cf. **Fig. 3.16(b)**). The corresponding disturbance transfer function of the control loop

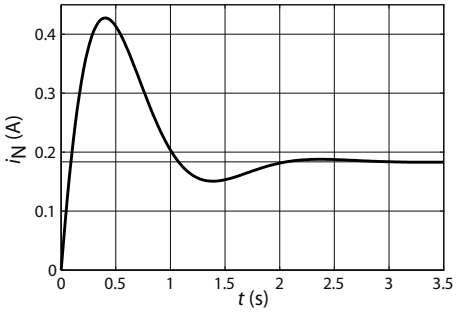
$$F_{\mathrm{z}}(s) = \frac{\delta_{\mathrm{z}}(s)}{i_{\mathrm{N}}(s)} \tag{3.40}$$

of the VR250 rectifier system is plotted in **Fig. 3.20(a)**.

Due to the P + Lag type controller the disturbance can not be compensated and a steady state deviation remains. The DC gain is 25 dB which means that an error in the duty cycle of 1 % yields to a steady state deviation of the input current of 0.178 A. According to **Fig. 3.20(a)** the influence increases for frequencies between 1 kHz and 10 kHz which is a side effect of the PDT1 controller and which is, unfortunately, the frequency range where the resonance of the input filter occurs.
Fig. 3.20(b) shows the response to a step of $\delta_{\mathrm{z}} = 0.01$. After a short oscillation the system settles at a steady state deviation of 0.178 A. A PI-type controller would in general be able to compensate this error but as will be discussed in section 6.3.1 for the Δ-switch rectifier system the integral part of the PI-type control results in problems in the vicinity of the zero crossings of the input currents.
A careful implementation of the input voltage feedforward signal is therefore essential for a good performance of the current controller. This is immediately evident as the input voltage feedforward signal is in fact responsible for the generation of a duty cycle which balances to the sinusoidally shaped input voltage and the current controller only compensates deviations from the ideal feedforward signal.



(a)



(b)

Fig. 3.20: Influence of an error in the voltage feedforward signal (expressed as duty cycle error δ_z); (a) Bode plot of the disturbance transfer function $F_z(j\omega) = \frac{i_N(j\omega)}{\delta_z(j\omega)}$ and (b) system response $F_z(s)$ to a step in the duty cycle of $\delta_z = 0.01$.

3.2.2 Output Voltage Controller

Up to now only the AC-side of the rectifier system has been considered. In order to control the rectifier output voltage v_o an appropriate model of the DC-side has been derived in [120] (cf. **Fig. 3.21**) and the results are summarized here with some extensions.
According to the equivalence of the output power $p_o = i_{D,avg}\ v_{o,avg} \approx i_D\ v_o$ and the input power $p_{in} = 3V_N I_N \cos(\varphi_{vi}) - p_v$, where p_v expresses the rectifier system power losses. Under negligence of the energy stored

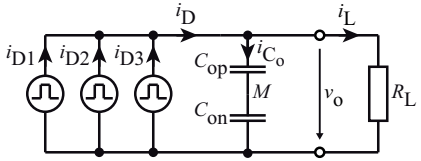


Fig. 3.21: Model of the DC-side of the VR topology for a resistive load R_L. The currents $i_{\mathrm{D}i}$ are the pulse-shaped currents of the free-wheeling diodes $D_{\mathrm{F}i}$.

in the boost inductors and a $\cos(\varphi_\mathrm{vi}) = 1$

$$i_{\mathrm{D,avg}} v_\mathrm{o} = 3\eta V_\mathrm{N} I_\mathrm{N} \tag{3.41}$$

can be set. This nonlinear equation can be linearized around the operating point V_{o_0}, V_{N_0}, I_{D_0} and I_{N_0} using

$$\begin{aligned} v_\mathrm{o} &= V_{\mathrm{o}_0} + \tilde{v}_\mathrm{o} \\ v_\mathrm{N} &= V_{\mathrm{N}_0} + \tilde{v}_\mathrm{N} \\ i_{D,avg} &= I_{\mathrm{D}_0} + \tilde{\bar{i}}_\mathrm{D} \\ i_\mathrm{N} &= I_{\mathrm{N}_0} + \tilde{\bar{i}}_\mathrm{N} \ . \end{aligned} \tag{3.42}$$

This results in

$$\tilde{\bar{i}}_\mathrm{D} = \frac{3\eta V_{\mathrm{N}_0}}{V_{\mathrm{o}_0}} \tilde{\bar{i}}_\mathrm{N} + \frac{3\eta I_{\mathrm{N}_0}}{V_{\mathrm{o}_0}} \tilde{v}_\mathrm{N} - \frac{I_{\mathrm{D}_0}}{V_{\mathrm{o}_0}} \tilde{v}_\mathrm{o} \tag{3.43}$$

where an interrelationship between input currents $\tilde{\bar{i}}_N$ and current $\tilde{\bar{i}}_\mathrm{D}$

$$k_\mathrm{p1} = \frac{\tilde{\bar{i}}_\mathrm{D}}{\tilde{\bar{i}}_\mathrm{N}} = \frac{3\eta V_{\mathrm{N}_0}}{V_{\mathrm{o}_0}} \tag{3.44}$$

is found.
In case of a resistive load the load side can be modeled by

$$H_\mathrm{Load}(s) = \frac{R_\mathrm{L}}{1 + sR_\mathrm{L}C_\mathrm{o}/2} \tag{3.45}$$

if equal output capacitors $C_\mathrm{o}/2 = C_\mathrm{op} = C_\mathrm{on}$ are assumed[3].

[3]In case of constant power load $H_\mathrm{Load}(s)$ would be $\frac{V_\mathrm{o}^2/P_\mathrm{o}}{s(V_\mathrm{o}^2/P_\mathrm{o})C_\mathrm{o}/2-1}$.

As the reference currents $i^*_{\mathrm{N}i}$ are calculated by multiplying the mains voltages $v_{\mathrm{N}i}$ with the conductance G^*_{e} a linear model of the multiplication and the division given in (3.30) has to be derived which can be done by linearizing around an operating point. According to [120] this results in

$$\tilde{i}^*_{\mathrm{N}} = \frac{1}{3V_{\mathrm{N}_0}}\tilde{p}^*_{\mathrm{o}} + \left(\frac{P^*_{\mathrm{o}_0}}{3V^2_{\mathrm{N}_0}} - \frac{2I^*_{\mathrm{N}_0}}{V_{\mathrm{N}_0}}\right)\tilde{v}_{\mathrm{N}} \tag{3.46}$$

if

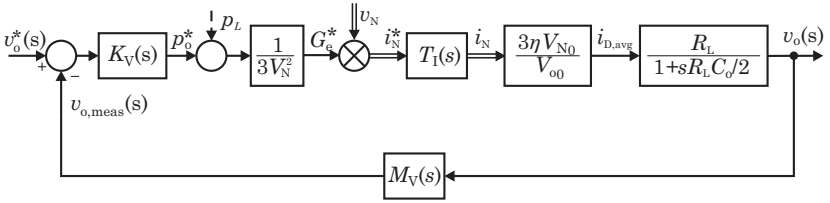
$$\begin{aligned} p^*_{\mathrm{o}} &= P^*_{\mathrm{o}_0} + \tilde{p}^*_{\mathrm{o}} \\ v_{\mathrm{N}} &= V_{\mathrm{N}_0} + \tilde{v}_{\mathrm{N}} \\ i^*_{\mathrm{N}} &= I^*_{\mathrm{N}_0} + \tilde{i}^*_{\mathrm{N}} \end{aligned} \tag{3.47}$$

are used which results in the interrelationship

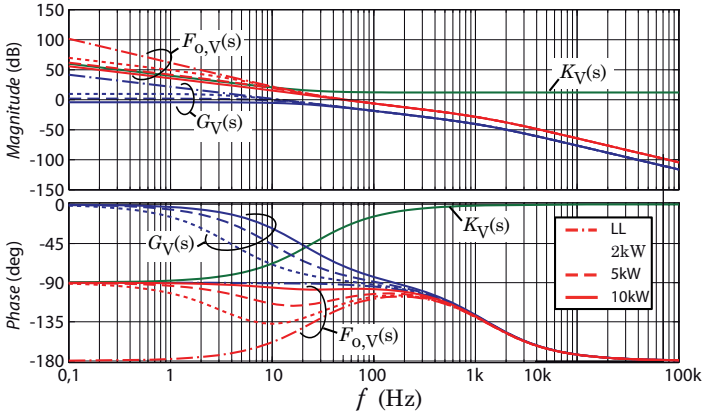
$$k_{\mathrm{p2}} = \frac{\tilde{i}^*_{\mathrm{N}}}{\tilde{p}^*_{\mathrm{o}}} = \frac{1}{3V_{\mathrm{N}_0}} \ . \tag{3.48}$$

Using the small signal models (3.44), (3.48) and (3.45) the control loop given in **Fig. 3.22(a)** can be drawn where $K_{\mathrm{V}}(s)$ is the output voltage controller, $T_{\mathrm{I}}(s)$ is the closed loop transfer function of the current controller and $M_{\mathrm{V}}(s)$ is the transfer function of the measurement circuit.
In order to prevent steady state output voltage control errors a PI-type controller is usually applied. In addition a possible feedforward signal of the load condition p_{L} (e.g. by measuring the load current or by using some informations coming e.g. from a following DC/DC circuit) is shown which can be used to considerably improve the dynamic of the output voltage controller.

In **Fig. 3.22(b)** the Bode plot of a controller design for the VR250 rectifier system (cf. section 7.2) for different load conditions is shown where $G_{\mathrm{V}}(s)$ is the model of the rectifier circuit $K_{\mathrm{V}}(s)$ is the transfer function of the PI-type controller and $F_{\mathrm{o,V}}(s)$ is the open-loop transfer function. The no-load condition (LL) shows the smallest phase margin for the given load cases and is therefore used for stability analysis of the rectifier circuit.
The rectifier should be able to handle a single phase loss and due to the occurring output voltage ripple at $2f_{\mathrm{N}}$ during two-phase operation the



(a)



(b)

Fig. 3.22: (a) Control loop of the output voltage controller and (b) Bode plot of a voltage controller design for the VR250 rectifier system for different load conditions (controller parameters: $k_{p,v} = 4$, $k_{I,v} = 0.0625\,s$).

bandwidth of the output voltage controller must be sufficiently below $2f_N$. The VR250 rectifier system is designed for aerospace applications ($f_N = 360\,Hz \ldots 800\,Hz$) and the achieved cross-over frequency of 60 Hz using the controller parameters $k_{p,v} = 4$, $k_{I,v} = 0.0625\,s$ where

$$K_V(s) = k_{p,v} + \frac{k_{I,v}}{s}\ , \tag{3.49}$$

is therefore suitable.

3.2.3 Output Voltage Symmetry Controller

As discussed in [121] an unbalanced output voltage

$$v_{\mathrm{M}} = \frac{1}{2}\left(v_{\mathrm{op}} - v_{\mathrm{on}}\right) \tag{3.50}$$

which could e.g. result from unequal leakage currents of the output capacitors or from an asymmetrical load of the two rectifier outputs, results in an asymmetrical distribution of the switching actions which finally yields to increased input current distortions.

The average neutral point current $i_{\mathrm{M,avg}}$ can be formed by averaging over a switching period

$$i_{\mathrm{M,avg}} = \delta_1 i_{\mathrm{N1}} + \delta_2 i_{\mathrm{N2}} + \delta_3 i_{\mathrm{N3}} \tag{3.51}$$

and this current causes unbalanced output voltages according to

$$i_{\mathrm{M}} = 2C_{\mathrm{o}}\frac{dv_{\mathrm{M}}}{dt} \tag{3.52}$$

if equal output capacitors $C_{\mathrm{op}} = C_{\mathrm{on}} = C_{\mathrm{o}}$ are assumed.
As already discussed in section 3.1, a third harmonic center point current is generated due to the modulation of the rectifier which also leads to a third harmonic output voltage unbalance. It can be minimized by a proper third harmonic injection signal (cf. 3.1) but is still present.
According to [96] a possible output voltage unbalance v_{M} is stable if average mode current control in conjunction with a pulse-width modulation is applied. This can be verified using **Fig. 3.23(a)** where the corresponding modulation functions m_i are plotted for $\varphi_{\mathrm{N}} = 10\,^\circ$. In the following only the sector $\varphi \in [-30\,^\circ \ldots 30\,^\circ]$ is used and an output voltage unbalance

$$\begin{aligned} V_{\mathrm{op}} &= \frac{V_{\mathrm{o}}}{2} + \Delta V \\ V_{\mathrm{on}} &= \frac{V_{\mathrm{o}}}{2} - \Delta V \end{aligned} \tag{3.53}$$

is assumed. According to (3.31), the increased output voltage V_{op} would result in a decreased input current. Accordingly, the current controller increases the duty-cycle of phase 1 which is performed by a

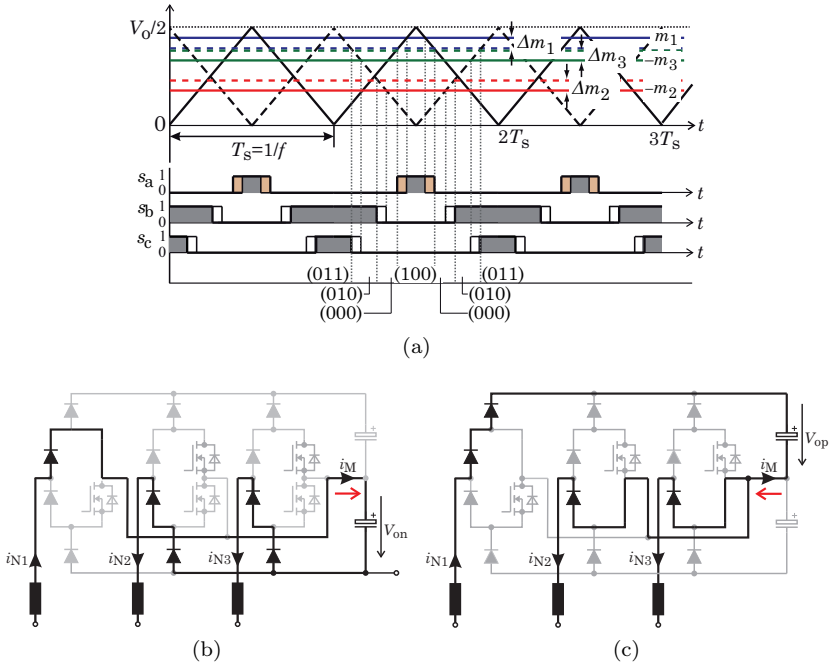


Fig. 3.23: (a) Pulse-width modulation and switching sequence illustrating the self stability of an unbalanced output voltage without an active output voltage balancing if the proposed PWM-based average mode current control is applied ($\varphi_N = 10\,°$). (b) Center point current for the switching state (100) $i_M = i_{N1}$ and (c) for (011) $i_M = -i_{N1}$ ($\varphi_N = 10\,°$).

decrease of the modulation function by Δm_1. On the other hand phases 2 and 3 generate a too low output voltage V_{on} and the corresponding duty-cycles are reduced by increasing the corresponding modulation functions by Δm_2 and Δm_3. The resulting modulation signals, as altered by the current controller, are plotted in **Fig. 3.23(a)** by dashed lines and the switching sequence is given as well. The optimized switching sequence is still present but compared to a balanced output voltage the duration of switching state (100) is enlarged and the duration of the switching state (011) is shortened. The two switching states are redundant concerning the formation of the DM input current but show center point currents with opposite directions as shown in **Fig. 3.23(b,c)**. Whereas switching state (100) results in a

positive center point current which charges C_{on} and discharges C_{op} the switching state (011) yields to a negative center point current which discharges C_{on} and charges C_{op}. The asymmetric distribution of the two redundant switching states caused by the actions of the current controller counteracts the voltage unbalance by discharging of C_{op} and charging of C_{on} which automatically stabilizes the output voltage unbalance. A possible unbalanced output voltage is therefore stable if the proposed PWM-type phase-oriented control strategy is applied but the unbalance may not be reduced to zero. Note, that other control strategies such as hysteresis control may not yield to stable operation without active balancing in case of unbalanced output voltages [96].

An output voltage symmetry controller is therefore required to actively balance the two output voltages. The redundant switching states with different directions of the central point current i_{M} can be used for active balancing. This can be achieved by adding a variable DC component v_0 to all three modulation functions given in (3.17) which results in

$$m_{i,\mathrm{tri}}(\varphi_{\mathrm{N}}) = M\left|\left(\cos\left(\varphi_{\mathrm{N}} - \frac{2\pi}{3}(i-1)\right) + \frac{1}{4}\mathrm{tri}\,(3\varphi_{\mathrm{N}})\right) + v_0\right| . \quad (3.54)$$

The resulting modulation signals, switching states and switching sequence are illustrated in **Fig. 3.24**. The dependency of $I_{\mathrm{M,avg}}$ (averaged over one main cycle) as a function of the DC component v_0 can be carried out by evaluation of (3.51) which yields to

$$I_{\mathrm{M,avg}} = k_{\mathrm{s}}\hat{I}_{\mathrm{N}} M v_0 \quad (3.55)$$

with $k_{\mathrm{s}} \approx -\frac{6}{\pi}$.[4]

As already derived in [106] and also shown in [120] an unbalance of the partial output voltages $v_{\mathrm{M}} = 1/2(v_{\mathrm{op}} - v_{\mathrm{on}})$ without any active balancing yields to an average mid point current

$$I_{\mathrm{M,avg}} = -\frac{3}{V_{\mathrm{o}}} M \hat{I}_{\mathrm{N}} v_{\mathrm{M}} \quad (3.56)$$

which stabilizes the unbalanced operating point.

[4] Note, that in contrast to the result given in [120] with $k_{\mathrm{s}} = -1.732$ a careful evaluation of (3.51) results in $k_{\mathrm{s}} \approx -\frac{6}{\pi}$.

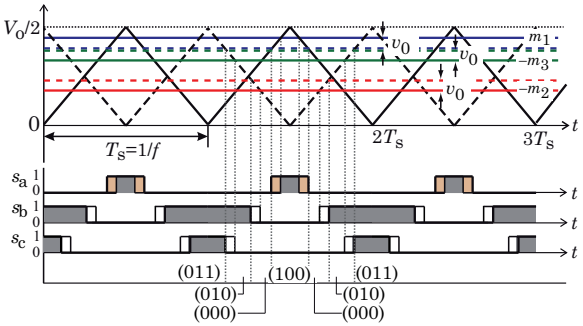


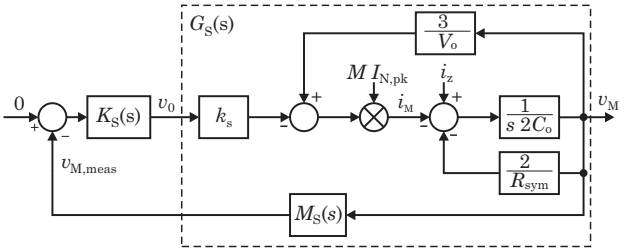
Fig. 3.24: Influence of a DC component v_0 added to all three modulation functions on the switching sequence of the rectifier system for $\varphi_N = 10\,°$. The component v_0 inversely changes the relative on time of the redundant switching states (100) and (011) and can therefore be used for active output voltage balancing.

Using (3.55) and (3.56) the control loop for the output voltage symmetry controller can be derived (cf. **Fig. 3.25(a)**). On the right hand side the characteristic of the rectifier system itself is given where it is obvious that the balancing feedback (including the controller loop) is dependent on $\hat{I}_N$ which means that a balancing at no-load or light load condition is not possible. Balancing resistors (e.g. $R_{sym} = 400\,k\Omega$) are therefore used to balance the output voltage during no-load or light load condition. The two output capacitors $C_{op} = C_{on}$ appear to be in parallel for the output voltage symmetry controller.
The measurement of the output voltage unbalance is modeled by $M_S(s)$ and $-v_{M,meas}$ is the input of the PI-type output voltage symmetry controller $K_S(s)$. The controller output i_0 is multiplied by k_s and added to the rectifier system. Instead of the PI-type controller also a P-type controller can be applied as the plant itself shows integral behavior.
According to **Fig. 3.25(a)** the open-loop transfer function

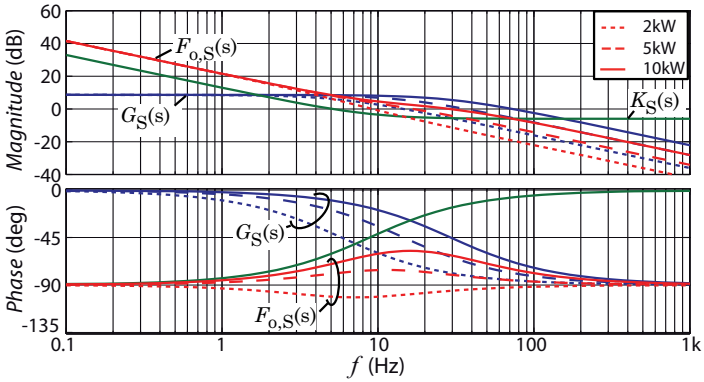
$$F_{o,S}(s) = \frac{R_{sym}}{1 + k_1 R_{sym} + K_S(s) R_{sym} k_2 + s 2 C_o R_{sym}} \tag{3.57}$$

can be calculated where $k_1 = 3M\hat{I}_N/V_o$ and $k_2 = k_S M_S(s) M \hat{I}_N$.

Fig. 3.25(b) shows the Bode plots of the controller design again for the VR250 rectifier system for different load conditions. There, $G_S(s)$ are the transfer functions of the model of the rectifier system for different load conditions, $K_S(s)$ is the transfer function of the PI-type output



(a)



(b)

Fig. 3.25: (a) Control loop of the output voltage symmetry controller and (b) Bode plot of the output voltage symmetry controller design for the VR250 rectifier system for different load conditions (controller parameters: $k_{p,v} = 0.5$, $k_{I,v} = 0.0126\,s$).

voltage symmetry controller and $F_{o,S}(s)$ are the resulting open control loop transfer function. Due to the inherent third harmonic neutral point current the control bandwidth has to be selected sufficiently lower than $3f_N$. An output power of $P_o = 10\,kW$ is used for controller design and according to **Fig. 3.25(b)** a maximum cross-over frequency of 30 Hz can be read at $P_o = 10\,kW$ with a sufficiently high phase margin. It is good practice to assign the lowest control bandwidth to the output voltage symmetry controller.

3.2.4 Load Unbalance

Up to now only symmetrically loading of the rectifier system has been analyzed. Unbalanced load currents result in a considerable neutral point current. The possible amount of neutral point current is however defined by the distribution of the redundant switching states and is therefore limited. The rectifier system is hence only able to handle a limited amount of load unbalance. This circumstance is already analyzed in detail in [106] and [96] and will be summarized here for completeness.

The work given in [106] is based on space vector modulation where the control system can directly choose one of the redundant voltage space vectors with different neutral point current directions. The distribution is described using the ratio

$$\rho_{--} = \frac{\delta_{--}}{\delta_{++} + \delta_{--}} \ , \quad \rho_{--} \in [0 \dots 1] \tag{3.58}$$

where ρ_{--} denotes the relative on-time of the switching state giving a negative center point current and ρ_{++} denotes the relative on-time of the switching state resulting in a positive center point current. An equal distribution is given by $\rho_{--} = 0.5$.
The load unbalance is defined with the factor

$$a_\mathrm{r} = \frac{R_{\mathrm{L}+} - R_{\mathrm{L}-}}{R_{\mathrm{L}+} + R_{\mathrm{L}-}} \tag{3.59}$$

which results according to [106] in the maximal possible load unbalance of

$$\begin{aligned} |a_\mathrm{r}| = \Bigg| \frac{2}{\pi}(1 - 2\rho_{--}) \Bigg(\frac{1}{M} + \frac{1}{2M^2} \Big(\sqrt{3M^2 - 1} - \frac{1}{\sqrt{3}} \Big) - \\ - \frac{\sqrt{3}}{4} \Big(1 + \frac{2\pi}{\sqrt{3}} - 2\sqrt{3} \arcsin\Big(\frac{1}{\sqrt{3}M} \Big) \Big) \Bigg) \Bigg| \ . \end{aligned} \tag{3.60}$$

The results are plotted in **Fig. 3.26**. It is obvious that for a typically high modulation index only a limited load unbalance can be handled (e.g. $\approx 25\,\%$ for $M = 1$). The reason can be found in the decreasing on-times of the redundant switching states for higher modulation indices. Also at $M = 2/3$ a load unbalance of $100\,\%$ ($a_\mathrm{r} = 1$) cannot be handled.

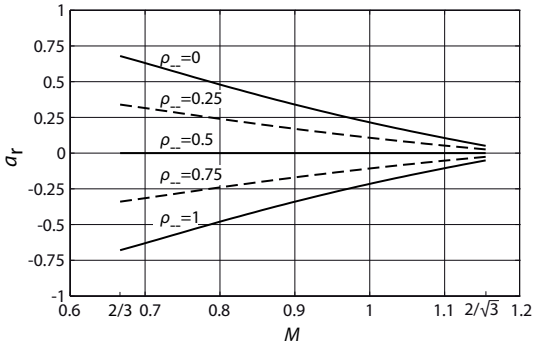


Fig. 3.26: Admissible load unbalance a_r as a function of the the modulation index M and the ratio ρ_{--} according to (3.60) and [106].

3.2.5 Operating Range

The rectifier system requires a set of protection features in order to guarantee a safe operation within the specifications. One of the most important features is the observation of the output voltage v_o and the balancing of the two output voltages v_M as the boost circuit would continue to boost up the output voltage to unacceptable levels in case of a malfunction of the output voltage measurement. If an overvoltage is detected the rectifier system immediately should stop operation which can be achieved by disabling the PWM and SCRs.

In case of an overload the situation is more precarious. The limitation of the input power can be achieved by limitation of the output of the voltage controller P_o^* or by limitation of the conductance G_e^* which also guarantees sinusoidal input currents in case of an overload. Besides the limitation of G_e^* also the output voltage has to be observed. One has to keep in mind that by limitation of G_e^* only the input power is limited and not the output power. If a larger power level is required from the load the output voltage and therefore also the delivered output power will decrease until it is equal to the input power limitation. Assuming resistive load the output voltage will decrease according to the additional required power if the system is operating with a modulation index below $M = 1$.

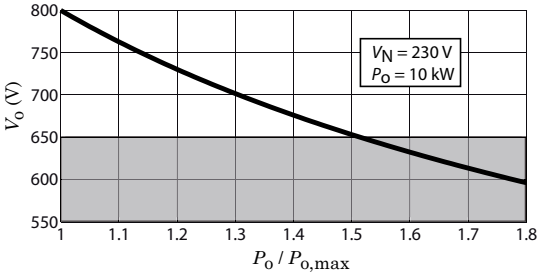


Fig. 3.27: Decrease of output voltage V_o if the rectifier is overloaded with a resistive load expressed as output power at nominal output voltage V_o ($V_N = 230\,V$, $M = 0.813$). Please note that the input power is limited and that therefore the output voltage and hence also the output power is reduced until it is equal to the limited input power.

Fig. 3.27 shows the reduced output voltage

$$V_o = V_{o,nom}\sqrt{\frac{P_{o,max}}{P_o}} \tag{3.61}$$

as a function of the overload situation for a rectifier system operating with $M = 0.813$ ($V_{o,nom} = 800\,V$, $V_N = 230\,V$) at resistive load. According to **Fig. 3.27** an overload of $1.5P_{o,max}$ does not yield to an unsafe operating condition as the rectifier output voltage is reduced to 650 V which also reduces the output power to 10 kW for a resistive load as defined by the maximum admissible input current. If the rectifier system is, however, further overloaded the output voltage reaches the peak-to-peak values of the mains voltage and the controllability of the rectifier system is lost due to the conducting rectifier diodes of the diode bridge. This has to be avoided by disabling of the rectifier control system which can be performed by disabling the PWM and the SCRs. In general a boost-type rectifier circuit can not limit the output power or output current due to the existing boost diodes.

As a power limitation for overload has to be implemented also a power limitation on the input is required. Due to the limited current capability of the applied semiconductors an overcurrent protection must be considered. This limits the operating range of the rectifier system at lower mains voltages. **Fig. 3.28** shows the power limitation for a 10 kW rectifier system (VR250). The rectifier system is able to deliver the full

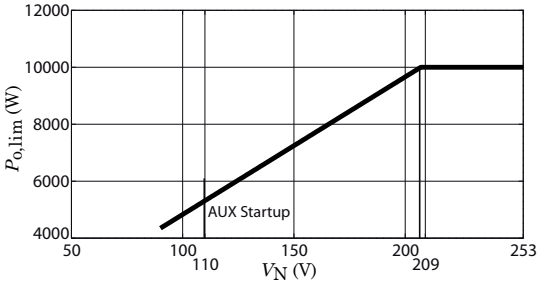


Fig. 3.28: Output power limitation as a function of low mains voltage V_N for the VR250 rectifier system.

output power for mains voltages between $V_N = 209\,V$ and $V_N = 253\,V$. The output power must, however, be limited to

$$P_{o,lim} = 3V_N I_{N,lim} \tag{3.62}$$

if the mains voltage V_N is further reduced (an ideal symmetrical mains supply is assumed for the calculation) where $I_{N,lim}$ is the maximum rms input current. As the auxiliary power supply starts to operate at $V_N = 110\,V$ this mains voltage is the absolute minimum for a safe operation of the rectifier system.
Besides an overcurrent detection for the input currents also the mains voltages must therefore be observed.

To summarize, the following protection functions must be implemented in a constructed rectifier system:

- Observation of output voltage;
- Observation of output voltage balance;
- Input current limitation;
- Limitation of input/output power according to the mains voltage and input current limitation;
- Observation of mains voltages;
- Overtemperature protection;

3.2.6 Reactive Power Capability

It was assumed for the previous calculations that the input currents are in phase with the mains voltages which means that ideally a power factor of $\lambda = 1$ is achieved. As the inductor currents are used for current control, only these currents are in phase with the mains voltages. The leading currents, drawn by the EMI filter capacitors, however, decrease the power factor at light load or no-load conditions. These capacitive currents are negligibly small for systems with a mains frequency of 50 Hz/60 Hz, but must be taken into account for the mains frequency range of 360 Hz–800 Hz. The power factor of the rectifier system could be improved if operation with a lagging inductor current is possible. Such a phase displacement implies, that in addition to the active power also reactive power is generated and in the following the reactive power capability of the VR topology is therefore analyzed.

An analysis performed in [80] resulted in a possible phase displacement between mains voltage and inductor current of

$$-30\,^\circ \leq \varphi_{\mathrm{vi}} = \varphi_v - \varphi_{\mathrm{i}} \leq 90\,^\circ\ . \tag{3.63}$$

The sector $\varphi_{\mathrm{N}} \in [-30\,^\circ, 30\,^\circ]$ is used in the following to discuss this result. The possible switching states of this sector are depicted in **Fig. 3.29(a)**. One has to keep in mind, that the sign of the input currents determines the transitions from one sector to the next sector. A current space vector located $\underline{i}_{\mathrm{N}}$ at the sector boundary $\varphi_{\mathrm{i}} = 30\,^\circ$ is shown in **Fig. 3.29(a)**.

According to **Fig. 3.29(a)**, leading voltage space vectors $\underline{v}_{\mathrm{r}}$ in the gray shaded area can be generated. Note, that practical implementations typically show a modulation index between $M = 2/3$ and $M = 2/\sqrt{3}$ if the voltage drop across the boost inductors is neglected. This is typically permitted for rectifier systems with high power density. A maximal rectifier voltage space vector magnitude equal to the magnitude of the voltage vector for switching state (110) can be generated which yields to a lagging phase-shift capability of $\varphi_{\mathrm{vi,lag}} = 30\,^\circ$. The result is only valid for $M = 2/3$ and has to be reduced for higher modulation indices.

In [80] the voltage drop of the boost inductors is not neglected which results, depending on the size of the boost inductor, in a considerably

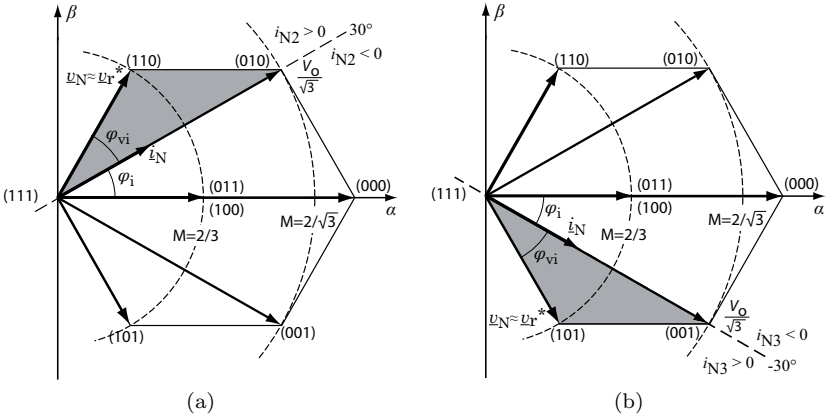


Fig. 3.29: Space vector diagrams illustrating the phase displacement capability of the VR system. (a) Space vectors for maximal lagging input current at the sector limit $\varphi_i = 30\,°$ and (b) space vectors for maximal leading input current at the sector limit $\varphi_i = -30\,°$ for the sector $\varphi_i \in [-30\,°, 30\,°]$.

increased phase displacement capability. A maximal lagging phase shift capability of $\varphi_{vi,lag} = 90\,°$ can theoretically be achieved by a sufficiently large boost inductor.

Fig. 3.29(b) shows the situation for maximal leading inductor currents. A current space vector at the sector boundary $\varphi_i = -30\,°$ is marked. It is obvious that, similar to the situation for maximal lagging input current, the maximal rectifier voltage space vector magnitude is equal to the switching voltage vector magnitude for state (101) which yields to a leading phase shift capability of $\varphi_{vi,lead} = -30\,°$ for $M = 2/3$.

The derived phase displacement capability is only valid for a modulation index of $M = 2/3$ and decreases for higher modulation indices. Using simple geometric interrelationships on **Fig. 3.29**, a practical phase displacement capability of

$$-\left(\arcsin\left(\frac{1}{M\sqrt{3}}\right) - 30\,°\right) \leq \varphi_{vi} \leq \left(\arcsin\left(\frac{1}{M\sqrt{3}}\right) - 30\,°\right) \quad (3.64)$$

can be calculated which is dependent on the modulation index M. This is a more practical limitation compared to the theoretical limits given in (3.63).

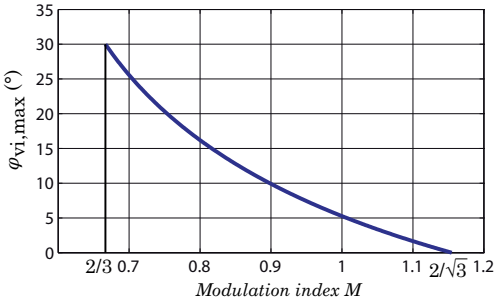


Fig. 3.30: Possible phase displacement of the VR system according to (3.64) as a function of the modulation index M.

The possible phase displacement is plotted in **Fig. 3.30** as a function of the modulation index M. A phase displacement of $\pm 15\,^\circ$ can be read at the nominal operating point of $V_\mathrm{N} = 230\,\mathrm{V}$ and $V_\mathrm{o} = 800\,\mathrm{V}$ ($M = 0.815$).

Implementation

In order to implement the derived phase displacement capability, adequate switching states have to be selected which could be performed using SVM. As verified by simulation, the average mode current controller of section 3.2.1 in conjunction with the proposed PWM concept of section 3.1.1 cannot directly be applied without considerably increased input current distortions even if a phase-shifted feedforward signal is used.

Fig. 3.31 shows schematically the input voltage and input current of the rectifier system for a phase displacement of $\varphi_\mathrm{vi} = 30\,^\circ$. The switch S_{1-} is gated with the PWM signal during negative phase voltages. After zero-crossing of the input current the situation of positive input current direction with simultaneous negative input voltage occurs. The negative mains diode $D_{1\mathrm{N}-}$ blocks and the switching actions of S_{1-} take no effect. An adjusted feedforward of the mains voltage does not help to improve the situation as the remaining phase voltage is still negative during this period.

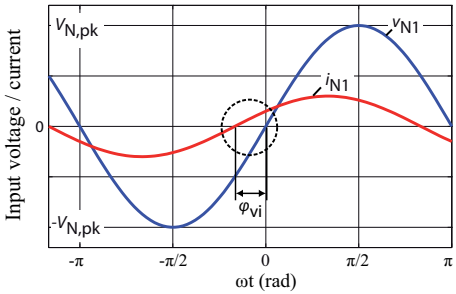


Fig. 3.31: Input voltage v_{N1} and input current i_{N1} of the VR system for a phase displacement of $\varphi_{vi} = 30\,^\circ$.

The proposed PWM concept can, however, be applied if a proper CM-signal is added to the modulation function such that after the zero crossing of i_{N1} also a positive input voltage is present with respect to the output voltage midpoint M (cf. **Fig. 3.32**).

The CM voltage can be implemented by rectangular voltage blocks with a specific amplitude at the time instants where the currents and voltages show different sign. A phase shifted voltage $v_{Ni,p}$ can be used thereto in the controller implementation. **Fig. 3.32** shows the simulated system behavior of a rectifier system operating with a (maximum) phase lag of 15 ° for $M = 0.815$ ($V_N = 230\,V$, $f_N = 400\,Hz$, $V_o = 800\,V$ and $P_o = 10\,kW$). The rectangular CM voltages are added to the modulation function and the resulting behavior of m_1 at zero crossing can be read in **Fig. 3.32**. The mains currents show no input current distortions which confirms the proper operation of the proposed concept. The minimum required amplitude to shift the modulation voltage is given by

$$v_{CM,p} = \hat{V}_N \sin(\varphi_{vi}) \ . \tag{3.65}$$

In a digital implementation, the corresponding voltage levels can either be determined using a lookup table for the sin-function or by the approximation $\sin(x) \approx x$ which is only valid for small x.
Another possibility is to use the maximum possible phase-shift which is a function of the modulation index M. The amplitude is then given by

$$v_{CM,p} = \hat{V}_N \sin\left(\arcsin\left(\frac{1}{M\sqrt{3}}\right) - 30\,^\circ\right) \tag{3.66}$$

which is also not very convenient for a digital implementation. A linear

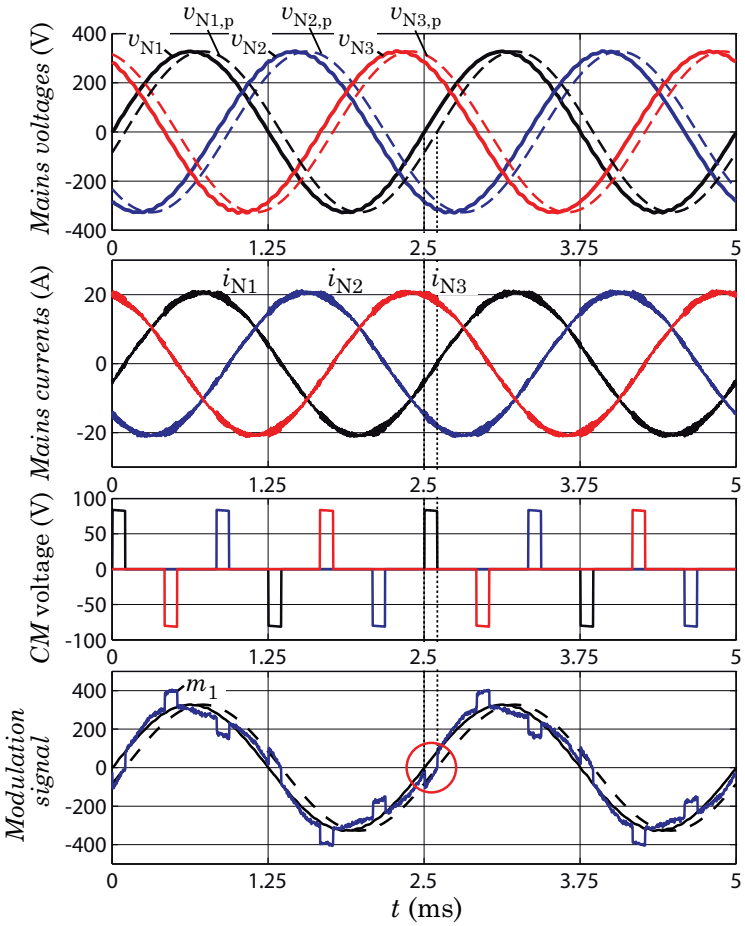


Fig. 3.32: Simulation result of a VR system operating with a lagging current of 15 ° using the proposed CM voltages for $M = 0.815$ ($V_N = 230\,V$, $f_N = 400\,Hz$, $V_o = 800\,V$ and $P_o = 10\,kW$).

approximation

$$v_{CM,p} = \frac{V_o}{2}\Big(0.76 - 0.67M\Big) \tag{3.67}$$

can, however, be used to simplify this relationship (cf. **Fig. 3.33**) which is suitable for a digital implementation. This approximation is

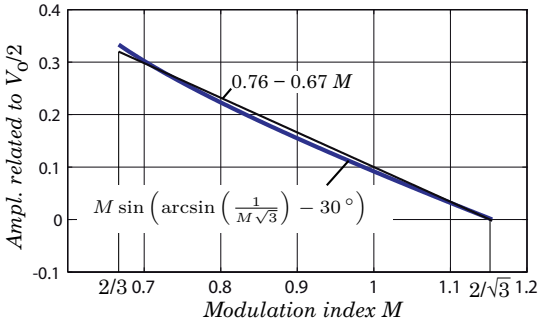


Fig. 3.33: Linear approximation of $v_{\mathrm{CM,p}}/(V_\mathrm{o}/2)$ given in (3.66).

used for the simulation results given in **Fig. 3.32**.

If the amplitude of the injected CM-voltage is too large, the modulation function will exceed its maximum voltage and over-modulation will occur which finally results in considerably increased input current distortions. It therefore has to be checked whether the proposed CM-voltages exceed the modulation range in a specific operation point.
The CM-voltages are added to all three phases and the largest voltage occurs at 60 ° for the duration of the phase shift φ_vi (zero-crossing of another phase). The sum of the phase voltage and the added CM-signal must not exceed the modulation range which is equal to $V_\mathrm{o}/2$. This yields to

$$\begin{aligned} \hat{V}_\mathrm{N} \sin\left(\varphi_\mathrm{vi} + 60\,^\circ\right) + \hat{V}_\mathrm{N} \sin\left(\arcsin\left(\frac{1}{M\sqrt{3}}\right) - 30\,^\circ\right) &\leq \frac{V_\mathrm{o}}{2} \\ M \sin\left(\varphi_\mathrm{vi} + 60\,^\circ\right) + M \sin\left(\varphi_\mathrm{vi}\right) &\leq 1 \\ 2M \sin\left(\varphi_\mathrm{vi} + 30\,^\circ\right) \cos\left(30\,^\circ\right) &\leq 1 \\ M\sqrt{3} \sin\left(\varphi_\mathrm{vi} + 30\,^\circ\right) &\leq 1 \end{aligned} \tag{3.68}$$

and with a maximum possible phase-shift of $\varphi_\mathrm{vi} = 30\,^\circ$ at $M = \frac{2}{3}$ the relation

$$\begin{aligned} M\sqrt{3} \sin\left(\varphi_\mathrm{vi} + 30\,^\circ\right) &\leq 1 \\ \frac{3M}{2} &\leq 1 \end{aligned} \tag{3.69}$$

is fulfilled which confirms that the modulation range is not exceeded by

application of the proposed modulation function given in (3.66).
The proposed CM-voltage can be used in combination with the low-frequency third harmonic signal used to increase the modulation range or to reduce the low-frequency current magnitude in the output capacitor (cf. section 3.1.2). It has to be noted, however, that the proposed concept increases the current ripple in the output capacitor C_{o}.
Alternative to the proposed concept where rectangular CM voltages are used, a low-frequency phase-shifted third-harmonic sinusoidal signal can be used to implement the reactive power capability. The amplitude and phase of the third-harmonic signal must then, however, be adjusted such that the resulting zero-crossing of the modulation signal is in phase with the corresponding mains current which is a complex task. The proposed concept in contrast derives the CM-signal from the input voltages/currents in combination with an easy calculation using the modulation index M and is therefore preferred.

Chapter 4

Multi-Objective Optimization of Power Electronic Systems

The performance of a power electronic system is given by several characteristics. Such characteristics can be the total volume or weight of the system, the total efficiency or the total costs. Power electronic systems designed for different applications have to fulfill different requirements. This becomes immediately apparent if e.g. the requirements of a mains interface for a photovoltaic (PV) system are compared with the requirements of a mains interface for MEA applications. An outstanding efficiency and low system costs are the main requirements for the PV system. As such a system is mounted on the ground power density and weight are rather secondary requirements.
In contrast to PV systems, a mains interface to be applied on an aircraft has to exhibit a small size, low weight and a high reliability. System costs are also very important but are rather secondary requirements for aircraft applications. Of course, also a high efficiency and good input current quality are necessary but a slightly reduced efficiency can be tolerated if the size or the weight of the power electronic system is decreased on the other hand. These two examples clearly illustrate that different applications basically show equal requirements but different weighting of the specific items.

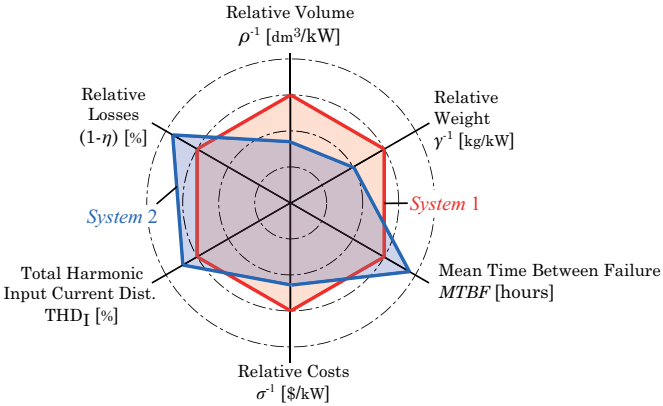


Fig. 4.1: System performance of a power electronic system where only performance indices being important for aircraft applications are shown. Two different systems (e.g. System 2 is designed for higher power density) will show different performance indexes.

Fig. 4.1 shows the most important characteristics for aerospace applications together with the corresponding performance indices. Next to efficiency, volume and weight also reliability, costs and input current quality are of high importance. Several other characteristics such as shape, EMI noise emissions, operating temperature, etc., may of course also be of high importance and may be added to **Fig. 4.1**. All the characteristics are described by a corresponding performance index which will shortly be discussed below. In **Fig. 4.1** a reference system (*System 1*) is compared to a *System 2* which is optimized for higher power density and lower weight. A higher power density and lower weight can be achieved by an increase in switching frequency. Due to increased switching losses, the efficiency of the rectifier system will be reduced. Also a lower input current quality and maybe a lower reliability could result. The optimization considering only one performance index may, accordingly, result in a considerably reduction of the performances characterized by other performance indices. A compromise must therefore be found between several competing requirements which can be done by a multi-objective optimization which will be discussed below.

The performance indices given in **Fig. 4.1** will shortly be defined

and discussed in the following.

A) Power Density

Power Density describes the degree of compactness of a converter system

$$\rho = \frac{P_\mathrm{o}}{V_\mathrm{tot}} = \left[\frac{\mathrm{kW}}{\mathrm{dm}^3}\right] \tag{4.1}$$

using the output power P_o and the total volume V_tot of the power electronic system. The power density of a constructed system can easily be determined by measuring the total volume. During an analytical optimization of the system the evaluation of the total volume is, however, a very complex task and the sum of the boxed volumes of system elements is often used instead. Also power densities given in literature must be read very carefully as often the EMI filter or cooling system is not included what, of course, increases the power density considerably. The performance of the cooling system itself can be described using the Cooling System Performance Index (CSPI) [122]

$$CSPI = \frac{1}{R_\mathrm{th} V_\mathrm{hs}} = \left[\frac{\mathrm{W}}{\mathrm{Kdm}^3}\right] \tag{4.2}$$

using the thermal resistance R_th and the volume V_hs of the cooling system. Optimized forced air coolers reach values up to $20\,\mathrm{W/(Kdm^3)}$ as shown in [123].

B) Efficiency

The most common performance index of a power electronics system is the efficiency

$$\eta = \frac{P_\mathrm{o}}{P_\mathrm{in}} \cdot 100\,\% \tag{4.3}$$

where P_in is the input power of the system. This index increases in importance due to rising energy prices and increasing demand for environmentally friendly products. The rated output power is typically used for calculation of the system efficiency which may not deliver very meaningful results for applications where also the efficiency at partial load is important. A mean efficiency, as given in [124] and [125], can be defined for such applications. It has to be added here, that a high converter efficiency may not automatically yield to highest efficiency of the total system.

C) Output Power to Unit Weight
The relative weight of a power electronic system can be expressed by the output power to unit weight ratio

$$\gamma = \frac{P_{\mathrm{o}}}{W_{\mathrm{tot}}} = \left[\frac{\mathrm{kW}}{\mathrm{kg}}\right] \tag{4.4}$$

where W_{tot} is the total weight of the power electronic system. This performance index is very important for aircraft applications and for all mobile applications as the fuel consumption can be reduced if a high γ is achieved. On the other hand, a large weight is acceptable for ground based stationary systems, such as e.g., uninterruptible power supplies for computer servers.

D) Output Power to Costs Ratio
A very important performance index in industry are the relative costs

$$\sigma = \frac{P_{\mathrm{o}}}{C_{\mathrm{tot}}} = \left[\frac{\mathrm{kW}}{\$}\right] \tag{4.5}$$

using C_{tot} describing the total costs of the power electronic system. The calculation of the relative costs is difficult as on one hand the system costs are mainly dependent on the number of manufactured units and on the other hand detailed cost models of several companies, e.g., cost models for manufacturing of inductors, are not public so that a profound research is hardly possible. Despite these uncertainties relative costs are often used to compare different commercially available products. In this case the correctness of the absolute costs is of limited importance

E) Reliability
Reliability of power electronic systems is a huge research area and will only be mentioned briefly here. The reliability of a system is often characterized by the mean time between failure (MTBF [hours]) or the failure rate per unit - year λ [1/year] and the MIL-Handbook-217F [126] or the IEEE-Std. 493-2007 [127] can be used to determine the reliability of a system. One has to keep in mind, that the MTBF and the failure rate λ are probabilities and do not include any information on individual failures. Some informations on life-time prediction of semiconductor modules can be found in [128] and [129].

F) Input Current Quality
As this work deals with unidirectional three-phase rectifier systems this performance index is added which is actually only relevant for rectifier systems. The input current quality is expressed by the total harmonic distortion of the input currents

$$\mathrm{THD_I} = \sqrt{\frac{\sum_{k=2}^{K} I_{(\mathrm{k}),\mathrm{rms}}^2}{I_{(1),\mathrm{rms}}^2}} \cdot 100\,\% \tag{4.6}$$

where $I_{(\mathrm{k}),\mathrm{rms}}$ denotes the rms current value of the k-th input current harmonic, $k = 1$ is the fundamental, and K is the total number of harmonics used to calculate the $\mathrm{THD_I}$. Next to the requirements of low weight, high power density or high efficiency, this requirement fundamentally influences the suitable rectifier topology. A high input current quality, expressed by a low $\mathrm{THD_I}$, can for instance not be achieved by a simple three-phase diode bridge or requires a multi-pulse, hybrid or active rectifier topology or both. Next to the $\mathrm{THD_I}$-value also limitations on the individual harmonics must be fulfilled (see also section 1.1) but such a side condition cannot easily be considered for a system comparison or optimization or both.

Design and implementation of a power electronic system means that design parameters, such as switching frequency or amount of inductor current ripple etc., are chosen in such a way that selected performance indices are met. In [130], a mathematical viewpoint of the power electronic system design is discussed in detail and only summarized at this point as this mathematical description clearly illustrates the arising optimization problems.

All free design parameters can be summarized in a parameter vector

$$\boldsymbol{x} = (x_1, x_2, \ldots x_n) \tag{4.7}$$

and all design constants, e.g., relative permeability μ_r or saturation flux density B_sat of a magnetic material or forward voltage drop of a diode in the design constants vector

$$\boldsymbol{k} = (k_1, k_2, \ldots k_m)\ . \tag{4.8}$$

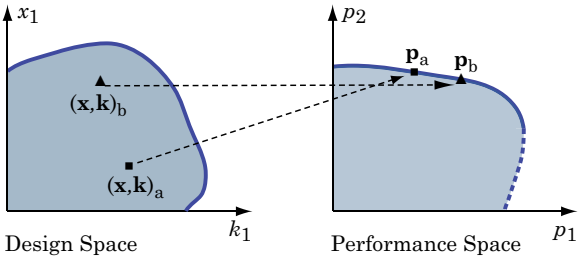


Fig. 4.2: Mapping of the Design Space into the Performance Space. The two different points in the Design Space $(\vec{x},\vec{k})_\mathrm{a}$ and $(\vec{x},\vec{k})_\mathrm{b}$ result in two different points in the Performance Space $\vec{p}_\mathrm{a}$ and $\vec{p}_\mathrm{b}$.

In addition, all system specifications and system operating requirements, such as input voltage range, output voltage or nominal output power are summarized in the requirement vector

$$\boldsymbol{r} = (r_1, r_2, \ldots r_l) \ . \tag{4.9}$$

The vectors $\boldsymbol{x}$ and $\boldsymbol{k}$ form together a multi-dimensional Design Space and exactly one point is allocated for each parameter combination. In **Fig. 4.2(a)**, a two-dimensional Design Space is shown as example where the points $(\boldsymbol{x},\boldsymbol{k})_\mathrm{a}$ and $(\boldsymbol{x},\boldsymbol{k})_\mathrm{b}$ are depicted. To give an example, the design parameter x_1 and the design constant k_1 shall be the switching frequency f_s and the permeability μ_r of an applied magnetic material. The point $(\boldsymbol{x},\boldsymbol{k})_\mathrm{a}$ may correspond to a switching frequency of 10 kHz and the magnetic material N87 from Epcos Inc. ($\mu_\mathrm{r} = 2200$). A switching frequency of 500 kHz is on the other hand assumed in the point $(\boldsymbol{x},\boldsymbol{k})_\mathrm{b}$ and for the higher switching frequency the high-frequency magnetic material N49 from Epcos Inc. with a permeability of $\mu_\mathrm{r} = 1500$ may be chosen.

Also the performance indices define a multi-dimensional Performance Space (cf. **Fig. 4.2(b)**). The performance of the design can now be expressed using the performance indexes

$$p_i = f_i(\boldsymbol{x},\boldsymbol{k}) \tag{4.10}$$

and the boundary conditions

$$g_\mathrm{p} = (\boldsymbol{x},\boldsymbol{k},\boldsymbol{r}) = 0 \quad p = 1,2\ldots H \tag{4.11}$$

$$h_\mathrm{q} = (\boldsymbol{x},\boldsymbol{k},\boldsymbol{r}) \geq 0 \quad q = 1,2\ldots Q \ . \tag{4.12}$$

The mapping functions $f_i(\ldots)$ map the points of the Design Space into the Performance Space (see also **Fig. 4.2**). A variation of the system parameters and constants results in an array of points in the Performance Space.

Several approaches for optimizing power electronic circuits can be applied. A single-objective optimization

$$p_i \rightarrow \max \tag{4.13}$$

tries to find the best design regarding one performance index.

Highest possible efficiency or power density of a converter system would be an example of such single-objective optimization. A high efficiency, however, typically reduces the power density of the power electronic system which is not considered in this optimization as e.g. only a system with highest possible efficiency should be achieved. Such optimization will be discussed in section 5, where the highest possible power density of the three-phase VR topology is evaluated regardless of a drop in efficiency. A single-objective optimization of a single-phase rectifier circuit regarding highest efficiency can be found in [131] and a single-objective optimization of a 5 kW DC/DC converter system for telecom applications is given in [132].
An optimization procedure which considers several performance indices such as efficiency, power density and costs

$$\sum w_i p_i = \sum w_i f_i(\boldsymbol{x}, \boldsymbol{k}) \Rightarrow Min \ , \tag{4.14}$$

is called a multi-objective optimization [130]. The variable w_i defines the weighting of the different performances. A multi-objective optimization results in a so called Pareto Front as it illustrates the maximal possible performance index p_{i} at a performance index p_j for the applied technologies (cf. **Fig. 4.2**). Careful evaluation of this Pareto Front allows to give a general statement on the examined performance indexes. An even more powerful statement can be given if also some major design parameters are marked in the Performance Space.
An interesting performance analysis can be performed using the performance indices efficiency η and power density ρ which finally results in the η-ρ-Pareto Front. Such an analysis has been carried out for single-phase rectifier systems and the very interesting results can be found in [133]. Results for a 5 kW DC-DC converter are given in [134].

The evaluation of the η-ρ-Pareto Front for hard switched DC/DC converters is given in [135].
Another interesting Pareto Front using other performance indices can be calculated for rectifier systems: The efficiency η is there plotted as a function of the maximum achievable input current quality $\mathrm{THD_I}$ which results in the η-$\mathrm{THD_I}$-Pareto Front [136]. Details will be discussed in section 5.5.

The mutual dependence of performance indices e.g., of the efficiency η on the power density ρ, can be determined by calculating the gradients of the tangents to the Pareto Curve which results for the given example in

$$s_{\eta\rho} = \left.\frac{\partial \eta}{\partial \rho}\right|_P \tag{4.15}$$

where P is the corresponding design point.

In order to calculate the influence of a specific technology or of a specific design parameter on the system performances, the sensitivity matrices

$$\mathbf{s_{px}} = \begin{pmatrix} \frac{\partial p_1}{\partial x_1} & \cdots & \frac{\partial p_1}{\partial x_n} \\ \vdots & & \vdots \\ \frac{\partial p_i}{\partial x_1} & \cdots & \frac{\partial p_i}{\partial x_n} \end{pmatrix} \tag{4.16}$$

and

$$\mathbf{s_{pk}} = \begin{pmatrix} \frac{\partial p_1}{\partial k_1} & \cdots & \frac{\partial p_1}{\partial k_m} \\ \vdots & & \vdots \\ \frac{\partial p_i}{\partial k_1} & \cdots & \frac{\partial p_i}{\partial k_m} \end{pmatrix} \tag{4.17}$$

can be calculated. Using the two sensitivity matrices the impact of a technology improvement $\Delta \boldsymbol{k}$ or of an adaption of a design parameter $\Delta \boldsymbol{x}$ can be studied using

$$\Delta \boldsymbol{p}_\mathbf{x} = \mathbf{s_{px}} \Delta \boldsymbol{x} \tag{4.18}$$

$$\Delta \boldsymbol{p}_\mathbf{k} = \mathbf{s_{pk}} \Delta \boldsymbol{k} \ . \tag{4.19}$$

The sensitivity matrices are very useful to evaluate whether a possible technology step considerably improves the performance indexes or not. Details regarding the sensitivity analysis can be found in [130] and [137] where a change in semiconductor technology (from Si to

SiC) is evaluated for a 3.2 kW bridgeless PFC rectifier and where the evaluation surprisingly shows only a minor improvement in efficiency.

Multi-objective optimizations as given in (4.14) and the calculation of a multi-dimensional Performance Space as well as a sensitivity analysis according to (4.16)-(4.19) are a very powerful tools to analyze and illustrate the characteristics and performances of a power electronic system. One has, however, to keep in mind that all results rely on the applied analytical models used to calculate the performance indices. Whereas, for instance, the efficiency η can be calculated very precisely, the calculation of the power density ρ is a more complex task as the power density is heavily dependent on the final construction of the power electronic system. This can be avoided if boxed volumes are used which is very effective to compare different technologies but the resulting power density will not fully coincide with the power density of an actually constructed system. Another hardly predictable performance index is the input current quality $\mathrm{THD_I}$ as several effects such as cusp distortion or DCM operation must be included into the model. More details on the modeling of the input current distortions will be given in section 5.1.2.

In the following, a more practical single-objective optimization regarding maximum achievable power density for a 10 kW VR system will be shown where several theoretical and practical issues will be addressed.

Chapter 5

Power Density Optimization of VR Topology

In this chapter, the design and implementation of a power density optimized 10 kW active VR system is discussed. A single-objective optimization only focusing on the maximum achievable power density ρ and accepting a considerable drop in efficiency will be applied. The six-switch Vienna-type rectifier topology (cf. **Fig. 5.1**) is selected for optimization as it has been identified as an ideal topology for a high power density unity power factor rectifier in past research and development projects. The final constructed rectifier system shall fulfill the specifications listed in **TABLE 5.1**. The system is only designed for a mains frequency of 50 Hz/60 Hz but the results are conditionally also valid for the higher mains frequency of aircraft applications (360 Hz–800 Hz).

The rectifier system must comply with the EMI standard CISPR Class A [138] and water cooling shall be applied. Based on the experiences derived from the implementation of a rectifier system with a switching frequency of 400 kHz and a power density of $\rho = 8.5\,\mathrm{kW/dm^3}$ [117], the route to very high power density has been drafted in [139]. An increase of power density implies a reduction of the converter size if the power level is unchanged. The size of the active components, such as switches and diodes, can be minimized by application of a low

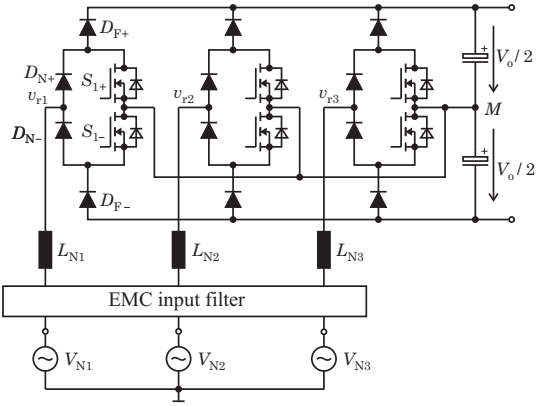


Fig. 5.1: Schematic of the three-phase three-level six-switch Vienna-type rectifier used for power density optimization.

TABLE 5.1: Specification of the 10 kW rectifier system considered for the implementation of a maximum power density demonstrator.

Input voltage	$V_{N,ll} = 320\,V \ldots 480\,V$
Mains frequency	$f_N = 50\,Hz/60\,Hz$
Output power	$P_o = 10\,kW$
Output voltage	$V_o = 2 \times 400\,V$
Output voltage ripple	$\Delta V_o < 0.1 V_o$
EMI	Compliance with CISPR Class A
Cooling	Water cooled

profile power module including all semiconductor dies. Such a module, using CoolMOS switches and SiC free-wheeling diodes, was already used in [117]. The applicability of this module has to be evaluated.
The size of the passive components, i.e. of the EMI filter, boost inductors, etc., can only be reduced by increasing the switching frequency. In [140] a maximal possible power density only of the EMI filter and cooling system of $\rho_{EMI,max} = 63.9\,kW/dm^3$ at a switching frequency of 2.1 MHz is calculated. This calculation is very optimistic and as will be shown in this work, the power density of a practical EMI filter implementation is far from this calculated value. An interesting result of the EMI filter power density optimization given in [140] is that the switch-

ing frequency has to be in the MHz-range. An increase in switching frequency, however, comes along with higher switching losses reducing the efficiency of the rectifier system. Therefore, not only the switching frequency but also the switching speed has to be increased. The maximal achievable switching speed of the semiconductors is mainly limited by parasitic elements, i.e., by parasitic and coupling capacitances and stray inductances and the switching behavior of the intended diode/switch combination is therefore analyzed in detail in section 5.1 and an approach to damp switching transient oscillations is given in 5.2.
Because of the very high switching frequency another parasitic effect of MOSFETs plays a role: The effective duty cycles of the MOSFET are enlarged due to turn-off delays of the MOSFETs which finally yields to input current distortions. This effect is analyzed and discussed in detail in section 5.1.2 and an approach to overcome this drawback is proposed.
Based on the derived limitations regarding switching speed a switching frequency is chosen in section 5.1.5 for the intended 10 kW hardware prototype showing highest power density. A detailed derivation of semiconductor losses is given and the resulting system efficiency is calculated. The calculated efficiency is combined in section 5.5 with the estimated input current quality which finally results in the $\eta - \mathrm{THD_I}$-Pareto Front illustrating the mutual dependence of input current quality and efficiency.

Limited switching speed and consequentially increased switching losses are not the only limiting factors for an increase in switching frequency. Current control of such MHz-switched three-phase converter systems poses a real challenge. A classical analog average current controller shows several problems such as limited precision. On contrary, a purely digital implementation suffers from the limited processing speed of the processing hardware (e.g., digital signal processor (DSP)). Field programmable gate arrays (FPGAs) intrinsically offer parallelization and can therefore be used to overcome this limitation and a novel current controller implementation employing a modern high speed FPGA is proposed in section 5.6.

The design and implementation of a power density optimized EMI filter is shown in section 5.7. A novel CM filter strategy is employed where the rectifier output shows no high frequency CM voltage. Selection of applicable materials for filter construction turned out to be one

of the decisive points for switching frequencies in the MHz-range.

The constructed hardware prototype is finally discussed in section 5.8 and measurements confirming the proper operation of the prototype system are given in section 5.9.

5.1 High-Speed Switching Behavior

The reduced semiconductor voltage stress of the VR topology supports the application of common high efficiency Super Junction (SJ) devices (e.g., CoolMOS [141]) showing a blocking voltage of 600 V even for a grid voltage of 230 V and an output voltage of $V_o = 800\,V$. This circumstance is the key to ultra-high switching frequencies as with IGBTs only switching frequencies up to 20-50 kHz can be implemented. In order to achieve a high efficiency conduction losses as well as switching losses have to be reduced. The on-state resistance of high-voltage (HV) MOSFETs ($V_{BR,SS} = 600\,V$) is dominated by the drift region resistance and it is well known that this resistance is intrinsically dependent on the break-down voltage $V_{BR,SS}$ of the device according to

$$R_{DSon} \propto {V_{BR,SS}}^{2.4...2.7} \tag{5.1}$$

(cf. [142]). Superjunction devices break with this rule and achieve much lower area specific on-state resistances [143]. Switching losses are dominant for hard switched converters with switching frequencies in the MHz-range. In order to limit switching losses, the switching speed must be increased if the converters switching frequency is raised. The switching speed is determined mainly by parasitic elements of the power semiconductors (MOSFETs and diodes) and by the wiring. The parasitic capacitances of the MOSFET hence mainly influence the system behavior and efficiency [144]. In respect of losses, a more meaningful Figure Of Merit (FOM)

$$FOM = \frac{1}{R_{DSon} E_{400V}} \tag{5.2}$$

can be defined [145], where R_{DSon} is the MOSFETs on-state resistance and E_{400V} is the stored energy in the MOSFETs output capacitance (C_{oss}) at $V_{DS} = 400\,V$. Modern SJ devices exhibit smaller output capacitances (at $V_{DS} = 400\,V$) than standard HV-MOSFETS and are therefore ideally suited for hard-switched high-frequency rectifier systems. The MOSFETs output capacitance is proportional to the

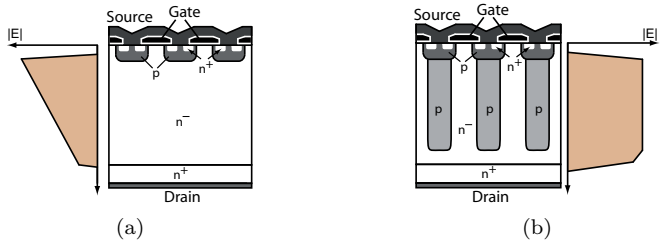


Fig. 5.2: Cross-section and electrical field distribution of (a) a conventional HV-MOSFET and (b) a SJ device (e.g. CoolMOS)). Whereas the HV-MOSFET shows a triangular shaped electrical field distribution a SJ device shows a mostly squared distribution.

chip area A_{Chip} and shows a strong nonlinear dependency on the applied drain-source voltage. The output capacitance of super junction MOSFETs rises from a few 100 pF to over 10 nF for low-blocking voltage levels. As published in [117], this effect causes long delay times at turn-off of the device which result in significant current distortions at lower current levels. This effect is even more distinctive if higher switching frequencies are used or if a device with a large chip area is applied. This is in basic contradiction to the requirement of low conduction losses (low R_{DSon}). A trade-off between efficiency and input current quality has therefore to be accepted at selection of the switches.

In order to understand and describe the switching action of a MOSFET-diode combination a switching model of the power MOSFET is required. In **Fig. 5.2** the structure of a "conventional" high-voltage MOSFET is shown together with the structure of a SJ device. A low-doped n^- drift-zone, resulting in a wide depletion zone at blocking of the device, is used to achieve the required breakdown voltage for conventional HV-MOSFETs. The level of doping and the length of this n^- layer therefore depends on the breakdown voltage and as the full drain-source current has to flow through this layer also the on-state resistance of the device depends on the breakdown voltage which finally results in the relation given in (5.1). The structure of a HV-MOSFET results in a triangular electrical field distribution which is also depicted in **Fig. 5.2(a)**.

SJ devices, which are based on the idea of charge-balancing between

alternating n- and p-regions during the blocking state [141], have been introduced to further improve the on-state resistance of high voltage MOSFETs. As apparent in **Fig. 5.2(b)**, p-pillars are inserted which range deep into the n^- layer. The additional charge of the higher doped n-layer (used to reduce the on-state resistance) is balanced by the p-doped regions[1] and this yields a lateral electrical field component. If a blocking voltage is applied to the device the space charge region initially grows laterally along the p-n junction and at a relatively low blocking voltage, e.g. 50 V, the full area is depleted. In order to further increase the blocking voltage the depleted region acts like a pin-structure and only the vertical electrical field component is increased for higher blocking voltages resulting in an almost rectangular electrical field distribution. The SJ-structure has been analyzed in detail in [146] and the calculation shows, that the on-state resistance is only linearly dependent on the breakdown voltage

$$R_{\mathrm{DSon,SJ}} \propto V_{\mathrm{BR,SS}} \ . \tag{5.3}$$

The operating principle of SJ devices is based on a perfect charge compensation in the n- and p-pillars and as it is shown in [147] a charge imbalance would yield a reduced breakdown voltage $V_{\mathrm{BR,SS}}$. The fabrication of mostly charge compensated n- and p-pillars is hence the key to enable this technology. Detailed information on the device physics, implementation issues and behavior of SJ devices can be found in [148], [149] and [150].

A simplified equivalent circuit of a power MOSFET is shown in **Fig. 5.3(a)**, which is valid for frequencies up to several MHz. The capacitances C_{GS}, C_{GD} and C_{DS} are actually distributed over the active area of the device and are lumped to these single capacitors. In addition, the parasitic inductance of the source lead L_{S} is depicted. High di/dt-rates of the drain-source current induce a voltage that reduces the effective gate voltage in terms of a negative feedback. This parasitic inductance has a major impact on switching losses which will be discussed below. Whereas C_{GS} shows only minor variations with applied V_{DS} the capacitances C_{GD} and C_{DS} are strongly dependent on V_{DS}.
If a blocking voltage is applied to a HV-MOSFET a space charge region grows into the epi-layer n^- and this junction-depletion capacitance is

[1] As the additional charges in the n^--layer are compensated by the p-columns these devices are also called "charge-compensated devices".

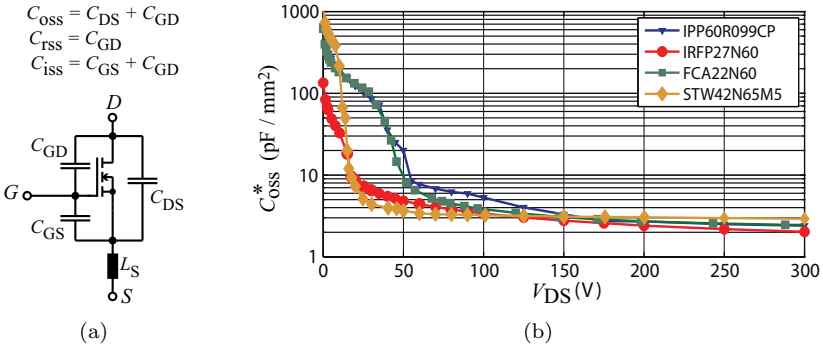


Fig. 5.3: (a) Equivalent circuit of a power MOSFET valid for frequencies up to several MHz. (b) Measured area specific output capacitance C^*_{oss} as a function of the applied blocking voltage V_{DS} of several SJ devices from different manufacturers compared to a HV-MOSFET (IRFP27N60).

modeled by the capacitance C_{DS}. It is directly proportional to the chip area A_{Chip} and shows for HV-MOSFETs the relation

$$C_{DS} \approx A_{Chip} \cdot C^*_{DS,0} \sqrt{\frac{V_{DS,0}}{V_{DS}}} \tag{5.4}$$

where $V_{DS,0}$ is the drain source voltage where $C^*_{DS,0}$ is measured (see also [151]). The voltage dependence of the gate-drain capacitance C_{GD} is very similar to C_{DS} even if it is not a junction-depletion capacitance but this is not discussed further here.
Fig. 5.3(b) shows the measured output capacitance per chip area $C^*_{oss} = C^*_{DS} + C^*_{GD}$ of a "conventional" HV-MOSFET (IRFP27N60) compared to the output capacitance of SJ devices of different manufacturers. The behavior given in (5.4) is obvious for the HV-MOSFET.

In SJ MOSFETs, the space charge region starts to grow along the p-n junctions of the inserted p-stripes if a blocking voltage is applied to the device which yields to a drastically increased internal surface of the pn-junction [152]. The output capacitance C_{oss} is consequently very large at low V_{DS} and (5.4) is not valid for these devices. At a relative low blocking voltage ($\approx 50\,V$) the depletion layers of the pn-junctions merge and at this point C_{oss} decreases abruptly. According to **Fig. 5.3(b)**, all SJ-devices show this effect and the devices from different manufacturers

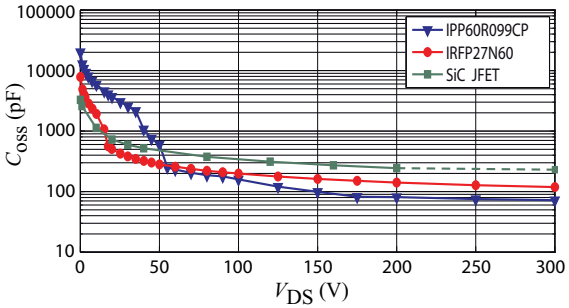


Fig. 5.4: Measured output capacitance C_{oss} of a HV-MOSFET (IRFP27N60), a SJ device (IPP60R099CP) and a SiC-JFET (1200 V/30 A, normally OFF) as a function of the applied blocking voltage V_{DS}.

only differ in the drain-source voltage where this abrupt decrease occurs.

In **Fig. 5.4**, the measured output capacitances C_{oss} of a SJ device (IPP60R099CP) and a HV-MOSFET (IRFP27N60) are plotted together with the output capacitance of a 1200 V/30 A normally-off SiC-JFET device (SJEP120R063). Specific parameter of the devices are listed in **TABLE 5.2**. The small chip area required for the SJ device yields to a small C_{oss} at V_{DS}=300 V. Due to the larger chip area, the HV-MOSFET shows a higher C_{oss} at V_{DS}=300 V but its capacitance only rises according to (5.4) and is much smaller than the C_{oss} of the SJ device for $V_{DS} < 50$ V. In comparison to the devices based on the Si-technology, the SiC JFET requires the smallest chip-area but shows the largest C_{oss} at 300 V. Only a rather small increase can, however, be observed at smaller drain-source voltages.

A boost-type test circuit is built (cf. **Fig. 5.5**) in order to analyze the switching behavior of different semiconductors. Next to the main elements of the boost circuit, switch S_1, boost diode D_1, boost inductor L_{boost} and output capacitor C_o also the dominant parasitics of the circuit are depicted. The inductances L_{wire} model the interconnections forming the commutation path, $C_{j,D}$ the parasitic junction capacitance of the boost diode and C_{oss} the nonlinear output capacitance of the MOSFET. The input capacitor C_{in} as well as C_o are partly implemented by ceramic and electrolytic capacitors in order to guarantee a low impedance path even at frequencies of 100 MHz and above.

TABLE 5.2: Parameters of the MOSFETs used for benchmarking.

	$V_{\mathrm{BR,SS}}$ (V)	A_{Chip} (mm^2)	C^*_{oss} ($\mathrm{pF/mm}^2$) (300 V)	R^*_{DSon} (Ω mm^2) (25 °C)	$(R_{\mathrm{DSon}}E_{400\mathrm{V}})^{-1}$ $(\Omega\mu\mathrm{J})^{-1}$ (FOM)	Q^*_{G} ($\mathrm{nC/mm}^2$) (15 V)	$E_{400\mathrm{V}}$ (μJ) (400 V)
IPP60R099CP	650	30	2.4	2.7	0.97	2.8	11.5
IPP60R165CP	650	20	2.4	2.7	0.85	2.8	7.5
SPW47N60C3	650	68	2.6	4.8	0.86	2.8	16.5
IRFP27N60	600	59	2	10.6	0.44	3.0	12.5
STW42N50M5	650	33	2.9	2.6	1.58	4.3	8
FCA22N60	600	19.5	2.45	3.2	0.81	3.89	7.5
DE475-501N44A	500	126	2.5	16.4	0.26	2.06	30
SiC JFET	1200	8	12.5	0.36	2.29	7.5[1)]	9.7
SiC MOSFET	1200	22.1	6.7	1.76	0.84	3.3	14.8

[1)] V_{G} =2.5 V.

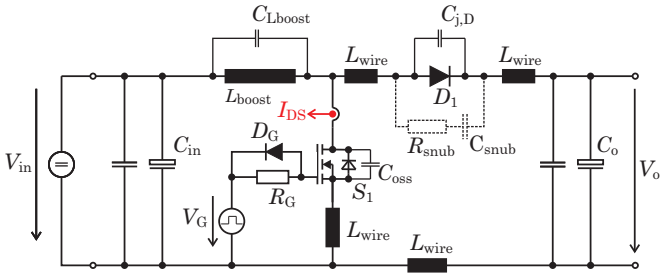


Fig. 5.5: Boost-type test circuit used to analyze the switching behavior of different MOSFETs. The test circuit is also used for determining the switching losses of different semiconductors.

Fig. 5.6: Constructed AC current transformer with a sensitivity of 100 mV/A to measure the drain source current I_{DS} of the MOSFET.

The MOSFET current I_{DS} is measured with a specifically designed AC-current probe based on a current transformer (cf. **Fig. 5.6**). The current transformer consists of a small toroid R6.3 of the material T38 of Epcos Inc. with a single layer winding ($N = 28$ turns). The output of the senor is terminated with a burden resistor of $R_{\mathrm{B}} = 3\,\Omega$. To minimize the influence of the measurement cable the input of the oscilloscope has to be set to $50\,\Omega$ which is the characteristic impedance of the applied coax cable. The characteristic impedance is in parallel to the burden resistance which results in a sensitivity of

$$S = \frac{R_{\mathrm{B}}}{N} = \frac{3\,\Omega // 50\,\Omega}{28\,\mathrm{turns}} = 100\,\mathrm{mV/A} \tag{5.5}$$

for the current sensor. The lower bandwidth limit of the sensor can be calculated using

$$f_{\mathrm{l}} = \frac{R_{\mathrm{B}}}{2\pi L_{\mathrm{m}}} = 225\,\mathrm{Hz} \tag{5.6}$$

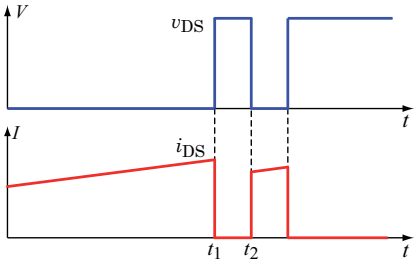


Fig. 5.7: Schematic voltage and current waveforms used to test the switching behavior of several semiconductors.

where L_m is the magnetizing inductance of the CT. The core is not driven into saturation if the pulsed current and/or i_m follows the relation

$$\int_0^t \frac{i_m}{N} R_B dt < N B_{max} A_{Fe} \ . \tag{5.7}$$

The performance of the constructed sensor has been compared to a 2 GHz shunt of T&M research [153] and shows very good results even for frequencies beyond 100 MHz. Due to its small size the CT can be plugged directly on the connection leads of a TO220 or TO247 package which minimizes distortions caused by the insertion of the current sensor in the commutation path.

A low impedance, high output current gate driver is used with gate voltages between 10 V and 18 V in conjunction with a gate resistor R_G. A diode is connected in parallel to the gate resistor to increase the turn-off speed of the device. The gate resistor is therefore only used for turn-on.

A test waveform as given in **Fig. 5.7** is applied for studying the switching behavior of the semiconductors. The switch S_1 is closed and the current in L_{boost} ramps up according to $V_{in} = L_{boost} di/dt$. At time instant t_1 the switch is turned-off and the current commutates from the switch S_1 to the boost diode D_1. The turn-off behavior can hence be studied at the corresponding current level. After a short interval, the switch S_1 is turned on again at t_2 and the turn-on behavior can be analyzed. Note, that the current amplitude is slightly reduced during the free-wheeling time ($t_1 < t < t_2$).

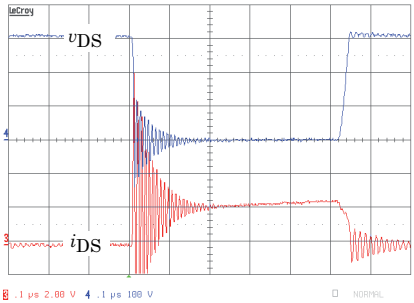


Fig. 5.8: Current and voltage wave forms at turn-on of S_1 at $I_{DS} = 20\,A$; v_{DS} : 100 V/Div, i_{DS} : 20 A/Div, time scale: 50 ns/Div.

5.1.1 Current and Voltage Switching Transients

Fig. 5.8 shows the measured voltage and current waveforms of the CoolMOS SPW47N60C3 (specifications are listed in **TABLE 5.2**) in combination with the SiC diode IDT10S60C. A gate voltage of 15 V and a gate resistor of 1 Ω is used. Unacceptable large current and voltage oscillations with a frequency of approximately 100 MHz are measured, especially at turn-on of the transistor. The origin of the undesired switching transient oscillations shall be described briefly in the following using the test circuit given in **Fig. 5.5**.

At turn-on of the MOSFET S_1 the converter's input current has to commutate from diode D_1 to MOSFET S_1. As SiC-Schottky diodes are used, there is no reverse recovery current I_{rr}. A displacement current is, however, charging the voltage dependent junction capacitance $C_{j,D}$ of D_1. This capacitance in connection with the wiring inductance L_{wire} forms a series resonant circuit which is only damped by the on-state resistance R_{DSon} of S_1 and by the high-frequency resistance of the wiring.

At turn-off of S_1, the input current has to commutate from MOSFET S_1 to diode D_1 and now the voltage dependent output capacitance C_{oss} of the MOSFET forms a weakly damped series resonant circuit with the wiring inductance L_{wire} of the PCB. In [154], the turn-off behavior of the MOSFET is analyzed and an analytical expression for the turn-off switching transient overvoltage is given.

The unwanted ringing can basically be reduced by application of snubber circuits (a survey of snubber circuits can be found in [155] and [142]). An easy RC snubber for the boost diode is often used in power electronics to damp unwanted oscillations (resulting mainly from the reverse recovery for Si-diodes). The losses of such a snubber circuit would, unfortunately, be far too high for a switching frequency in the MHz-range which will be discussed in greater detail below. Ferrite beads [156] or amorphous magnetic materials [157] can be used alternatively at low current levels to limit the di/dt-rate at turn-off of the boost diode, but these magnetic devices are not applicable at higher current levels due to their limited power dissipation capability. Various diode recovery suppression circuits have furthermore been developed [158], but these circuits are also not very well suited for switching frequencies in the MHz range. Specific interconnection concepts with low-pass characteristics based on high-ϵ-materials have been analyzed [159, 160] but these approaches are only applicable in case of longer interconnection distances to achieve the desired damping behavior.

The application of a GaAs diode, e.g. DGSS 10-06CC [161] which intrinsically shows a smaller parasitic capacitance as the SiC diode, only moves the resonance to a higher frequency region and does not solve the problem. This was also verified by measurements. The mentioned GaAs diode, however, implements the 600 V breakdown voltage capability by a series connection of two diodes in a single package. Next to the unclear voltage distribution of the devices, the two series connected diodes show a much higher forward voltage drop which results in higher conduction losses. GaAs-diodes are therefore not very well suited to solve this problem.

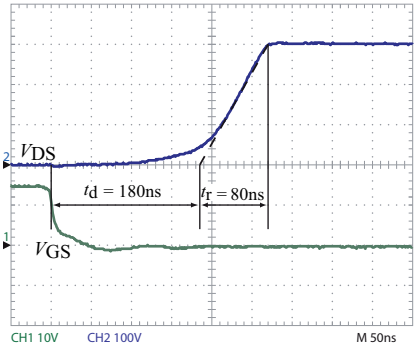
Active control of the switching transients, as known from IGBT gate drive circuit research [162, 163, 164] would be an enhanced method for reducing the oscillations. This active control, to be implemented into the gate drive stage of the MOSFET, would require a reasonably high control gain in the frequency region of the oscillations to be damped (e.g., typ. 100 MHz for state-of-the-art power MOSFETs) or a large control loop bandwidth or both, and is therefore no option at present for a discrete implementation.

In section 5.2 a magnetically coupled damping layer will be discussed in detail. This promising approach shows good results and less losses compared to a classical snubber circuit. The limited coupling of the damping layer and the wiring layer, however, limits its performance.

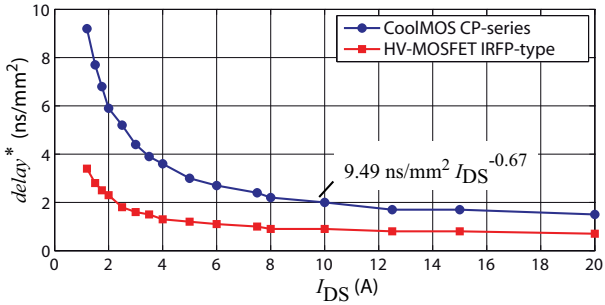
The PCB inductance of the commutation path can be minimized using a proper PCB layout. The final construction and especially the PCB layout of the commutation path is therefore essential for limited oscillations. A small residual value of L_{wire} will, however, remain. The only applicable way to reduce or prevent these oscillations is therefore to lower the switching speed of the device by increasing the gate resistor. On the other hand, this considerably increases switching losses. The adaption of the gate resistor must therefore be performed very carefully at the final constructed hardware to find a trade-off between sufficiently damped oscillations and limited switching losses.

5.1.2 Turn-Off Delay of MOSFET

In the intended PFC-application, C_{oss} has to be charged by the input current at turn-off of the MOSFET and the voltage-rise of V_{DS} is hence dependent on the input current. **Fig. 5.9(a)** shows the measured turn-off behavior of the MOSFET IPP60R099CP for an input current of 1.3 A and a drain source voltage of 300 V. The total turn-off delay can be separated into a pure delay time t_{d}, where the large C_{oss} for $V_{\mathrm{DS}} < 50\,\mathrm{V}$ is charged (see also **Fig. 5.3(b)** and **Fig. 5.4**), and in a rise time t_{r}. This current dependent turn-off delay distorts the intended pulse pattern in terms of extended on-times and its influence increases with increased switching frequency.
The drain source current dependent turn-off delays of several SJ devices of the CoolMOS CP-series (Infineon Inc., e.g. IPP60R099CP) and HV-MOSFETs (Vishay Siliconix Inc., e.g. IRFP27N60) have been measured. As C_{oss} scales approximately linearly with the chip area A_{Chip} also the turn off delay scales linearly with A_{Chip}. Using the specific chip areas of the devices (cf. **TABLE 5.2**) the chip area specific turn-off delays of the two semiconductor families can be calculated. The results are plotted in **Fig. 5.9(b)**. In general, the SJ-devices show a higher chip-area specific turn-off delay than the HV-MOSFET devices. The SJ-devices show in addition a comparatively pronounced increase of turn-off delay at smaller I_{DS}. According to [151], C_{oss} shows only minor



(a)



(b)

Fig. 5.9: (a) Measured inductive turn-off switching characteristic of the SJ device IPP60R099CP at a drain source current of 1.3 A and an output voltage of 300 V using a gate resistance of $R_G = 7.5\,\Omega$ and a gate voltage of $V_G = 14$ V; (b) Measured chip area dependent turn-off delay of the CoolMOS CP-series and the HV-MOSFET IRFP-type as a function of I_{DS}.

dependence on temperature and hence the turn-off delay can be modeled without consideration of the temperature which has been confirmed by measurements. The measured turn-off delays can be fitted by

$$delay \approx A_{Chip}\ del^* \left(\frac{I_{DS}}{[A]}\right)^{\alpha} \tag{5.8}$$

using the least square method where del^* and α are the variable parameters, I_{DS} is the drain source current at turn-off, A_{Chip} the chip area of the device and $[A]$ indicates that the current I_{DS} is in Ampere. This

TABLE 5.3: Parameters used to approximate the turn-off delays by (5.8).

Semiconductor family	del^*	α
CoolMOS CP-series	$9.49\,\mathrm{ns/mm^2}$	-0.67
IPP60R099CP	$284\,\mathrm{ns}\,(I_{\mathrm{DS}})^{-0.67}$	
HV-MOSFET IRFP-type	$3.64\,\mathrm{ns/mm^2}$	-0.54
IRFP27N60	$214\,\mathrm{ns}\,(I_{\mathrm{DS}})^{-0.54}$	

approximation will be used in the next section to determine the resulting input current distortions. The corresponding parameters (del^* and α) for the two semiconductor families are listed in TABLE 5.3.

Evaluation of Input Current Distortions

In the following the effects of this duty cycle distortion on the input current quality will be analyzed. The required duty cycle $\delta_i \in [0 \ldots 1]$ of phase number i of the rectifier system is given by

$$\delta_i(\varphi_{\mathrm{N}}) = 1 - M \left| \cos\left(\varphi_{\mathrm{N}} - \frac{2\pi}{3}(i-1)\right)\right| \quad i \in 1,2,3 \tag{5.9}$$

(see also section 3.1) where for the sake of simplicity the possible third-harmonic injection is not included. This duty cycle is calculated by the controller and the generated pulse patterns of (5.9) are, dependent on the input current, enlarged by the turn-off delay of the MOSFET (cf. **Fig. 5.9(b)**). Note, that the duty cycle is limited to 1 (MOSFET is permanently on). In **Fig. 5.10** the required duty cycle (Ref.) of switch S_1 is plotted for an output power of P_{o}=5 kW and a modulation index $M = 0.813$ in conjunction with the grid voltages. As a unity power factor shall be achieved by the rectifier system, the input currents are assumed to be in phase with the input voltages and are therefore not shown. The required duty cycle is plotted together with the resulting duty cycle considering the turn-off delay for the SJ device IPP60R099CP and additionally the deviation is depicted. The biggest deviations can be observed in the vicinity of the phase-voltage zero-crossings where the duty cycle is near 100 %. It is also apparent, that small duty cycles (turn-on times smaller than the turn-off delay)

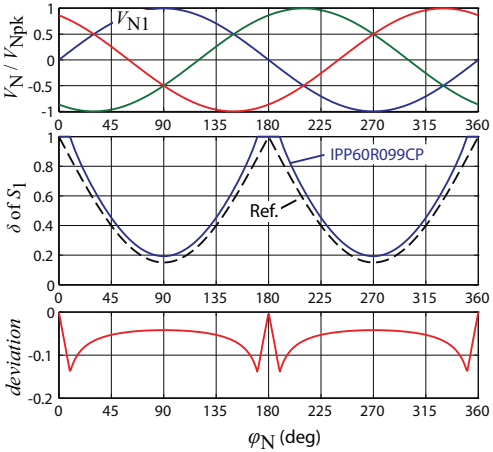


Fig. 5.10: Required duty cycle of switch S_1 and effective duty cycle due to the turn-off delay of the MOSFET for a modulation index of $M = 0.813$ ($V_N = 230\,V$ and $V_o = 800\,V$) and a switching frequency of 1 MHz and P_o =5 kW.

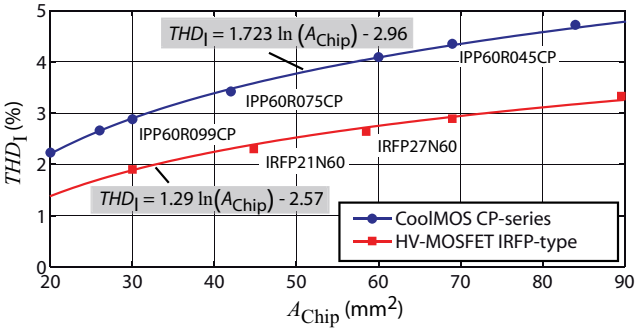


Fig. 5.11: Simulated THD_I of the input currents as a function of chip area A_{Chip} for a 10 kW VR system with a switching frequency of 1 MHz ($f_N = 50\,Hz$, $V_N = 230\,V$, $V_o = 800\,V$).

cannot be implemented.

The measured delays given in **Fig. 5.9** are subsequently used in a computer simulation to determine the resulting input current distortions. This is not easily possible in an analytical manner as the current controller is partially able to compensate this error. The current

controller is designed according to [165] and for evaluation of the input current distortions the THD_I-value of the input current is calculated. The results of this calculation are plotted in **Fig. 5.11** for a switching frequency of 1 MHz ($V_N = 230\,V$, $V_o = 800\,V$, $P_o = 10\,kW$) where the resulting THD_I value is given as a function of the chip area A_{Chip}. The calculated THD_I-value here takes only the current distortions caused by the turn-off delay into account and serves as a good comparison diagram. A practical implemented system, however, will show higher THD_I-values as other effects such as cusp distortion or DCM operation will also take effect.

A curve fitting is used to approximate the delays for further calculations and the corresponding functions are given in **Fig. 5.11** for the two semiconductor families. Consistent with **Fig. 5.9**, the HV-MOSFET shows a better chip area dependent input current quality but a larger turn-off delay for a device with equal R_{DSon}. The chip area dependent input current quality $THD_I(A_{Chip})$ will be combined in section 5.4.3 with the calculated efficiency $\eta(A_{Chip})$ (cf. **Fig. 5.49**) which finally results in the η-THD_I-Pareto Front.

The simulated results are plotted in **Fig. 5.12(a)** as a function of chip area A_{Chip} and switching frequency f_s for the CoolMOS CP-series. In **Fig. 5.12(b)** the input current distortions are given for different CoolMOS CP devices as a function of f_s and the corresponding specifications of the devices are listed in **TABLE 5.2**. It is obvious that the input current distortions rise with higher switching frequency. The input current distortions are smaller than 2.5 % for all semiconductors, if a switching frequency below 250 kHz is used. If, however, for instance a switching frequency of 1 MHz shall be applied, only the devices IPP60R165CP and IPP60R099 will show input current distortions near 2.5 %.
In **Fig. 5.11** and **Fig. 5.12**, the input current distortions are plotted for an output power of 10 kW. Considerably increased input current distortions, however, occur at operation with partial load as the current to charge C_{oss} gets smaller. Also a higher mains frequency, e.g. 400 Hz, results in increased input current distortions. **Fig. 5.13** shows the simulated 5 kW THD_I value as a function of f_s for a mains frequency of $f_N = 400\,Hz$.

As expected, an increased THD_I value can be observed at partial load. A device with a preferable small chip size, which consequently shows a smaller output capacitance C_{oss} and smaller turn-off delay, must

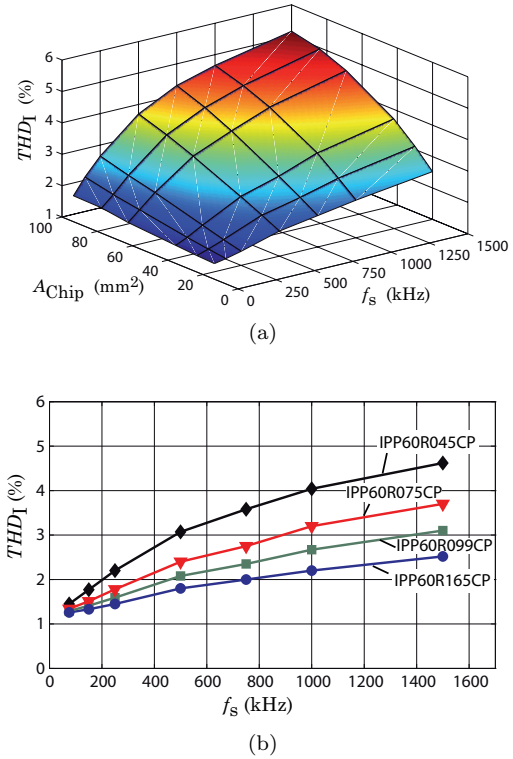
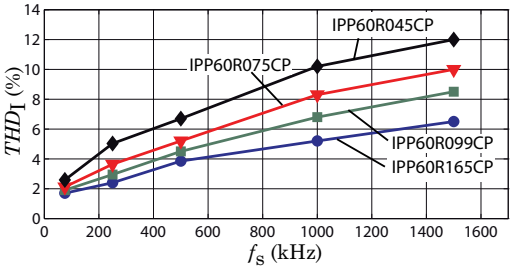


Fig. 5.12: (a) Simulated $\mathrm{THD_I}$ of the input currents a function of chip area A_{Chip} and switching frequency f_{s} for the CoolMOS CP-series. (b) Simulated $\mathrm{THD_I}$ as a function of switching frequency f_{s} for different CoolMOS-CP devices ($f_{\mathrm{N}} = 50\,\mathrm{Hz}$, $V_{\mathrm{N}} = 230\,\mathrm{V}$, $V_{\mathrm{o}} = 800\,\mathrm{V}$).

therefore be used for a high-frequency implementation, especially if a high input current quality at partial load is required.

Feed-Forward Compensation of the Delay

The input current distortions caused by the turn-off delay of the MOSFET can be reduced considerably, if a feed-forward compensation is implemented. The input current dependent turn-off delay $\delta_{i,\mathrm{pre}}$ given in (5.8) can thereto be added to the current controller output $\delta_{i,\mathrm{contr}}$ in terms of a pre-control signal



(a)

Fig. 5.13: Simulated $\mathrm{THD_I}$ of the input currents as a function of switching frequency f_s at half output power $P_\mathrm{o} = 5\,\mathrm{kW}$ and $f_\mathrm{N} = 400\,\mathrm{Hz}$ ($V_\mathrm{N} = 230\,\mathrm{V}$, $V_\mathrm{o} = 800\,\mathrm{V}$).

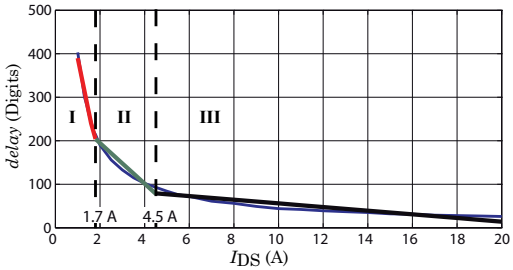


Fig. 5.14: Approximation of the turn-off delay of the switch IPP60R165CP by piecewise linear functions for digital pre-control implementation. The delay is plotted in digits where a value of 1024 (10 bit) relates to a full switching period ($f_\mathrm{s} = 1\,\mathrm{MHz}$).

TABLE 5.4: Piecewise linear functions used to approximate turn-off delay of the CoolMOS device IPP60R165CP plotted in **Fig. 5.14**.

I	$I_\mathrm{DS} < 1.7\,\mathrm{A}$	$640\,\mathrm{digits} - 250\,\mathrm{digits/A}\ I_\mathrm{DS}$
II	$1.7\,\mathrm{A} < I_\mathrm{DS} < 4.5\,\mathrm{A}$	$288\,\mathrm{digits} - 47\,\mathrm{digits/A}\ I_\mathrm{DS}$
III	$4.5\,\mathrm{A} < I_\mathrm{DS}$	$98\,\mathrm{digits} - 4\,\mathrm{digits/A}\ I_\mathrm{DS}$

$$\delta_{i,\mathrm{eff}}(\varphi_\mathrm{N}) = \delta_{i,\mathrm{contr}}(\varphi_\mathrm{N}) - \delta_{i,\mathrm{pre}}(\varphi_\mathrm{N})\ . \tag{5.10}$$

In the practical implementation the input current dependent pre-

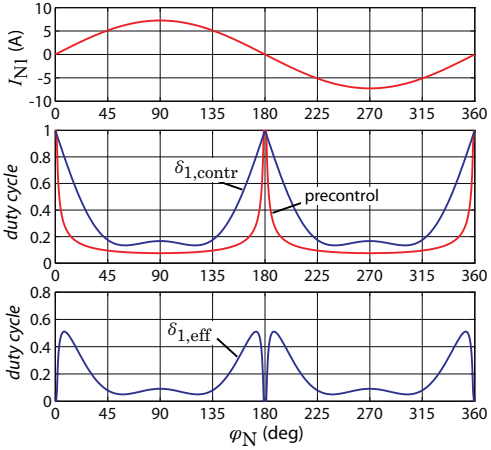


Fig. 5.15: Required duty cycle $\delta_{1,\mathrm{contr}}$ generated from the current controller and pre-control signal used to compensate the turn-off delays of the MOSFET leading to the resulting effective duty cycle $\delta_{1,\mathrm{eff}}$.

control signal can be added to the modulation function (see also section 3.1.2). The modulation function given in (3.54) can be extended by the pre-control which yields to

$$m_{i,\mathrm{tri}}(\varphi_\mathrm{N}) = M\left|\left(\cos\left(\varphi_\mathrm{N} - \frac{2\pi}{3}(i-1)\right) + \frac{1}{4}\mathrm{tri}\,(3\varphi_\mathrm{N})\right) + v_0 - i_\mathrm{FF}\right|, \tag{5.11}$$

where i_FF is the input current dependent pre-control signal according to (5.10) and (5.8). The value of this pre-control has to be adapted according to the modulation function and the switching frequency. As the calculation of the pre-control signal according to (5.8) is a time-consuming task in a digital controller implementation (e.g. DSP, FPGA, etc.,), it can be approximated by piecewise linear functions as shown in **Fig. 5.14** for the CoolMOS device IPP60R165CP. The delay is given in digits where a value of 1024 (10 bit) relates to a full switching period ($f_\mathrm{s} = 1\,\mathrm{MHz}$). Three piecewise linear functions are used and the interval boundaries are set to 1.7 A and 4.5 A respectively. The resulting approximations are listed in **TABLE 5.4** which can easily be implemented in an FPGA.

Fig. 5.15 shows the required duty cycle $\delta_{1,\mathrm{contr}}$ to generate sinusoidal input currents. This duty cycle is generated by the current controller and a third harmonic injection is included which is used to increase the input voltage range. In addition, the necessary pre-control signal used to compensate the turn-off delay and the resulting effective duty cycle $\delta_{1,\mathrm{eff}}$ is plotted. The greatest influence of the pre-control signal can be observed in the vicinity of the input current zero-crossings, where the duty cycle $\delta_{1,\mathrm{contr}}$ is almost unity. The duty cycle there has to be reduced considerably as the input current, which charges the output capacitance C_{oss}, is small and enlarges the pulse width. According to **Fig. 5.15** the duty cycle distortion can be compensated over long periods but, dependent on the applied MOSFET, a minimum pulse-length of 100 ns–200 ns is required to fully turn-on the MOSFET which limits the effectiveness of the proposed feed-forward compensation signal. The pre-control signal also only compensates the signal distortions caused by the turn-off delays of the MOSFETs. As a result, zero crossing distortions caused e.g. by the cusp-effect[2] or by small phase differences between input voltage and input current, which could occur in the intended aircraft application, will remain.

In order to verify the effectiveness of the proposed pre-control signal the rectifier system VR250 with a switching frequency of 250 kHz is used (cf. section 7.2). The measurement results of this system operating at $f_{\mathrm{N}} = 400\,\mathrm{Hz}$ and $P_{\mathrm{o}} = 4.7\,\mathrm{kW}$ with and without the pre-control signal are given in **Fig. 5.16**. Whereas the system without the pre-control shows significant input current distortions at the zero-crossings of the measured phase and at the zero-crossings of the two other phases (every 60 °) the input current quality is improved considerably if the pre-control is enabled. A $\mathrm{THD_I}$ of 3.4 % is measured without the feed-forward signal which can be reduced to 1 % if the proposed pre-control is applied. The measurement clearly illustrates that the turn-off delay causes significant input current distortions even for a "moderate" switching frequency of 250 kHz.

Simulation of the resulting input current distortions is a delicate task

[2] Cusp distortions occur after the mains voltage has crossed zero where the mains voltage and therefore the resulting voltage across the inductor is too small to program the required current slew rate. A deviation of the input current occurs during this time (see also [166, 167]).

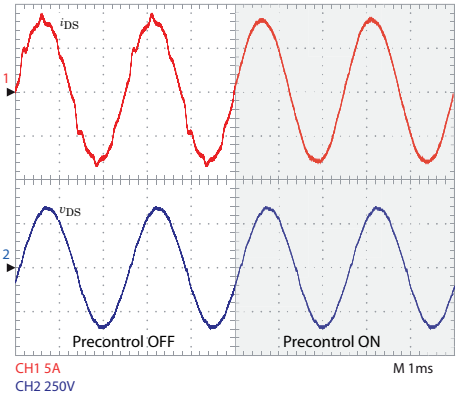


Fig. 5.16: Measurement of the input current of the rectifier system VR250 operated with and without feed-forward compensation of the turn-off delay. The rectifier system operates with $f_s = 250\,\text{kHz}$ (V_N=230 V, $f_N = 400\,\text{Hz}$, $V_o = 800\,\text{V}$, $P_o = 4.7\,\text{kW}$); Ch1 (red): I_{N1}, 5 A/Div, CH2 (blue): V_{N1}, 250 V/Div, time scale: 1 ms/Div.

if a given pre-control signal is applied. The pre-control signal is only an approximation and due to component variations the pre-control signal may not fully compensate the delay. A deviation of 10 %, the applied pre-control signal is assumed to be 10 % smaller then the required pre-control signal and therefore only compensates 90 % of the turn-off delay, seems to be a practical value and is therefore assumed for simulation of the resulting THD_I including a pre-control signal. The simulation results of the input current distortions with pre-control signal have to be regarded with suspicion. They can, however, be used to benchmark different semiconductor technologies if equal deviations are used.

Fig. 5.17 shows the simulated THD_I values of the 10 kW rectifier system if a pre-control with an error of 10 % is applied. Whereas a negligible dependency of the input current distortion can be observed for $P_o = 10\,\text{kW}$, still a pronounced chip area dependent input current distortion is present for $P_o = 5\,\text{kW}$. This verifies, that a device with preferably small chip area A_{Chip} shall be applied if a high input current quality at partial load operation is required. The distortions at $P_o = 10\,\text{kW}$ and $P_o = 5\,\text{kW}$ are almost equal at small chip sizes (e.g. $A_{\text{Chip}} = 20\,\text{mm}^2$) which is a result of the smaller turn-off delays at

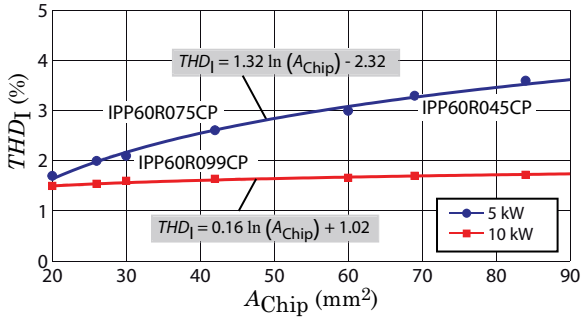


Fig. 5.17: Simulated $\mathrm{THD_I}$ of the input currents as a function of chip area A_{Chip} for a 10 kW rectifier system with a switching frequency of 1 MHz using a proper pre-control signal ($f_{\mathrm{N}} = 50\,\mathrm{Hz}$, $V_{\mathrm{N}} = 230\,\mathrm{V}$, $V_{\mathrm{o}} = 800\,\mathrm{V}$). Only devices of the CoolMOS CP-series are considered and an error of 10 % is assumed for the pre-control signal.

smaller chip areas - the current controller is almost able to compensate the turn-off delay. It has, however, to be mentioned here that such small chip sizes cannot be applied for a 10 kW rectifier system due to the excessive conduction losses (cf. section 5.3.2). According to the presented simulations, the CoolMOS device IPP60R099CP seems to be an ideal candidate for a switching frequency of 1 MHz.

5.1.3 Switching Loss Measurement

The determination of switching losses is a relatively complex task. Several research groups developed models for switching loss calculation [168, 169] but the most accurate approach still seems to be a to measurement of the switching losses of the MOSFET/diode combination of interest. Due to the intended very high switching frequency the SiC-diode IDT10S60 is selected. It is well known that SiC-diodes show no reverse recovery current but a capacitive displacement current is flowing if a blocking voltage is applied.
Switching losses are usually separated into turn-on losses and turn-off losses. Turn-on losses can be determined by a voltage/current measurement according to [170]. The drain source current I_{DS} charges the nonlinear capacitance C_{oss} at turn-off and causes therefore no turn-off losses. According to [171], the energy stored in C_{oss}, however, considerably contributes to the turn-on losses as C_{oss} has to be

discharged through the channel of the MOSFET at turn-on. These losses are not covered by the switching loss measurement at turn-on but can be calculated using the stored energy in the parasitic capacitance C_{oss} of the MOSFET. The calculated stored energies at $V_{\mathrm{DS}}400\,\mathrm{V}$ $E_{400\mathrm{V}}$ are listed in TABLE 5.2. Alternatively to the values given in the data-sheet the energy stored in the output capacity of the MOSFET can be measured at turn-off of the device. The total switching losses can therefore be determined by measuring the voltage and current transients at turn-on/turn-off the MOSFET diode combination.

The boost-type test circuit given in **Fig. 5.5** is used to determine the turn-on losses and the MOSFETs are gated with the test pulse shown in **Fig. 5.7**. The switching losses are mainly determined by the switching speed of the devices (with the exception of capacitive contributions) and, as already discussed, the switching speed is limited by the transient voltage and current oscillations. The gate resistor is therefore increased to a value which results in a fast transition without significant oscillations. In order to give a fair comparison of different semiconductor families the switching transients (v_{DS} and i_{DS}) of the SJ device IPP60R099CP are used as reference. The gate-resistors are modified for other MOSFETs until the switching transients roughly match with this reference. The devices will then show approximately equal turn-on losses independent of A_{Chip}. This is, however, only possible for devices showing chip areas in the same order of magnitude. The comparably fast switching transient reference may not be achieved for a device with a considerably larger chip area. The internal gate-resistor of a MOSFET and the negative feedback behavior of the parasitic source inductance L_{S} may inhibit such a fast transient. In this work only MOSFET devices are considered that are able to achieve the selected switching transient reference.

Fig. 5.18 shows the turn-on voltage and current transients of a CoolMOS device (IPP60R099CP) at $I_{\mathrm{DS}} = 5\,\mathrm{A}$ and $V_{\mathrm{DS}} = 400\,\mathrm{V}$ using a gate resistance of $R_{\mathrm{G}} = 7.5\,\Omega$ and a gate voltage of $V_{\mathrm{G}} = 14\,\mathrm{V}$. The switching action takes about 10 ns and a current overshoot up to 15 A can be measured which is mainly caused by the mentioned capacitive displacement current of the SiC diode. Channel A (green curve) corresponds to the instantaneous power $v_{\mathrm{DS}} \times i_{\mathrm{DS}}$ and its area is equivalent to the turn-on switching loss energy E_{on}. Different MOSFET/diode combinations may

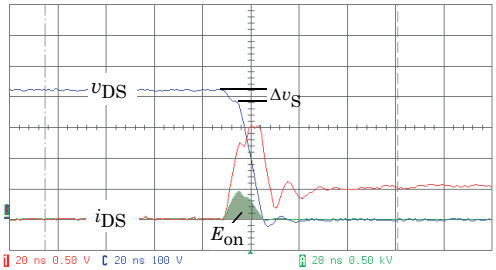


Fig. 5.18: Measured MOSFET turn-on switching transient at $I_{DS} = 5\,A$ and $V_{DS} = 400\,V$ for $R_G = 7.5\,\Omega$ and $V_G = 14\,V$. CH1: i_{DS} (5 A/Div), CHC: v_{DS} (100 V/Div), CHA: $p(t) = v_{DS}(t) \times i_{DS}(t)$, time scale: 20 ns/Div.

show different switching transients. The reverse recovery current of the diode is for instance be much higher if a Si diode is used instead of the SiC-diode.
MOSFET devices of different vendors differ in the gate threshold voltage $V_{G(th)}$ and transconductance g_m and the transconductance g_m defines the turn-on slew rate of I_{DS}. The threshold voltage as well as g_m are further dependent on the junction temperature T_j and as the parasitic capacitances of the MOSFET devices show no temperature dependence these two elements are responsible for the slight temperature dependence of the turn-on switching loss energies.
The high di/dt-rate of I_{DS} causes a voltage drop in v_{DS} due to the wiring inductance of the commutation path $\Delta v = L_{wire}\, di_{DS}/dt$ (cf. **Fig. 5.18**) which can be used to determine the total parasitic inductance of the wiring path. On the other hand, the MOSFET device shows a source inductance L_S (cf. **Fig. 5.3(a)**). High di/dt rates induce a voltage

$$\Delta v_S = L_S \frac{di_{DS}}{dt} \tag{5.12}$$

which reduces the effective gate voltage of the MOSFET in terms of a negative feedback and limits the switching speed of the device. An optimized gate drive loop showing a small loop inductance is therefore essential for high switching speeds.
The slew rate of the falling drain source voltage is defined by the Miller capacitance of the MOSFET C_{GD} and the maximum gate-drive current.

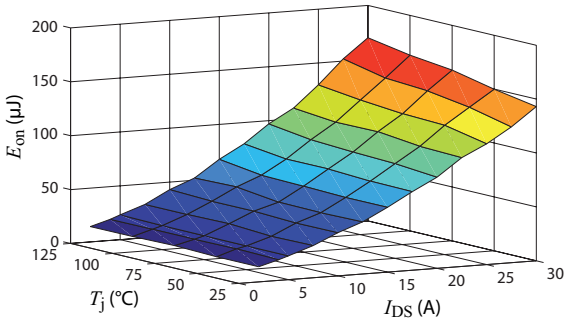


Fig. 5.19: Measured turn-on energies of the CoolMOS-CP semiconductor series as a function of I_{DS} and junction temperature T_j at $V_{DS} = 400\,V$.

As the charging current

$$i_G = C_{GD}\frac{dv_{DS}}{dt} = \frac{V_G - V_{GS(th)}}{R_G} \tag{5.13}$$

is defined by V_G and R_G a low enough gate resistance R_G and high gate voltage V_G are required for low switching losses where R_G is the lumped resistance consisting of the internal resistance of the gate-drive stage, the internal parasitic gate resistance of the MOSFET and the external applied gate resistor. Omitting an external gate resistor therefore does not result in $R_G \approx 0$.

The approved test circuit is now used to measure the switching loss energies $E_{on}(\Delta T, I_{DS})$ of the CoolMOS CP series as a function of I_{DS} and the junction temperature ($\Delta T = T_j - 25\,°C$) and the results are given in **Fig. 5.19**.

The measured turn-on switching energy curves for an output voltage of 400 V can be fitted by

$$E_{on}(\Delta T, I_{DS}) = \left(k_0 + k_1 I_{DS} + k_2 I_{DS}^2\right)\left(1 + (\gamma I_{DS})\Delta T\right) \tag{5.14}$$

for further loss calculations and the parameters of this curve fitting are listed in **TABLE 5.5**.

TABLE 5.5: Parameters of (5.14) for approximation of the turn-on energies of the CoolMOS CP series given in **Fig. 5.19**.

k_0	$7.85\,\mu J$	k_1	$2.53\,\mu J/A$
k_2	$0.066\,\mu J/A^2$	γ	$80E^{-6}\,K^{-1}$

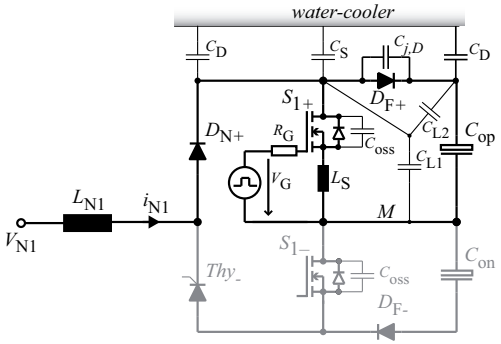


Fig. 5.20: Simplified model of the commutation path of switch S_{1+} of the constructed VR1000 VR system (cf. section 5.8) including main parasitic capacitances.

5.1.4 Influence of Hardware Construction

Initial efficiency measurements on the final constructed hardware (cf. section 5.8) showed that the total semiconductor losses are much higher than calculated and the origin was found in considerably larger switching losses. The optimized boost-type test circuit given in **Fig. 5.5** is used to determine the turn-on switching energies plotted in **Fig. 5.19** and this test circuit shows very small parasitic capacitances.

A more comprehensive model of the commutation path for the switch S_{1+} considering main parasitic capacitances is given in **Fig. 5.20**. All semiconductors are mounted on a heat sink implemented using a water cooler and the parasitic capacitances to the heat sink (C_D and C_S) are added to the model. Next to the junction capacitance $C_{j,D}$ of the SiC diode also parasitic capacitances of the layout C_{L1} and C_{L2} have to be included. All parasitic capacitances connected to the drain of the MOSFET have to be charged/discharged in every switching cycle

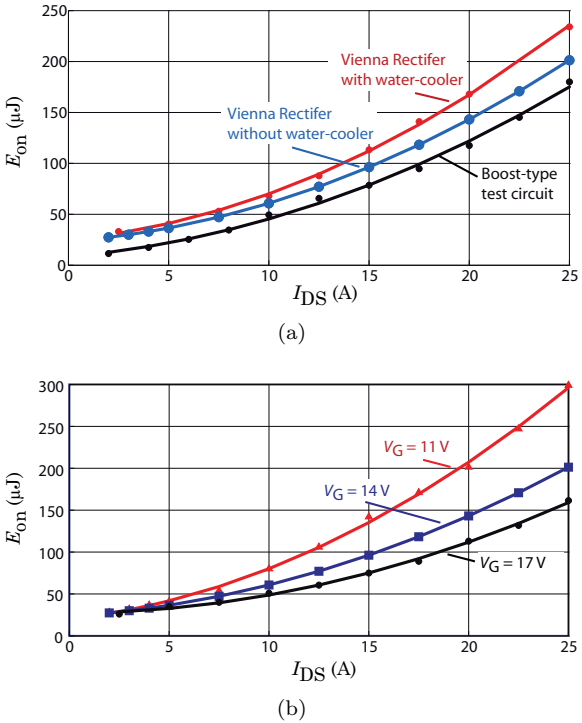


Fig. 5.21: Turn-on switching loss energies measured on the constructed VR1000 prototype employing the switch IPP60R125CP. (a) Influence of the unfavorable PCB layout and water cooler on the loss energies for $V_G = 14\,V$ and (b) switching energies (without water cooler) for different gate voltages V_G.

and accordingly increase switching losses. Due to an unfavorable layout error of the constructed hardware the parasitic layout capacitances C_{L1} and C_{L2} show values above 100 pF which finally results in the high switching losses.

The measured switching loss energies of the boost-type test circuit are compared in **Fig. 5.21(a)** with measured energies taken from the VR1000 prototype employing the CoolMOS device IPP60R125CP. On one hand, higher switching loss energies are measured due to the unfavorable PCB layout and on the other hand the turn-on energies are further increased if the water cooler is attached. The influence of

the gate-drive voltage on switching losses is depicted in **Fig. 5.21(b)** where an increase of the switching loss energy with higher drain source current can be observed. As for a reduced gate voltage of $V_G = 11\,V$ increased turn-on energies can occur, the switching loss energies could be reduced if V_G is increased from 14 V to 17 V. The higher gate voltage, however, results in a higher gate drive power requirement which may be relevant for switching frequencies in the MHz range.

The measurements in **Fig. 5.21** impressively illustrate that switching losses are considerably affected by the final hardware setup like the PCB layout and that also the heat sink plays an important role. Switching losses must therefore be measured on the final constructed prototype for precise modeling. The boost-type test circuit can, however, be used to benchmark different semiconductor technologies or to get a rough idea of switching losses in an early development state.

5.1.5 Selection of Switching Frequency

In the previous sections several limitations of high switching frequencies have been discussed. The switching speed of the MOSFETs is limited due to parasitic capacitances and inductances of the commutation path and of the devices. This yields to high switching losses if the switching frequency is increased. Next to the high switching losses also turn-off delays occur which yield to input current distortions. Based on the derived results of the previous sections a switching frequency of 1 MHz is chosen for implementation of the high power density 10 kW VR system. In the following an approach to damp the unwanted current and voltage switching transients is presented, followed by a detailed power loss and efficiency calculation of the intended rectifier system for a switching frequency of 1 MHz. The finally constructed hardware prototype is discussed in section 5.8.

5.2 Magnetically Coupled Damping Layer

In this chapter a novel approach to attenuate the unwanted switching transient oscillations, which occurred in section 5.1.1 as a result of the very high switching speed, is discussed. The approach uses a novel magnetically coupled damping layer which was initially introduced in [172]

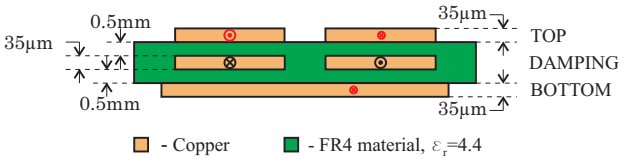


Fig. 5.22: Layer stack of the proposed magnetically coupled damping layer.

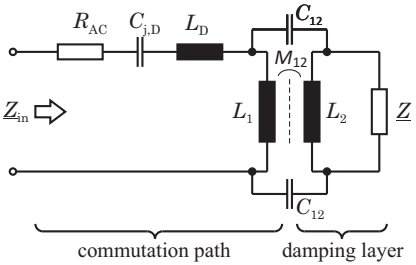


Fig. 5.23: Model of the test circuit with damping layer at turn-on of the MOSFET.

and further analyzed in [173]. An additional layer is thereto inserted between the two wiring layers (cf. **Fig. 5.22**). If the copper path of the damping layer winding is terminated by an appropriately designed RC network, the currents induced in the damping layer will significantly reduce the parasitic oscillations in the wiring layers. An optimized termination network results in a very good damping behavior and significantly lower losses compared to a classical snubber circuit. The damping network uses standard materials (FR4, copper) and no extra manufacturing processes are needed, which leads to low implementation costs.

5.2.1 Analysis of the Damping Layer

In the following only the behavior of the circuit at turn-on of the MOSFET is analyzed. The turn-off behavior can, however, be treated in a similar way.

A simple model for the turn-on behavior of the MOSFET including the damping layer is shown in **Fig. 5.23** where the following symbols are used:

- R_{AC} HF-resistance of the wiring in the commutation path;

- $C_{\mathrm{j,D}}$ Junction capacitance of the SiC-Schottky diode;
- L_{D} Parasitic inductance of diode and MOSFET;
- L_1 Effective inductance of the commutation path;
- L_2 Inductance of the damping layer;
- M_{12} Mutual inductance between commutation path and damping layer;
- C_{12} Coupling capacitances between wiring layer and damping layer;
- $\underline{Z}$ Termination network for damping layer.

Although the inductance of the commutation path can be minimized using a proper layout, a small residual value will remain. An excellent PCB layout offers stray inductances in the range of the parasitic inductances of the diode and the MOSFET packages. The component parasitics must therefore be added to the model. Due to skin effect, the current of the high-frequency oscillations flows only in a thin layer at the surface of the copper layer and so the HF-resistance R_{AC} has to be used. The skin effect additionally reduces the effective area of the copper wires which reduces the high-frequency coupling capacitance C_{12} to small values so that it can be neglected in a first approximation for sake of an easier model. The parasitic capacitance C_{Lboost} of the boost inductor can furthermore be neglected as the analyzed oscillations at turn-on of T_1 are not directly affected by C_{Lboost}. The natural frequency f_0 and characteristic impedance Z_0 of the LC-tank at turn-on are

$$f_0 = \frac{1}{2\pi\sqrt{L_{\mathrm{wire}} C_{\mathrm{j,D}}}} \ , \quad Z_0 = \sqrt{\frac{L_{\mathrm{wire}}}{C_{\mathrm{j,D}}}} \ . \tag{5.15}$$

The resonance frequency f_0 lies in the 100 MHz range for SiC-diodes with some 100 pF junction capacitance and some 10 nH stray inductance. In order to achieve a proper damping, the value of the damping resistor in series to the LC-tank has to be in the range of Z_0.

Using (5.15), the stray inductance of the commutation path can easily be determined by measuring the frequency of the voltage or current oscillation and by using the junction capacitance $C_{\mathrm{j,D}}$ of the diode, specified in the data sheet.

A simple RC-snubber

$$\begin{aligned} C_{\text{snub}} &= 3C_{\text{j,D}} = 300\,\text{pF} \\ R_{\text{snub}} &\approx Z_0 = \sqrt{\frac{L_{\text{wire}}}{C_{\text{j,D}}}} = 11.8\,\Omega \end{aligned} \tag{5.16}$$

could be designed for a SiC-diode with $C_{\text{j,D}} = 100\,\text{pF}$ and an estimated wiring inductance of $L_{\text{wire}} = 14\,\text{nH}$.
According to [155] the power dissipation of the snubber resistor R_{snub} could be estimated by

$$P_{\text{R,snub}} \approx 2 f_{\text{s}} \frac{C_{\text{snub}} V_{\text{o}}^2}{2} \ . \tag{5.17}$$

If a switching frequency of $f_{\text{s}} = 1\,\text{MHz}$ and an output voltage of $V_{\text{o}} = 400\,\text{V}$ is assumed, the resulting power dissipation would be $P_{\text{R,snub}} = 48\,\text{W}$ what clearly shows that RC-snubbers are not applicable advantageously for such high switching frequencies. Accordingly, a damping concept which is effective only for high-frequency AC signals and in a given frequency range must be employed.

In the following several possibilities for implementing the proposed magnetically coupled damping layer will be discussed.

A) Resistive Material in Damping Layer
The idea of this implementation is to use resistive material in the damping layer itself. The currents induced in the resistive layer generate losses and therefore damp the unwanted oscillations. A model of this approach is shown in **Fig. 5.24(a)**. The magnetically coupled damping layer is modeled by the magnetizing inductance L_{m}, the leakage inductance L_{lk} and an ideal transformer with a ratio of $u : 1$. The full leakage inductance is here considered on the secondary side. As is well known from coreless transformer designs [174], the magnetizing inductance L_{m} is quite small as compared to the leakage inductance L_{lk} due to the limited coupling of the layers. The major part of the input current is therefore flowing through the magnetizing inductance as

$$|X_{\text{m}}| = \omega L_{\text{m}} << \left| R_{\text{S}} u^2 + \text{j}\omega L_{\text{lk}} \right| \ , \tag{5.18}$$

which results in a limited damping effect. The inductance L_{m} and hence the coupling of the two layers could be increased using a ferrite

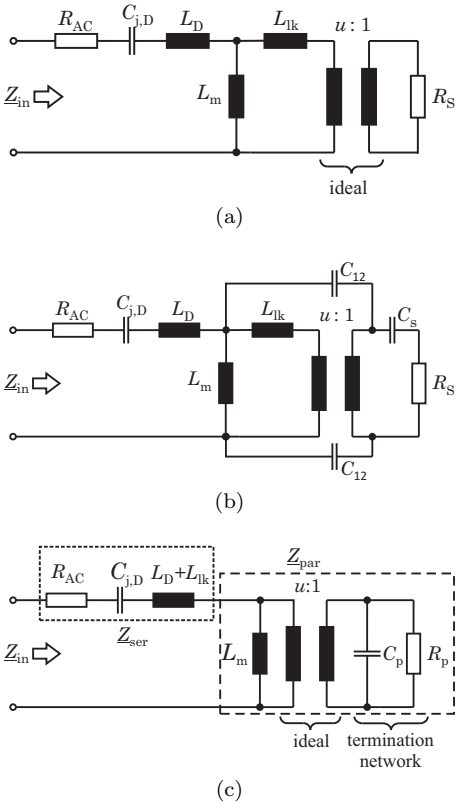


Fig. 5.24: Equivalent circuits of **Fig. 5.23** for turn-on of the MOSFET for the proposed damping layer implementations using (a) resistive material in the damping layer, (b) a series R-C connection or (c) a parallel R-C connection (leakage inductance considered on the primary side) as termination network of the magnetically coupled damping layer.

core or a magnetic layer as done in [175]. This, however, also raises the inductance of the commutation path and is therefore no option in the case at hand. Besides the limited damping capability of this approach the demand of including resistive materials into the layer stack of the PCB is a drawback. Additional materials and production steps are required which results in significantly higher manufacturing costs of the PCB.

B) Series R-C Connection

The high leakage inductance can be compensated if a well designed capacitor C_s is placed in series to the resistor R_s (cf. **Fig. 5.24(b)**). This capacitance forms a series resonant circuit together with the leakage inductance L_lk, which has to be tuned to a resonant frequency being equal to the frequency of the oscillations to be damped. Simulations of the proposed system, however, showed that the coupling capacitance C_{12} can not be neglected in this case and that even a very small coupling capacitance of a few pF overrides the positive effect of canceling the leakage inductance. The best results have been achieved by using a parallel connection of R_p and C_p as termination network which will be discussed in the following.

C) Parallel R-C Connection

According to **Fig. 5.24(c)** the series resonant circuit, formed by $C_\mathrm{j,D}$ and the sum of the inductances L_lk and L_D, is connected in series with a well damped parallel resonant circuit, formed by the termination network and the inductance L_m. The two elements C_p and R_p have to be transferred to the primary side (C'_p, R'_p) considering u:

$$C'_\mathrm{p} = \frac{C_\mathrm{p}}{u^2} \ , \quad R'_\mathrm{p} = R_\mathrm{p} u^2 \ . \tag{5.19}$$

If the resonance frequency f_par of the parallel resonant circuit is chosen according to

$$f_\mathrm{par} = \frac{1}{2\pi\sqrt{L_\mathrm{m} C'_\mathrm{p}}} = f_\mathrm{ser} = \frac{1}{2\pi\sqrt{(L_\mathrm{D} + L_\mathrm{lk}) C_\mathrm{j,D}}} \tag{5.20}$$

leading to

$$C_\mathrm{p} = \frac{L_\mathrm{D} + L_\mathrm{lk}}{L_\mathrm{m}} C_\mathrm{j,D} u^2 \tag{5.21}$$

and the damping resistor is chosen to

$$R_\mathrm{p} u^2 = R'_\mathrm{p} \approx Z_1 = \sqrt{\frac{L_\mathrm{D} + L_\mathrm{lk}}{C_\mathrm{j,D}}} \ , \tag{5.22}$$

the damping of the resulting system can be increased significantly. A Bode plot of the input impedance

$$\underline{Z}_\mathrm{in} = \underline{Z}_\mathrm{ser} + \underline{Z}_\mathrm{par} \tag{5.23}$$

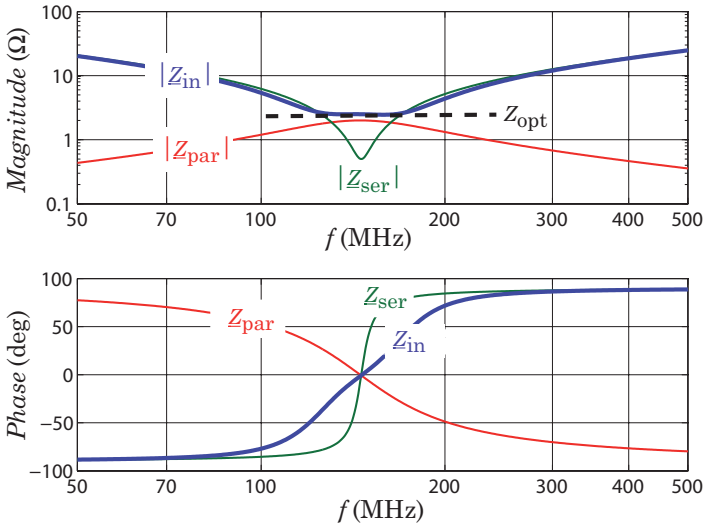


Fig. 5.25: Calculated Bode diagram of impedances $\underline{Z}_{\mathrm{ser}}$, $\underline{Z}_{\mathrm{par}}$ and $\underline{Z}_{\mathrm{in}}$ for the system: $L_1 = 10\,\mathrm{nH}$, $L_2 = 10\,\mathrm{nH}$, $M_{12} = 5\,\mathrm{nH}$, $L_{\mathrm{D}} = 6\,\mathrm{nH}$ and $C_{\mathrm{j,D}} = 126\,\mathrm{pF}$.

with

$$\underline{Z}_{\mathrm{ser}} = \frac{1 + sR_{\mathrm{AC}}C_{\mathrm{j,D}} + s^2 C_{\mathrm{j,D}}\left(L_{\mathrm{D}} + L_{\mathrm{lk}}\right)}{sC_{\mathrm{j,D}}} \tag{5.24}$$

and

$$\underline{Z}_{\mathrm{par}} = \frac{sL_{\mathrm{m}}}{1 + s\frac{L_{\mathrm{m}}}{R'_{\mathrm{p}}} + s^2 L_{\mathrm{m}} C'_{\mathrm{p}}} \tag{5.25}$$

is given in **Fig. 5.25**. The damping of the system is increased when the magnitude of the input impedance is increased at the resonant frequency.

As (5.22) is only an approximation, the optimal values for a maximal damping can be found by application of the following optimization function:

$$Z_{\mathrm{opt}} = \left|\underline{Z}_{\mathrm{in}}\left(f, C_{\mathrm{p}}, R_{\mathrm{p}}\right)\right|\Big|_{\arg(\underline{Z}_{\mathrm{in}}(\mathrm{f}))=0^\circ} \rightarrow \max \ . \tag{5.26}$$

The result of the optimization for an assumed system with the parameters $L_1 = 10\,\mathrm{nH}$, $L_2 = 10\,\mathrm{nH}$, $M_{12} = 5\,\mathrm{nH}$, $L_{\mathrm{D}} = 6\,\mathrm{nH}$ and

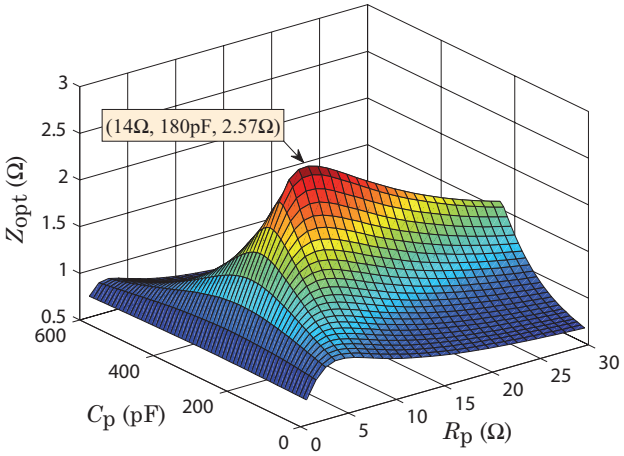


Fig. 5.26: Calculated magnitude of impedance Z_{opt} as a function of the termination network parameters R_p and C_p.

TABLE 5.6: Calculated values for the termination network according to (5.19) and (5.22), and results of the optimization according to (5.26).

	R_p	C_p
Calculated values	9 Ω	186 pF
Result of optimization	14 Ω	180 pF

$C_{j,D} = 136\,\text{pF}$ is depicted in **Fig. 5.26** and the results are summarized in **TABLE 5.6**.

5.2.2 Design of a Damping Layer

The performance of the damping layer is verified using a boost converter as design example (cf. **Fig. 5.5**). This circuit is also used to study the switching behavior of different MOSFET devices. To achieve very fast switching transients, a low impedance gate driver DEIC420 featuring a peak current capability of over 20 A is used. A 600 V SiC-Schottky diode CSD20060D is used for the boost diode D_1. The output capacitance C_o and also C_{in} are partly implemented by several 220 nF / 630 V ceramic type SMD capacitors, providing high current capability and low

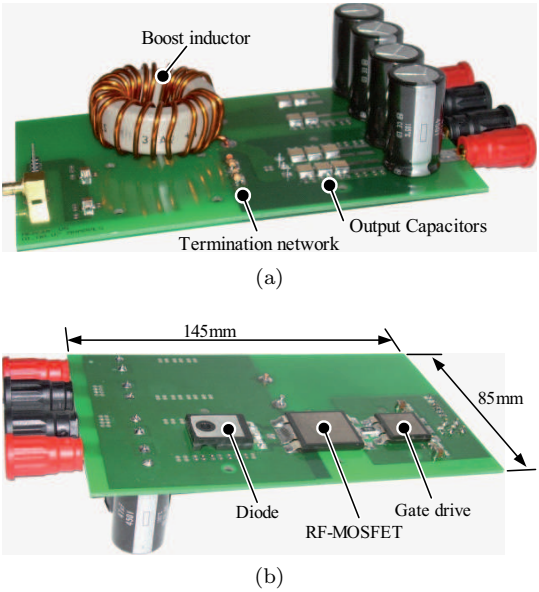


Fig. 5.27: Constructed prototype of the boost circuit with PCB board wiring including a damping layer with optimized termination network. (a) TOP view and (b) BOTTOM view of the prototype which can directly be mounted on a heat sink.

inductance. In [171], it is shown that the switching losses are dominated by the intrinsic capacitance $C_{\mathrm{oss}}(v_{\mathrm{DS}})$ of the MOSFET when very fast switching is used.
The applied CoolMOS devices show, as discussed in detail in section 5.1.2, long delay times at turn-off of the device which finally leads to significant current distortions for lower current values in single-phase and three-phase active rectifier applications.

To overcome the drawback of long delay times a RF switch-mode power MOSFET DE475-501N44 is used. This device shows a much less pronounced $C_{\mathrm{oss}}(v_{\mathrm{DS}})$-characteristic than SJ MOSFETs. The RF MOSFET in addition utilizes a DE475 package which is optimized for high speed, high frequency, high power applications (cf. **Fig. 5.27**). Due to the symmetrical package design, where the two source terminals lie on either side of the drain terminal, the parasitic inductance of the device can be reduced to less than 5 nH [176]. Two commutation paths must therefore be considered in the model. The layout of the boost circuit

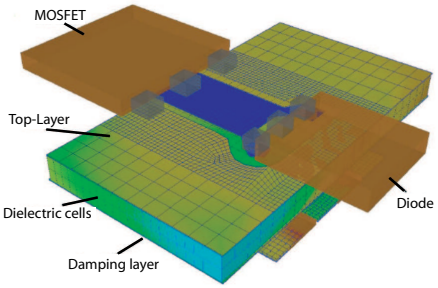


Fig. 5.28: PEEC model of the constructed prototype with damping layer.

is optimized for very low wiring inductances in the commutation path. To form the proposed damping structure, a copper loop terminated by the proposed RC-network, is routed in a layer that is between the two wiring layers (see also **Fig. 5.22**). The MOSFET current i_{DS} is measured using a self-made AC-current probe. A short wire is required for inserting the current sensor into the circuit, resulting in an additional inductance of approximately 8 nH for the commutation path which has to be considered in the model of the damping circuit.

Design using the PEEC Method

The parasitic elements of the system have to be considered for designing an optimal termination network of the damping layer. These elements could be determined by impedance measurements on the constructed hardware using an adequate impedance analyzer. As precise measurements in the pF/nH-range are rather difficult, an alternative method to determine the parameters in an early state of system design based on simulations without building a dedicated prototype shall be used. The PEEC method emerged as a computational efficient and accurate technique for a simulation including layout parasitics [177, 178]. The PCB layout is thereto discretized into a large number of individual elements as shown in the 3D-model of the prototype layout (cf. **Fig. 5.28**). The PEEC method creates matrices of partial elements representing the magnetic and electric field couplings and the resulting equations subsequently are solved in a Spice-like circuit simulator. Recent development makes PEEC an integrated full wave method, which can handle non-orthogonal elements [179] as well as dielectrics [180].

TABLE 5.7: Measured and simulated parasitics of the constructed prototype.

	Measurements (HP4294A)	Simulation (PEEC method)
L_{D}	10 nH (per diode)	–
$C_{\mathrm{j,D}}$	55 pF	–
L_{FET}	4 nH (per lead)	–
L_{Sensor}	8 nH	–
R_{AC}	500 mΩ	–
$L_{1\mathrm{a}}/L_{1\mathrm{b}}$	8.2 nH / 7.7 nH	11.3 nH / 10.5 nH
$L_{2\mathrm{a}}/L_{2\mathrm{b}}$	9.9 nH / 8.1 nH	11.5 nH / 10.6 nH
$M_{12,\mathrm{a}}/M_{12,\mathrm{b}}$	5 nH / 5.3 nH	6.4 nH

In **TABLE 5.7** both simulation results of the PEEC method and measurement results, using the impedance analyzer HP4294A, are summarized. The difference between the measured and calculated layout inductances L_{1i}, L_{2i} and $M_{12,i}$ has its origin in the measurement technique, which poses a challenge due to the compact geometry of an optimized layout. As all parameters of the prototype are identified, a simplified model of the boost circuit can be drawn (cf. **Fig. 5.29**). The optimization of (5.26) results in $R_{\mathrm{p,opt}} = 22\,\Omega$ and $C_{\mathrm{p,opt}} = 184\,\mathrm{pF}$ for the termination network. The optimized components of the termination network are added to the PEEC model.

The capacitive coupling C_{12} between the proposed damping layer and the circuit layout, which was neglected for the sake of easy modeling, lowers the damping performance. Due to the distributed nature of this parasitic capacitance it can not accurately be modeled by a single capacitor. In addition it is difficult to determine C_{12} by measurement due to its small value in the pF-range. The PEEC method considers the distributed nature [181] and was thus used to verify the total effectiveness of the proposed layout, including the dielectric of the FR4 material with $\epsilon_{\mathrm{r}} = 4.4$, and a dissipation factor of $\tan\delta = 0.02$.

The simulated total impedance of the commutation path with opti-

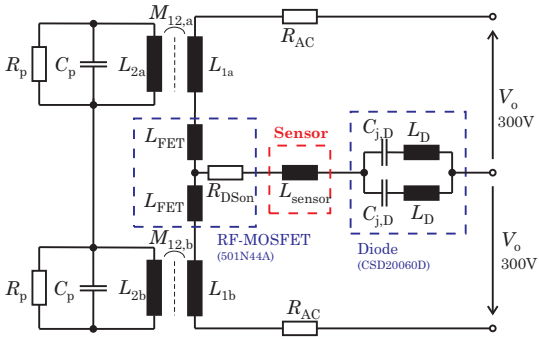


Fig. 5.29: Simplified model of the constructed prototype with damping layer including parasitic elements of the RF-MOSFET, current sensor and the SiC-diode.

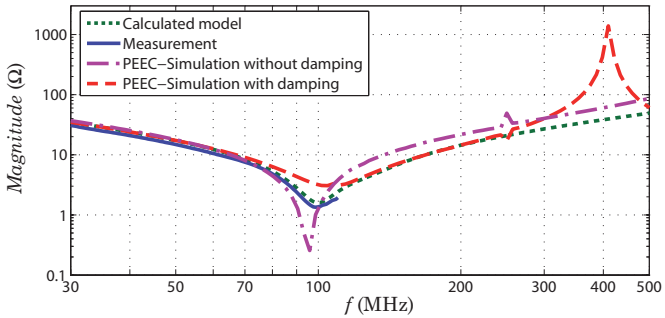


Fig. 5.30: Impedance measurement, calculated impedance using (5.24) - (5.26) and corresponding PEEC simulation of the commutation path, including the effect of the damping layer.

mized damping network, including the dielectric properties of the FR4 material ($\epsilon_r = 4.4$), is depicted in **Fig. 5.30**. There is also an impedance measurement included, taken from the constructed prototype, as well as the calculated impedance of the simplified model of **Fig. 5.29**. The measurements could only be performed up to 110 MHz due to the bandwidth limitation of the used impedance analyzer HP4294A. Comparing the simulation result without damping circuit to the results with optimized termination network ($R_{p,opt}$, $C_{p,opt}$) the damping effect on the resonance at 100 MHz is apparent. A small shift in resonance frequency to a higher value is observed when the damping network is applied. This is due to the lowered inductance as the magnetic fields of

both layers attenuate each other. The resonance due to C_{12} is above 400 MHz and has therefore no significant influence on the ringing behavior at 100 MHz. In addition the PEEC simulation showed that the dielectric dissipation inside the FR4 material does not alter the attenuation behavior significantly. It is therefore reasonable to neglect dielectric loss effects in the model.

The entire effectiveness of the proposed damping layer and the validity of the simplified model of **Fig. 5.29** are approved by PEEC simulation, even though the impedance analyzer measurement in **Fig. 5.30** shows a slightly reduced damping performance compared to the PEEC simulation. This deviation probably has its origin either in measurement errors of the small parasitic inductance values or the fact that the parasitic inductances of the switch and the diode were included as lumped inductances in the PEEC model, which do not couple magnetically with the layout inductances of the model. The consistency of simulation and measurement is however acceptable, but also the simplified model with lumped elements shows good results.

5.2.3 Experimental Results

The constructed prototype with optimized damping network has been tested for a boost converter output voltage of 300 V and for current levels up to 20 A. The results for a current of 10 A are given in **Fig. 5.31** where for **Fig. 5.31(a)** the damping layer of the PCB has been left open. The switching transient oscillations are reduced significantly if the damping layer is applied. The first voltage/current peak is unfortunately still present, but the decay of the ringing is enhanced noticeably.

In **Fig. 5.31(c)** a measurement of a purely resistive damping layer is shown. A 0.2 mm transformer-core Fe-sheet is therefore inserted between the two wiring layers with the thickness of 0.5 mm. The drain-source current $I_{\mathrm{DS,res}}$ (with inserted transformer sheet) is compared to a measurement without any damping $I_{\mathrm{DS,o}}$ and the results confirm the limited damping capability of this approach. The damping effect of a copper layer terminated by a 10 Ω resistor ($I_{\mathrm{DS,10\Omega}}$) is shown as well.

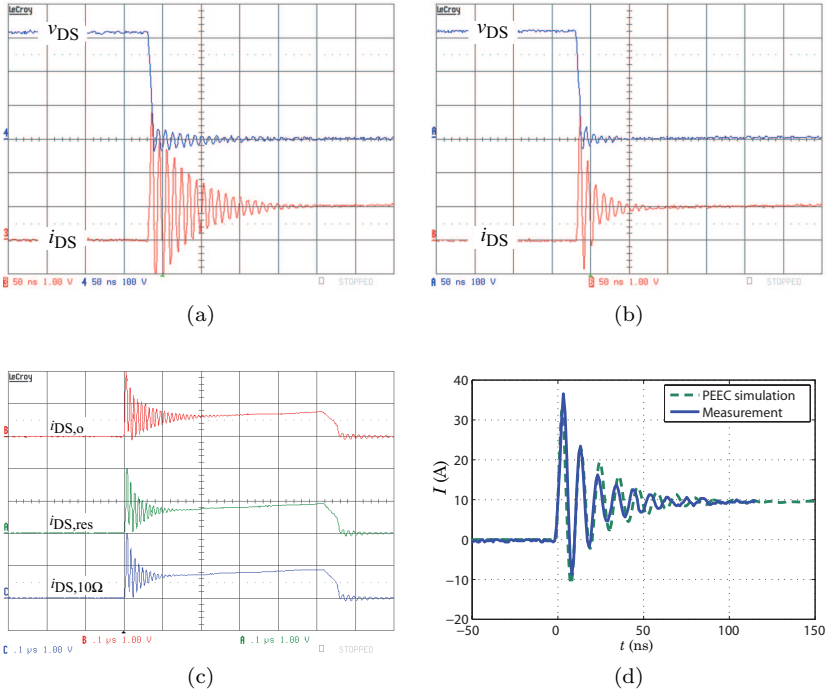


Fig. 5.31: Measurement results taken from the constructed prototypes; (a) Measurement without damping layer and (b) with damping layer terminated by an optimized RC-network. v_{DS}(300 V/Div), i_{DS} (10 A/Div), time scale: 50 ns/Div; (c) Purely resistive damping layer: $i_{DS,i}$ (10 A/Div), time scale: 100 ns/Div; (d) Measured and calculated current shape obtained from a numeric Laplace transform of the impedance curve of **Fig. 5.30**.

The time domain response of the commutation path exited by a step function is calculated based on the simulated impedance curve. In **Fig. 5.31(d)** the numerical result of this transformation is compared to a current measurement taken from the constructed prototype for a current of 10 A. The amplitude of the input step of the numerical system is thereto scaled to obtain an equal final value. The oscillation frequency of the simulated system is slightly smaller than the measured value which can also be seen at the lower resonance point in **Fig. 5.30**. The simulated maximum peak current and especially the damping effect are in good agreement with the measurement results. A PEEC

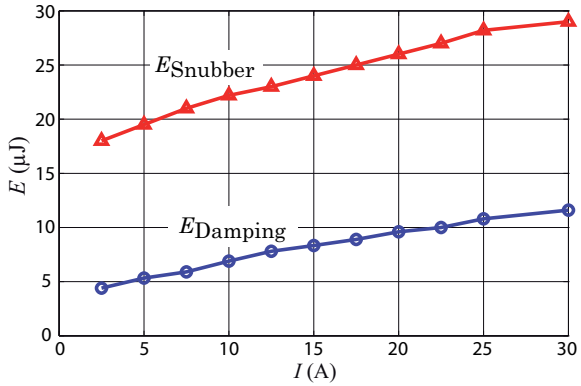


Fig. 5.32: Measured loss-energies of the proposed damping concept (E_{Damping}) compared with the loss-energies of a RC-snubber (E_{Snubber}) designed to achieve similar damping.

simulation can therefore be used to directly analyze the performance of the designed damping system in an early development state with good accuracy.

In **Fig. 5.32** measured damping resistor loss-energies for the proposed magnetically coupled damping layer are compared to losses generated by a RC snubber across the boost diode (cf. (5.17), $R_{\mathrm{snub}} = 10\,\Omega$, $C_{\mathrm{snub}} = 150\,\mathrm{pF}$). The measurements were done at $V_{\mathrm{o}} = 300\,\mathrm{V}$ and the RC snubber is designed to achieve roughly the same damping behavior as the damping layer with optimized termination network. Only the high-frequency oscillations are coupled to the damping resistor in the termination network for the tuned damping layer with parallel RC-termination. On the contrary, the snubber capacitor C_{snub} has to be charged / recharged in every switching cycle which results in significantly higher losses. This confirms that considerable damping can be achieved with the proposed damping layer by only moderate losses in the damping resistor even at switching frequencies in the MHz-range.

5.2.4 Conclusion

In this section a novel passive damping layer was introduced for attenuating the undesired voltage/current ringing appearing at the switch-

ing instants of hard-switched power electronic converters. An additional copper layer, terminated by an optimally designed RC-network, is thereto inserted between the PCB wiring layers of the converter. The additional copper loop is magnetically coupled to the commutation loop of the power circuit. The experimental results show that the ringing can be reduced considerably and that significantly lower losses in the damping resistor occur compared to a traditional RC snubber circuit. The first voltage/current peak of the oscillation is, however, still present. The reason can be found in the weak magnetic coupling of the two loops. The coupling could be improved by application of magnetic material, e.g. ferrite cores or a magnetic layer, but this is no option as this also increases the inductance of the commutation loop. Adding additional resistive materials into the layer stack of the PCB requires additional production steps and results in significantly higher production costs of the PCB which is a serious drawback.
The proposed concept is shown for a boost-type test circuit but is not limited to such topologies. It may be used in other applications where an increase of inductance caused by the magnetic material can be tolerated. Impedance measurements of the built PCB would be necessary for the arrangement and optimization of the termination network. It is shown in this work that by application of the PEEC simulation method the system can be designed and analyzed in an early development state without an existing hardware prototype.

5.3 Semiconductor Power Losses

As a next step the semiconductor power losses of the VR system are calculated where also the cooling system and the thermal interface of the semiconductors are considered. The semiconductor current stresses listed in **TABLE 3.1** are used to calculate the power losses and the dependence of the MOSFET losses on the used chip area A_{Chip} is evaluated. The selected semiconductors are listed in **TABLE 5.8** where also some key specifications are given.

Next to the selection of the MOSFET also the choice of the freewheeling diodes $D_{\mathrm{F}+}$ and $D_{\mathrm{F}-}$ is a crucial factor for implementing a system with highest power density as the reverse recovery current strongly determines the appearing switching losses. The SiC-diode IDT10S60C is selected as it shows no reverse recovery current and only a small charge of $Q_{\mathrm{c}} = 24\,\mathrm{nC}$ of the parasitic junction capacitance. A classical Si-diode would show a considerably higher reverse current which would result in too high switching losses for a switching frequency in the MHz range. The rectifier diode 10ETS08 is used for the mains side diodes $D_{\mathrm{N}+}$ as these diodes are only commutated with mains frequency. The thyristor TYN825 completes the list of applied semiconductors. In the following the semiconductor power losses are calculated.

TABLE 5.8: Semiconductors selected for implementation of the high power density VR system.

Part	Type
S_+, S_-	CoolMOS CP-series $V_{\mathrm{BRR}} = 650\,\mathrm{V}$, $R_{\mathrm{DSon}} = 2.7\,\Omega\mathrm{mm}^2/A_{\mathrm{Chip}}$
$D_{\mathrm{F}+}$, $D_{\mathrm{F}-}$	SiC Schottky diode IDT10S60C $V_{\mathrm{RRM}} = 600\,\mathrm{V}$, $I_{\mathrm{F}} = 10\,\mathrm{A}$
$D_{\mathrm{N}+}$	Rectifier diode 10ETS08 $V_{\mathrm{RR}} = 800\,\mathrm{V}$, $I_{\mathrm{F,avg}} = 10\,\mathrm{A}$
Thy	Thyristor TYN825 $V_{\mathrm{RRM}} = 800\,\mathrm{V}$, $I_{\mathrm{T,rms}} = 25\,\mathrm{A}$

5.3.1 MOSFET Power Losses

The power losses of the MOSFET can be divided into switching losses $P_{\mathrm{FET,sw}}$ and conduction losses $P_{\mathrm{FET,con}}$

$$P_{\mathrm{FET}} = P_{\mathrm{FET,con}} + P_{\mathrm{FET,sw}} \ . \tag{5.27}$$

The conduction losses can be calculated using the on-state resistance R_{DSon} of the MOSFET channel and the switching losses can be determined using the measured turn-on energies given in **Fig. 5.19** and **TABLE 5.5**. The on-state resistance R_{DSon} is a function of the junction temperature T_{j} and the drain source current I_{DS} and scales with $R_{\mathrm{DSon}} \propto 1/A_{\mathrm{Chip}}$ and therefore R^*_{DSon} is defined as $R^*_{\mathrm{DSon}} = R_{\mathrm{DSon}} A_{\mathrm{Chip}}$. A curve fit of data sheet values results in

$$R_{\mathrm{DSon}}(\Delta T_{\mathrm{js}}, I_{\mathrm{DS}}) = \frac{R^*_{\mathrm{DSon,25}}}{A_{\mathrm{Chip}}} \left(1 + \alpha_1 \Delta T_{\mathrm{js}} + \alpha_2 \Delta T_{\mathrm{js}}^2\right) \left(1 + \beta_1 I_{\mathrm{DS}} + \beta_2 I_{\mathrm{DS}}^2\right) \tag{5.28}$$

where $R^*_{\mathrm{DSon,25}}$ is the chip area dependent on-state resistance at $T_{\mathrm{j}} = 25\,^{\circ}\mathrm{C}$ and $I_{\mathrm{DS}} = 0$. The corresponding parameters of this curve fit are listed in **TABLE 5.9**.

The conduction losses

$$P_{\mathrm{FET,con}} = \frac{1}{T_{\mathrm{N}}} \int_0^{T_{\mathrm{N}}} R_{\mathrm{DS,on}}\left(\Delta T_{\mathrm{js}}, I_{\mathrm{DS}}\right) i_{\mathrm{DS}}^2(t)\ dt \tag{5.29}$$

have to be calculated by integration over one mains period as (5.28) is nonlinear. The total MOSFET losses can then be calculated by use of (5.27).
Both, (5.14) and (5.28) require the junction temperature

$$T_{\mathrm{j}} = T_{\mathrm{s}} + R^*_{\mathrm{th,js}} A_{\mathrm{Chip}} P_{\mathrm{FET}} \tag{5.30}$$

which is a function of the chip area dependent thermal interface to the heat sink, expressed by $R^*_{\mathrm{th,js}}$, with the heat sink temperature T_{s} and of the total MOSFET losses P_{FET}. Equation (5.27) has to be solved iteratively by application of (5.29), (5.14) and (5.30).

TABLE 5.9: Selected power devices including main parameters for implementation of the high power density VR system.

MOSFET CoolMOS IPP60R099CP	
Channel	Switching Losses
$R_{\mathrm{DSon},25} = 80\,\mathrm{m\Omega}$	$k_0 = 7.85\,\mu\mathrm{J}$
$\alpha_1 = 0.0083\,\mathrm{K}^{-1}$	$k_1 = 2.53\,\mu\mathrm{J/A}$
$\alpha_2 = 43 \cdot 10^{-6}\,\mathrm{K}^{-1}$	$k_2 = 0.07\,\mu\mathrm{J/A}^2$
$\beta_1 = -0.67 \cdot 10^{-6}\,\mathrm{A}^{-1}$	$\gamma = 80 \cdot 10^{-6}\,\mathrm{K}^{-1}$
$\beta_2 = 0.17 \cdot 10^{-3}\,\mathrm{A}^{-2}$	$E_{400\mathrm{V}} = 11.5\,\mu\mathrm{J}$
Diode $D_{\mathrm{F}i}$ IDT10S60C	
$V_{\mathrm{F,SiC}} = 0.74\,\mathrm{V}$	
$r_{\mathrm{D,SiC}} = 84\,\mathrm{m\Omega}$	
Diode $D_{\mathrm{N}i+}$ 10ETS08	**Thyristor TYN825**
$V_{\mathrm{F}} = 0.7\,\mathrm{V}$	$V_{\mathrm{F,Thy}} = 0.77\,\mathrm{V}$
$r_{\mathrm{D}} = 27.5\,\mathrm{m\Omega}$	$r_{\mathrm{D,Thy}} = 14\,\mathrm{m\Omega}$
Output Capacitors	
$13 \times$ Rubycon BXA $6.8\,\mu\mathrm{F}/450\,\mathrm{V}$	
$ESR = 10\,\Omega$	$I_{\mathrm{leak}} = 79\,\mu\mathrm{A}$
$19 \times$ KEMET X7R $220\,\mathrm{nF}/500\,\mathrm{V}$	
$f_{\mathrm{res}} = 8.5\,\mathrm{MHz}$	
Boost Inductor $20\,\mu\mathrm{H}$	
$A_{\mathrm{Fe}} = 90.7\,\mathrm{mm}^2$	$V_{\mathrm{Fe}} = 6720\,\mathrm{mm}^3$
$N = 18$	
Core Material Micrometals -8, E-core E137-8	
Low Frequency (50/60 Hz)	*High Frequency* (1 MHz)
$K_{\mathrm{NF}} = 2.85\,\mathrm{W/mm}^3$	$K_{\mathrm{HF}} = 0.19\,\mathrm{W/mm}^3$
$\alpha_{\mathrm{NF}} = 1.02$	$\alpha_{\mathrm{HF}} = 1.25$
$\beta_{\mathrm{NF}} = 2.02$	$\beta_{\mathrm{NF}} = 2.24$

An appropriate model of the chip area dependent thermal interface to the heat sink $R_{\mathrm{th,js}}(A_{\mathrm{Chip}})$ is thereto required. A chip area dependent

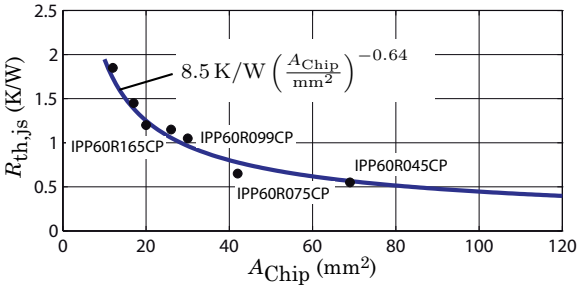


Fig. 5.33: Chip area dependent thermal resistance $R^*_{\mathrm{th,js}}$ of several discrete CoolMOS devices considering a thermal conducting electrical isolation sheet. A curve fitting is given which is used for further calculations.

thermal resistance $R_{\mathrm{th,js}}(A_{\mathrm{Chip}})$ is proposed in [182] where the whole chip is implemented in a single power module using an Al_2O_3 DCB ceramic substrate. Discrete semiconductors using TO220 or TO247 packages shall, however, be applied for the application at hand. Several devices have therefore been analyzed and the corresponding thermal resistances are plotted in **Fig. 5.33** considering also an isolation sheet with a thermal resistance of $R_{\mathrm{th,iso}} = 0.7\,\mathrm{K/W}$. A curve fit of the thermal resistances results in

$$R_{\mathrm{th,js}} = 8.5\,\mathrm{K/W}\left(\frac{A_{\mathrm{Chip}}}{\mathrm{mm}^2}\right)^{-0.64} \tag{5.31}$$

for CoolMOS-CP devices in the TO220 and TO247 case.

Due to the thermal capacitances of the MOSFET devices roughly a constant temperature ΔT_{js} of the MOSFET is assumed within a mains period where the cooling systems ensures a constant heat sink temperature T_{s}. Based on this assumption the total MOSFET power losses can be calculated using the iteration process illustrated in **Fig. 5.34**. At the beginning of the iteration a junction temperature $T_{\mathrm{j}}[0]$ is defined. Based on this junction temperature, the power semiconductor losses $P_{\mathrm{FET}}[n]$ are calculated. According to (5.31) and (5.30), the calculated power losses on the other hand yield to a junction temperature $T_{\mathrm{j}}[n]$. This temperature is compared to the junction temperature of the former calculation step and compared with the termination limit ϵ. As the switching losses $P_{\mathrm{FET,sw}}$ as well as the conduction losses $P_{\mathrm{FET,con}}$

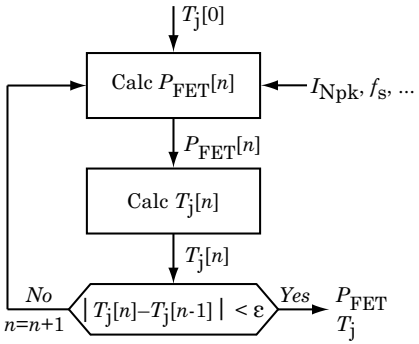


Fig. 5.34: Graphical illustration of the iteration process used to calculate the final junction temperature T_j and total MOSFET losses P_{FET}.

are monotonically increasing function with respect to the junction temperature T_j, this iteration process converges.

The conduction losses have to be calculated by integration over one mains period

$$P_{FET,con} = \frac{1}{2\pi}\int_0^{\pi} \frac{R^*_{DSon,25}}{A_{Chip}}\Big(1+\alpha_1\Delta T_{js}+\alpha_2\Delta T_{js}^2\Big) \Big(1+\beta_1 I_{DS}(\varphi_N)+\beta_2 I_{DS}(\varphi_N)^2\Big) i_{DS}(\varphi_N)^2\delta(\varphi_N)d\varphi_N \quad (5.32)$$

where

$$i_{DS}(\varphi_N) = \hat{I}_N\cos(\varphi_N) \quad (5.33)$$

and the duty cycle has to be inserted according to the applied modulation function (cf. section 3.1.1).
The calculation of the conduction losses can be simplified if the drain source rms and avg currents

$$P_{FET,con,approx} = \frac{R^*_{DSon,25}}{A_{Chip}}\Big(1+\alpha_1\Delta T+\alpha_2\Delta T^2\Big) \Big(1+\beta_1 I_{DS,avg}+\beta_2 I_{DS,rms}^2\Big) I_{DS,rms}^2 \quad (5.34)$$

are used instead of integration over one period. This is mathematically not correct but may be tolerated if the error is rather small. The deviation for a 10 kW rectifier system is given in **Fig. 5.35** where for practical

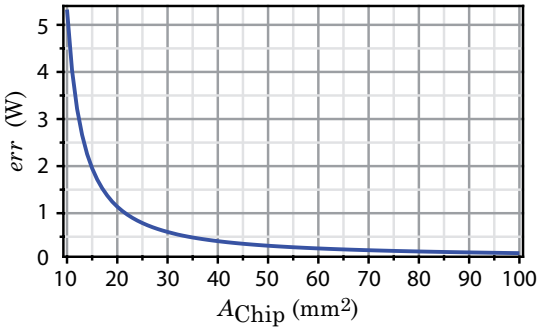


Fig. 5.35: Deviation of the calculated conduction losses $P_{\mathrm{FET,con}}$ as a function of the chip area A_{Chip} if (5.34) is used instead of (5.32).

reasonable chip areas of $A_{\mathrm{Chip}} > 20\,\mathrm{mm}^2$ an error

$$err = P_{\mathrm{FET,con}} - P_{\mathrm{FET,con,approx}} \tag{5.35}$$

below 2 W can be observed. In the case at hand with dominating switching losses the approximation is therefore tolerable.

Similar to the conduction losses the switching losses of the MOSFET device can be calculated by integration over one mains period

$$P_{\mathrm{FET,sw}} = \frac{1}{T_{\mathrm{N}}} \int_0^{T_{\mathrm{N}}} f_{\mathrm{s}}\; E_{\mathrm{on}}\left(\Delta T_{\mathrm{js}}, i_{\mathrm{DS}}(t)\right) dt + \frac{f_{\mathrm{s}}}{2} E^*_{400\mathrm{V}} A_{\mathrm{Chip}} \tag{5.36}$$

using the measured switching loss energies listed in **Fig. 5.19** and **TABLE 5.5**, where T_{N} is the mains period. A comparison of different CoolMOS devices with diverse chip areas shows, that the energy stored in C_{oss} is also directly proportional to A_{Chip} which is modeled using the stored energy $E^*_{400\mathrm{V}}$ in C_{oss}. The integration in (5.36) can be avoided if the temperature coefficient of the switching energies is assumed to be independent of I_{DS} (γ_1 instead of γI_{DS}). The switching losses can then

be calculated to

$$\begin{aligned} P_{\mathrm{FET,sw}} &= \frac{1}{2\pi} f_{\mathrm{s}} \int_0^{\pi} \left(k_0 + k_1 \hat{I}_{\mathrm{N}} \sin(\varphi_{\mathrm{N}}) + k_2 \left(\hat{I}_{\mathrm{N}} \sin(\varphi_{\mathrm{N}}) \right)^2 \right) \\ &\quad \left(1 + \gamma_1 \Delta T \right) d\varphi_{\mathrm{N}} + \frac{f_{\mathrm{s}}}{2} E^*_{400\mathrm{V}} A_{\mathrm{Chip}} = \\ &= \frac{f_{\mathrm{s}}}{2} \left(k_0 + k_1 \frac{2\hat{I}_{\mathrm{N}}}{\pi} + k_2 \frac{\hat{I}_{\mathrm{N}}^2}{2} \right) \left(1 + \gamma_1 \Delta T \right) + \\ &+ \frac{f_{\mathrm{s}}}{2} E^*_{400\mathrm{V}} A_{\mathrm{Chip}} = \\ &= \frac{f_{\mathrm{s}}}{2} \left(k_0 + k_1 I_{\mathrm{N,avg}} + k_2 I_{\mathrm{N,rms}}^2 \right) \left(1 + \gamma_1 \Delta T \right) + \\ &+ \frac{f_{\mathrm{s}}}{2} E^*_{400\mathrm{V}} A_{\mathrm{Chip}} \end{aligned} \tag{5.37}$$

which results in

$$\begin{aligned} P_{\mathrm{FET,sw}} &= \frac{f_{\mathrm{s}}}{2} \left(k_0 + k_1 I_{\mathrm{N,avg}} + k_2 I_{\mathrm{N,rms}}^2 \right) \left(1 + \gamma_1 \Delta T \right) + \\ &+ \frac{f_{\mathrm{s}}}{2} E^*_{400\mathrm{V}} A_{\mathrm{Chip}} \ . \end{aligned} \tag{5.38}$$

Using the approximation (5.34) for the conduction losses and (5.38) for the switching losses, the iteration process given in **Fig. 5.34** is not required and the total losses of the MOSFET (5.27) can directly be solved under consideration of the thermal interface (5.31).

The calculated chip area dependent power losses of the SJ CoolMOS-CP series for the intended 10 kW three-phase VR system are depicted in **Fig. 5.36** for a switching frequency of $f_{\mathrm{s}} = 1\,\mathrm{MHz}$. Due to the high switching frequency, the MOSFET power losses are dominated by switching losses. They show a minimum at $A_{\mathrm{Chip}} \approx 27\,\mathrm{mm}^2$ which would be the optimal chip area for the intended rectifier system. Next to the good performance regarding input current distortions the CoolMOS device IPP60R099CP is also an ideal candidate regarding losses and is therefore used for the hardware implementation.

The optimal chip area $A_{\mathrm{Chip,opt}}$ yielding minimal semiconductor losses can be calculated as a function of the switching frequency f_{s} and

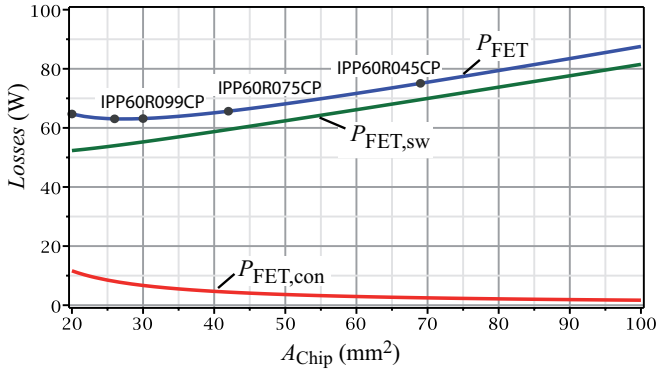


Fig. 5.36: Dependency of the MOSFET power losses P_{FET} consisting of conduction losses $P_{FET,con}$ and switching losses $P_{FET,sw}$ on the chip area A_{Chip} at a switching frequency of $f_s = 1\,MHz$ and an output power of $P_o = 10\,kW$.

the results are given in **Fig. 5.37(a)** for the CoolMOS-CP series. The optimal chip size decreases for higher switching frequencies and shows a minimum at $f_s \approx 800\,kHz$. Due to the better thermal interface of a larger chip area and the linearly increasing switching losses for higher switching frequencies, the optimal chip size increases for switching frequencies above 800 kHz. A chip size of $A_{Chip} \approx 30\,mm^2$ can therefore be achieved if a switching frequency of $f_s = 1\,MHz$ is applied.
The corresponding junction temperature T_j is in addition given in **Fig. 5.37(b)** as a function of f_s, where a heat sink surface temperature of $T_s = 50\,°C$ is assumed. Due to the linearly rising switching losses also the junction temperature rises linearly. The CoolMOS-CP series allows a maximal junction temperature of $T_{j,max} = 150\,°C$. A maximal switching frequency of 1.23 MHz can accordingly be implemented using the CoolMOS-CP series. Note that this switching frequency limitation is only valid for the applied model using the thermal interface given in (5.31), for a heat sink temperature of 50 °C and for the switching loss parameters given in **TABLE 5.5**. A different thermal interface, or heat sink temperature or different parasitic capacitances of the final construction will result in a different switching frequency limitation. The maximal switching frequency will, however, be in the range between 1 MHz and 1.5 MHz.

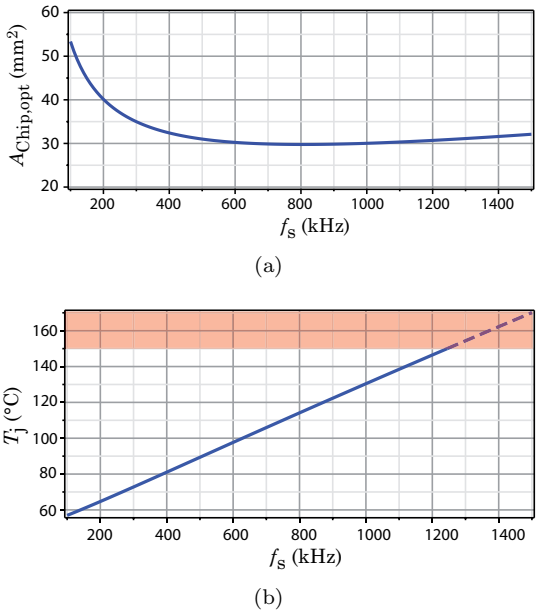


Fig. 5.37: (a) Optimal chip area $A_{\mathrm{Chip,opt}}$ yielding to minimal MOSFET power losses as a function of switching frequency f_s and (b) corresponding junction temperature T_j as a function of f_s.

5.3.2 Total Semiconductor Power Losses

In the following the total power losses are calculated for a 10 kW VR system. Due to the turn-off delay of the MOSFET coming along with input current distortions, the limited switching speed of the devices caused by parasitic oscillations and the increasing switching losses a switching frequency of $f_\mathrm{s} = 1\,\mathrm{MHz}$ is chosen for the rectifier system with highest possible power density. As already discussed the SJ CoolMOS device IPP60R099CP with a chip area of $A_\mathrm{Chip} = 30\,\mathrm{mm}^2$ is chosen for the power transistor.
The remaining semiconductor conduction losses can be calculated using the average and rms current stresses listed in **TABLE 3.1** in combination with data sheet values given in **TABLE 5.9**.
The total conduction losses of the free-wheeling diodes $D_{\mathrm{F}i+}$ and $D_{\mathrm{F}i-}$

TABLE 5.10: Calculated semiconductor power loss break-down of a 10 kW VR for a switching frequency of $f_s = 1\,\text{MHz}$ ($P_o = 10\,\text{kW}$, $V_o = 800\,\text{V}$, $f_N = 50\,\text{Hz}$).

Input voltage (line rms)	207	230	253	V
Input current (rms)	17.2	15.5	14.1	A
Modulation index	0.735	0.816	0.898	
Losses				
MOSFET conduction losses	73.8	42	24.6	W
MOSFET switching losses	381	330.6	294	W
Total MOSFET losses	454.8	372.6	318.6	W
Diode losses D_{Fi}	66.6	61.9	58.1	W
Diode losses D_{N+}	28.6	24.6	21.5	W
Thyristor losses	24.1	21.2	18.85	W
Total semiconductor losses	574.1	480.3	417.1	W
Semiconductor efficiency	94.3	95.2	95.8	%

can be calculated using

$$P_{D_F} = 6\left(V_{F,SiC} I_{D_F,avg} + r_{D,SiC} I^2_{D_F,rms}\right) \ . \tag{5.39}$$

The conduction losses of the mains diodes D_{Ni+} and the thyristors Thy can be calculated in a similar way

$$P_{D_N} = 3\left(V_F I_{D_N,avg} + r_D I^2_{D_N,rms}\right) \tag{5.40}$$

$$P_{Thy} = 3\left(V_{F,Thy} I_{D_N,avg} + r_{D,Thy} I^2_{D_N,rms}\right) \ . \tag{5.41}$$

The semiconductor power losses are calculated using the derived formulas and the results are given in **TABLE 5.10** for $V_N = 230\,\text{V} \pm 10\,\%$ and for a switching frequency of $f_s = 1\,\text{MHz}$. Further system parameters are $P_o = 10\,\text{kW}$, $V_o = 800\,\text{V}$ and $f_N = 50\,\text{Hz}$.

The calculated semiconductor power losses are illustrated in **Fig. 5.38** where the incredibly high amount of $P_{v,semi} = 480.3\,\text{W}$ can be observed which causes a relatively low semiconductor efficiency of $\eta_{semi} = 95.2\,\%$. The semiconductor power losses are, due to the high switching frequency, dominated by switching losses which take approximately 69 % of the total power losses. The second largest loss amount

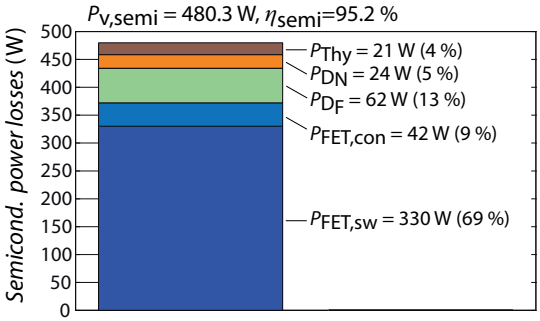


Fig. 5.38: Calculated semiconductor power loss break-down for a switching frequency of $f_s = 1\,\text{MHz}$ if the SJ CoolMOS IPP60R099CP is applied; System parameters: $f_N = 50\,\text{Hz}$, $V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$ and $P_o = 10\,\text{kW}$.

are the conduction losses of the SiC-diodes which take 13 %. According to the calculation derived in section 5.3.1 the junction temperature of the MOSFET increases up to $T_j = 130\,°\text{C}$ for $V_N = 230\,\text{V}$. If the mains voltage is reduced to the lower limit $V_N = 0.9 \cdot 230\,\text{V} = 207\,\text{V}$ the junction temperature will rise to $T_j = 158\,°\text{C}$ which is slightly over the limit of 150 °C and an operation at rated power with the reduced mains voltage is hence not possible. The rectifier system is, however, implemented using the switch IPP60R099CP and the switching frequency $f_s = 1\,\text{MHz}$ to demonstrate that a high power density and operation with such a high switching frequency is possible. An operation with main voltages below 230 V, e.g. 230 V − 10 % may therefore not possible if the temperature of the heat sink is $T_s = 50\,°\text{C}$.

With regard to the high semiconductor power losses the question arises if the system can be cooled by a properly designed cooler. It has been verified, that the junction temperature stays below $T_{j,max} = 150\,°\text{C}$ for $V_N = 230\,\text{V}$ if a heat sink temperature of $T_s = 50\,°\text{C}$ can be ensured. How this is achieved is discussed in the following section where the design of a proper water cooler is described.

5.3.3 Design of a Water Cooler

According to **Fig. 5.38**, the cooling system has to dissipate a heat flow of 480 W and the temperature of the heat sink shall be below 50 °C. A water cooler is designed in the following for this purpose. A single water

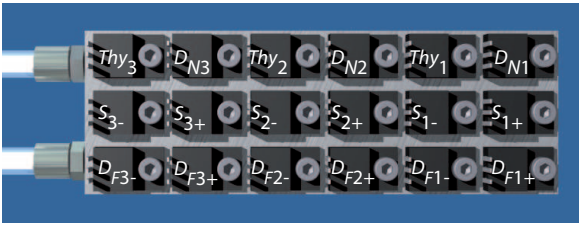


Fig. 5.39: Placement of the semiconductors on the designed water cooler with dimensions of 110 mm × 38 mm × 10 mm.

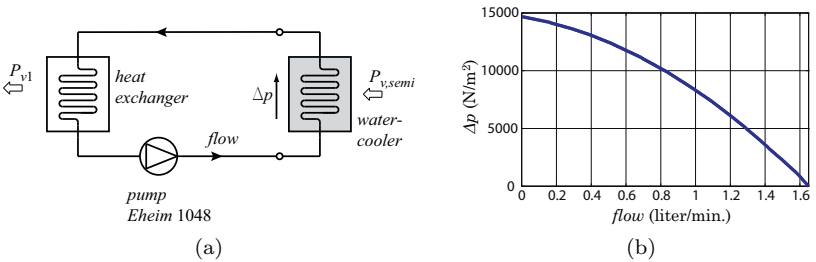


Fig. 5.40: (a) Cooling system employing water cooler, heat exchanger, pump and pipes and (b) characteristic of the applied pump.

cooler is used in order to achieve a very high power density and all discrete devices are mounted on top with small distances. **Fig. 5.39** shows the semiconductor placement on the water cooler with the dimensions of 110 mm×38 mm×10 mm. All MOSFETs are mounted in the middle row flanked by the free-wheeling diodes $D_{\mathrm{F}i}$ on one side and by the mains diodes $D_{\mathrm{N}i+}$ and thyristors Thy_i on the other side. All semiconductors use the non-isolated TO220-case and are electrically insulated using a Kapton insulation foil. This electrical insulation is already included in the thermal interface given in (5.31).

The basic structure of the cooling system, consisting of a water pump, water cooler, heat exchanger and pipes is shown in **Fig. 5.40(a)**. The achieved water flow is dependent on the pressure drop of the water cooler and the characteristic of the applied pump (cf. **Fig. 5.40(b)**) which is discussed in detail in [183]. A similar pump as in [183] is used for the following analysis.

Many different channel structures are possible for implementing the

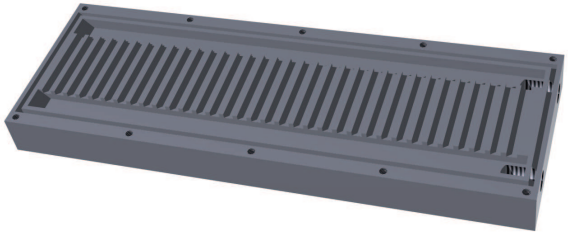


Fig. 5.41: Possible Design of a water cooler using a horizontal fin structure.

water channel. Some research has been dedicated to the cooling of processors and Very Large Scale Integrated (VLSI) systems [184, 185]. Application for an IGBT module is given in [186] and a special channel configuration known as *Shower Power* is proposed in [187] and [188]. In [183] a direct water cooler using a structure of parallel channels was proposed and analyzed. It has to be clarified in the following whether this interesting structure is applicable in the intended application or not. A 3D-model of such a water cooler is shown in **Fig. 5.41** where the parallel channels with a depth of 1 mm are clearly visible. The dimensions of these channels are chosen according to the optimization results of [183] and show a width of 2 mm followed by a 1 mm aluminum bar.

A FEM simulation is used to determine the pressure drop and the heat distribution of the designed water cooler. A pump with a fixed flow rate of 1.4 liter/min is connected to the inlet and the calculated semiconductor losses are applied as heat sources according to the locations given in **Fig. 5.39**. First of all the pressure drop of the cooling system has to be evaluated which can be used to evaluate the operating point of the cooling system using the measured pump characteristic. This is an iterative process as the flow must be adapted according to the pressure drop. A pressure drop of $2000\,\mathrm{N/m^2}$ can be observed for the case at hand which is in good agreement with the selected flow rate of 1.4 liter/min. If the surface temperature of the water cooler is, however, analyzed a continuing temperature rise from S_{3-} to S_{1+} is visible (cf. **Fig. 5.42(a)**). The heat sink temperature at the last MOSFET S_{1+} is 67 °C which is quite above the desired temperature limit of 50 °C. The inhomogeneous pressure distribution in the parallel channels in combination with the limited thickness of the inlet and outlet channels, located on the right

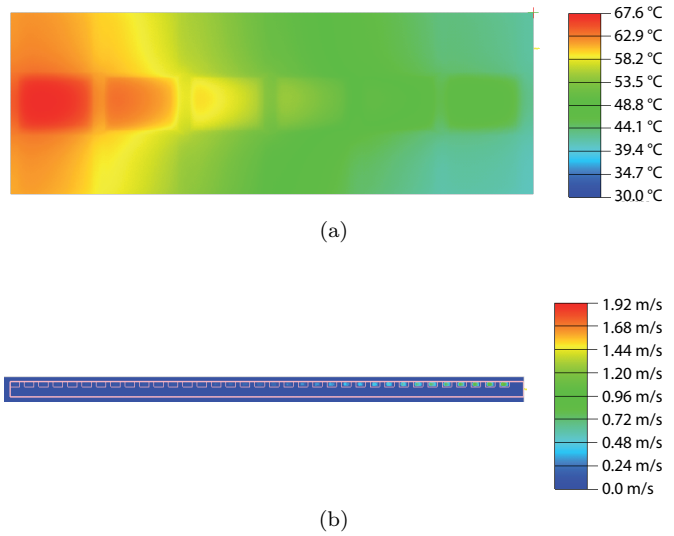
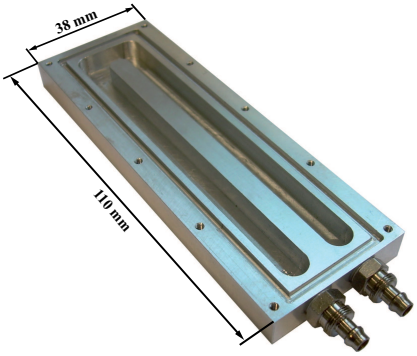


Fig. 5.42: (a) Temperature distribution on the water cooler implemented according to **Fig. 5.41** and (b) water flow rate in the parallel channels.

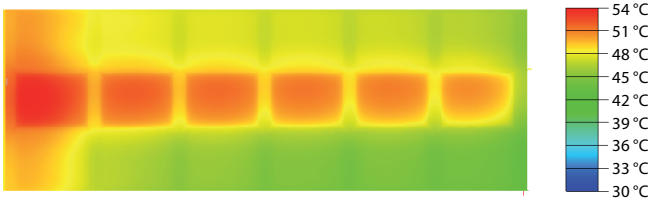
and left side of the parallel channels, results in unequal flow rates in the particular channels. According to **Fig. 5.42(b)**, a considerably reduced flow rate occurs for the channels located farther from the in/outlet.

The effective area of the inlet and outlet channels can not be increased as the semiconductors are screwed onto the water cooler and the rest of the cooler material has is reserved for the screws. The thickness of the effective area of the parallel channels can be increased with increasing length of the water cooler in order to achieve similar pressure drops in the channels. This improvements are, however, limited as the geometry of the water cooler, especially the long length in combination with small width, is unfavorable for such an implementation.

A more optimized implementation using channels with different widths results in a maximal heat sink temperature of 58 °C. Due to the limited performance and due to some other mechanical issues another channel geometry has to be found.



(a)



(b)

Fig. 5.43: (a) Implemented water cooler using a single slot water channel and (b) simulated temperature distribution.

A single water channel with a width of 7 mm and a depth of 6 mm is used for the finally constructed water cooler (cf. **Fig. 5.43(a)**). This channel can favorably be inserted between the mounting holes of the semiconductors. The iterative adaption of flow-rate and pressure drop in combination with the pump characteristic of the intended pump results in a flow rate of 1.58 l/min and a pressure drop of only 700 N/m^2. The resulting temperature distribution of the water cooler is given in **Fig. 5.43(b)** where a maximum heat sink temperature of 54 °C can be observed. A water temperature at the inlet of 30 °C is used which is in good agreement with the actual implemented system. If the water temperature of the inlet is reduced to 25 °C a maximum heat sink temperature of 49 °C occurs which fulfills the requirement. An appropriate heat exchanger is therefore required for operation of the rectifier system with full power.

The thermal resistance of the water cooler is calculated according to [183] which results in $R_{\mathrm{th,sa}} = 0.05\,\mathrm{K/W}$ which is also in good agreement with the measured temperature rise.

5.4 Passive Components

5.4.1 Boost Inductor

The volume of the boost inductor scales with switching frequency and can be reduced by increasing the switching frequency. According to section 3.1.3 a boost inductor value of $L_N = 20\,\mu H$ has to be chosen for a switching frequency of 1 MHz if a peak-to-peak current ripple of 20 % is allowed ($k = 0.2$). As analyzed in [120] the major switching ripple spectral components occur at f_s and $2f_s$ and the magnetic material used to implement the boost inductor must show low losses in this frequency range.

The frequency dependency of the complex permeability $\mu = \mu' - j\mu''$ of the widely used ferrite materials N97 and N49 from EPCOS Inc. is shown in **Fig. 5.44(a)**. The real part of the permeability μ' of material N97 is, according to **Fig. 5.44(a)**, only constant up to a frequency of $\approx 1\,MHz$ and drops quickly for higher frequencies. In addition, the imaginary part μ'', which is related to core losses, rises steeply. The material N97 can therefore not be applied for implementation of the boost inductors and is also not a good option for construction of the DM filter inductors as will be discussed in section 5.7.

An implementation using the material N49 would be possible for $f_s = 1\,MHz$ employing two ELP32 cores but the resulting total volume of the inductor would be too high. The permeability of the powder core material -8 from Micrometals Inc. stays constant up to a frequency of 100 MHz (cf. **Fig. 5.44(b)**) and shows acceptable losses. This material is therefore chosen for implementation of the boost inductor. Two E-cores (E137-8) with an A_L value of $A_{L0} = 67\,nH$ are used for implementation. Under consideration of a current dependent drop in permeability of 10 % the required number ob turns to implement $L_N = 20\,\mu H$ can be calculated as

$$N = \sqrt{\frac{L_N}{0.9 A_L}} = 18\,\text{turns}\ . \tag{5.42}$$

The averaged volume related core losses can be calculated using the improved generalized Steinmetz equation (iGES)

$$p_{v,core,avg} = \frac{1}{T_N} \int_0^{T_N} k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{(\beta-\alpha)}\, dt \tag{5.43}$$

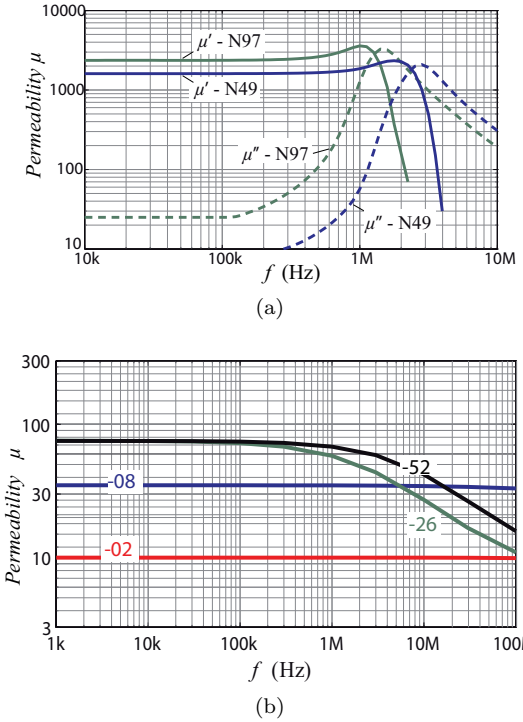


Fig. 5.44: (a) Real and imaginary part of complex permeability $\mu = \mu' - j\mu''$ for the ferrite materials N97 and N49 from EPCOS Inc.; (b) Initial permeability of the powder core materials from Micrometals.

presented in [189], where α and β are the Steinmetz parameters of the magnetic material which can be extracted from the data sheet. This approach is intended for ferrite materials but can approximately be used also for powder core materials. The flux density curve can now be divided into minor loops with minor peak flux densities ΔB. In the intended application of a boost inductor the minor loops relate to the switching ripple and the major loop is the flux density component with mains frequency. As the ripple current and therefore also the flux density are piecewise linear functions the simplified version

$$p_{\mathrm{v,core,avg}} = \frac{k_{\mathrm{i}}}{T_{\mathrm{N}}} \sum_m \left(\Delta B(\Delta t_{\mathrm{m}})\right)^{\beta-\alpha} \left|\frac{\Delta B_m}{\Delta t_m}\right|^{\alpha} \Delta t_m \tag{5.44}$$

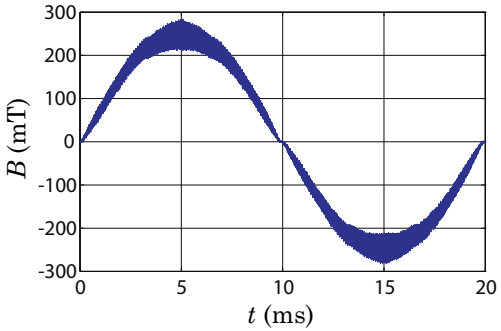


Fig. 5.45: Simulated flux density curve of the boost inductor: Parameter $f_s = 1\,\text{MHz}$, $f_N = 50\,\text{Hz}$, $V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$ and $P_o = 10\,\text{kW}$).

with

$$k_i = \frac{K}{2^{\beta+1}\pi^{\alpha-1}\left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)} \tag{5.45}$$

can be applied (cf. [189]). The minor loops, which relate to the switching frequency ripple, are extracted from the flux density waveform which is generated by a computer simulation of the VR system (cf. **Fig. 5.45**). The flux density is quite below 300 mT and the peak-to-peak flux density of the high-frequency loops is below 40 mT. The authors of [189] supply a Matlab script [190] which provides the extraction of the minor loops and the calculation of the core losses. This script uses equal Steinmetz parameters for the high-frequency minor loops and for the low-frequency major loop. In order to get more accurate results different Steinmetz parameters for low and high frequencies are used. This is possible because the minor loops are related to the switching frequency and the major loop is related to the mains frequency. The used Steinmetz parameters are listed in **TABLE 5.11** and applying the modified algorithm on the the flux density curve shown in **Fig. 5.45** results in

$$P_{v,\text{core}} = 0.78\,\text{W}\ . \tag{5.46}$$

for the 20 µH boost inductor using two E137-8 E-cores.

Next to core losses also high-frequency losses in the winding due to skin and proximity effect occur besides the losses caused by the low-frequency AC resistance and/or mains frequency current component.

TABLE 5.11: Steinmetz parameters of the magnetic material -8 from Micrometals Inc. for different frequency ranges.

$f = 50/60\,\mathrm{Hz}$	$f = 1\,\mathrm{MHz}$
$K_{\mathrm{LF}} = 2.85\,\mathrm{W/m^3}$	$K_{\mathrm{HF}} = 0.19\,\mathrm{W/m^3}$
$\alpha_{\mathrm{LF}} = 1.016$	$\alpha_{\mathrm{HF}} = 1.25$
$\beta_{\mathrm{LF}} = 2.024$	$\beta_{\mathrm{HF}} = 2.24$

The skin-depth of copper at 1 MHz can be calculated to

$$\delta_{\mathrm{Cu,1MHz}} = \sqrt{\frac{1}{\mu\pi\gamma_{\mathrm{Cu}} f_s}} = 71\,\mu\mathrm{m} \tag{5.47}$$

which would result in unacceptable high copper losses if a single copper wire would be used even if only a small current ripple of a few amps would occur. A litz-wire can be used to overcome this drawback but a litz-wire shows a small window utilization factor. The volume of such an implementation would be considerably large which would not allow to reach a very high power density. A bunched copper wire consisting of 5 strands with a diameter of $d = 0.9\,\mathrm{mm}$ is used instead of the litz-wire and shows a notable improvement compared to the single copper wire. The copper wires show therefore a current density of

$$J = \frac{I_{\mathrm{N}}}{5A_{\mathrm{Cu}}} = 7.5\,\mathrm{A/mm^2}\ . \tag{5.48}$$

A practical constructed inductor shows, beneath its inductance, also parasitic capacitances, mainly the capacitance of the winding. This parasitic capacitance has to be charged/discharged during the switching actions of the semiconductors and generates additional capacitive switching losses. As will be discussed in section 5.7, the boost inductor is advantageously used for the first filter stage of the EMI filter and should therefore show a high resonance frequency. A helical winding arrangement, as shown in **Fig. 5.46(a)**, is used in order to minimize the winding capacitance. Each strand is wounded on a single layer starting with the first strand and the second strand starts above the beginning of the first strand which automatically results in a helical winding arrangement if all strands are connected in parallel after manufacturing. However, due to the different length

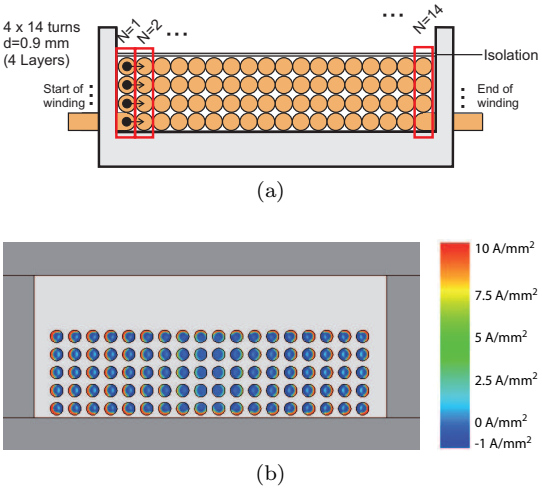


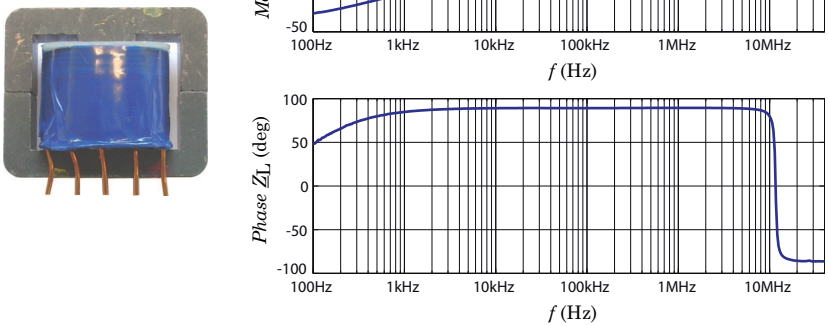
Fig. 5.46: (a) Winding arrangement of the constructed boost inductor and (b) simulated current densities of the current ripple using the FEM-simulator MAXWELL.

of the paralleled strands the current distribution will not exactly be equally in the five strands and a slightly higher current will flow in the strand with the smallest winding length. This effect, as well as the proximity effect has to be considered when the current density of the wires are defined.

The finally constructed boost inductor is shown in **Fig. 5.47** where also a Bode plot of the inductors' impedance is given. The resonance can be found at $f_{\mathrm{res}} = 11.7\,\mathrm{MHz}$ and a winding capacitance of only $C_{\mathrm{w}} = 8.1\,\mathrm{pF}$ can be calculated.

The high-frequency losses of the winding are composed of losses due to skin effect and proximity effect. A 2D-FEM simulation is performed to determine these losses using the FEM-simulation software Maxwell. A sinusoidal current ripple with a frequency of 1 MHz and an rms-value of 3 A is used as current source. The simulated current densities in the winding are shown in **Fig. 5.46(b)**. The high-frequency copper losses can now be calculated using these current densities which finally results in

$$P_{\mathrm{Cu,1MHz}} = 1.25\,\mathrm{W}\ . \tag{5.49}$$



(a) (b)

Fig. 5.47: (a) Constructed boost inductor with $L_N = 20\,\mu H$ and (b) Bode plot of the inductor impedance. Parallel resonance occurs at $f_{res} = 11.7\,MHz$.

Considering the copper losses caused by the low-frequency mains current ($P_{Cu,50Hz} = 2.4\,W$) the total copper losses

$$P_{v,Cu} = P_{Cu,50Hz} + P_{Cu,1MHz} = 3.65\,W \tag{5.50}$$

and subsequently the total inductor losses

$$P_{v,L} = P_{v,Cu} + P_{v,core} = 4.4\,W \tag{5.51}$$

can be calculated. This value is relatively large and a small fan is therefore placed near the boost inductors for cooling as also the CM inductors require some amount of cooling. Further details are discussed in section 5.8.

5.4.2 Output Capacitor

Several design criteria such as output voltage ripple, holdup time or current ripple stress exist for the design of the output capacitors. Holdup time requirements typically result in large capacitance values

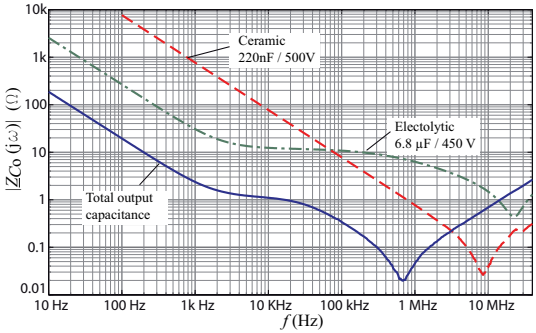


Fig. 5.48: Measured impedance of different capacitor types (device only) used for implementing the output capacitor C_o and measured impedance of the finally implemented C_o (including PCB).

and these requirements are not compatible with a very high power density and are therefore not further considered here. Output voltage ripple is an important design criterion in case of a phase loss as the rectifier system then behaves like a single-phase system and a pulsating power flow, as typical for single-phase systems, exists.

The output capacitors have to handle the high-frequency current ripple which can be calculated according to the formula given in **TABLE 3.1**. Note, that also a low-frequency current (third harmonic neutral point current, cf. section 3.1.1) is present. Due to the parasitic elements of the capacitors, e.g., the ESR of the electrolytic capacitors, this current ripples generate losses. Several capacitor types can be used to implement C_o and in **Fig. 5.48** the measured impedance curve of a 220 nF/500 V capacitor (X7R, SMD, Kemet) is compared to an electrolytic capacitor (Rubycon BXA-series, 6.8 μF/450 V). The impedance of the electrolytic capacitor is limited by its ESR for frequencies beyond 5 kHz, which is about 10 Ω. The ceramic capacitor, in contrast, shows no distinctive ohmic behavior. Only a resonance frequency at about 10 MHz caused by the parasitic inductance of the device is visible. Its impedance is, however, much smaller than the impedance of the electrolytic capacitor at $f_s = 1$ MHz . A combination of these two capacitor types is therefore used. In total 19×220 nF/630 V ceramic capacitors are connected in parallel to $13 \times 6.8\,\mu$F/450 V electrolytic capacitors

which yields a total output capacitance of

$$C_{\mathrm{o,tot}} = 19 \cdot 220\,\mathrm{nF} + 13 \cdot 6.8\,\mu\mathrm{F} = 92.6\,\mu\mathrm{F}\ . \tag{5.52}$$

The resulting measured impedance curve of $C_{\mathrm{o,tot}}$ including the PCB is also given in **Fig. 5.48**. Due to the smaller impedance of the ceramic capacitors only a small amount of the ripple current ($\approx 500\,\mathrm{mA}$) flows through the electrolytic capacitors which is much smaller than the rated current ripple of 150 mA per device given in the data sheet.

5.4.3 Total Power Losses

As a next step the total system losses are determined. In addition to the semiconductor power losses calculated in section 5.3.2 and the losses of the boost inductor and the output capacitor, all remaining loss components must be taken into account. Those additional losses are mainly due to the losses of the EMI filter. The power losses of the EMI filter are estimated in section 5.7.4 and result in $P_{\mathrm{EMI}} = 30\,\mathrm{W}$.

The second largest additional loss component is the power required for the auxiliary supply which also includes the gate drive power. Due to the very high switching frequency of 1 MHz the power required to charge/discharge the gate of the MOSFETs cannot be neglected. Using the chip area dependent gate charge Q_{G}^{*} listed in **TABLE 5.2**, the gate drive power demand of the MOSFET IPP60R099CP can be calculated to

$$P_{\mathrm{G}} = V_{\mathrm{G}}\ Q_{\mathrm{G}}^{*}\ A_{\mathrm{Chip}}\ f_{\mathrm{s}} = 1.2\,\mathrm{W}\ . \tag{5.53}$$

If the current consumption of the DSP, of the FPGA and of the analog circuitry is considered an auxiliary power of 17 W is estimated which includes the gate drive power for all six switches.
An additional loss component of $P_{\mathrm{add}} = 10\,\mathrm{W}$ containing all losses not specifically covered by the preceding calculations such as conduction losses of the PCB is considered.
The total power losses and the total efficiency of the system can be calculated using all calculated loss elements. The resulting, chip area dependent system efficiency for a system employing SJ devices of the CoolMOS CP series is given in **Fig. 5.49**. As in section 5.1.2 the turn-off delays and subsequently the input current quality of the CoolMOS CP series is compared to HV-MOSFETs also semiconductor losses and

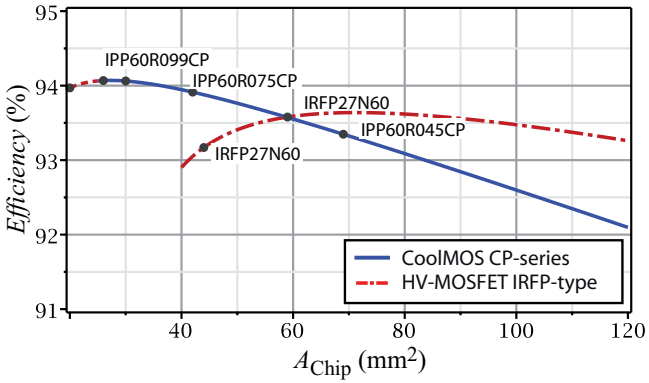


Fig. 5.49: Calculated system efficiency as a function of the chip area for a switching frequency of $f_s = 1\,\text{MHz}$ using either the CoolMOS CP series or HV-MOSFETs; ($V_N = 230\,\text{V}$, $f_N = 50\,\text{Hz}$ and $P_o = 10\,\text{kW}$).

rectifier efficiency is calculated for the HV-MOSFETs. The results are also given in **Fig. 5.49** even if a detailed loss calculation is omitted for the sake of brevity.

Due to the very high switching frequency and, in consequence the high switching losses, only an efficiency slightly above 94 % can be achieved even if SJ devices are applied. The junction temperature of the SJ devices for a chip area below $25\,\text{mm}^2$ would rise above the limit of $150\,^\circ\text{C}$ and a practical implementation is inhibited because of the limited performance of the thermal interface. This interval is marked by a red dotted line. Because of the significant higher area specific on-resistance R^*_{DSon} of HV-MOSFET devices a larger chip area is required. A maximum efficiency of 93.6 % might be achievable for the HV-MOSFETs. The chip area dependent energy $E^*_{400\text{V}}$ stored in the C_{oss} of the HV-MOSFET is smaller than $E^*_{400\text{V}}$ of the SJ devices (cf. **TABLE 5.2**) and a system employing HV-MOSFETs would show advantages regarding efficiency for $A_{\text{Chip}} > 60\,\text{mm}^2$. A system using SJ-devices, however, reaches a higher efficiency at a smaller chip size and SJ devices are therefore preferred for a switching frequency of 1 MHz.

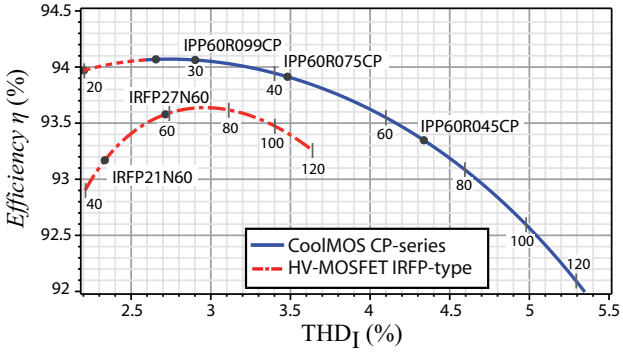
5.5 Efficiency-THD-Pareto Front

In section 5.1.2 the influence of the turn-off delay of the MOSFET on the input current quality has been evaluated (cf. **Fig. 5.11**). The result of this analysis is a curve showing the THD_I of the input currents as a function of the chip area. On the other hand the result of section 5.4.3 is an efficiency curve as a function of the chip area (cf. **Fig. 5.49**).

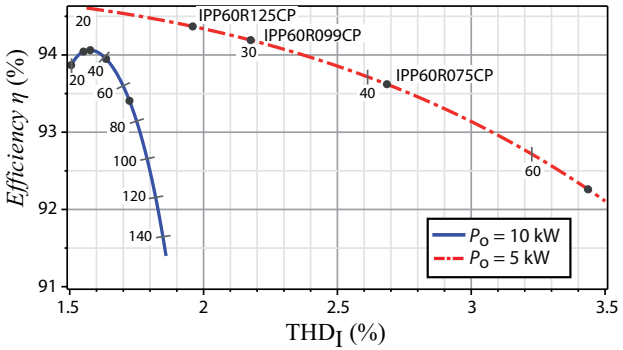
The two results can now be combined and the calculated system efficiency η can be plotted as a function of input current distortion THD_I where A_{Chip} acts as a parameter. This yields to the η-THD_I-Pareto Front where the trade-off between efficiency and input current quality is clearly illustrated. The input current quality as well as the system efficiency are strongly dependent on the switching frequency. Thereby, for every selected switching frequency a dedicated η-THD_I-Pareto Front exists.

The resulting η-THD_I-Pareto Front for a switching frequency of 1 MHz and an output power of 10 kW is shown in **Fig. 5.50(a)** for the SJ devices (CoolMOS-CP) and HV-MOSFETs. The given results are without the proposed feedforward signal. The corresponding chip areas (in mm^2) are marked in the two curves. A maximal efficiency of 94.1 % can be achieved for CoolMOS-CP devices and a THD_I of 2.7 % can be read at this point. Devices with smaller chip areas would show a better input current quality but show increased conduction losses because of the increased on-state resistance at small chip sizes ($R_{DSon} \propto A_{Chip}$). Due to the limited thermal resistance of the discrete devices (see also **Fig. 5.33**) the junction temperature would rise above the limit of 150 °C. A classical HV-MOSFET on the contrary, shows a substantially better THD_I at same chip size but is not able to show its strength due to higher losses.

If the proposed pre-control signal is implemented the input current distortion can be mostly compensated which results in the Pareto Front given in **Fig. 5.50(b)**. A deviation of 10 % is assumed for the pre-control signal for simulation of the resulting THD_I. The THD_I stays below 2 % for a system operating at 10 kW. It has to be stated once again, that this THD_I value only considers input current distortions caused by the turn-off delay of the switches and its non-ideal feedforward signal and that the actually measured THD_I may be quite higher. If the



(a)



(b)

Fig. 5.50: Graphical representation of the trade-off between input current quality (expressed by the THD_I value) and efficiency for a 10 kW rectifier system with a switching frequency of 1 MHz. (a) System operated without feedforward signal and (b) with pre-control signal at 10 kW and 5 kW. Corresponding chip areas A_{Chip} are marked along the curves (in mm^2). Sections of the curves with increasing THD_I for increasing efficiency represent a Pareto Front.

system is, however, operated at partial load (e.g. 5 kW) a considerably increased THD_I occurs.

5.6 High Speed Current Control

Current control of three-phase PWM rectifier circuits using switching frequencies in the MHz-range poses a challenge. A classical analog average current controller as in [116] shows several problems, especially, the high-speed analog PWM suffers from limited accuracy and configurability.

Using purely digital current control, the application of a modern high-speed DSP, is a good way to control PWM rectifiers for medium and high switching frequencies ($f_s = 20 \ldots 200\,\text{kHz}$) [117] as the internal ADCs and PWM units can be used (cf. **Fig. 5.51(a)**). Research into digital control of single-phase PFCs has been performed by several groups [191, 192, 193, 194, 195] and a good introduction to digital current mode control can be found in [196]. Input voltage feedforward has emerged as a very effective way to improve the input behavior of digitally controlled PFC circuits [197]. Furthermore, special care has to be taken for practical implementations concerning the sampling point of the current measurement becomes very important as the disturbances of the current measurement signal occur in the vicinity of the switching instants [198].

In all these approaches, the data processing and numerical calculations of the current controller have to be executed within one switching cycle, which limits the switching frequency of the rectifier system. This is even more difficult to achieve in a single DSP solution as the control of three currents has to be performed sequentially as illustrated in **Fig. 5.51(b)**. One approach to overcome this limitation is to calculate a new duty cycle for only one phase of the three-phase rectifier during a switching period and to hold the duty cycles of the two other phases constant during this time. In the next switching cycle, the second phase is controlled and the two other phases are held constant, whereas in the following switching cycle, the third phase is controlled. This method was used in [117] to control a VR system with a switching frequency of 400 kHz. The calculation time of the current controller (for one phase) has been reduced to 1 µs for this implementation. The delay time of the ADC must, unfortunately, be added to this calculation time. The inductance value and therefore also the physical inductor size consequently has to be increased

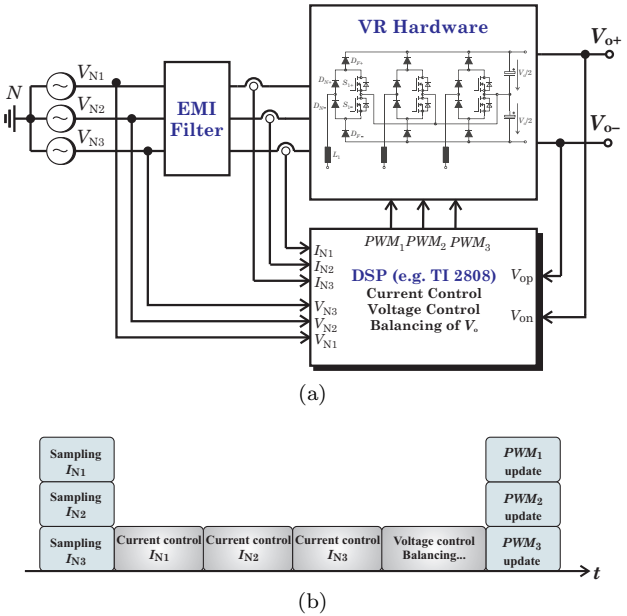


Fig. 5.51: (a) General digital control structure using a single DSP and (b) corresponding timing diagram.

to achieve a small current ripple. This approach shows in addition only a limited improvement by a factor of three in the calculation speed.

In [199], a digital "offline" control technique is presented, where the duty cycles of a single-phase boost converter are calculated in advance based on the power balance equation of the converter. This offline calculation is performed for several operating points and a set of duty cycles is stored in a memory. Depending on the operating point of the rectifier, a specific set of duty cycles is selected to control the switches. This control strategy is not directly dependent on the switching frequency of the converter but cannot be used for the desired application due to the very large input current distortion; its application is hence limited to a small number of operating points. Another predictive algorithm presented in [200] shows several improvements, but this approach is also not applicable in systems with variable AC input frequencies.

The key to overcome the limited processing speed is "parallelization." This could be implemented by using one DSP for each phase of the three-phase system, but the number of instructions executed between the sampling instants is still limited and the cost of implementation is high. Another option is to use a field-programmable gate array (FPGA) for current control, which intrinsically offers parallelization. In contrast to the sequential operation of DSPs, all operations can be executed simultaneously within an FPGA and so a substantial increase in processing speed can be achieved. In [201], a digital controller implementation in an FPGA using a switching frequency of 50 kHz is presented. The efficient implementation of proportional-integral-differential controllers in an FPGA is discussed in [202] as well as predictive algorithms using an FPGA in [203]. All these designs use conventional logic cells for implementation of the controller elements and the processing speed of these elements (dependent on the type of the FPGA) is still limited to clock rates of less than 100 MHz.
Another limitation is the implementation of a Digital PWM (DPWM). A clock frequency of over 2 GHz would be necessary for a classical symmetrical counter/comparator implementation with a resolution of 10 bit, which is far too high, even for high-speed FPGAs. As switching frequencies in the MH-range are common in low-power DC/DC converters, comprehensive research on this issue has been carried out by research groups dealing with these converter types [204, 205, 206]. However, most of the reported solutions are, unfortunately, not directly applicable for an FPGA implementation.
Several concepts for implementation of a high-speed, high-resolution DPWM in an FPGA have been developed [207, 208, 209, 210], but all these concepts implement only edge-aligned PWMs. A new high-speed DPWM scheme is hence developed in this section which allows generation of three-phase symmetrical PWM signals.

In this section, two controller implementations for a 1 MHz three-phase VR are presented which use modern high-speed FPGAs (cf. **Fig. 5.52(a)**). Today's high-speed FPGAs contain DSP blocks including hardware multipliers that can be used advantageously to implement the control algorithm. The effort to implement a controller for switching frequencies above 1 MHz increases rapidly. Two implementations using FPGAs from different vendors are therefore presented. A maximal

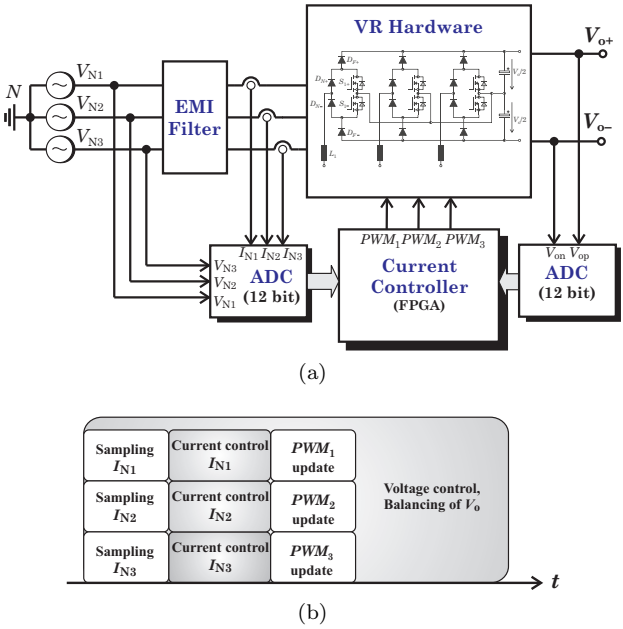


Fig. 5.52: (a) Structure of the three-phase current controller for the VR system using a single FPGA and (b) corresponding timing diagram.

switching frequency of 1 MHz is intended for the first implementation (C1) and the high-speed FPGA ECP2 LFE2-12E-6T144I with a speed grade 6 from Lattice is used. The second implementation (C2) is for switching frequencies beyond 1 MHz based on a high-speed FPGA from Xilinx Corporation (VIRTEX4 XC4-VLX25-10FF668 FPGA with speed grade 10). The finally constructed 1 MHz VR system uses the controller implementation C1.

5.6.1 Design of the Control System

As there are no ADCs included in the mentioned FPGAs, external converters are required. The main limitation for the ADC is its delay time (time between sampling instant and availability of the sampled data), which is also influenced by the interface type of the ADC. Two different ADCs with different interface types are therefore used for the two implementations. In order to implement a three-phase controller

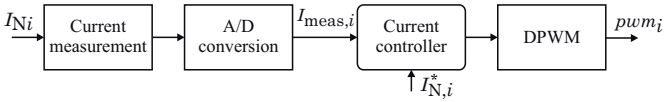


Fig. 5.53: Single-phase signal chain of the digital current controller for a three-phase VR system.

with a switching frequency beyond 1 MHz, each element of the complete signal chain, comprising current measurement, A/D conversion, digital controller, and high-speed DPWM generation, has to be considered in detail (cf. **Fig. 5.53**).

As a first step, the timing requirements on the system blocks have to be defined. A timing diagram of the sampling strategy (of one-phase current) is shown in **Fig. 5.54**. In addition to the fundamental, i.e. local average of the rectifier input current $i_{\mathrm{N}i,\mathrm{avg}}$, a current ripple is present. As is well known, the sample value $I_{\mathrm{N}i}[n]$ is in single-phase systems equivalent to the average current value $i_{\mathrm{N}i,\mathrm{avg}}$ if the sampling point is located in the center of the PWM period (assuming a symmetric center-aligned PWM). Furthermore, a large amount of ringing occurs in the measurement signal near the switching instants. The influence of this ringing on the current measurement can be minimized by this sampling strategy. Synchronization between PWM generation and sampling of the currents is hence very essential. This synchronization can be implemented by a center-aligned, symmetrical PWM generation. The center-aligned PWM offers in addition the advantage of reduced input current distortions in the intended VR application [100] and is therefore used here for controller implementation.

After sampling the actual current value $I_{\mathrm{N}i}[n]$, the ADC requires some time to convert the sampled analog value into a digital word. This result is used by the current controller to calculate the new duty cycle of the PWM signal. At the sampling instant $n+1$, the PWM value is updated with the new modulation function value $m[n]$. This sampling strategy is also known as uniformly sampled modulation [211]. According to **Fig. 5.54**, the whole controller calculation, consisting of A/D conversion, calculation of current controller, and update of the PWM, has to be done within a single switching cycle. This delay (dead time) of one cycle has to be included in the controller design and reduces the phase margin of the controller loop considerably. For lower switch-

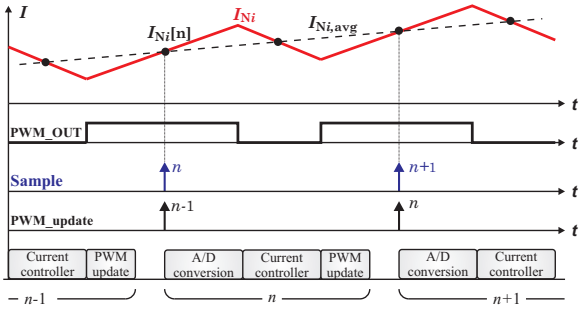


Fig. 5.54: Timing diagram of the sampling strategy. The current signal is sampled in the middle of the pulse period. After the A/D conversion time, the duty cycle δ is calculated by the current controller and updated at the start of the next PWM cycle. Remark: For the sake of clarity the graphical representation is related to single-phase system. The phase current ripple shows a different shape for the actual three-phase system.

ing frequencies, a double update of the PWM is possible, which reduces this delay, and therefore, increases the stability of the current controller.

Current Measurement

Due to the intended very high switching frequency also an increased bandwidth requirement for the current sensor applies. Especially control strategies such as Direct Power Control [212] or Decoupled Hysteresis Control [213, 114], where the switching instants are directly derived from the measured currents, require exact knowledge of the current ripple. But also average mode control requires a large current sensor bandwidth in order to implement the sampling strategy shown in **Fig. 5.54**.

The implementation of a novel current sensor concept with a bandwidth of [DC . . . 1 MHz] is proposed in [214] where also an overview of isolated current measurement methods is given.

The schematic of the proposed current sensor is shown in **Fig. 5.55(a)**. The sensor uses an AC current transformer (CT) with special demagnetization circuitry to prevent the core from saturation or to allow the measurement of a DC current component or both. In the considered active rectifiers the input currents have

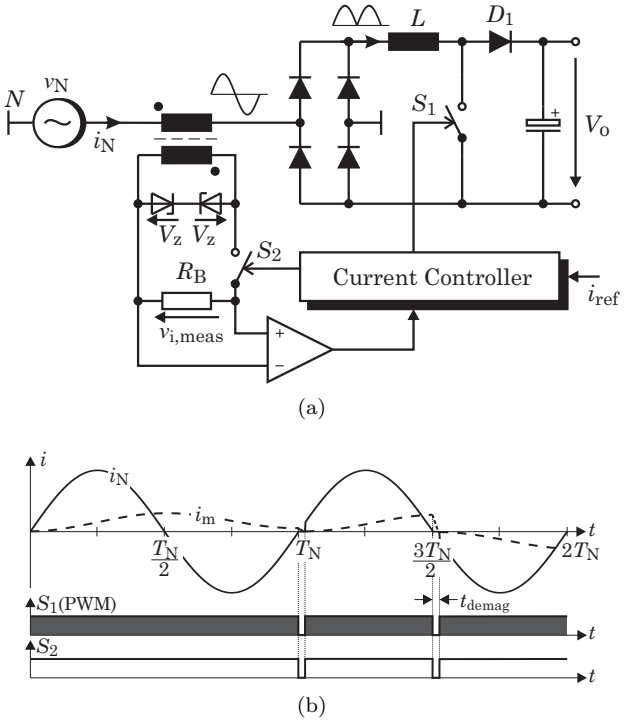


Fig. 5.55: (a) Schematic of the proposed current sensor consisting of a current transformer and a demagnetization circuit shown for a single-phase PFC rectifier; (b) Demagnetization concept with demagnetization after a full mains period ($t < T_N$) and after a half-period ($t > T_N$).

approximately a sinusoidal shape and therefore show zero crossings at fixed time intervals. The measurement signals of the input currents are only required during the positive/negative half-wave between the zero crossings. The new sensor therefore consists of a conventional CT, which does not saturate during the half-wave of the input current and measures the AC and DC component of the input current during this time. During the zero crossings the current is kept for a short time at zero by the current controller and the magnetic core is reset/demagnetized, so that the flux is again zero at the beginning of the next half wave and it could measure the current during the next half-wave (cf. **Fig. 5.55(b)**).

As there are already distortions at the zero crossings of the input currents of a PFC rectifier which cannot be avoided completely [166], the short time for demagnetizing the phase current sensors does not cause noticeable additional distortions. The proposed sensor concept using a CT in combination with minor extensions in the current controller can consequently be used for measuring the AC as well as the DC components of the input current without any additional sensor element. A detailed analysis of the sensor concept is given in [214] and not further discussed here. Also an adapted version of the sensor concept suited for the VR structure is given in [214]. The size of the magnetic core of the CT, however, inhibits an application of this promising sensor concept for the intended ultra-high power density system.

The current sensor CDS4025 from Sensitec Inc. [215] is used instead in the constructed prototype. The sensor is based on the magneto resistive effect, shows a bandwidth of 200 kHz and is able to measure AC currents as well as DC currents. A detailed discussion of the measuring principle and suggestions how to extend the bandwidth of this sensor type is given in [216]. As average mode control is used in this work a detailed knowledge of the current ripple is not required and the bandwidth of the Sensitec sensor is adequate. Due to its small size it is particularly suitable for the intended high power density implementation.
During initial operation of the rectifier system a distorted measurement signal caused by the surrounding magnetic field of the current sensor has been observed. A proper placement of the current sensor is therefore very important to achieve a high performance. As a solution for the case at hand the whole sensor is wrapped with a small Mu-metal foil with a thickness of 0.1 mm which considerably reduced the coupling effects.

A/D Conversion

Next, an appropriate ADC has to be chosen. A converter with a resolution of 12 bit is required. The main selection criterion is, however, its delay, as ADCs with high sampling rates usually show a relatively long delay between sampling and availability of the data. ADCs with sampling frequencies of 3 MSa/s are commercially available with a simple SPI interface and such a converter is used for the controller implementation C1. Only ADCs with parallel or LVDS interface [217] are available

TABLE 5.12: Specifications of the used ADCs.

	Controller C1 AD7274	Controller C2 ADS5240
Sampling frequency	1 MSa/s	25 MSa/s
Resolution	12 bit	12 bit
Converters / Package	1	4
Interface	SPI	LVDS
Delay	448 ns	300 ns
Cots (per 1000 pcs.)	US$ 6.58	US$ 25.88

for higher sampling frequencies. A pipelined ADC with a sampling frequency of $f_{\text{sample}} = 25\,\text{MHz}$ and an LVDS interface is consequently used for controller implementation C2.

The main specifications of the used ADCs are listed in **TABLE 5.12** where also the prices are listed.
The LVDS interface, in general, is well-suited for industrial applications as it is based on current drivers and differential signaling. The circuit effort of using an LVDS interface, however, is much higher than for a simple SPI interface. The selected FPGAs are indeed able to directly drive the LVDS signals without any additional components, but impedance-controlled and length-matched PCB tracks have to be implemented. In addition, as discussed below, the digital implementation of the LVDS interface in the FPGA is much more complex. The serial LVDS interface is, however, the only alternative to a parallel interface if very high switching frequencies of $f_s > 1\,\text{MHz}$ are to be implemented.

Controller Design

Two different strategies are possible for the design of a digital controller. One strategy is to design an appropriate analog controller and convert it into the digital domain ("digital redesign"). The other strategy, known as direct digital design, is to directly design the controller in the z-domain. The direct digital design method results in a slightly better controller performance with regard to phase margin and achievable bandwidth [218]. On the other hand, digital redesign offers the capability to use the well-known design methods of the continuous-time

implementations. A digital redesign of an analog controller will hence be used.

The analog model of the current control loop, derived in section 3.2.1, is used to design a proper digital current controller. The delay of one sampling step caused by the controller calculation (cf. **Fig. 5.54**)

$$G_{\mathrm{calc}}(s) = e^{-sT_{\mathrm{s}}} \tag{5.54}$$

and the delay introduced by the symmetrical PWM

$$G_{\mathrm{PWM}}(s) = e^{-sT_{\mathrm{s}}/2} \tag{5.55}$$

have to be considered.
The bilinear (Tustin) transformation is used for discretization of the analog controller given in (3.34) which results in

$$K_{\mathrm{I}}(z) = K\frac{1 - k_1 z^{-1}}{1 - k_2 z^{-1}} \ . \tag{5.56}$$

The behavior of the designed controller can now be verified in the z-domain. A block diagram of the control loop is given in **Fig. 5.56(a)**. According to [219], delay of the symmetrical PWM is modeled by a sample and hold element $G_{\mathrm{H0}}(s)$ and the controller delay $G_{\mathrm{calc}}(s)$ is considered by the block z^{-1}. The bandwidth limitation of the current sensor is included in the model by $M_{\mathrm{I}}(s)$.
In **Fig. 5.56(b)** the Bode plot of the resulting control loop for the 1 MHz system using the controller parameters $K = 0.25$, $k_1 = 0.96$ and $k_2 = 0.99$ is depicted where a phase margin of 45° can be found. There, $G(z)$ is the transfer function of the converter system including pulse-width modulation and including the transfer function of the current measurement $M_{\mathrm{I}}(s)$.

Several additional parts have to be added to the current controller for the final controller implementation and the resulting structure is shown in **Fig. 5.57**. In order to increase the modulation range of the rectifier, a third harmonic signal $v_{\mathrm{h3}}[n]$ is added and a zero-sequence current component $i_0[n]$, generated from the voltage symmetry controller. In addition, the current feedforward signal $i_{\mathrm{ff}}[n]$ used to compensate the turn-off delay of the CoolMOS switches, is shown. Two DPWM units are necessary to generate the gate signals for the two switches, where the

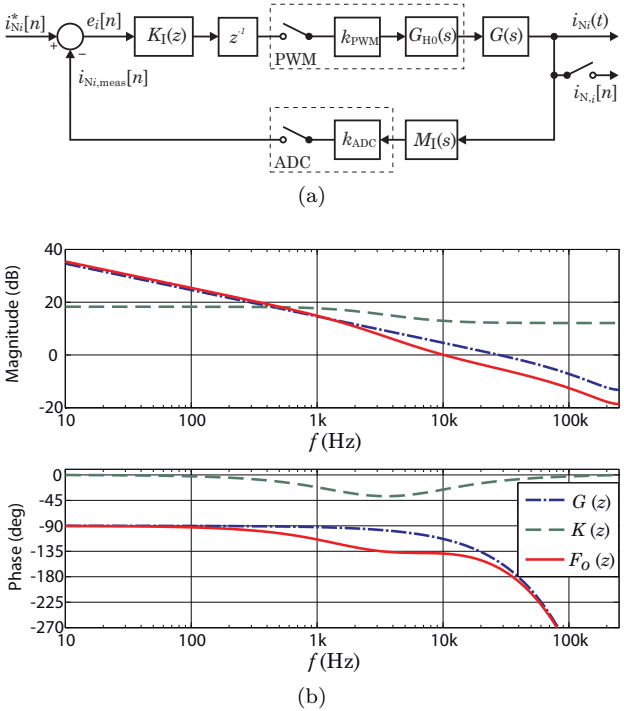


Fig. 5.56: (a) Model of the digital current control loop and (b) Bode plot of the digital current controller. The designed controller shows a phase margin of 45 °.

PWM signal of the switch S_{i-} has to be inverted. The POS_OFFSET and NEG_OFFSET signals are used to implement the proper duty cycles without the need of an additional, 180°-phase shifted, carrier signal for the PWM. These two offsets can also be adapted by a superimposed controller to achieve better performance in DCM [220].

PWM Generator

The generation of the symmetrical high-speed PWM signals must be implemented inside the FPGA as there is no external PWM unit readily available for such high frequencies. There are several possibilities known in literature to implement a digital high-speed PWM using an FPGA. The performance of a counter/comparator approach is limited due to

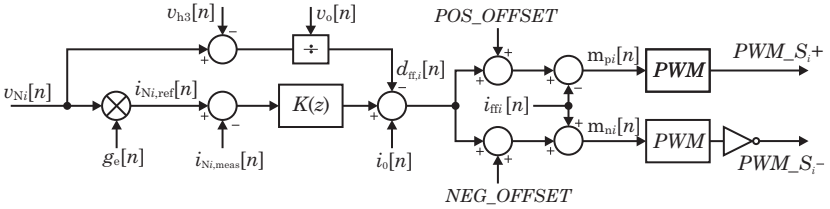


Fig. 5.57: Structure of the digital current controller for one phase.

the very high clock frequencies required to implement a high-frequency PWM. An FPGA implementation using a hybrid delay line and counter scheme is described in [207] which is, however, only applicable to trailing edge modulators, shows a strong temperature dependence, and is not easy to implement. It has been shown in [208] that the resolution of a counter/comparator approach can be increased by application of phase-shifted clocks. This approach is, however, also limited to trailing edge modulators.

In this work, a novel symmetrical DPWM implementation using two phase-shifted clocks is proposed (cf. **Fig. 5.58**). The modulator consists of two different counters/comparators running with a phase shift of 180°. The least significant bit selects, if either the PWM signal with 180° phase shift or the PWM signal without phase shift is used. A combination of the two signals is used to increase the resolution of the modulator by 1 bit. Only switching between the two phase-shifted PWM signals would result in asymmetrical signals, and therefore, the comparator value m of the 180° phase-shifted modulator has to be adapted. This is done at the two instants, where the counter direction has to be reversed ($Cntr = 0$, $Cntr = \max$) and the modulator is also updated with the new modulator values at these instants. Both comparator limits (PWM_0 and PWM_{180}) have to be set to m while counting up, whereas the comparator value for the 180° phase-shifted modulator has to be set to $m + 1$ while counting down.

The necessary comparator values m are summarized in **TABLE 5.13** and the resulting PWM patterns for $m = 3$ are plotted in **Fig. 5.58(b)**. The two phase-shifted signals have to be treated as asynchronous signals in the FPGA. The multiplexer must therefore be implemented by logic cells without a (pipeline) register and operates continuously. The

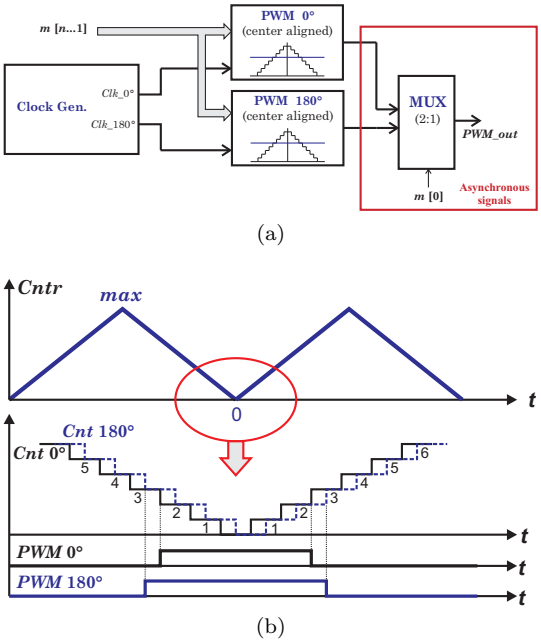


Fig. 5.58: Proposed concept for a center-aligned DPWM implementation; (a) Block diagram describing the concept and (b) generation of the PWM patterns for a comparator value of $m = 3$.

multiplexer output is changed at the same instant when the modulator is updated and the output is set according to the least significant bit of the comparator value $m[0]$. Timing and routing constraints must therefore be used in the design implementation. This concept could also be extended to four 90° phase-shifted modulators (modern FPGAs are typically able to generate 90° phase-shifted clocks by an internal delay-locked loop), which would increase the resolution by one more bit. The more complex adaption of the comparator value m inhibits a high-speed implementation of this extended concept at present.

5.6.2 Implementation of the System

In this section, the two implementations of the current controllers using the two FPGAs are discussed. Even though the implementations are

TABLE 5.13: Comparator values m for the proposed DPWM implementation.

	$PWM_{0°} = 1$	$PWM_{180°} = 1$
Count up	$Cntr < m$	$Cntr < m$
Count down	$Cntr < m$	$Cntr < m + 1$

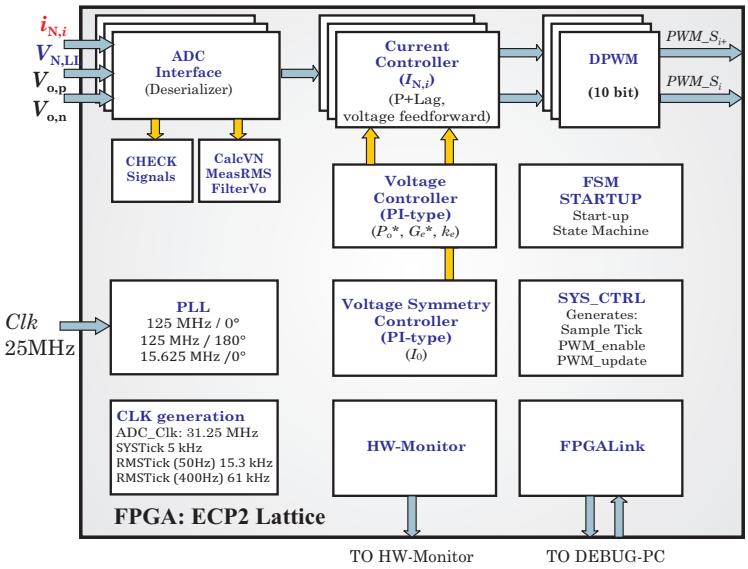


Fig. 5.59: Overview of a controller implementation in a single FPGA. Next to the current controller also voltage controller, balancing of the output voltages and several system tasks are shown.

adjusted to fit the selected FPGAs in this work, nearly all other FPGA vendors offer devices with similar functionality, and could therefore be selected.

An overview of the controller implementation, listing all implemented blocks, is shown in **Fig. 5.59**. All three current controllers, one for each phase, are processed in parallel. Additional system parts, like the voltage and voltage symmetry controller, system management, startup state machine, debug interfaces and clock generation for the DPWM,

are also shown. The implementation of the whole system is fully written in very high speed integrated circuit hardware description language (VHDL). To synthesize and fit the implemented controller, the freely available design tools from the vendors are used (ispLEVER starter for implementation C1 and Xilinx ISE Webpack for the implementation C2). Both implementations are running with an internal system clock of 125 MHz.

Implementation of the ADC Interface

According to section 5.6.1, the sampling instants have to be synchronized to the PWM generation. The PWM module therefore generates the start of conversion signal for the ADC.

1) Implementation C1:
The implementation of an SPI interface in an FPGA is relatively simple. The serial data stream has to be deserialized, which can easily be done by a simple shift register. The ADC clock of 31.25 MHz is generated in the FPGA by application of an existing phase-locked loop. In general, there are two possibilities to implement this interface - either the asynchronous ADC clock is used as clock signal for the ADC interface in the FPGA or the ADC signals (clock and data) are synchronized to the internal system clock. In general, multiple clock domains should be avoided in FPGAs whenever this is possible; synchronization is hence the better way. Several fast clock nets are, however, available in the selected FPGA and so the external ADC clock is used as the clock signal for implementation of the ADC interface, which results in a very simple system. Of course, the ADC data has to be synchronized to the system clock after deserialization by application of two D-flip flops.

2) Implementation C2:
In contrast to the very straight forward implementation of the SPI interface of controller C1, the LVDS interface implementation of controller system C2 is much more complex. The ADC interface is implemented according to an application note of Xilinx [221] and it seemed to be straightforward but several issues occurred, which will be discussed in the following. The used Xilinx FPGA offers the capability to drive LVDS signals without any external components. The sampled data is trans-

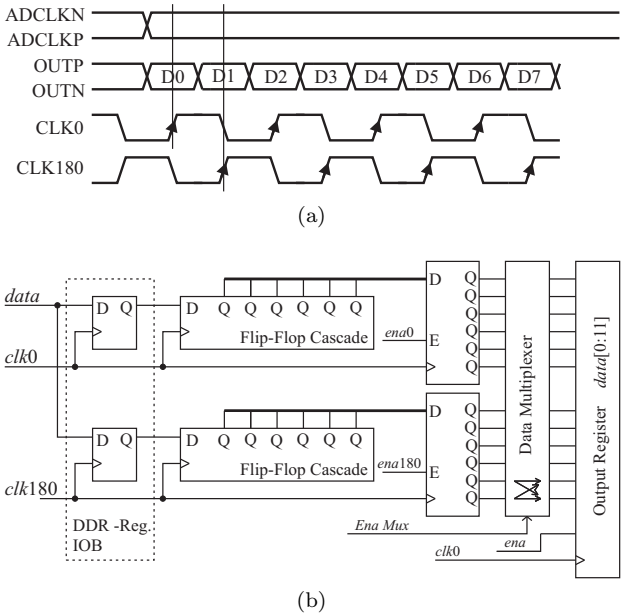


Fig. 5.60: LVDS interface of the ADCs according to [221]; (a) Timing of the interface. The data is sampled at the rising and falling edge of the clock signal and (b) overview of the implementation in the FPGA.

ferred at the rising and falling edge of the differential clock signal (cf. **Fig. 5.60**). To deserialize this serial data stream, the internal DDR input registers (clock signal on positive and negative edges) of the FPGA are used. In this implementation, the ADC ADS5240 runs with a sampling frequency of 25 MHz. This high sampling frequency in conjunction with a resolution of 12 bit results in a serial data rate of 300 Mbit/s. To handle such high data rates inside of the FPGA, care has to be taken with the signal timing. Defined timing and routing constraints are therefore needed for a successful implementation, which requires a detailed knowledge of the FPGA slices. Special attention has to be provided to the generation of the *Ena_Mux* signal, as there, from the FPGAs point of view, the asynchronous signals are matched together to form one data word. The resulting routing of the interface is shown in **Fig. 5.61**.

In an FPGA, data and clock inputs show slightly different delays,

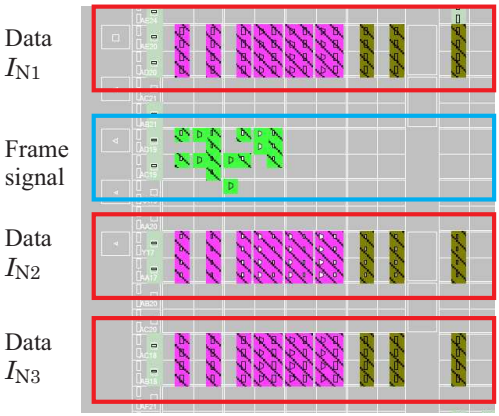


Fig. 5.61: Resulting placement of the ADC interface (current inputs) in the Xilinx FPGA (implementation C2).

TABLE 5.14: Summary of the ADC interface implementation on the FPGAs.

	Slices	$f_{\mathrm{clk,max}}$
C1 (ECP2-LFE2-12E)	43	180 MHz
C1 (XC4VLX25)	47	248.16 MHz

and therefore, the phase of the clock signal has to be adjusted dynamically. Special clock management blocks are available inside of the FPGA for that purpose. But, unfortunately, it has been found that this clock management block does not work well in the desired frequency range although the frequencies still fulfill the specifications. This phase adjustment is therefore not implemented, and as a result, the maximal sampling frequency is limited to 25 MSa/s, although the maximal sampling frequency of the ADC is 40 MSa/s. Compared to the simple SPI interface, the LVDS implementation requires much more detailed knowledge of the used FPGA but offers very high data rates and a reduced delay between sampling instant and availability of the data. A summary of the used logic cells and achieved timing is given in **TABLE 5.14**.

Controller Implementation

The controller given in (5.56) results in the control algorithm

$$\begin{aligned} e[n] &= i_{\text{ref}}[n] - i_{\text{meas}}[n] \\ u[n] &= K(e[n] - k_1 e[n-1]) + k_2 u[n-1] \\ m[n] &= u[n] + d_{\text{ff}}[n] + i_{\text{ff}}[n] \end{aligned} \tag{5.57}$$

where $d_{\text{ff}}[n]$ and $i_{\text{ff}}[n]$ are the voltage and current feedforward parts. There are several possibilities to implement this control algorithm inside of an FPGA. An implementation of a 12×12 bit multiplication using normal logic units of the FPGA is possible, but requires a large number of logic cells and shows a limited timing capability. Alternatively, the multiplications can be avoided by application of shift operators, but then the possibilities of choosing K, k_1, and k_2 are limited. To overcome this limitation, modern FPGAs offer so-called DSP blocks that include hardware multipliers. These multipliers are able to process an 18×18 bit (signed) multiplication in a single clock-cycle and offer additional functionality such as multiplication and addition or multiplication and accumulation. They can run with clock frequencies of over 300 MHz, if all multiplier stages are pipelined. Hardware multipliers are therefore used for the controller implementation. The DSP blocks can be targeted in a number of ways, where the most promising way is provided by upcoming tools, which allow a system design using MATLAB Simulink, and the design is automatically converted into VHDL code. These tools are, unfortunately, currently only applicable for low clock frequencies, and the DSP blocks are therefore directly inferred by VHDL code.

In a first step, after receiving the data from the ADC, it has to be transferred from binary offset to two's complement number representation. This can be done by a simple inversion of the most significant bit of the ADC data word. An 18 bit signed number representation is used in the FPGA because of the 18 bit inputs of the DSP blocks, but the 12 bit range is not extended to 18 bit which has the advantage that no overflows can occur. On the other hand, accuracy is given away. A fractional number representation, as given in **Fig. 5.62(a)**, is used for the controller constants K, k_1, and k_2 and after the multiplication, the remainder is discarded.
The implementation of the controller in an FPGA differs from an implementation in a DSP, as all calculations are processed in parallel in

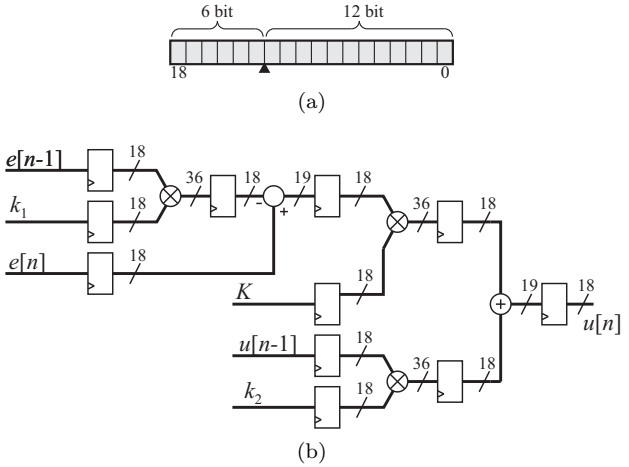


Fig. 5.62: (a) Fractional number presentation of K, k_1 and k_2 in the FPGA and (b) implementation of the P + Lag current controller for one phase in the FPGA using HW multipliers of the FPGA. All the multipliers are pipelined by registers for highest possible throughput.

the FPGA. This does however not mean, that enable signals have to be generated for every block. As an example, the implementation of the P + Lag current controller of (5.57) using the HW multipliers is shown in **Fig. 5.62(b)**. It is very important that all stages are pipelined for a high-frequency implementation. According to **Fig. 5.62(b)**, the controller output $u[n]$ is valid after five clock cycles and it only has to be ensured that the result is not used for PWM generation before these five clock cycles are completed.
As the controller implementation is more or less identical in the two FPGAs, no comparison will be made for this part. The delay of the full current controller is 128 ns for both implementations and is much lower than the calculation time of a DSP implementation (e.g., 1 µs in the implementation presented in [117]).

PWM Generation

A clock frequency of 250 MHz is used for implementation of the DPWM[3]. A higher clock frequency is not possible even with the

[3]Note, that the clock frequency of the other system parts is only 125 MHz.

TABLE 5.15: Summary of the DPWM implementation in the FPGAs.

	Slices	$f_{\mathrm{clk,max}}$
C1 (ECP2-LFE2-12E)	232	253.16 MHz
C1 (XC4VLX25)	712	255.36 MHz

high-speed FPGA of implementation C2.

1) Implementation C1:
The counter/comparator approach without phase shift is used for this implementation. This results in a PWM resolution of only 7 bit at a switching frequency of 1 MHz. The VHDL data-type *std_logic_vector* has to be used for the implementation of the required 7 bit high-speed counters, as much better results can be achieved as using the VHDL data-type *integer*. A separate counter is used for each modulator, which further increases the speed. It has to be said, that a detailed statement about maximal clock frequency of the implementation can only be given if the whole system is fixed by routing constraints; otherwise, the timing is influenced by other system parts. Only timing constraints are used for the implementation at hand and the results are summarized in **TABLE 5.15**.

2) Implementation C2:
The resolution is increased to 8 bit for C2 by implementation of the proposed PWM concept. The 180 ° phase-shifted 250 MHz clock is generated by the DCM of the FPGA. The two phase-shifted modulators have here to be treated as asynchronous signals in the FPGA so that adding timing and routing constraints to the FPGA design is essential. Special attention has to be paid to the connection of the modulators' output to the multiplexer and further on to the output pin, as the multiplexer has no register. This means that different delays of these signal paths directly result in a phase difference of the two PWM signals. There exists no timing constraint to define the same routing delay for several signal paths. Manual placement of the output register and multiplexer has therefore to be done instead. With that, delay differences under 50 ps could be achieved. A drawback of the proposed PWM concept is that glitches of the multiplexer can occur. But, in

TABLE 5.16: Report summary of the controller implementations.

	C1 (ECP2-LFE2-12E)	**C2** (XC4VLX25)
DSP-block utilization	87 %	68 %
Logic utilization	25 %	10 %
Clock management	50 %	40 %
I/O Pins	41 %	8 %

the desired application, several "slow" components (optocoupler, gate driver) would "absorb" these glitches. The duty cycle can be updated twice a period for lower switching frequencies (e.g., $f_s = 500\,\text{kHz}$), to minimize the delay of the PWM modulator.

Summary of the Implementation

The two designs have been successfully fitted into the two FPGAs. A summary of the report is given in **TABLE 5.16**. The utilization of the DSP blocks (one DSP block contains several multipliers) of 68 % and 87 % means, in practice, nearly a full usage, as there are some mapping limitations of the multipliers into the DSP blocks that inhibit a usage of 100 %. In contrast to the utilization of the DSP blocks, only a small amount of the available logic cells and I/O pins are used for the controller implementation. This clearly illustrates that the speed of the FPGA is needed and not its size.

The resulting timings of the implementations for a switching frequency of 1 MHz are depicted in **Fig. 5.63**. The biggest part of the processing time is the ADC delay, even if a pipelined ADC with a sampling frequency of tens of megahertz is used. The second largest part of delay is introduced by the controller implementation caused by pipelining of all the multiplier stages. According to **Fig. 5.63(b)**, the controller implementation C2 is able to handle switching frequencies up to 2 MHz.

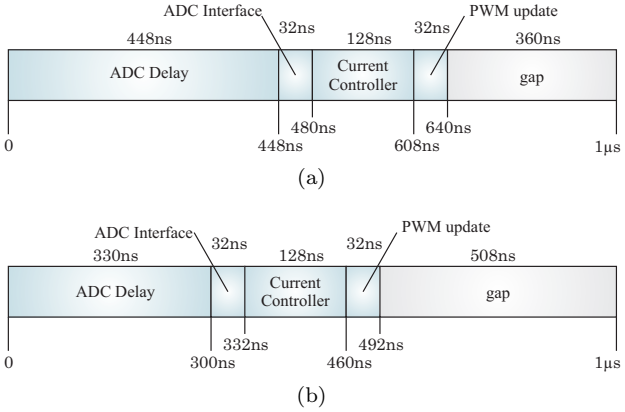
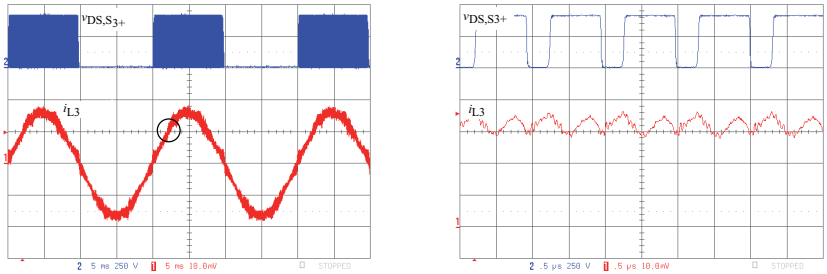


Fig. 5.63: Resulting timings of (a) current controller implementation C1 and (b) current controller implementation C2 for a switching frequency of 1 MHz.

5.6.3 Experimental Results

The designed high-speed controller is tested using the constructed hardware prototype with a switching frequency of 1 MHz (cf. section 5.8). Due to the large effort to build the controller hardware for the three-phase VR prototype only controller implementation C1 is used. Six ADCs are required for input current and input voltage measurement. The PWM is operating with single update mode and the current controller is implemented with the parameters $K = 0.25$, $k_1 = 0.96$ and $k_2 = 0.99$. Detailed measurements of the VR system will be given in section 5.9.

Measurements of the ripple of the inductor current i_{L3} and the drain-source voltage of switch S_{3+} are shown in **Fig. 5.64**. The switch S_{3+} is only modulated at positive input currents and is permanently on at negative input currents. As is typically the case for three-phase rectifier systems, the current ripple is not only affected by the switching actions of the corresponding phase, but also by the switching actions of the two other phases. This results in a current ripple which shows in addition to the spectral components at switching frequency also substantial harmonics at multiples of the switching frequency. According to **Fig. 5.64(b)**, the duty cycle of the switch S_{3+} does not vary significantly as it may be the case for a malfunction controller or PWM



(a) (b)

Fig. 5.64: Measurements taken from the implemented VR laboratory prototype employing controller implementation C1. (a) Drain-Source voltage $v_{\mathrm{DS,S3+}}$ and corresponding inductor current i_{L3} at $f_{\mathrm{N}} = 50\,\mathrm{Hz}$ and $P_{\mathrm{o}} = 4.2\,\mathrm{kW}$; Ch1: 5 A/Div, Ch2: 250 V/Div; timebase: 5 ms/Div. (b) Detail of current ripple Ch1: 2 A/Div, Ch2: 250 V/Div; timebase: 500 ns/Div. As typically for three-phase rectifier systems, the current ripple is not only affected by the switching actions of the corresponding phase, but also by the switching actions of the two other phases.

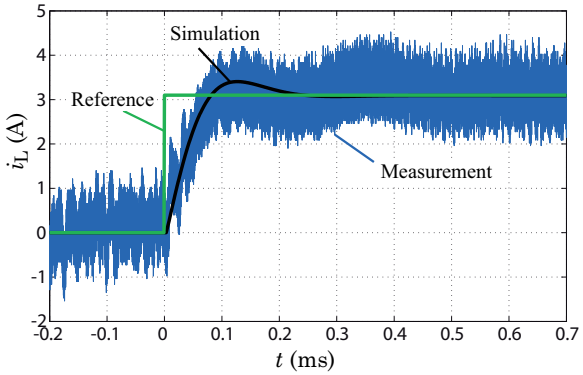


Fig. 5.65: Measured step response for controller implementation C1 to a reference current step of 3 A compared to the simulated step response.

implementation, thus confirming the proper operation of the controller.

In **Fig. 5.65**, the measured inductor current control step response to a reference value step of 3 A is shown together with the simulated quantity. Please note that due to $i_{\mathrm{N1}} + i_{\mathrm{N2}} + i_{\mathrm{N3}} = 0$ also steps

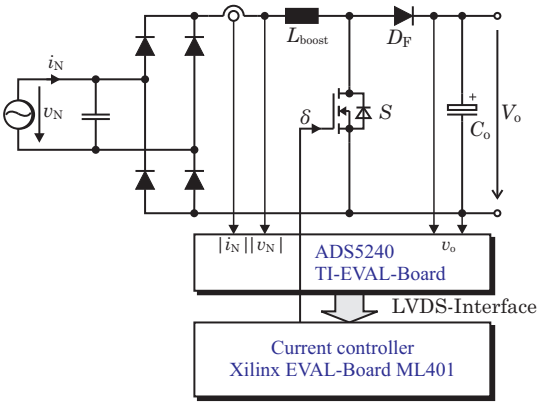
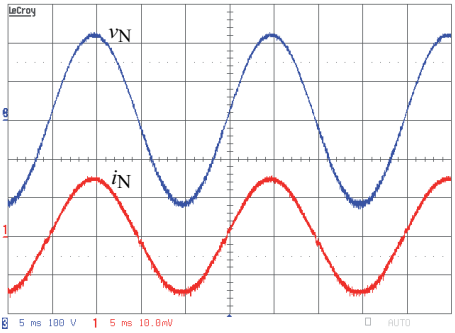


Fig. 5.66: Structure of the single-phase test system for controller implementation C2.

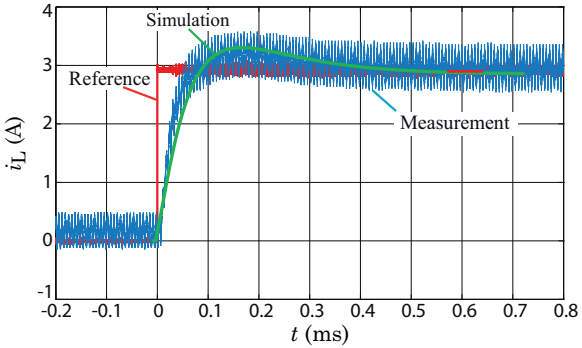
with -1.5 A on the two other phases have to be applied. The current reference of the three-phase current controller signal is created by a step in the conductance G_e^*, which, in normal operation, is modulated by the much slower output voltage controller. The step responses are in good agreement, but the measured current shows slightly underdamped behavior.

Controller Implementation C2:
As mentioned earlier, controller implementation C2 was not used for the final hardware prototype. In order to test the controller implementation C2, an existing single phase PFC prototype with the following key specifications was used in combination with the TI-evaluation board ADS5240 (implementation of ADCs with LVDS interface) and the Xilinx evaluation bard ML401 employing the Virtex4 FPGA (cf. **Fig. 5.66**):

- input voltage: $V_N = 230\,V$;
- input frequency: $f_N = 50/60\,Hz$;
- output voltage: $V_o = 400\,V$;
- output power: $P_o = 3\,kW$;
- switching frequency: $f_s = 150\,kHz$;
- boost inductance: $L_{boost} = 200\,\mu H$.



(a)



(b)

Fig. 5.67: Measurements taken from the single-phase PFC employing the controller implementation C2. (a) Input current and input voltage at a line frequency of $f_N = 50\,\text{Hz}$ and a power level of $P_o = 1.5\,\text{kW}$; Ch1: 5 A/Div, Ch3: 100 V/Div; timebase: 5 ms/Div. (b) Measured response of the inductor current to a reference value step of 3 A compared to the simulated step response of the current controller.

The controller structure of implementation C2 has not been changed for that purpose; only, the internal clock frequencies have been reduced to handle the lower operating frequency. According to section 5.6.2, timing analysis of the implementation C2 using the Xilinx design tools verified that an implementation is possible employing the Virtex4 FPGA for switching frequencies up to 2 MHz. The implemented system is, however, tested with a switching frequency of 150 kHz. A measurement of the input current at $P_o = 1.5\,\text{kW}$ is plotted in **Fig. 5.67(a)**.

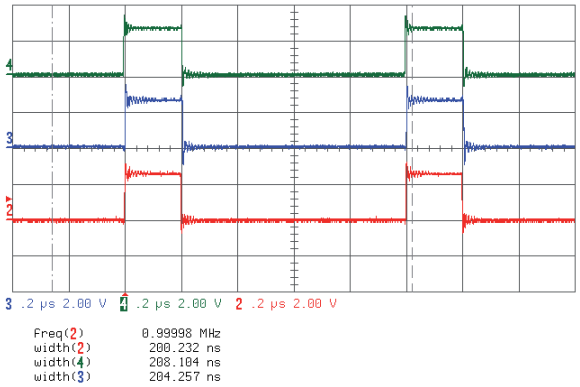


Fig. 5.68: Measurement result of the proposed DPWM concept with a PWM frequency of 1 MHz and the PWM-values: Ch2 (2 V/Div): $m = 50$ (200 ns); Ch3 (2 V/Div): $m = 51$ (204 ns) and Ch4 (2 V/Div): $m = 52$ (208 ns); timebase: 200 ns/Div.

In **Fig. 5.67(b)**, the measured step response of the current controller is compared to the simulated step response of the designed current controller, where both responses are in good agreement.

The behavior of the proposed DPWM is tested using the evaluation board. The PWM has a frequency of 1 MHz and all three PWM channels are programmed for test purposes to a fixed duty cycle only differing in 1 bit. According to **Fig. 5.68**, a modulator value of $m = 50$ results in a pulse-width of 200 ns for an 8 bit PWM with a maximum counter value of 125. A modulator value of $m = 51$ results in a pulse-width of 204 ns, and for $m = 52$, a pulse-width of 208 ns can be measured. This confirms that a symmetrical PWM with a resolution of 4 ns has been implemented.

5.6.4 Discussion

In this section the successful implementation of a digital current controller for a three-phase rectifier system operating at 1 MHz has been shown. The entire signal chain, starting with the current measurement and ending with the PWM generation has been considered.

The way to minimize the delay introduced by the ADC has been shown by application of two different high-speed ADC implementations. Implementation C1 uses a converter with a sampling frequency of 1 MHz and a well-known SPI interface that results in an effective delay of 448 ns. In contrast, implementation C2 uses a high-speed converter with $f_{\text{sample}} = 25\,\text{MHz}$ and a high-speed LVDS-interface reduces this delay to 300 ns. The implementation of this high-speed interface is, however, much more complex and should only be used in cases where the SPI interface is not applicable anymore.
One limitation for a high-speed controller implementation is the generation of a symmetrical high-speed PWM signal. In this work, an enhanced DPWM generator with a resolution of 4 ns (7 bit at $f_{\text{s}} = 1\,\text{MHz}$) with symmetrical pulse patterns is developed, which is based on a phase-shifted counter/comparator approach. Timing and routing constraints need to be considered for a successful implementation in an FPGA, which, in turn, may require detailed knowledge of FPGA design. If a higher PWM frequency has to be implemented special developed integrated PWM chips would be required as the emerging concepts for implementation of the PWM are not directly applicable in a commercial FPGA.
The implemented controller shows, however, very good performance as illustrated in section 5.9 and is a good solution for the intended switching frequency of 1 MHz.

The question arises if it is really necessary to have the current controller output updated with the switching frequency of 1 MHz, or if a current controller operating at 500 kHz combined with a switching frequency of 1 MHz (PWM output updated every second period) would be sufficient. On first view, it seems that the calculated controller bandwidth is more than enough for a 50 Hz line frequency. Simulations, however, show that the current ripple would be approximately 10 % higher for a 500 kHz current controller, and therefore, the size of the boost inductor and of the EMI filter has to be increased in order to fulfill the given design specifications. Also a larger delay time is introduced in the control loop from the control point of view if the PWM modulator is updated every second period. The phase margin of the control loop is therefore reduced from 45 ° to 36 °. In order to achieve the same phase margin as the controller with an update rate of 1 MHz, the controller gain has to be reduced approximately by a factor of two. This

was tested on the existing prototype at an output power level of 4.1 kW and the THD_I increased from 2.2 % (update rate 1 MHz) to 3.1 % when the output was updated with 500 kHz. One has hence to be aware, that a combination of a switching frequency of 1 MHz at a controller update of 500 kHz results in higher switching losses and a reduced input current quality but, however, a somewhat lower EMI filter volume could be expected. If a high switching frequency is to be implemented, the current controller should be fast enough to benefit from the high switching frequency.

5.7 EMI Filter Design

Active three-phase rectifiers show a large high frequency noise level and require a proper EMI filter. Passive low-pass filters employing inductors and capacitors in connection with resistors providing passive damping can be used to attenuate resulting conducted emissions (CE) of the systems [222, 223, 175]. These passive filter elements take up a relatively large portion of the overall system volume and can be reduced in size only by increasing the switching frequency.

It is common and very helpful for filter design to split the generated EMI emissions into a common mode (CM) and into a differential mode (DM) component. Whereas DM noise currents flow in and out through the phases, CM currents return via earth. Different filter strategies and filter elements have hence to be applied to handle the two emission types. As will be shown in section 5.7.1, asymmetrical currents to earth caused by asymmetrical impedances of the rectifier system also generate DM noise. These type of emissions are called "non intrinsic differential mode noise" [224] or "mixed-mode noise" (MM) and their origin was analyzed in [225, 226] for single-phase flyback converters. MM noise in three-phase diode front-end converters was discussed in [227, 228].

The performance of the DM filter can be well predicted and, dependent on the required attenuation, multi-stage LC-filters are usually applied [229]. Also "Zero-ripple" DM filter concepts have been proposed [230]. On the contrary, CM noise currents are mainly determined by parasitic elements such as capacitances of semiconductors to the heat sink, capacitances between heat sink and earth, magnetic couplings of inductors, etc., and are therefore difficult to identify and quantify.
In [231, 232], a CM noise modeling technique for single-phase PFC systems was proposed which considers these parasitic capacitances. Several works on three-phase systems were also published [233, 234] where some insights into CM noise sources and propagation paths in three-phase systems are given. These papers, however, only include limited information and guidelines for final EMI filter design.

In this work the CM noise modeling technique for single-phase PFC [231, 232] will be extended to three-phase systems and an EMI filter design and implementation for an ultra-compact three-phase/level VR

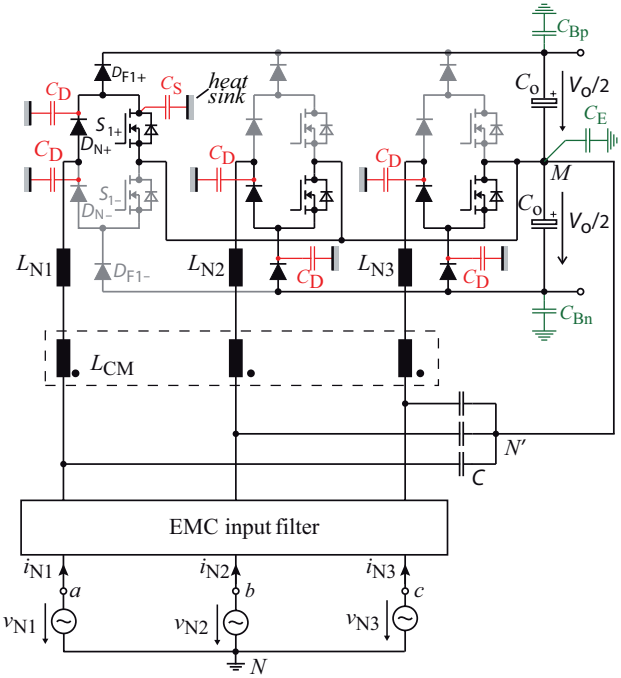


Fig. 5.69: Schematic of the three-phase/level VR including relevant parasitic capacitances from semiconductors to heat sink (C_S, C_D) and from the DC output rails to earth (C_{Bp}, C_{Bn} and C_E) for $i_{N1} > 0$, $i_{N2}, i_{N3} < 0$. In addition, the proposed CM voltage reduction concept is shown, where the output voltage midpoint M is connected to an artificial mains star point N'. High-frequency CM currents are limited by a three-phase CM inductor L_{CM}.

[81] will be discussed (cf. **Fig. 5.69**, where the parasitic capacitances relevant for $i_{N1} > 0$, $i_{N2}, i_{N3} < 0$ are shown).
The formation of the CM voltage was analyzed in detail in [101] but for sake of simplicity only a single lumped capacitor from the output voltage midpoint M to earth was used to model the CM current paths. This is a reasonable approach to get an overview of the CM behavior of a system but proved to be insufficiently accurate for designing the EMI filter. Based on the modeling technique considering parasitic capacitances of the semiconductors to the heat sink and from the output voltage rails to earth a more detailed CM model will be developed in section 5.7.1.

In [101] also a concept for minimizing the high-frequency CM emis-

sions was proposed (further concepts can be found in [235]). The output voltage midpoint M is connected to an artificial mains star-point N' formed by three filter capacitors C. Whereas the low-frequency CM voltage, used to increase the input voltage range of the rectifier, drops across the capacitors C, all high frequency CM output voltage components are attenuated by the low-pass filter action of the boost inductors $L_{\mathrm{N}i}$ and the capacitors C. This concept, unfortunately, results in a considerably increased ripple of the boost inductor currents or in higher copper and core losses or both. The basic concept therefore advantageously is extended according to [236] by placing a three-phase CM inductor L_{CM} in series to the boost inductors $L_{\mathrm{N}i}$ which considerably reduces the additional high-frequency current ripple.

5.7.1 Converter Noise Model

The semiconductors of a power electronics converter are typically mounted on a common heat sink which is usually connected to earth and parasitic capacitances to earth therefore exist. In order to fully understand the propagation of the resulting CM noise currents these capacitances have to be considered and/or a detailed CM noise model has to be derived. First of all, however, a review on noise components in three-phase systems shall be given.

Review on Three-Phase Noise Components

Separation of CM and DM noise in three-phase systems is not easily possible. Orthogonal transformations as reported in [237, 238] can be applied but these transformations are only valid if the three-phase system is symmetrical, linear and time-invariant. Regardless of the intended three-phase system and its noise sources the CM current can be defined as the current flowing out through the phases and returning via earth. The CM current is hence the sum of all three phase currents

$$i_{\mathrm{CM}} = i_1 + i_2 + i_3 \ . \tag{5.58}$$

The DM currents on the other hand can be defined as the currents flowing out through one phase and returning through the two other phases which implies $i_{\mathrm{DM},1}+i_{\mathrm{DM},2}+i_{\mathrm{DM},3} = 0$. A general high-frequency noise model of a three-phase system is given in **Fig. 5.70**, where the LISN is modeled as three $50\,\Omega$ resistors. In addition to the DM noise

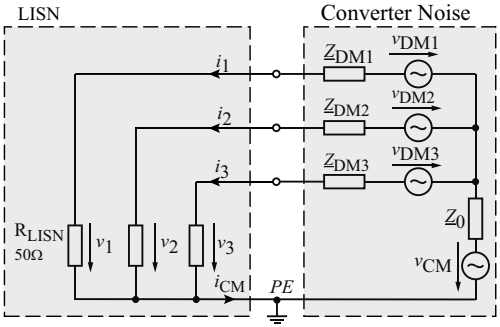


Fig. 5.70: High frequency noise model of a three-phase rectifier system connected to a three-phase LISN.

sources $v_{\mathrm{DM},i}$ and their source impedances $\underline{Z}_{\mathrm{DM},i}$ the CM noise source v_{CM} is also shown together with a single lumped impedance to earth $\underline{Z}_0$. This model implies that the propagation paths of the DM and CM currents can be separated - which may not be true in each case. If current and voltage signals at the interconnections of the System Under Test (SUT) to the LISN are considered, the definition of (5.58) is still valid even if coupled noise propagation paths exist. The CM voltage at the LISN can be calculated as

$$v_{\mathrm{CM}} = i_{\mathrm{CM}} \frac{R_{\mathrm{LISN}}}{3} \;=\; \frac{v_1 + v_2 + v_3}{3} \tag{5.59}$$

where R_{LISN} is the input resistance of the LISN. By using (5.59) the DM voltage component of phase 1 can be calculated to

$$v_{\mathrm{DM},1} = v_1 - v_{\mathrm{CM}} \;=\; \frac{2v_1}{3} - \frac{v_2}{3} - \frac{v_3}{3}\ . \tag{5.60}$$

If a symmetrical distribution of the CM current i_{CM} on the three phases is assumed each phase current can be written as

$$i_i = i_{\mathrm{DM},i} + \frac{i_{\mathrm{CM}}}{3}\ . \tag{5.61}$$

Note that some authors, e.g. [225], define the CM current based on $i_i = i_{\mathrm{DM},i} + i_{\mathrm{CM}}$ which results in a current to earth of $3i_{\mathrm{CM}}$ instead of i_{CM}. If, unlike in **Fig. 5.70**, the impedances of the three phases to earth differ, the CM current distribution in the three phases is also not equal.

Let Δi be the deviation of the CM current in phase number 1 to the current i_0 of the two other phases. According to (5.58) the resulting CM current is given by $i_{\mathrm{CM}} = 3i_0 + \Delta i$. The input currents can therefore be written as

$$\begin{aligned} i_1 &= i_{\mathrm{DM},1} + \frac{i_{\mathrm{CM}}}{3} + \frac{2\Delta i}{3} \\ i_2 &= i_{\mathrm{DM},2} + \frac{i_{\mathrm{CM}}}{3} - \frac{\Delta i}{3} \\ i_3 &= i_{\mathrm{DM},3} + \frac{i_{\mathrm{CM}}}{3} - \frac{\Delta i}{3} \end{aligned} \tag{5.62}$$

which yields to the CM voltage

$$v_{\mathrm{CM}} = R_{\mathrm{LISN}} \left(i_0 + \frac{\Delta i}{3} \right). \tag{5.63}$$

By subtracting the CM voltages from the according phase voltages $v_{\mathrm{DM},i} = v_i - v_{\mathrm{CM}}$ the DM voltages result in

$$\begin{aligned} v_{\mathrm{DM,MM},1} &= R_{\mathrm{LISN}} \left(i_{\mathrm{DM},1} + \frac{2\Delta i}{3} \right) \\ v_{\mathrm{DM,MM},2} &= R_{\mathrm{LISN}} \left(i_{\mathrm{DM},2} - \frac{\Delta i}{3} \right) \\ v_{\mathrm{DM,MM},3} &= R_{\mathrm{LISN}} \left(i_{\mathrm{DM},3} - \frac{\Delta i}{3} \right) \end{aligned} \tag{5.64}$$

which show, in comparison to (5.60), an additional part caused by the unequally distributed CM currents. Unbalanced CM noise hence also causes DM noise and this supplementary DM noise is called "non-intrinsic DM noise" or "mixed mode noise". The applied definition of the CM current offers an explanation of the phenomenon of non-intrinsic DM noise, whereas the model with $i_{\mathrm{Earth}} = 3i_{\mathrm{CM}}$ can not explain it without introducing an additional noise source.

Derivation of Noise Model

In the following, the modeling approach given in [231, 232] for single-phase PFC will be extended to three-phase systems.

In **Fig. 5.69**, the relevant parasitic capacitors between semiconductors and heat sink are drawn for $i_{\mathrm{N1}} > 0$, $i_{\mathrm{N2}}, i_{\mathrm{N3}} < 0$. The capacitors

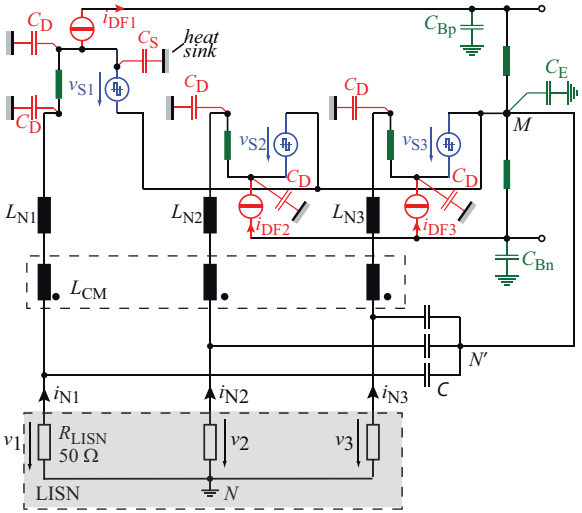


Fig. 5.71: High-frequency equivalent circuit if the operated switches are replaced by voltage noise sources and the corresponding free-wheeling diodes are replaced by current noise sources. Model is valid for $i_{N1} > 0$, $i_{N2}, i_{N3} < 0$.

C_S and C_D represent the stray capacitance of a MOSFET's drain and a diode's cathode to the heat sink which is approximately 60 pF for the applied TO220 package. These capacitances are present for all semiconductors of the rectifier system, but capacitors of circuit paths which are not carrying current in $-30° < \varphi_N < 30°$ are not shown. The capacitors C_{Bp} and C_{Bn} model the stray capacitances of the positive and negative output voltage rail to earth. The capacitor C_E models the parasitic capacitance of the output voltage midpoint to earth but also includes possible parasitic capacitances of the load. The capacitance of C_E can therefore be quite large, e. g. several nF. In order to develop a high-frequency CM model of the circuit the MOSFETs are replaced by voltage sources $v_{ri,M}$, which are impressing the switched voltage waveforms. In a similar manner the diodes D_{F1+}, D_{F2-} and D_{F3-} are replaced by current sources showing the same pulsed current waveform as occurring in the actual diodes. The impedance of the output capacitor C_o, implemented partly with ceramic capacitors, is very small at switching frequency and therefore modeled as a short-circuit. The corresponding mains diodes D_{N+}/D_{N-} are permanently on during a half mains period

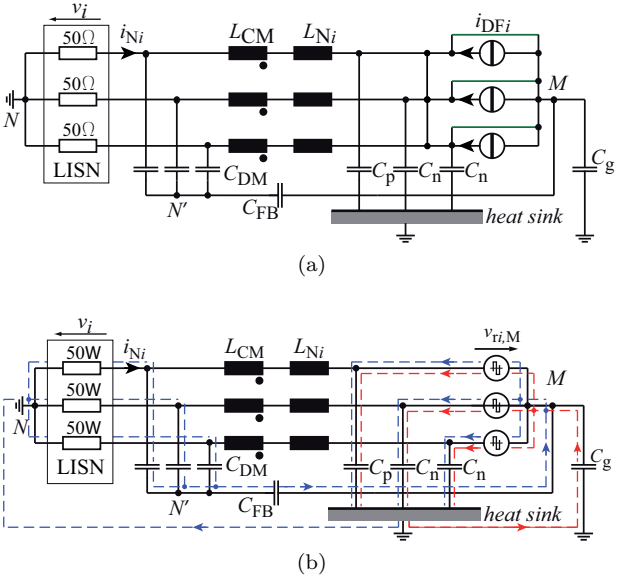


Fig. 5.72: Detailed noise models valid for $i_{N1} > 0$, $i_{N2}, i_{N3} < 0$ if the heat sink is connected to earth if (a) only noise current sources and (b) only noise voltage sources are considered. In (b) only current paths involving the parasitic capacitors C_p and C_n are shown.

and are hence also replaced by a short-circuit. The resulting equivalent circuit is given in **Fig. 5.71**. As the rectifier system is modeled by linear elements the influence of the noise sources can be analyzed by application of the superposition principle. In **Fig. 5.72(a)** the corresponding noise model is drawn if only current noise sources are considered. It is obvious that the current sources are shorted by the low impedance paths established by the output capacitors and that they do not contribute to the noise measured in the LISN.
If only noise voltage sources are considered, the equivalent circuit given in **Fig. 5.72(b)** can be derived.

The phase leg with positive input current (i_{N1}) shows a total capacitance of $C_p = 2C_D + C_S$ to the heat sink and the phase-legs with negative input currents (i_{N2} and i_{N3}) show a total capacitance of $C_n = 2C_D$ which is different to C_p. Note that this model is only valid for $i_{N1} > 0$, $i_{N2}, i_{N3} < 0$, i.e. $-30° < \varphi_N < 30°$, and that the capacitance

of C_p and C_n is changing if one of the input phase currents changes its sign, i.e. every 60°. The capacitor C_g models all capacitances from the output voltage rails and the output voltage midpoint to earth ($C_\mathrm{g} = C_\mathrm{E} + C_\mathrm{Bp} + C_\mathrm{Bn}$). The detailed function of the CM filtering based on a connection of M with N' will be discussed later. Note that the voltage sources $v_{\mathrm{r}i,\mathrm{M}}$ include DM emissions as well as CM emissions. In **Fig. 5.72(b)** only current paths involving the parasitic capacitors C_p and C_n are shown.
Different possibilities for defining the heat sink potential exist and the most important ones will be discussed shortly as they result in different CM behavior.

1) Heat sink connected to the output voltage midpoint M:
If the heat sink is connected to M, C_p and C_n lie in parallel to the voltage sources. The noise currents through them are guided directly back to the noise source and thus no additional external CM noise occurs. This is the best option from the EMI perspective but one must keep in mind that M will show a low-frequency CM voltage of a few 100 V if a third harmonic injection signal is applied and this may, depending on the application, not be permitted.

2) Heat sink connected to earth:
In many applications the heat sink has to be connected to earth due to safety reasons. The largest impact on the noise emissions can then be observed. According to **Fig. 5.72(b)** the three phases show different capacitances to earth and therefore a separation into CM and DM equivalent circuits is not directly possible. These unequal impedances to earth result in an unbalanced CM current distribution of the three phases which finally yields to non-intrinsic DM emissions as shown before. These non-intrinsic DM emissions are not analyzed further in this work but are subject to further research on this topic.
If the parasitic capacitors are assumed to be equal an equivalent circuit with separated CM and DM emissions can be drawn. This will be further discussed in section 5.7.2.

3) Heat sink floating:
If the heat sink is floating, it would show a parasitic capacitance to earth of a few pF. This parasitic capacitance is now connected in series to the capacitances C_p and C_n. As this parasitic capacitance is typically

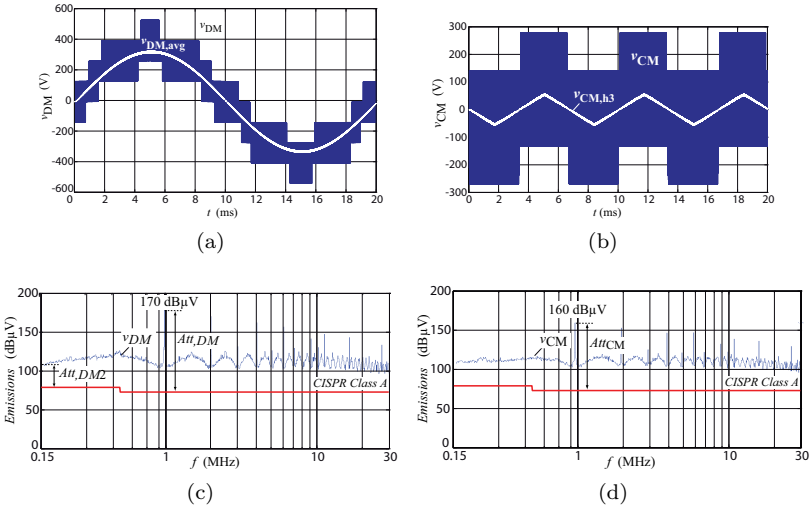


Fig. 5.73: Simulated voltage waveforms of the rectifier system operated at an output power of $P_o = 10\,kW$ and corresponding predicted EMI noise spectra using peak-detection; (a) DM voltage; (b) CM voltage; (c) Predicted DM emission and (d) predicted CM emission.

much smaller than C_p and C_n, the resulting total capacitances to earth are almost equal and an equivalent circuit with separated CM and DM emissions can be drawn. Please note, that the (equal) capacitance values of the equivalent circuit with floating heat sink are therefore much smaller than the capacitance values of a heat sink directly connected to earth.

5.7.2 Filter Design

In order to design a proper EMI filter the CM and DM noise levels of the three-phase rectifier system are required. A computer simulation is used to determine the DM and CM voltage waveforms (cf. **Fig. 5.73**) generated by the rectifier system ($f_s = 1\,MHz$, $V_N = 230\,V$, $f_N = 50/60\,Hz$, $V_o = 800\,V$ and $P_o = 10\,kW$). It has to be stated here, that different modulation strategies result in different CM and DM voltage waveforms which would finally lead to different EMI filter requirements. A third harmonic triangular signal according to (3.17) is added to the sinusoidal phase voltage reference values in order to increase the input

voltage modulation range which results in a triangular low-frequency component ($v_{\mathrm{CM,h3}}$) of the CM voltage (cf. **Fig. 5.73(b)**).

According to the calculation scheme given in [229] the Quasi-Peak (QP) or Peak (PK) weighted DM and CM spectrum can be calculated. The calculated PK weighted spectra of the voltages shown in **Fig. 5.73**a,b are depicted in **Fig. 5.73(c,d)**, together with the limit defined by CISPR11 class A [239]. The results of this calculation are the spectra of the simulated voltage waveforms where the PK characteristic of the detector is included but, contrary to [229], the influence of the LISN is not considered. The EMI filter must now be designed such that the noise emissions do not exceed the CISPR11 class A limit. The impedances of the LISN must be considered later in the EMI filter design process.

According to **Fig. 5.73**, the main amplitudes of harmonics occur at multiples of the switching frequency. The required attenuation of the DM and CM filter can therefore be calculated by comparing the simulated emissions with the limit specified in CISPR11. This results in a required attenuation of

$$\begin{aligned} A_{\mathrm{DM}}[\mathrm{dB}] = v_{\mathrm{DM}}(f_{\mathrm{s}})[\mathrm{dB\mu V}] - \mathit{Limit}[\mathrm{dB\mu V}] \\ + \mathit{margin}[\mathrm{dB}] \cong 103\,\mathrm{dB}\ , \end{aligned} \tag{5.65}$$

for the DM filter where a margin of 6 dB is included. The required attenuation of the CM filter can be calculated as

$$\begin{aligned} A_{\mathrm{CM}}[\mathrm{dB}] = v_{\mathrm{CM}}(f_{\mathrm{s}})[\mathrm{dB\mu V}] - \mathit{Limit}[\mathrm{dB\mu V}] \\ + \mathit{margin}[\mathit{dB}] \cong 93\,\mathrm{dB}\ . \end{aligned} \tag{5.66}$$

The process employed for calculating the noise spectra is a time-consuming task. The result of this calculation are noise amplitudes over the whole frequency range. However, as shown above only the amplitude of the emissions generated at the switching frequency is used for EMI filter design (in case of $f_{\mathrm{s}} \geq 150\,\mathrm{kHz}$). In [240] an approximation method for determining the EMI emission has been presented, where only the DM component at the switching frequency is considered. All switching frequency harmonics with higher order are merged into this "fundamental" component at switching frequency. This method, however, can also be applied to determine the CM filter requirements. The rms value of the CM voltage $V_{\mathrm{CM,rms}}$, which comprises a low-frequency component

$V_{\mathrm{CM,h3,rms}}$ and a high frequency component $V_{\mathrm{CM,noise,rms}}$ containing all switching frequency harmonics, must therefore be calculated. This could be done purely analytically but for the sake of simplicity the rms value of the total CM voltage is determined using the simulated CM voltage shown in **Fig. 5.73(b)**. The rms value of the high-frequency CM noise $V_{\mathrm{CM,noise,rms}}$ is therefore given as

$$V^2_{\mathrm{CM,noise,rms}} = V^2_{\mathrm{CM,rms}} - V^2_{\mathrm{CM,h3,rms}} \tag{5.67}$$

which finally yields

$$V^2_{\mathrm{CM,noise,rms}} = V^2_{\mathrm{CM,rms}} - \frac{\left(\frac{\hat{V}_{\mathrm{N}}}{4}\right)^2}{3} \tag{5.68}$$

and an estimated noise level of

$$V_{\mathrm{CM,noise,rms}} = 164\,\mathrm{dB\mu V}\ . \tag{5.69}$$

The difference to the result given in **Fig. 5.73(d)** is only $4\,\mathrm{dB}\mu\mathrm{V}$ and therefore, the proposed procedure is a very reasonably accurate and simple method to estimate the EMI filter requirements.

According to **Fig. 5.73**c,d a relatively large noise floor of $\approx 110\,\mathrm{dB}$ is generated by the rectifier system. The reason for this can be found in the time behavior of the DM and CM voltages. As reported in [241,242,243] carrier sideband harmonics are present in the spectrum of a PWM signal with low-frequency local average. This leads to an increased noise floor which has to be considered in the DM filter design. The DM filter has therefore to reach an attenuation of at least

$$\begin{aligned} A_{\mathrm{DM2}}[\mathrm{dB}] = {} & v_{\mathrm{DM}}(150\,\mathrm{kHz})[\mathrm{dB\mu V}] - \mathit{Limit}[\mathrm{dB\mu V}] \\ & + \mathit{margin}[\mathrm{dB}] \cong 37\,\mathrm{dB} \end{aligned} \tag{5.70}$$

at the lower frequency limit for conducted emissions measurements, i.e. at 150 kHz. At least one filter stage has to be designed such that the required attenuation at 150 kHz is achieved. This means the volume of this filter stage can not be reduced by a high switching frequency. Among other limitations, such as the lack of available high frequency magnetic materials, this is a main limitation of EMI filter volume reduction by increasing the switching frequency.

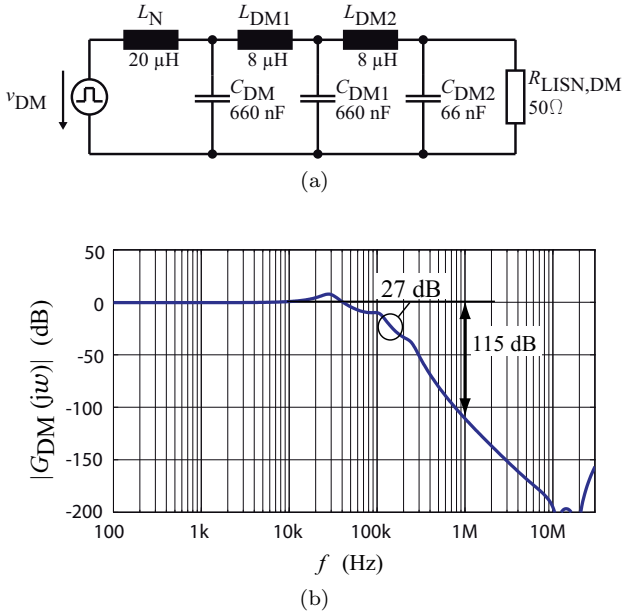


Fig. 5.74: (a) Equivalent single-phase DM model and (b) calculated transfer function $G_{\mathrm{DM}}(\mathrm{j}\omega)$ of the designed DM filter.

DM Filter Design

In addition to the required filter attenuation for DM filter design the phase displacement of the mains currents resulting from the currents drawn by the filter capacitors must also be considered. If the maximum phase displacement should be limited to 10° at an output power of $0.1P_{\mathrm{o}}$, the DM filter capacitors here are limited to a total capacitance of $C_{\mathrm{DM}} = 3.5\,\mu\mathrm{F}$ per phase.

According to the specifications given in (5.65) and (5.70) an LC-filter with three stages is used for construction of the DM filter. The single-phase equivalent circuit of the DM filter is shown in **Fig. 5.74(a)**. The boost inductor of the rectifier represents the first filter stage. The inductance value of the boost inductor is defined by the maximum allowed current ripple. A maximum allowed current ripple of $\Delta i_{\mathrm{L,pp}} = 0.2\hat{I}_{\mathrm{N,i}}$ is defined for the implementation at hand, which results in an inductance of $L_{\mathrm{N}i} = 20\,\mu\mathrm{H}$. In [244] it was shown that a maximum attenuation

for a multi-stage LC-filter can be achieved if all inductance values and all capacitance values are equal, which also implies that the cut-off frequencies of all filter stages are identical. Unfortunately, (5.65) as well as (5.70) must be satisfied, and the cut-off frequency of the filter for the case at hand has to be designed according to (5.70) which increases the total filter volume as at least one filter stage has to implement a specific amount of damping at 150 kHz. This concept shows in addition the problem of multiple equal filter resonance frequencies which have to be damped. The cut-off frequencies of the filter stages are hence selected in a distributed manner and the resulting filter components are chosen also considering aspects of practical implementation. This will be discussed further in section 5.7.3. The calculated transfer function $G_{\mathrm{DM}}(\mathrm{j}\omega)$ of the designed filter is depicted in **Fig. 5.74(b)**.

CM Filter Design

In a first design step of the CM filter the influence of the parasitic capacitors C_{p} and C_{n} (cf. **Fig. 5.72**) is neglected. Safety regulations must be considered in the selection of CM capacitors where the leakage earth current is limited to a few mA. This results in a limited total capacitance connected to earth which fundamentally influences the CM filter design. If a conventional multi-stage LC low-pass filter would be implemented at least three stages would be necessary whilst the large CM component of V_{o} would still be present. By connecting the output voltage midpoint M to an artificial star-point N' as shown in **Fig. 5.69**, the CM component of the output can, however, be reduced significantly without violating the safety regulations. The capacitors C_{DM} of the first DM filter stage can be used advantageously to form N'. An equivalent circuit of the proposed CM filter concept is shown in **Fig. 5.75(a)**. The converter voltage $v_{\mathrm{v},i}$ there is split into a DM voltage $v_{\mathrm{DM},i}$ and a CM voltage v_{CM}

$$v_{\mathrm{r}i,\mathrm{M}} = v_{\mathrm{DM},i} + v_{\mathrm{CM}} \tag{5.71}$$

where the CM voltage

$$v_{\mathrm{CM}} = v_{\mathrm{CM},\sim} + v_{\mathrm{CM,h3}} \tag{5.72}$$

comprises a high frequency component $v_{\mathrm{CM},\sim}$ and a low-frequency component $v_{\mathrm{CM,h3}}$ which represents the third harmonic injection mentioned above. The CM filter path is implemented by a capacitor C_{FB} in series

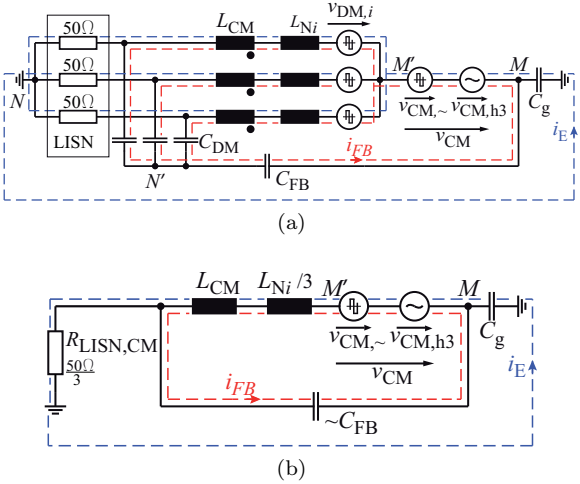


Fig. 5.75: (a) Conducted noise equivalent circuit of the three-phase/level VR system for the proposed CM filter concept if C_p and C_n are neglected; (b) simplified CM equivalent circuit.

to the DM capacitors forming N'. In addition, the capacitance C_g, representing the lumped capacitance between M and earth, is shown which is significantly influenced by the load. If this parasitic capacitance is neglected for a first analysis, the generated CM voltage appears across circuit L_{Ni}, L_{CM} and the series connection of the capacitors C_{FB} and C_{DM}. The capacitors C_{FB} and C_{DM} are not connected to earth and are therefore not limited in capacitance by equipment safety regulations. The construction of a CM inductor which is able to handle the third harmonic voltage component $v_{CM,h3}$ without saturation is possible but would result in a very large and bulky element. If the feedback capacitor C_{FB} is designed such that it represents a short-circuit for the high-frequency CM signals ($v_{CM,\sim}$) but a high impedance element for the third harmonic component ($v_{CM,h3}$), the low-frequency component will drop across the feedback capacitor and only $v_{CM,\sim}$ has to be handled by the inductors. Unfortunately, three-phase CM inductors typically allow only a very small zero-sequence current without saturation because of their very high permeability. Due to

$$i_{FB,h3} \approx C \frac{dv_{CM,h3}}{dt} \ . \tag{5.73}$$

the feedback capacitor has to be as small as possible to prevent saturation of the CM inductor. The relatively large DM capacitors C_{DM} (660 nF per phase) can hence not be used alone for implementation and a low capacitance feedback capacitor C_{FB} is connected in series to the star-point N'.

The CM inductor on the other hand has to hold the high-frequency CM voltage and core saturation is avoided if

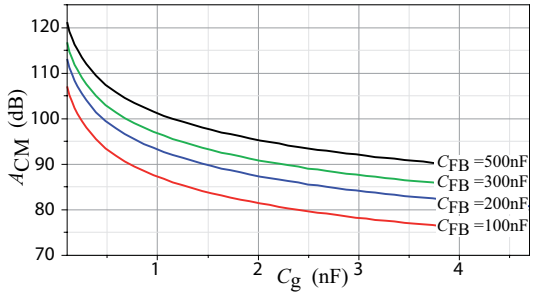
$$B_{\mathrm{sat}} > B_{\mathrm{CM,max}} = \frac{\int_0^{T_\mathrm{p}} v_{\mathrm{CM},\sim} dt}{N\, A_{\mathrm{Fe}}} = \frac{\frac{V_\mathrm{o}}{3} T_\mathrm{s}}{N\, A_{\mathrm{Fe}}} \tag{5.74}$$

where $T_\mathrm{s} = 1/f_\mathrm{s}$ and T_p denotes the maximal length of a CM pulse which was set to $T_\mathrm{p} = T_\mathrm{s}$ for a worst case approximation, N is the number of turns and A_{Fe} is the effective magnetic area of the core.
As the CM inductors are placed in series to the boost inductors $L_{\mathrm{N}i}$ the full phase current including the high-frequency ripple flows through their windings. The high-frequency DM current ripple does not cause core losses due to the mutual compensation of the magnetomotive forces but copper losses caused by the AC current fundamental and the skin and the proximity effect (current ripple) have to be considered.

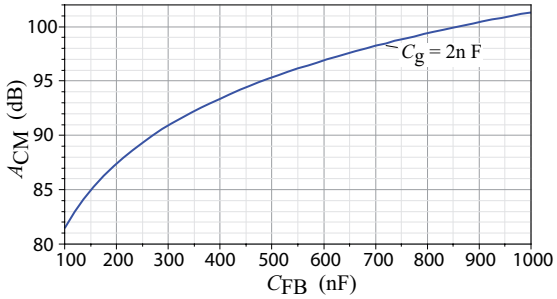
In **Fig. 5.75(b)** the CM equivalent circuit is shown. If the lumped capacitance C_g is not neglected, part of the total CM current does not return through the feedback path i_{FB}. Depending on the size of C_g this results in a notable earth current through the LISN. In order to limit this current, the feedback capacitor should be large which is, however, in contradiction to the design criteria given in (5.73). Depending on the parasitic capacitances C_g and C_{FB} the attenuation A_{CM} can be calculated by

$$\begin{aligned} A_{\mathrm{CM}} &= 20\, \log_{10}\left(\left|\frac{1 + A\, s + \underline{Z}_\mathrm{L}\, C_\mathrm{g}\, C_{\mathrm{FB}}\, R_{\mathrm{LISN,CM}}\, s^2}{R_{\mathrm{LISN,CM}} C_\mathrm{g}\, s}\right|\right) \\ A &= C_\mathrm{g}\, (\underline{Z}_\mathrm{L} + R_{\mathrm{LISN,CM}}) + \underline{Z}_\mathrm{L}\, C_{\mathrm{FB}} \end{aligned} \tag{5.75}$$

where $\underline{Z}_\mathrm{L}$ denotes the total impedance of the CM inductor and $R_{\mathrm{LISN,CM}}$ is the equivalent high-frequency CM impedance of the LISN ($R_{\mathrm{LISN,CM}} = 16.7\,\Omega$). In **Fig. 5.76(a)** the resulting attenuation of the constructed filter is plotted as a function of the earth capacitance C_g. It is obvious that the required attenuation of 93 dB can only



(a)



(b)

Fig. 5.76: (a) Attenuation A_{CM} of the proposed CM filter concept as a function of earth capacitance C_g and (b) achieved attenuation as a function of C_{FB} for $C_g = 2\,nF$ ($f = 1\,MHz$).

be achieved with the proposed concept if either $C_{FB} > 500\,nF$ or $C_g < 1\,nF$. A higher amount of capacitance to earth would result in an attenuation lower than the required value given in (5.66). According to **Fig. 5.76(b)**, a higher capacitance of C_{FB} would increase the attenuation but this would also increase the low-frequency current $i_{CM,h3}$ and is therefore not an option. A compromise of $C_{FB} = 200\,nF$ is therefore used for the filter at hand. As a result, an additional CM filter stage, which must show the missing attenuation of $\approx$20 dB, is required.

Until this point, the capacitors C_p and C_n of the extended noise model given in **Fig. 5.72** have been neglected for the CM filter design. According to (5.71) the total converter noise $v_{ri,M}$ can be divided into DM and

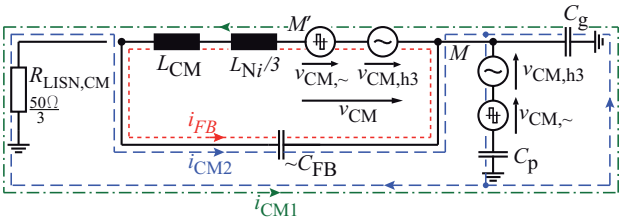


Fig. 5.77: CM equivalent circuit of the three-phase/level PWM rectifier with heat sink connected to earth if C_p and C_n are assumed to be equal.

CM emissions, if the two lumped parasitic capacitors are assumed to be equal ($C_p = C_n$). A simplified CM model can hence be drawn which is shown in **Fig. 5.77**. It is obvious that even if the proposed CM concept operates ideally ($i_{CM1} = 0$), a CM current i_{CM2} through the LISN exists (marked as a blue dashed line). This current is caused by the parasitic capacitances of the semiconductors to the heat sink (if the heat sink is connected to earth) and can only be reduced by insertion of an additional CM filter stage. As already discussed, this additional filter stage is needed in any case in order to achieve the required attenuation given in (5.66). It has to be stated here, that the proposed CM filter concept (connection of M with N') supports the propagation of this type of CM emissions and that a large capacitance C_g would help to reduce the emissions. The advantage of an output voltage without high-frequency CM component, however, clearly dominates this drawback.

5.7.3 Filter Construction

After determination of the EMI filter topology and the calculation of the filter performance the implementation of the passive components is an important step. A proper magnetic material has to be chosen for implementation of the inductors and as for the boost inductors the powder core material -8 from Micrometals Inc. is chosen for the DM inductors due to its high-frequency performance and low core losses. Single layer winding toroids T90-8 with $N = 16$ turns are used to construct the DM inductors with very low parasitic capacitance. This results in a high self-resonance frequency of 25.9 MHz.

Three 220 nF/630 V X7R ceramic capacitors in parallel are used for the construction of the DM capacitors C_{DM1} and C_{DM2}. The capaci-

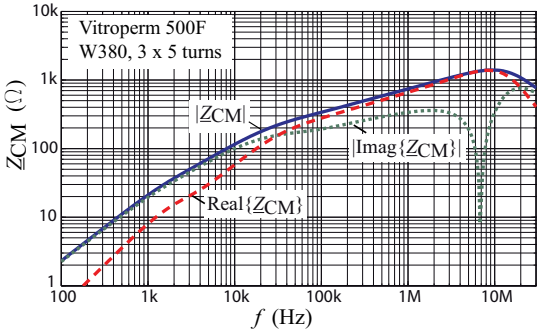


Fig. 5.78: Measured impedance of the constructed three-phase CM inductor ($N = 5$ turns) employing Vitroperm 500F from VAC.

tance of these ceramic capacitors is, unfortunately, strongly dependent on the applied voltage which results in a significantly lower effective capacitance at high voltage. Five capacitors must be used hence for the implementation at hand. This can be avoided by application of foil capacitors although this results in a greater volume.

The nanocrystalline material Vitroperm 500F of Vacuumschmelze Inc. is used for the CM inductors. The measured complex insertion impedance $\underline{Z}_{\mathrm{CM}}$ of the CM inductor is plotted in **Fig. 5.78**. The inductor exhibits a substantial real part of $\underline{Z}_{\mathrm{CM}}$ at $f = 1\,\mathrm{MHz}$ which has to be considered for the design of the CM filter stage. As the material Vitroperm 500F is not typically applied in the frequency range of several 100 kHz, the manufacturer provides no core loss information for these frequencies. The core losses of the Vitroperm 500F material at 1 MHz have hence been measured resulting in the parametrization of the Steinmetz equation

$$P_{\mathrm{VP500F}} = K_{\mathrm{c}} f^{\alpha} B^{\beta} = 44.66 \cdot 10^{-6} [\mathrm{W/dm^3}]\ f^{1.56} B^{1.77} \qquad (5.76)$$

where the frequency f is in Hz and the peak flux-density B is in T. Note that these parameters $(K_{\mathrm{c}}, \alpha, \beta)$ are only valid for frequencies in the vicinity of 1 MHz. Due to the relatively large loss density at 1 MHz three inductors are connected in series for implementation of L_{CM1} in order to limit the core losses. By use of (5.76) the resulting core losses of each Vitroperm 500F core (W380) can be calculated to $P_{\mathrm{Fe,CM}} = 3.7\,\mathrm{W}$. In order to limit the temperature rise of the CM and

TABLE 5.17: Components used to implement the DM EMI-filter.

Part	Type
L_{N}	Micrometals E137-8, $N = 18$ (5 strands, $d = 0.9\,\mathrm{mm}$)
	$L_{\mathrm{N}} = 20\,\mu\mathrm{H}$, $f_{\mathrm{res}} = 11.7\,\mathrm{MHz}$
L_{DM1}, L_{DM2}	Micrometals T90-8, $N = 16$ ($d = 1.8\,\mathrm{mm}$)
	$L_{\mathrm{DM}} = 9\,\mu\mathrm{H}$, $f_{\mathrm{res}} = 25.8\,\mathrm{MHz}$
C_{DM}, C_{DM1}	3 x Ceramic cap. $220\,\mathrm{nF}/500\,V_{\mathrm{DC}}$ in parallel
	$f_{\mathrm{res}} = 9\,\mathrm{MHz}$
C_{FB}	Ceramic cap. $220\,\mathrm{nF}/500\,V_{\mathrm{DC}}$
	$f_{\mathrm{res}} = 9\,\mathrm{MHz}$
C_{DM2}	2 x Ceramic cap. X2 $33\,\mathrm{nF}/250\,V_{\mathrm{AC}}$ in parallel
	$f_{\mathrm{res}} = 21\,\mathrm{MHz}$

boost inductors small fans are placed between them (cf. **Fig. 5.79**). The core W409 (also utilizing Vitroperm 500F) is used for the second CM filter stage in conjunction with 4.7 nF Y2-rated ceramic capacitors which show a very small volume.

The complete schematic of the built filter including detailed information on the used materials used is given in **Fig. 5.79**. The impedance mismatch concept described in [245] is used for arrangement of the different filter stages. According to this concept, the impedance of the last DM filter stage (C_{DM2}) should be much smaller than the impedance of the LISN ($R_{\mathrm{LISN,DM}} = 50\,\Omega$) which is given for the arrangement shown in **Fig. 5.79**. This should also be considered for the last CM filter stage (C_{CM2}). The LISN shows, however, a reduced CM impedance $R_{\mathrm{LISN,CM}} = 16.7\Omega$ and in addition the impedance reduction of the last CM filter stage is limited by equipment safety regulation (C_{CM2}). An additional CM inductor (L_{CM3}) is therefore needed to fulfill the impedance mismatch criteria. This CM inductor uses a ferrite core which is clamped to the power cable. The CM inductors are placed in series to the DM inductors as the stray inductance of the CM inductors then can be used advantageously to increase the DM attenuation.

The constructed EMI filter prototype is shown in **Fig. 5.80**. The overall dimensions of the EMI filter board are $124.5\,\mathrm{mm} \times 110\,\mathrm{mm} \times 33\,\mathrm{mm}$ which results in a power density of $22.1\,\mathrm{kW/dm^3}$ for the EMI filter.

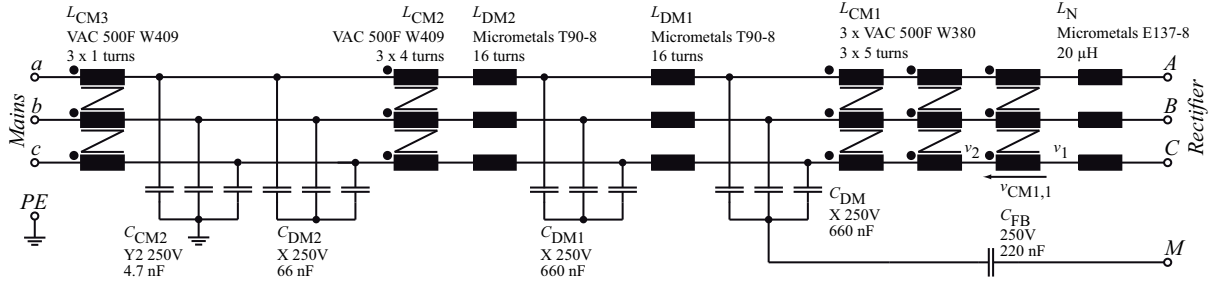


Fig. 5.79: Complete schematic of the implemented EMI filter including information on the used materials.

TABLE 5.18: Components used to implement the CM EMI-filter.

Part	Type
$L_{\mathrm{CM1},i}$	3 x VAC Vitroperm 500F W380 (3×5 turns) in series
	$d = 1.8\,\mathrm{mm}$, $\lvert\underline{Z}_{\mathrm{CM}}\rvert$ @ 1 MHz=970 Ω
L_{CM2}	VAC Vitroperm 500F W409 (3×4 turns)
	$d = 1.8\,\mathrm{mm}$, $\lvert\underline{Z}_{\mathrm{CM}}\rvert$ @ 1 MHz=520 Ω
L_{CM3}	VAC Vitroperm 500F W409 (3×4 turns)
	$\lvert\underline{Z}_{\mathrm{CM}}\rvert$ at 1 MHz=32 Ω
C_{CM2}	Ceramic cap. Y2 4.7 nF/250 V_{AC}

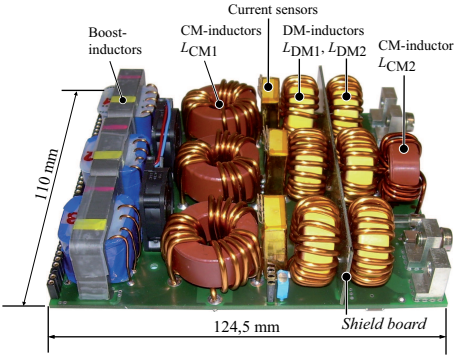


Fig. 5.80: Constructed prototype of EMI filter for the ultra-compact 10 kW rectifier system with a switching frequency of 1 MHz.

The experimental results of the EMI filter and several practical aspects of the filter implementation such as component arrangement, shielding layers, magnetic coupling, etc., are discussed in section 5.9 and verified by measurements.

5.7.4 EMI Filter Power Losses

In the following, the power losses of the EMI filter will be estimated. The calculations are only performed for $P_{\mathrm{o}} = 10\,\mathrm{kW}$, $f_{\mathrm{N}} = 50\,\mathrm{Hz}$ and $V_{\mathrm{N}} = 230\,\mathrm{V}$.
A negligible ripple current flows through the DM filter inductors L_{DM1} and L_{DM2} and the dc-resistance of the DM inductors ($R_{\mathrm{DC,DM}} = 5\,\mathrm{m\Omega}$)

can be used to calculate the copper losses which results in

$$P_{\mathrm{cu,DM}} = R_{\mathrm{DC,DM}} I^2_{\mathrm{N,rms}} = 1.15\,\mathrm{W}\ . \tag{5.77}$$

The peak flux density of the core is 240 mT and the core losses are, according to the loss parameters given in [246], only 50 mW. The total losses of the DM inductors are therefore

$$P_{\mathrm{DM,tot}} = 6\,(P_{\mathrm{cu,DM}} + P_{\mathrm{Fe,DM}}) = 7.2\,\mathrm{W}\ . \tag{5.78}$$

The core losses of the CM chokes have been calculated before and resulted in $P_{\mathrm{Fe,CM}} = 3.7\,\mathrm{W}$. The copper losses of the CM inductors are in a first step calculated using only the DC-resistance of the winding. With $R_{\mathrm{DC,CM}} = 2\,\mathrm{m\Omega}$ the copper losses of one inductor is

$$P_{\mathrm{cu,CM}} = 3R_{\mathrm{DC,CM}} I^2_{\mathrm{N,rms}} = 1.35\,\mathrm{W} \tag{5.79}$$

which yields to

$$P_{\mathrm{CM,tot}} = 3(P_{\mathrm{cu,CM}} + P_{\mathrm{Fe,CM}}) = 15\,\mathrm{W}\ . \tag{5.80}$$

Taking the losses of the third CM filter stage and losses of the capacitors at the input into account the total losses of the EMI filter are approximately

$$P_{\mathrm{EMI}} = P_{\mathrm{DM,tot}} + P_{\mathrm{CM,tot}} + P_{\mathrm{EMI,add}} \approx 30\,\mathrm{W}\ . \tag{5.81}$$

5.7.5 Parasitic Couplings

In a practical filter implementation parasitic magnetic and capacitive couplings between filter elements exist. One has to be aware that inductive couplings can cause problems in the lower frequency range of several 100 kHz whereas the impact of capacitive coupling is more pronounced at higher frequencies (typ. $>$ 1 MHz). Due to these two effects, parasitic couplings between the different filter stages of the multi-stage filter and also between the three phases occur which typically degrade the actual filter performance. Some research in this area is described in literature and some interesting results can be found in [247, 248, 249]. The influence of parasitic couplings on the EMI filter at hand is subject of ongoing research but, some effects will be discussed shortly in the the following.

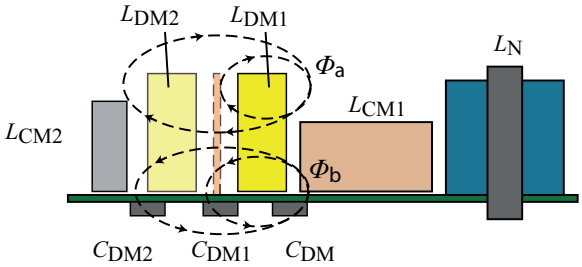


Fig. 5.81: Arrangement of the EMI filter and inductive coupling caused by the external field of the DM-inductor L_{DM1}.

It has to be stated here that typical filter elements (capacitors and magnetic materials used for construction of the inductors) typically show component variations of 10 % and more and that these component variations might take a stronger influence on the filter performance than parasitic couplings if a proper PCB layout is done. Parasitic capacitances between traces in the PCB layout are typically in the range of some 10 pF and may hence show a more pronounced influence than coupling through air. Also relatively large magnetic coupling loops may be generated by the traces on the PCB. This highlights that a proper high-frequency oriented PCB layout is very important to achieve the desired filter performance.

Fig. 5.81 illustrates the arrangement of the EMI filter stages. The specific inductors are mounted on the top-side of the PCB whereas the SMD-type ceramic capacitors are soldered on the bottom side. The standard toroid winding configuration of the DM inductors presents a large loop area (equivalent to a single turn) which creates an external flux (shown for L_{DM1} in **Fig. 5.81**). As discussed in [247], magnetic coupling between the inductors and filter capacitors could significantly degrade the filter performance for frequencies beyond a few MHz if foil capacitors are used. At the implementation at hand ceramic capacitors are used for filter implementation which show a much smaller coupling area than foil capacitors. No pronounced filter degradation caused by this parasitic magnetic coupling is therefore expected but this is subject for further research.

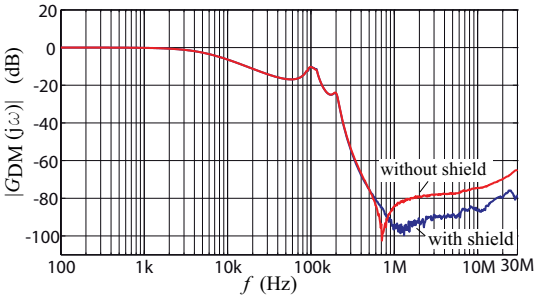
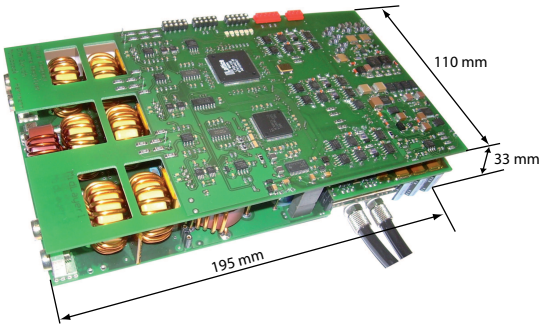


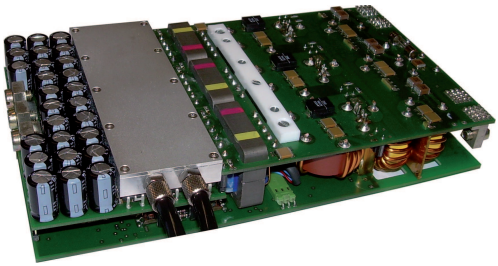
Fig. 5.82: Measured transfer function $G_{\mathrm{DM}}(\mathrm{j}\omega)$ of the DM filter with and without shield board.

As can be seen in **Fig. 5.80**, the DM inductors L_{DM1} and L_{DM2} are arranged face to face. The implemented winding configuration of these inductors shows a large loop area which presents a large magnetic coupling to other components. Due to the coupling of L_{DM1} and L_{DM2} the attenuation of the DM filter stage is reduced. This effect could be minimized by a proper arrangement of the DM inductors but this is not an option for the implementation at hand due to the objective of a very high power density. Another possibility would be to reduce the coupling area of the DM inductors by a winding technique shown in [245]. This winding technique is, however, more expensive and difficult to perform due to the small core geometries in conjunction with the relatively large diameter of the solid copper wire ($d = 1.8\,\mathrm{mm}$). Instead, a magnetic shield board (0.1 mm thick Mu-metal foil glued on a PCB with solid copper layer) is inserted between the two stages to reduce the coupling (also shown in **Fig. 5.80**).

In **Fig. 5.82** the measured transfer function $G_{\mathrm{DM}}(\mathrm{j}\omega)$ of the filter with and without shield board is plotted. An improvement of $\approx 10\,\mathrm{dB}$ can be measured for frequencies above 1 MHz whereas for frequencies below 800 kHz no difference occurs. It has to be stated here that the dynamic range of the used network analyzer Bode100 [250] is 100 dB and that the measurement results are therefore limited to this value.



(a)



(b)

Fig. 5.83: (a) Top view and (b) bottom view of the constructed ultra-compact 10 kW Vienna Rectifier prototype VR1000 showing dimensions of 195 mm×110 mm×33 mm which yields to a remarkable power density of 14.1 kW/dm^3.

5.8 Construction of the Rectifier System

The finally constructed rectifier prototype is shown in **Fig. 5.83**. The overall dimensions of the system are 195 mm × 110 mm × 33 mm, thus giving a remarkable power density of 14.1 kW/dm^3 including the water cooler. The system shows a total a weight of 1.06 kg resulting in an extremely high power to weight ratio of 9.44 kW/kg. A modular design is chosen, where the system consists of three PCB boards. The power board (cf. **Fig. 5.84(a)**) contains all semiconductors, the output capacitors, the designed water cooler and the output connectors. In order to keep the commutation loop of the rectifier as small as possible

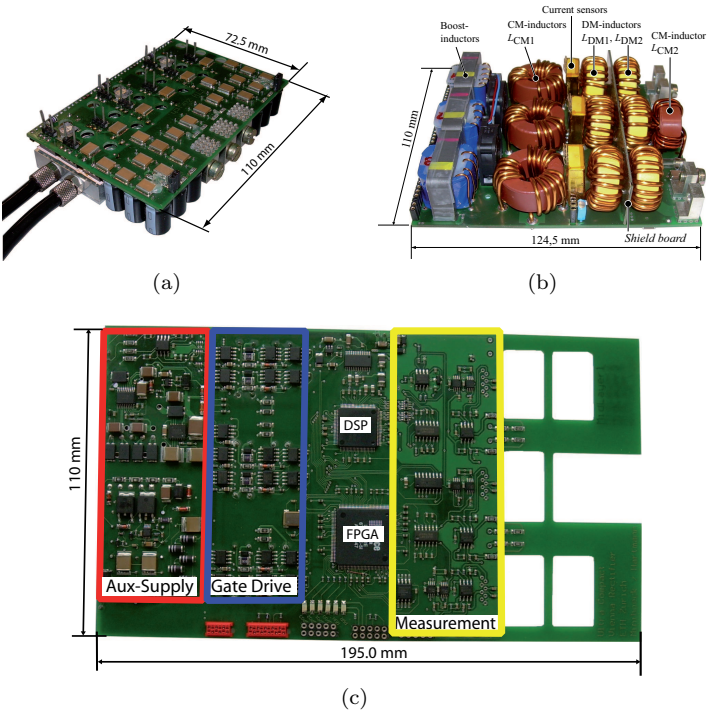


Fig. 5.84: (a) Power board, (b) EMI board and (c) control board of the constructed hardware prototype VR1000.

the ceramic capacitors are placed closely to the semiconductors. The power board is connected to the EMI Board (cf. **Fig. 5.84(b)**) which contains the boost inductors, the multi-stage DM and CM EMI filter, current sensors and the input connectors.

The control board (**Fig. 5.84(c)**) contains all elements of the digital controller including analog measurement circuitry, auxiliary power supply and gate drives. The heart of the control board is the digital high-speed controller which is implemented using an FPGA. A DSP is used for calculation of the output voltage/output voltage symmetry controller, system management and debugging of the rectifier system. A simple serial interface between the DSP (superimposed output voltage controller) and the FPGA (high-speed current controller) is imple-

TABLE 5.19: Volumes of the main system elements of the constructed rectifier system VR1000.

	Volume (dm^3)	Amount of total volume
Semicond./ water cooler	$0.084\,dm^3$	12 %
Output cap. (C_o)	$0.07\,dm^3$	10 %
Boost ind. (L_{Ni})	$0.081\,dm^3$	11 %
EMI filter	$0.34\,dm^3$	48 %
Auxiliary supply	$0.053\,dm^3$	8 %
Gate drive	$0.047\,dm^3$	7 %
Control	$0.032\,dm^3$	4 %
Total	$0.707\,dm^3$	100 %

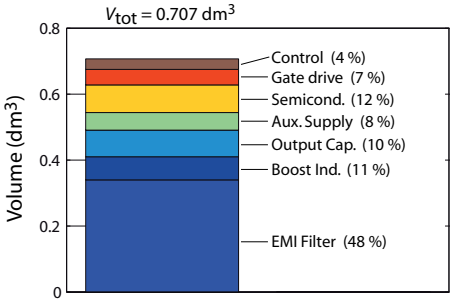


Fig. 5.85: Proportion of the main system elements of the constructed rectifier system VR1000.

mented. Next to the DSP the voltage and current measurement units are located. The ADCs are placed as near as possible to the particular measurement units. The noise sensitive areas of the specific measurement units are therefore kept very small which improves the signal quality of the measured quantities. In addition to the measurement units also the gate drives are placed on the control board. The auxiliary power supply, which is located next to the gate drive stages, is supplied by the mains voltage using a three-phase diode bridge.

The volumes occupied by the main elements of the constructed rectifier system are listed in **TABLE 5.19** and the volume distribution

TABLE 5.20: Occupied volumes of the particular boards.

	Volume (dm^3)	Power density (kW/dm^3)	Amount of total volume
Power board	$0.16\,dm^3$	$62.7\,kW/dm^3$	22 %
EMI board + Boost ind.	$0.41\,dm^3$	$24.3\,kW/dm^3$	59 %
Control board	$0.13\,dm^3$	−−	19 %
Total	$0.7\,dm^3$	$14.1\,kW/dm^3$	100 %

is plotted in **Fig. 5.85**. The volumes of the three boards (cf. **Fig. 5.84**) are listed in **TABLE 5.20**. The boxed volumes of the system parts are used for this calculation which includes the air between the components. The semiconductors (including water cooler) and the output capacitors consume only 12 % and 10 % of the total volume. The power board, consisting of these two elements, takes therefore only 22 % of total system volume which results in a very high power-density of the power board of $63.7\,kW/dm^3$.

The EMI board, consisting of the EMI filter and the boost inductors, is the biggest system part and consumes 59 % of the total rectifier volume, in which the EMI filter (DM and CM filter) takes 48 % and the boost inductors take 11 %. This clearly demonstrates, that the passive elements, mainly represented by the EMI filter limit the power density. Even at the implemented switching frequency of 1 MHz the EMI filter takes approximately 60 % of the total system volume. The reason can be found on one hand in the lack of a proper magnetic materials with a high permeability at some MHz and on the other hand, the EMI filter has to implement a certain amount of noise attenuation at the lower boundary of the EMI measurement range ($f = 150\,kHz$). The size of the inductor windings are in addition limited by copper losses and this inhibits a smaller volume of the inductive components.

In the given power density only the size of the water cooler is considered which "transfers" the heat from the semiconductors just to the water. The heat exchanger, pump system, etc., are not considered which one has to keep in mind when the given power densities are examined. The rest of the volume is occupied by the control board. In the volumes of the auxiliary power supply and the gate drive some air is included

which results from the mechanical construction of the rectifier system and allows to omit an additional share labeled with “Air”.

5.9 Experimental Results

Measurement results taken from the VR prototype at different load conditions are shown in **Fig. 5.86** for a mains frequency of $f_N = 50\,\text{Hz}$. The parameters $K = 0.25$, $k_1 = 0.96$ and $k_2 = 0.99$ are used for the current controller and the MOSFETs IPP60R099CP are employed. In **Fig. 5.86(a)**, the input current i_{N3} and phase voltage v_{N3} are plotted for an output power of $P_0 = 9.6\,\text{kW}$ ($V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$). The current shows nearly ideal sinusoidal shape being in phase with the mains voltage which is expressed by a measured THD_I of only 1.8 % and a power factor of 0.999. A measurement at $P_o = 6.6\,\text{kW}$ is given in **Fig. 5.86(b)** ($V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$) where a THD_I of 3 % and a power factor of 0.999 is measured.
As shown in **Fig. 5.86(c)**, a slightly improved THD of 2.6 % can be measured ($V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$, $P_o = 5.8\,\text{kW}$) if the rectifier system is employed with the MOSFETs IPP60R165CP which show a smaller chip area and therefore smaller turn-off delays. In **Fig. 5.86(d)**, a measurement at $f_N = 400\,\text{Hz}$ and an output power of $P_o = 5.8\,\text{kW}$ is given where a THD_I of 2.4 % can be measured. An operation of the rectifier system at higher output load at $f_N = 400\,\text{Hz}$ or even $f_N = 800\,\text{Hz}$ is inhibited by the magnetic material of the boost and DM inductors which is not suitable for these mains frequencies.

The measurement results confirm the good performance of the implemented current controller and despite the high switching frequency a very good input current quality ($\text{THD}_I < 2\,\%$) can be achieved at nominal load. As derived in section 5.1.2, a better input current quality is inhibited by the turn-off delays of the MOSFETs whose influence increases with increasing switching frequencies.

The measured efficiency and input current quality, expressed by the THD_I, are given in **Fig. 5.87** as a function of output power P_o. Due to the large switching losses only a moderate maximum efficiency of 94 % can be measured which further drops when the system is operated with power levels below $P_o < 4\,\text{kW}$. The measured efficiency is, however, quite below the calculated efficiency given in section 5.4.3. As discussed in section 5.1.3, the reason can be found in increased switching losses due to an “error” in the PCB layout. If the switching losses are corrected a good agreement of calculated and measured values can be observed.

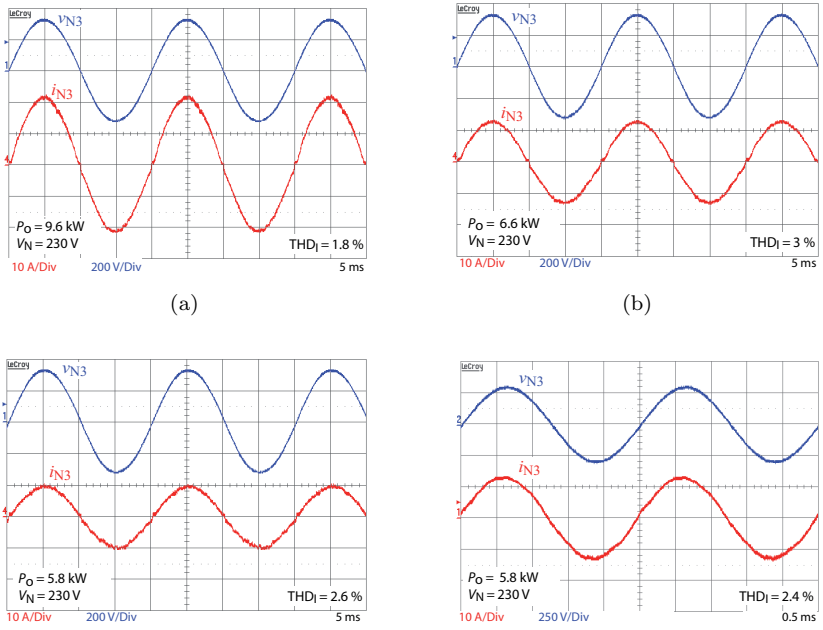
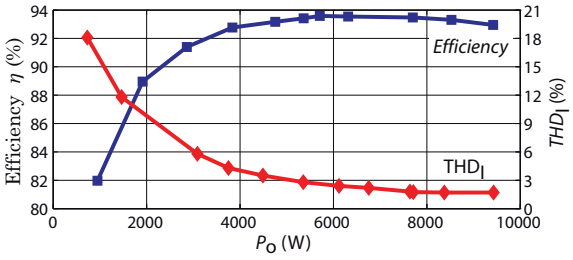
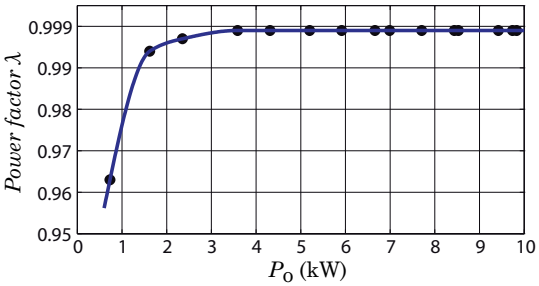


Fig. 5.86: Measured input current waveforms of the constructed rectifier system operating at different power levels (f_N = 50 Hz, V_N = 230 V, V_o = 800 V); (a) Nominal load P_o = 9.6 kW, Ch1: v_{N3}, 200 V/Div, CH4: i_{N3}, 10 A/Div; timebase: 5 ms/Div. (b) P_o = 6.6 kW, Ch1: v_{N3}, 200 V/Div, CH4: i_{N3}, 10 A/Div; timebase: 5 ms/Div. (c) Measurement of the system employing the MOSFET IPP60R165CP at P_o = 5.8 kW, Ch1: v_{N3}, 200 V/Div, CH4: i_{N3}, 10 A/Div; timebase: 5 ms/Div, and (d) operation at f_N = 400 Hz, P_o = 5.8 kW, Ch1: v_{N3}, 250 V/Div, CH4: i_{N3}, 10 A/Div; timebase: 5 ms/Div.

As a result of the non-optimal PCB layout resulting in higher switching losses the TO220 package of the MOSFETs reaches its thermal limit and the junction temperature of the device rises to a value above 150 °C which finally would damage the transistor. A continuous operation of the rectifier system with an output power of P_o = 10 kW is therefore not possible at present. This power level would be no problem if the layout error described in section 5.1.4 would be fixed.
The measured power factor λ of the rectifier system at operation with



(a)



(b)

Fig. 5.87: (a) Measured efficiency and input current quality of the constructed rectifier system VR1000 operating at $f_N = 50\,\text{Hz}$ and $V_N = 230\,\text{V}$. (b) Measured power factor λ.

50 Hz is given in **Fig. 5.87(b)**. Due to the very small amount of filter capacitance ($C_{\text{DM,tot}} \approx 1.5\,\mu\text{F}$) at the input, a power factor of 0.999 can be measured down to an output power of $P_o = 3.5\,\text{kW}$ and at 10 % nominal load still a power factor of 0.975 is given. This is a positive effect of the very high switching frequency.

The measured efficiency of the rectifier system employing CoolMOS devices IPP60R165CP instead of devices IPP60R099CP is given in **Fig. 5.88**. This would yield to improved input current quality. A reduced efficiency at higher load levels can, however, be observed due to the higher conduction losses and an operation with this MOSFET is therefore not possible. Even if the layout error would be fixed, the junction temperature would remain in the area of the thermal limit of the device which is 150 °C.

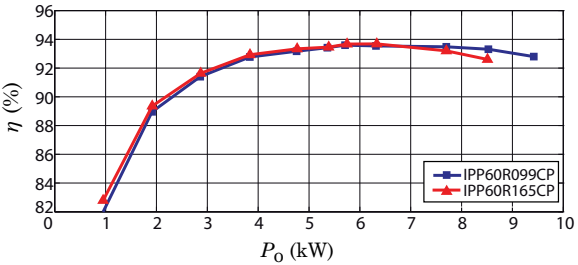


Fig. 5.88: Measured efficiency of the rectifier system using either CoolMOS devices IPP60R099CP ($A_{\mathrm{Chip}} = 30\,\mathrm{mm}^2$) or IPP60R165CP ($A_{\mathrm{Chip}} = 20\,\mathrm{mm}^2$).

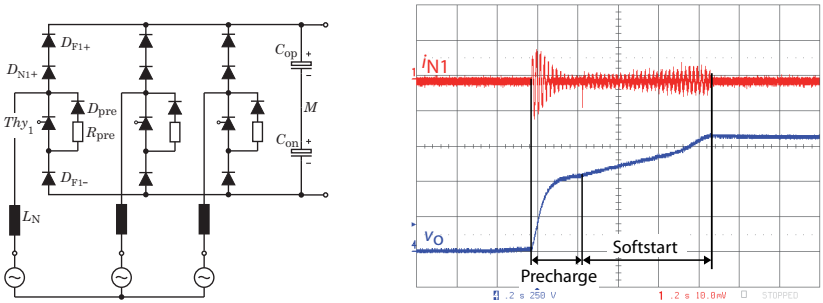


Fig. 5.89: (a) Simplified start-up circuit of the rectifier system and (b) measured automatic startup sequence of the rectifier system; Ch1: $I_{\mathrm{N1}}, 5\,\mathrm{A/Div}$, Ch4: $V_{\mathrm{o}}, 250\,\mathrm{V/Div}$, timebase: $0.2\,\mathrm{s/Div}$.

A start-up sequence is implemented in the controller such that the rectifier system can directly be connected to the grid and starts up fully autonomous. In order to limit the inrush current charging the output capacitors to the mains line-to-line voltages, a start-up circuit is employed (cf. **Fig. 5.89(a)**). The lower mains diode $D_{\mathrm{N}-}$ is therefore replaced by by a thyristor and a start-up resistor R_{pre}, implemented by a PTC connected in series to a precharge diode D_{pre}, is connected in parallel to the thyristors. No additional start-up element is therefore inserted into the circuit's power path during normal operation. A measurement of the automatic start-up process is given in **Fig. 5.89(b)**. When the rectifier system is connected to the grid, the thyristors Thy_i

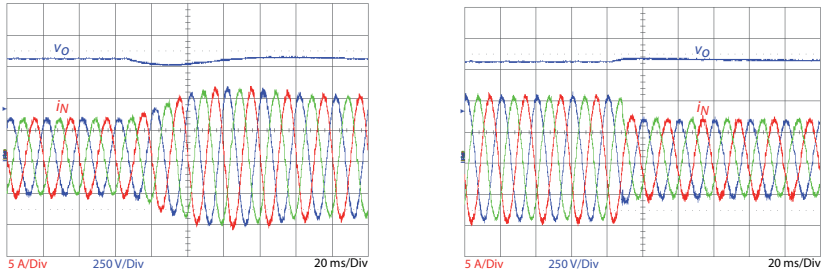


Fig. 5.90: Measured response of the rectifier system on load steps ($f_N = 50\,Hz$, $V_N = 230\,V$, $V_o = 800\,V$); (a) Load step from $P_o = 3\,kW$ to $P_o = 5\,kW$ and (b) load step from $P_o = 5\,kW$ to $P_o = 3\,kW$. Phase currents i_{Ni}, 5 A/Div, output voltage v_o, 250 V/Div; timebase: 20 ms/Div.

are open and the charging current of the output capacitors is limited by the resistors R_{pre}. The current controller is disabled during this time interval and the MOSFETs are permanently off. This time interval is marked in **Fig. 5.89(b)** as "precharge". After the precharge state, the output capacitors are fully charged and the input currents become zero. Now an offset calibration of the main current sensors can be performed. The thyristors are turned on after the output voltage V_o has reached the line-to-line peak voltage of the mains and the output voltage controller ramps up the output voltage to the desired output voltage level. This interval is marked as "softstart". The total startup process lasts approximately 0.9 s. The thyristors can also be used to disconnect the rectifier system from the mains in case of an error condition (e.g., overvoltage, overcurrent, etc.). In this case the thyristors are not turned on again after a positive cycle of the corresponding mains phase voltage and the precharge resistors remain inserted between rectifier and mains.

The measured system response of the rectifier to load steps is shown in **Fig. 5.90**. The output voltage controller shows a bandwidth of 23 Hz and a phase margin of 85 °. The load steps are generated by connecting/disconnecting a 2 kW resistive load to the output with a base load of 3 kW. Due to the requirement that the rectifier system must be able to handle a single phase loss the bandwidth of the voltage controller must be sufficiently below 100 Hz. A relative large voltage

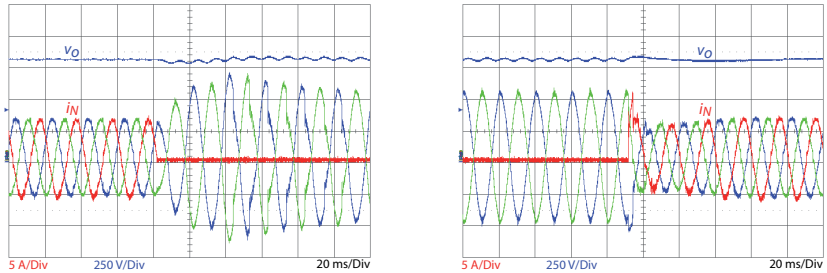


Fig. 5.91: (a) Measured single phase loss and (b) phase return of the constructed rectifier system operating at a power level of $P_o = 3.1\,\text{kW}$ ($f_N = 50\,\text{Hz}$, $V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$); Phase currents i_{Ni}, 5 A/Div, output voltage v_o, 250 V/Div; timebase: 20 ms/Div.

drop of 80 V is therefore obvious in **Fig. 5.90(a)** for the load step of 2 kW. The increase of v_o at load removal is much smaller which could be achieved by a nonlinear controller implementation where the gain is increased for a short-time if a specific higher level of v_o is detected. The performance of the output voltage controller could be improved considerably if the load current is measured and used as feedforward signal of the output voltage controller. Also some actual information on required power from the DC/DC converter supplied could be used to improve the performance. Such a feedforward signal is, however, not implemented in the rectifier system at hand and a load step of 100 % is therefore not possible as the overvoltage detection circuit would trip.

The constructed rectifier system can handle different error conditions. Beside a loss of a single phase also a short circuit between two phases at the rectifier input can be handled at a reduced output power level ($P_o < 0.57 P_{o,nom}$). **Fig. 5.91(a)** shows the system response on a single phase loss at an output power level of $P_o = 3.1\,\text{kW}$ ($f_N = 50\,\text{Hz}$, $V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$). One phase is thereto disconnected from the rectifier system. The output power is now delivered by only two phases and a power flow from the mains to the DC-side pulsating with twice the mains frequency occurs. This can be seen by the low frequency ripple of the output voltage during two-phase operation. Note, that no changes in the controller structure are performed to handle this error condition.

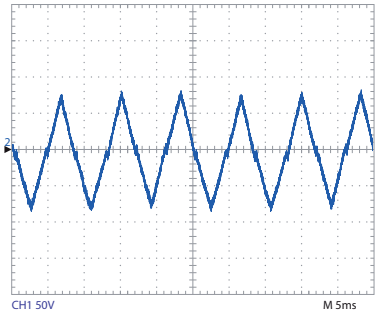


Fig. 5.92: CM output voltage time behavior (measured from M to earth) employing the proposed CM filter concept ($f_N = 50\,\text{Hz}$, $V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$).

A measurement for the return of the lost phase is depicted in **Fig. 5.91(b)**. After the third phase is up again, suddenly an increased input power is available and the output voltage rises. Due to the limited bandwidth of the output voltage controller, V_o would increase to unacceptable levels and the overvoltage detection would trip. The nonlinear controller, however, increases the voltage control gain in case of an overvoltage and therefore, according to **Fig. 5.91(b)**, only a limited overvoltage occurs.

5.9.1 EMI Measurements

As a first step, the proper operation of the proposed concept reducing the high-frequency CM voltage of the output is checked. **Fig. 5.92** shows the voltage of the output midpoint M against earth. No high-frequency CM voltage is present and only the third harmonic triangular signal $v_{CM,h3}$, used for increasing the rectifier modulation range, is measured. This verifies the proper operation of the proposed CM filter concept.

In **Fig. 5.93** the results of an EMI measurement according to CISPR 11 are shown together with the limits of CISPR 11 Class A. A three-phase DM/CM noise separator according to [251] is applied to measure the DM and CM noise separately. As expected, the main peaks in the spectra occur at f_s and $2f_s$ and are well below the limit. The peak at 5 MHz results from a shielding layer in the PCB and will be discussed later. The peak in the DM spectrum at 400 kHz has its origin in the

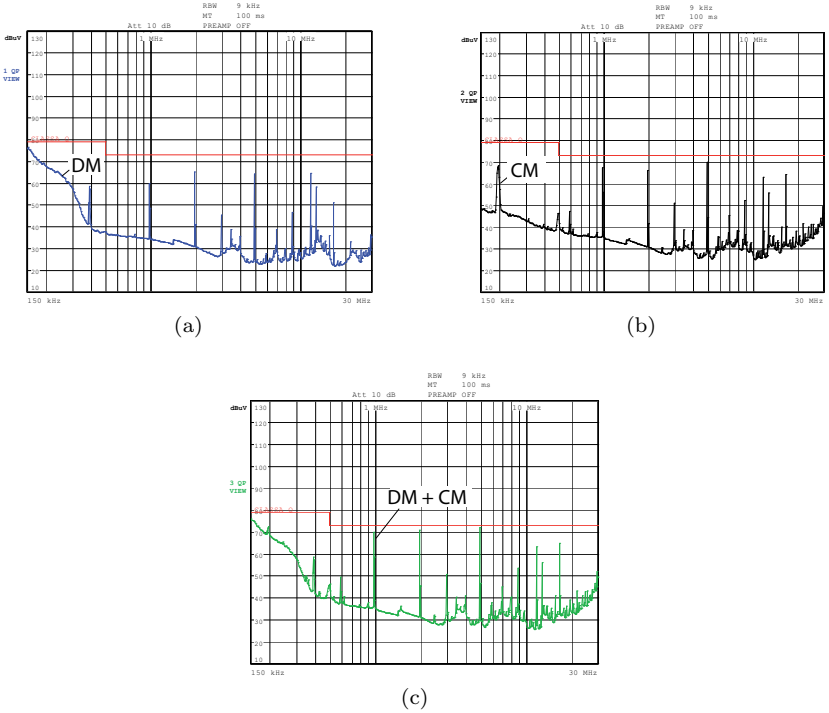


Fig. 5.93: Final CE measurements of the rectifier system as constructed; (a) DM emissions, (b) CM emissions and (c) total emissions.

auxiliary power supply and the peak of the CM emissions at 200 kHz is caused by the auxiliary supplies of the gate drives.

Next, the influence of the arrangement of the first DM and CM filter stages (impedance mismatch) is examined. The DM filter capacitors C_{DM2} are moved behind the CM choke L_{CM2} (cf. **Fig. 5.94(a)**) for this purpose. As nothing is changed for the CM path the three Y2-capacitors (4.7 nF) now constitute an additional DM filter stage with the leakage inductance of the CM choke. The impedance of the Y2-capacitors $|Z_{\mathrm{C,CM2}}|_{1\,\mathrm{MHz}} = 1/\omega C_{\mathrm{CM2}} = 33.8\,\Omega$ is unfortunately in the same range as the DM impedance of the LISN ($R_{\mathrm{LISN,DM}} = 50\,\Omega$) and the current is more or less distributed equally on the LISN and and the filter capacitor. In order to achieve low EMI noise values the impedance

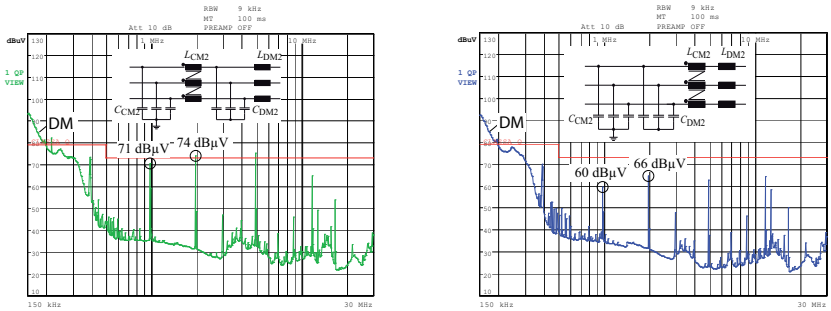
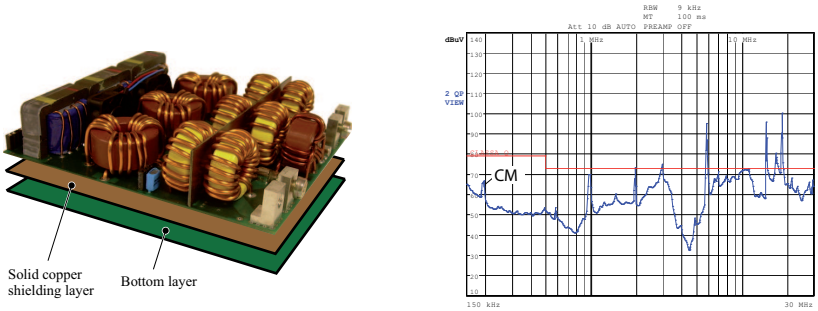


Fig. 5.94: (a) Measured DM emissions of the given CM filter stage arrangement (C_{CM2} and L_{CM2}) with unfavorable arrangement of the DM filter stage and (b) measured DM emissions if the improved filter arrangement.

of the filter capacitors should be much smaller than the impedance of the LISN which is known as *impedance mismatch* in literature [245]. This results in 10 dB higher noise level compared to a implementation shown in **Fig. 5.94(b)** where the DM filter capacitors are moved to the input of the rectifier system. Using this arrangement, the stray inductance of the CM choke advantageously contributes to the attenuation of DM noise. The arrangement of filter stages must therefore be handled with care in order to achieve the desired attenuation.

In the following the question if a solid copper layer in the PCB covering the whole power and EMI filter component arrangement (cf. **Fig. 5.95(a)**) could act as an advantageous shielding layer is discussed. The intention is to connect this copper layer to M in order to catch high-frequency noise currents similar to the proposed CM filter concept. This shielding layer, unfortunately, also introduces a capacitive coupling path from the interconnections of the three CM chokes forming L_{CM1} to M (cf. **Fig. 5.79**). Due to this capacitive coupling, a uniform voltage distribution between the three CM chokes is inhibited. According to the measurements given in **Fig. 5.96**, a phase-shift of the voltage v_2 (after the first CM inductor $L_{CM1,1}$) drives this inductor into saturation ($v_{CM1,1}$ with shield). A uniform voltage distribution, however, occurs if the shielding layer is not connected to M which can be verified by the measured voltage ($v_{CM1,1}$ with shield not connected) which amplitude corresponds to $v_{CM,\sim}/3$.



(a) (b)

Fig. 5.95: (a) Arrangement of the unfavorable solid copper shielding layer in the PCB and (b) measured CM emissions if this shielding layer is present. The CM filter is capacitively short circuited by the shielding layer for frequencies above 5 MHz.

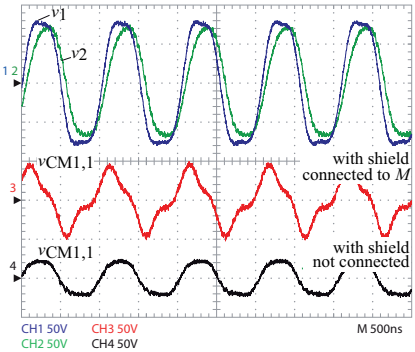


Fig. 5.96: Measured voltage of CM inductor $L_{\mathrm{CM1,1}}$ with and without PCB shield layer connected to M ($f_{\mathrm{N}} = 50\,\mathrm{Hz}$, $V_{\mathrm{N}} = 230\,\mathrm{V}$, $V_{\mathrm{o}} = 800\,\mathrm{V}$).

If the shielding layer is left open, another effect can be observed: the copper layer covers the whole EMI filter and causes a capacitive coupling which forms a low-impedance path bypassing the EMI filter at higher frequencies. An EMI measurement considering solely CM emissions with a copper layer beneath the whole EMI filter is given in **Fig. 5.95(b)** and verifies increased emissions. This copper layer was cut after the CM inductors L_{CM1} for the final construction but the remaining part still caused a noise peak at 5 MHz in **Fig. 5.93**. Shielding layers have hence to be handled with special care.

5.10 Conclusions

The successful implementation of a 10 kW Vienna Rectifier system with an very high switching frequency of 1 MHz yielding to a power density of 14.1 kW/dm^3 has been presented. During the design and detailed analysis of the rectifier system several technical limitation emerged which are restricting an increase of the power density of the chosen VR topology. The main limitations are:

- Limitation in switching speed due to parasitic inductances and capacitances of the semiconductors and the PCB layout.
- Accordingly, high switching losses and limited thermal performance of the semiconductors.
- Turn-off delays of the MOSFET switches which reduce the input current quality. This influence can be reduced by a proper feedforward signal in the current controller.
- Limited performance (e.g. permeability μ_r) of commercially available magnetics for construction of the EMI filter and boost inductors.

An increase in switching frequency goes hand in hand with increased losses, mainly switching losses of the semiconductors but also high-frequency core losses of the magnetic elements and high-frequency losses in the conductors caused by skin and proximity effects. In order to limit the switching losses of the rectifier system not only the switching frequency but also the switching speed must be increased. The switching speed is, unfortunately, limited by parasitic elements of the semiconductors and the wiring inductances of the commutation paths. These elements form together an LC resonant tank which is excited by the very fast switching transients. This results in a pronounced voltage and current ringing which increases the voltage stress and losses of the semiconductors and also the EMI emissions. A classical snubber circuit is not applicable because of far too high losses and a novel magnetically coupled damping concept is proposed to overcome this drawback. The proposed damping concept reduces the switching transient oscillations considerably, although the first peak of the current and voltage ringing is still present.

An active control of the voltage and current slopes, as discussed for modern IGBT gate drives, would be an enhanced method for reducing

the oscillations. This active control, to be implemented in the gate drive stage of the MOSFET, however, would require a control loop bandwidth in the frequency range of the oscillations to be damped (e.g., typically 100 MHz for state-of-the-art power MOSFETs) and is therefore no option at present for a discrete implementation. An integrated implementation, where the intelligent gate driver and power MOSFET are integrated into a single power module, probably could allow such implementation in future.

As a consequence, the switching transients of the MOSFETs have to be set to $\approx 20\,\text{ns}$ which leads to relatively high switching losses. MOSFETs with a small parasitic output capacitance show reduced switching losses but exhibit a higher on-state resistance. Due to the predominance of the switching losses a MOSFET with a small chip area should preferably be chosen. The SJ CoolMOS device IPP60R099CP with a chip area of $30\,\text{mm}^2$ is selected for the final implementation and this selection is based on a detailed chip area dependent loss calculation.

Care should also be taken on the PCB layout and final construction of the rectifier system as parasitic capacitances and inductances of the PCB layout and to the heat sink strongly influence switching losses. As clearly demonstrated in this work, switching loss measurements can only be performed in combination with the constructed prototype system in order to get sensible results. Results of a switching loss measurement taken on a test circuit can be used to benchmark different semiconductors but are not suitable to exactly predetermine switching losses of the final rectifier system.
The cooling system of the constructed rectifier system has been designed according to switching loss measurements taken from the boost-type test circuit which shows very small parasitic capacitances. Due to a non-ideal PCB layout in the power circuit of the finally constructed VR1000 rectifier system considerably increased switching losses occur and the cooling system reaches its limits. The limitation there is the thermal resistance between junction and heat sink $R_{\text{th,js}}$ which can, according to [182], not be improved considerably by applying a power module. As a result of the higher switching losses it has to be recognized that the built rectifier prototype cannot permanently be operated at an output power level of $P_\text{o} = 10\,\text{kW}$. An improved PCB layout of the power board would, however, make a continuous operation of the rectifier system at $P_\text{o} = 10\,\text{kW}$ and $f_\text{s} = 1\,\text{MHz}$ possible.

Another limitation of very high switching frequencies is the turn-off delay of power MOSFETs caused by the nonlinear parasitic output capacitance C_{oss}. The turn-off delay finally leads to input current distortions and this effect is even more pronounced for SJ devices such as the CoolMOS CP family. As C_{oss} is directly proportional to A_{Chip} a device with a preferably small chip area should be selected if very high switching frequencies are to be implemented. This is, however, in contradiction to a preferably large chip area required for low conduction losses. A compromise between these two requirements has to be found and an efficiency - input current quality-Pareto Front (η-$\mathrm{THD_I}$-Pareto Front) is constructed which clearly illustrates the relation between the two performance indices.
The input current quality can, however, be improved considerably by application of an appropriate feedforward signal in the current controller trying to compensate the turn-off delay. A compensation in practice means that the corresponding MOSFET has to be turned off earlier in order to achieve the intended duty cycle which limits the performance of the feedforward signal as for instance duty cycles below 25 % cannot be implemented properly at a switching frequency of 1 MHz.
A very good $\mathrm{THD_I}$ of 1.8 % can, however, be achieved at $f_{\mathrm{N}} = 50\,\mathrm{Hz}$ and $P_{\mathrm{o}} = 10\,\mathrm{kW}$ if the feefworward signal is used and at $P_{\mathrm{o}} = 5\,\mathrm{kW}$ still a $\mathrm{THD_I}$ of 3 % can be measured.

A modern high-speed FPGA must be used for digital current control of the VR system for switching frequencies in the MHz-range. A single DSP control system cannot handle such high switching frequencies. The biggest part of the time used for controller calculation is the delay time of the external A/D converter which typically amounts to more than 300 ns. The three-phase current controller implementation in the FPGA on the other hand takes only 180 ns. The generation of a high resolution symmetrical high-speed PWM is the major limitation of a current controller implementation as the internal clock frequencies of several GHz, required for a counter/comparator approach, are not possible. Several alternative implementation methods for high-speed PWMs have been proposed in literature but more or less all of them cannot be implemented using an FPGA. A detailed knowledge of temperature and core voltage would be required for the proposed solution which is

not available in FPGAs. External, configurable integrated PWM blocks would be optimal for switching frequencies above 1 MHz.
A novel PWM implementation is proposed in this work for implementation of a symmetrical 8 bit PWM with a frequency of 1 MHz which fits the needs for the implementation at hand. This approach, however, reaches its limits if higher switching frequencies are to be implemented. Altogether, the discussed implementation of the three-phase current controller clearly demonstrates that a digital controller implementation is possible for several MHz and even more if an external high-speed PWM block would be available.

Also the EMI filter design is not straight forward for such high switching frequencies. Due to the spectrum of the symmetrical PWM rectifier voltage, the EMI filter not only has to implement a proper amount of damping at switching frequency harmonics (mainly f_s and $2f_s$), but also has to ensure a considerable damping at the lower frequency limit of the EMI measurement (e.g., 150 kHz for CISPR11 Class A). The pulse width modulated nature of the rectifier voltage results in a high noise floor of $\approx 110\,\mathrm{dB\mu V}$ which would exceed the EMI limit of CISPR11 Class A if the EMI filter would not show proper attenuation at this frequency. At least one filter stage must be designed to attenuate this noise and the volume of this filter stage is determined by 150 kHz. Its volume can therefore not be reduced by increasing the switching frequency.
The lack of commercially available magnetic materials and components for frequencies in the MHz range is the other limitation of a volume reduction of the EMI filter. The core loss at such high frequencies yield to a limited volume reduction. As will be discussed in section 7 in detail the volume of the EMI filter could only be reduced by 12.6 % if the switching frequency is increased from 500 kHz to 1 MHz. In the final VR hardware prototype, the EMI filter still takes 58 % of total system volume.
The design of an EMI filter for $f_s = 1\,\mathrm{MHz}$ and above is in addition a very challenging task as parasitic elements of the devices and of the interconnections show a strong influence on the EMI filter performance. The final performance of the EMI filter can therefore only be predicted in a limited manner by simulations or calculations.

Chapter 6

Three-Phase Delta-Switch Rectifier

In this chapter the three-phase Δ-switch rectifier system will be analyzed in detail. By application of space vector calculus possible switching sequences are derived and an optimal switching sequence in terms of minimal system power losses is derived. It will be shown that a pulse-width modulator using a proper carrier signal is able to implement this optimized switching sequence and that space vector control (which comes along with a high signal processing demand in the digital controller) is not required for control of the rectifier system. To facilitate the design, analytical relationships for calculating the power component's average and rms current ratings are derived and design guidelines for the passive components are given. The DM and CM voltages of the rectifier system are analyzed and the corresponding emissions are predicted. In addition the rectifier's mains current phase displacement control range is determined and the question is clarified to what extend this phase shift capability can be used to improve the rectifiers power factor.

6.1 System Operation

The basic schematic of the three-phase Δ-switch rectifier system is depicted in **Fig. 6.1**. The system consists of a three-phase diode bridge

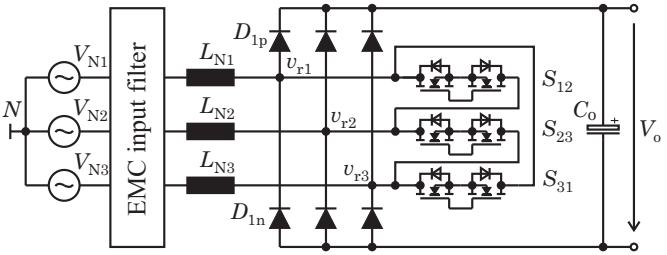


Fig. 6.1: Schematic of the two-level three-phase Δ-switch rectifier.

and three bidirectional (current) bipolar (voltage) switches S_{ij} $(i, j \in \{1, 2, 3\})$ which are connected between the phases (Δ-connection).

The three boost inductors L_{Ni} are connected at the input of the rectifier bridge. Together with the boost inductors the three switches S_{ij} are used to generate sinusoidal input currents which are proportional to the mains voltage. Due to the rectifier diodes, a short-circuit of the DC-link voltage is not possible. In contrast to a conventional rectifier bridge the diodes commutate with switching frequency and have to be chosen according to this requirement. Diodes showing a low reverse-recovery current (e.g. SiC-diodes) are essential in order to limit the switching losses of the rectifier system.

For implementation of the bidirectional (current), bipolar (voltage) switches a (single) true bipolar switch would be needed which is unfortunately not commercially available. **Fig. 6.2** shows two possibilities of implementing the bidirectional switches where in **Fig. 6.2((a))** an implementation using two back-to-back connected MOSFETs is shown. In normal operation always one MOSFET and the body diode of the second MOSFET is conducting. The (parasitic) body diode of the MOSFET, however, shows a rather large forward conduction voltage (e.g. $V_{SD} \approx 1\,V$ at $I_{SD} = 10\,A$ for the CoolMOS device IPP60R075CP) which would lead to high conduction losses especially for small currents. These conduction losses can be reduced using the low-resistance path of the MOSFET channel, if the second MOSFET is turned on as well. In **Fig. 6.2((b))** a bidirectional switch using a diode bridge consisting of four diodes and a single MOSFET is given. The disadvantage of this implementation is the fact that always two diodes and the MOSFET are conducting which yields to large conduction losses. The

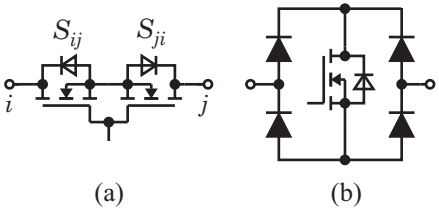
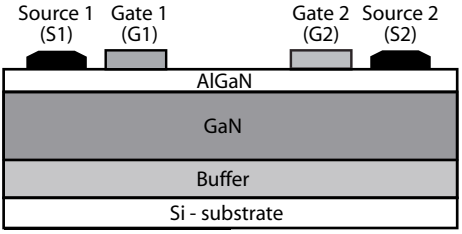


Fig. 6.2: Possible implementations of a bidirectional (current), bipolar (voltage) switch using (a) two back-to-back connected MOSFETs and (b) a MOSFET and a diode bridge.

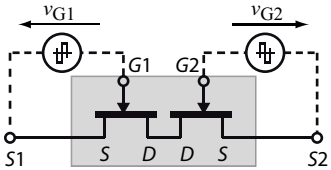
implementation shown in **Fig. 6.2(a)** is hence preferable.

In [252] a true monolithic bidirectional switch with a blocking voltage of 650 V is presented. This switch uses a AlGaN/GaN based gate injection transistor. The structure and corresponding equivalent circuit of such a bidirectional switch is given in **Fig. 6.3**. It is obvious that two gate-drive stages are required in order to be able to block currents in both directions. The switch shows an on-state resistance of $R^*_{\mathrm{DSon}} = R_{\mathrm{DSon}} A_{\mathrm{Chip}} = 0.34\,\Omega\mathrm{mm}^2$ which is much smaller than the R^*_{DSon} of state-of-the-art superjunction devices ($\approx 2.7\,\Omega\mathrm{mm}^2$) and is hence very promising. GaN is a wide bandgap material which means that this technology is capable of high-voltage high-temperature operation. Some information about the material properties and the basic device operation can be found in [253]. Existing designs of AlGaN/GaN devices suited for power electronic applications typically show a lateral implementation where the the GaN layer is grown on either a sapphire, SiC or Si substrate [254] - [255]. Due to the high availability of the Si substrate these approaches seem to have the highest potential for a commercial implementation. GaN transistors using the Si substrate with a break down voltage of 200 V are already commercially available [256] and 600 V versions will follow in the near future.
The lateral implementation shows limited performance regarding higher current and power levels and a vertical implementation as shown in [257] would be able to overcome this drawback. A GaN wafer is needed as substrate for such an implementation and at present its high price is the limiting factor which may change in future.

By application of space vector calculus the discrete converter voltage



(a)



(b)

Fig. 6.3: (a) Cross-section and (b) equivalent circuit of the monolithical bidirectional switch according to [252] based on the 2 dimensional electron gas (2DEG) formed by the AlGaN/GaN heterostructure. For true bidirectional operation two gate-drive stages are required.

space vector can be calculated by

$$\underline{v}_{\mathrm{r}} = \frac{2}{3}(v_{\mathrm{r1}} + \underline{a}v_{\mathrm{r2}} + \underline{a}^2 v_{\mathrm{r3}}) \text{ with } \underline{a} = e^{j\frac{2\pi}{3}} \tag{6.1}$$

where $v_{\mathrm{r}i}$ are the corresponding converter phase voltages. The possible converter voltages $v_{\mathrm{r}i}$ are dependent on the state of the switches s_{ij} ($s_{ij} = 1$ denotes the turn-on state of switch S_{ij}) and on the direction of the input phase currents $i_{\mathrm{N}i}$. Therefore, the available voltage space vectors change over if one of the input currents changes its sign (i.e. every 60° of the mains period). If (s_{12}, s_{23}, s_{31}) describes the different switching states, the resulting voltage space vectors for $\varphi_{\mathrm{N}} \in [-30°, 30°]$ ($i_{\mathrm{N1}} > 0$, $i_{\mathrm{N2}} < 0$, $i_{\mathrm{N3}} < 0$) can be calculated as

$$(000), (010) : \underline{v}_{\mathrm{r}_1} = \frac{2}{3}V_{\mathrm{o}} \tag{6.2}$$

$$(001) : \underline{v}_{\mathrm{r}_2} = \frac{2}{3}V_{\mathrm{o}}e^{-j60°} \tag{6.3}$$

$$(100) : \underline{v}_{\mathrm{r}_3} = \frac{2}{3}V_{\mathrm{o}}e^{j60°} \tag{6.4}$$

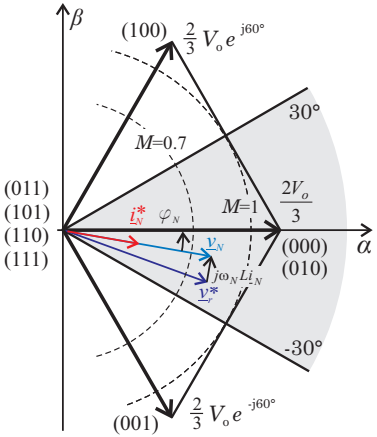


Fig. 6.4: Space vector diagram of the Δ-switch rectifier for the sector $\varphi_N \in [-30°, +30°]$ ($i_{N1} > 0$, $i_{N2} < 0$, $i_{N3} < 0$).

$$(011), (101), (110), (111) : \underline{v}_{r_4} = 0 \tag{6.5}$$

and the resulting voltage space vectors are depicted in **Fig. 6.4**. Also the trajectories of the local average space vector for a modulation index of $M = 1$ (maximal modulation index) and $M = 0.7$ ($V_N = 115\,V$, $V_o = 400\,V$) are shown where the modulation index M is defined as

$$M = \frac{\sqrt{3}\hat{V}_N}{V_o} \ . \tag{6.6}$$

Only states (000), (001), (010) and (100) show a non-zero magnitude and the voltage space vector of (010) is equal to the space vector for state (000). In each 60°-sector there is a redundancy of the (000)-vector and therefore only 4 different voltage space vectors can be generated by the converter in each sector.
These discrete voltage space vectors are used to approximate the converter's voltage reference vector

$$\underline{v}_r^* = \hat{V}_r^* \ e^{j\varphi_{\underline{v}_r^*}} \tag{6.7}$$

in the time average over the pulse-period. In conjunction with the mains voltage system

$$\underline{v}_N = \hat{V}_N \ e^{j\varphi_N} \ , \ \varphi_N = \omega_N t \tag{6.8}$$

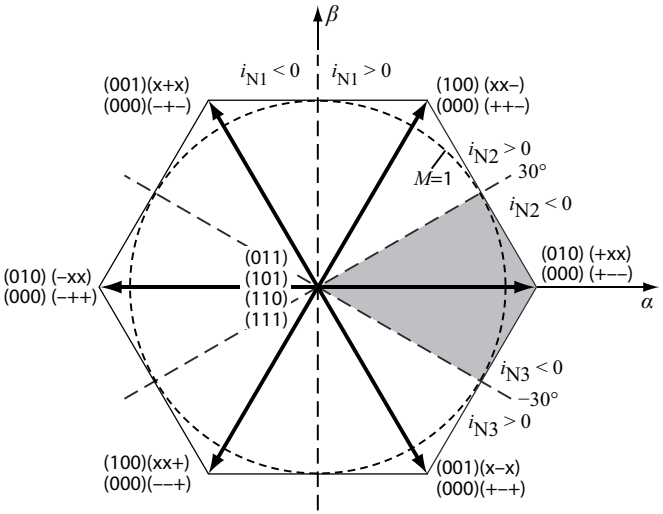


Fig. 6.5: Total available voltage space vectors of the Δ-switch rectifier system. Depending on the input phase current directions only four voltage space vectors can be generated. Each vector is marked with $(s_{12},s_{23},s_{32})(\text{sign}(i_{N1}),\ \text{sign}(i_{N2}),\ \text{sign}(i_{N3}))$ where 1 means that the corresponding switch S_{ij} is turned-on and 0 that it is turned-off. The current direction is marked with +/− for currents flowing into/out of the rectifier system and x that the vector is independent of the current direction of the corresponding phase (cf. **Fig. 6.1**).

the voltage difference

$$\underline{v}_N - \underline{v}_r^* = L\frac{d\underline{i}_N^*}{dt} \tag{6.9}$$

leads to the input current

$$\underline{i}_N^* = \hat{I}_N^*\ e^{j\varphi_{\underline{i}_N^*}}\ , \tag{6.10}$$

if only average values over one pulse period are considered. The controller of the rectifier system therefore has to generate a voltage reference vector $\underline{v}_r^*$ that results in a difference voltage across the boost inductor needed to generate sinusoidal input currents in phase with the mains voltage (more details on the controller implementation are discussed in 6.2.1).

In a three-level Vienna-type rectifier system in comparison, seven non-zero voltage space vectors are available for approximation of $\underline{v}_r^*$.

The two-level Δ-switch rectifier system hence shows a considerably higher current ripple in the boost inductor as the three-level topology. In other words, for the same amount of current ripple a larger boost inductor has to be built for the Δ-switch rectifier.

The total available voltage space vectors are depicted in **Fig. 6.5**. Each vector is marked with (s_{12},s_{23},s_{32})(sign(i_{N1}), sign(i_{N2}), sign(i_{N3})) where 1 means that the corresponding switch S_{ij} is turned-on and 0 that it is turned-off. The current direction is marked with +/– for currents flowing into/out of the rectifier system and x that the vector is independent of the current direction of the corresponding phase.

All voltage space vectors with two or three switches in the on-state short all three input phases on the rectifier side and are therefore redundant. On contrary to the three-level Vienna-type rectifier system, the redundancy cannot be used advantageously and only two switches can hence be used to control the input currents. The remaining switch has to be permanently off during this sector. The required clamping action will be discussed in section 6.2.1.

6.1.1 Switching Sequences

As already discussed the required voltage space vector $\underline{v}_r^*$ has to be approximated in terms of a time-average of the surrounding available converter voltages. It is essential for switching and conduction losses which voltage space vectors are used and particularly in which sequence they are applied. In addition also the generated DM and CM voltages rely on this selection. Basically, only the switching action of one switch should be necessary for a change over from a current switching state (e.g. switching state (000)) to the next switching state (e.g. switching state (100)). Based on this rule still two different reasonable switching sequences can be generated with a minimum number of switching actions in each 60°-sector. **Fig. 6.6** shows the corresponding modulation signals of the bidirectional switches ($\varphi_N = -15°$), and equivalent circuits are given for the time interval where both switches are on. For sequence A ((000)-(001)-(101)-(001)-(000), $S_{23} = \text{OFF}$), the positive input current i_{N1} is shared by S_{12} and S_{31} dependent on the on-states of the switches. In contrast to sequence A, the whole current i_{N1} is carried by switch S_{31} for sequence B ((000)-(001)-(011)-(001)-(000),

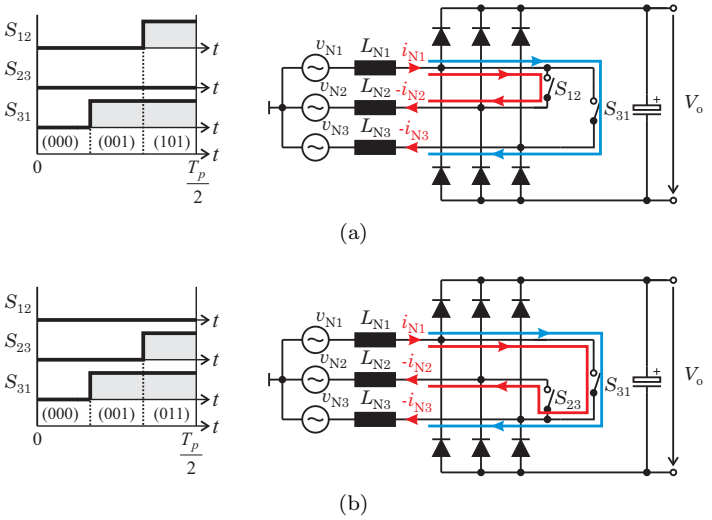


Fig. 6.6: Possible switching sequences for $\varphi_N = -15°$ and equivalent circuits for the time interval where both switches are on; (a) Sequence A: (000)-(001)-(101)-(001)-(000), S_{23} = OFF; (b) Sequence B: (000)-(001)-(011)-(001)-(000), S_{12} = OFF.

TABLE 6.1: Currents through the bidirectional switches for the possible zero vectors at $\varphi_N = -15°$ ($|i_{N1}| > |i_{N2}|, |i_{N3}|$).

State	(011)	(101)	(110)	(111)
$i_{S_{12}}$	0	$-i_{N2}$	i_{N1}	$\frac{1}{3}(i_{N1} - i_{N2})$
$i_{S_{23}}$	i_{N2}	0	$-i_{N3}$	$\frac{1}{3}(i_{N2} - i_{N3})$
$i_{S_{31}}$	$-i_{N1}$	i_{N3}	0	$\frac{1}{3}(i_{N3} - i_{N1})$

S_{12} = OFF) during the state (011). This results in higher conduction losses and therefore sequence A is preferable.

According to **Fig. 6.6(a)** the switch S_{23} is permanently off. This is true for the whole 60°-sector as an easy analysis shows and this switch can be actively clamped to off state during this time interval.
As reported in [258], a further improvement regarding conduction losses can be achieved if all three switches are turned on for implementing the zero state (e.g. (101) for $\varphi_N = -15°$). If equal on-state resistances

of the switches are assumed the phase currents will be equally shared by the three switches which results in reduced switch currents. The corresponding switch currents of the different zero states are listed in **TABLE 6.1**. The instantaneous conduction losses of the switches can in a first approximation be calculated by

$$P_{\mathrm{con}}(t) = R_{\mathrm{DSon}}\Big(i^2_{\mathrm{S}_{12}}(t) + i^2_{\mathrm{S}_{23}}(t) + i^2_{\mathrm{S}_{31}}(t)\Big) \tag{6.11}$$

if equal on-state resistances R_{DSon} are assumed and by use of the different switch currents listed in **TABLE 6.1**, the reduction of the conduction losses is visible. If a linear dependence of the switching losses on the switched current is assumed also no additional switching losses would occur if all three switches are closed during the zero state. Two switching actions are typically required for implementing this zero state. This would be feasible, as the zero vectors itself are not dependent on the switching state of the third switch if already two switches are closed but shows higher complexity in the PWM controller implementation in the DSP. On the other hand, no conduction losses occur in the clamped switch (e.g. S_{23} for $\varphi_{\mathrm{N}} = -15°$) during this $120\,°$ interval. Due to the reduced complexity of the modulation strategy, which clamps always one switch to the off-state, this simple modulation strategy is used in this work instead of closing all three switches during the zero state.

6.1.2 DM/CM Voltages

The Δ-switch rectifier system generates, due to the switching actions, DM as well as CM voltages. The DM voltages are used to force the input phase currents to follow the sinusoidal mains voltages. The CM voltage on the contrary is typically an unwanted effect. CM currents, caused by parasitic elements (e.g. capacitances between the semiconductors and the heat sink and between the heat sink and earth), are often the reason for malfunction of power electronic systems. This intrinsic CM voltage can, however, sometimes advantageously be used to improve the system performance. It can for instance be used to increase the possible modulation range for the three-phase Vienna-type rectifier or to minimize the intrinsic third harmonic current in the connection to the output voltage midpoint of the three-level topology (cf. section 3.1.2).

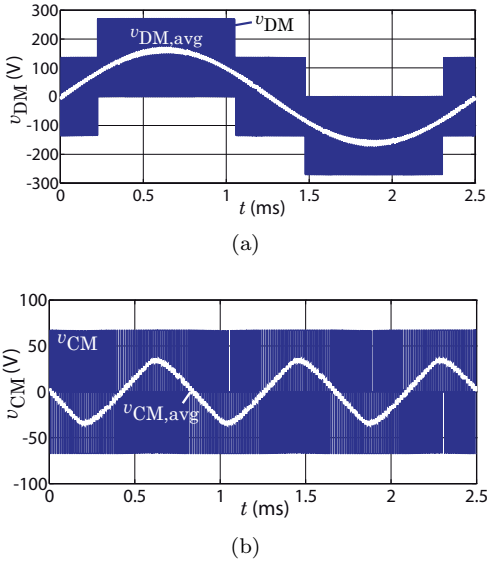


Fig. 6.7: Simulated voltage waveforms of the Δ-switch rectifier system (Parameters: $V_N = 115\,V$, $V_o = 400\,V$, $P_o = 5\,kW$, $f_N = 400\,Hz$ and $f_s = 72\,kHz$); (a) DM voltage and (b) predicted CM voltage if a symmetrical diode bridge (equal leakage currents in the blocking state) is assumed.

The (high-frequency) CM and DM voltages cause high-frequency emissions which are limited by EMI-norms and hence the DM/CM emissions have to be attenuated by a proper EMI filter. The amplitude and shape of the particular DM and CM voltages are used for defining the requirements concerning the EMI filters.

In TABLE 6.2 the voltage space vectors $\underline{v}_r$, phase voltages including CM components v_{ri}, phase voltages without CM components v_{DMi} and the corresponding CM voltage v_{CM} in dependency of the switching state (s_{12}, s_{23}, s_{31}) for $\varphi_N \in [-30°, +30°]$ are listed. The half output voltage $\frac{V_o}{2}$ is used as a virtual reference point for the CM voltage. The DM voltage shows voltage steps with a maximal amplitude of $\frac{2}{3}V_o$ and the CM voltage steps show only an amplitude of $\frac{1}{6}V_o$ for all switching states.
For the case that two or three switches are closed all three input phases are shorted, no bridge diode is conducting and hence no connection

TABLE 6.2: Calculated voltage space vectors $\underline{v}_\mathrm{r}$, phase voltages including CM components $v_{\mathrm{r}i}$ phase voltages $v_{\mathrm{DM}i}$ without CM components and CM voltage v_CM in dependency of the switching state (s_{12}, s_{23}, s_{31}) for $\varphi_\mathrm{N} \in [-30°, +30°]$.

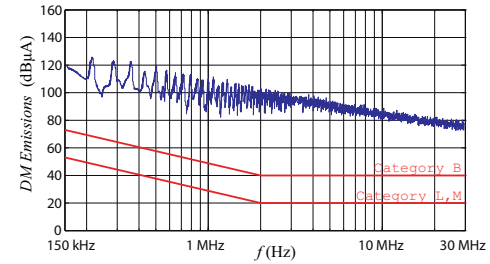
	$v_{\mathrm{r}1}$	$v_{\mathrm{r}2}$	$v_{\mathrm{r}3}$	$v_{\mathrm{DM}1}$	$v_{\mathrm{DM}2}$	$v_{\mathrm{DM}3}$	v_CM	$\underline{v}_\mathrm{r}$
(0 0 0)	$\frac{1}{2}V_\mathrm{o}$	$-\frac{1}{2}V_\mathrm{o}$	$-\frac{1}{2}V_\mathrm{o}$	$\frac{2}{3}V_\mathrm{o}$	$-\frac{1}{3}V_\mathrm{o}$	$-\frac{1}{3}V_\mathrm{o}$	$-\frac{1}{6}V_\mathrm{o}$	$\frac{2}{3}V_\mathrm{o}$
(0 0 1)	$\frac{1}{2}V_\mathrm{o}$	$-\frac{1}{2}V_\mathrm{o}$	$\frac{1}{2}V_\mathrm{o}$	$\frac{1}{3}V_\mathrm{o}$	$-\frac{2}{3}V_\mathrm{o}$	$\frac{1}{3}V_\mathrm{o}$	$\frac{1}{6}V_\mathrm{o}$	$\frac{2}{3}V_\mathrm{o}e^{-j60°}$
(0 1 0)	$\frac{1}{2}V_\mathrm{o}$	$-\frac{1}{2}V_\mathrm{o}$	$-\frac{1}{2}V_\mathrm{o}$	$\frac{2}{3}V_\mathrm{o}$	$-\frac{1}{3}V_\mathrm{o}$	$-\frac{1}{3}V_\mathrm{o}$	$-\frac{1}{6}V_\mathrm{o}$	$\frac{2}{3}V_\mathrm{o}$
(1 0 0)	$\frac{1}{2}V_\mathrm{o}$	$\frac{1}{2}V_\mathrm{o}$	$-\frac{1}{2}V_\mathrm{o}$	$\frac{1}{3}V_\mathrm{o}$	$\frac{1}{3}V_\mathrm{o}$	$-\frac{2}{3}V_\mathrm{o}$	$\frac{1}{6}V_\mathrm{o}$	$\frac{2}{3}V_\mathrm{o}e^{j60°}$
(0 1 1)	0	0	0	*)	*)	*)	*)	0
(1 0 1)	0	0	0	*)	*)	*)	*)	0
(1 1 x)	0	0	0	*)	*)	*)	*)	0

*) CM voltage is not defined by the switching state - only by parasitic elements.

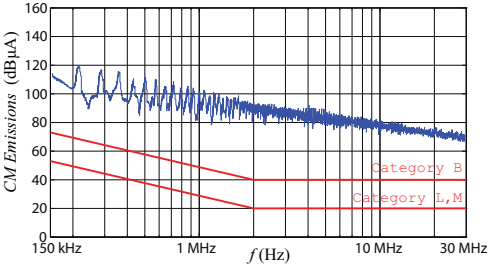
between the DC side and the AC side exists. The CM voltage is therefore not defined by the switching states during this time period. A CM voltage will appear in practice which depends on parasitic circuit elements (e.g. leakage currents of the blocking rectifier diodes $D_{i\mathrm{p}}$ and $D_{i\mathrm{n}}$, parasitic capacitances of the semiconductors to the heat sink, etc.,). The required attenuation of the CM filter stage has thus to be analyzed carefully at the practically implemented prototype. It also has to be noted that the Δ-switch rectifier topology is not able to actively generate a CM voltage. This can be verified if the amplitude of the mains voltage is assumed to be zero. In this case no CM voltage can be generated by any switching actions due to the Δ-connection of the switches and due to the missing connection to the output.

If equal leakage currents of the blocking rectifier bridge diodes are assumed and if parasitic capacitances to the heat sink or to earth are neglected, the DM and CM voltage waveforms can be determined by simulation. The nominal operation point of the intended application ($V_{\mathrm{N}} = 115\,\mathrm{V}$, $V_{\mathrm{o}} = 400\,\mathrm{V}$, $P_{\mathrm{o}} = 5\,\mathrm{kW}$, $f_{\mathrm{N}} = 400\,\mathrm{Hz}$ and $f_{\mathrm{s}} = 72\,\mathrm{kHz}$) is chosen for this simulation and the results are plotted in **Fig. 6.7**. The calculated DM voltage steps with a magnitude of $\frac{2}{3}V_{\mathrm{o}}$ the CM voltage steps with an amplitude of $\frac{1}{6}V_{\mathrm{o}}$ can be verified for the case of an ideal symmetrical system. The average DM voltage $v_{\mathrm{DM,avg}}$, averaged over one pulse period T_{p} is of sinusoidal shape which is needed in order to achieve sinusoidal input currents. It is also obvious that the applied modulation scheme (cf. section 6.2.1) yields to a third harmonic triangular shaped low-frequency CM part. The CM voltage waveform, however, changes completely if parasitic capacitances are considered.

At least for the design of the DM filter stage the voltage waveform shown in **Fig. 6.7** can be used to apply the filter design procedure presented in section 5.7. By application of the calculation scheme given in [229] the peak weighted DM an CM spectra can be determined. In the EMI standard DO160F [31], however, noise current limits are given. The resulting voltages noise spectra have been used in combination with the frequency dependent impedance of the LISN ($50\,\mu\mathrm{H}$, $50\,\Omega$) to calculate the noise currents. The results of this calculation process are plotted in **Fig. 6.8** together with the limits listed in the EMI standard DO160F. Due to the chosen switching frequency of $f_{\mathrm{s}} = 72\,\mathrm{kHz}$, the third switching frequency harmonic ($3f_{\mathrm{s}} = 216\,\mathrm{kHz}$) is the first harmonic which is



(a)



(b)

Fig. 6.8: Calculated peak detection weighted current noise spectra using the simulated DM and CM voltages of **Fig. 6.7**; (a) DM noise spectrum and (b) predicted CM noise spectrum provided that a symmetrical diode bridge exists.

covered by the EMI norm. This harmonic presents the highest DM as well as CM noise peak and the envelope of further noise peaks decreases approximately with -23 dB/decade. This can be used to calculate the required frequency dependent attenuation of the DM and CM EMI filter stage

$$A_{\mathrm{DM/CM}}[\mathrm{dB}](f) = i_{\mathrm{DM/CM}}(f)[\mathrm{dB}\mu\mathrm{A}] - Limit[\mathrm{dB}\mu\mathrm{A}] + margin[\mathrm{dB}], \tag{6.12}$$

where typically a margin of 6 dB is included. The required attenuation of the DM and CM filter stage can therefore be calculated as a function of the frequency and the results are plotted in **Fig. 6.9**. The highest attenuation has to be provided at the kink in the EMI standard at 2 MHz.

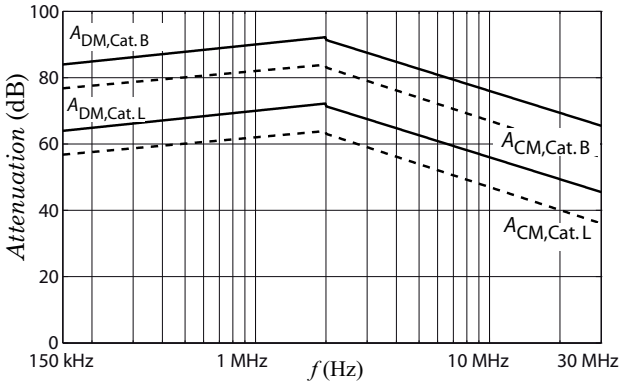


Fig. 6.9: Required attenuation of the DM and CM filter stage in order to fulfill EMI noise limits of the EMI standard DO160F.

6.2 Control of the Delta-Switch Rectifier System

In this section the control of the Δ-switch rectifier system will be discussed. The controller has to force the input currents to follow the sinusoidal input mains voltages and has to ensure a constant output voltage. In addition it has to ensure a stable and safe operation under a wide range of load conditions including no-load condition and the rectifier system must be able to deal with a distorted or unsymmetrical mains voltage. Several concepts for the control of three-phase rectifiers exist and a survey of these methods can be found in [213]. In this work a cascade control consisting of a three-phase current controller and a superimposed voltage controller will be analyzed. Several possibilities for implementing a three-phase current controller exist and the capability of the different concepts will be evaluated in section 6.2.1.
The modulator, generating the corresponding gate signals of the switches, plays an important role in the control loop. As will be shown in this section, a PWM modulator using a proper carrier signal is able to implement the optimized switching sequence derived in section 6.1.1. A stability analysis of the current controller and the design of a proper output voltage controller are discussed as well. In order to ensure a high reliability of the rectifier system the controller must be able to handle a single-phase loss and further operation at a reduced power level.

6.2.1 PWM Current Controller

The aim of the current controller is to force the input currents of each phase to follow the (sinusoidal) mains voltages and to ensure that the low frequency input current harmonics stay below the limits listed in [31].
A control method for the Δ-switch rectifier based on low switching frequencies is given in [259] but cannot be used for the desired application due to the high mains current harmonics.
A hysteresis controller as shown in [88] would be an easy way to control the rectifier system, but its varying switching frequency increases the effort of EMI filtering. A controller implementation using the one-cycle control method is presented in [260], but there the controller structure has to be changed over every 60° and the input current control is always limited to two phases.
In [261, 86] a PWM control method for the rectifier system is proposed but no information was given about the exact switching sequence of the switches, which mainly influences the efficiency of the rectifier system. Hence, a control scheme using a PWM modulator is derived in this section which automatically implements the optimal switching sequence as discussed in section 6.1.1.

The Δ-connected switches directly influence the line-to-line voltages. The idea of controlling virtual Δ-currents is therefore near at hand but is unfortunately not very convenient due to the necessary clamping actions caused by the large number of redundant switching states. This can be avoided if the phase currents $i_{\mathrm{N}i}$ of the rectifier are controlled. The resulting phase-oriented modulation signals then have to be transferred to Δ-oriented quantities.
The high redundancy of the switching states, more precisely the fact that all switching states where two or three switches are closed, i.e. all three mains phases are shortened by the bidirectional switches and no current flows from the mains-side to the DC-side, result in an equal voltage space vector with a magnitude of zero (cf. **Fig. 6.5**), prohibits a direct implementation of the phase-oriented control method. As discussed in section 6.1.1, switching sequence A should be implemented by the current controller and it has been shown that for instance during the 60°-sector $\varphi_{\mathrm{N}} \in [-30°, +30°]$ the switch S_{23} has to be clamped to the off state. In this way all three phase currents can be controlled

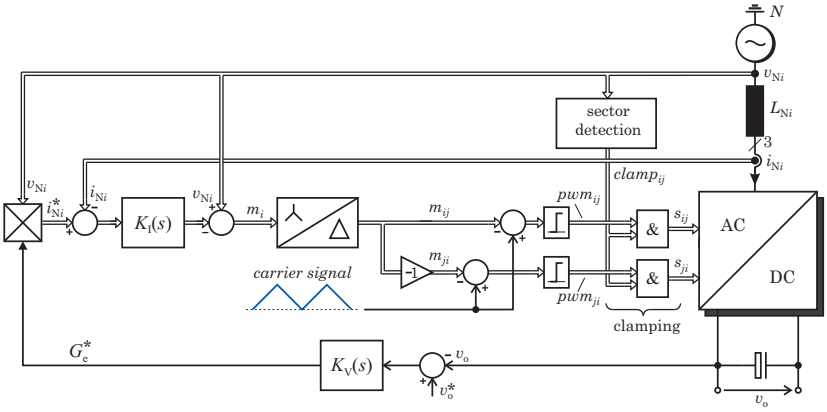


Fig. 6.10: Structure of the proposed cascaded control including the phase-oriented PWM current control. Signal paths being equal for all three phases are shown by double lines.

permanently and the necessary clamping actions are performed in a final logic unit just before the PWM signals s_{ij} are transferred to the switches. This shows the advantage that the structure of the current controller does not need to be changed for different 60 °-sectors of the mains period.

The structure of the proposed controller is shown in **Fig. 6.10**. All three input currents $i_{\mathrm{N}i}$ are sensed by appropriate current sensors and compared with the corresponding reference currents $i^*_{\mathrm{N}i}$. The reference currents are generated by multiplying the mains voltages $v_{\mathrm{N}i}$ by a reference conductance G^*_{e} which is defined by the superimposed output voltage controller $K_{\mathrm{V}}(s)$. The output voltage controller is typically implemented as a PI-type controller in order to avoid steady state deviations. Due to the multiplication with the G^*_{e}, ohmic input current behavior is achieved.

Together with a mains voltage feedforward signal [118], the current controller $K_{\mathrm{I}}(s)$, implemented as P-type controller, generates the required converter phase voltages $v^*_{\mathrm{r}i}$ or the phase related modulations signals m_i or both. The bidirectional switches are connected between

two phases and therefore the equivalent line-to-line modulations signals

$$\begin{aligned} m_{12} &= m_1 - m_2 \\ m_{23} &= m_2 - m_3 \\ m_{31} &= m_3 - m_1 \end{aligned} \tag{6.13}$$

are required for PWM generation which correspond to the line-to-line voltages v_{ij}.
The star-Δ transformation is followed by two pulse-width modulators which generate the PWM signals for the MOSFETs of the bidirectional switches. The bidirectional switches are implemented according to **Fig. 6.2(a)**. In general, dependent on the current direction of the bidirectional switch, only one MOSFET has to be gated. If the second MOSFET is permanently off during this time, the current is carried by its body diode. The body diode shows a relative large forward voltage drop which yields to higher conduction losses. These losses can be reduced by the low-resistance path of the MOSFET channel, if the second MOSFET is turned on as well. This reduction of conduction losses is only possible until the voltage drop over the MOSFET channel $R_{\mathrm{DSon}} i_{\mathrm{DS}}$ is larger than the forward voltage of the body diode. Higher drain source currents are shared by the body diode and the channel of the MOSFET. The current direction of the switch only changes every 120° and this MOSFET can therefore be permanently on during this time interval. Two independent PWM signals are hence required for the bidirectional switches. As shown in **Fig. 6.2(a)**, MOSFET S_{ij} connects port i of the bidirectional switch to port j and its PWM signals are defined by pwm_{ij}. The operation of the modulator will be discussed in the next section.

The clamping actions are controlled by a sector-detection unit which derives the clamping signals $clamp_{ij}$ from the mains voltage. The resulting clamping actions considering all 60°-sectors are summarized in TABLE 6.3 for all MOSFETs, where i.e. 0 indicates that the corresponding MOSFET is permanently off in this sector. The clamping action signals can easily be derived from the mains line-to-line voltages. According to **Fig. 6.11** the bidirectional switch of the phase with the smallest line-to-line voltage amplitude absolute value has to be clamped to off-state which is very easy to perform in the DSP.

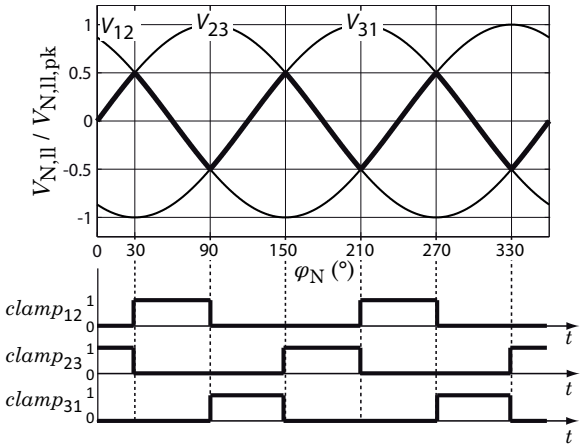


Fig. 6.11: Determination of the required clamping actions from the line-to-line mains voltages. $clamp_{ij} = 1$ means that the corresponding switch S_{ij} is clamped to off state.

TABLE 6.3: Required clamping actions; 0 indicates that the corresponding MOSFET is off for the whole interval; 1 indicates a continuous turn-on in the considered interval and pwm_{ij} that the MOSFET is modulated by the current controller.

	s_{12}	s_{21}	s_{23}	s_{32}	s_{13}	s_{31}
330° ... 30°	pwm_{12}	1	0	0	pwm_{13}	1
30° ... 90°	0	0	pwm_{23}	1	pwm_{13}	1
90° ... 150°	1	pwm_{21}	pwm_{23}	1	0	0
150° ... 210°	1	pwm_{21}	0	0	1	pwm_{31}
210° ... 270°	0	0	1	pwm_{32}	1	pwm_{31}
270° ... 330°	pwm_{12}	1	1	pwm_{32}	0	0

6.2.2 PWM Modulator

A space vector control method, calculating the particular turn-on times and switching sequences, would be a possibility to operate and control the rectifier system. This is, however, a time consuming task in the digital controller and limits the rectifiers switching frequency. In the following a PWM modulation scheme is presented which automatically

selects the desired voltage space vectors and implements the preferable switching sequences.

On one hand the modulator has to assure the optimal switching sequence and on the other hand it has to generate the duty cycles

$$\begin{aligned} v^*_{\mathrm{r}ij}(t) > 0: \;\; \delta_{ij}(t) &= 1 - \frac{v^*_{\mathrm{r}ij}(t)}{V_\mathrm{o}} = 1 - m_{ij}(t) \\ \delta_{ji}(t) &= 1 \end{aligned} \tag{6.14}$$

$$\begin{aligned} v^*_{\mathrm{r}ij}(t) < 0: \;\; \delta_{ij}(t) &= 1 \\ \delta_{ji}(t) &= 1 - \frac{v^*_{\mathrm{r}ji}(t)}{V_\mathrm{o}} = 1 - m_{ji}(t) \; . \end{aligned} \tag{6.15}$$

By use of the modulation index M defined in (6.6) the ideal modulation functions based on perfectly sinusoidal mains voltages are given by

$$m_{ij}(\varphi_\mathrm{N}) = M \cos\left(\varphi_\mathrm{N} - \frac{2\pi}{3}(i-1) + \frac{\pi}{6}\right) \; . \tag{6.16}$$

A single unipolar triangular carrier signal is used for implementation of the PWM modulator (cf. **Fig. 6.12**). As for the Vienna-type rectifier system a sawtooth carrier signal would not yield to the optimized switching sequences. The modulation signal m_{ij} is compared to the triangular carrier signal and if the carrier signal exceeds m_{ij}, the output of the modulator is changing to the high state. Unlike the unipolar triangle signal, the modulation signals m_{ij} are bipolar and hence a duty cycle of 100% is generated for negative modulation voltages. According to

$$m_{ij} = (-1) \cdot m_{ji} \; , \tag{6.17}$$

one MOSFET of the bidirectional switch is always permanently on (e.g. S_{21} for $\varphi_\mathrm{N} \in [-30°, 30°]$), which reduces the on-state losses of the bidirectional switch. The required clamping actions to ensure the continuous on-state (as listed in **TABLE 6.3**) are therefore automatically performed by the modulator and no additional clamping logic is needed. **Fig. 6.12** shows the operation of the pulse-width modulator at $\varphi_\mathrm{N} = -15°$. The two modulation signals m_{21} and m_{31} are negative and result in a duty cycle of 100%. According to TABLE 6.3, switches S_{23} and S_{32} are permanently off in this sector and are therefore not shown.

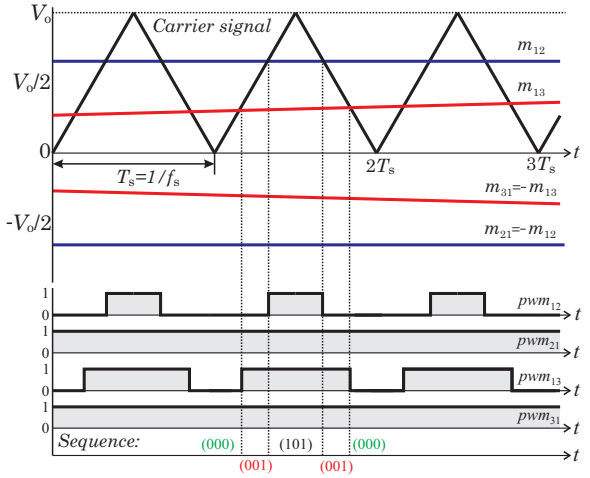


Fig. 6.12: PWM modulation and resulting switching sequence at $\varphi_N = -15°$. Switches S_{23} and S_{32} are not shown as they are continuous off in this sector. The resulting (optimal) switching sequence is (000)-(001)-(101)-(001)-(000).

The remaining modulation signals m_{12} and m_{13} are used and result in the desired optimal switching sequence (000)-(001)-(101)-(001)-(000) (see also **Fig. 6.6**).

6.2.3 Simulation Results

A digital computer simulation using the simulation software Gecko [262] is performed to confirm the operation of the proposed control concept. A P-type controller is used to implement the current control which will be discussed in section 6.3. **Fig. 6.13** demonstrates a good performance of the proposed concept at an input frequency of $f_N = 800\,\text{Hz}$ ($V_{Ni} = 115\,V_{rms}$, $V_o = 400\,V_{DC}$, $P_o = 5\,\text{kW}$, $L_{Ni} = 330\,\mu\text{H}$). The input currents i_{Ni} follow the sinusoidal 800 Hz input voltages V_{Ni}, even for a rather low switching frequency of 72 kHz. The current ripple of the clamped phase is furthermore not higher than in the two controlled phases. It has to be mentioned again that the current controller works permanently, i.e without any structural changes over the mains period, and that only a logic-block just before the modulator output provides the necessary clamping actions.

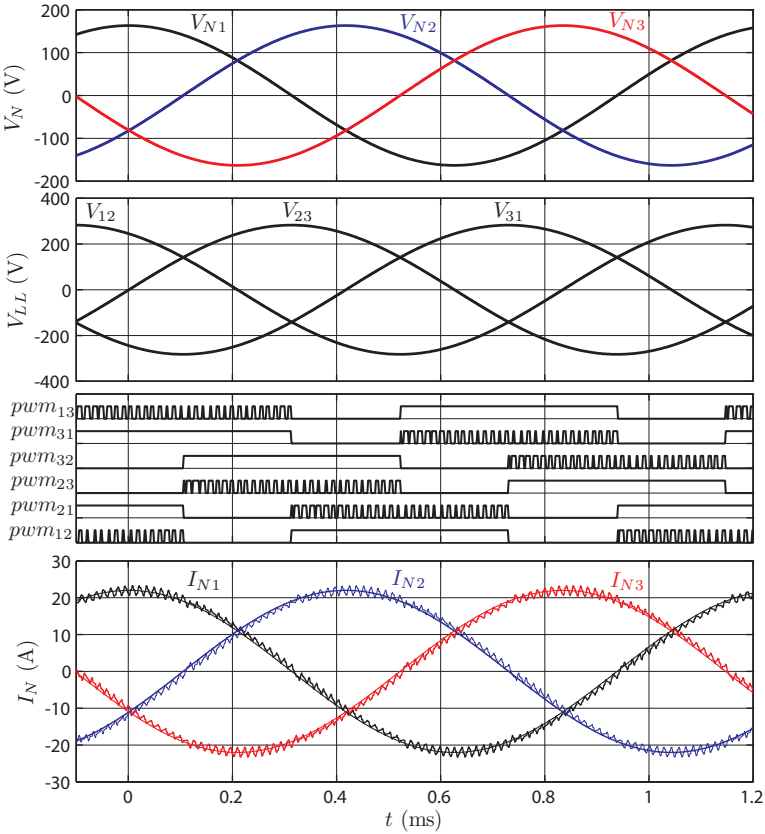


Fig. 6.13: Simulation results of the Δ-switch rectifier; (a) $V_{\mathrm{N}i} = 115\,\mathrm{V}$, $f_{\mathrm{N}} = 800\,\mathrm{Hz}$, $V_{\mathrm{o}} = 400\,\mathrm{V}$, $P_{\mathrm{o}} = 5\,\mathrm{kW}$, $L_{\mathrm{N}i} = 330\,\mu\mathrm{H}$

6.3 Controller Design

In order to be able to design the voltage and current controller adequate models of the rectifier system are required. The digital controller will be implemented using a DSP and sampling effects and delay times caused by the calculation time of this digital implementation have to be considered for the stability analysis of the controller loops. Due to sampling of the analog signals the phase margin of the system may be reduced considerably and a system model neglecting these effects will

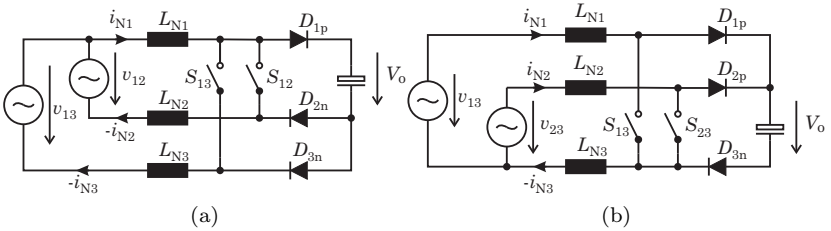


Fig. 6.14: Equivalent dual-boost circuits for (a) $\varphi_N \in [-30°, +30°]$ and (b) $\varphi_N \in [30°, 90°]$.

not yield to an optimal control of the rectifier system.

6.3.1 Current Controller Design

Prior the design of a proper current controller, an appropriate model of the three-phase rectifier system is needed. The three switches are connected between the phases which means that all three currents are directly affected by the switching action of one bidirectional switch. Due to the high redundancy of voltage space vectors one switch is always continuously clamped to the off-state in a 60 °-sector. An equivalent circuit consisting of two boost circuits (dual-boost circuit), as already shown in [260], can be drawn for each sector. **Fig. 6.14(a)** shows the resulting dual boost circuit for $\varphi_N \in [-30°, +30°]$. The input voltages v_{12} and v_{13} show positive values and the input current i_{N1} shows positive direction whereas the input currents i_{N2} and i_{N3} show negative direction. Switches S_{12} and S_{13} are pulse-width modulated and according to **TABLE 6.3** the switches S_{23} and S_{23} are clamped to the off-state. It is obvious that the boost inductor L_{N1} and the rectifier diode D_{1p} are shared by the two virtual boost circuits. **Fig. 6.14(b)** shows the equivalent dual-boost circuit for the sector $\varphi_N \in [30°, 90°]$.

An analysis of all sectors shows that for each sector a corresponding equivalent dual-boost circuit similar to the circuits given **Fig. 6.14** can be derived. A dual-boost circuit according to **Fig. 6.14(a)** can be derived for sectors $\varphi_N \in \{[-30°, 30°], [90°, 150°], [210°, 270°]\}$, whereas sectors $\varphi_N \in \{[30°, 90°], [150°, 210°], [270°, 330°]\}$ can be modeled by **Fig. 6.14(b)**. The resulting parameters of the dual-boost circuits for

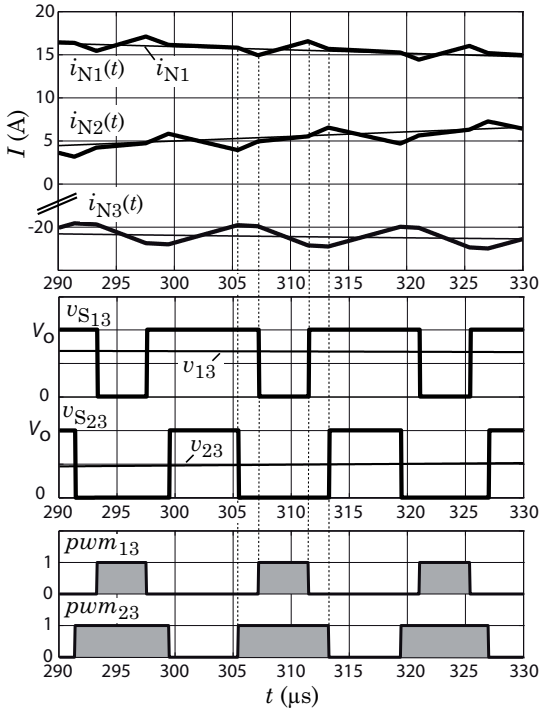


Fig. 6.15: Simulated voltage and current waveforms for $\varphi_N = 45\,^\circ$ System parameters: $V_N = 115\,\text{V}$, $V_o = 400\,\text{V}$, $f_N = 400\,\text{Hz}$, $L_N = 330\,\mu\text{H}$ and $P_o = 5\,\text{kW}$).

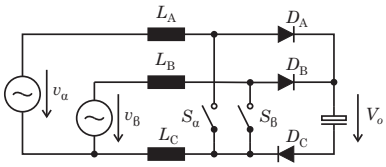
each sector are listed in **TABLE 6.4**.

In the following a model for sector $\varphi_N \in [30°, 90°]$ is derived. The approach can be applied in a similar manner to the other sectors.

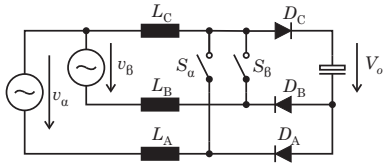
Average mode control will be used to control the rectifier system. This means that all signals are averaged over one switching period. **Fig. 6.15** shows the simulated voltage and current waveforms around $\varphi_N = 45\,^\circ$ ($V_N = 115\,\text{V}$, $V_o = 400\,\text{V}$, $f_N = 400\,\text{Hz}$, $L_N = 330\,\mu\text{H}$ and $P_o = 5\,\text{kW}$), where $v_{S_{13}}$ and $v_{S_{23}}$ are the corresponding voltage waveforms of the bidirectional switches and v_{13} and v_{23} are the line-to-line mains voltages. The averaged input current $i_{N1,avg}$ for instance can be calculated using

$$i_{N1,avg} = \frac{1}{T_s} \int_0^{T_s} i_{N1}(t)\, dt \tag{6.18}$$

TABLE 6.4: Equivalent dual-boost circuits of the Δ-switch rectifier and corresponding circuit elements for each 60 °-sector.



Circuit C_1



Circuit C_2

φ_N	Circuit	v_α	v_β	L_A	L_B	L_C	S_α	S_β	D_A	D_B	D_C
$-30° \ldots 30°$	C_2	v_{12}	v_{13}	L_{N2}	L_{N3}	L_{N1}	S_{12}	S_{13}	D_{2n}	D_{3n}	D_{1p}
$30° \ldots 90°$	C_1	v_{13}	v_{23}	L_{N1}	L_{N2}	L_{N3}	S_{13}	S_{23}	D_{1p}	D_{2p}	D_{3n}
$90° \ldots 150°$	C_2	v_{21}	v_{23}	L_{N1}	L_{N3}	L_{N2}	S_{21}	S_{23}	D_{1n}	D_{3n}	D_{2p}
$150° \ldots 210°$	C_1	v_{21}	v_{31}	L_{N2}	L_{N3}	L_{N1}	S_{21}	S_{31}	D_{2p}	D_{3p}	D_{1n}
$210° \ldots 270°$	C_2	v_{32}	v_{31}	L_{N2}	L_{N1}	L_{N3}	S_{32}	S_{31}	D_{2n}	D_{1n}	D_{3p}
$270° \ldots 330°$	C_1	v_{12}	v_{32}	L_{N1}	L_{N3}	L_{N2}	S_{12}	S_{32}	D_{1p}	D_{3p}	D_{2n}

where $T_\mathrm{s} = 1/f_\mathrm{s}$ is one pulse period. In the following, only i_N1 is written instead of i_N1avg for a better readability but means the averaged value over one pulse period. Averaging over one pulse period and application of Kirchhof's law on the circuit given in **Fig. 6.14(b)** results in

$$\begin{aligned} v_{13} - L_\mathrm{N1}\frac{di_\mathrm{N1}}{dt} + L_\mathrm{N3}\frac{di_\mathrm{N3}}{dt} &= (1-\delta_{13})\,V_\mathrm{o} \\ v_{12} - L_\mathrm{N1}\frac{di_\mathrm{N1}}{dt} + L_\mathrm{N2}\frac{di_\mathrm{N2}}{dt} &= (1-\delta_{12})\,V_\mathrm{o} \end{aligned} \tag{6.19}$$

where $(1-\delta_{13})\,V_\mathrm{o}$ is the averaged voltage across switch S_{13}. The forward voltage drops of the switches and diodes are neglected in (6.19). Due to the missing neutral wire connection in addition

$$i_\mathrm{N1} + i_\mathrm{N2} + i_\mathrm{N3} = 0 \tag{6.20}$$

has to be satisfied. The output voltage controller ensures a constant output voltage V_o which is in most cases fulfilled (except during load transients). In a first approach V_o is assumed to be constant so that the nonlinear equation (6.19) gets linear. The Laplace transform can therefore be applied and if equal boost inductors $L_\mathrm{N1} = L_\mathrm{N2} = L_\mathrm{N3} = L_\mathrm{N}$ are assumed (6.19) and (6.20) yield to

$$\begin{aligned} v_{13} - i_\mathrm{N1}L_\mathrm{N}s + i_\mathrm{N3}L_\mathrm{N}s &= (1-\delta_{13})\,V_\mathrm{o} \\ v_{12} - i_\mathrm{N1}L_\mathrm{N}s + i_\mathrm{N2}L_\mathrm{N}s &= (1-\delta_{12})\,V_\mathrm{o} \\ i_\mathrm{N1} + i_\mathrm{N2} + i_\mathrm{N3} &= 0 \end{aligned} \tag{6.21}$$

This simplification yields to an easy model for current control where the impacts of output voltage variations or saturation effects of the boost inductors are not considered. Solving (6.21) results in

$$\begin{aligned} \begin{pmatrix} i_\mathrm{N1} \\ i_\mathrm{N2} \\ i_\mathrm{N3} \end{pmatrix} = \frac{V_\mathrm{o}}{L_\mathrm{N}s} \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} \\ -\frac{1}{3} & -\frac{1}{3} \end{pmatrix} \begin{pmatrix} \delta_{13} \\ \delta_{23} \end{pmatrix} + \frac{V_\mathrm{o}}{L_\mathrm{N}s} \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} \\ -\frac{1}{3} & -\frac{1}{3} \end{pmatrix} \begin{pmatrix} v_{13} \\ v_{23} \end{pmatrix} + \\ + \frac{V_\mathrm{o}}{L_\mathrm{N}s} \begin{pmatrix} -\frac{1}{3} \\ -\frac{1}{3} \\ \frac{2}{3} \end{pmatrix}. \end{aligned} \tag{6.22}$$

According to (6.22), the input currents are dependent on the duty-cycles δ_{ij}, the line-to-line mains voltages v_{ij} and the output voltage V_o. Using

the modulation function m_{12} the duty cycle is defined by

$$\delta_{ij} = 1 - m_{ij} \ . \tag{6.23}$$

The Δ-related modulation functions are given by

$$m_{ij} = m_i - m_j \tag{6.24}$$

where the corresponding duty cycles of the virtual single-phase systems are

$$\delta_i = 1 - m_i \ . \tag{6.25}$$

In the final controller implementation an input voltage feedforward part is used in conjunction with a P-type controller. The mains phase voltage v_i, related to the output voltage V_o, is there added to the output of the current controller m_i

$$m_{i,\mathrm{ff}} = \left(m_i + \frac{v_\mathrm{i}}{V_\mathrm{o}} \right) \ . \tag{6.26}$$

After a short calculation the Δ-related duty-cycles δ_{ij} result in

$$\delta_{ij,\mathrm{ff}} = 1 + \delta_i - \delta_j - \frac{v_{ij}}{V_\mathrm{o}} \ . \tag{6.27}$$

By use of (6.27), the input currents can be described as a function of the phase related duty-cycles

$$\boldsymbol{i_\mathrm{N}} = \begin{pmatrix} i_{\mathrm{N}1} \\ i_{\mathrm{N}2} \\ i_{\mathrm{N}3} \end{pmatrix} = \frac{V_\mathrm{o}}{L_{\mathrm{N}\mathrm{S}}} \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{pmatrix} \begin{pmatrix} \delta_1 \\ \delta_2 \\ \delta_3 \end{pmatrix} = \mathbf{G}(s)\ \boldsymbol{\delta} \tag{6.28}$$

where $\mathbf{i_N}$ and $\boldsymbol{\delta}$ are vectors and the 3×3 matrix $\mathbf{G}(s)$ is the multiple input/multiple output (MIMO) small signal average mode transfer function describing the Δ-switch rectifier system.
It is obvious that not only the elements $G_{ii}(s)$ but also elements outside of the main diagonal $\mathrm{G}_{ij}(s)|_{i \neq j}$ are not zero. This means that for instance a change in the duty-cycle δ_1 does not only take effect just on the phase current $i_{\mathrm{N}1}$ but also on the input currents $i_{\mathrm{N}2}$ and $i_{\mathrm{N}3}$.
The reason for this strong coupling can be explained by use of (6.20). Due to the missing neutral connection of the rectifier system the sum

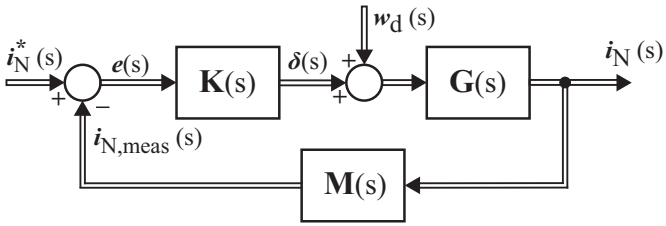


Fig. 6.16: Multiple-input multiple-output controller loop of the rectifier system consisting of the controller $\mathbf{K}(s)$, model of the rectifier system $\mathbf{G}(s)$ and current measurement $\mathbf{M}(s)$. The vector $\boldsymbol{w}_\mathrm{d}(s)$ models a disturbance in the duty cycle.

of all three input currents is forced to zero. A change of the duty-cycle δ_1 therefore result in a change of input current $i_{\mathrm{N}1}$ which automatically affects the currents $i_{\mathrm{N}2}$ and $i_{\mathrm{N}3}$. Due to this circumstance the cross couplings are physical in nature and cannot be neglected.
The elements in the main diagonal of $\mathbf{G}(s)$ are equal and the elements outside of the principle diagonal are equal which results in a symmetrical system behavior. The step responses on δ_1 and the step responses on δ_2 are equal with respect to the corresponding phase current $i_{\mathrm{N}i}$.

The matrix $\mathbf{G}(s)$ given in (6.28) was only derived for the sector $\varphi_\mathrm{N} \in [30°, 90°]$ and is only valid in this sector. However, due to the symmetry of the system all sectors result in the same transfer matrix (6.28) as can easily be verified by repetition of the calculation for other sectors.

Because of the non-zero non-diagonal elements of $\mathbf{G}(s)$ in general a multivariable controller $\mathbf{K}(s)$ (3×3 matrix) has to be designed. Nine controller elements $K_{ij}(s)$ would have to be determined in order to implement a proper controller. The multivariable controller structure is depicted in **Fig. 6.16**, where $\mathbf{G}(s)$ is the derived model of the rectifier system, $\mathbf{K}(s)$ is the multivariable controller and $\mathbf{M}(s)$ is the transfer function of the current measurement. It is assumed that the measurement systems are not coupled and that $\mathbf{M}(s)$ is a diagonal matrix. The vector $\boldsymbol{w}_\mathrm{d}(s)$ models a possible disturbance in the duty cycle generation (e.g. turn-off delays of the MOSFETs).
As for single-phase control systems the poles of the multivariable control systems are decisive. They can be calculated by solving the character-

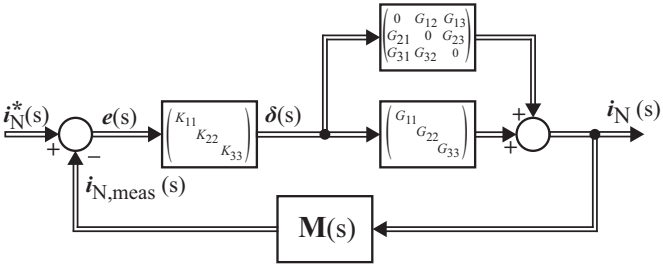


Fig. 6.17: Control loop illustrating the basic idea of the direct Nyquist control design method. The three controller elements $K_{ii}(s)$ are designed according to the main diagonal elements $G_{ii}(s)$. The operating controller, however, has to deal with the full system $\mathbf{G}(s)$.

istic equation

$$\det\left[\mathbf{I} + \mathbf{G}(s)\mathbf{K}(s)\mathbf{M}(s)\right] \;=\; 0\;. \tag{6.29}$$

All poles have to lie in the left (negative) half-plane for stability of the multivariable control system. A return difference matrix

$$\mathbf{F}(s) = \left[\mathbf{I} + \mathbf{G}(s)\mathbf{K}(s)\mathbf{M}(s)\right] \tag{6.30}$$

can be defined which will be used below.

An easy approach for controller design is to ignore the cross-couplings of $\mathbf{G}(s)$ in a first step. The multivariable control problem then simplifies to three independent single-input single-output (SISO) control systems according to the elements $G_{ii}(s)$ and the influence of the remaining cross-couplings have to be analyzed carefully after the controller elements have been designed. **Fig. 6.17** illustrates the basic idea of this control method [263]. The precondition for this control approach are loose cross-couplings of $\mathbf{G}(s)$ and the amount of cross-coupling can be estimated by calculation of the corresponding Gershgorin bands. The Gershgorin-theorem states that the eigenvalues of the return difference matrix $\mathbf{F}(s)$ lie in bands with the radii

$$D_j(j\omega) = \sum_{j=1, j\neq i}^{m} \left|F_{ij}(j\omega)\right|\;. \tag{6.31}$$

The following design method will be used below:

1. Design of three single-phase controllers $K_{ii}(s)$ which show, together with the diagonal elements $G_{ii}(s)$ and $M_{ii}(s)$, the desired

transfer characteristic.

2. Check if the poles of the characteristic equation (6.29) lie in the negative half-plane or if

$$\begin{aligned} \left|F_{ii}(j\omega)\right| &> \sum_{j=1,j\neq i}^{m} \left|F_{ij}(j\omega)\right| \\ &\text{or} \\ \left|F_{ii}(j\omega)\right| &> \sum_{j=1,j\neq i}^{m} \left|F_{ji}(j\omega)\right| \end{aligned} \tag{6.32}$$

   is fulfilled.

3. If 1. and 2. are fulfilled the resulting multivariable control system is stable. Otherwise the controller structure has to be altered as long as 2. can be satisfied.

This controller design method is known as direct Nyquist method [263].

The measurement system can be modeled by a gain k_{M} typically representing the number of bits per ampere. The matrix $\mathbf{M}(s)$ results in

$$\mathbf{M}(s) = \begin{pmatrix} k_{\mathrm{M}} & 0 & 0 \\ 0 & k_{\mathrm{M}} & 0 \\ 0 & 0 & k_{\mathrm{M}} \end{pmatrix} \tag{6.33}$$

and together with the P-type controller matrix

$$\mathbf{K}(s) = \begin{pmatrix} k_{\mathrm{p}} & 0 & 0 \\ 0 & k_{\mathrm{p}} & 0 \\ 0 & 0 & k_{\mathrm{p}} \end{pmatrix} \tag{6.34}$$

the return difference matrix can be calculated to

$$\mathbf{F}(s) = \mathbf{I} + \mathbf{G}(s)\mathbf{K}(s)\mathbf{M}(s) =$$

$$= \begin{pmatrix} \frac{s3L_{\mathrm{N}}+2k_{\mathrm{p}}k_{\mathrm{M}}V_{\mathrm{o}}k_{\mathrm{pwm}}}{3L_{\mathrm{N}}s} & -\frac{k_{\mathrm{p}}k_{\mathrm{M}}V_{\mathrm{o}}k_{\mathrm{pwm}}}{3L_{\mathrm{N}}s} & -\frac{k_{\mathrm{p}}k_{\mathrm{M}}V_{\mathrm{o}}k_{\mathrm{pwm}}}{3L_{\mathrm{N}}s} \\ -\frac{k_{\mathrm{p}}k_{\mathrm{M}}V_{\mathrm{o}}k_{\mathrm{pwm}}}{3L_{\mathrm{N}}s} & \frac{s3L_{\mathrm{N}}+2k_{\mathrm{p}}k_{\mathrm{M}}V_{\mathrm{o}}k_{\mathrm{pwm}}}{3L_{\mathrm{N}}s} & -\frac{k_{\mathrm{p}}k_{\mathrm{M}}V_{\mathrm{o}}k_{\mathrm{pwm}}}{3L_{\mathrm{N}}s} \\ -\frac{k_{\mathrm{p}}k_{\mathrm{M}}V_{\mathrm{o}}k_{\mathrm{pwm}}}{3L_{\mathrm{N}}s} & -\frac{k_{\mathrm{p}}k_{\mathrm{M}}V_{\mathrm{o}}k_{\mathrm{pwm}}}{3L_{\mathrm{N}}s} & \frac{s3L_{\mathrm{N}}+2k_{\mathrm{p}}k_{\mathrm{M}}V_{\mathrm{o}}k_{\mathrm{pwm}}}{3L_{\mathrm{N}}s} \end{pmatrix}. \tag{6.35}$$

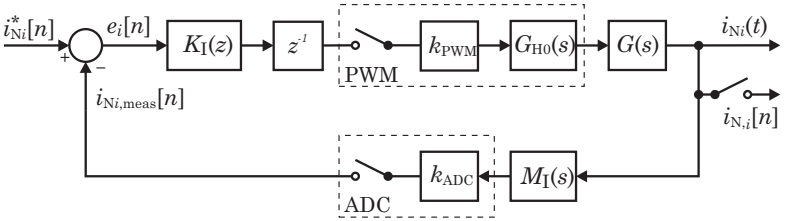


Fig. 6.18: Single-input single-output control loop of input current i_{N1} if the occurring cross-couplings are neglected.

It is now assumed, that the P-type controller with the gain k_p is designed in such a way that the single-phase control loop is stable (details about that are discussed later). The stability of the MIMO control system has then to be checked by examining (6.32). It is obvious, that independent of the gain k_p

$$\begin{gathered} \left|F_{ii}(j\omega)\right| > \sum_{j=i,j\neq i}^{m} \left|F_{ij}(j\omega)\right| \\ \left|\frac{3L_N j\omega + 2k_p k_M V_o k_{pwm}}{3L_N j\omega}\right| > \left|\frac{2k_p k_M V_o k_{pwm}}{3L_N j\omega}\right| \end{gathered} \tag{6.36}$$

is fulfilled. This means that the whole rectifier system is stable if the equivalent single-phase control loops are stable.

As a next step, the controller elements $K_{11}(s)$, $K_{22}(s)$ and $K_{33}(s)$ have to be determined according to the diagonal elements $G_{11}(s)$, $G_{22}(s)$ and $G_{33}(s)$. The three elements $G_{ii}(s)$ are luckily equal and the design of the three independent controllers can be reduced to the design of one controller. The control system will be implemented in a DSP and sampling effects and scaling constants have to be considered as shown in section 5.6.1 for the VR system. The resulting (single-phase) control loop for the elements $G_{11}(s)$ and $K_{11}(s)$ is shown in **Fig. 6.18**. The current sensor and analog measurement circuits contain a first order low-pass filter and the more comprehensive model

$$M_{ii}(s) = \frac{k_m}{1 + sT_M} \ , \tag{6.37}$$

where k_m is the number of samples per ampere and T_M is the filter constant, is used.

TABLE 6.5: System parameter for design of the controller.

Mains voltage:	$V_o = 400\,\mathrm{V}$
Mains frequency:	$f_s = 72\,\mathrm{kHz}$
Boost inductor:	$L_N = 330\,\mu\mathrm{H}$
Scaling measurement:	$k_m = 821\,\mathrm{Digits/A}$
Meas. time constant:	$T_M = 2.4\,\mu\mathrm{s}$.
Scaling PWM:	$k_{pwm} = 11104\,\mathrm{Digits/Period}\,T_s$

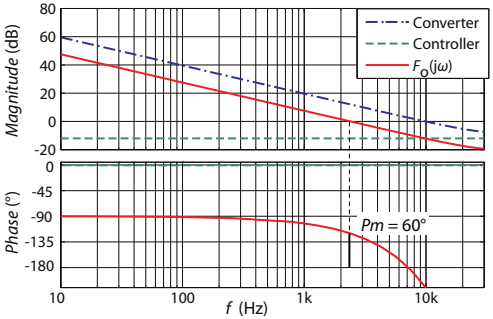


Fig. 6.19: Calculated Bode plot of the (digitalized) equivalent single-phase system. A P-type controller with a gain of $k_p = 0.25$ leads to a phase margin of 60 °.

A P-type controller is designed in the following for a system with the parameters listed in **TABLE 6.5**. **Fig. 6.19** shows the Bode plot of the equivalent single-phase system with and without the P-type current controller. The controller gain was set to $k_p = 0.25$ which yields a phase margin of 60 °. Due to the limited sampling frequency of 72 kHz and the dead time $T_t = 13.9\,\mu\mathrm{s}$ introduced by the calculation time of the controller a pronounced drop of the phase with increasing frequency can be observed. The system therefore has to be analyzed as sampled data system (as shown here) for a proper control design and cannot be treated as continuous system which is frequently done in order to simplify the controller design. A controller design neglecting the sampling effects would result in a control loop with considerably reduced phase margin which could finally cause instability of the rectifier system. At least the robustness of the controller is reduced.

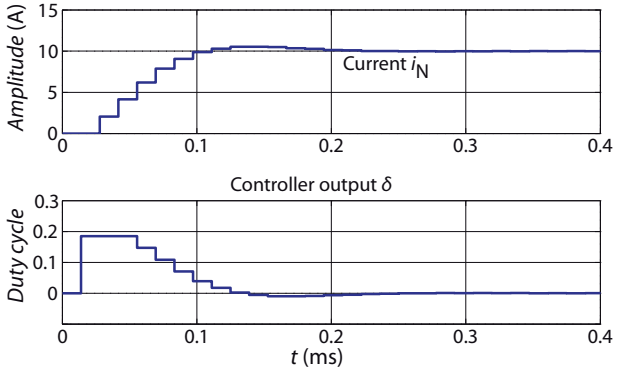


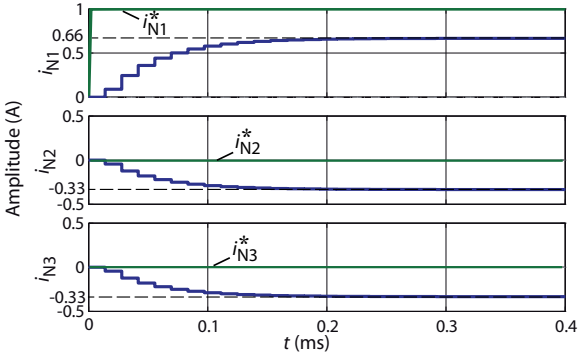
Fig. 6.20: Simulated response to a current reference step $i_N = 0 \rightarrow 10\,A$ and controller output of the equivalent single-phase system.

Fig. 6.20 shows the step response of the digitalized single-phase system for a step of $i_{N1} = 10\,A$, if cross-couplings from/to the other phases are not considered. An overshoot of only 5 % can be observed. In addition, the controller output (duty cycle δ) is plotted. A P+Lag-type controller as shown for the VR-system in section 3.2.1 could also be used for implementation of the current controller which could further increase the input current quality as the controller gain is reduced for higher frequencies. The selected P-type controller, however, shows good results and the simpler implementation supports this selection. The influence of the EMI filter and the (unknown) impedance of the mains are not considered in this controller design for the sake of a simplicity; these elements could require a reduction of the controller gain k_p.

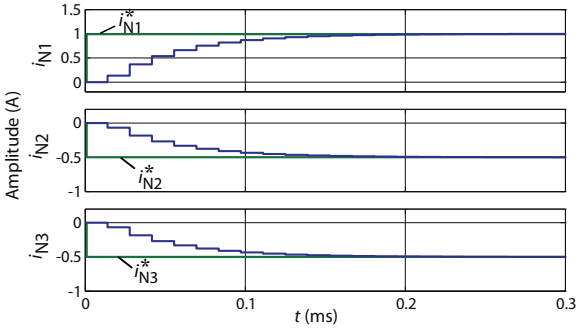
Using the designed current controller $\mathbf{K}(s)$, the MIMO control transfer function

$$\mathbf{T}(s) = \frac{k_p k_{pwm} V_o}{sL_N + k_{pwm} k_p k_m V_o} \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{pmatrix} \tag{6.38}$$

can be calculated. With this transfer function the step response of the MIMO rectifier system on a step in i_{N1} can be calculated. The



(a)



(b)

Fig. 6.21: Simulated response of the MIMO control system for a (a) forced current step of only i^*_{N1} to 1 A and (b) of i^*_{N1} to 1 A and i^*_{N2}, i^*_{N3} to -0.5 A.

responses of the three input currents are depicted in **Fig. 6.21(a)**. Such a current step is in practice not possible due to $i_{N1} + i_{N2} + i_{N3} = 0$ and accordingly a response of all three phases can be observed. The response is, however, useful to study the influence of a control action in one phase on the other two phases. According to **Fig. 6.21(a)** the input current i_{N1} reaches only an amplitude of 0.66 and the two remaining phases show a response in neg. direction. Both responses show the same time constants which can also be verified by inspecting the elements of $\mathbf{T}(s)$. A control action in one phase therefore intrinsically affects the two other phases.

Fig. 6.21(b) shows the step response of the input currents for refer-

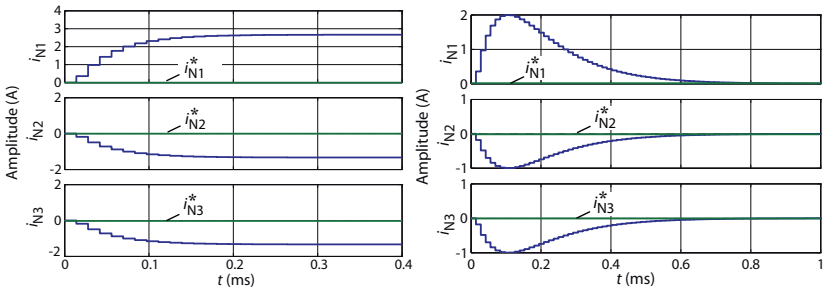


Fig. 6.22: Simulated step responses of the MIMO control system to a disturbance in the duty-cycle $w_{\mathrm{d1}} = 0.33$ using (a) a P-type controller ($k_{\mathrm{p}} = 0.25$) and (b) a PI-type controller $k_{\mathrm{p}} = 0.25$, $T_N = 0.2\,\mathrm{ms}$).

ence values not violating $i_{\mathrm{N1}} + i_{\mathrm{N2}} + i_{\mathrm{N3}} = 0$. A step of i^*_{N1} to 1 A and i^*_{N2}, i^*_{N3} to $-0.5\,\mathrm{A}$ is performed. Quite evidently, the system response shows the same time constants with the difference that no steady state control errors occur.

According to **Fig. 6.16** also the disturbance transfer function

$$\mathbf{F_d}(s) = \frac{\boldsymbol{w_d}(s)}{\boldsymbol{i_N}(s)} = \\ = \frac{k_{\mathrm{pwm}} V_{\mathrm{o}}}{sL_{\mathrm{N}} + k_{\mathrm{pwm}} k_{\mathrm{p}} k_{\mathrm{m}} V_{\mathrm{o}}} \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{pmatrix} \tag{6.39}$$

can be calculated. The simulated response of the rectifier system to a step in $w_{\mathrm{d1}} = 0.33$ is plotted in **Fig. 6.22(a)**. As well known from single-phase systems a P-type controller cannot fully compensate such distortions. According to **Fig. 6.22(a)**, this is also true for the Δ-switch rectifier system. A PI-type controller would be able to compensate this disturbances and the simulated system response to a step in w_{d1} using a PI-type controller ($k_{\mathrm{p}} = 0.25$, $T_N = 0.2\,\mathrm{ms}$) is shown in **Fig. 6.22(b)**.

A PI-type controller seems to be the ideal solution for implement-

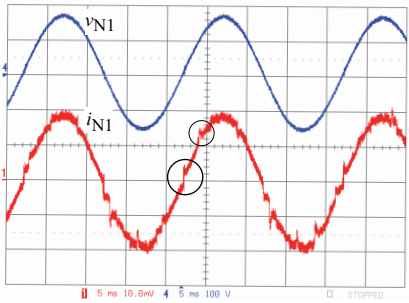


Fig. 6.23: Measured input current i_{N1} and input voltage v_{N1} taken from the implemented laboratory prototype if a PI-type current controller is used ($V_N = 115\,V$, $f_N = 50\,Hz$, $P_o = 2.5\,kW$); CH1: i_{N1}, 10 A/Div; CH4: v_{N1}, 100 V/Div; timebase: 5 ms.

ing from this point of view. The PI-type controller, however, generates distortions in the vicinity of the zero crossings. Directly after a zero-crossing the integral part of the controller shows a wrong sign and has to be reduced by an according control error (with the integrator time constant T_N). The resulting (wrong) duty cycle yields to input current distortions. **Fig. 6.23** shows a measurement result taken from the implemented laboratory prototype (cf. section 6.5), where a PI-type controller is implemented. Rather large distortions in the vicinity of the zero crossings can be observed. In addition, due to the cross-couplings of the rectifier system, the zero-crossing distortions of the two other phases are evident (every 60 °). An implementation of a zero-crossing detection, which allows to reset the integral part of the PI-type controller directly after a zero crossing occurred, would be a possibility to reduce this negative effect. The system operation, however, then depends on the correct detection of the zero-crossings which should be omitted. The designed P-type controller is therefore used for implementation of the rectifier system.

6.3.2 Voltage Controller Design

The results derived in section 3.2.2 can be used to design the output voltage controller. The Δ-switch rectifier system shows a two-level structure and in contrast to the three-level VR topology the output capacitor is not divided. An output voltage symmetry controller is therefore not

needed and only an output voltage controller has to be designed. In accordance to the VR-system, the output current i_d of the rectifier system is formed by a combination of the three phase currents (depending on the switching state) which means that (3.44) can directly by applied. The reference value of the input currents is calculated by multiplying the phase voltages with the conductance G_e^*

$$i_{\mathrm{N}i} = G_\mathrm{e}^* \; v_{\mathrm{N}i}. \tag{6.40}$$

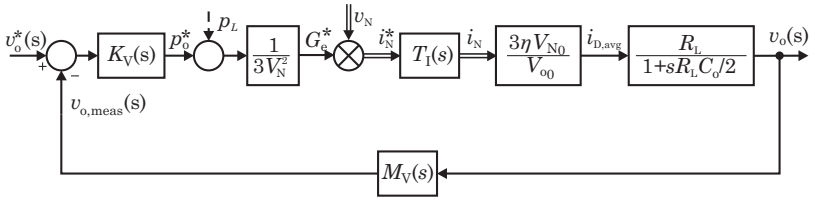
The conductance is defined by

$$G_\mathrm{e}^* = \frac{P_\mathrm{o}^*}{V_{\mathrm{N1,rms}}^2 + V_{\mathrm{N2,rms}}^2 + V_{\mathrm{N3,rms}}^2} \tag{6.41}$$

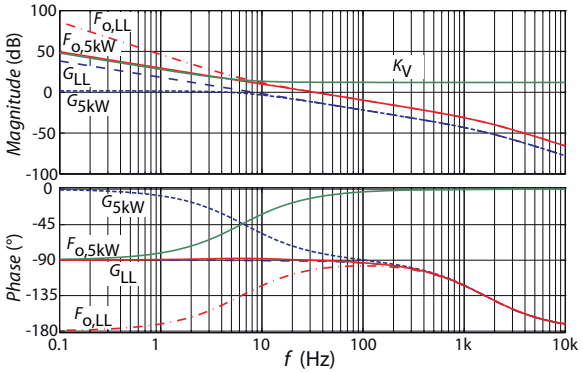
using the desired output power level P_o^* and the mains rms voltages $V_{\mathrm{N}i,\mathrm{rms}}$. The linearized small signal model given in (3.48) can therefore be used. **Fig. 6.24(a)** shows the resulting output voltage control loop. There, and also for the following discussion, a resistive load R_L is assumed. By altering this resistor the system behavior can be analyzed for different load conditions starting from no-load condition to full-load condition. The control error of the output voltage is the input of the PI-type output voltage controller $K_\mathrm{V}(s)$. The output of the voltage controller p_o^* is a control variable equivalent to the required output power of the system. A possible feedforward signal can be added for a better transient behavior of the system. The required conductance G_e^* and reference current $i_{\mathrm{N}i}^*$ are then calculated which is the input of the current controller $T_\mathrm{I}(s)$ which actually processes sinusoidal phase currents. An equivalent PT1-element

$$T_\mathrm{I}(s) = \frac{1}{1 + sT_\mathrm{i}} = \frac{1}{1 + s \cdot 0.1\,\mathrm{ms}} \tag{6.42}$$

can be used to model the behavior of the current controller. The total output capacitance of the constructed rectifier system is 1.47 mF.
The rectifier should be able to handle a single-phase loss and during the two-phase operation an oscillating power flow (with $f = 2f_\mathrm{N}$) from the input to the output of the rectifier system occurs (similar to a single-phase PFC). This finally results in an output voltage ripple and the output voltage controller must not compensate this ripple in order to prevent input current distortions. The bandwidth of the output voltage controller must therefore be sufficiently lower than $2f_\mathrm{N}$.



(a)



(b)

Fig. 6.24: (a) Linearized small signal output voltage control loop for a resistive output load R_L and (b) Bode plot of the open voltage control loop for the case of no-load condition and nominal load $P_o = 5\,\text{kW}$ for the controller parameters $k_{pv} = 4$ and $T_{Nv} = 0.031\,\text{s}$.

As the no-load condition shows the smallest phase margin of the different load cases the PI-type controller is designed according to the no-load condition. The PI-type voltage controller

$$K_v(s) = k_{pv}\frac{1 + sT_{Nv}}{sT_{Nv}} \tag{6.43}$$

with the parameters $k_{pv} = 4$ and $T_{Nv} = 0.031\,\text{s}$ yields to a crossover frequency of about 35 Hz and a phase margin of 78 °. **Fig. 6.24(b)** shows a Bode plot of the linearized rectifier model, the PI-type voltage controller $K_v(j\omega)$ and the open control loop $F_o(j\omega)$ for no-load condition (LL) and nominal load $P_o = 5\,\text{kW}$.

The simulated step response of the control loop for an output voltage step from 350 V to 400 V is shown in **Fig. 6.25** where only a small

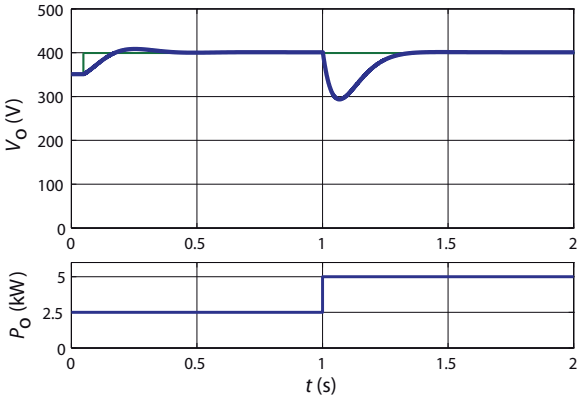


Fig. 6.25: Simulated step response and response of a load step from $P_o = 2.5\,\text{kW}$ to $P_o = 5\,\text{kW}$ of the voltage control loop depicted in **Fig. 6.24(a)**.

voltage overshoot of about 20 V can be read. In addition the system response on a load step from $P_o = 2.5\,\text{kW}$ to $P_o = 5\,\text{kW}$ is shown. A voltage drop of about 100 V occurs which might be too large in a practical application. The voltage control loop can only react on a deviation of the output voltage and due to the limited gain crossover frequency this large voltage drop occurs. This behavior can be significantly improved if some information of the load condition (e.g. output power of the following DC/DC converter stage or information of the load current) is available which can be used as feedforward signal.
The undershoot/overshoot of the output voltage caused by connection/disconnection of load can also be reduced by implementation of a nonlinear controller part (cf. section 5.9).

6.3.3 Two-Phase Operation

The control system must be able to handle a single phase loss (e.g. caused by tripping of the fuse at one phase input) as shown in **Fig. 6.26(a)** without any changes in the controller structure. **Fig. 6.26(b)** illustrates the voltage phasor diagram of a three-phase power system. All three phase-to-neutral voltages (and also the line-to-line voltages) show the same amplitude and are phase shifted by 120 °. The voltage phasors of a system with disconnected mains voltage at L_{N1} is plotted in **Fig. 6.26(c)**. In this case the input currents of the

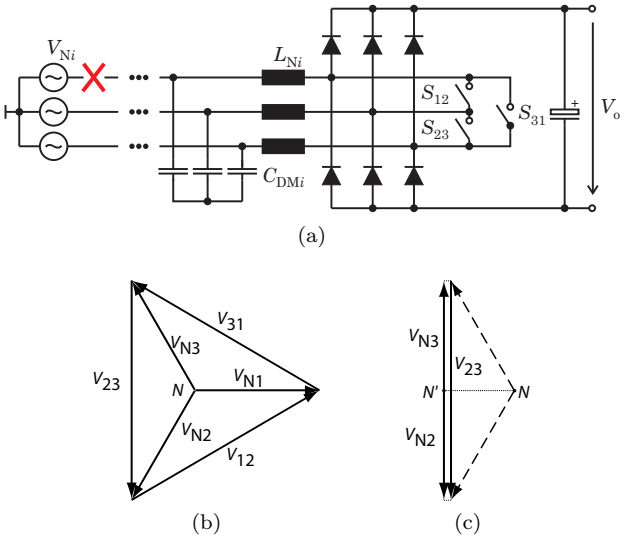


Fig. 6.26: (a) Simplified schematic of the Δ-switch rectifier system during a single phase loss if the first EMI filter stage is considered; (b) Voltage phasor diagram of the three-phase mains and (c) voltage phasors for two-phase operation.

two remaining phases are directly controlled by the switch S_{23}. The virtual neutral point N, which is built by three star-connected resistors as the neutral wire is typically not connected to the rectifier system, moves then to the line-to-line voltage V_{23} (N'). The two remaining phase voltages are in phase/180 ° out of phase with the corresponding line-to-line voltage. A sudden phase-shift of 30 ° will hence appear in the two remaining phases. According to **Fig. 6.26(c)**, the proposed phase-oriented control of the input currents followed by a star-Δ transformation can still be applied.

Considering the maximal input current amplitude the output power has to be reduced in order to prevent the semiconductors from overcurrent. In three-phase operation mode the output power can be calculated as

$$P_o = 3\eta V_N I_N \ . \tag{6.44}$$

During two-phase operation, power is only delivered to the output by a single line-to-line voltage source

$$P_{o,PL} = \eta V_{ij} I_N \tag{6.45}$$

and hence the maximal available output power

$$P_{\mathrm{o,PL}} = \frac{P_{\mathrm{o}}}{\sqrt{3}} \tag{6.46}$$

can be calculated if it is assumed that the amplitude of the input current is as for (6.44).
As a next step the influence of a single phase loss on the output voltage control loop is analyzed. According to **Fig. 6.24(a)** the output of the voltage controller is equivalent to the desired output power of the rectifier system. The conductance G_{e}^{*} is calculated by dividing the required output power P_{o}^{*} by the sum of the squared phase voltage. In case of a phase loss this yields to

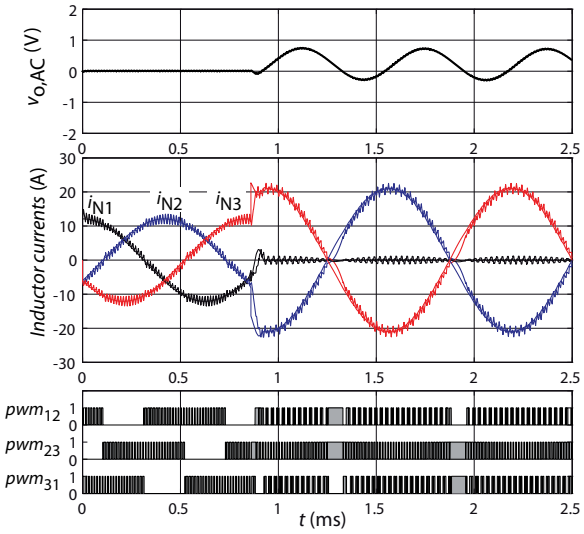
$$G_{\mathrm{e}}^{*} = \frac{P_{\mathrm{o}}}{V_{\mathrm{N1}}^2 + V_{\mathrm{N2}}^2 + V_{\mathrm{N3}}^2} = \frac{P_{\mathrm{o}}}{0 + V_{\mathrm{N2}}^2 + V_{\mathrm{N3}}^2} = \frac{P_{\mathrm{o}}}{2\left(\frac{V_{ij}}{2}\right)^2} \tag{6.47}$$

and the phase current is calculated by multiplying the conductance G_{e}^{*} with the phase voltage

$$i_{\mathrm{N}i}(t) = v_{\mathrm{N}i}(t) G_{\mathrm{e}}^{*} = \frac{v_{ij}(t)}{2} G_{\mathrm{e}}^{*} \tag{6.48}$$

which is in agreement with (6.45). Therefore, no changes in the structure of the output voltage control are required. Care should be taken if a limitation of the conductance G_{e}^{*} shall be implemented due to the larger conductance expressed by (6.47).
Fig. 6.27 shows the simulated system response of the boost inductor currents on a single phase loss at $t = 0.85\,\mathrm{ms}$. After some minor ringing the system operates in two-phase mode without any changes in the controller structure or parameters. After the phase loss occurs, an output voltage ripple is apparent which is caused by the non-constant power flow from the mains to the load. Due to the large output capacitor $C_{\mathrm{o}} = 1.47\,\mathrm{mF}$ only a very small voltage ripple occurs.

In **Fig. 6.26(a)**, the implementation of an EMI filter with DM capacitors ($C_{\mathrm{DM}i}$) after the boost inductors is shown. Together with the boost inductors these filter capacitors form a resonant circuit which is excited by the switching actions of the corresponding switches S_{ij}. If phase L_1 is disconnected from the mains the input currents of the two remaining phases (L_2 and L_3) are controlled by the switching actions

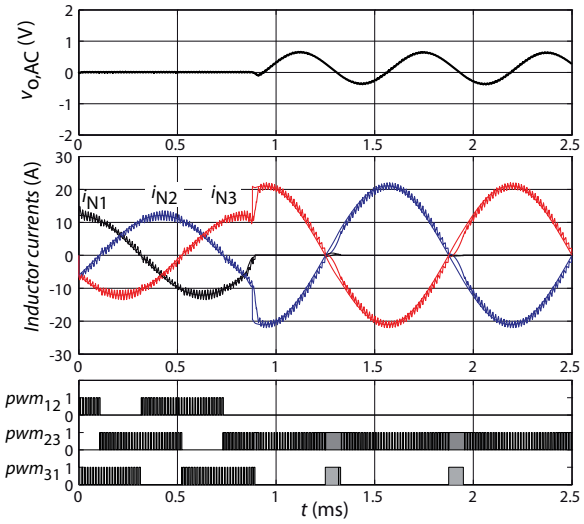


(a)

Fig. 6.27: (a) Simulated system response for a single phase loss at $t = 0.85\,\text{ms}$ ($V_\text{N} = 115\,\text{V}$, $V_\text{o} = 400\,\text{V}$, $f_\text{N} = 800\,\text{Hz}$, $L_\text{N} = 330\,\mu\text{H}$ and $P_\text{o} = 2.5\,\text{kW}$).

of switch S_{23}. According to **Fig. 6.27** more or less random switching actions of the two remaining switches occur if the controller structure is not changed. If both switches are turned on (S_{12} and S_{31}) the switch S_{23} is shortened by these two switches and the (random) switching actions also influence the input currents on the two remaining phases. As a result a current oscillation in the boost inductor of the disconnected phase occurs which is much more pronounced in a practical implementation.

A simple RC-snubber circuit could be connected in parallel to the DM capacitors in order to damp these unwanted oscillations but the power dissipation in the snubber resistor would be far to high for a mains frequency of $f_\text{N} = 800\,\text{Hz}$. A much better solution is to clamp one of the two switches to permanent off-state during two-phase operation (e.g. S_{12}) which is finally implemented in the constructed rectifier system. Accordingly, a possible phase loss has to be detected which can for instance be done by the rms measurement of the input voltages (which is typically needed for output voltage control).



(a)

Fig. 6.28: (a) Simulated system response on a single phase loss at $t = 0.85\,\text{ms}$ if switch S_{12} is clamped permanently to off-state after a loss of phase L_1 is detected ($V_\text{N} = 115\,\text{V}$, $V_\text{o} = 400\,\text{V}$, $f_\text{N} = 800\,\text{Hz}$, $L_\text{N} = 330\,\mu\text{H}$ and $P_\text{o} = 2.5\,\text{kW}$).

The simulation results of the rectifier system, where after detection of a loss of phase L_1 the switch S_{12} is clamped to permanent off-state, is given in **Fig. 6.28**. No oscillations in the boost inductor of the disconnected phase are now present which verifies the effectiveness of this approach. The input currents are only controlled by the switching actions of switch S_{23}. Only minor changes in terms of enabling/disabling of PWM signals have to be done in order to achieve an optimal system behavior. These changes in the controller structure are in principle not required and the operation in two-phase mode is therefore only improved by this clamping action.

6.3.4 Reactive Power Capability

Up to this point, it was assumed that the mains currents are in phase with the mains voltages which means that ideally a power factor of $\lambda = 1$ is achieved. The inductor currents are used for current control and hence only the inductor currents are in phase with the mains voltages. The

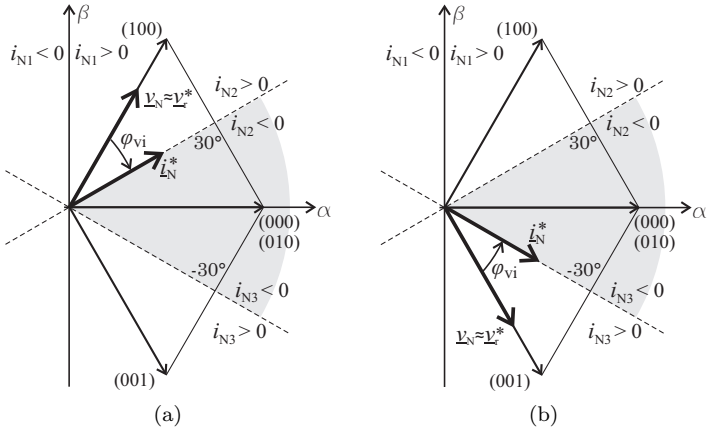


Fig. 6.29: Space vector diagrams used to explore the limits of the phase angle between mains voltage and rectifier input current. (a) Space vectors for maximal lagging input current at the sector limit $\varphi_N = 30\,°$ and (b) space vectors for maximal leading input current at the sector limit $\varphi_N = -30\,°$ for the sector $\varphi_N \in [-30°, 30°]$.

leading currents drawn by the EMI filter capacitors, however, decrease the power factor at light load or no-load conditions. These capacitive currents are often negligibly small for systems with a mains frequency of 50 Hz/60 Hz but have to be taken into account for the mains frequency range of 360 Hz–800 Hz. As for the VR-system the question again arises whether the system can operate with a limited phase difference between input voltage and inductor current or not. The power factor of the rectifier system could be improved if operation with a lagging inductor current is possible. A phase difference between inductor current and mains voltage implies that in addition to the active power also reactive power is generated. This can for instance be used to interface induction generators as well as permanent-magnet synchronous generators for wind energy applications as discussed in [258]. The reactive power capability of the rectifier system is now analyzed in detail.

For the following discussion the sector $\varphi_N \in [-30°, 30°]$ is chosen and **Fig. 6.29(a)** shows the available voltage space vectors for this sector. The sector limits, which are identical with the points where one input phase changes its direction, are plotted with dashed lines. The input current i_{N1} is therefore always positive in the right half plane of the

space vector diagram and negative in the left half plane. The rectifier circuit generates the voltage space vector $\underline{v}_\mathrm{r}^*$ by pulse-width modulation of the corresponding switches. This voltage can be generated in such a way that the input current space vector $\underline{i}_\mathrm{N}$ is leading or lagging the mains voltage space vector. **Fig. 6.29(a)** is used to discuss the case of lagging input currents. The capacitive currents drawn by the EMI filter capacitors are neglected in a first step. Similar to the discussion of the VR system also the voltage drop of the boost inductor is neglected as it is normally small in comparison to $\underline{v}_\mathrm{r}^*$. The rectifier system moves on to the next sector as soon as the current space vector reaches the sector limit. The discrete, non-zero voltage space vectors (001), (000), (010) and (100) can be generated in the selected sector $\varphi_\mathrm{N} \in [-30°, 30°]$. A maximally displaced voltage space vector can be generated by switching state (001) for an input current space vector at the sector limit $\varphi_\mathrm{i} = 30\,°$ and therefore a maximal phase difference of $\varphi_\mathrm{vi} = \varphi_\mathrm{v} - \varphi_\mathrm{i} = 30\,°$ can be generated by the rectifier system for the condition of a negligible voltage drop across the boost inductor.

Similar considerations can be applied for the case of leading input phase current (cf. **Fig. 6.29(b)**). In that case an input current space vector at the sector limit $\varphi_\mathrm{i} = -30\,°$ has to be assumed and the voltage space vector with the largest phase difference is resulting for switching state (001). As a result a maximal phase difference of $\varphi_\mathrm{vi} = -30\,°$ can be generated by the rectifier system in case of leading current. In both cases, leading and lagging input current, the feasible phase shift is independent of the voltage transfer ratio and the modulation index M. The phase angle between the voltage and current space vector is equal to the phase angle between the mains voltage and input currents for balanced three-phase systems and the Δ-switch rectifier system is therefore able to generate input currents with a phase of

$$-30\,° \leq \varphi_\mathrm{vi} = \varphi_\mathrm{v} - \varphi_\mathrm{i} \leq 30\,° \;. \tag{6.49}$$

This wide phase angle range is possible due to the fact that line-to-line voltages are used to form the input currents. This can also be confirmed by the phase angle range of $\varphi_\mathrm{vi} \in [-30°, 30°]$ which corresponds with the phase shift between the line-to-neutral and line-to-line voltages. Lets, for instance, take the negative zero crossing of input current i_L1 under consideration. The zero crossing of phase voltage v_N1 already occurred and v_N1 shows a negative amplitude at positive input current

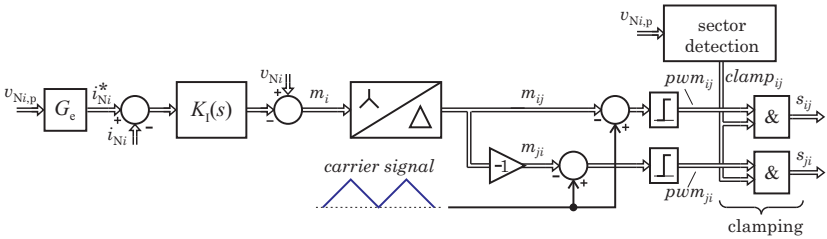


Fig. 6.30: Basic schematic of the current controller structure.

i_{N1} for lagging input currents. The line-to-line voltage v_{13}, however, is still positive and can be used to impress positive input currents without any additional input current distortion which clearly demonstrates the phase angle capability. Similar considerations can be used for the positive zero crossings and leading input currents.
Note that, similar to the VR-system in general theoretical phase angles of $-30\,° \leq \varphi_{vi} \leq 90\,°$ can be generated if the voltage drop across the boost inductors are not neglected or limited. In practical systems, however, this voltage drop is small and (6.49) applies. Equation (6.49) describes the phase limits of the rectifier system which can be achieved without increased input current distortions. Considerably increased input current distortions would occur if larger phase differences would be generated.

The Δ-switch rectifier system is therefore able to generate input currents with a phase angle given in (6.49) but up to now no information on implementation of such a phase shifted operation was given in literature. A space vector control could be used to select the optimal space vectors (and switching sequences) also in the case of a phase shift between input currents and phase voltages. In the following it will be analyzed if an implementation using the proposed pulse-width modulators and phase related current controllers is also able to generate such phase differences with optimal switching sequence.

The simplified structure of the current controller is again depicted in **Fig. 6.30** (see also **Fig. 6.10**). In order to achieve phase shifted input currents, the reference currents i^*_{Ni} must be generated by multiplying the phase shifted phase voltages $v_{Ni,p}$ with the conductance G^*_e

generated by the output voltage controller. The generation of the phase shifted voltages is discussed below. According to **Fig. 6.30** the input voltage $v_{\mathrm{N}i}$ is added to the current controller output in terms of a voltage feedforward. This feedforward signal is used to get rid of the input voltage terms in the transfer function of the rectifier system (cf. (6.27)) and hence the measured, mains voltages (without phase shift) must be used for this signal. Another explanation of using the non-phase shifted mains voltages for feedforward can be found if the duty-cycle generation is examined. If the phase shifted voltages would be used as feedforward signal the generated duty-cycle would be different to the actually existing phase voltages. This would require a large current controller gain in order to prevent massive zero crossing distortions and would finally result in a non-stable current control loop. The phase shifted input voltages $v_{\mathrm{N}i,\mathrm{p}}$ on contrary must be used for sector detection and clamping. Otherwise the system would switch to the next sector too early or too late which would finally lead to considerably increased input current distortions.

A digital computer simulation is used to clarify if still optimal switching sequences are generated by the proposed pulse-width modulated current controller in case of a phase difference between input current and input voltage. **Fig. 6.31** shows a simulated behavior of a system operating with a phase shift of 30 °. The input currents are sinusoidal and no additional zero-crossing distortions occur. In practice, however, due to other parasitic effects (distortions caused by limited current slew-rate after zero-crossing (cusp distortion), turn-off delay of the MOSFETs, etc.,) slightly increased zero-crossing distortions will appear. The corresponding switches are operated according to the phase shifted input voltages $v_{\mathrm{N}i,\mathrm{d}}$ which are in phase with the inductor currents but are not shown in **Fig. 6.31**. The clamping signals are derived from this phase voltages as well.

Fig. 6.32 shows the PWM signals in the vicinity of $\varphi_{\mathrm{N}} = 30\,°$. The current space vector is lagging the input voltage space vectors and according to **Fig. 6.29(a)** the rectifier states (000), (100) and (101) shall be used for approximation of $\underline{v}_{\mathrm{r}}^{*}$. The switching sequence (000)-(100)-(101)-(100)-(000) can be read which confirms that the optimal switching sequence is selected by the proposed current controller even if the system operates in phase-shift mode. **Fig. 6.33** shows the simulation results of

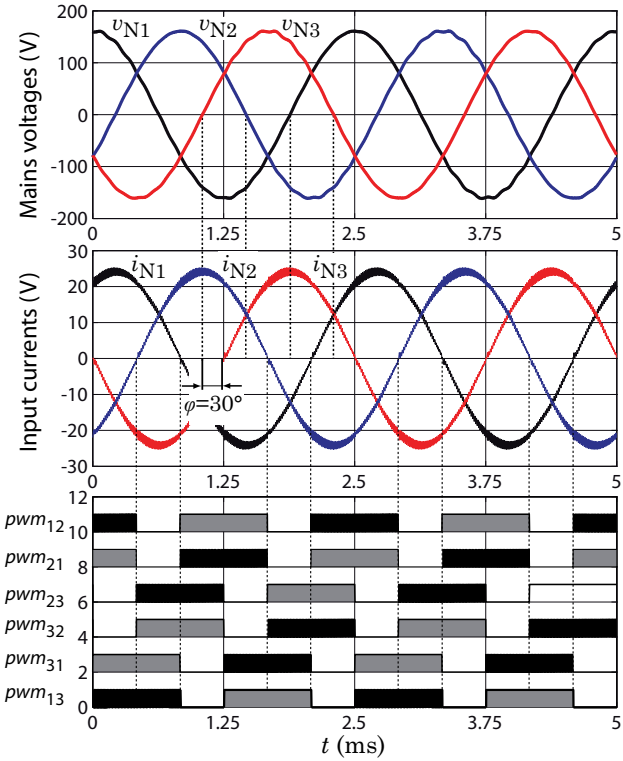


Fig. 6.31: Simulation result of a Δ-switch rectifier system operating with 30 ° lagging phase currents using the proposed current controller ($V_{Ni} = 115\,\mathrm{V}$, $f_N = 400\,\mathrm{Hz}$, $V_o = 400\,\mathrm{V}$, $P_o = 5\,\mathrm{kW}$).

a system operating with a phase-shift of $\varphi_{vi} = -15\,°$.

Reactive Power Compensation

In order to fulfill the input current harmonics limits and EMI requirements filter capacitors are needed at the input of the rectifier system and these filter capacitors considerably degrade the rectifiers power factor λ. The phase-shift capability of the Δ-switch rectifier system can be used advantageously to improve the decreasing power factor at partial load. Note that the rectifier system is only able to shift the phase of the input currents and cannot generate any reactive power during no

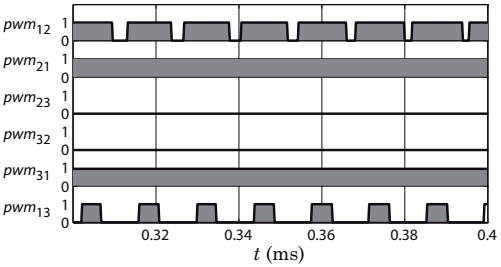


Fig. 6.32: Switching sequence of the simulation results plotted in **Fig. 6.31** for $t = 0.3 \ldots 0.4\,\mathrm{ms}$. The switching sequence (000)-(100)-(101)-(100)-(000) can be read which is the optimized sequence concerning to conduction losses.

load condition. The possible amount of reactive power compensation is therefore dependent on the load connected to the rectifier system.

Fig. 6.34(a) shows the simplified equivalent single-phase circuit of the rectifier. The inductor current i_L is forced by the current controller to follow the sinusoidal references and the rectifier system is therefore modeled by a controlled current source. In addition the (lumped) filter capacitor C_{DM} is shown which draws the current $i_{\mathrm{C,DM}}$ and the total input current i_{N} is the sum of i_L and $i_{\mathrm{C,DM}}$. In **Fig. 6.34(b)** the corresponding phasor diagram is plotted where the rectifier system is assumed to operate in phase shift mode with a lagging current (φ_{vi}). If the amount of capacitive current $i_{\mathrm{C,DM}}$ cannot fully be compensated by the implemented phase shift between the inductor current and phase voltage, a phase shift φ between rectifier input current and mains voltage remains. The projection of the input current on the mains voltage is responsible for the active power transferred to the load and is given by

$$i_{\mathrm{p}} = \frac{P_{\mathrm{o}}}{3V_{\mathrm{N}}} \tag{6.50}$$

if system losses are neglected. According to **Fig. 6.34(b)** the remaining power factor of the input current can be calculated using the capacitor current $|i_{\mathrm{C,DM}}| = V_{\mathrm{N}}\omega C_{\mathrm{DM}}$ and

$$|i_{\mathrm{C,DM}}| = i_{\mathrm{p}}\big(\tan(\varphi_{\mathrm{vi}}) + \tan(\varphi)\big) \tag{6.51}$$

which results by use of (6.50) in

$$\lambda = \cos(\varphi) = \cos\left(\arctan\left(\frac{3V_{\mathrm{N}}^2\omega C_{\mathrm{DM}}}{P_{\mathrm{o}}} - \tan(\varphi_{\mathrm{vi}})\right)\right) . \tag{6.52}$$

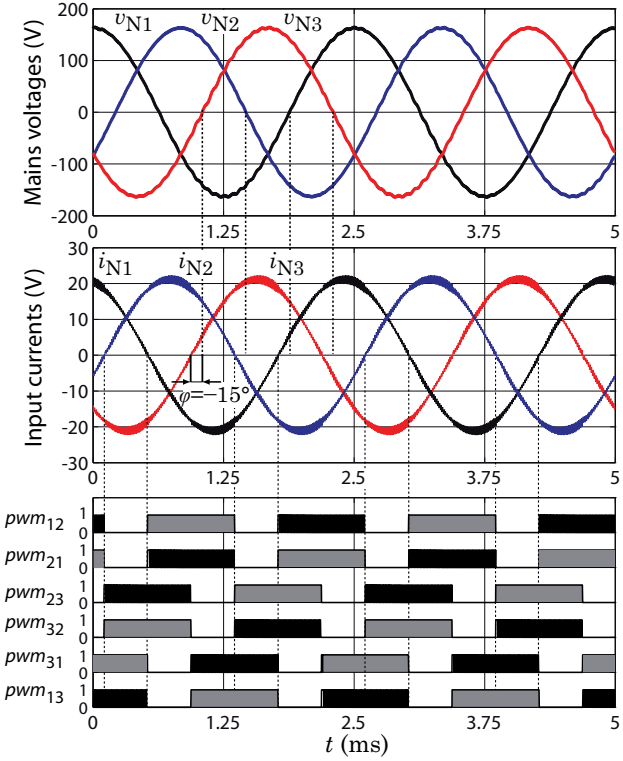


Fig. 6.33: Simulation result of a Δ-switch rectifier system operating with a current phase angle of $-15\,^\circ$ using the proposed current controller ($V_{Ni} = 115\,\mathrm{V}$, $f_N = 400\,\mathrm{Hz}$, $V_o = 400\,\mathrm{V}$, $P_o = 5\,\mathrm{kW}$).

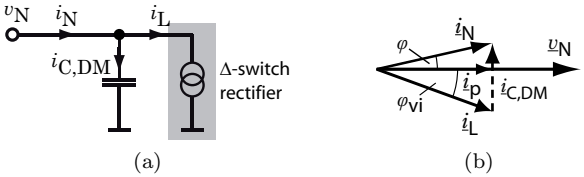


Fig. 6.34: (a) Simplified equivalent single-phase circuit including the input capacitors C_{DM} and (b) corresponding phasor diagram considering the phase shift capability of the rectifier system..

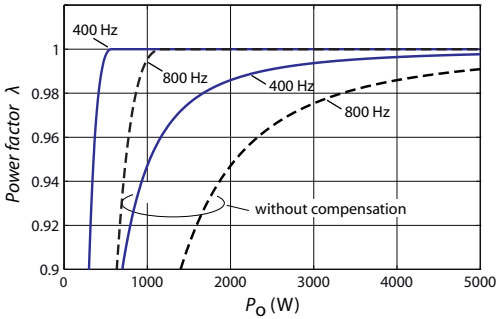


Fig. 6.35: Calculated maximal achievable power factor with and without compensation of currents drawn by filter capacitors at the input of the rectifier system ($V_N = 115\,V$, $C_{DM} = 3.4\,\mu F$, $\varphi_{vi} = 30\,°$).

Using (6.52) the maximal achievable power factor for a given amount of filter capacitance can be calculated. The results for star connected filter capacitors $C_{DM} = 3.4\,\mu F$ are depicted in **Fig. 6.35**. A strong decrease in the power factor especially for $f_N = 800\,Hz$ can be observed without compensation if the load is reduced. In addition the power factor of a system using compensation by altering the phase shift between inductor current and mains voltage in the full range ($\varphi_{vi} \in [0\,° \ldots 30\,°]$) is shown. The system is able to achieve a unity power factor down to an output power of approximately 500 W for $f_N = 400\,Hz$ and for $f_N = 800\,Hz$ down to 1 kW. For smaller output power levels the phase shift cannot be compensated anymore and the power factor drops very quickly.
The corresponding output power limits $P_{o,lim}$ for full compensation are plotted in **Fig. 6.36** as a function of the total amount of filter capacitors C_{DM} and the mains frequency f_N. It is obvious that especially for $f_N = 800\,Hz$ the total amount of filter capacitance should be held as small as possible in order to achieve a high power factor.

To conclude on the reactive power compensation capability of the Δ-switch rectifier system it has to be summarized that in theory the system is able to increase the power factor at light load by introducing a phase shift between inductor current and mains voltage. This phase shift is limited to $\varphi_{vi} \in [-30° \ldots 30°]$ which finally defines a minimum output power $P_{o,lim}$ where a unity power factor can be achieved without

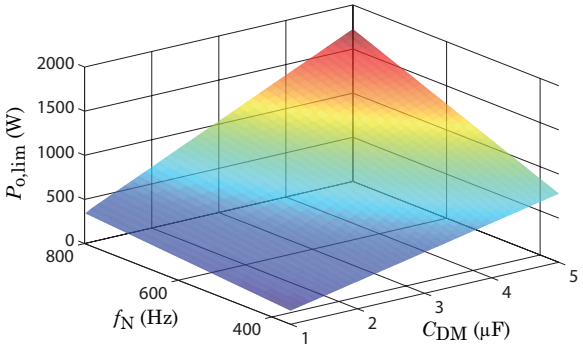


Fig. 6.36: Calculated minimum output power limit for enabling full filter capacitor reactive power compensation as a function of total amount of filter capacitors C_{DM} and mains frequency f_N.

any additional input current distortions. As it is shown in section 5.1.2 increased input current distortion will occur due to other effects such as the turn-off delay of the MOSFETs which finally limits the performance of this compensation in practical applications.

6.4 System Design

In this section some issues of the design and the practical implementation of the Δ-switch rectifier will be discussed.

6.4.1 Startup

At startup of the rectifier system the output capacitors have to be charged to the peak value of the line-to-line phase voltage. The output capacitors are connected to the mains by the three-phase diode bridge and the (small) boost inductors. If the system would directly be connected to the mains a huge inrush current would occur. In order to limit this inrush current a startup circuit and sequence is required.
Fig. 6.37(a) shows the proposed startup circuit for the Δ-switch rectifier system. The pre-charge circuit consisting of diode D_{pre}, resistor R_{pre} and thyristor Thy_{pre} is employed on the DC side of the rectifier. During startup, the thyristor is off and the pre-charge resistor limits

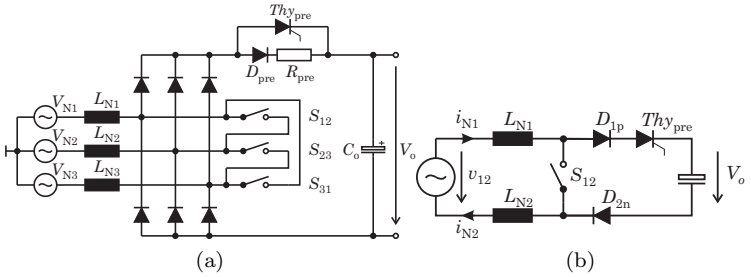


Fig. 6.37: (a) Proposed pre-charge circuit for startup of the rectifier, consisting of pre-charge diode D_{pre}, precharge resistor R_{pre} and thyristor Thy_{pre}; (b) Equivalent circuit for switch S_{12} at $\varphi_{\mathrm{N}} = -15°$.

the inrush current. The bidirectional switches are permanently off during startup and also the current controller is disabled during this time. The thyristor and pulse-width modulator are turned on as soon as the capacitors are completely charged to the peak value of the line-to-line voltage and the controller ramps up the output voltage to the desired value. This functionality has to be implemented in the digital controller – for the system at hand in the DSP.

Fig. 6.37(b) shows the commutation path for the switch S_{12} for $\varphi_{\mathrm{N}} = -15°$. The thyristor is unfortunately located within the commutation path of the rectifier ($S_{12}, D_{1\mathrm{p}}, Thy_{\mathrm{pre}}$ and D_{n2}). In order to minimize the thyristors influence on the parasitic inductance of the commutation path, three thyristors (one thyristor closely placed to each switch) can be used in parallel. This also reduces the on-resistance and therefore the conduction losses of the additional element advantageously.

6.4.2 Component Stresses

In order to evaluate the performance of the rectifier and to design the system the on-state losses of the semiconductors are required. The current rms and average values are therefore calculated and simple analytical approximations are derived. For the following calculations it is assumed that the rectifier has

- a purely sinusoidal phase current shape;
- a phase difference between mains voltage and input current is in the range of φ_{vi} (cf. (6.49));

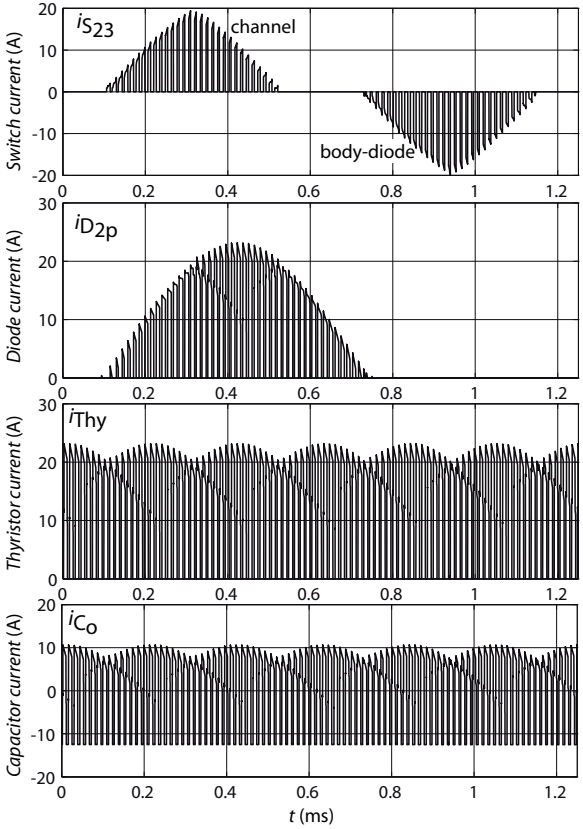


Fig. 6.38: Simulated current waveforms of the switch current $i_{S_{23}}$ (channel and body diode), rectifier diode current $i_{D_{2p}}$, thyristor current i_{Thy} and output capacitor current i_o for $V_N = 115\,V$, $V_o = 400\,V$, $f_N = 800\,Hz$, $\varphi_{vi} = 0$ and $P_o = 5\,kW$).

- no low-frequency voltage drop across the boost inductors for the sinusoidal shaping of the input currents;
- a constant switching frequency;
- a linear behavior of the boost inductors (inductance is not dependent on the current level).

1) Bidirectional switches S_{ij}

Each bidirectional switch of **Fig. 6.2(a)** consists of two MOSFETs

and hence two elements have to be considered: the MOSFET which is modulated by the current controller and the body diode of the second MOSFET. The current average values of the semiconductors are therefore not zero, although the entire average current of the bidirectional switch is zero (averaging over a full line-frequency period). The simulated current waveforms of the MOSFET and the body diode are plotted in **Fig. 6.38**. Positive currents are drawn by the channel of the MOSFET, whereas negative currents flow through the bode-diode of the switch. The envelopes of the modulated currents are sections of sinusoidal current waveforms. In the following the average and rms current values of the MOSFETs are derived using the switch S_{23}. The results are, however, valid for all six switches.

The switch S_{23} is modulated between $30\,^\circ < \varphi_\mathrm{N} < 150\,^\circ$, and according to **TABLE 6.4** the line-to-line voltage v_{23} has to be used to determine the corresponding duty cycle

$$\delta_{23}(\varphi_\mathrm{N}) = \begin{cases} 1 - M\sin(\varphi_\mathrm{N} - \frac{\pi}{6} + \varphi_\mathrm{vi}) & \text{for } 30\,^\circ < \varphi_\mathrm{N} < 150\,^\circ \\ 0 & \text{else} \end{cases} . \quad (6.53)$$

The average current of the MOSFET and the body diode can be calculated by

$$\begin{aligned} I_\mathrm{T,avg} &= \frac{1}{2\pi}\int_0^{2\pi} i_{\mathrm{S}_{23}}(\varphi)\delta_{23}(\varphi)d\varphi = \\ &= \frac{2}{2\pi}\int_0^{\frac{\pi}{3}} \hat{I}_\mathrm{N}\sin(\varphi)\left(1 - M\sin\left(\varphi - \frac{\pi}{6} + \varphi_\mathrm{vi}\right)\right)d\varphi = \\ &= \hat{I}_\mathrm{N}\left(\frac{1}{2\pi} - \frac{M}{4\sqrt{3}}\cos(\varphi_\mathrm{vi})\right) \end{aligned} \quad (6.54)$$

and the rms-current of the MOSFET and the body diode is given by

$$\begin{aligned} I_\mathrm{T,rms} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2_{\mathrm{S}_{23}}(\varphi)\delta_{23}(\varphi)d\varphi} = \\ &= \sqrt{\frac{2}{2\pi}\int_0^{\frac{\pi}{3}} \left(\hat{I}_\mathrm{N}\sin(\varphi)\right)^2\left(1 - M\sin\left(\varphi - \frac{\pi}{6} + \varphi_\mathrm{vi}\right)\right)d\varphi} = \\ &= \hat{I}_\mathrm{N}\sqrt{\left(\frac{1}{6} - \frac{\sqrt{3}}{8\pi}\right) - \frac{M}{2\sqrt{3}\pi}\cos(\varphi_\mathrm{vi})} . \end{aligned} \quad (6.55)$$

Please note, that the calculated current stress is only valid for the proposed modulation strategy discussed in section 6.1.1. Other modulation strategies (such at the ones given in [258]) may lead to different average and rms currents of the switches.

2) Rectifier Diodes $D_{\mathrm{p}i}$, $D_{\mathrm{n}i}$

The simulated current waveform of the rectifier diode $D_{2\mathrm{p}}$ is illustrated in **Fig. 6.38**. In contrast to the switch currents, where the switching actions of the switch directly influence the current, the current flowing through the rectifier diodes is determined by the switching actions of two switches.

$$i_{\mathrm{D}_{2\mathrm{p}}} = \begin{cases} f\left(S_{23}\right) & \text{for } 30\,^\circ < \varphi_{\mathrm{N}} < 90\,^\circ \\ f\left(S_{12}, S_{23}\right) & \text{for } 90\,^\circ < \varphi_{\mathrm{N}} < 150\,^\circ \\ f\left(S_{12}\right) & \text{for } 150\,^\circ < \varphi_{\mathrm{N}} < 210\,^\circ \\ 0 & \text{else} \end{cases} . \tag{6.56}$$

After a short calculation similar to (6.54) and (6.55) the average and rms currents of the rectifier diodes follow as

$$\begin{aligned} I_{\mathrm{D,avg}} &= \hat{I}_{\mathrm{N}} \frac{M}{2\sqrt{3}} \cos(\varphi_{\mathrm{vi}}) \ , \\ I_{\mathrm{D,rms}} &= \hat{I}_{\mathrm{N}} \sqrt{\frac{M\left(5+2\sqrt{3}\right)}{12\pi} \cos(\varphi_{\mathrm{vi}})} \ . \end{aligned} \tag{6.57}$$

3) Startup Thyristor Thy_i

The thyristor current is a combination of the diode currents. The average value of the thyristor is equal to the load current and is given by

$$I_{\mathrm{Thy,avg}} = 3 \cdot I_{\mathrm{D,avg}} = \widehat{I}_{\mathrm{N}} \frac{M\sqrt{3}}{2} \cos(\varphi_{\mathrm{vi}}) \tag{6.58}$$

and the rms-current results in

$$I_{\mathrm{Thy,rms}} = \widehat{I}_{\mathrm{N}} \sqrt{\frac{5M}{2\pi} \cos(\varphi_{\mathrm{vi}})} \ . \tag{6.59}$$

4) Output Capacitor C_{o}

The rms current stress of the output capacitor for a constant load current I_{o} can be calculated by considering the characteristic thyristor current values

$$I_{\mathrm{C_o,rms}} = \sqrt{I_{\mathrm{Thy,rms}}^2 - I_{\mathrm{Thy,avg}}^2} \ , \tag{6.60}$$

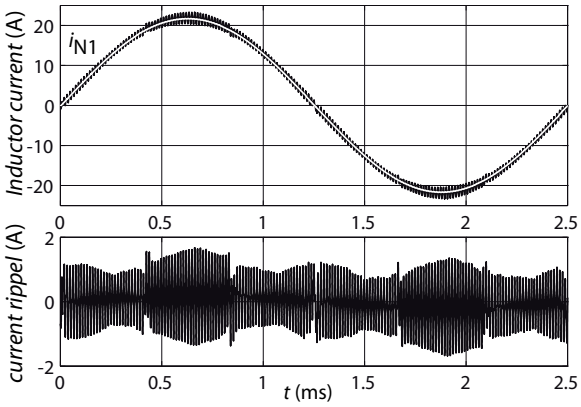


Fig. 6.39: Simulated current waveform i_{N1} (in boost inductor L_{N1}) and corresponding current ripple for $P_{\mathrm{o}} = 5\,\mathrm{kW}$ ($V_{\mathrm{N}} = 115\,\mathrm{V}$, $V_{\mathrm{o}} = 400\,\mathrm{V}$, $f_{\mathrm{N}} = 400\,\mathrm{Hz}$, $L_{\mathrm{N}} = 330\,\mu\mathrm{H}$ and $f_{\mathrm{s}} = 72\,\mathrm{kHz}$).

which leads to

$$I_{\mathrm{C_o,rms}} = \widehat{I}_{\mathrm{N}} \sqrt{\frac{5M}{2\pi}\cos(\varphi_{\mathrm{vi}}) - \frac{3\left(M\cos(\varphi_{\mathrm{vi}})\right)^2}{4}}\,. \tag{6.61}$$

5) Boost Inductor $L_{\mathrm{N}i}$

In order to be able to design the boost inductors the maximum amplitude of the input current ripple is needed. Ohmic fundamental mains behavior ($\varphi_{\mathrm{vi}} = 0$) is assumed for the calculation below. The simulated current waveform and current ripple of the boost inductor current i_{N1} for $P_{\mathrm{o}} = 5\,\mathrm{kW}$, $L_{\mathrm{N}} = 330\,\mu\mathrm{H}$ and a switching frequency of $f_{\mathrm{s}} = 72\,\mathrm{kHz}$ is plotted in **Fig. 6.39**. It can be verified that the maximum amplitude of the ripple current occurs when the two operating switches show equal duty cycles (e.g. $t = 0.625\,\mathrm{ms}$ in **Fig. 6.39**). This means that also the two line-to-line voltages are equal in this point and the dual boost circuit collapses to a single boost circuit. The maximal current ripple occurs at $\varphi_{\mathrm{N}} = 0\,^\circ$ or $\varphi_{\mathrm{N}} = 180\,^\circ$ for the inductor L_{N1} (consider that cos-waveforms are assumed). According to **TABLE 6.4**, the switch S_{12} is modulated in this point and with the duty-cycle

$$\delta_{12}(\varphi_{\mathrm{N}}) = 1 - M\cos\left(\varphi_{\mathrm{N}} + \frac{\pi}{6}\right) \tag{6.62}$$

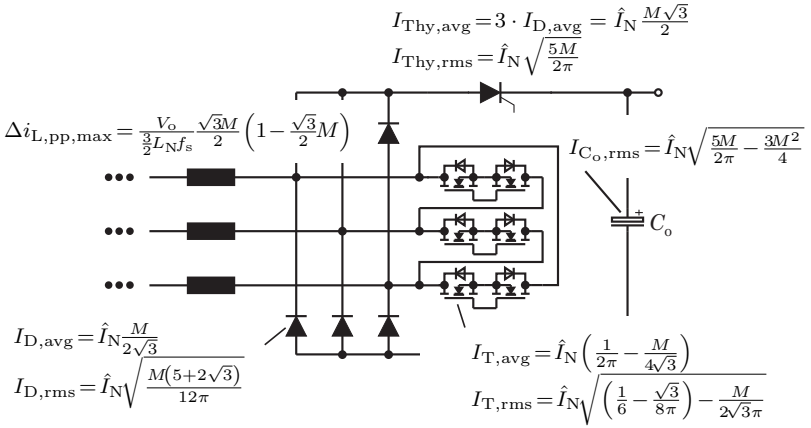


Fig. 6.40: Summary of the analytical approximations for the average and rms current values of the semiconductors and main passive components for $\varphi_{\mathrm{vi}} = 0$.

the inductor voltage balance results in

$$\frac{3}{2} L_{\mathrm{N}} \frac{\Delta i_{\mathrm{L_1,pp,max}}}{\Delta t} = \hat{V}_{12} \cos\left(\varphi_{\mathrm{N}} + \frac{\pi}{6}\right) . \tag{6.63}$$

With $\Delta t = \delta_{12}/f_{\mathrm{s}}$ the maximal peak to peak current ripple at $\varphi_{\mathrm{N}} = 0$

$$\Delta i_{\mathrm{L,pp,max}} = \frac{\hat{V}_{12}}{\frac{3}{2} L_{\mathrm{N}} f_{\mathrm{s}}} \cos\left(\frac{\pi}{6}\right) \left(1 - M \cos\left(\frac{\pi}{6}\right)\right) = \tag{6.64}$$

$$= \frac{V_{\mathrm{o}}}{\frac{3}{2} L_{\mathrm{N}} f_{\mathrm{s}}} \frac{\sqrt{3}}{2} M \left(1 - \frac{\sqrt{3}}{2} M\right) . \tag{6.65}$$

can be calculated. The required boost inductor in order to limit the ripple current to $\Delta i_{\mathrm{L,pp,max}} = k\hat{I}_{\mathrm{N}}$ is therefore given by

$$L_{\mathrm{N}} = \frac{V_{\mathrm{o}}}{k\widehat{I}_{\mathrm{N}} f_{\mathrm{s}}} \frac{M}{\sqrt{3}} \left(1 - \frac{\sqrt{3}}{2} M\right) . \tag{6.66}$$

The factor k is typically chosen to $k = 0.1 \ldots 0.2$ which gives a peak to peak current ripple of 10 to 20 %. The analytical approximations are summarized in **Fig. 6.40**.

TABLE 6.6: Analytically calculated and simulated mean and rms current values of the semiconductors for $\varphi_{\mathrm{vi}} = 0$ and $P_{\mathrm{o}} = 4\,\mathrm{kW}$, $V_{\mathrm{N}} = 115\,\mathrm{V}$ ($M = 0.7$), $f_{\mathrm{s}} = 72\,\mathrm{kHz}$, $L_{\mathrm{N}i} = 330\,\mu\mathrm{H}$.

	Simulated	**Calculated**
$\widehat{I}_{\mathrm{N}}$	16.5 A	16.5 A
$I_{\mathrm{T,avg}}$	0.98 A	0.95 A
$I_{\mathrm{T,rms}}$	3.09 A	3.0 A
$I_{\mathrm{D,avg}}$	3.33 A	3.35 A
$I_{\mathrm{D,rms}}$	6.53 A	6.56 A
$I_{\mathrm{Thy,avg}}$	10.0 A	10.06 A
$I_{\mathrm{Thy,rms}}$	12.3 A	12.35 A
$I_{\mathrm{C,rms}}$	7.16 A	7.16 A
$\Delta i_{\mathrm{L,pp,max}}$	2.6 A	2.67 A

To verify the derived formulas the mean and rms currents for an output power of 4 kW and mains voltage of $V_{\mathrm{N}i} = 115\,\mathrm{V}$ ($M = 0.7$) have been calculated. The results of this calculation are compared in **TABLE 6.6** to the results of a simulation and show a good accuracy.

6.4.3 Calculation of Power Losses

By use of the derived rms and average current levels, the semiconductor losses and the efficiency considering only semiconductors can be calculated. In the following, only the favorable bidirectional switch realization using two series connected MOSFETs, as given in **Fig. 6.2**, will be discussed. The power losses of the MOSFET in general can be divided into switching losses $P_{\mathrm{FET,sw}}$ and conduction losses $P_{\mathrm{FET,con}}$

$$P_{\mathrm{FET}} = P_{\mathrm{FET,con}} + P_{\mathrm{FET,sw}} \ . \tag{6.67}$$

1) Power MOSFET Conduction Losses

Two back to back connected MOSFETs are used to implement the bidirectional switch. Dependent on φ_{N} always one MOSFET is forward biased whereas the second MOSFET is reverse biased during this system state.

In order to calculate the conduction losses of the bidirectional switch the transfer characteristic of a MOSFET, or more precisely of a

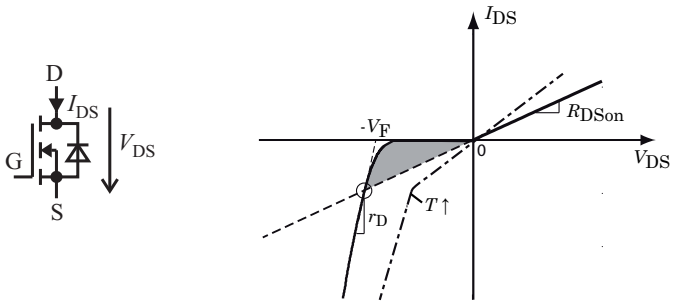


Fig. 6.41: Bidirectional transfer characteristic of a MOSFET where the dashed line shows the transfer characteristic if the MOSFET is turned on.

superjunction device (e.g. CoolMOS), is required. In **Fig. 6.41** the transfer characteristic of a MOSFET is shown. If the MOSFET is forward biased and turned on, the channel conducts current and a voltage drop according to the temperature dependent on-state resistance R_{DSon} occurs. If the MOSFET is reverse biased it's parasitic body diode conducts current. The characteristic of the body diode can be approximated by a forward voltage drop V_F and a small differential resistance r_D. The forward voltage drop would yield to increased conduction losses if the MOSFET is reverse biased which can be lowered by turning the MOSFET on even if it is reverse biased (equivalent to operation of a synchronous rectifier).
The resulting ohmic transfer characteristic is given in **Fig. 6.41** by a dashed line and a considerably reduced voltage drop can be observed which results in reduced conduction losses. The voltage drop of the MOSFET channel reaches the transfer characteristic of the body diode for higher currents and from this point on the current is shared by the channel and by the body diode. Due to the smaller voltage drop of the body diode for currents beyond this point the total conduction losses of the diode/channel configuration will be smaller than the conduction losses of the MOSFET channel alone. The on-state resistance of the MOSFET and the transfer characteristic of the body diode, however, are strongly dependent on temperature which means that the intersection point of voltage drop of the channel and voltage drop of the body diode is also temperature dependent. Whereas the MOSFET channel shows a positive temperature coefficient the body diode shows a negative temperature coefficient. It is therefore excepted

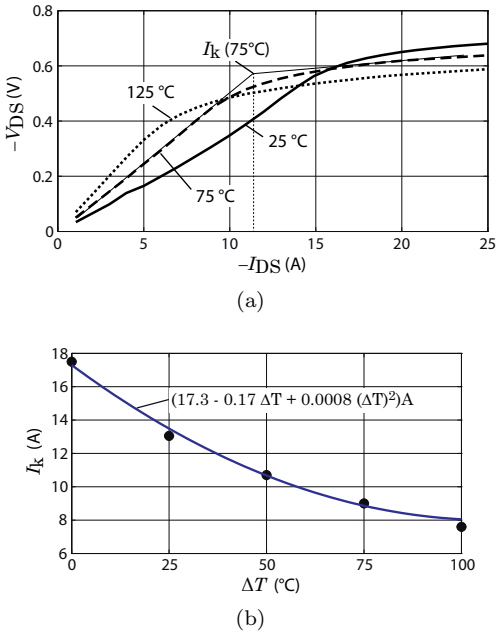


Fig. 6.42: (a) Measured voltage drop of a reverse biased CoolMOS IPW60R045CP as a function of drain-source current I_{DS} and temperature and (b) corresponding currents I_k as a function of temperature difference $\Delta T = T_j - 25\,^{\circ}\mathrm{C}$.

that the intersection point moves down to smaller drain-source currents for higher temperature levels.

It is difficult to model this behavior using the semiconductor parameters listed in the data sheet due to very spare informations on the temperature dependency of the forward characteristic of the body diode. An accurate approach is to measure the temperature dependent voltage drop of the reverse biased MOSFET in on-state. The result of such a measurement using the CoolMOS device IPW60R045CP is given in **Fig. 6.42(a)**.

The MOSFET channel shows, as expected, a low impedance path until the voltage drop across the on-state resistance R_{DSon} is equal to the forward voltage of the body diode. In this region a kink in the characteristic of the drain source voltage V_{DS} occurs and a much lower gradient can be read for higher current levels. The gradients before and after

the kink and the current I_k are additionally plotted in **Fig. 6.42(a)** for a temperature of 75 °C. The current transition from the channel to the body diode is not sharp, but a smooth transition can be observed. In order to determine the temperature dependent kink current $I_\mathrm{k}(T)$, linear approximations of the curve sections can be used (cf. **Fig. 6.42(a)**). It is obvious that the kinks appear at considerably lower current levels for higher temperatures. The corresponding currents I_k are plotted in **Fig. 6.42(b)** as a function of the temperature difference $\Delta T = T_\mathrm{j} - 25\,^\circ\mathrm{C}$. It can be approximated by

$$I_\mathrm{k} = \Big(17.3 - 0.17\Delta T + 0.0008\,(\Delta T)^2\Big)\,\mathrm{A} \tag{6.68}$$

for further calculations.

The transfer characteristic given in **Fig. 6.42** is nonlinear and the conduction losses of the corresponding MOSFETs can therefore not directly be calculated by application of the rms (6.54) and average (6.55) current values of the switch. The voltage drop can, however, be approximated by two piecewise linear elements separated by the current level I_k. The voltage drop can by modeled by the R_DSon for currents below I_k of the MOSFET and for larger currents a diode characteristic modeled by a forward voltage drop V_F and a differential resistor r_D can be applied. Without loosing generality the temperature dependent power losses of the reversed biased switch can be calculated using

$$\begin{aligned} P_{\mathrm{FET,con,r}}(\Delta T) = \frac{2}{2\pi}\Bigg(& \int_0^{\varphi_k} R_\mathrm{DSon}(\Delta T) i_{\mathrm{S}ij}^2(\varphi)\delta_{ij}(\varphi)d\varphi + \\ & + \int_{\varphi_k}^{\frac{\pi}{3}} \Big(i_{\mathrm{S}ij}(\varphi)V_\mathrm{F}(\Delta T) + i_{\mathrm{S}ij}^2(\varphi) r_\mathrm{D}(\Delta T)\Big)\delta_{ij}(\varphi)d\varphi\Bigg) \end{aligned} \tag{6.69}$$

for $\varphi_\mathrm{k} < \frac{\pi}{3}$ where φ_k can be calculated by

$$i_{\mathrm{S}ij}(\varphi_\mathrm{N}) = \hat{I}_\mathrm{N}\sin(\varphi_\mathrm{k}) = I_\mathrm{k}(\Delta T)\ . \tag{6.70}$$

Please note, that in contrast to other derivations in this work a $\sin(x)$-function is assumed instead of the $\cos(x)$-function which corresponds to the space vector representation. If φ_k is larger than $\frac{\pi}{3}$, e.g. due to partial load condition, only the on-state resistance of the channel has to be considered and the distinction of cases is not required. The junction

temperature T_j is assumed to be constant over one mains period, which is justified by the thermal capacitances of the semiconductor chip and case, and the on-state resistance $R_\mathrm{DSon}(\Delta T)$ can therefore be considered as a constant for integration of (6.69). The corresponding duty cycle δ_{ij} can be written as

$$\delta_{ij}(\varphi_\mathrm{N}) = 1 - M \sin\left(\varphi_\mathrm{N} + \frac{\pi}{6}\right) \ . \tag{6.71}$$

Equation (6.69) is a function of the junction temperature T_j which is on the other hand a result of semiconductor losses and a direct solution is hence not possible. An iterative approach can however be applied. Integration of (6.69) is possible but yields to an unhandy solution and is therefore not given here.

According to the measurement results the temperature dependent parameters of the MOSFET IPW60R045CP can be modeled by

$$\begin{aligned} V_\mathrm{F}(\Delta T) &= V_\mathrm{F,25}\left(1 + \alpha_{\mathrm{V_F}}\Delta T\right) = 0.7\,\mathrm{V}\left(1 - 66 \cdot 10^{-6}\mathrm{K}^{-1}\Delta T\right) \\ r_\mathrm{D}(\Delta T) &= r_\mathrm{D,25}\left(1 + \alpha_{\mathrm{r_D}}\Delta T\right) = 9.7\,\mathrm{m\Omega}\left(1 - 3 \cdot 10^{-5}\mathrm{K}^{-1}\Delta T\right) \ . \end{aligned} \tag{6.72}$$

Analogous to the calculation shown in section 5.3.1, the conduction losses of the forward biased MOSFET can be calculated using its temperature dependent on-state resistance

$$\begin{aligned} R_\mathrm{DSon}(\Delta T, I_\mathrm{DS}) = R_\mathrm{DSon,25}\left(1 + \alpha_1\Delta T + \alpha_2\Delta T^2\right) \\ \left(1 + \beta_1 I_\mathrm{DS} + \beta_2 I_\mathrm{DS}^2\right) \end{aligned} \tag{6.73}$$

where $R_\mathrm{DSon,25}$ is the chip area dependent on-state resistance at $T_j = 25\,^\circ\mathrm{C}$ and $I_\mathrm{DS} = 0\,\mathrm{A}$. If the dependence on I_DS is neglected the conduction losses of the forward biased MOSFET can be calculated using the rms current stress of the bidirectional switch derived in (6.55)

$$P_\mathrm{FET,con,f}(\Delta T) = R_\mathrm{DSon}(\Delta T) I_\mathrm{T,rms}^2 \ . \tag{6.74}$$

According to **Fig. 6.38**, each MOSFET is forward biased and reverse biased for a duration of $120\,^\circ$ and the total conduction losses of one MOSFET are given by

$$P_\mathrm{FET,con} = P_\mathrm{FET,con,f} + P_\mathrm{FET,con,r} \ . \tag{6.75}$$

2) Power MOSFET Switching Losses

The switching losses are separated into turn-on losses and turn-off losses

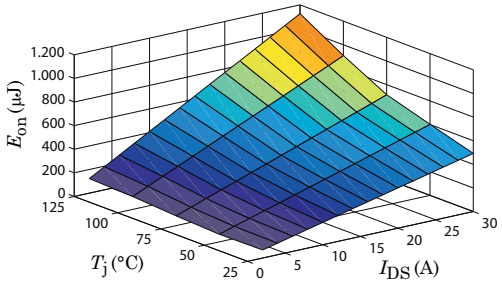


Fig. 6.43: Measured turn-on energies of the combination CoolMOS IPW60R045CP and the Si-diode APT30B60BHB as a function of I_{DS} and junction temperature T_j at $V_{DS} = 400\,V$.

(see also section 5.3.1). A Si-diode is used as rectifier diode for implementation of the Δ-switch rectifier system instead of the SiC-diodes used for the VR system (cf. **TABLE 5.8**). Si-diodes show a pronounced, temperature dependent reverse recovery current and a measurement of turn-on losses is essential for determining the turn-on switching losses. During turn-off of the MOSFET it's nonlinear output capacitance is charged by the input current which does not create additional losses. The energy stored in this capacitance is, however, dissipated during turn-on in the MOSFETs channel and this part of switching losses can be described by the stored energy E_{400V} given in the data sheet.

As can easily be verified, the current only commutates between one diode and one switch even if at least an additional rectifier diode and the second MOSFET of the bidirectional switch implementation are involved in the commutation path. The boost-type test circuit of section 5.1 (cf. **Fig. 5.5**) is used to measure the switching losses of the CoolMOS IPW60R045CP and Si-diode APT30B60BHB combination. The results are illustrated in **Fig. 6.43** and for further calculations the measured turn-on energies can be fitted by

$$E_{on}(\Delta T, I_{DS}) = \left(k_0 + k_1 I_{DS} + k_2 I_{DS}^2\right)(1 + \gamma \Delta T) \ . \qquad (6.76)$$

Due to the pronounced reverse recovery current of the Si-diode the applied combination shows much higher turn-on losses then the CoolMOS/SiC-diode combination. This can be tolerated due to the moderate switching frequency of 72 kHz. The Si-diodes typically show

smaller forward voltages yielding to smaller conduction losses which justifies the use of Si-diodes. It has to be noted here again that the most accurate results can be achieved if the switching loss measurements are performed on the final hardware using the final PCB layout. The reason for that are the parasitic capacitances of the construction and the PCB layout which considerably affect switching losses.
Using the measured turn-on energies the switching losses can be calculated under consideration of **Fig. 6.38** by

$$\begin{aligned}
P_{\mathrm{sw}} &= f_{\mathrm{s}} \frac{2}{2\pi} \int_0^{\frac{\pi}{3}} \left(k_0 + k_1 \hat{I}_{\mathrm{N}} \sin(\varphi) + k_2 \big(\hat{I}_{\mathrm{N}} \sin(\varphi)\big)^2 \right) \big(1 + \gamma \Delta T\big) d\varphi + \\
&\quad + f_{\mathrm{s}} E_{400\mathrm{V}} = \\
&= \frac{f_{\mathrm{s}}}{\pi} \left(k_0 \varphi + k_1 \hat{I}_{\mathrm{N}} \big(-\cos(\varphi)\big) + \frac{k_2 \hat{I}_{\mathrm{N}}^2}{2} \left(\varphi - \frac{\sin(2\varphi)}{2} \right) \right) \big(1 + \gamma \Delta T\big) \Bigg|_0^{\frac{\pi}{3}} + \\
&\quad + f_{\mathrm{s}} E_{400\mathrm{V}} = \\
&= f_{\mathrm{s}} \left(\left(\frac{k_0}{3} + \frac{k_1}{4} I_{\mathrm{N,avg}} + k_2 I_{\mathrm{N,rms}}^2 \left(\frac{4\pi - 3\sqrt{3}}{12\pi} \right) \right) \big(1 + \gamma \Delta T\big) + E_{400} \right)
\end{aligned} \tag{6.77}$$

if in contrast to other derivations in this work, where $\cos(x)$-functions of the current shape are assumed, $\sin(x)$-functions are used.

3) Total Power MOSFET Losses
The total MOSFET power losses

$$P_{\mathrm{FET,tot}} = 6 \left(P_{\mathrm{con,f}} + P_{\mathrm{con,r}} + P_{\mathrm{sw}} \right) \tag{6.78}$$

can be calculated using the derived results for the power MOSFET conduction and switching losses. Each switch is partly operating in forward and in reverse direction in sections of the mains period and hence the forward conduction losses $P_{\mathrm{con,f}}$ and reverse conduction losses $P_{\mathrm{con,r}}$ must be considered.

4) Rectifier Diode Losses
In order to calculate the conduction losses of the rectifier diodes the derived average and rms currents of (6.57) can be used in conjunction with the data sheet values of the rectifier diodes. As for the body diode of the MOSFET the transfer characteristic of the rectifier diode can be

approximated by a forward voltage drop V_F and a differential resistance r_D and the conduction losses can therefore be calculated by

$$P_\mathrm{D,tot} = 6P_\mathrm{D} = 6\left(V_\mathrm{F} I_\mathrm{D,avg} + r_\mathrm{D} I_\mathrm{D,rms}^2\right) \ . \tag{6.79}$$

5) Thyristor Losses

The calculation of the thyristors conduction losses can be performed in an equal manner using the current levels given in (6.58) and (6.59). In the final construction three thyristors are connected in parallel in order to optimize the commutation path of the switches. A uniform current distribution on the three thyristors is assumed and under consideration of the parameters given in the data sheet the total conduction losses of the three thyristors

$$P_\mathrm{Thy,tot} = 3P_\mathrm{Thy} = 3\left(V_\mathrm{F,Thy}\frac{I_\mathrm{Thy,avg}}{3} + \left(\frac{I_\mathrm{Thy,rms}}{3}\right)^2 r_\mathrm{D,Thy}\right) \tag{6.80}$$

can be calculated.

5) Output Capacitor Losses

Electrolytic capacitors are typically used for the output capacitors due to the high energy density of this capacitor technology [123]. The ESR of this capacitor type in conjunction with the rms current stress of the capacitors yields to power losses. Also the leakage current of the capacitors has to be considered. If N is the total number of capacitors connected in parallel used to realize the output capacitor C_o the total capacitor losses

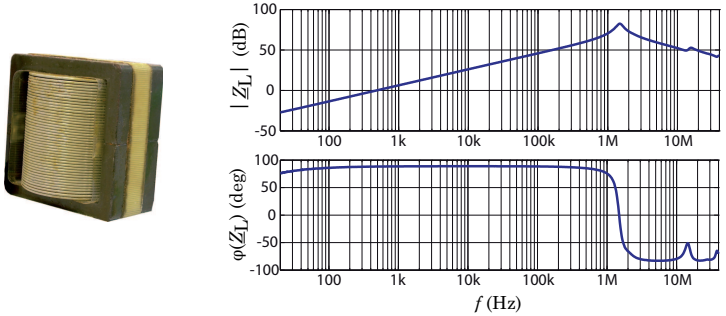
$$P_{\mathrm{C_o}} = I_\mathrm{C,rms}^2 \frac{ESR}{N} + N\left(I_\mathrm{C,leak} V_\mathrm{o}\right) \tag{6.81}$$

can be calculated using the rms current stress derived in (6.61) and the leakage current $I_\mathrm{C,leak}$ listed in the data sheet.

5) Losses in the Boost Inductors

In this section only a very rough and practical discussion on boost inductor losses will be given. Several calculation methods and models exist for each loss mechanism which may yield to more accurate prediction of power losses but will not be discussed here for sake of a simple converter loss model.

In general the boost inductor losses can be divided into copper losses caused by the winding and core losses caused by the hysteresis effect



(a) (b)

Fig. 6.44: (a) Helical winding boost inductor (Schott Inc. HWT-19) with $L_{\mathrm{N}} = 330\,\mu\mathrm{H}$ using the magnetic material -52 from Micrometals Inc. and (b) Bode plot of inductor impedance. Resonance occurs at 1.44 MHz which yields to a parasitic winding capacitance of $C_{\mathrm{w}} = 37\,\mathrm{pF}$.

and eddy currents in the magnetic material. Regarding copper losses, skin and proximity effects play a major role and are defined by the effective copper area and winding arrangement. Dependent on the winding configuration, which is in a practical implementation also dependent on the magnetic core geometry, models for skin and proximity effects can be derived and copper losses can be calculated by application of these models. In this section the copper losses, and also the core losses, of an already manufactured inductor are determined (Schott Inc. HWT-19, cf. **Fig. 6.44**). The helical copper foil winding results in a large copper filling factor at a moderate parasitic capacitance. Skin and Proximity effects, however, increase the AC winding resistance for higher frequencies. Due to the orthogonality of the sine-function of different frequencies

$$\int_0^{2\pi} \sin(n\varphi)\sin(m\varphi)d\varphi = 0 \quad \text{for} \quad m \neq n \tag{6.82}$$

the current waveform can be separated into a low-frequency part $I_{\mathrm{N,rms}}$ showing only the fundamental mains frequency f_{N} and a ripple current $I_{\mathrm{r,rms}}$ at switching frequency f_{s}. All higher switching frequency harmonics and all low-frequency harmonics of the mains are neglected for this purpose.

In a next step the AC-resistances of the implemented inductor winding are measured using the Bode network analyzer [250] which results in the

resistances $R_{\mathrm{Cu,400Hz}}$, $R_{\mathrm{Cu,800Hz}}$ and $R_{\mathrm{cu,72kHz}}$. Using the rms values of the fundamental current and the current ripple the cooper losses can approximately be calculated using

$$P_{\mathrm{v,Cu}} = R_{\mathrm{Cu,f_N}} I_{\mathrm{N,rms}}^2 + R_{\mathrm{Cu,f_s}} I_{\mathrm{r,rms}}^2 \ . \tag{6.83}$$

On one hand the approach shown in section 5.4.1 using the improved generalized Steinmetz equation can be applied for the calculation of the core losses. The corresponding flux densities can be calculated by

$$B(\varphi_{\mathrm{N}}) = \frac{i(\varphi_{\mathrm{N}}) L_{\mathrm{N}}}{A_{\mathrm{Fe}} N} \tag{6.84}$$

where L_{N} is the boost inductance value, A_{Fe} is the effective magnetic area and N is the number of turns. A separation of flux-density into a fundamental part and a ripple flux-density in a strict sense is not possible. The high frequency current ripple results in small magnetizing loops (minor loops) which shows, due to the nonlinear material properties of the magnetic material, different power losses dependent on the instantaneous value of the low-frequency component of the flux density. This effect can, however, be neglected in a first approach without making a large error. According to the loss formulas given in the data sheet of the applied material -52 of Micrometals Inc. [246] the core losses can therefore be approximated by

$$\begin{aligned} P_{\mathrm{v,core}} = & \frac{f_{\mathrm{N}}}{\frac{a}{\hat{B}_{\mathrm{N}}^3} + \frac{b}{\hat{B}_{\mathrm{N}}^{2.3}} + \frac{c}{\hat{B}_{\mathrm{N}}^{1.65}}} + d f_{\mathrm{N}}^2 \hat{B}_{\mathrm{N}}^2 + \\ & + \frac{f_{\mathrm{s}}}{\frac{a}{\hat{B}_{\mathrm{s}}^3} + \frac{b}{\hat{B}_{\mathrm{s}}^{2.3}} + \frac{c}{\hat{B}_{\mathrm{s}}^{1.65}}} + d f_{\mathrm{s}}^2 \hat{B}_{\mathrm{s}}^2 \end{aligned} \tag{6.85}$$

where $\hat{B}_{\mathrm{N}}$ is the peak flux density caused by the fundamental frequency f_{N} and $\hat{B}_{\mathrm{s}}$ is the peak flux density caused by the ripple current. The parameters a, b, c and d are given in the data sheet. The resulting inductor losses

$$P_{\mathrm{v,L,tot}} = 3 P_{\mathrm{v,L}} = 3 \left(P_{\mathrm{v,Cu}} + P_{\mathrm{v,core}} \right) \tag{6.86}$$

can be determined summarizing the calculated copper and core losses.

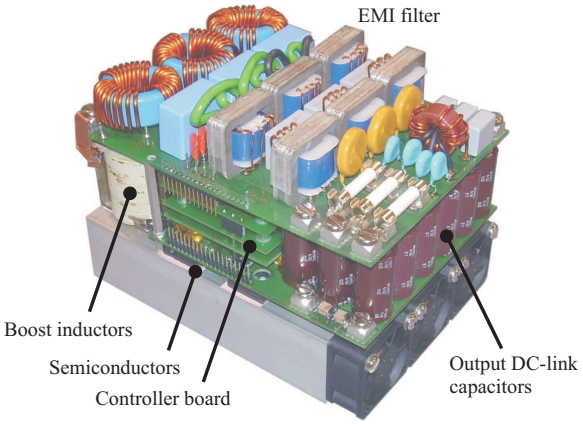


Fig. 6.45: 5 kW Δ-switch rectifier laboratory prototype. Dimensions: 170 mm × 120 mm × 128 mm.

6.5 Laboratory Prototype

Based on the proposed controller concept a laboratory setup of the Δ-switch rectifier according to the specifications given in TABLE 6.7 has been built. The prototype is shown in **Fig. 6.45**. An existing EMI filter, originally designed for a 72 kHz Vienna-type rectifier, was applied to this rectifier. The overall dimensions of the system are 170 mm × 120 mm × 128 mm (6.69 in × 4.72 in × 5.04 in), thus giving a power density of 1.9 kW/dm^3 (or 31.4 W/in^3). The system is forced air-cooled and has a weight of 3.78 kg resulting in a power to weight ratio of 1.3 kW/kg. The proposed controller is digitally implemented in a fixed point Texas Instruments DSP (TI 320F2808) and a switching frequency of 72 kHz is used. CoolMOS power transistors IPP60R045CP with a very low R_{DSon} of 45 mΩ are used for implementation of the bidirectional switches, and the Si-diodes APT30D60BHB are employed as rectifier diodes. A summary of the devices is given in **TABLE 6.9**.

The occupied volumes of the main system elements are listed in **TABLE 6.8** and illustrated in **Fig. 6.46**. The boxed volumes of the system elements/PCB boards are used for volume calculation and the gaps between these boxes are summarized to the item "Air". The air in between the components is included into the boxed volumes. The heat sink in-

TABLE 6.7: Specifications of the implemented laboratory prototype.

Input voltage (L-N):	$V_N = 97\,V_{RMS} \ldots 132\,V_{RMS}$
Input frequency:	$f_N = 360\,Hz \ldots 800\,Hz$
Switching frequency:	$f_s = 72\,kHz$
Output voltage:	$V_o = 400\,V_{DC}$
Output power:	$P_o = 5\,kW$

TABLE 6.8: Volumes of the main system elements of the implemented Δ-switch rectifier system.

	Volume (dm^3)	Share of tot. volume
Semiconductors, Aux, Control	$0.34\,dm^3$	13 %
Boost inductors	$0.3\,dm^3$	12 %
Output capacitors	$0.25\,dm^3$	10 %
EMI filter	$0.63\,dm^3$	24 %
Heat sink, fans	$0.82\,dm^3$	31 %
Air	$0.27\,dm^3$	10 %
Total	$2.61\,dm^3$	100 %

cluding fans, is the biggest system part and takes about 31 % of the total system volume. It is interesting, that the semiconductors together with the gate drive PCB, auxiliary supply and control PCB take nearly the same share of system volume as the boost inductors. The second largest system element is the EMI filter which amounts to 24 %. Even if the EMI filter has not been designed for the two-level Δ-switch rectifier topology a proper designed EMI filter will show similar volume and as will be shown below the applied EMI filter nearly fulfills the EMI norms. The output capacitors are designed to be able to take on the ripple current. In order to guarantee a certain possible holdup time the required capacitance and volume could be much higher. An increase in switching frequency would reduce the volume of the EMI filter and the boost inductors but would on the other hand increase the volume of the heat sink.

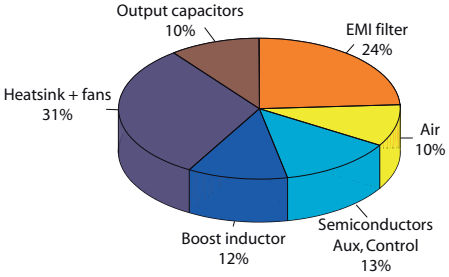


Fig. 6.46: Volume distribution of the main system elements of the constructed 5 kW laboratory prototype with a switching frequency of $f_s = 72\,\text{kHz}$.

6.5.1 Calculated and Measured Efficiency

The power losses and the resulting efficiency of the implemented Δ-switch rectifier system are calculated in this section for $f_N = 400\,\text{Hz}$ using the analytical expressions derived in section 6.4.3. The corresponding component parameters, partly based on data sheet specifications and partly based on measurements, are listed in **TABLE 6.9**. As shown in section 5.3.1, the thermal interface of the semiconductors to the heat sink and also the heat sink itself have to be modeled in order to determine the junction temperatures of the semiconductors. The corresponding equations for conduction and switching losses can thus not be solved directly. An iterative solution is used instead where a junction temperature is assumed for calculation of the losses and verified using the calculated system losses and the properties of the thermal interface. All the semiconductors are mounted on a forced air-cooled heat sink with a thermal resistance of

$$R_{\text{th,sa}} = 0.3\,\frac{\text{K}}{\text{W}} \tag{6.87}$$

and the MOSFETs show a total thermal resistance of

$$R_{\text{th,js}} = 0.8\,\frac{\text{K}}{\text{W}} \tag{6.88}$$

if also a Kapton-foil for isolation is considered. Due to the lack of accurate thermal parameters of the applied rectifier diodes and thyristors the temperature dependence of V_F and r_D is not modeled and the values for a junction temperature of 100 °C are used instead.

TABLE 6.9: Selected power devices and corresponding parameters for implementation of the Δ-switch rectifier.

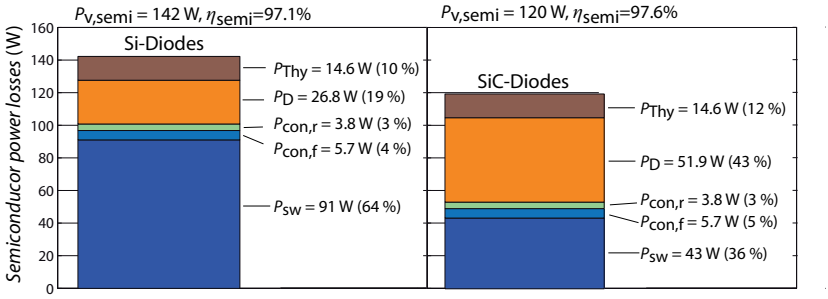
MOSFET CoolMOS IPW60R045CP	
Channel	Body diode
$R_{\mathrm{DSon},25} = 39\,\mathrm{m\Omega}$	$V_{\mathrm{F},25} = 0.7\,\mathrm{V}$
$\alpha_1 = 0.0083\,\mathrm{K}^{-1}$	$\alpha_{\mathrm{V_F}} = -66 \cdot 10^{-6}\,\mathrm{K}^{-1}$
$\alpha_2 = 43 \cdot 10^{-6}\,\mathrm{K}^{-1}$	$r_{\mathrm{D},25} = 9.7\,\mathrm{m\Omega}$
$\beta_1, \beta_2 = 0$	$\alpha_{\mathrm{r_D}} = -3 \cdot 10^{-5}\,\mathrm{K}^{-1}$
Switching Losses	
$k_0 = 38.3\,\mu\mathrm{J}$	$k_1 = 15\,\frac{\mu\mathrm{J}}{\mathrm{A}}$
$k_2 = 0$	$\gamma = 0.011\,\mathrm{K}^{-1}$
$E_{400\mathrm{V}} = 27.5\,\mu\mathrm{J}$	
Diode APT30B60BHB	**Thyristor 40TPS12A**
$V_{\mathrm{F}} = 0.8\,\mathrm{V}$	$V_{\mathrm{F,Thy}} = 1.04\,\mathrm{V}$
$r_{\mathrm{D}} = 13\,\mathrm{m\Omega}$	$r_{\mathrm{D,Thy}} = 10\,\mathrm{m\Omega}$
Output Capacitors 18× **Nippon Chemicon KXG** 82 µF/**450 V**	
$ESR = 1\,\Omega$	$I_{\mathrm{leak}} = 250\,\mu\mathrm{A}$
Boost Inductor Schott HWT-193 326 µH	
$A_{\mathrm{Fe}} = 227\,\mathrm{mm}^2$	$V_{\mathrm{Fe}} = 27000\,\mathrm{mm}^3$
$N = 44$	
Core Material Micrometals -52	
$a = 10^9$	$c = 2.1 \cdot 10^6$
$b = 1.1 \cdot 10^8$	$d = 6.9 \cdot 10^{-14}$
Winding Resistance	
$R_{\mathrm{Cu},50\mathrm{Hz}} = 12\,\mathrm{m\Omega}$	$R_{\mathrm{Cu},400\mathrm{Hz}} = 27\,\mathrm{m\Omega}$
$R_{\mathrm{Cu},800\mathrm{Hz}} = 45\,\mathrm{m\Omega}$	$R_{\mathrm{Cu},72\mathrm{kHz}} = 3.6\,\Omega$

The results of the loss calculation using different mains voltages for $f_{\mathrm{N}} = 400\,\mathrm{Hz}$ and $P_{\mathrm{o}} = 5\,\mathrm{kW}$ are given in TABLE 6.10 where also the calculated semiconductor and total efficiencies are listed.

TABLE 6.10: Calculated power loss break-down and efficiency of the proposed Δ-switch rectifier for an output power of $P_o = 5\,\text{kW}$, a switching frequency of $f_s = 72\,\text{kHz}$ and a mains frequency of $f_N = 400\,\text{Hz}$.

Input voltage (line rms)	97.7	115	132	V
Input current (rms)	17.9	15.2	13.3	A
Modulation index	0.598	0.704	0.808	
Losses				
MOSFET conduction losses	16.3	9.6	5.4	W
MOSFET switching losses	102.3	91	83.1	W
Total MOSFET losses	118.6	100.6	88.5	W
Diode losses	27.8	26.8	26	W
Thyristor losses	14.7	14.6	14.4	W
Total semiconductor losses	161.1	142	128.9	W
Semiconductor efficiency	96.7	97.1	97.4	%
Input choke	83.9	66.8	55.8	W
Output capacitors	9.3	6.7	4.8	W
Auxiliary power	10	10	10	W
Additional losses (EMI,...)	30	30	30	W
Total power losses	294.3	255.5	229.5	W
Efficiency	94.1	94.9	95.4	%

The semiconductor losses are illustrated in **Fig. 6.47** for $V_N = 115\,\text{V}$. The total semiconductor losses of 142 W are clearly dominated by switching losses of the Si-diode/CoolMOS combination. The second largest portion of semiconductor losses are the conduction losses of the rectifier diodes followed by the conduction losses of the thyristors. The forward and reverse biased conduction losses of the MOSFETs on the other hand are rather small. A semiconductor efficiency of 97.1 % can be achieved with the described semiconductors. Consideration of the the heat sink and the semiconductors thermal interfaces yields to a MOSFET junction temperature of $T_j = 105\,°\text{C}$ if an ambient temperature of $T_a = 45\,°\text{C}$ is assumed.
The dominating switching losses can be reduced by application of SiC-diodes which show, except of a capacitive current charging the



(a)

Fig. 6.47: Calculated semiconductor power loss break-down if either Si diodes or SiC diodes are used; System parameters: $f_N = 400\,\text{Hz}$, $V_N = 115\,\text{V}$, $V_o = 400\,\text{V}$, $f_s = 72\,\text{kHz}$ and $P_o = 5\,\text{kW}$.

parasitic output capacitance at turn-off, no reverse recovery current. As already mentioned, SiC-diodes show a larger forward voltage drop which yields to higher conduction losses on the other hand. The switching losses of the SiC/CoolMOS combination are estimated using the switching loss measurements given in section 5.1.3 and the results are also summarized in **Fig. 6.47**. Whereas the switching losses can be cut in half, the conduction losses of the rectifier diodes are doubled which all together slightly increases the semiconductor efficiency to 97.6 %. Using SiC-diodes the distribution of semiconductor losses on the particular components is more even which could be an advantage for cooling of the devices. On the other hand, the costs of SiC-diodes are much higher than the costs of Si-diodes and since the total semiconductor losses of the two implementations are more or less equal the use of Si-diodes is preferred for the switching frequency of 72 kHz. The SiC-diodes would show their strength if the switching frequency would be increased to higher values where Si-diodes would end up with far to high switching losses.

Fig. 6.48 shows the power loss break-down considering the main passive components. Next to the largest part of semiconductor losses $P_{v,semi}$ (56 %) the total system losses are dominated by the inductor losses $P_{v,L}$ which are mainly dominated by core losses at $f_N = 400\,\text{Hz}$. The constructed rectifier system and also the boost inductors are designed for 50 Hz applications and unfortunately the core material is not suited for

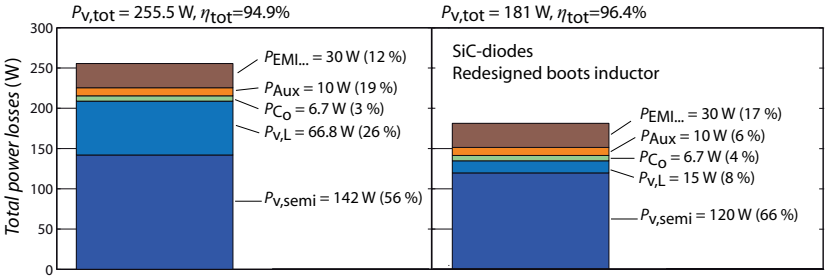
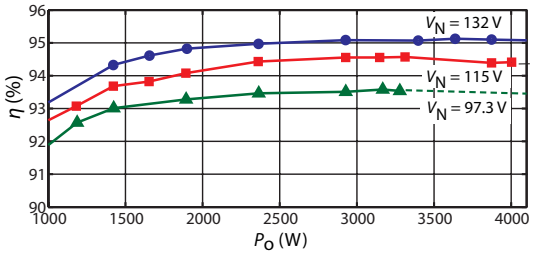


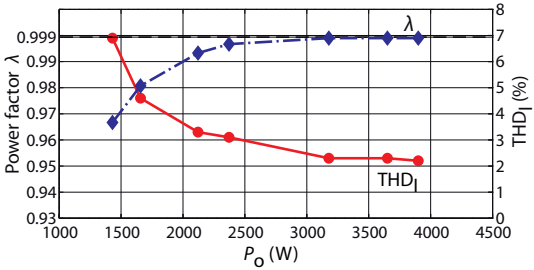
Fig. 6.48: Calculated total system power loss distribution of the constructed rectifier system and a rectifier system using SiC-diodes and optimized boost inductors. System parameters: $f_N = 400\,\text{Hz}$, $V_N = 115\,\text{V}$, $V_o = 400\,\text{V}$, $f_s = 72\,\text{kHz}$ and $P_o = 5\,\text{kW}$.

360 Hz - 800 Hz and yields to inadmissible high inductor losses. The total system losses are 255.5 W and this results in a total system efficiency of only 94.5 % at $f_N = 400\,\text{Hz}$.
A more sophisticated design of the boost inductors using a ferrite core instead of the unsuited powder core could reduce the inductor losses considerably and the total boost inductor losses are excepted to be $P_{v,L} = 15\,\text{W}$ instead of 66.8 W which is a reduction of almost 80 %. The loss break-down of a rectifier system using SiC-diodes and redesigned boost inductors is illustrated in **Fig. 6.48**. The main losses are now semiconductor losses which take about 60 % of total system power losses. The remaining power losses are more or less equally spread on boost-inductor losses $P_{v,L}$, losses caused by the EMI filter and the wiring P_{EMI}, auxiliary power supply P_{Aux} and losses in the output capacitors P_{C_o}. It is obvious that the total system losses could be reduced to 181 W which would result in an efficiency of 96.4 %.

The measured efficiency for the specified input voltage range is depicted in **Fig. 6.49(a)**. The measured efficiency varies between 93.5% and 95% and the results are in good agreement with the calculated efficiencies which verifies the correctness of the derived loss models. The measured efficiencies are somewhat lower than the calculated values and the difference has been found in the current dependent losses of the EMI filter. For the sake of brevity these losses have been considered as a constant term in the calculation. A three-phase power source [264] is used for testing the rectifier and the output current capability of this power source (5 kW, 13 A_{rms}) limits the power level for the given efficiency measurements.



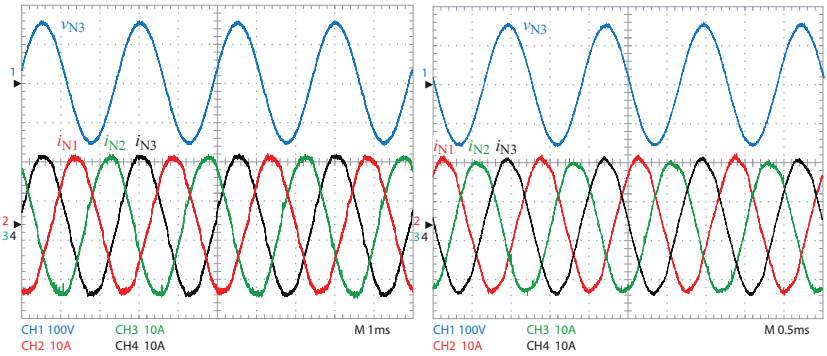
(a)



(b)

Fig. 6.49: (a) Measured efficiency of the 5 kW laboratory prototype at $f_N = 400$ Hz for the specified mains voltages and (b) measured power factor λ and input current quality THD_I as a function of P_o ($f_N = 400$ Hz, $f_s = 72$ kHz and $V_N = 115$ V).

The measured power factor λ is plotted in **Fig. 6.49(b)** together with the measured input current quality (expressed by the THD_I-value). Whereas at high power levels a power factor of $\lambda = 0.999$ can be achieved the power factor drops to lower values at partial load. The reason can be found in the capacitive current drawn by EMI filter capacitors. As already mentioned, an existing EMI filter originally designed for a 50 Hz VR system is used for the Δ-switch rectifier system. The total amount of input capacitance for a system operated with 360 Hz – 800 Hz may be reduced but one has to keep in mind that a specific amount of input capacitance is needed for proper operation of the rectifier system. As analyzed in [258], the Δ-switch rectifier system would be able to compensate a specific amount of current phase lag which is discussed below. **Fig. 6.49(b)** also confirms that a very good input current quality ($THD_I < 4\,\%$) can be achieved despite the relatively low switching



(a) (b)

Fig. 6.50: Measurement results taken from the laboratory prototype at an output power level of $P_o = 4\,\text{kW}$; (a) Input currents and phase voltage at $f_N = 400\,\text{Hz}$ ($\text{THD}_I = 2.3\,\%$, $\lambda = 0.999$) and (b) at $f_N = 800\,\text{Hz}$ ($\text{THD}_I = 2.9\,\%$, $\lambda = 0.999$).

frequency of 72 kHz.

6.5.2 Experimental Results

The measured input currents of the rectifier system are given in **Fig. 6.50(a)** for $P_o = 4\,\text{kW}$, $f_N = 400\,\text{Hz}$ where an excellent THD_I of 2.3 % and a power factor of $\lambda = 0.999$ have been measured. **Fig. 6.50(b)** shows a measurement of the input currents at $P_o = 4\,\text{kW}$ and $f_N = 800\,\text{Hz}$. There, a THD_I of 2.9 % and a power factor of $\lambda = 0.999$ have been measured. This verifies, that even at 800 Hz a good input current quality can be achieved by the Δ-switch rectifier system.

In **Fig. 6.51** the measured inductor current i_{N1} over two periods is shown for $P_o = 4\,\text{kW}$, $V_N = 115\,\text{V}$ and $f_N = 400\,\text{Hz}$. An increased current ripple can be observed in the phase drawing the largest input current (e.g. $\varphi_N \in [-30° \ldots 30°]$ for i_{N1}), where the ripple current shows its maximum at $\varphi_N = 0°$. This is in good agreement with the simulation results and confirms the operation of the proposed current controller.

The individual input current harmonics of the rectifier system operating at $P_o = 4\,\text{kW}$ and $f_N = 400\,\text{Hz}$ are summarized in **Fig. 6.52**

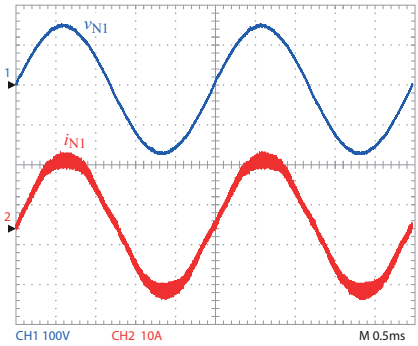


Fig. 6.51: Measured inductor current i_{N1} at $P_o = 4\,\text{kW}$, $V_N = 115\,\text{V}$ and $f_N = 400\,\text{Hz}$.

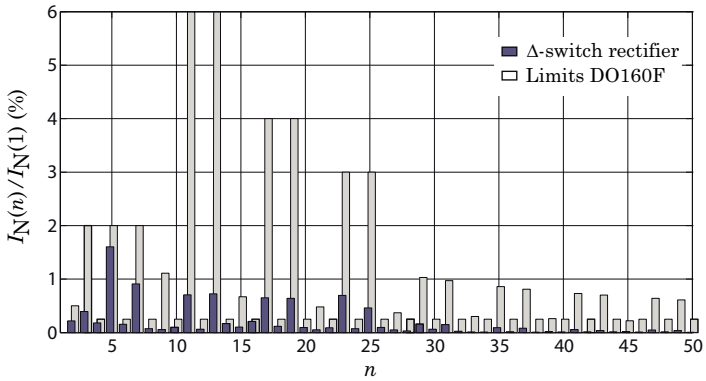


Fig. 6.52: Measured input current harmonics compared to the limits of the standard DO160F ($P_o = 4\,\text{kW}$ and $f_N = 400\,\text{Hz}$).

together with the limits of the airborne standard DO160F. Each harmonic $I_N(n)$ is related to the fundamental $I_N(1)$. All harmonics are quite below the limits of DO160F which highlights the good performance of the Δ-switch rectifier system. The standard itself also covers ATUs and TRUs which explains the large harmonic limits for $n = 11, 13, 17, 19, ...$ (the limits for $n = 11, 13$ are not fully shown). The relative large amount of fifth harmonic is a result of the rather low switching frequency.

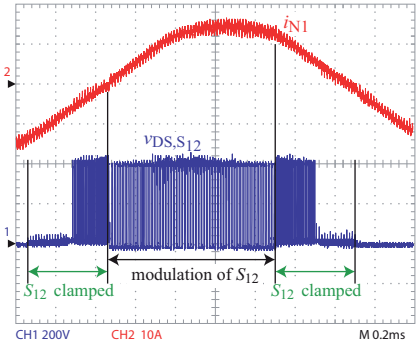


Fig. 6.53: Measured drain-source voltage v_{DS} of switch S_{12} at an output power level of $P_o = 4\,\text{kW}$.

As mentioned in section 6.4, the commutation paths include four semiconductor devices. It is therefore difficult to minimize the parasitic inductance of this path in practice. The result is a considerable ringing of the MOSFETs drain-source voltages at turn off. In **Fig. 6.53**, a measurement of the drain-source voltage v_{DS} of switch S_{12} is shown. Although the layout has been optimized to minimize the commutation path inductance, a voltage overshoot of $\approx 60\,\text{V}$ can be observed in case the switch is PWM operated. In addition the MOSFET, as depicted in **Fig. 6.53**, experiences a PWM shaped blocking voltage, originating from the two other switches while the device is clamped into continuous off state (S_{12} in $\varphi_N \in [30° \ldots 90°, 210° \ldots 270°]$). This voltage overshoot is unfortunately even higher than the over-voltage generated from the switch itself which has to be considered in the system design.
The occurring over voltage is a major practical problem of the Δ-switch rectifier topology. Each bidirectional switch has, depending on the input current direction, two different commutation paths. This is tightened by the fact that if for instance the commutation path of switch S_{12} is optimized in the PC layout, automatically the commutation paths of S_{23} and S_{31} are degraded. A careful PCB layout is therefore essential for a successful implementation of a Δ-switch rectifier system.

Fig. 6.54(a) shows the measured system behavior in case of a single phase loss at $P_o = 2.25\,\text{kW}$ and $f_N = 400\,\text{Hz}$. Input phase L_1 is therefore disconnected from its power source. In agreement with

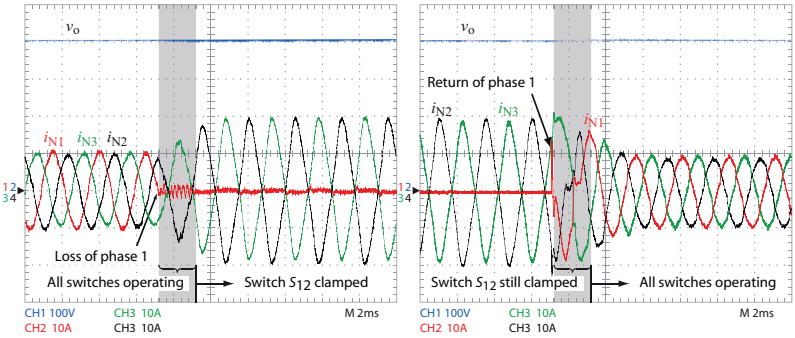
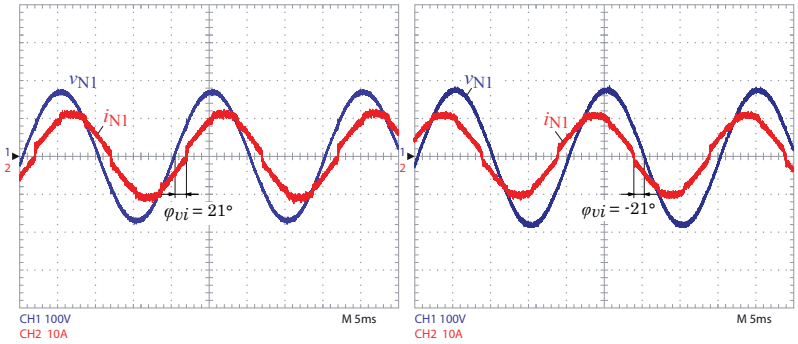


Fig. 6.54: Measured response of the rectifier system on a loss of phase L_1; Parameters: $P_o = 2.25\,\text{kW}$ and $f_N = 400\,\text{Hz}$; (a) Measured inductor currents i_{Ni} and output voltage v_o at loss of one phase and (b) return of the phase voltage.

the simulation results given in **Fig. 6.13** the system further operates in two phase mode without any changes in the controller structure (cf. **Fig. 6.54(a)**). During two-phase operation a pulsating power flow from the mains to the rectifier output with a frequency of $2f_N$ occurs which results in a corresponding output voltage ripple. Note, that this voltage ripple cannot be seen in the measurement due to the large output capacitance (1.47 mF) and the unfavorable scaling of the output voltage. As already discussed in section 6.3.3 one switch has to be clamped during two-phase operation. The rms measurement of the phase voltage, which is already implemented for calculation of the required conductance G_e^*, is used for detection of the phase loss. In **Fig. 6.54(a)** the phase loss is detected approximately after half a period and switch S_{12} is subsequently clamped to permanent off-state. After this clamping action no oscillations occur. In theory a change of the controller structure is not necessary but in practice appearing current oscillations can be prevented if one of the remaining switches is clamped to permanent off state.

Fig. 6.54(b) shows the behavior of the rectifier system if phase L_1 is connected to the grid again. Due to the clamping action of S_{12} the rectifier system is not able to generate sinusoidal input currents (cf. gray shaded area in **Fig. 6.54(b)**) but the amplitude of the



(a) (b)

Fig. 6.55: Measured input current i_{N1} and input voltage v_{N1} if the phase current is phase shifted by the controller ($P_o = 2.5\,\text{kW}$ and $f_N = 400\,\text{Hz}$) for (a) lagging input current ($\varphi_{vi} = 21\,°$) and (b) leading input current ($\varphi_{vi} = -21\,°$).

currents is still limited. After approximately half a mains period the control system detects that the corresponding phase is up again and the clamped switch S_{12} is released. This confirms that the rectifier system is able to handle a single phase loss at a reduced power level.

The phase shift capability of the Δ-switch rectifier system has been tested and the results for $\varphi_{vi} = \pm 21\,°$ are depicted in **Fig. 6.55**. In contrast to the simulation results slightly increased input current distortions in the vicinity of the current zero crossings can be observed which results in a THD_I of 3.5 % instead of 2.8 % for operation without phase shift. Please note, that the input currents without phase-shift show similar distortions in the vicinity of the zero crossings as given in **Fig. 6.55**. The current distortions could, however, be reduced by application of the turn-off delay compensation as discussed in section 5.1.2. Due to the phase-shift, the actual line-to-line voltage available to generate the required current slope at near the zero crossing gets smaller which results in addition in increased zero crossing distortions called cusp-distortions (see also [167]). The measurement results of **Fig. 6.55**, however, clearly demonstrate the phase shift capability of the rectifier system.
In addition, it has been determined to what extend the phase shift capability can be used in practice to improve the power factor of the

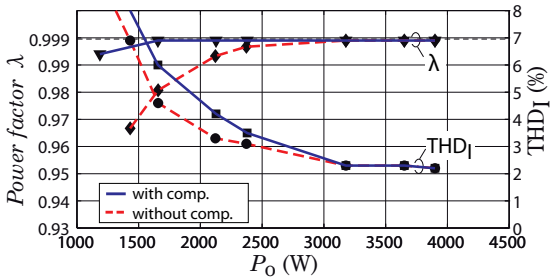


Fig. 6.56: Measured power factor and input current quality with and without enabled reactive power compensation by the rectifier system for $V_N = 115\,V$, $f_s = 72\,kHz$ and $f_N = 400\,Hz$.

rectifier system and the results are plotted in **Fig. 6.56**. The power factor can be improved considerably for partial load. Whereas without compensation the power factor already degrades for P_o below 2.5 kW, λ can be kept above 0.99 for $P_o > 1\,kW$. On the other hand, an increased THD_I can be measured caused by the phase shift action of the rectifier system. Below $P_o = 1\,kW$ the load current is too small to generate the required reactive power and the power factor drops very quickly accompanied by heavily distorted input currents. The phase shift capability of the Δ-switch rectifier system can therefore be used advantageously to improve the power factor for intermediate output power levels.

In order to get a basic idea of the conducted EMI emissions of the Δ-switch rectifier, initial EMI measurements were performed for an input frequency of $f_N = 50\,Hz$. For that purpose a standard LISN according to CISPR 16 ($50\,\mu H$, $50\,\Omega$) [138] was used. A three-phase DM/CM noise separator [251] was applied to measure the DM and CM noise separately. The measurements were done without a specific EMI filter, but to provide proper operation of the rectifier, capacitors of $3.4\,\mu F$ per phase have been placed at the rectifier input in star connection. In the airborne standard DO160F [31] emission limits for the noise currents are defined, but only noise voltage measurements have been performed. Under consideration of the frequency dependent impedance of the LISN the required current noise levels have been calculated using the measured noise voltages. The results of the

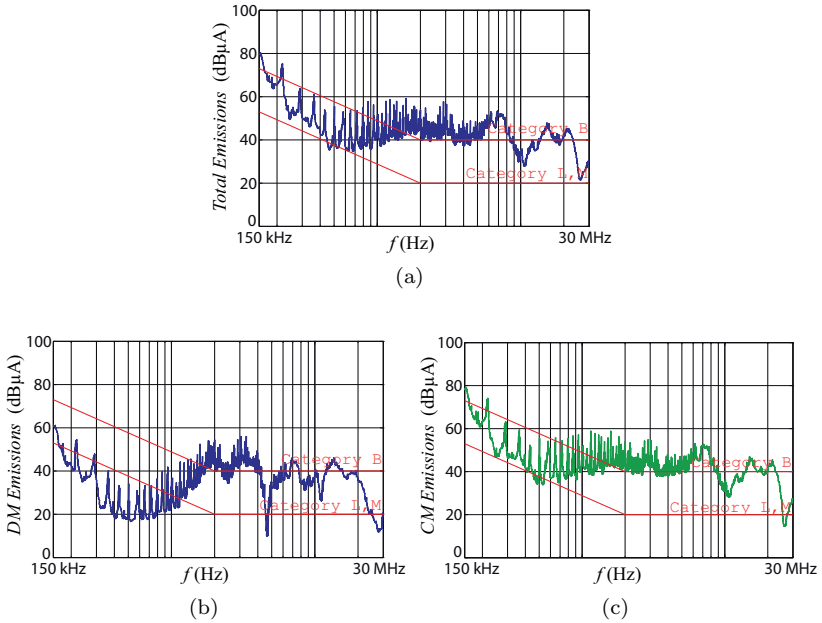


Fig. 6.57: Initial CE measurements of the rectifier system without EMI filter at $f_N = 50\,\text{Hz}$ using a standard LISN according to CISPR 16 ($50\,\mu\text{H}$, $50\,\Omega$); (a) Total conducted emissions, (b) DM emissions and (c) CM emissions.

peak-measurements and subsequent calculations for the frequency range $150\,\text{kHz} \ldots 30\,\text{MHz}$ are shown in **Fig. 6.57** together with the limits of the airborne standard DO160F (Category B and Category L,M,H). According to **Fig. 6.57**, CM emissions are the main noise components of the converter. A preferably accurate modeling of the parasitic CM paths and careful design of the CM filter stage is therefore essential and subject for further research. The total amount of input capacitors ($3.4\,\mu\text{F}$) would almost be sufficient for DM noise and this type of emissions can therefore be handled by a common multi-stage LC-filter.

TABLE 6.11: Power devices selected for power loss calculation of a Δ-switch rectifier system with $V_{\mathrm{N}} = 230\,\mathrm{V}$.

Part	**Device Description**
S_{ij}	IPW90R500C3 ($V_{\mathrm{DS}} = 900\,\mathrm{V}$, $R_{\mathrm{DSon}} = 0.5\,\Omega$)
$D_{\mathrm{n}i}$, $D_{\mathrm{p}i}$	IDH15S120 ($V_{\mathrm{RRM}} = 1200\,\mathrm{V}$, $I_{\mathrm{F}} = 15\,\mathrm{A}$)
Thy_{i}	TYN1012 ($V_{\mathrm{RRM}} = 1000\,\mathrm{V}$, $I_{\mathrm{F}} = 12\,\mathrm{A}$)
C_{o}	2 × 12 Nippon Chemicon KXG 82 µF/450 V
$L_{\mathrm{N}i}$	730 µH (2× E65 cores, material: Epcos N87, $N = 47$ turns)

6.6 Delta-Switch Rectifier for 230 V Mains Voltage

The 650 V-CoolMOS devices and 600 V-rectifier diodes used for the constructed prototype cannot be used anymore if the Δ-switch rectifier system shall be employed for future aircraft mains voltage of 230 V. One possibility is to use 1200 V-IGBTs and 1200 V-rectifier diodes but the switching behavior of the IGBTs and rectifier diodes does not allow a high switching frequency and a switching frequency in the range of 25 kHz has to be selected instead. This considerably increases the volume of the passive components such as boost inductors and EMI filter.
If the input voltage range is for instance limited to $230\,\mathrm{V} \pm 10\,\%$, recently developed CoolMOS devices with a breakdown voltage of 900 V can be applied in conjunction with 1200 V SiC-diodes. With this combination the switching frequency can be kept at 72 kHz or even raised to higher values. In order to demonstrate the capability of the Δ-switch rectifier topology for a mains voltage of 230 V and an output power of 10 kW the system losses and expected volumes of the main components are calculated according to 6.4.3. The intended components are listed in **TABLE 6.11** where also the main parameters are given.

The output voltage is chosen to be 650 V and according to (6.66) a boost inductor value of 720 µH is required if 20 % peak to peak current ripple is allowed. Two E65 cores with the material N87 from Epcos Inc. are assumed for implementation of the boost inductors where

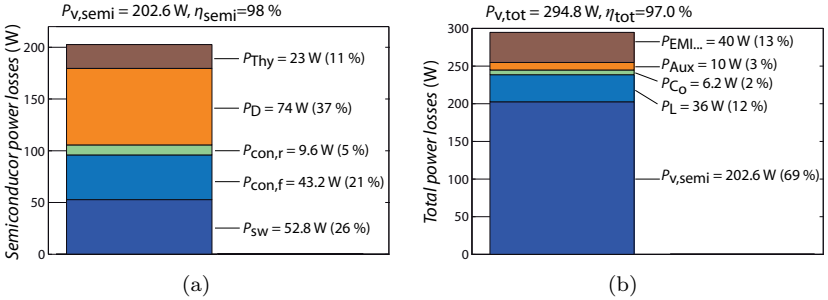


Fig. 6.58: Calculated power loss distribution of a 10 kW Δ-switch rectifier system for $V_N = 230$ V using 900 V CoolMOS devices and 1200 V SiC-diodes for $f_s = 72$ kHz.

$N = 47$ turns are required in order to prevent the core from saturation. Each inductor would show the dimensions $65 \times 65 \times 65\,\text{mm}^3$ which is significantly larger than the boost inductor required for a comparable three-level VR system (cf. VR72 in section 7). Two capacitor banks, each with $12 \times 82\,\mu\text{F}/450\,\text{V}$ electrolytic capacitors, are connected in series for implementation of the output capacitor C_o.

Fig. 6.58 illustrates the results of the loss calculation. The selected CoolMOS devices IPW90R500C3 show a relatively large R_{DSon} of 0.5 Ω which results, besides the large switching losses, in significant conduction losses. The switching losses are estimated using the switching loss measurements given in section 5.1.3. These switching loss measurements are performed for a drain source voltage of 400 V and have to be estimated for 650 V. In addition, the CP-series of the CoolMOS devices has been used which may show a different switching behavior than 900 V CoolMOS C3 devices. The estimated switching losses are therefore the biggest uncertainty of the loss calculation. Also the 1200 V SiC-diodes show, due to their large forward voltage drop, significant conduction losses.

Despite that, a semiconductor efficiency of 98 % is expected. In **Fig. 6.58(b)** the estimated total system losses including the losses of the main passive components are shown. The biggest part are the semiconductor power losses followed by the estimated losses in the boost inductor and the EMI filter. All together, a total system efficiency of 97 % can be expected which is quite good. The efficiency may, however, be reduced to lower values in case larger switching losses occur.

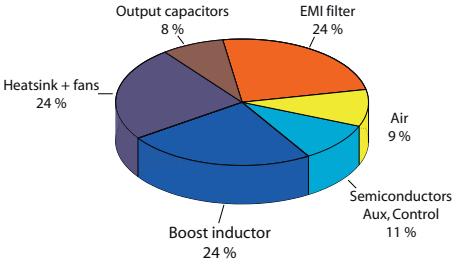


Fig. 6.59: Estimated volumes of the 10 kW Δ-switch rectifier system with $V_N = 230\,V$ and $f_s = 72\,kHz$.

TABLE 6.12: Specifications of the rectifier systems used for benchmarking.

Mains voltage (L-N):	$V_N = 230\,V \pm 10\,\%$
Mains frequency:	$f_N = 360\,Hz \ldots 800\,Hz$
Switching frequency:	$f_s = 72\,kHz$
Output voltage:	$V_o = 800\,V_{DC}$
Output power:	$P_o = 10\,kW$

Fig. 6.59 shows the estimated volumes of the intended 10 kW rectifier system. The volume occupied by the semiconductors, auxiliary power supply and gate drive units is assumed to be equal to the volume of the 5 kW rectifier system. The major increase in volume can be observed by the boost inductors which take now 24 % of the total volume. The boxed volume of the system would be $3.4\,dm^3$ which would result in a power density of $2.9\,kW/dm^3$. This power density only considers the boxed volumes and the corresponding air taken from the constructed 5 kW rectifier system without doing a construction or component arrangement. In a final implementation the power density may therefore slightly be reduced.

6.7 Comparison with the Vienna Rectifier

In the following the characteristics of the Δ-switch rectifier (cf. **Fig. 6.60(a)**) are benchmarked with the Vienna-type rectifier shown in **Fig. 6.60(b)**. Both systems require the same number of rectifier

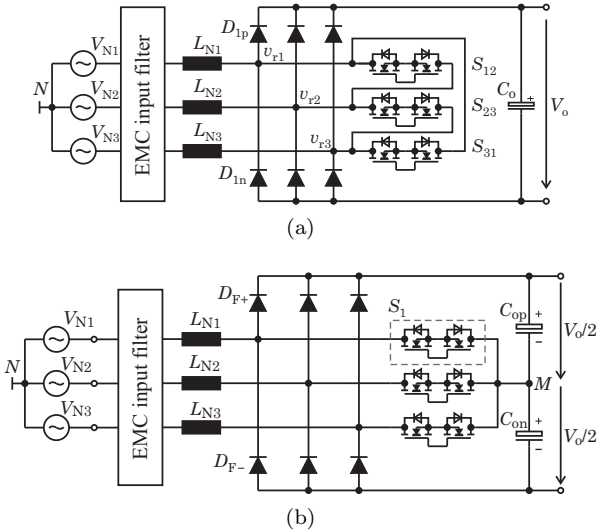


Fig. 6.60: Rectifier systems used for the comparative evaluation. (a) Two-level Δ-switch rectifier and (b) three-level VR structure.

diodes and bidirectional switches which are implemented by back-to-back connection of MOSFETs. The systems are designed to obtain the specifications listed in **TABLE 6.12**. A mains voltage level of 230 V is chosen as this might be the AC voltage level of future aircraft. All rectifier diodes have to be implemented by either by high-voltage ultrafast Si diodes or 1200 V SiC diodes. The switches of the Δ-switch rectifier system can be implemented using 900 V CoolMOS devices as discussed in section 6.6 or by recently released 1200 V SiC-MOSFET [78]. The switches of the VR on the other hand are only stressed with $V_o/2$ and 600 V CoolMOS devices can be used. Compared to the original VR structure shown in **Fig. 3.1(a)**, or the 6-switch version given in **Fig. 3.1(b)**, this implementation shows lower diode conduction losses as only one diode is now present in the free-wheeling path. These diodes must, however, exhibit a larger voltage blocking capability compared to the diodes in the VR structures shown in **Fig. 3.1**.

The benchmark can now be done using a detailed calculation of the power losses and specific volumes of the system elements as shown in [265, 45, 266, 267] and [47]. Detailed models of the rectifier systems

and time consuming calculations would therefore be necessary.
An easy and powerful topology evaluation method, only based on the component voltages and current average and rms values, has been proposed in [49]. No detailed calculation of the power losses is there required which makes it very interesting for a first, rough evaluation. Specific advantages of the rectifier topologies are not directly addressed by this approach and have to be considered in a more detailed evaluation.
In the following this approach will be used for the comparison of the two rectifier topologies and the performance indices derived in [49] will be modified to fulfill the requirements of unidirectional three-phase rectifier systems. The average and rms current stresses of the Δ-switch rectifier derived in section 6.4.2 and of the Vienna Rectifier system given in **TABLE 3.1** are used for the following calculation.

1) Transistors:
The relative transistor VA-rating

$$\text{Rel. Transistor VA-rating} = \frac{1}{\mu_\text{T}} = \frac{\sum_n V_{\text{DS,max},n} I_{\text{DS,max},n}}{P_\text{o}} \tag{6.89}$$

is the reciprocal of the transistor utilization μ_T defined in [49] where $V_{\text{DS,max}}$ and $I_{\text{DS,max}}$ are the maximum voltage/current values of the transistor occurring over a mains period. The maximum values do not have to appear simultaneously and the results of all switches are summed up. The VA-ratings are finally related to the nominal output power P_o. This performance index reflects the voltage/current stress of the switches and the smaller this index is the better.

The conduction losses of the switches are benchmarked using the sum of the transistors rms values

$$p_{\text{T,con}} = \frac{\sum_n I_{\text{DS,rms},n}}{I_\text{o}} \tag{6.90}$$

related to the load current I_o. One may claim that the squared rms currents would have to be summed in order to get a meaningful result. If, however, also the thermal interface of the semiconductor chips is considered (i.e. a larger chip area is provided for larger losses) a short calculation shows that the conduction losses are proportional to $I_{\text{DS,rms}}$

and not to $I^2_{\mathrm{DS,rms}}$.

Regarding switching losses the performance index

$$p_{\mathrm{T,sw}} = \frac{\sum_n I_{\mathrm{DS,avg},n} V_{\mathrm{DS,off}}}{P_{\mathrm{o}}} \tag{6.91}$$

can be calculated assuming a linear dependency of the switching losses on the switched current, where $V_{\mathrm{DS,off}}$ is the drain source voltage during the off-state. This approach can only be used if V_{DS} stays constant over the whole mains period which is true for the considered boost topologies.

2) Diodes:
As for the switches, a diode VA-rating

$$\text{Diode VA-rating} = \frac{1}{\mu_{\mathrm{D}}} = \frac{\sum_n V_{\mathrm{D,max},n} I_{\mathrm{D,max},n}}{P_{\mathrm{o}}} \tag{6.92}$$

can be calculated and a performance index for the diode conduction losses is defined by

$$p_{\mathrm{D}} = \frac{\sum_n I_{\mathrm{D,avg},n}}{I_{\mathrm{o}}} \tag{6.93}$$

using the average diode currents.

3) Passive Components:
The converter topology determines which passive components must be taken into account. While for a boost-type rectifier system the boost inductor and the output capacitor have to be selected, the input capacitor and the DC side inductor would have to be used for buck-type rectifier systems. Also different performance indices may be calculated for different topologies.
The boost inductor of the three-phase rectifier system can in a first step be described by the percentage reactance

$$p_{\mathrm{L,p}} = \frac{2\pi f_{\mathrm{N}} I_{\mathrm{N,rms}} L_{\mathrm{N}}}{V_{\mathrm{N,rms}}} \ . \tag{6.94}$$

Accordingly, a system requiring a larger inductor value, such as a two level system, shows a higher percentage reactance.

The stress on the output capacitor is modeled by a performance factor considering its current stress

$$p_{\mathrm{C}} = \frac{I_{\mathrm{C,rms}}}{I_{\mathrm{o}}} \tag{6.95}$$

which, considering data sheets, is related to a certain capacitance requirement.

3) EMI Filter:
The EMI filter requirements can be evaluated using the approach proposed in [240] which is used in section 5.7.2 to calculate the required attenuation of the CM filter stage. A computer simulation can be used to derive the DM and CM voltage waveforms of the rectifier systems. The DM and CM noise voltages are then calculated using the rms values of the simulated voltage waveforms $V_{\mathrm{DM,tot}}$ and $V_{\mathrm{CM,tot}}$

$$\begin{aligned} V_{\mathrm{DM}}^2 &= V_{\mathrm{DM,tot}}^2 - V_{\mathrm{N}}^2 \\ V_{\mathrm{CM}}^2 &= V_{\mathrm{CM,tot}}^2 - V_{\mathrm{CM,LF}}^2 \end{aligned} \tag{6.96}$$

where V_{N} is the mains voltage and $V_{\mathrm{CM,LF}}$ is the low frequency CM voltage, e.g. a third harmonic voltage signal used to increase the modulation range of the rectifier system.

The calculated performance indexes of the two rectifier systems are summarized in **TABLE 6.13**. In order to illustrate the performance of the system a radar chart of the performance indexes can be drawn (cf. **Fig. 6.61**). The particular performance indexes of an element (e.g. of transistors or diodes) are arranged together so that the performances of these elements can easily be compared. All plotted performance indexes are then connected which finally defines an area in the performance space. This is done for both systems and the system resulting in a smaller area, in a qualitative sense, shows a better performance. It has to be stated here that the total area may be a function of the arrangement of the individual performance indexes and that an appropriate arrangement could pretend a higher performance of one system. It is, however, a very powerful method to illustrate the performance of a system as all indexes can be observed at a first glance and as the specific performance indexes of two systems can directly be compared also detailed information of one system can be read from the diagram.

TABLE 6.13: Calculated performance indexes of the two rectifier circuits.

	Δ-switch rectifier	Vienna-type Rectifier
Num. of transistors	6	6
Num. of diodes	3	3
Trans. VA-rating (μ_{T}^{-1})	7.69	4.55
Trans. cond. losses $p_{\mathrm{T,con}}$	2.01	3.02
Trans. switch. losses $p_{\mathrm{T,sw}}$	1.41	0.7
Diode. VA-rating (μ_{D}^{-1})	8.85	8.85
Diode Cond. Losses $p_{\mathrm{D,con}}$	2	2
Percentage reactance $p_{\mathrm{L,p}}$	0.7	0.41
Cap. current stress p_{C}	0.4	0.4
DM Noise V_{DM}	165 dBµV	159 dBµV
CM Noise V_{CM}	159 dBµV	162 dBµV

The VR system shows a smaller transistor's VA-rating as the bidirectional switches are only stressed with half of the output voltage. This can also be seen in the switching losses as also there only the half output voltage has to be taken into account. The Δ-switch rectifier on the other hand shows smaller conduction losses as the Δ-connected switches are stressed with smaller currents. Both rectifier topologies show equal performance indexes for the diodes as they are stressed with the same current and voltage levels.
The percentage reactance of the Δ-switch rectifier is larger than the one of the VR as the VR system allows a smaller boost inductor due to the three-level topology. This is also visible in the smaller DM noise level of the three-level topology. The CM noise level of the Δ-switch rectifier system is, however, smaller than the noise level of the VR.

Overall, the VR shows a better performance than the Δ-switch rectifier system and is therefore the better choice for a mains voltage of 230 V. The Δ-switch rectifier shows, however, a slightly better efficiency than the VR system at equal size and power density for a mains voltage of 115 V and an output voltage of 400 V as shown in [268]. The Δ-switch rectifier is therefore the optimal choice for a mains voltage of 115 V and a corresponding output voltage of $V_{\mathrm{o}} = 400\,\mathrm{V}$.

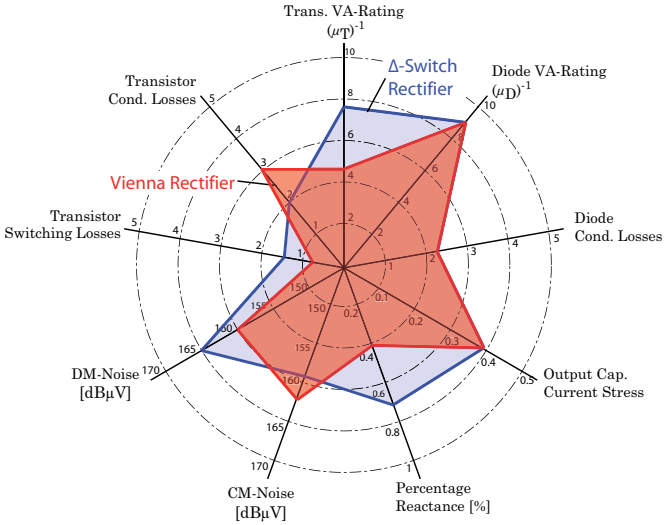


Fig. 6.61: Radar diagram illustrating the performances of the Δ-switch rectifier and of the VR.

6.8 Conclusion

In this section the three-phase Δ-switch rectifier circuit has been analyzed. Due to the high voltage stress of the Δ-connected switches, state-of-the-art SJ MOSFETs with a blocking voltage of 650 V cannot be used. The topology is, however, ideally suited for a mains voltage of 115 V. The required bidirectional switches are implemented using two back-to-back connected MOSFETs as there are no bidirectional switches commercially available. True bidirectional switches using the semiconductor material GaN have, however, been presented in research which would be ideally suited to reduce the conduction losses. Also recently released SiC MOSFETs with a blocking voltage of 1200 V would allow an operation of the Δ-switch rectifier at a mains voltage level of 230 V. As a calculation of semiconductor losses shows the Δ-switch rectifier performs well at $V_N = 230$ V if semiconductors with a higher blocking voltage are applied (e.g. 900 V CoolMOS devices or SiC MOSFETs). The main advantage of the topology is the reduced current stress of the Δ-connected switches.

A novel phase-related current control concept is proposed which continuously controls all phase currents and uses a pulse-width modulator. A proper implementation of the modulator yields to optimized switching sequences resulting in reduced conduction losses. The controller concept is easy to implement and only a simple clamping logic is required. In addition, the concept can handle a single phase loss without any changes in the controller structure. The rectifier system is able to operate with a phase displacement of $\pm 30\,\%$ which can be used advantageously to improve the power factor at partial load.
The implemented laboratory prototype with a power level of $5\,\mathrm{kW}$ shows a power density $2.35\,\mathrm{kW/dm^3}$ and a $\mathrm{THD_I}$ of $2.3\,\%$ is measured at $f_\mathrm{N} = 400\,\mathrm{Hz}$. As a detailed loss calculation shows, the measured efficiency of $\eta = 96.4\,\%$ can be improved considerably to $96.5\,\%$ by a more sophisticated design of the employed magnetics and by application of SiC diodes.

Chapter 7

Constructed Vienna Rectifier Systems

In chapter 5, an optimization regarding power density has been discussed for the VR topology where a maximum power density of $14.1\,\mathrm{kW/dm^3}$ has been achieved using a switching frequency of 1 MHz. The very high switching frequency, however, causes input current distortions and a relation between input current quality and efficiency has been derived. This finally yields to the η-$\mathrm{THD_I}$-Pareto Front (cf. **Fig. 5.50**) illustrating this limitation.
Another interesting relation exists between efficiency η and power density ρ and a η-ρ-Pareto Front can also be derived here. The derivation of such a η-ρ-Pareto Front is demonstrated in [133] for single-phase rectifier systems accompanied by measurements taken from constructed rectifier demonstrator systems. In order to calculate the η-ρ-Pareto Front for the discussed three-phase PFC rectifier systems a detailed model of the volume of the EMI filter would be required as the EMI filter, including boost inductors, takes approximately 60 % of the total volume in a power density optimized system (cf. **TABLE 5.20**). Such a model is given in [140] but, as shown in section 5.7, the calculated volumes are too optimistic and the given power densities cannot be achieved by a practical system. An enhanced model of the EMI filter volume would therefore be required which is, however, not derived in this work or a topic of further research.

7.1 Efficiency-Power Density Pareto Front

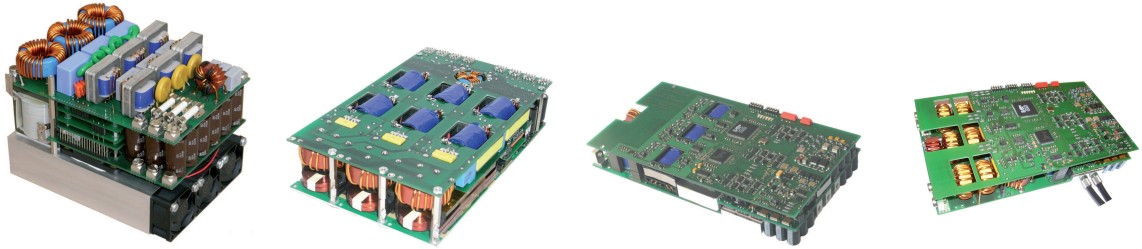
Another approach, based on constructed rectifier systems, will be presented here. Several VR systems with a power level of 10 kW and different switching frequencies between 72 kHz and 1 MHz have been built in the course of this work (cf. **TABLE 7.1**). This set of rectifier systems can be used to determine the η-ρ-Pareto Front. The derived curve is then based on real constructed systems and not on theoretical calculations which may differ from a practical implementation.

During the design of each considered rectifier system the focus was laid on a high power density and the component selection/arrangement was done according to this requirement.
The volume of the EMI filter, boost inductor, etc., can subsequently be analyzed using the data of the constructed systems which allows to give a statement on the achievable power density. The resulting power densities may, however, not be the highest possible values for the corresponding switching frequencies and topologies but could serve as basis for a first orientation.

An overview on the constructed rectifier systems is given in **TABLE 7.1**. The rectifier system VR72, with a switching frequency of 72 kHz, is rather a standard solution as used in industry today. The system is forced air cooled and shows a power density of 6 kW/dm^3 (without cooling system). Further details of this rectifier system can be found in appendix A. The rectifier system VR250, with a switching frequency of 250 kHz, and a power density of 10 kW/dm^3 and an efficiency of 96.7 % represents a good trade-off between power density and efficiency. It is therefore discussed below in more detail where also measurement results are given.
The rectifier system VR500, using $f_s = 500$ kHz, is water cooled and was a intermediate step during the exploration of the maximum possible power density. Further details on this rectifier can be found in appendix A as well. The constructed VR1000 rectifier system with $f_s = 1$ MHz has been discussed in detail in section 5.

A breakdown of the particular volumes of the rectifier systems is

TABLE 7.1: Constructed VR prototypes with an output power level of $P_o = 10\,\text{kW}$ using different switching frequencies.



VR72	**VR250**	**VR500**	**VR1000**
$f_s = 72\,\text{kHz}$	$f_s = 250\,\text{kHz}$	$f_s = 500\,\text{kHz}$	$f_s = 1\,\text{MHz}$
$\rho = 6\,\text{kW/dm}^3$	$\rho = 10\,\text{kW/dm}^3$	$\rho = 13.8\,\text{kW/dm}^3$	$\rho = 15.1\,\text{kW/dm}^3$
$\eta = 97.3\,\%$	$\eta = 96.7\,\%$	$\eta = 95.2\,\%$	$\eta = 93\,\%$

TABLE 7.2: Breakdown of particular volumes and calculated power densities of the constructed VR prototypes using either an optimized forced air cooling system with a $CSPI = 17.5\,\mathrm{K/(Wdm^3)}$ or water cooling.

	VR72	**VR250**	**VR500**	**VR1000**
Semicond.	$0.059\,\mathrm{dm^3}$	$0.042\,\mathrm{dm^3}$	$0.038\,\mathrm{dm^3}$	$0.038\,\mathrm{dm^3}$
Output cap.	$0.255\,\mathrm{dm^3}$	$0.174\,\mathrm{dm^3}$	$0.07\,\mathrm{dm^3}$	$0.07\,\mathrm{dm^3}$
Boost ind.	$0.285\,\mathrm{dm^3}$	$0.223\,\mathrm{dm^3}$	$0.117\,\mathrm{dm^3}$	$0.08\,\mathrm{dm^3}$
EMI filter	$0.612\,\mathrm{dm^3}$	$0.403\,\mathrm{dm^3}$	$0.345\,\mathrm{dm^3}$	$0.34\,\mathrm{dm^3}$
AUX	$0.104\,\mathrm{dm^3}$	$0.019\,\mathrm{dm^3}$	$0.053\,\mathrm{dm^3}$	$0.053\,\mathrm{dm^3}$
Gate drive	$0.074\,\mathrm{dm^3}$	$0.045\,\mathrm{dm^3}$	$0.047\,\mathrm{dm^3}$	$0.047\,\mathrm{dm^3}$
Control	$0.059\,\mathrm{dm^3}$	$0.053\,\mathrm{dm^3}$	$0.032\,\mathrm{dm^3}$	$0.032\,\mathrm{dm^3}$
Air	$0.22\,\mathrm{dm^3}$	$0.039\,\mathrm{dm^3}$	$0.021\,\mathrm{dm^3}$	$\approx 0\,\mathrm{dm^3}$
Total volume	$1.67\,\mathrm{dm^3}$	$0.998\,\mathrm{dm^3}$	$0.723\,\mathrm{dm^3}$	$0.66\,\mathrm{dm^3}$
Power density (No cooler)	$6\,\mathrm{kW/dm^3}$	$10\,\mathrm{kW/dm^3}$	$13.8\,\mathrm{kW/dm^3}$	$15.1\,\mathrm{kW/dm^3}$
Forced air cooling				
Heat sink	$0.32\,\mathrm{dm^3}$	$0.39\,\mathrm{dm^3}$	$0.58\,\mathrm{dm^3}$	$0.86\,\mathrm{dm^3}$
Tot. volume	$1.99\,\mathrm{dm^3}$	$1.38\,\mathrm{dm^3}$	$1.30\,\mathrm{dm^3}$	$1.52\,\mathrm{dm^3}$
Power density	$5\,\mathrm{kW/dm^3}$	$7.2\,\mathrm{kW/dm^3}$	$7.7\,\mathrm{kW/dm^3}$	$6.57\,\mathrm{kW/dm^3}$
Water cooling				
Heat sink	$0.092\,\mathrm{dm^3}$	$0.074\,\mathrm{dm^3}$	$0.046\,\mathrm{dm^3}$	$0.046\,\mathrm{dm^3}$
Tot. volume	$1.77\,\mathrm{dm^3}$	$1.07\,\mathrm{dm^3}$	$0.77\,\mathrm{dm^3}$	$0.71\,\mathrm{dm^3}$
Power density	$5.7\,\mathrm{kW/dm^3}$	$9.3\,\mathrm{kW/dm^3}$	$13\,\mathrm{kW/dm^3}$	$14.1\,\mathrm{kW/dm^3}$

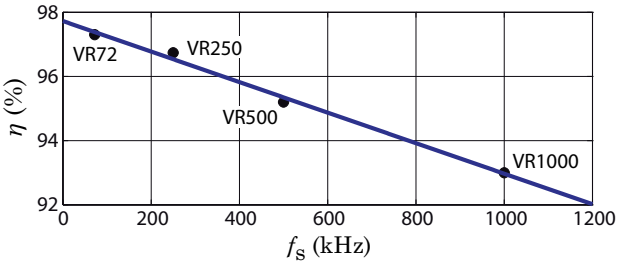


Fig. 7.1: Measured efficiency of the constructed rectifier systems as a function of switching frequency f_s.

given in **TABLE 7.2** where boxed volumes are used for the system elements. This means that all parts include some air in between the components. The volume contribution denominated as "Air" is the remaining space between the boxed volumes of the specific elements. The boxed volumes fit more or less "seamless" together for the VR1000 rectifier system and no "Air"-volume is therefore specified for this prototype.

The measured efficiencies of the single rectifier systems at $V_N = 230\,V$, $f_N = 50\,Hz$, $V_o = 800\,V$ and $P_o = 10\,kW$, are depicted in **Fig. 7.1**. The efficiency decreases roughly linearly with increasing switching frequency and an efficiency below 93 % can be observed for $f_s = 1\,MHz$ whereas an efficiency of 97.3 % is achieved for $f_s = 72\,kHz$. All systems use CoolMOS devices and the efficiencies are therefore comparable. The degradation of efficiency is a result of the switching losses which increase linearly with switching frequency. The extrapolated linear approximation shown in **Fig. 7.1** may be a too pessimistic estimation for low switching frequencies where the conduction losses exceed the switching losses. This is, however, not further discussed here.

The volumes of the corresponding boost inductors are given in **Fig. 7.2**. All inductors are designed for a peak current value of 27 A. According to **Fig. 7.2**, this volume decreases continuously for higher frequencies. A high-frequency material (Micrometals -8) must be used for a switching frequency of 1 MHz in order to avoid high core losses. Due to the considerably reduced permeability of this material (see also **Fig. 5.44**) the size of the inductor is bigger than the one of a system using a material with higher permeability. Another limitation can be

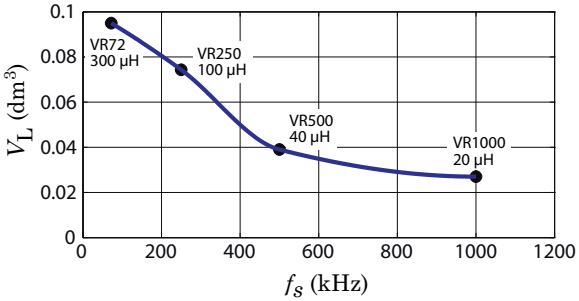


Fig. 7.2: Volumes of the constructed boost inductors for the implemented 10 kW rectifier systems.

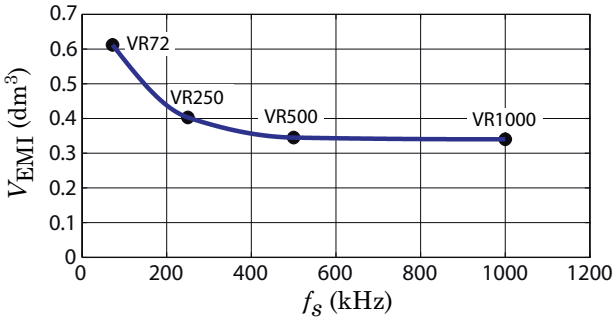


Fig. 7.3: EMI filter volumes of the implemented 10 kW rectifier systems as a function of switching frequency.

found in the minimum required copper area of the winding as the rms current of the inductor does not scale with switching frequency.

Next, the volumes of the EMI filters are inspected and the corresponding volumes are plotted in **Fig. 7.3** as a function of switching frequency. It is obvious, that an increase of switching frequency from 500 kHz to 1 MHz does not result in a significant volume reduction of the EMI filter. The reason can again be found on one hand in the lack of a suitable magnetic material. On the other hand, two small fans are inserted into the VR1000 rectifier system in order to improve the cooling of the inductors operating at their thermal limit. These fans consume the reduced space obtained by the increase of switching

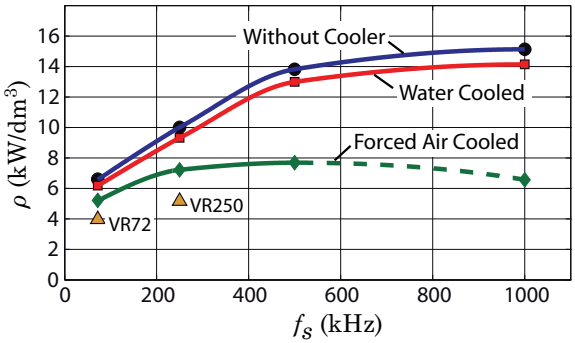


Fig. 7.4: Achieved power densities of the constructed rectifier systems without cooling. In addition the power densities are given if either a water cooler or a forced air cooler with a $CSPI$ of 17.5 K/(Wdm^3) is used for cooling.

frequency. An additional limitation is the lower emission limit of the EMI standard for high frequencies (see also **Fig. 1.8** or section 5.7) which requires a higher attenuation for a switching frequency of 500 kHz or 1 MHz.
An increase to such high switching frequencies is therefore, from the EMI filters point of view, not as beneficial as expected. If the emission limit of the EMI standard DO160D given in **Fig. 1.8** applies, a switching frequency below 666 kHz or below 500 kHz is recommended as then the third/forth switching frequency harmonic is still below the kink in the emission limit curve. Similar considerations apply for the emission limits of CISPR class A and class B. The switching frequency might there be chosen below 500 kHz in order to benefit from the higher emission limit of the EMI standard.

Using the volumes listed in **TABLE 7.2** the power densities of the rectifier systems can be calculated and the results are given in **Fig. 7.4**. The volumes of the heat sinks are not included in this power density. Two of the systems are forced air cooled (VR72 and VR250) and the other two systems use a water cooler (VR500 and VR1000). The volumes of the constructed systems are therefore not directly comparable. Due to the limited volume reduction of the EMI filter for switching frequencies above 500 kHz also the power density saturates. A maximal power density of 15.1 kW/dm^3 is achieved for $f_s = 1$ MHz if the heat sink is not considered.

A practical system, however, requires a heat sink and its volume must be included in the power density as the switching losses and therefore also the cooling demand increases with increasing switching frequency. The calculated power densities including a water cooler are plotted in **Fig. 7.4** as well. The designed water cooler discussed in section 5.3.3 is applied for the water cooled systems (VR500 and VR1000). A water cooler with a thickness of 11 mm and an area equivalent to the power module is assumed for the systems VR72 and VR250. Only a slight reduction of power density can be observed if a water cooler is attached. The VR1000 system then results in a remarkably high power density of 14.1 kW/dm^3 but it is worth noting that even for $f_s = 72$ kHz a power density of 6.5 kW/dm^3 can be achieved.

The question arises how the VR system performs if forced air cooling is used. According to [123] an optimized heat sink with a Cooling System Performance Index (CSPI) of $CSPI = 17.5\,\mathrm{K/(Wdm^3)}$ is assumed which is the practically achievable maximum value for an aluminum heat sink. Using

$$V_{\mathrm{hs}} = \frac{P_{\mathrm{o}}\left(\eta^{-1} - 1\right)}{CSPI} \frac{1}{(T_{\mathrm{s}} - T_{\mathrm{a}})} \tag{7.1}$$

where T_{s} is the temperature of the heat sink and T_{a} is the ambient temperature, the volume of the heat sink V_{hs} can be determined. A heat sink temperature of $T_{\mathrm{s}} = 75\,^{\circ}\mathrm{C}$ and an ambient temperature of $T_{\mathrm{a}} = 25\,^{\circ}\mathrm{C}$ are assumed and the total power densities including the heat sink are given in **Fig. 7.4**. The power density is now considerably reduced and a maximal value of 8 kW/dm^3 results for a switching frequency of 500 kHz. According to (7.1) a theoretical heat sink volume of 1.8 dm^3 would be required for $f_s = 1$ MHz in order to limit the heat sink temperature to $T_s = 75\,^{\circ}\mathrm{C}$ but then problems with heat spreading may occur. It has to be stated therefore that a switching frequency of 1 MHz cannot be implemented using forced air cooling. The power density curve is hence continued in **Fig. 7.4** with a dashed line to high frequencies in order to illustrate this limitation.
In addition, the power densities of the practically implemented air cooled rectifier systems VR72 and VR250 are shown (orange triangles). The cooling system of these rectifiers show a $CSPI$ below $17.5\,\mathrm{K/(Wdm^3)}$ and a reduced power density is therefore obtained.

If the power densities are plotted using a logarithmic scale for f_s (cf.

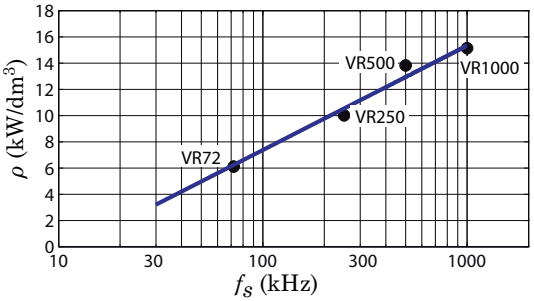


Fig. 7.5: Logarithmic plot of the power densities over switching frequency.

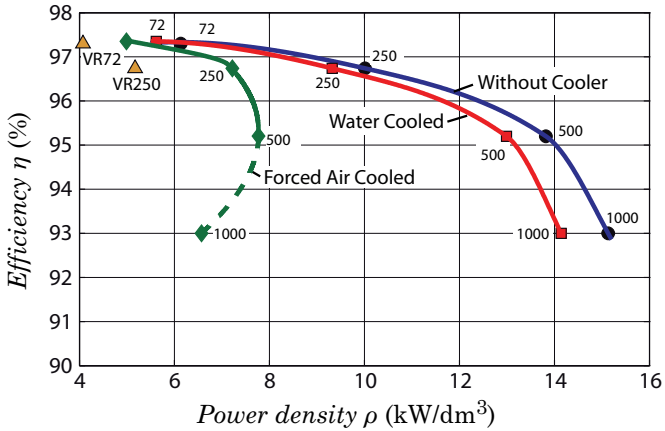


Fig. 7.6: Efficiency-Power density η-ρ-Pareto Fronts of the VR topology. Pareto Fronts without a cooler, using forced air cooling with $CSPI = 17.5\,\mathrm{K/(Wdm^3)}$ and using a properly designed water cooler are given. Switching frequencies (in kHz) are marked along the particular curves.

Fig. 7.5) the improvement of power density as a function of switching frequency can directly be read. A straight line is therefore fitted into the achieved power densities plotted in the logarithmic scale. According to **Fig. 7.5** the power density is improved by a factor of 1.88 (≈ 2) if the switching frequency is increased by a factor of 10.

The resulting η-ρ-Pareto Fronts are given in **Fig. 7.6** where corresponding switching frequencies (in kHz) are marked along the curves. The Pareto Fronts based on the systems without considering the heat

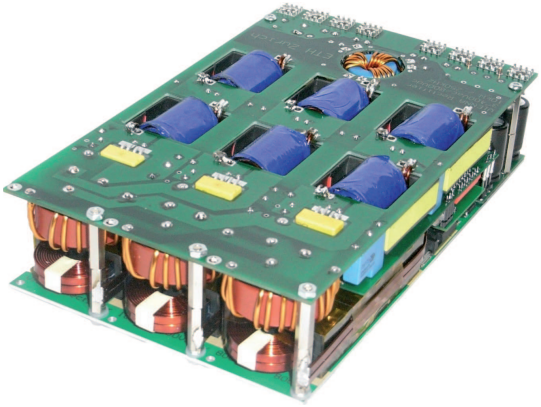
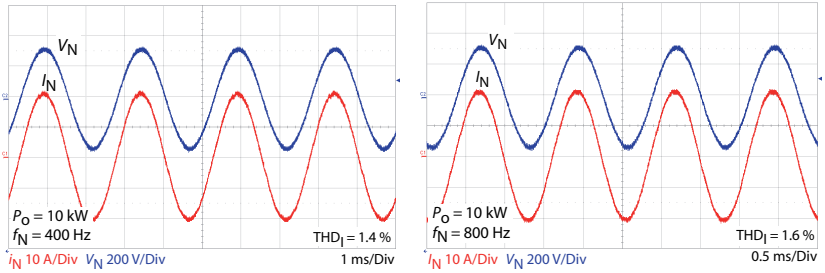


Fig. 7.7: Constructed VR prototype employing a switching frequency of 250 kHz. System dimensions: 195 mm × 120 mm × 42.7 mm.

sink and for the water cooled system shows a smooth degradation of efficiency with increasing power density for frequencies below 500 kHz. A severe drop in efficiency can be observed for switching frequencies beyond 500 kHz which is in agreement with the results given in **Fig. 7.4**. The Pareto Front, based on the forced air cooled systems shows a decreasing power density for switching frequencies above 500 kHz which indicates that an implementation of such a system makes no sense in practice.

According to **Fig. 7.6**, a water cooled rectifier system using a switching frequency of 250 kHz shows still a high efficiency of 96.7 % at a high power density of 9.3 kW/dm^3. Considering the outstanding input current quality in combination with the high efficiency and power density, a switching frequency of 250 kHz is therefore recommended for an implementation focused on high power density. The rectifier system VR250 is therefore discussed shortly below including measurement results at 50 Hz and 400/800 Hz confirming the very good performance.



(a) (b)

Fig. 7.8: Measured input currents taken from the constructed rectifier system VR250 at (a) $f_N = 400\,\text{Hz}$ (timebase: 1 ms/Div) and (b) $f_N = 800\,\text{Hz}$ (timebase: 0.5 ms/Div); $V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$, $P_o = 10\,\text{kW}$; I_N: 10 A/Div, V_N: 200 V/Div.

7.2 Vienna Rectifier System VR250

The constructed VR prototype with a switching frequency of 250 kHz is shown in **Fig. 7.7**. The rectifier system exhibits dimensions of 195 mm × 120 mm × 42.7 mm resulting in a power density of $\rho = 10\,\text{kW/dm}^3$ if the cooling system is not considered. Taking the non-optimized aluminum heat sink and fans of the implemented rectifier system into account, still a quite high power density of $5.7\,\text{kW/dm}^3$ is achieved (cf. **Fig. 7.4**). With a weight of only 2.7 kg the rectifier system exhibits a power to weight ratio of 3.37 kW/kg which is of high importance as the system is designed for aerospace applications. This means further, that all magnetic components are able to handle the main frequencies of 360 Hz-800 Hz. The system is fully digital controlled by use of a single FPGA from Lattice Inc. and offers several debug capabilities.

The measured input currents of the rectifier system operating at $f_N = 400/800\,\text{Hz}$ and $P_o = 10\,\text{kW}$ are given in **Fig. 7.8** ($V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$). The currents show an excellent sinusoidal shape, are in phase with the phase voltages and an incredibly low THD_I of 1.4 % is measured at 400 Hz which slightly increases to 1.6 % for $f_N = 800\,\text{Hz}$.

Fig. 7.9(a) shows the measured efficiency of the rectifier system operating with a mains frequency of 400 Hz and 800 Hz ($V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$) and in **Fig. 7.9(b)** the measured input current quality THD_I and power factor λ are given for these mains frequencies. The

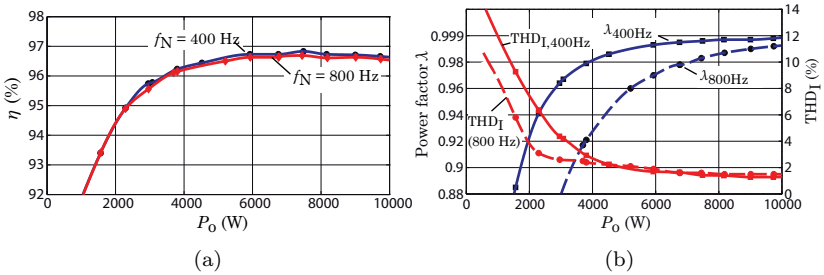


Fig. 7.9: (a) Measured efficiency and (b) measured power factor λ and input current quality THD_I of the built VR250 prototype at $f_N = 400/800$ Hz without compensation of the phase shift; ($V_N = 230$ V, $V_o = 800$ V).

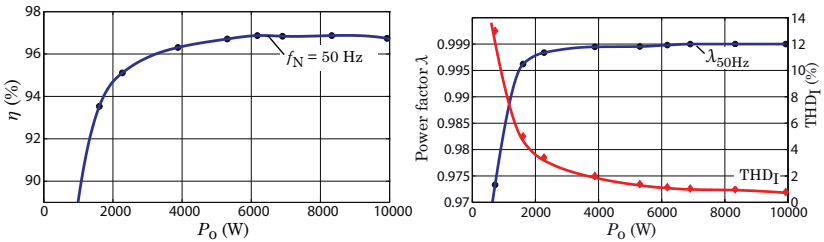


Fig. 7.10: (a) Measured efficiency and (b) measured power factor λ and input current quality THD_I of the built VR250 prototype at $f_N = 50$ Hz; ($V_N = 230$ V, $V_o = 800$ V).

THD_I value stays below 2 % for output power levels above 5 kW. The input current quality decreases for smaller output levels whereas the system shows better THD_I values for 800 Hz. This can be explained by the higher capacitive, sinusoidal currents drawn by the DM capacitors of the EMI filter. These capacitors, 2.35 µF in total, are on the other hand responsible for the reduced power factor, especially at $f_N = 800$ Hz. The power factor may be compensated in a limited range using the reactive power capability of the VR topology (cf. section 3.2.6).

The measured efficiency of the rectifier system at $f_N = 50$ Hz is

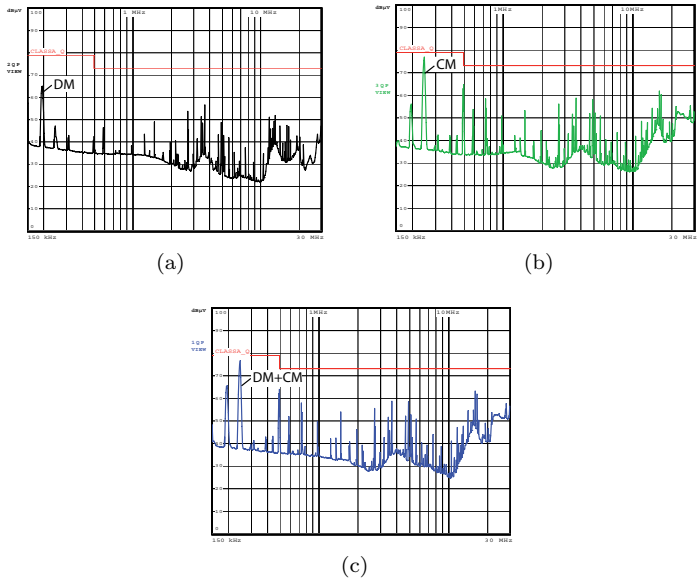


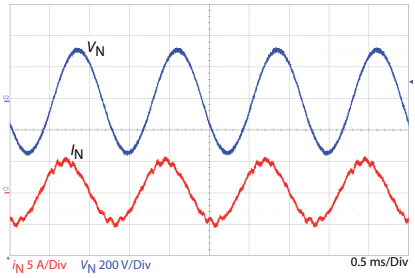
Fig. 7.11: Final QP CE measurements of the VR250 rectifier system as constructed; (a) DM emissions, (b) CM emissions and (c) total emissions.

depicted in **Fig. 7.10(a)** and the measured input current quality and power factor are given in **Fig. 7.10(b)**. In contrast to the measurement at $f_N = 800\,\text{Hz}$, the power factor stays above 0.99 for $P_o > 1.5\,\text{kW}$.

The results of a CE measurement are shown in **Fig. 7.11**. The DM emissions as well as the CM emissions stay well below the limit of CISPR class A which confirms the performance of the designed EMI filter. In order to fulfill the limits of CISPR class B an additional CM filter stage would be required as the noise peak at f_s exceeds the desired limit of CISPR class B (not shown in **Fig. 7.11**).

7.3 Stability Issues

During operation of the VR250 rectifier system with an active voltage source (linear power amplifier from Spitzenberger Inc.) at $f_N = 400\,\text{Hz}$ or 800 Hz, oscillations in the input currents are observed. A measure-



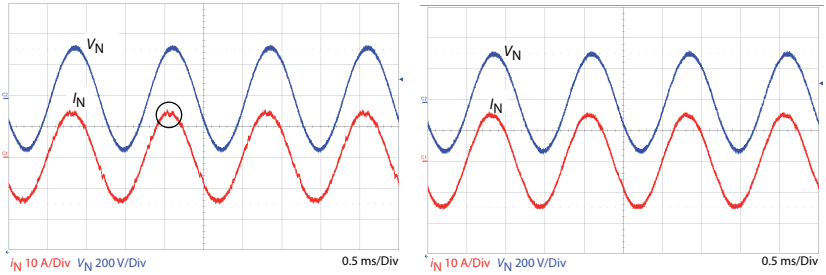
(a)

Fig. 7.12: Measured input currents taken from the constructed rectifier system VR250 at $f_N = 800\,\text{Hz}$, $V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$ and $P_o = 1.6\,\text{kW}$.

ment of the input current at $P_o = 1.6\,\text{kW}$ ($f_N = 800\,\text{Hz}$ $V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$) is shown in **Fig. 7.12**. The oscillations are excited at the zero-crossings of the two other phases and degrade the input current quality considerably. The origin of these unwanted oscillations has been found in interactions between the converter and the power source. Similar behavior has been observed in [269] for single-phase PFC rectifier systems and based on an analysis using the output impedance of the source and the input impedance of the single-phase rectifier system it is concluded that the lack of sufficient dynamic stability margin could be the origin of system harmonic currents. There, a simple RC-snubber circuit in parallel to the DM filter capacitor is proposed to attenuate the oscillations.
Three $1.5\,\Omega$ resistors are connected in series to the input terminals of the rectifier circuit for the case at hand and the measurement results with and without these resistors are given in **Fig. 7.13**.

The stability analysis of a single-phase PFC rectifier circuits in combination with various AC sources is discussed in [270] where also the impedances of the source and of the converter are used. Both systems use the impedance criterion published by Middlebrook [271] to determine stability. A review of other small signal methods is given in [272] and an input impedance analysis of single-phase rectifier circuits is given in [273].

Stability analysis of three-phase systems is, however, much more



(a) (b)

Fig. 7.13: Measured input currents taken from the constructed rectifier system VR250 at $f_N = 800\,\text{Hz}$, $V_N = 230\,\text{V}$, $V_o = 800\,\text{V}$ and $P_o = 10\,\text{kW}$. (a) Rectifier directly connected to the three-phase power source and (b) including three $1.5\,\Omega$ resistors for damping in series.

difficult as typically all three phases are coupled due to the missing connection to the star point of the rectifier system. It prevents the stability analysis using equivalent single-phase systems. In [274] an impedance criterion for three-phase rectifier circuits is derived which is based on a transformation into the dq-reference frame. Due to this transformation the time-varying AC voltages and AC currents are transferred into a constant operating point and the generalized Nyquist criterion can be applied to determine system stability. There, also simpler stability criteria based on matrix norms are given.

If the frequency of the occurring oscillation is below the upper bandwidth limit of the current controller the concept of a virtual resistor for attenuation of the oscillations can be applied as shown in [275, 276]. In [277] it is demonstrated that filter resonances can be shifted using the concept of a virtual impedance emulated by the control of the rectifier circuit.

All these methods for stability analysis or stability improvement of the complete system require a detailed knowledge of the impedance characteristics of the source as well as of the rectifier system. Measurement of the impedances, preferably in the dq-reference frame, is therefore essential. It has to be performed during operation of the rectifier circuit in order to consider nonlinear effects of the filter and of

the output impedance of the source. Three-phase impedance analyzers which are able to sustain the high mains voltages and with an upper bandwidth limit of approximately 100 kHz are required. Alternatively, injection methods as proposed in [278] can be used.
A detailed analysis of the stability condition of the discussed rectifier systems, including the calculation and measurement of the input impedance is, however, not performed in this work and is subject of further research.

Chapter 8

Conclusion and Future Work

Based on a survey on unidirectional three-phase rectifier systems two rectifier topologies, the two-level Δ-switch rectifier and the three-level Vienna Rectifier, are selected and analyzed with regard to aerospace applications. Especially the high mains frequency of 360 Hz ... 800 Hz and the tight requirements on input current quality are challenging for rectifier design. The operation principle of both rectifier systems is analyzed and detailed loss models are derived. Also the reactive power capability of the topologies is determined and it is shown how it can be used advantageously to improve the power factor of the system.
In aircraft applications, power density and weight are of high concern and a single-objective power density optimization of the VR topology is given. There, the switching frequency is raised to 1 MHz and finally a prototype with a power density of 14.1 kW/dm^3 (including water cooler) is built. Due to the high switching frequency several parasitic effects such as the turn-off delay or limited switching speed of the MOSFETs have to be considered. Those limitations are discussed in detail and a η-$\mathrm{THD_I}$-Pareto Front is derived which clearly illustrates the dependency between efficiency and input current quality. Despite these effects, still a good $\mathrm{THD_I}$ below 2 % can be measured. The derivations showed that the three-level three-phase VR topology is ideally suited for aerospace applications with a mains voltage of 230 V.

One limitation for increasing the switching frequency is the implementation of a symmetrical PWM. As shown in section 5.6, classical approaches based on the counter/comparator concept reach their limit at switching frequencies in the range of 500 kHz. The development of an external integrated PWM chip, which is able to generate symmetrical pulse patterns, would be required to overcome this limitation.

The two-level Δ-switch rectifier is well suited for applications with a mains voltage of 115 V. The proposed digital phase-oriented control concept shows good results and is able to handle a single phase loss without any changes in the controller structure. The constructed rectifier shows good input current quality and an efficiency of 94.5 % which can be improved to 96.5 % by a redesign of the magnetic components and by application of SiC diodes.

As shown in section 5.1, switching frequencies in the MHz-range require a very high switching speed. Unfortunately, this comes along with switching transient oscillations which reduce the efficiency of the rectifier circuit and worsen the EMI behavior. An active gate-drive stage (with a bandwidth of 100 MHz) would be able to prevent such oscillations by a control of the switching transient. A discrete implementation is, however, not possible for such high bandwidth. An integrated implementation could be possible and is subject of further research. A power module, integrating all semiconductors of the VR structure and active gate drive stages would thereto be required. Also some amount of DC-link capacitance could directly be included into this module in order to keep commutation loops as small as possible. In addition, similar damping approaches as proposed in section 5.2 could be applied in such a module.

In section 5.7, the EMI filter design of the VR topology is discussed where the appearance of mixed-mode noise is determined. This noise source and its influence on the EMI behavior of the rectifier system has to be analyzed in more detail. Also the existing noise current paths must be analyzed in more detail for a better understanding of the rectifiers' EMI behavior. This also applies to the Δ-switch rectifier as no dedicated EMI filter design is presented, neither in this work, nor in literature. In addition, it has to be clarified whether the artificial output voltage midpoint M can be connected to earth or not.

Based on the results given in [140], more detailed volume models of the EMI filter components must be derived under consideration of the limitations discussed in this work. This would allow to calculate the η-ρ-Pareto Front which is very useful for converter design. Also the concept of frequency dithering in order to reduce the EMI noise level should be tested.

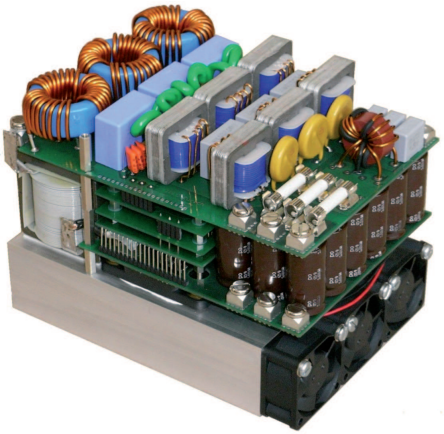
The recently released SiC MOSFET with high blocking voltages enable several new possibilities. The application of SiC MOSFETs with a blocking voltage of 1200 V allows to use the Δ-switch rectifier circuit also for a mains voltage of 230 V and initial calculations (cf. section 6.6) promise good results.
The application of high-voltage SiC diodes enables the implementation of a VR system according to **Fig. 6.60(b)** and a rough calculation certifies that an efficiency of nearly 99 % is possible.
The availability of a true monolithic bidirectional switch with high blocking voltage, as presented in [252], would allow to further increase the efficiency of the VR system as well as of the Δ-switch rectifier.

Next to the research demand on the discussed rectifier topologies, also the power supply structure of future aircraft requires further research. As discussed in section 7.3 interactions between the rectifier systems and the weak mains of an aircraft exist which may also worsen input current quality, especially for three-phase rectifier equipments connected to the mains. Stability criteria and design aids are required to support the system design. The measurement of the source output impedance and of the rectifier input impedance are thereto of high importance and equipment for measuring theses impedances during operation must be developed.

Appendix A

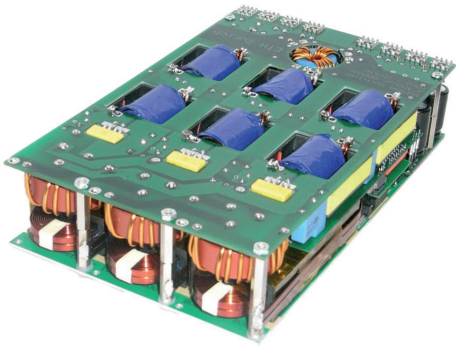
Constructed Rectifier Systems

Vienna Rectifier VR72



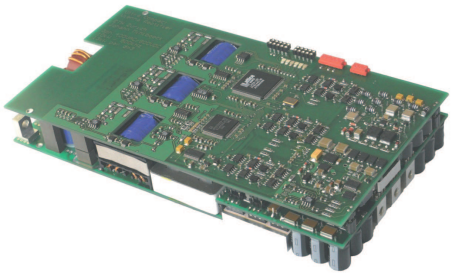
Input	
Input line-to-line voltage	320 V–520 V
Input current	23 A_{rms}
Mains frequency	50/60 Hz
Power factor ($>$ 25 % load)	> 0.99
Input current THD_I	< 3 % @ 50 Hz ($>$ 50 % load)
Output	
Rated output power ($P_{o,nom}$)	12 kW
Rated output voltage	800 V_{DC} ($\pm 400V$)
Output power in case of phase loss	57 % $P_{o,nom}$
Overvoltage protection	$\pm$450 V
Characteristics	
Dimensions	170 mm $\times$ 120 mm $\times$ 128 mm
Power density	5.7 kW/dm^3 with water cooler 4.6 kW/dm^3 with constr. forced air cooler
Weight	3.78 kg
Power to weight ratio	3.17 kW/kg
Switching frequency	72 kHz
Cooling	forced air cooling
Controller	fully digital control (single DSP)

Vienna Rectifier VR250



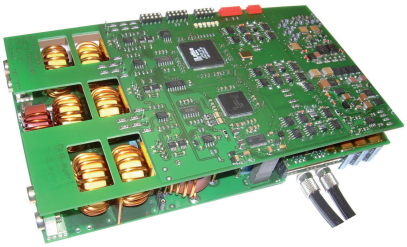
Input	
Input voltage (line-to-neutral)	$230\,\mathrm{V} \pm 10\,\%$
Input current	$20\,\mathrm{A_{rms}}$
Mains frequency	$50/60\,\mathrm{Hz}$, $360\,\mathrm{Hz} \ldots 800\,\mathrm{Hz}$
Power factor ($> 25\,\%$ load)	> 0.99
Input current $\mathrm{THD_I}$	$< 2.5\,\%$ @ $800\,\mathrm{Hz}$ ($> 50\,\%$ load)
	$< 2\,\%$ @ $800\,\mathrm{Hz}$ (full load)
Output	
Rated output power ($P_{\mathrm{o,nom}}$)	$10\,\mathrm{kW}$
Rated output voltage	$800\,\mathrm{V_{DC}}$ ($\pm 400V$)
Output power in case of phase loss	$57\,\%$ $P_{\mathrm{o,nom}}$
Overvoltage protection	$\pm 450\,\mathrm{V}$
Characteristics	
Dimensions	$195\,\mathrm{mm} \times 120\,\mathrm{mm} \times 42.7\,\mathrm{mm}$
Power density	$9.3\,\mathrm{kW/dm^3}$ with water cooler
	$7.2\,\mathrm{kW/dm^3}$ with forced air cooler
Weight	$3.37\,\mathrm{kg}$
Power to weight ratio	$2.97\,\mathrm{kW/kg}$
Switching frequency	$250\,\mathrm{kHz}$
Cooling	forced air cooling
Controller	fully digital control (single FPGA)

Vienna Rectifier VR500



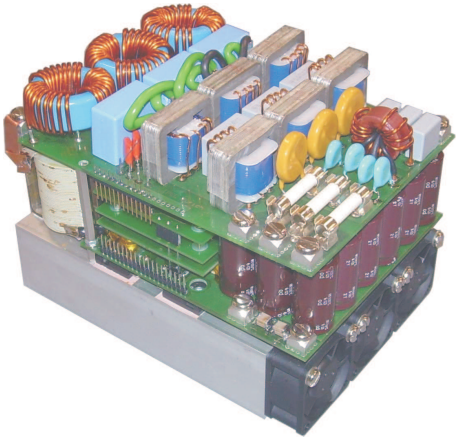
Input	
Input line-to-line voltage	320 V–520 V
Input current	20 A_{rms}
Mains frequency	50/60 Hz, (360 Hz − 800 Hz)
Power factor (> 25 % load)	> 0.99
Input current THD_I	< 2 % @ 50 Hz (> 50 % load) < 3.5 % @ 800 Hz(> 50 % load)
Output	
Rated output power ($P_{o,nom}$)	10 kW
Rated output voltage	800 V_{DC} ($\pm 400V$)
Output power in case of phase loss	57 % $P_{o,nom}$
Overvoltage protection	±450 V
Characteristics	
Dimensions	212 mm × 110 mm × 33 mm
Power density	13 kW/dm^3 with water cooler 7.7 kW/dm^3 with forced air cooler (CSPI=17.5 K/Wdm^3)
Weight	1.48 kg
Power to weight ratio	6.75 kW/kg
Switching frequency	500 kHz
Cooling	water cooled
Controller	fully digital control

Vienna Rectifier VR1000



Input	
Input line-to-line voltage	320 V–520 V
Input current	20 A_{rms}
Mains frequency	50/60 Hz
Power factor ($>$ 25 % load)	> 0.99
Input current THD_I	< 3 % @ 50 Hz ($>$ 50 % load) < 2 % @ 50 Hz (full load)
Output	
Rated output power ($P_{o,nom}$)	10 kW
Rated output voltage	800 V_{DC} ($\pm 400V$)
Output power in case of phase loss	57 % $P_{o,nom}$
Overvoltage protection	$\pm$450 V
Characteristics	
Dimensions	195 mm $\times$ 110 mm $\times$ 33 mm
Power density	14.1 kW/dm^3 with water cooler
Weight	1.06 kg
Power to weight ratio	9.44 kW/kg
Switching frequency	1 MHz
Cooling	water cooled
Controller	fully digital control

△-Switch Rectifier DS72



Input	
Input line-to-neutral voltage	$115\,\mathrm{V} \pm 10\,\%$
Input current	$20\,\mathrm{A_{rms}}$
Mains frequency	50/60 Hz, 360 Hz . . . 800 Hz
Power factor ($> 50\,\%$ load)	> 0.99 @ 400 Hz
Input current $\mathrm{THD_I}$	$< 4\,\%$ @ 400 Hz ($> 2\,\mathrm{kW}$)
	$< 2.5\,\%$ @ 400 Hz (full load)
Output	
Rated output power ($P_{\mathrm{o,nom}}$)	5 kW
Rated output voltage	$400\,\mathrm{V_{DC}}$
Output power in case of phase loss	$57\,\%\ P_{\mathrm{o,nom}}$
Overvoltage protection	$\pm 450\,\mathrm{V}$
Characteristics	
Dimensions	$170\,\mathrm{mm} \times 120\,\mathrm{mm} \times 128\,\mathrm{mm}$
Power density	$2.83\,\mathrm{kW/dm^3}$ with water cooler
	$1.91\,\mathrm{kW/dm^3}$ with constr. forced air cooler
Weight	3.78 kg
Power to weight ratio	1.32 kW/kg
Switching frequency	72 MHz
Cooling	forced air cooled
Controller	fully digital control (single DSP)

Appendix B

Notation

Abbreviations

ADC	Analog to Digital Converter
APU	Auxiliary Power Unit
ATU	Auto Transformer Unit
BEHA	Backup Electro Hydraulic Actuator
CISPR	Comité International Spécial des Perturbations Radioélectriques
CLBBC	Current DC-Link Back-to-Back Converter
CM	Common Mode
CMOS	Complementary Metal Oxide Semiconductor
CSPI	Cooling System Performance Index
CT	Current Transformer
DC	Direct Current
DCM	Discontinuous Mode of Operation
DDR	Double Data Rate
DHC	Decoupled Hysteresis Control
DM	Differential Mode
DPWM	Digital Pulse Width Modulator
DSP	Digital Signal Processor
DUT	Device Under Test
ECPE	European Center for Power Electronics
EHA	Electro Hydraulic Actuator

EMA	Electro Mechanical Actuator
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FBW	Fly-by-Wire
FEM	Finite Element Method
FOM	Figure-of-Merit
FPGA	Field Programmable Gate Array
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HF	High Frequency
HV	High Voltage
HW	Hardware
IEEE	Institute of Electric and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IMC	Indirect Matrix Converter
I/O Pin	Input Output Pin
JFET	Junction Field Effect Transistor
LISN	Line Impedance Stabilization Network
LVDS	Low Voltage Differential Signaling
MC	Matrix Converter
MEA	More Electric Aircraft
MIMO	Multiple Input Multiple Output
MM	Mixed Mode Noise
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTBF	Mean Time Between Failure
NPC	Neutral Point Clamped
PCB	Printed Circuit Board
PEEC	Partial Element Equivalent Circuit
PI	Proportional Integral
PFC	Power Factor Correction
PK	Peak Detection
PSM	Permanent Synchronous Machine
PTC	Positive Temperature Coefficient
PV	Photovoltaic
PWM	Pulse Width Modulator(n)
QP	Quasi Peak Detektion
RMS	Root Mean Square
SRM	Switched Reluctance Machine
SVM	Space Vector Modulation

SiC	Silicon Carbide
SISO	Single Input Single Output
SCR	Silicon Controlled Rectifier
SMD	Surface Mounted Device
SJ	Super Junction
THD	Total Harmonic Distortion
TRU	Transformer Rectifier Unit
UVA	Unmanned Aerial Vehicles
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VLBBC	Voltage Link Back-to-Back Converter
VLSI	Very Large Scale System Integration
VR	Vienna Rectifier

Definitions

x, $x(t)$	Time-varying quantity or signal
$\hat{X}$	Peak value
X	DC component or RMS value for AC quantities
X_{avg}	Average value
$\boldsymbol{x}$	Single column vector
$\boldsymbol{X}$	Matrix
x^*	Reference value for x
$\underline{x}$	Space vector or Complex number $\underline{x} = \lvert\underline{x}\rvert e^{j\varphi_{\mathrm{x}}}$

Commonly used Variables

A_{DM}, A_{CM}	Required Attenuation of DM/CM filter
A_{Chip}	Chip area of MOSFET
A_{Cu}	Copper area of inductor wire
A_{Fe}	Equivalent area of magnetic core
a_{r}	Load unbalance factor
B_{sat}	Saturation flux density of magnetic core
C	Capacitor
C_{12}	Coupling capacitance between wiring layer and damping layer
C_{Bp}, C_{Bn}	Parasitic capacitance of busbar to earth
C_{CM}	Common mode filter capacitance
C_{D}	Parasitic capacitance from MOSFET drain to ground or to heat sink
C_{DM}	Differential mode filter capacitance
C_{DS}	Drain-Source capacitance of MOSFET
C_{E}	Lumped capacitance from M to earth
C_{FB}	Feedback capacitance of EMI filtering concept
C_{in}	Input capacitance of the boost-type test circuit
$C_{\mathrm{j,D}}$	Parasitic junction capacitance of diode
C_{L1}, C_{L2}	Parasitic layout capacitances
C_{o}	Output capacitance
C_{op}, C_{on}	Output capacitances

C_{oss}	Parasitic output capacitance of MOSFET
C^{*}_{oss}	Chip area dependent MOSFET output capacitance
C_{p}	Capacitance of termination network
C_{snub}	Snubber capacitance
C_{tot}	Total system costs
C_{w}	Parasitic capacitance of winding
$delay$	Turn-off delay of MOSFET
$del*$	Parameter to describe turn-off delay of MOSFET
D_{F}	Freewheeling diode
D_{M}	Diodes of the Vienna Rectifier connected to M
D_{N}	Diodes of the Vienna Rectifier connected the mains
$D_{1\mathrm{p}}$, $D_{1\mathrm{n}}$	Rectifier diodes
D_{pre}	Pre-charge diode for start-up
e	Control error of current control
$E_{400\mathrm{V}}$	Energy stored in the output cap. of MOSFET
E_{on}	Turn on switching energy
f_0	Natural frequency of LC-tank
$F_{\mathrm{d}}(s)$	Disturbance transfer function
f_{l}	Lower bandwidth limit of AC current sensor
f_{N}	Mains frequency
$F_{\mathrm{o}}(s)$	Open loop transfer function of current control loop
$F_{\mathrm{o,V}}(s)$	Open loop transfer function of voltage control loop
$F_{\mathrm{o,S}}(s)$	Open loop transfer function of voltage symmetry control loop
$F_{\mathrm{z}}(s)$	Disturbance transfer function of current control
f_{s}	Switching frequency
f_{sample}	Sampling frequency of AD converter
G_{e}	Conductance used to generate the ref. currents
g_{m}	Transconductance of MOSFET
$G(s)$	Transfer function of the converter model for the current controller
$G_{\mathrm{DM}}(s)$	Transfer function of DM EMI filter
$G_{\mathrm{PWM}}(s)$	Transfer function of PWM
$G_{\mathrm{V}}(s)$	Transfer function of the converter model for the voltage controller
h_3	third harmonic injection signal
$H_{\mathrm{load}}(s)$	Transfer function of the load
$I_{\mathrm{C_o}}$	Current in output capacitor
i_{D}	Current of rectifier diode

$I_{\mathrm{D_F}}$	Current of free-wheeling diode
$I_{\mathrm{D_M}}$	Current of diode connected to M
$I_{\mathrm{D_N}}$	Current of mains side diode
i_{DS}	Drain source current
i_{FF}	Feedforward signal to compensate turn-off delay of MOSFETs
i_{L}	Load current
i_{N}	Mains input current
$i_{\mathrm{N}\sim}$	High-frequency current ripple of i_{N}
$i_{\mathrm{N}}[n]$	Sample point n of i_{N}
$I_{\mathrm{N}}(n)$	n-th harmonic of I_{N}
i_{m}	Magnetizing current
i_{M}	Mid-point current
I_{S}	Current of switch
J	Current density
k	Defines amount of ripple current
	Design constants of multi-objective optimization
k_0,k_1,k_2	Parameters of curve fit for switching loss energies
$K_{\mathrm{I}}(s)$	Transfer function of current controller
K_{p}	Gain of the P+Lag controller
k_{p2}	Constant of model for voltage controller
$k_{\mathrm{p,v}}$	Proportional part of the PI-type voltage controller
$k_{\mathrm{I,v}}$	Integral part of the PI-type voltage controller
k_{PWM}	Gain of pulse-width modulator
$K_{\mathrm{S}}(s)$	Transfer function of output voltage sym. contr.
k_{s}	Constant of the model for output volt. sym. contr.
$K_{\mathrm{V}}(s)$	Transfer function of voltage controller
L	Inductor
L_1	Effective inductance of the commutation path
L_2	Inductance of the damping layer
L_{CM}	Inductor of common mode filter
L_{lk}	Leakage inductance
L_{D}	Parasitic inductance of diode and MOSFET
L_{DM}	Inductor of differential mode filter
L_{m}	Magnetizing inductance of a transformer
L_{M}	Inductance of the mains
L_{N}	Boost inductor
L_{S}	Parasitic source inductance of the MOSFET
L_{wire}	Parasitic inductance of the wiring

M	Modulation index
	Output voltage midpoint
M_{12}	Mutual inductance between commutation path and damping layer
M_3	Modulation index of third harmonic injection
$M_\mathrm{I}(s)$	Transfer function of current measurement
$M_\mathrm{V}(s)$	Transfer function of voltage measurement
$M_\mathrm{S}(s)$	Transfer function of volt. unbal. measurement
m_i	Modulation function
n	Harmonic order, sample instant
N	Neutral point
	Number of turns
P_CM	Power losses of CM inductor
$P_\mathrm{v,Cu}$	Inductor copper losses
P_con	Conduction losses
P_D	Conduction losses of a diode
P_DM	Power losses of DM inductor
P_EMI	Total power losses of EMI filter
P_FET	MOSFET power losses
$P_\mathrm{FET,con}$	MOSFET conduction losses
$P_\mathrm{FET,sw}$	MOSFET switching losses
P_G	Gate drive power losses
P_in	Input power
P_L	Feedforward of load condition
P_o	Output power
$P_\mathrm{o,nom}$	Nominal output power
$P_\mathrm{o,lim}$	Maximum possible output voltage
P_{Thy}	Conduction losses of thyristor
$P_\mathrm{v,core}$	Power losses of magnetic core
$P_\mathrm{v,L}$	Total inductor losses
$P_\mathrm{v,semi}$	Total semiconductor power losses
$P_\mathrm{v,tot}$	Total power losses
Q	Reactive power
Q_G	Gate charge of MOSFET
R	Resistor or resistive load
R_B	Burden resistor of AC current sensor
r_D	Differential resistor of diode or SCR
R_DSon	On-state resistor of MOSFET
R^*_DSon	Chip area dependent on-state res. of MOSFET

R_{LISN}	Equivalent resistance of the LISN
R_{p}	Resistor of termination network
R_{pre}	Pre-charge resistor for start-up
R_{sym}	Resistor used for balancing
R_{snub}	Snubber resistor
R_{th}	Thermal resistance
S	Sensitivity of AC current sensor
S_i	Switch
s_i	Switching state of switch S_i
S_{ij}	Δ-connected switches
s_{ij}	Switching state of Δ-connected switches
t	time
T_{a}	Ambient temperature
T_{s}	Switching period $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$
	Heat sink temperature
T_{D}, T_1	Parameters of P+Lag controller
$T_{\mathrm{I}}(s)$	Closed loop transf. function of current contr.
T_{j}	Junction temperature
T_{N}	Mains period
u	Transfer ratio of transformer
$V_{\mathrm{BR,SS}}$	Breakdown voltage of the MOSFET
V_{c}	Total volume of cooling system
v_{CM}	Total common mode noise voltage
$v_{\mathrm{CM,h3}}$	Third harmonic common mode noise voltage
$v_{\mathrm{CM},\sim}$	High-frequency common mode noise voltage
$v_{\mathrm{CM,p}}$	CM voltage of VR system for operation with phase displacement
v_{DM}	Differential mode noise voltage
$v_{\mathrm{DM,avg}}$	Low-frequency differential mode noise voltage
$v_{\mathrm{DM},\sim}$	High-frequency differential mode noise voltage
v_{DS}	Drain source current of MOSFET
V_{EMI}	Volume of EMI filter
V_{F}	Forward voltage drop of diode or SCR
V_{G}	Gate voltage
$V_{\mathrm{GS,th}}$	Threshold voltage of MOSFET
V_{L}	Volume of boost inductor
v_{N}	Mains voltage
$v_{\mathrm{N,p}}$	Phase shifted mains voltage
v_{M}	Output voltage unbalance

V_o	Output voltage
V_op, V_on	Pos. and neg. output voltages
v_r	Rectifier input voltage
$v_{\mathrm{r}i,\mathrm{M}}$	Noise voltage with respect to M
V_tot	Total volume of converter
W_tot	Total weight of converter
$\underline{Z}$	Impedance of the termination network of damping layer
$\underline{Z}_\mathrm{L}$	Impedance of CM inductor
Z_0	Characteristic impedance of LC tank
α	Parameter to describe turn-off delay of MOSFET
α_1, α_2	Parameters for curve fit on R_DSon
β_1, β_2	Parameters for curve fit on R_DSon
δ	Relative on time
$\delta_{(\mathrm{xxx})}$	Relative on time of switching state (xxx)
δ_{--}	Relative on-time of switching state giving a negative center point current
δ_{++}	Relative on-time of switching state giving a positive center point current
δ_ff	Feedforward signal of duty cycle
δ_res	Resulting duty cycle considering δ_ff
δ_z	Disturbance input of current control loop
$\Delta i_{\mathrm{L,pp}}$	Peak-to-peak current ripple of boost inductor
Δp	Pressure drop of water pump
ΔT	Temperature difference
Δv_N	Deviation of the input voltage feedforward
ΔV_o	Output voltage ripple
Δv_s	Voltage drop over
η	Efficiency
γ	Output power to unit weight ratio Parameter for curve fit on switching loss energies
λ	Power factor
μ	Permeability
φ_N	Phase angle of mains
$\varphi_{\underline{\mathrm{i}}_\mathrm{N}}$	Phase angle of current space vector $\underline{i}_\mathrm{N}$
φ_i	Phase angle of mains current
φ_v	Phase angle of mains voltage
φ_vi	Phase displacement between mains voltage and mains current

ρ	Power density
ρ_{--}	Distribution of switching states for balancing of v_{o}
σ	Relative costs
ω	Angular frequency.

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Curriculum Vitae

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