Doctoral Thesis

A self-alignment strategy for parallel C4 MEMS packaging

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A Self-Alignment Strategy for Parallel C4 MEMS Packaging

A dissertation submitted to
ETH ZÜRICH

for the degree of
Doctor of Sciences

presented by
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This dissertation includes material previously published in:


It also contains material submitted for publication:

Kurzfassung

Die Aufbau- und Verbindungstechnik (engl.: packaging) ist einer der Hauptkostenreiber bei der Herstellung elektro-mechanischer Mikrosysteme (MEMS). Derzeit werden MEMS Chips hauptsächlich mittels Drahtbondens (engl.: wire bonding) elektrisch mit dem Verdrahtungsträger verbunden. Im Rahmen dieser Dissertat

ion wurde eine auf Selbstausrichtung zurückgreifende Methode entwickelt, die es erlaubt, mit einem einzigen Manipulator gleichzeitig mehrere MEMS auf Verdrahtungsträgern aufzubringen, an diesen auszurichten und mit diesen zu kontaktieren. Der Prozess bietet hohen Durchsatz und exakte Ausrichtung und verursacht dabei geringe Kosten. Der controlled-collapse chip connection (C4) Flip Chip Prozess wurde den speziellen Bedürfnissen elektro-mechanischer Mikrosysteme angepasst. Indem ein relativ ungenauer Roboter mit von flüssigem Lot angetriebener Selbstausrichtung kombiniert wird, kann eine präzise Positionierung und Ausrichtung der MEMS Chips zu den Verdrahtungsträgern sichergestellt werden.


Die Hersteller mobiler Geräte werden weiterhin einen steigenden Bedarf an
Abstract

Packaging is one of the major cost drivers for microelectromechanical systems (MEMS). Currently, wire bonding is the dominant method for electrically connecting MEMS chips to substrates. A self-alignment method for packaging multiple MEMS at the same time while using a single manipulator has been developed. The process achieves high throughput and precise alignment at low cost. The controlled-collapse chip connection (C4) process has been adapted to the specific requirements of MEMS. The combination of coarse robotics and liquid solder self-alignment guarantees precise positioning and alignment of the individual MEMS chips to the respective substrates.

The new method has been implemented in a case study. In the study, force sensors are packaged. Precise angular alignment of the sensors is critical for receiving accurate measurements. Results of the application are presented. We analyze the alignment accuracy. Furthermore, a model describing the alignment dynamics has been developed. It takes liquid solder driven self-alignment peculiarities such as the wetting, oxides, oxide removal, and flux solvent evaporation into account.

The soldering process is driven by a newly developed Joule heater that is embedded into the substrate. The heater operates in a closed-loop temperature-controlled fashion. Without additional sensors the heater provides temperature feedback from within the substrate. Soldering temperatures are reached in as few as 5 s. We show that, using the tightly temperature-controlled heater, very short soldering times are feasible.

Major incentives to switch MEMS packaging to flip-chip technology can be expected by the continued drive of the mobile device industry to switch to ever decreasing package sizes. This work provides a low-cost method to do so. The technology also provides a viable high-throughput method for packing chips that have been singulated by etching.
Abbreviations

**ADC** analog-to-digital converter.

**C4** controlled-collapse chip connection.

**C4NP** C4 new process.

**CAD** computer-aided design.

**CMOS** complementary metal-oxide semiconductor.

**CSEM** *Centre Suisse d'Electronique et de Microtechnique* sA.

**CSP** chip-scale package.

**CTE** coefficient of thermal expansion.

**DC** direct current.

**DCA** direct chip attach.

**DNP** distance to the neutral point.

**DRIE** deep reactive-ion etching.

**EFD** *Engineered Fluid Dispensing Systems*.

**EMI** electromagnetic interference.

**FCOB** flip chip attached to organic board.

**FCOB** flip chip on board.

**FR-4** flame retardant 4.
**Abbreviations**

**GUI** graphical user interface.

**HYDROMEL** Hybrid ultra precision manufacturing process based on positional- and self-assembly for complex micro-products.

**IBM** International Business Machines.

**IC** integrated circuit.

**IMC** intermetallic compound.

**IP** internet protocol.

**IR** infrared.

**IRIS** Institute of Robotics and Intelligent Systems.

**KGD** known good die.

**LED** light-emitting diode.

**MCM** multi-chip module.

**MEMS** microelectromechanical system.

**MOEMS** micro-opto-electromechanical system.

**NTC** negative temperature coefficient.

**PADS** plasma-assisted dry soldering.

**PC** personal computer.

**PCB** printed circuit board.

**PCI** peripheral component interconnect.

**PFC** phase-fired controller.

**PID** proportional–integral–derivative.
**Abbreviations**

**PWM** pulse-width modulation.

**RAM** random-access memory.

**RF-MEMS** radio-frequency microelectromechanical system.

**RIE** reactive-ion etching.

**SDS** *Structure Diagnostic Solutions Ltd.*

**SEM** scanning-electron microscope.

**SIP** system in package.

**SLT** solid-logic technology.

**SMBUS** system-management bus.

**SMT** surface mount technology.

**SOI** silicon on isolator.

**TAB** tape-automated bonding.

**TCP** transmission control protocol.

**TCP/IP** transmission control protocol (TCP) over internet protocol (IP).

**TSV** through-silicon via.

**UBM** under-bump metallization.

**USB** universal serial bus.

**WAVE** wide-area vertical expansion.

**WLP** wafer-level packaging.
1 Introduction

The market for microelectromechanical systems (MEMS) continues to grow at a
tremendous rate. Devices such as inertia sensors, pico projectors, ink-jet printers,
digital microphones, and pressure sensors are used in an increasing number of
devices. Every modern car, smart phone, tablet, and notebook computer contains
several MEMS. The largest part of the costs generated by the production of these
devices originates from packaging. The process and technologies developed in this
work can help reduce these costs.

This is achieved by reducing the number of process steps, parallelizing the
process (i.e., packaging multiple MEMS simultaneously), and reducing the robotics
requirements and, therefore, machine costs. Extended exploitation of self alignment
plays a prominent role in enabling these optimizations.

Apart from streamlining the packaging of existing MEMS, the newly developed
assembly process has the potential to become the missing enabling technology for a
group of devices that, so far, are difficult or impossible to economically manufacture.

Motivation

The global MEMS market has reached a volume in excess of 10 billion US Dollars
in 2011. It is predicted to continue growing at a compound annual growth rate of
13 % over the coming years (see fig. 1.1; Yole, 2012). A large part (60 % to 80 %) of
the manufacturing cost of MEMS devices can be attributed to packaging (Lau et al.,
2009).

MEMS by definition contain mechanical structures that in some way need to
move to enable either sensing or actuation. Depending on the intended application
these devices can be fragile. Especially prior to packaging, the devices must be
handled with extreme care to avoid damage or destruction.

To increase packaging throughput in a serial process, the handling speed and
acceleration of the respective machines need to be increased. The fragile nature of
MEMS places a limit on this. The logical consequence is to manufacture multiple devices at the same time; either by using multiple machines or by using a technology that enables a single machine to handle multiple assemblies in parallel. The method proposed in this work does just that.

Bonding Technology

Traditionally solder-bump packaging approaches\(^1\) have only been attractive for high pin-count and for high-speed devices or when package size is a major concern. On the other hand wire bonding is chosen for low-pin-count devices. Because they generally feature a very low pin count, nearly all MEMS devices are connected using wire-bonding technologies. Furthermore, wire-bonded devices are more tolerant to mismatching thermal expansion of the involved materials. However, by relying on wire bonding, MEMS devices cannot take advantage of attractive solder-bumped flip-chip properties such as the free placement of connection pads resulting in excellent space utilization, shorter connections leading to better electrical performance and thermal dissipation, and the superfluity of a separate mechanical fixation.

The technology developed in the course of this thesis turns solder-bump bonding into an attractive alternative for low pin count applications such as MEMS. It does so by reducing equipment costs while at the same time significantly increasing

\(^1\) Because the chip needs to be turned upside-down in the process these approaches are often referred to as flip-chip bonding.
throughput. The bonding technology also removes the need to flip the chip that is traditionally required in solder-bump applications.

HYDROMEL Project

Large parts of this work were conducted at Centre Suisse d'Electronique et de Microtechnique SA (CSEM) in the scope of the HYDROMEL European project. In this project, several technologies combining classical robotics and self-assembly methods were developed and evaluated by approximately thirty participating companies and institutions. Five demonstrators were build to prove the feasibility of the developed technologies. The work leading to this thesis was at the heart of “Demonstrator 1”.

FemtoTools GmbH Force Sensor

The task of Demonstrator 1 was the optimization of the packaging of FemtoTools force sensors; in particular, the FT-S260 sensor was used as the testbed for the developed technology (see fig. 1.2). The packaging process was to be optimized

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2 The full name of the project is “Hybrid ultra precision manufacturing process based on positional- and self-assembly for complex micro-products”. For more details on HYDROMEL please refer to the project website at http://www.hydromel-project.eu/.
both in terms of yield and in terms of speed. Major constraints of this task were the fragile nature of the MEMS chip and the fact that the chip may not be brought into contact with fluids (e.g., for cleaning or handling).

Areas of Work

The planning, simulating, and, in particular, the implementation of the novel assembly method required work in diverse fields: electronic circuits were designed, simulated, laid out and manufactured; a robotic software stack was developed and programmed; mechanical components were designed and build; a graphical user interface was programmed; last but not least communication protocols were conceived to link the various peripheral components, the robotic system, and the main application and, thus, integrate all the different constituents of the system.

Contribution to the Field

Several contributions to the field of MEMS packaging have been achieved in the process of this work:

*Parallel c4 packaging method* This work presents a new method for packaging several MEMS devices simultaneously while aligning them independently. A means for packaging quickly and precisely at the same time has been developed. By lowering the precision requirements of the employed robotic actuators and by reducing the number of process steps involved, the entry cost for a MEMS packaging machine has been lowered substantially.

*Analysis of solder self-alignment dynamics* An extensive review of the liquid solder propelled self-alignment literature was conducted. Based on this review solder self-alignment specific properties are isolated. An adapted solder self-alignment model taking these factors into account was developed, implemented, and experimentally verified.

*Reach-through chip-handling system* Conventional flip-chip chip-handling designs require the MEMS chip to be contacted on both sides. A new method has
been developed that only contacts the mems chip from one side. This allows fragile structures to be spread over the complete untouched side.

Localized heating system  A temperature-controlled closed-loop heating system has been developed that can precisely and quickly heat specific parts of support substrates. In a parallel application, such as ours, each substrate’s temperature can be controlled individually.

Automated packaging of nonfixated chips  Completely separating the chips from the wafer in an etching process is of special interest to mems manufacturing. Common processes produce debris that can easily damage the mems or inhibit the motion of tiny structures. While regular electronic chips can easily be cleaned, mems chips cannot. Once they are contaminated by debris, they must generally be discarded. However, when the chips are completely separated from the wafer by an etched groove, their precise position is no longer defined. Owing to its misalignment tolerance, our parallel packaging method makes chip singulation by etching feasible.

Robot software stack  A modular real-time robot control software stack was developed. The software solely relies on open-source software and, thus, does not create license fee costs. Parts of the software are being integrated into the Linux kernel.

Structure of this Dissertation

The next chapter presents current mems packaging methods. Chapter 3 outlines the general working principle of the developed packaging method. Chapter 4 continues to describe the application of the method to the FemtoTools FT-S260 sensor. Following that, the components developed to enable the new packaging method are described in chapter 5. Of the components, special focus is put on the localized heating system. It is described and analyzed in detail in chapter 6. We model the self-alignment dynamics and compare the outcome of our simulation to experimental data in chapter 7. Results from testing of the assembled products are presented in chapter 8. Finally, in chapter 9, we summarize our findings and give an outlook on possible future research.
2 State of the Art

The research presented in this thesis touches several fields. This chapter provides an overview on the current state of the art in the core areas discussed. It starts by giving an overview on current MEMS packaging technologies. It concentrates on two bonding technologies also applied to integrated circuits (ICs).

The state of the art in solder-bump heaters will be given in chapter 6 where a novel heater is discussed. Similarly, the current literature on solder self-alignment will be discussed at the beginning of chapter 7.

2.1 MEMS Packaging

Microelectromechanical systems combine mechanical and electrical components in a space of a few cubic millimeters or less. Most MEMS can either be classified as a sensor or as an actuator. In the case of a MEMS actuator an electrical signal controls some form of actuation. In the case of a MEMS sensor a mechanical quantity is measured. Examples for MEMS actuators include ink-jet print heads or the digital micro mirrors devices used in light projectors. MEMS sensors include accelerometer, gyroscopes, pressure sensors, microphones, biological and chemical sensors. There are also devices that combine actuation and sensing such as the evolving field of MEMS oscillators.

Most MEMS have to interact with the environment in one way or another, many of them physically. This is in stark contrast to purely electronic devices where shielding the device from environmental influences normally is a prime objective. Even when a MEMS device does not need to physically interact with the environment, the package must not interfere with the mechanical action of the MEMS.

2.1.1 Components

MEMS devices are generally made from silicon, similar to the way ICs are manufactured. Multiple devices are made from a silicon wafer using a combination of


Table 2.1: Packaging hierarchy (Ulrich and Brown, 2006, p. 589; Lau, 2000a, fig. 1.1).

<table>
<thead>
<tr>
<th>Level</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>wires within the IC</td>
</tr>
<tr>
<td>1</td>
<td>IC package (single or multi-chip module)</td>
</tr>
<tr>
<td>2</td>
<td>printed circuit board (PCB)</td>
</tr>
<tr>
<td>3</td>
<td>interconnect between PCBs</td>
</tr>
</tbody>
</table>

deposition, photolithographical printing, etching, doping, and similar processes.

Depending on the device manufactured, the chip can either be directly attached to a printed circuit board (PCB) (see also section 2.3.7 on direct chip attach) or to a substrate that serves as an interposer between the printed circuit board and the MEMS chip. The connection between the chip and the interposer substrate is generally referred to as level 1 connection. The connection between the intermediate substrate and a printed circuit board is called level 2 connection (see table 2.1). Unless explicitly noted this work describes the connection the MEMS chip is directly involved in. If an intermediate substrate is involved this is a level 1 connection. If no interposer substrate is involved this is a level 2 connection.

Nomenclature

The nomenclature slightly varies in the literature. In this work, chip as well as device refer to the MEMS chip while final device and the assembly refer to the packaged device (including the substrate). Substrate generally refers to the object the chip is to be attached to. The land location is the place on the substrate, the chip is intended to be placed.

2.1.2 Package Functions

The major functions MEMS packaging must fulfill are:

1. Create electrical connections between the chip and the substrate. This is required for both providing power to the chip and interchanging signals.

2. Mechanically fixate the MEMS chip on the substrate.

3. Protect the MEMS chip from the environment. Depending on the application, the MEMS chip must even be hermetically sealed. However, nearly all
2.1 MEMS Packaging

MEMS applications require some form of physical interaction with the environment. Only in some applications (such as the widely used accelerometers and gyroscopes) can these interactions occur from within a completely sealed package. Due to the different forms of environment interactions required, packages are highly application specific. This is a major cost driver. (Baldwin and Higgins, 2004, p. 8.8)

4. Remove heat produced by the MEMS chip.

This work only deals with the first two of the above functions.¹

2.1.3 Preparation

Prior to packaging, the chips are singulated, that is separated from the wafer. This process is often referred to as dicing. It is typically achieved by sawing the wafer with diamond blades. During and after the cutting process the emerging chips are held in place by dicing tape (also called blue tape). The adhesion of the tape must be strong enough to hold the chips in place during the sawing operation. On the other hand it must allow the chips to be easily removed by the later handling operations. This is commonly achieved by modifying the dicing tape’s adhesion properties by exposing it to ultraviolet light.

MEMS

Contrary to regular ICs, the delicate moving structures of MEMS can be obstructed by sawing debris. This contamination would be impossible to remove in a later cleaning step. Liquid cleaning is generally not possible for MEMS as the liquids can cause the fine structures to stick together. Therefore, MEMS chips are encapsulated prior to dicing. The process is generally referred to as capping. Depending on how the final device must interact with the environment, the capping is permanent (typically another silicon wafer) or temporary (typically one or more layers of adhesive tape). Electrical connections through a permanent cap can, for example, be obtained by through-silicon vias (TSVs) (Kühne and Hierold, 2011). Independent of which method is used, when permanent capping is employed, major parts of

¹ Why this is the case will be elaborated in chapter 3.
packing are performed at the wafer level. This is closely related to \textit{wafer-level packaging} which is detailed below (section 2.1.6). Permanent capping often has the disadvantage of increased component height. This is a major concern for mobile applications. (Gilleo, 2005, ch. 4.2)

Other singulation methods have been developed for \textit{MEMS}. In Singh et al., 1999 the chips are etched free from the wafer except for a thin tether. During singulation the chip is pulled away and the tether is broken. The device used in chapter 4 is completely etched free from the wafer and, thereby, released onto a support structure. Using this method the exact position of the chips is no longer defined, however. (Sun, Fry, et al., 2005)

2.1.4 System in Package

In their quest for ever increasing package density and higher switching frequencies, manufacturers are moving to \textit{system-in-package (SiP)} technology where multiple chips and passive components are integrated in a single package. Compared to custom systems on a chip, SiP offers reduced design costs. The short connections between the chips guarantee excellent electrical performance. (Baldwin and Higgins, 2004)

Packages in which all components are placed on a single substrate are referred to as \textit{2D-SiP} while those in which the components are (also) stacked are often called \textit{3D-SiP}.

MEMS often require a driver chip and passive components. In these cases \textit{SiP} is an attractive packaging option. However, depending on the \textit{MEMS} production yield as well as the balance of costs between the \textit{MEMS} and the other components, costs are significantly increased by (unknowingly) packaging defective \textit{MEMS}.

2.1.5 Known Good Die

\textit{Known-good-die (KGD)} testing describes the process of testing a chip before it is packaged. This is particularly important for \textit{SiP} applications. It is obvious that a single broken part in a module renders the complete module useless (if it cannot be exchanged). Thus, the expected yield of the entire package ($Y_p$) of $n$ devices with
individual yield \((Y_i)\) is limited by:

\[
Y_p \leq \prod_{i=1}^{n} Y_i.
\] (2.1)

Similar effects come into play when the chips are directly attached to the circuit board (see section 2.3.7). (Lau, 1995, ch. 1)

Verification of MEMS is particularly difficult since it cannot solely rely on electrical testing.\(^2\) In the scope of the HYDROMEL project, a testing method for the FemtoTools force sensors and grippers was developed. It allows testing of the devices’ mechanical fitness while the devices are still contained in the wafer. (Beyeler, Muntwyler, and Nelson, 2010; M. Yang et al., 2010)

#### 2.1.6 Wafer-level Packaging

Normally devices are to a large degree packaged after they have been separated from the wafer. In contrast, when wafer-level packaging (WLP) is employed, most of the packaging occurs while the chips are still part of the wafer, i.e., are not yet singulated. At this point the dies are located at defined positions inside the wafer. Because of this, it is possible to package all devices contained in a wafer in parallel. The package consists of an interposer that redistributes the chip connections. Various technologies are used for the chip-to-package connections. The wafer-level-packaging implementations often provide features that guarantee compensation for the thermal expansion mismatch (see section 2.3.4, below) between the chip and the printed circuit board.

Device testing (see also section 2.1.5) and burn-in are typically also performed while the chips are still part of the wafer. WLP leads to package footprints that do not exceed the device size and, therefore, have the smallest possible dimensions. If the above features are taken advantage of, significant time and cost savings can be achieved. However, sufficient device yield is a precondition for WLP to be viable. (Baldwin and Higgins, 2004, ch. 8.7; Patterson, 2002; Lau, 2000a, ch. 10)

#### 2.1.7 Technologies

The technologies employed in MEMS packaging are largely adapted from the IC industry. This comes as no surprise because these technologies have been developed

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\(^2\) There are exceptions to this, such as RF-MEMS switches, oscillators, etc.
more than 50 years ago and have since then been refined and verified. They are
well understood and mastered by chip foundries. Furthermore, they have been
certified for various kinds of applications. In particular, the technologies used
for connecting the MEMS devices to the substrate are identical to those employed
in IC manufacturing. In fact, MEMS devices are often produced on depreciated
complementary metal-oxide semiconductor (CMOS) manufacturing equipment.

Currently, there are two dominant methods for electrically connecting a MEMS
chip to the substrate: wire bonding and flip-chip bonding. The two methods feature
different characteristics leading to different preferred applications. This will be
outlined in the following sections.

In the scope of the present work a new form of flip-chip bonding has been
developed. Still, since wire bonding is the prevailing technology and the employed
method for producing FemtoTools sensors, a short presentation of wire bonding
will be given below.

### 2.2 Wire Bonding

Wire bonding was developed at Bell Telephone Laboratories as a response to an urgent
need for connection techniques in the early years of semiconductor technology.
Anderson, Christensen, and Andreatch (1957) describe how, under the application
2.2 Wire Bonding

of heat, a wire is pressed onto a contact pad and a lasting connection is formed. Figure 2.1 depicts connections created using this method. The contact pad surfaces must be clean, but no solder or flux are involved in the process. The temperature remains below the melting point of wire and pad. The connection was termed thermocompression bond. Soon semi-automated machines were developed (Hoopes et al., 1960) and refined (Köllner et al., 1966, 1967).

The wire material is typically copper, gold, or aluminium. The relatively high temperatures in wire bonding cause gold-aluminium intermetallic compound formation. To lower the temperature, part of the required bonding energy is often supplied using ultrasonic agitation. However, not all materials can be ultrasonically bonded (Harman, 2010). Today, the common bonding mechanisms are: thermocompression, ultrasonic, and thermosonic, a combination of thermocompression and ultrasonic bonding. (Hsu and Clatterbaugh, 2004, p. 40)

Since the connections are individually placed, wire bonding offers maximum flexibility. It imposes virtually no tooling costs for different chip layouts. When chips are designed for wire bonding the pads are placed at the periphery of the chip to keep connections short. While it is possible to create multiple rows of wire bonds, their number is limited by the space required by the wires. Only a fraction of the chip area can be used for interconnect purposes.

2.2.1 Manual Wire Bonding

In an experimental environment, manual wire bonding is a viable solution for creating substrate-to-chip connections. It offers high flexibility at the cost of requiring continuous control by an operator. Manual wire bonding is also applied to devices with low lot sizes that feature a limited number of connections.

Electrical connections between the FemtoTools FT-5260’s chip and substrate were created in this way prior to this work. FemtoTools achieved a bonding speed of about 6 bonds per minute.

2.2.2 Automatic Wire Bonding

Automatic wire bonders can operate at impressive speeds. For example the Esec Wire Bonder 3200 is specified at 22 bonds per second (Esec, 2009). Obviously, this requires a detailed plan of the desired connections and the location of the
individual pads. Programming this plan only generates limited set-up costs. It is this adaptivity that one of the biggest advantages of the wire-bonding technology. Still, even with the speed of modern high-end wire-bonding machines, it is nearly impossible to beat the throughput of a parallel approach that can create several hundred or even thousands of connections simultaneously. Flip-chip bonding is such a process.

2.3 Flip-Chip Bonding

The term flip chip generally refers to bonding technologies where the chip’s contact pads are directly connected to a matching pattern of contact pads on the substrate (see fig. 2.2). The connection can be established by different means such as brazing, soldering, thermocompression or through the use of conducting adhesives. The process is referred to as flip chip because the chip is often required to be turned upside-down prior to the alignment of the contact pads (see fig. 2.2). All flip-chip technologies share certain features. These are:

- The same element is used to create both structural support and electrical connections.
- Flip-chip connections are very short and provide excellent electrical and thermal performance.
- Nearly all of the chip surface can be used for electrical connections.
- Due to parallelization effects, “flip-chip technology is cost effective if the pin count and density of the IC devices are high” (Lau, 2000a, p. 35).
In this work a new flip-chip method will be presented. Since it relies on the liquid solder surface forces to self-align substrate and chip, the method is limited to solder flip chip.

The following sections give an overview of existing flip-chip technologies. Technologies that do not relate to the new method will be largely omitted. This includes the complete field of flip chip using adhesives for bonding.\(^3\)

### 2.3.1 Beam-Lead Technology

According to Lau (ibid., foreword) flip chip has been used at Bell Laboratories since the 1950s. In 1964 *beam-lead technology* was presented at several conferences and later published by Bell Labs in Lepselter et al., 1965 and Lepselter, 1966. Beam-lead devices feature cantilevered leads that are used both for electrically and mechanically connecting the device to a substrate (see fig. 2.3).

The leads are created on the silicon wafer containing the individual chips using a combination of sputtering, electroforming, etching and back-sputtering techniques. Once the leads have been created, the silicon surrounding the devices is etched away. The individual chips are separated and the leads are now cantilevered beyond the chips. The chip–substrate connection is formed using for example thermocompression bonding or spilt-tip welding. (Kalberman, 1972; Lepselter, 1966; Lepselter et al., 1965)

Beam-lead technology does not require dicing of the individual chips. Also, since

---

\(^3\) Adhesives have a much lower surface tension than solders. Still, epoxy resin self-alignment has been demonstrated successfully (J.-M. Kim, Shin, and Fujimoto, 2004; J.-M. Kim, Yasuda, and Fujimoto, 2005). Nonetheless, the suitability of adhesives for the developed technology is limited.
the beam leads are cantilevered, alignment of chip and substrate is particularly straightforward. Beam-lead technology is also known as air-bridge technology.

2.3.2 Solid-Logic Technology

In 1964 IBM introduced the System/360. It used the novel solid-logic technology (SLT): several active and passive electronic components are placed into a single polymer-enclosed package forming small modules. Inside the module, copper spheres are attached to the contact pads of glass-encapsulated active components (e.g., diodes and transistors) using solder. All of the spheres are on the same surface of the individual devices. The devices are then placed onto a ceramic substrate featuring solder-tinned land patterns that match the position of the solder balls (see fig. 2.4). When the solder is reflowed the devices are both electrically and mechanically connected to the substrate. (Davis et al., 1964; Hymes, Sopher, and Totta, 1967; Totta and Sopher, 1969)

2.3.3 Controlled Collapse Chip Connection

Five years after Davis et al. published their work on solid-logic technology, IBM presented its work on controlled-collapse chip connections,\(^4\) or short c4, in L. F. Miller, 1969b: In contrast to solid-logic technology it does not require the use of metal spheres. Instead, the connection between the pads of the chip and the pads of the substrate are solely formed by solder. This change was necessary to enable the use of flip-chip technology with larger chip sizes.

The ductile all-solder connection is better suited to compensate thermal expand-

---

\(^4\) Originally the process was called controlled collapse reflow chip joining. Also, it is often referred to by the more general term solder-bump flip chip.
2.3 Flip-Chip Bonding

![Diagram](image)

**Figure 2.5:** Solder-bump flip-chip self-alignment. The substrate (green) is at the bottom, the chip (blue) above. In (a) the substrate is not yet wetted. In (b) it is wetted and the solder (red) exerts a force on the movable chip. The solder surface and wetting forces have aligned chip and substrate in (c). (Redrawn from Wale and Edge, 1990.)

...sion mismatch between chip and substrate (see section 2.3.4). The soft connections reduce strain and contact failures and help to compensate for nonplanar substrate surfaces. Increased connection height leads to increased flexibility and (up to a certain point) higher reliability (Goldmann, 1969).

Previously, in **SLT**, the copper spheres acted as spacers between substrate and chip. In the absence of these spacers the solder would naturally spread out as much as possible and the gap between chip and substrate could collapse. This in turn could lead to shorted contacts. **C4** uses nonwettable areas on the substrate and chip to limit the space the solder can extend to and, thus, makes the amount of collapse controllable. Different forms of substrate passivation have been developed. (L. F. Miller and Spielberger, 1968; L. F. Miller, 1969b)

To this day, **C4** and its derivatives are the dominant flip-chip processes.6

**Self-Alignment**

It is pointed out in the original paper, that **C4** provides self-alignment of chip and substrate (see fig. 2.5): “The devices are, to a large extend, self-aligning on the limited solder areas, so that when contact is made between a part of each solder pad on the device and on the land solder, the chip will float into the position during the reflow process. Considerable misalignment in chip placement registration can

---

5 This was especially the case for the thick-film substrates used early-on. (Koopman, 1989, p. 433)

6 Literature on early flip-chip bonding machines can be found in Butera, 1969; Lynch, Otten, and Wenskus, 1971; Meyen et al., 1979.
be tolerated in some geometries due to this correcting mechanism.” (L. F. Miller, 1969b, p. 244) This “reduces the need for complex joining equipment and can permit wider control tolerances than other known methods.” (ibid., p. 239) It must be noted however, that self-alignment is only possible if no part of the assembly setup interferes with it. Often the heating mechanism is the critical point here. Since c4s are reworkable, self-alignment can also be achieved after an initial bonding by reheating the assembly (Butera, 1969).

2.3.4 Thermal Expansion Mismatch

One of the great difficulties in flip chip is dealing with the differing thermal expansion of silicon chip and possible substrates. As the temperature varies the distance between the contact pads alters to a different degree depending on the coefficients of thermal expansion (CTEs) of the materials. This effect is referred to as thermal expansion mismatch. It has to be ensured that neither the chip, nor the substrate, nor the connection are damaged by the stress created by a mismatch in expansion. The bonding material has to absorb most of the arising stress that manifests as shear forces on the bonds.

The amount of shear strain ($\gamma$) is dependent on the distance to the neutral point (DNP, $x$). The neutral point does not move during expansion and is generally located at the center of the chip. Since chip and substrate remain mostly flat and parallel, the amount of shear strain is approximated by:

$$\gamma \approx \frac{x}{h} \cdot \Delta T \cdot (\alpha_{L,\text{sub}} - \alpha_{L,\text{chip}}),$$

with $h$ denoting the stand-off height (i.e., the distance between substrate and chip), $\Delta T$ denoting the change in temperature, and $\alpha_L$ representing the coefficients of thermal expansion. From the equation it is obvious that the shear strain increases with the distance from the center of the chip. It therefore limits the size of flip-chip devices. (Beckham et al., 1986)

Different methods were developed to reduce shear stress. Among them special techniques to extend the height of the connections beyond that of regular c4 (Koopman, 1989).
MEMS

While generally the stress on the bonds is the most relevant effect caused by thermal expansion mismatch, in MEMS, the shear forces can affect the system’s performance substantially. The forces acting upon the MEMS chip at the contact pads can cause parts of the chip to be slightly deflected. This in turn can impact the mechanical performance of the MEMS.

In fact, owing to the MEMS’ sensitivity, it is common practice to use epoxies engineered to have a modulus value below 1 GPa for die attachment.\(^7\) For cases where even less stress is required special no-stress silicone adhesives exist. These feature a modulus below 5 MPa. (Gilleo, 2005, pp. 71–72)

### 2.3.5 Organic Substrates

The choice of exploitable substrate materials is severely limited by the effects of thermal expansion mismatch. Originally, pressed alumina ceramic was used as the substrate material for C4 due to its CTE matching that of silicon much better than organic alternatives such as the flame retardant 4 (FR-4) grade glass reinforced epoxy commonly used for PCBs (see table 2.2). However, the ceramic’s relatively high costs motivated research to investigate other options. Greer (1979) looked into alternative organic substrates that have closely matching CTEs. However, in the long run underfill (see the following section) was employed to moderate the shear

---

\(^7\) This applies to the MEMS chip fixation when using wire bonding. It is mentioned here to highlight the importance of minimizing stress in MEMS application and the amount of effort that is put into achieving this goal.
stress affecting the solder connections.\footnote{Other methods for reducing shear stress in flip-chip bonding have been invented. For example, Chow et al. (2009) use microsprings to absorb the difference in expansion. However, so far using underfill is by far the dominant approach.} Through the use of underfill encapsulation and novel multilayer organic substrate manufacturing technologies IBM’s Yutaka Tsukada, Syuhei Tsuchida, and Mashimoto (1992) succeeded in reliable flip-chip assembly onto organic substrates in 1992 (see also Appelt et al., 1999). This led to major cost savings and the increased adoption of solder-bump flip chip (Lau, 2000a).

2.3.6 Underfill

Underfill is a resin that is deposited in between chip and substrate in a way that it surrounds some or all of the individual solder connections (see fig. 2.6).

When indium started to be used in C4 solder alloys (Goldmann et al., 1977; Howard, 1982), corrosion became an issue potentially impairing device lifetime. The solder connections, therefore, needed to be sealed from the environment. Underfill was developed to enclose the connections and protect them from environmental influence such as moisture (Angelo, Poliak, and Susko, 1980). Later it was also used as a barrier shield to keep alpha particles from inducing soft errors (May and Woods, 1978) in integrated circuits (Beckham et al., 1986).

Only when epoxy resins started to be used as underfill was it found to significantly reduce fatigue (Beckham et al., 1986; Nakano, Soga, and Amagi, 1987; Soga et al., 1989). It does so by preventing oxidation and reducing the shear stress (\(\tau\) the
bonds are exposed to

$$\tau = \tan(\gamma) \cdot G = \frac{F}{A}.$$  \hspace{1cm} (2.3)

The increase in the area ($A$) the shear forces ($F$) are acting upon results in reduced shear forces acting upon the solder connections. ($G$ denotes the material dependant shear modulus.) The low cTE of epoxy underfill is typically achieved by adding filler material. Inorganic filler material can provide lower $\alpha$-particle emissivity than silica fillers (D. W. Wang and Paphthomas, 1993). Yutaka Tsukada, Mashimoto, et al. (1992) point out that in the presence of underfill the modulus of the substrate plays an important role. The more elastic the substrate is, the more the substrate is bend and through this deformation takes away stress from the solder connections. A glass epoxy such as FR-4 which is commonly used for printed circuit boards features a Young’s modulus ($E$) of approximately 21 560 MPa. When used in a low temperature flip-chip process along with an epoxy underfill very reliable connections can be achieved.

In summary, underfill achieves three major improvements:

- Shielding of environmental influence to prevent corrosion, etc.
- Reduction of stress on the solder connection.
- Prevention of soft errors caused by $\alpha$-particles.

While the last point is not relevant to this work, the first two are. To achieve these goals Suryanarayana et al. (1990) list (among others) the following desired properties for the underfill material:

- The cTE should match the cTE for the z-expansion of the solder joint.
- The material should cure at low temperatures to avoid deformation.
- At the dispensing temperature, good flow and wetting are required.
- Chemical resistance to organic solvents.
- Low $\alpha$-particle emission.

It should be noted that the use of underfill removes an important $\mu$ property: the assembly cannot be reworked if (or after, depending on the method of application)
underfill has been applied. This potentially increases costs. When the fitness of the chips can only be ascertained after packaging (see section 2.1.5 on KGD), the impact is particularly high for multi-chip module (MCM) and SIP applications.

MEMS

The load on the solder connection caused by the differing thermal expansion of substrate and chip is reduced by the use of underfill. However, this is achieved by coupling the chip and substrate more closely. This results in a stronger deformation of the MEMS chip. As previously pointed out (in section 2.3.4) this can have a negative effect on the MEMS performance. There is another problematic aspect to the use of underfill with MEMS devices that are not encapsulated; care must be taken that the underfill does not inhibit the free motion of the mechanical structures inherent to MEMS.

Because of the rather small size (compared to regular ICs) of MEMS the connections’ distances to the neutral point (DNPs) are fairly limited. Since the stress induced by thermal expansion is approximately proportional to the individual connection’s DNP, this confines the ramification of thermal expansion mismatch. Furthermore, MEMS typically produce very little heat by themselves. Unless temperature fluctuations are introduced from the outside, the temperature is nearly stable.

2.3.7 Direct Chip Attach

When the chip is directly bonded to the circuit board (i.e., no level 1 connection is involved), it is referred to as direct chip attach (DCA), flip chip on board (FCOB) or, if the board is organic, flip chip attached to organic board (also FCOB). The elimination of the level 1 connection leads to improved electrical performance. DCA to organic boards such as the widely used FR-4 generally requires underfill to be employed. Directly attaching chips using the C4 process works in a similar manner as regular surface mount technology (SMT). Since rework of underfilled DCA is prohibitively expensive, known good die testing (section 2.1.5) is essential for direct chip attach. The small pitch of the pads puts high demands on the (typically organic) substrate. (DeHaven and Dietz, 1994; Greer, 1996; Lau, 2000a, ch. 5–9)
2.3.8 Tape-Automated Bonding

*Tape-automated bonding (TAB)* is a technology quite similar to beam-lead technology. It is currently popular for high-volume devices. A flexible dielectric tape carrier is acting as an interposer. From the tape, cantilevered leads are connected to the chip either using individual bonding\(^9\) or gang bonding. The other end of the leads is then connected to the metallurgical contact pads of the package. In some applications the dielectric tape is equipped with contact pads for the *level 2* connection itself.\(^{10}\) The actual bonding method used for the tape–chip connection often is not solder based but some form of ultrasonic or thermosonic bonding. (Gilleo, 2005, ch. 4.7)

Due to the flexibility of the tape, *TAB* is nearly unaffected by thermal expansion mismatch.

2.3.9 Chip-Scale Package

 Packages are called a *chip-scale package (CSP)* when their size does not exceed around 1.2 times the size of the chip they contain. The small dimension of the package reduces the exposure to thermal expansion mismatch. (Baldwin and Higgins, 2004, p. 8.4–8.5)

2.4 Parallel Assembly

When looking at *parallel assembly* it quickly becomes clear that there are at least two kinds: parallel assembly of *coupled* parts and parallel assembly of *independent*, more or less free-standing parts.

2.4.1 Parallel Assembly of Coupled Parts

What has been described in this chapter so far clearly falls into the first category. Let us define a parallel assembly as one where in a *single* process, with a *single* setup, *multiple* analogue results are produced (nearly) *simultaneously*, here. Clearly

\(^9\) In which case it is, contrary to nearly every other flip-chip process, not a parallel process.

\(^{10}\) For example: *Hewlett-Packard Ink-Jet* packages.
Table 2.3: Comparison of parallelism of different packaging approaches. While wafer-level packaging typically is a special form of flip chip, it is listed here separately due to its unique features. (Here, $N$ is the number of connections per chip and $M$ is the number of devices per wafer.)

<table>
<thead>
<tr>
<th></th>
<th>Device</th>
<th>Connection</th>
<th>Conn. per iteration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire bonding</td>
<td>sequential</td>
<td>sequential</td>
<td>1</td>
</tr>
<tr>
<td>Flip chip</td>
<td>sequential</td>
<td>parallel</td>
<td>$N$</td>
</tr>
<tr>
<td>Wafer-level packaging</td>
<td>parallel</td>
<td>parallel</td>
<td>$N \cdot M$</td>
</tr>
</tbody>
</table>

The flip-chip technologies C4 and tape automated bonding can be classified as such assemblies; multiple analogue connections are formed in a single process. Wafer-level packaging even fulfills the definition on two levels, all connections of a single chip as well as all chips of a wafer are connected at the same time. On the other hand, wire bonding is a completely sequential process. In fact, it takes two bonds—one for each end of the wire—to form an electrical connection. Table 2.3 compares wire bonding, flip chip, and wafer-level packaging.

For WLP it can be argued that at the time of assembly the chips are not yet separated and must be viewed as a single part, i.e., the wafer. Still, the number of manufacturing steps required to fabricate a certain amount of parts is significantly reduced by packaging the devices before dicing.

2.4.2 Parallel Assembly of Independent Parts

This argument does not arise when dealing with parts that are more or less independent from each other, i.e., that are not directly coupled. In this case, there has to be some method in place to achieve individual handling of the parts involved. Generally, this relies on one of two approaches:

- a deterministic one requiring multiple manipulators and sensory feedback (thereby being very similar to the multiplication of serial processes),

- or a stochastic one relying on self-assembly which offers low equipment costs but severely limits the size and complexity of the parts that can be assembled (G. Yang and Nelson, 2004; Böhringer, Fearing, and Goldberg, 2007).

The method we will present in this thesis employs the second approach.
Table 2.4: Comparison of flip-chip and wire-bonding characteristics in MEMS applications. (See Lau, 2000a, table 2.1.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Wire bonding</th>
<th>Flip chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flexibility</td>
<td>very high</td>
<td>medium</td>
</tr>
<tr>
<td>Resilience to CTE effects</td>
<td>excellent</td>
<td>poor</td>
</tr>
<tr>
<td>I/O Density</td>
<td>limited to perimeter</td>
<td>very high</td>
</tr>
<tr>
<td>Electrical performance</td>
<td>good</td>
<td>excellent (short conn.)</td>
</tr>
<tr>
<td>Thermal dissipation</td>
<td>poor by itself</td>
<td>excellent (short conn.)</td>
</tr>
<tr>
<td>Self-alignment</td>
<td>none</td>
<td>partly</td>
</tr>
<tr>
<td>Small footprint</td>
<td>fair</td>
<td>excellent (CSP, WLP)</td>
</tr>
<tr>
<td>Thin profile</td>
<td>fair</td>
<td>excellent</td>
</tr>
<tr>
<td>Direct chip attach</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>Concurrency</td>
<td>sequential</td>
<td>parallel</td>
</tr>
</tbody>
</table>

2.5 Summary

The dominant methods for chip packaging are wire bonding and various forms of flip chip. Primarily due to the low pin count and high sensitivity to thermal expansion mismatch of MEMS, wire bonding is generally preferred for MEMS. For few pins the fast wire bonders available on the market today easily equal the throughput of flip chip. Still, there are many interesting features that make flip chip attractive for MEMS applications (see table 2.4). In particular, the small size with regard to footprint as well as the thin profile is very desirable for tightly packaged devices such as mobile phones, computer hard drives, or tablets. The excellent electrical performance might play an important role in RF-MEMS and micro-opto-electromechanical systems (MOEMS) applications where high signal frequencies are common. Furthermore, high I/O density is required for high-resolution digital light projectors.

As the IC industry is switching to flip chip, the existing wire bonders can be reused for MEMS applications where electrical demands and the number of pins are still much lower. Since these machines are already depreciated, the machine costs for wire bonding are low. A switch to flip-chip MEMS packaging will most likely only occur on the basis of technical merits.
2 State of the Art

In the next chapter we will present a parallel assembly method for (partially) uncoupled parts. It combines the benefits of deterministic assembly and self-assembly. The method offers increased throughput and unique features at reduced costs.
3 Parallel C4: Principle of Operation

The packaging method developed in this research project creates the electrical connection between substrate and chip and it mechanically fixates the chip on the substrate. The method does not deal with protecting the device from the environment. In the application for which the new packaging method was primarily developed (described in detail in the next chapter) physical interaction with the environment is a necessity. Furthermore, the product is most often used in lab environments where protection from the environment is not a priority. Therefore, the chip is not sealed in the traditional way. The underside of the chip is somewhat protected by the presence of the substrate.

While it has not been an objective in the method’s development, our approach does provide an excellent thermal connection between substrate and die that could function as a means of heat transfer.

Currently, wire bonding is the dominant MEMS packaging method while flip chip plays a minor role. As pointed out in the previous chapter, this is primarily due to the fact that the major advantage of flip chip, creating all connections simultaneously, offers limited benefit in low pin count situations. At the same time wire bonding equipment induces less expenses to chip foundries. In this chapter a parallel C4 method will be introduced that combines the benefits of flip chip packaging with low costs—even at low pin counts.

Wire bonding and flip chip have been applied to MEMS in the same manner as they have been applied to the semiconductor ICs they have been originally developed for. However, while being similar the requirements for the packaging of ICs and MEMS devices are not identical. Most of the requirements have already been described in the previous chapter. They are summarized in table 3.1. Of particular interest for us are the fairly few and large contact pads of MEMS. Many MEMS inherently require exact placement to guarantee precise measurement or actuation. Relying on the self-alignment properties of C4 (see section 2.3.3) for fine positioning, we initially only align chip and substrate coarsely. The reduction of
Table 3.1: Comparison of packaging requirements for MEMS and ICs

<table>
<thead>
<tr>
<th>Requirement</th>
<th>IC</th>
<th>MEMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Protection against the environment</td>
<td>yes</td>
<td>yes*</td>
</tr>
<tr>
<td>Interaction with the environment</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>Electrical connection</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Mechanical fixation</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Small pad size</td>
<td>yes</td>
<td>no†</td>
</tr>
<tr>
<td>High pin count</td>
<td>yes</td>
<td>no†</td>
</tr>
<tr>
<td>Precise alignment</td>
<td>extraneously yes‡</td>
<td>inherently yes</td>
</tr>
<tr>
<td>Careful handling due to fragility</td>
<td>less</td>
<td>more</td>
</tr>
<tr>
<td>Difficult or impossible cleaning</td>
<td>no</td>
<td>yes</td>
</tr>
</tbody>
</table>

* Depending on the intended operating environment it may not be required.
† There are exceptions with many connections that require small pad sizes (such as, e.g., digital light projector MEMS).
‡ Precise alignment is required due to the small pad sizes.

Initial alignment precision reduces robotic manipulator costs. More importantly though, it enables simultaneous placement of several parts.

3.1 Workflow

As the name suggests, our process is based on C4. It creates both mechanical and electrical connections between MEMS chips and substrates. One of the essential features of our process is that the chips are not flipped. Instead, the chips are connected to the substrates when they are already separated from the containing wafer (e.g., by dicing or etching) but still located at their original position (on some form of support structure). Instead of flipping the chips, as is common practice, we flip the substrates upside down and place them above the wafer.¹ We do so with several substrates at a time. The batch of substrates is handled by a single robotic manipulator. The batch is arranged in a grid and spaced out at an interval matching the spacing of the chips in the wafer or a multiple thereof.

¹ The process therefore, technically, cannot be categorized as flip chip.
Figure 3.1: Parallel C4 setup. In the setup a batch of only two substrates is placed above the wafer. 100 denotes the device wafer. 101 points at substrate holding devices that are attached to a robotic manipulator. 102 are MEMS chips. The substrates are marked 111. 110 is a support structure that the device wafer rests on.
Figure 3.2: Parallel C4 chip extraction. In the figures, only a single device and substrate are displayed. The sketches to the right picture magnifications of a single pair of contact pads with solder. The numbers from fig. 3.1 are reused.

(a) The substrate pads are coarsely aligned to the MEMS pads. The substrate pads are covered with the liquid solder.

(b) The substrate was lowered bringing the solder into touch with the substrate pads. The solder now bridges the chip’s and the substrate’s pads.

(c) The robotic manipulator has lifted the substrate. The solder has pulled the chip along. Once the chip is free-hanging, self-alignment takes place.
3.2 Suction Needles

The robotic manipulator coarsely aligns the matching contact pads of the batch of substrates to those of the MEMS chips that are to be assembled. Figure 3.1 sketches a simple setup in this state (partly enlarged in fig. 3.2a). The contact pads of the substrate are equipped with solder. Using some form of heating the solder is liquefied. As the robotic manipulator lowers the batch of substrates, the corresponding pads of substrates and chips are connected through the liquefied solder (see fig. 3.2b). The substrates are then lifted pulling the chips along. Once the chips are free-hanging the surface forces of the molten solder will work toward minimizing the distance between matching pads and thereby align the chips (see fig. 3.2c).

Only MEMS chips which have passed known good die testing (see section 2.1.5) are considered. If the processed array of devices contains dies that failed to pass testing, the respective positions in the substrate array are left vacant.

Figure 3.3: Lifting of the chip using retractable suction needles (501). In (a) the needles are touching the chip while a vacuum is applied. As the needles are retracted they pull the chip along until the chip's pads touch the solder on the substrate's pads in (b).
the chips at the same time). Then a vacuum is applied to the needles. The chips are lifted out of the wafer by raising the substrates along with the needles. After extraction the needles are retracted and vented. Now, the only connection between chip and substrate is the liquid solder. How far the needles initially extend through the substrate determines the exact succession of steps: If the needles extend beyond the height of the solder bumps, the substrates cannot be lowered to the point where the solder touches the chips’ contact pads. The solder connection is only created during the retraction of the needles (see fig. 3.3). Alternatively, the needles can be shorter than the height of the liquid solder bump. This has the advantage that the solder can already wet the pads of the chip while that is being extracted.

The flowchart of the complete process including control of the needles is depicted in fig. 3.4.

### 3.3 Required Robotic Precision

A prerequisite for the self-alignment to take place is that the solder wets the facing pads of substrates and chips. Assuming that the solder bumps form a spherical shape when molten, the maximum misalignment allowed is about half the pad diameter. Larger alignment pads can be added to the pad layout if increased alignment tolerance is required. A similar approach involving smaller pads has previously been proposed to increase alignment accuracy (Bache et al., 1988; Patra and Y. C. Lee, 1991a).

### 3.4 Solder Selection

The risks caused by thermal-expansion mismatch in solder-bump flip chip have been highlighted already. MEMS flip-chip applications are especially sensitive to shear stress (see section 2.3.4). To a certain degree, thermal-expansion mismatch induced stress can be mitigated by the right choice of solder. The solder used in parallel C4 should fulfill the following specifications:

1. Substrate and chip feature different coefficients of thermal expansion \( (\text{CTE}) \). The solder has to be soft enough to limit the CTE mismatch induced stress the
Figure 3.4: Flowchart of parallel C4
contact pads and thereby the MEMS chip are exposed to during temperature variations.

2. Since the exact alignment of chip and substrate is achieved by self-alignment, the solder has to provide large surface forces in the liquid state.

3. It has to wet the contact pads well (and preferably quickly).

Wetting quality is a result of solder—under-bump metallization (UBM) interaction, the cleanliness of the pads, possible pad and solder oxidation, and the chosen flux. Chapter 7 will analyze most of these points in detail. Flux helps to reduce oxides and prevent new ones from building up. During the soldering process, the viscosity of flux is at first reduced. When a solder paste is used, the flux is expelled from the paste. There is a risk that the flux wets the movable parts of the MEMS, which in many cases would destroy the chip. For this reason, flux-less soldering processes have been considered extensively for MEMS solder-bump flip chip: D. C. Miller, Zhang, and Bright (2000) describe soldering in a formic acid environment, Heschel et al. (1998) soldering in a reduced oxygen environment, and Tilmans, Fullin, et al. (1999) use plasma-assisted dry soldering (PADS). (Boustedt, Persson, and Stranneby, 2002)

Finally, it has been demonstrated in (Koopman, Bobbio, et al., 1993) that soldering in air is possible after PADS cleaning if the solder heat-up time is below 5 s.

3.5 Process Applicability

No process is appropriate or optimal for every application. This section will point out where the bonding process can be applied and what restrictions apply. The major constraining factors are the requirement that the chips are separated at bonding time, requirements regarding the substrate layout, and implications that arise when suction needles are employed.

3.5.1 Cleaning

MEMS chips cannot be cleaned from dust in a reasonably practicable way. Therefore, chip singulation technologies emitting debris (e.g., sawing) cannot be used
without temporary capping of the chips to prevent contamination of the MEMS. This induces additional process steps and costs. To avoid these a separation technology avoiding debris emission should be chosen. The misalignment tolerance featured by parallel c4 provides the advantage that the chips do not have to stay in the exact same place. The use of blue tape (see section 2.1.3) can often be avoided.

3.5.2 Pad Size

The self-alignment employed by this process can compensate for a misalignment of about half a pad size. The process requires that the chips have been separated from the wafer prior to its application. At this point the chips are generally free moving to a certain degree. The space in which the chips can move must not exceed the maximum misalignment.

3.5.3 Maximum Pad Distance

While it has been demonstrated that resin can be used for chip-to-substrate self-alignment (J.-M. Kim, Shin, and Fujimoto, 2004), solder is the preferred choice due to its high surface tension. The rather rigid nature of the solder joints is only able to compensate a limited amount of shear force. The shear forces are caused by mismatches in the coefficient of thermal expansion of substrate and chip (see section 2.3.4). The problem is particularly pronounced when organic substrates are used. The shear force in a pad is proportional to its distance to the neutral point (DNP). The maximum distance between pads, therefore, is limited.²

For regular ICs underfill is often used to reduce the shear stress on the solder joints and prevent joint failure. However, this increases the stress on the chip and, thus, is often not appropriate for MEMS. Furthermore, liquids must be handled with extreme care in the vicinity of MEMS to prevent the moving parts of the device from being wetted. That would render the devices useless (see section 2.3.6).

3.5.4 Substrate Layout

Our process places the substrates above the wafer and lowers them to the point where the contact pads of the substrate land location nearly touch those of the chip with only the solder connection in-between them. At this point the devices are

² This limitation is common to all solder-bump flip-chip processes.
still contained in the wafer. This implies that the pads at the land location must be the most extended elevations on the substrate. Other components can, therefore, not be placed onto the substrate’s chip-facing surface in advance. There are some scenarios where this limitation could preclude the application of the presented method.

System in Package

When several chips are encapsulated in the same package they are also often placed on a single substrate. In this case, only the first of these chips can be bonded in the described way. Even then, the method will not exhibit its full potential. In the case of multiple chips being placed next to each other on a single substrate, parallelization is limited. Section 3.6 below will elaborate on this.

The IC industry is moving to 3D-SIP. Here, the various chips making up a system are stacked one over each other. Generally, the bonding technology used is solder bumping. This packaging paradigm, in general, is compatible with the presented bonding method.

Substrate Cavities

Certain substrates feature a cavity to ease later sealing. In this case, an edge surrounds the place where the MEMS chip is to be located (J. S. Lee et al., 2009; Tilmans, Peer, and Beyne, 2000)). This edge would touch the wafer during assembly before MEMS chip and substrate can do so.

Overcoming the Substrate Layout Limitations

Through the use of the suction needles detailed in section 3.2, the layout induced limitations described above can be overcome. The distance between wafer and substrate is adjusted so that the substrate’s elevations do not touch the wafer. Longer needles, capable of still reaching the chips, are used to bridge the distance to the wafer.

3.5.5 Vacuum Needles

Retractable vacuum needles come at a price, however. They require holes in the substrate to reach through. This creates two restrictions: for one, the space occupied
by the holes basically cannot be used for anything else. Depending on the kind of device and the desired sealing, the holes must be closed after bonding. This can, for packages requiring completely hermetrical sealing, be quite difficult to achieve. But even for packages that are only required to provide a less rigid encapsulation an additional process step is added.

Also, the vacuum needles increase machine costs. The retraction mechanism makes the machine more complicated. In particular, adapting the machine to different packages with different needle locations induces costs. These costs can, however, be largely avoided by package standardization.

3.6 Process Throughput

Obviously, the maximum throughput is directly linked to the achievable parallelization, defined by the number of devices that can be bonded simultaneously. The maximum achievable assemblies per process iteration is the number of substrates that fit on the wafer while the chip and substrate grids are aligned. Therefore, the larger the surface area of the substrate is, the less throughput will be achievable. On the other hand a larger wafer allows higher parallelization.

An interesting feature of this process is the fact that the amount of parallelization can be chosen within the above limit. For some devices, it might be rational to not exhaust the full parallelization potential to keep equipment costs low. Especially experimental setups in labs or small lot sizes come to mind here.

3.7 Relationship to Other Methods

From a parallelization perspective our method is most closely related to wafer-level packaging. It is the only other method where multiple devices are bonded simultaneously. However, there are important distinctions:

- Our method does not require the devices to be precisely aligned to each other.
- Parallel c4 does not restrict the substrate size to be (nearly) identical to the chip size.
- The method can leave chips that are identified as broken (by KGD testing) unpackaged.\(^3\)

- WLP often uses substrates with low elastic moduli to ensure compensation of the thermal-expansion mismatch. While this should, up to a certain degree, be possible for parallel C4 as well, this has not yet been verified.

Our method can easily provide chip-scale packages (CSPs). Since the parallelization achievable in inversely proportional to the substrate area, the method does not live up to its potential for DCA to boards of prevailing sizes. It is, however, suitable for bonding devices in 2D- and 3D-SIP applications (which generally have smaller footprints). The distinction between SIP and DCA is ambiguous for small unenclosed packages, especially when dealing with organic boards.

In fact, the application presented in the next chapter is such an ambiguous case: a use case will be presented where a chip is bonded to a small PCB using parallel C4.

\(^3\) *Tessera's WAVE WLP* method can selectively package devices as well. (Lau et al., 2009, ch. 10.6)
4 Application: Assembly of the FT-S260 Force Sensor

The method was verified in a case study. A demonstrator was built to bond Femto-Tools FT-S260 force sensors chips (see fig. 4.1) to substrates.

4.1 The Product

The FT-S260 consists of a MEMS chip, a small PCB, a few passive components, a converter IC, and an eight-pin connector. All the other components are mounted onto the PCB. The PCB material is FR-4. The chip is directly attached (DCA) to the organic substrate.¹ For the final device to produce accurate measurements, it is essential that the sensor is exactly orientated with regard to the substrate. Because the force sensor must directly contact its environment, it does not receive protective packaging.

¹ It can be argued that the case should be classified as an SIP application. Since there is no enclosure and due to its connector-based interface, we decided to classify it as DCA instead.

Figure 4.1: The assembled FemtoTools FT-S260 force sensor
4 Application: Assembly of the FT-S260 Force Sensor

4.1.1 Chip Manufacturing Process

The sensor is manufactured from a silicon-on-isolator (SOI) wafer using reactive-ion etching (RIE) and the Bosch variant (Laermer and Schilp, 2003) of deep reactive-ion etching (DRIE). (Sun, Fry, et al., 2005)

Chip Singulation

Contrary to the typical situation (see section 2.1.3), the transducer fabrication process does not require dicing of the wafer. Instead, the device wafer is placed on a support wafer. During the etching process the individual chips are completely separated from the device wafer. After that, they are resting on the support wafer. The chips can move freely in a 200 µm gap created by the etching process, and their precise position is no longer defined. The etching process generates heat. To prevent high temperatures from damaging the force sensor, the heat must be dissipated. As the devices are being separated from the device wafer, the device wafer can no longer absorb the heat. To remedy this, heat-conductive paste is placed between the nascent devices and the support wafer. This paste conducts the heat away from the individual chips.

4.1.2 Sensor Operation

The sensor’s probe tip is connected to elastic flexures. Using these, the force to be measured is converted into a deflection. The amount of deflection is detected by
two capacitor electrode arrays (differential *comb drives*, see fig. 4.2). (ibid.) The comb drives are tightly spaced. Liquid coming into contact with the comb drives’ electrodes will cause the electrodes to permanently adhere to each other. This prohibits the use of cleaning solutions. (Beyeler, Neild, et al., 2007)

4.1.3 Current Process Steps

Prior to this work, the devices have been manually wire bonded. Packaging consisted of the following steps (see also fig. 4.3):

*Extraction* First the sensors are manually extracted from the wafer using tweezers.

*Placement* They are then placed onto the substrate.

*Alignment* Afterwards chips are manually fine aligned to the substrate.

*Glue deposit* The aligned chip and substrate are permanently connected using an adhesive.

*Wire bonding* Finally, after the adhesive has cured, the electrical connections are created using manual wire bonding.

4.1.4 Pad Layout

The substrate features square pads with a side length of 380 µm while the chip features rectangular pads of 360 µm × 400 µm size. The maximum diagonal distance between pads is 3.6 mm.

To maximize self-alignment torque and to balance chip support the pad layouts of the chip and the substrate have been slightly modified for the new process.

4.1.5 Under Bump Metallurgy

The pads and traces on the substrate are made of copper. The pads are plated with 36 µm of nickel (Ni) and 50 nm to 150 nm of gold (Au). The contact pads of the MEMS chip are also gold plated (200 nm) to prevent oxidation and guarantee good solder wettability. The adhesion layer underneath the gold consists of 10 nm of titanium (Ti).
1a. Extraction of MEMS chips from the wafer.  
1b. Unpopulated PCB.

2. The chip is placed onto the PCB.  
3. The chip is aligned to the PCB.

4. An adhesive is deposited to fixate the chip on the PCB.  
5. Wire bonds are created to electrically connect the chip to the PCB.

**Figure 4.3:** Current processing steps. Note that devices packaged using the wire bonding process are placed on the same side the readout electronics are placed. Chips bonded using parallel C4 are placed on the opposite side.
4.2 Parallel C4 Parameters

4.2.1 Solder

In section 3.4 desirable properties of parallel C4 solder were pointed out. A low-melting-point\(^2\) soft solder can offer the required properties. A low soldering temperature also reduces the stress that results from the CTE mismatch during the cool-down after the assembly.

At the time different solders were evaluated we attributed another advantage to the use of a low-melting-point solder: Before MEMS bonding, the substrate is already equipped with several electronic components. These components are soldered onto the substrate, too. To make use of step soldering, the solder used in the MEMS assembly must have a melting point that is well below the one of the solder used for the assembly of the other electronic components—at least when nonlocal heating is employed.

In the process of this work we developed a localized heater. Using this heater the different melting points of the solder used for MEMS attachment versus those used for the other components are no longer a requirement (see chapter 6).

Owing to the experimental nature of this work and also to the type of product assembled, conformance to PbFree standards was not considered a necessity. A solder paste (Indium Corporation 5.5 LT) containing the eutectic bismuth (Bi, 46 % mass fraction), tin (Sn, 34 %), lead (Pb, 20 %) alloy (Indalloy 42, solder paste metal content: 84 %) was selected for this work. It features a melting point of 96 °C. Bismuth solders are ductile when exposed to slow shear speeds (such as the thermal expansion while heating up or the thermal shrinkage while cooling down); on the other hand they are brittle for quickly changing loads (Grimmer, 2012c). Bismuth solders provide very good wetting of noble metals (ibid.).

According to Indium Corporation, the maximum operating temperature of soft solder (such as this one) is 90 % of the absolute melting point temperature (Scalzo, 2011b). In the case of the alloy used, this is

\[
0.9 \cdot 369.15 \, \text{K} = 332.24 \, \text{K} \approx 59 \, ^\circ\text{C}.
\]

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\(^2\) Compared to solders routinely used in electronics assembly: The historically popular lead-containing 63Sn-37Pb alloy melts at 183 °C. Common lead-free solders have a higher melting
Gold Embrittlement

The large amount of tin (Sn) contained in the solder leads to high surface forces in the liquid state. However, it creates an intermetallic bond with the protective gold layers of the contact pads. The intermetallic compound (IMC) has been shown to accelerate solder joint fatigue (Judith Glazer, Kramer, and Morris, 1992). This effect is commonly called gold embrittlement. According to Scalzo (2011a), Indium Corporation considers pads with an UBM gold layer of up to 381 nm (15 μ”) thickness to be safe from being affected by embrittlement.

4.2.2 Flux

The solder paste contains no-clean flux. The presence of flux removes the need for extensive cleaning of the pads or a controlled assembly environment. As the name implies no-clean flux does not need to be removed after the soldering process—an essential feature for our application where fluids would destroy the sensor (see section 4.1.2).

4.3 Application Process Steps

The parallel c 4 process has already been described in section 3.1. This section describes the process steps of our experimental setup in detail. The flowchart depicted in fig. 3.4 applies here as well. The different system components will be described in detail in the next chapter.

In the demonstrator, batches of only three devices3 are bonded at a time. This keeps machine and tooling costs low while still proving the viability of the parallel approach. The solder application and substrate mounting and unmounting steps, in particular, would be implemented differently in a production setup.

Before being assembled, the individual devices are in-wafer-tested for defects using the resonance method described in (Beyeler, Muntwyler, and Nelson, 2010; M. Yang et al., 2010). Only known good dies (KGĐ, see section 2.1.5) are assembled.

3 When there are not enough devices left in a row, or chips have found to be faulty during in-wafer testing, fewer devices are bonded in one batch.
4.3 Application Process Steps

Figure 4.4: The micrograph shows the system right after chip pickup. At the bottom, the wafer table is depicted. Above that, three identical substrate holding devices that are attached to a robotic actuator are located. The arrows point to the probe tips of three MEMS chips that have just been separated from the wafer. The separation of the MEMS chips from the wafer was assisted by suction needles that reach through the substrate. In the picture the suction needles are still in their bottom position and are holding the chips.
The manufacturing process uses heat-conductive paste between the individual chips and the support wafer (see section 4.1.1). This paste is of a sticky nature. It prevents the chips from being lifted out of the wafer by the solder surface forces alone. Suction needles are utilized to assist lifting (see section 3.2).

4.3.1 Underfill

To limit the stress on the chip that could impede the sensor's measurement accuracy, we refrain from using underfill in our application (see section 2.3.6). Not using underfill also removes the risk of it cloaking the comb drives. In operation, the chip produces virtually no heat and large temperature variations are not expected.

4.3.2 Solder Application

Due to the relatively large pads used, it is not necessary to use expensive solder bumping methods such as vacuum metallization to obtain tinning of the chips' contact pads. Instead, solder paste is dispensed onto the substrate prior to the actual assembly taking place. The solder could also be dispensed onto the chips, but that approach offers no advantage in our setup. Dispensing the solder onto the substrate, on the other hand, allows the solder application to be easily corrected if necessary (i.e., by cleaning the substrate and reapplying the solder). For batches of significant size, mask printing of solder paste is feasible. When maximum deposition consistency or high throughput is required, \textit{c4 new process (C4NP)} (P. A. Gruber et al., 2005; Laine, Perfecto, et al., 2007) embodies the preferred alternative.

For solder application the \textit{EFD Ultimus Ultra 2400} half-automatic dispenser is used (see fig. 4.5). For a controlled amount of time pressurized air is allowed to extrude the solder paste out of a syringe. The operator holds the syringe needle against the pad the solder is applied to. While timing and pressure are closely controlled by the dispenser system, the amount of solder still varies. Both the angle the syringe is held at and the room temperature have a significant influence on the solder amount. For example, the viscosity of the \textit{Felder ISO-Cream EL 42/58} solder paste (viscosity of 200 Pa s at 25°C) decreases by about 10 Pa s per °C temperature increase (Grimmer, 2012a).

To verify the amount of solder paste that has been dispensed, the substrates, therefore, been weighted prior to and after dispensing. A \textit{Mettler Toledo Xp56}
4.3 Application Process Steps

Figure 4.5: Manual dispensing station

Figure 4.6: The precision scale used for determining the applied solder weight.
microbalance with 1 μg readability was used for the task (see fig. 4.6). In an industrial application solder dispensing would be automated and integrated with the rest of the process.

4.3.3 Wafer Registration and Heating

The wafer is placed onto the wafer table. There, it is held in place by vacuum. Furthermore, it is heated to 92 °C, a temperature just below the melting point of the solder (see section 5.4.2). Preheating the chips reduces the time required to heat the chips when they are first connected to the substrate. At that time there is no metallic link between the chip and substrate, and the heat transfer is still limited.

To determine the precise position of the wafer, two alignment marks are located by a custom image processing system (Wyss and Glocke, 2010). Relative to the marks, the approximate position of each chip contained in the wafer is known. A compact and low-cost camera system (section 5.7) is used for the alignment mark localization. The camera is attached to the same robotic manipulator as the substrate holders (see fig. 4.7). To overcome projection deficiencies of the optical system, the exact mark position is established in an iterative process. First the position of the mark is determined, then the camera is moved to that position. In doing so, the mark moves towards the center of the camera image where the optical distortion is smallest. The process is repeated in an alternating fashion until the mark is at most 50 μm from the image center in either direction.
4.3.4 Substrate Mounting and Heating

The PCB substrates are manually placed into substrate holders (see section 5.5) that are attached to a 3-axis Cartesian robot (see section 5.2). Sometimes not all substrate positions are matched by a functional chip. This regularly happens at the edge of the wafer. It can also occur when a broken chip has been detected by the in-wafer testing. In these cases the corresponding substrate holder is left vacant. In an industrial application the substrate PCBs would not be mounted manually but picked up automatically.

There is a Joule heater embedded into each of the substrates. This heater is later used to liquefy the solder. During the mounting of the substrates the electrical connection to the heater is created. The heater control electronics are capable of quickly detecting temperature changes in the substrate. However, they are not capable of measuring the absolute temperature of the substrate. They have to be primed with an initial temperature once for each new substrate. Since the substrate is manually mounted, the initial temperature is not known. The robotic manipulator moves the substrates to a position above infrared thermometers. The thermometers measure an initial temperature. From then on the heater can closely control the substrate temperature. The heater, its control electronics, and the initialization process are described in chapter 6.

The substrates are now locally heated at the land location. The temperature is set to 80 °C, still below the solder melting point. The solder is not yet melted to allow visual recording of the self-alignment. If the solder was melted now self-alignment would start as soon as the chips are picked-up and free-hanging. Again, in an industrial process, the visual monitoring of the alignment process would not be required and the solder could be melted immediately.

4.3.5 Chip Pick-Up

The robotic manipulator moves the substrate above the chips that are going to be picked up. The corresponding substrate and chip pads are now coarsely aligned. The suction needles are extended through the substrate (see fig. 4.8). The length of the needles is predefined so that their extended part is slightly shorter that the

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4 The temperature of the operators hands heats up the small substrates quickly.
solder bumps are height. The substrates are lowered towards the wafer, up to the point where both the suction needles and the solder touch the chip. At this point a vacuum is applied to the needles. As the substrate is lifted, the chips are pulled along (see fig. 4.9).

4.3.6 Self-Alignment

In principle, the needles could now be retracted and vented. Self alignment would start as soon as the solder is liquefied. To be able to observe this process, the robotic manipulator moves the batch of substrates and chips to a camera station first. The camera is up-facing and pointed at the middle substrate (fig. 4.10). After the recording is started, the needles are retracted and the heater is set to the soldering temperature. The chips are only connected to the substrate by the solder paste (which is designed to be tacky). As the temperature crosses the melting point of the solder, surface forces minimize the distance between the substrates’ pads and the corresponding chips’ pads. In the process the chip and substrate are aligned.

Once the assembly is finished, the heating is turned off and the assembled products are manually removed from the substrate holders. Once more, this process step would be automated in an industrial application.
4.3 Application Process Steps

$t = 0 \text{s}$
Before extraction
Suction needles and solder bumps can just be seen underneath the substrates.

$t = 1 \text{s}$
During extraction
The PCBs nearly touch the wafer

$t = 2 \text{s}$
After extraction
The chips are right underneath the substrates.

*Figure 4.9:* Chip extraction time series. In all of the three pictures the substrate holders (transparent and beige-colored) are shown with the substrate (green) attached. On the bottom the copper wafer table is depicted. The wafer on top of the table is difficult to see against the background. In the first and the last picture the chips’ land locations are marked by white ellipses.
**Figure 4.10:** Assemblies at the self-alignment tracking station. The chips have been extracted from the wafer and are hanging underneath the substrates. They have been moved above the camera (lighted box on the table to the left of the picture). Here, the substrates are heated to the soldering temperature. After the suction needles are retracted, self-alignment takes place.
5 System Components

This chapter describes the major components that make up the system. Most of
the components have already been mentioned in the previous chapters. The com-
ponents include a wafer table, substrate holders, a robotic manipulator, infrared
thermometers, cameras, a vacuum distribution station, a low-level hardware con-
troller, and a process controller. Before we describe the individual components in
detail, we will outline the component interaction.

5.1 Interaction

Except for the two cameras, one used for finding the alignment marks of the wafer
and one for recording the self-alignment, all other components are connected to the
low-level hardware controller. Figure 5.1 gives an overview of the inter-component
connections. The cameras are directly connected to the process controller. The
process controller also hosts the graphical user interface (GUI) the operator interacts
with. Process controller and hardware controller are connected through Ethernet.
The vacuum distribution station and the robotic manipulator are connected to the
low-level controller using various analog and digital electrical connections. The
remaining devices (infrared thermometers, substrate heaters and wafer heater)
interact with the low-level controller through a peripherals bus (section 5.3.4).

5.2 Robot

We use a Cartesian manipulator to move the substrates from one place to another.
The Cartesian manipulator is a modified Sysmec robot.
5 System Components

![System Component Interaction Diagram](image)

**Figure 5.1:** System component interaction

### 5.2.1 Electronics

All electrical parts of the robot except for the motors have been replaced. The incremental digital encoders have been exchanged for analog sinusoidal variants (*Heidenhain ERO 1480 1500* type). These provide a much higher measurement resolution (212.5 ticks per mm actuator movement, our custom *HiresEnc* encoder boards provide up to 12 bit interpolation of the analog signal). This allows for increased positional accuracy, stiffness, and speed. Ten-micrometer precision is achieved in our configuration. The robot is controlled by the low-level hardware controller that will be described below.

### 5.2.2 Actuators

The three actuators of the Cartesian manipulator feature gear racks that are driven by brushed DC motors (2.4 V, 2.1 A, 2100 min⁻¹). The motors are powered by *Elmo Harmonica 12/60* amplifiers. Each of these is controlled by an analog signal from the low-level hardware controller (section 5.3.5).
5.3 Low-Level Hardware Controller

The low-level hardware controller’s main tasks are interaction with the hardware, robot path-planning, and task scheduling. It receives its commands from the process controller. There are three relevant programs running on the low-level controller computer:

- the task scheduler,
- a program interacting mostly with robot hardware and also performing path planning (referred to as robot controller from hereon),
- and a program interacting with the peripherals network.

The low-level controller runs the Debian operating system version 5.0 in a minimal setup. It has been configured to use a custom Real-Time Linux (Rostedt and D. V. Hart, 2007) kernel version 26.33.7-rt29. Our software is written in the C programming language (Kernighan and Ritchie, 1988). It only links against the GNU C library (GLIBC, 2012). This combination allows us to create a hard real-time software stack without inducing royalty fees.
5 System Components

![Diagram](image.png)

**Figure 5.3:** IndustryPack device tree

### 5.3.1 Task Scheduling

The task-scheduling process is the outside interface to the low-level controller. Clients communicate with the scheduler through a simple, plain-text based protocol over TCP/IP.

The task scheduler (called taskplannerd) in turn communicates with the robot controller (sysmelec) and the peripherals controller process (temperated since all peripherals are temperature related). The scheduler is responsible for handling the individual commands it receives in the right order, and waiting for events before continuing. The robot and peripherals controllers periodically (robot: 5 kHz, peripherals: 10 Hz) broadcast their current state to the task scheduler. Commands from a client that query a state are executed out of order, that is, responded to immediately.

### 5.3.2 Hardware

The low-level controller hardware consists of a CompactPCI-based Industrial PC (Intel Pentium M 1.6 GHz processor, 512 MB RAM). It is equipped with three IndustryPack carrier boards (Tews Technologies TCP213). These boards in turn carry

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several digital and analog I/O (input/output) IndustryPack modules (Tews Technologies TIP670 and TIP570) and CSEM’s custom HiresEncoder analog encoder readout boards. The carrier boards act as interfaces between the IndustryPack devices and the PCI bus (see fig. 5.3). In the course of this thesis a Linux kernel IndustryPack subsystem and device drivers for the used devices have been written. This work is being merged back into the official Linux kernel.

5.3.3 Inter-Process Communication

Communication between the task scheduler and the robot and peripherals controllers follows a binary protocol and is executed over Unix domain sockets (Stevens, Fenner, and Rudoff, 2004). While a shared-memory based communication would be more efficient (i.e., it requires less copying of data and, therefore, less processor time), the chosen method offers easy and reliable synchronization between the processes. Each communication message is sent atomically. That means, it is either send or it is not. One of the processes could fail at any time and the timely execution of the other processes would not be affected. For example, if the task planner would stop working, the robot controller would still continue to execute the last commands it has received.

Several clients can communicate with the robot and peripherals controllers simultaneously. (E.g., the task scheduler is a client from the perspectives of the robot controller and of the peripherals controller.) Multiple connections have a negligible effect on the controller’s performance. This feature is mainly used for debugging. For example, we have implemented a small logging program that continuously outputs the robot controller state. The low-level controller has limited storage and no graphical interface. However, the output of the logger can easily be piped into the netcat program (Netcat-openbsd 2012) which in turn sends the output to a remote computer. There, the received data can be stored or directly analyzed.

Some interprocess communication methods can cause page faults. Page faults occur when a program tries to access a memory address that is not present in the computer’s physical memory at the time. The operating system, specifically its virtual memory subsystem, needs to rectify this situation, halting the running program while doing so. This causes latency, which would interfere with the robot
controller’s real-time operation. While continually supervised, no page faults have been observed.¹

5.3.4 Peripherals Network

IR sensors, substrate heater control electronics and the wafer heater are controlled by a peripherals controller software. The peripherals controller is a simple software interface to a bus of devices. It regularly polls these devices for the current state (e.g., the currently measured temperature, the output power, whether a substrate is connected, etc.) and sends commands to the devices. The network is built around the I²C bus (NXP, 2012) operating at 5 V and 100 kHz (standard-mode). To prevent the power supplies of the different devices from causing leakage currents, each connected device is galvanically isolated from the bus. The implemented protocol is SMBUS (SBS Implementers Forum, 2000) compatible and includes SMBUS check-summing to guarantee data integrity. A small interface board based on the Microchip PIC18F14K50 microcontroller interfaces the low-level controllers RS-232 serial connection to the peripherals network. A simple text-based protocol is used for the communication between process controller software and the interface board.

5.3.5 Robot Controller

The robot controller runs at a frequency of 5 kHz. In each loop the following steps are repeated:

1. the current hardware state is obtained,

2. the actuator controllers are run,

3. the actuator outputs are sent to the hardware,

4. the path-planner is run,

5. communication is handled.

¹ While we have found no formal specification guaranteeing Unix domain socket communication not to cause page faults, there seems to be a consensus that they do not.
This process is optimized to keep the time between reading the hardware state and writing the output values minimal.

Ensuring Real-Time Operation

Because we directly control the robot amplifiers (section 5.2.2) via a software PID controller, real-time operation is essential. We already mentioned that a real-time operating system is being used. This is not sufficient to guarantee actual “hard” real-time performance. One thing to avoid during real-time operation are memory allocations. We therefore allocate all the memory the robot controller requires during startup. After that no more memory is required. We are able to dispense with memory allocations because the robot controller task is separate from the task scheduler (section 5.3.1). The task scheduler would be difficult to implement without memory allocations, because in theory, the task queue can grow indefinitely. Using separated tasks and our interprocess communication approach (section 5.3.3), the task scheduler is separated from the robot controller and does not need to be executed in real-time. It cannot affect the robot controller’s performance.

5.3.6 Path Planner

In regular operation, the robot controller operates in a position controlled mode.\footnote{As opposed to a speed-controlled mode during axis initialization and opposed to an uncontrolled mode during position controller auto-tuning. These modes are not described in this thesis.} The path planner is based on the \textit{flexptpmotion} algorithm presented in (Luthiger, 1996). It has been extended to use a third order kinematic model instead of a second order kinematic model. The path planner has been continuously developed at CSEM Alpnach over the past years. Much of this work was done by Dr. Marcel Honegger. For the work leading to this thesis the algorithm has been reimplemented from the ground up.

Internally at CSEM, the algorithm is referred to as the \textit{adaptive} path planner. This is due to the fact that at any given point in time the path is calculated only on the basis of the current motion state and the target motion state. No other state information is used in any way. This in turn means that the goal can change at any
time and the path will be adapted immediately.

Motion State

A motion state is defined as position \(x\), velocity \(v\), and acceleration \(a\) of each axis within a coordinate system. The jerk \(j\) does not need to be stored because there is no limit to its rate of change. We generally plan within Cartesian coordinate systems.

Motion State Transformation

For path planning we transform the global coordinate system in a way that the origin is at the target position and the first axis points away from the current pose (i.e., the current position is on the negative side of the first axis). We transform the complete robot motion state accordingly.

Using the transformed motion state, we try to reach the origin of each axis. Our strategy is to reach the target as fast as possible while adhering to allowed ranges for velocity \(v \in [v_{min}, v_{max}]\), acceleration \(a \in [a_{min}, a_{max}]\), and jerk \(j \in [J_{min}, J_{max}]\).

Distance to Constant Velocity

The distance-to-constant-velocity calculation produces the fastest strategy to reach a constant velocity \(v_o\) within the constraints of the jerk and acceleration limits. (The velocity will be changed as quickly as possible, so the algorithm will not violate the velocity constraint if current \(v_3\) and target \(v_o\) velocities are within the constraint and the current acceleration \(a_3\) does not force it to.) It then determines the distance traveled when applying this strategy. Trying to find the quickest strategy results in the jerk either being assigned the maximum or minimum value as long as the acceleration is not bound by its limits.

The strategy consists of up to three phases. Within each phase the jerk is constant. The jerks in the three phases are called \(J_{p1}\) through \(J_{p3}\) for phase 1 through 3, respectively. As shown in figure 5.4 we define \(t\) so that motion has reached constant velocity at \(t = 0\). Furthermore, we define the velocity at \(t_i\) to be called \(v_i\), the acceleration \(a_i\), and the position \(x_i\). Even if not all phases are required, the index
5.3 Low-Level Hardware Controller

Figure 5.4: Motion phases

\( i = 3 \) always refer to the motion at the beginning of the strategy. The jerk can change abruptly at the phase boundaries. We will work with offset velocities and positions

\[
v' = v - v_o \quad \text{and} \quad x' = x - x_o. \tag{5.1}
\]

Depending on the initial speed \( v'_3 \) and acceleration \( a_3 \) a different number of motion phases will be required. Since phase 1 is always required it will be described first. Generally, phase 3 is also required. If a full stop cannot be achieved using these two phases a third phase 2 needs to be added. What exactly makes the different phases necessary will be described while the phases are defined. Even though we develop a full motion strategy in each path planning cycle, we discard it as soon as we have taken the appropriate action and the path-planning iteration ends. The planning starts over in the next iteration.

Phase 1 Phase 1 linearly reduces the acceleration modulus from \( a_1 \) at the start of the phase to \( a(t = 0) = 0 \). At first we examine what would happen if we assume \( a''_1 = a_3 \) and \( v''_1 = v_3 \) (i.e., directly start phase 1)

\[
f''_{p1} = f''_1(t_1 \leq t < 0) = \begin{cases} J_{\text{min}} & \text{if } a_3 \geq 0 \\ J_{\text{max}} & \text{if } a_3 < 0. \end{cases} \tag{5.2}
\]

A constant velocity is reached when \( a = 0 \). With

\[
a(t_1 \leq t < 0) = \int f \, dt \quad \text{with } a(t = 0) = 0
\]

\[= J_{p1} \cdot t \tag{5.3}
\]

and

\[
v''(t_1 \leq t < 0) = \int a \, dt \quad \text{with } v''(t = 0) = v''_0
\]

\[= \frac{1}{2} J_{p1} \cdot t^2 + v''_0 \tag{5.4}
\]
we obtain

\[ v''_0 = v'_3 + \frac{1}{2} j''_1 t_1^2. \] (5.5)

With eq. (5.5) we can deduce

\[ v''_0 = v'_3 - \frac{a_1^2}{2 j''_1}. \] (5.6)

In the unlikely event that \( v''_0 = 0 \), no additional phases are required and \( j_1 = j'_1, \ a_1 = a_3, \) and \( v'_1 = v'_3 \). However, if \( v''_0 < 0 \) we need to increase the speed prior to reaching phase 1 and if \( v''_0 > 0 \) we need to decrease the speed. At this point we can already determine most of our final strategy

\[ j_{p1} = j(t_1 \leq t < t_0) = \begin{cases} j_{\text{max}} & \text{if } v''_0 > 0 \\ j_{\text{min}} & \text{if } v''_0 < 0 \\ j''_1 & \text{otherwise} \end{cases} \] (5.7)

and

\[ j_{p3} = j(t_3 \leq t < t_2) = \begin{cases} j_{\text{min}} & \text{if } v''_0 > 0 \\ j_{\text{max}} & \text{if } v''_0 < 0 \\ 0 & \text{otherwise} \end{cases} \] (5.8)

After that, \( v''_0 \) can be discarded.

Now that we know the jerks for phase 1 and phase 3, we can determine the remaining parameters. Since, at the end of phase 1 the velocity \( v' = 0 \) (owing to eq. (5.1)), the speed at the beginning of phase 1 (\( v'_3 \)) can be deducted. The constant target velocity is assumed when

\[ v' = 0 \quad \land \quad a = 0 \quad \land \quad j = 0. \] (5.9)

This leads to the following equations for velocity and position of the actuator (with eq. (5.3) still being valid)

\[ v'(t_1 \leq t < t_0) = \int a \, dt \quad \text{with } v'(t = 0) = 0 \\
= \frac{1}{2} j_{p1} \cdot t^2 \] (5.10)
\[ x'(t_1 \leq t < 0) = \int v \, dt \quad \text{with } x'(t = 0) = 0 \]
\[ = \frac{f_1}{6 J p_1} \cdot t^3. \quad (5.11) \]

Given the acceleration \( a_1 \), we can deduce \( t_1 \) as the time when we will start reducing the acceleration modulus
\[ t_1 = \frac{a_1}{f p_1}. \quad (5.12) \]

At this point, the velocity needs to fulfill
\[ v'(t_1) = v'_1 = \frac{a_1^2}{2 J p_1} \quad (5.13) \]

for the motion to stop at \( t = 0 \). Before the (final) phase 1 can be initiated, a state fulfilling eq. (5.13) has to be produced.

**Phase 3**  This is done in phase 3, an initial decelerating or accelerating phase. The acceleration in this phase is changed from the initial \( a_3 \) to \( a'_3 \) at the beginning of the final phase 1 (assuming no phase 2 exists for now). Because we do not consider the acceleration limits, we work with \( a'_3 \) for now. The duration of the change \( \Delta t_{p3} \) and velocity change \( \Delta v'_{p3} \) during the phase are
\[ \Delta t_{p3} = t_2 - t_3 = \frac{a'_1 - a_3}{J p_3} \quad (5.14) \]
\[ \Delta v'_{p3} = v'_2 - v'_3 = \frac{a'_1 + a_3}{2} \cdot \Delta t_{p3}. \quad (5.15) \]

To achieve the complete speed change of \( v'_3 \) in the two phases, the summed velocity change in phases 1 and 3, \( \Delta v'_{p1,3} \), has to fulfill
\[ \Delta v'_{p1,3} = 0 - v'_3 = -v'_1 + \Delta v'_{p3} \]
\[ = -\frac{a_1^2}{2 J p_1} + \frac{a_1^2 - a_3^2}{2 J p_3}. \quad (5.16) \]

This is the case for
\[ |a'_1| = \sqrt{\frac{J p_1}{J p_1 - J p_3} \left( a_3^2 - 2 J p_3 v'_3 \right)} \]

with
\[ a'_1 = \begin{cases} |a'_1| \quad \text{for } j_1 < 0 \\ -|a'_1| \quad \text{otherwise.} \end{cases} \quad (5.17) \]
5 System Components

Phase 2  Accelerations are limited to be within \([a_{\text{min}}, a_{\text{max}}]\). If \(a'_1\) exceeds this range an additional phase 2 is required. During this phase the acceleration \(a_1\) is constantly applied. Depending on the value of \(a'_1\)

\[
a_1 = a_2 = a(t_2 \leq t < t_1) = \begin{cases} 
  a_{\text{max}} & \text{if } a'_1 > a_{\text{max}} \\
  a_{\text{min}} & \text{if } a'_1 < a_{\text{min}} \\
  a'_1 & \text{otherwise.}
\end{cases}
\]

(5.18)

Phase Durations  The duration of phase 1 was shown in eq. (5.12). Durations of phase 2 and 3 are given by

\[
\Delta t_{p3} = \frac{a_2 - a_3}{f_{p3}} \quad (5.19)
\]

\[
v'_2 = \frac{a_2 + a_3}{2} \cdot \Delta t_{p3} \quad (5.20)
\]

\[
\Delta t_{p2} = \frac{v'_1 - v'_2}{a_2}. \quad (5.21)
\]

After obtaining the parameter for the different phases as described above, the distances traveled in the individual phases can be calculated through integration.

Distance to stop

The distance-to-constant-speed calculation can easily be used for calculating the distance to stop. Knowing the distance required for stopping (dts), we can reduce the distance to the goal by that amount. Doing so gives us the latest point at which a stopping sequence needs to be initiated \(x_{\text{stop}}\).

Desired Speed

Until we reach this point we try to reach maximum speed as quickly as possible. While the motion state accelerates, distance to stop is elongated and the point at which the deceleration sequence needs to start moves towards the current axis position (since the goal is located at \(x = 0\), the modulus of \(x_{\text{stop}}\) grows). To prevent overshooting, we reduce the target velocity already shortly before reaching the deceleration point \(x_{\text{stop}}\).
5.3 Low-Level Hardware Controller

**Figure 5.5**: Point-to-point move from −50 mm to 50 mm. Position, Velocity and acceleration profile are depicted. At approximately \( t = 0.4 \) s, the position \( x \) reaches \( x_{\text{stop}} \). Up to this point, the algorithm tries to achieve \( v_{\text{max}} \) as quickly as possible. It never does, and the strategy is aborted. After reaching \( x_{\text{stop}} \), a full stop at \( x = 50 \) mm is approached. In general, the three-phase strategy described in section 5.3.6 is applied.

5.3.7 Update Step

With the desired speed determined, we completely update the transformed motion state using the strategy that is used in the distance to constant speed calculation. After that, the motion state is transformed back to the global coordinate space and from there to the actuator space. The actuator-space motion speed is then fed into PID controllers that are regulating the motor amplifiers. Figure 5.5 shows acceleration, velocity and position profiles for a point-to-point move. At the starting and target position the robot is in standstill. The move consists of five phases. In the first two, the desired velocity is \( v_{\text{max}} \). At \( t = 0.4 \) s, the axis has reached \( x_{\text{stop}} \) and the desired speed changes to zero. Since we initiate the stopping sequence already shortly before reaching \( x_{\text{stop}} \), the motion does not exactly follow the strategy described above. This can be seen particularly well towards the end of the acceleration figure.\(^3\)

---

\(^3\) As the movement slows down, the distance to stop gets shorter and the planner does not apply maximum deceleration. This would not occur if the stopping sequence would be initiated at exactly the right spot. However due to rounding errors, etc. some safety margin is indicated.
5 System Components

![Wafer Holding and Heating Device](image)

**Figure 5.6:** Wafer holding and heating device with wafer mounted. A wafer has been placed on the table. The heater control electronics are to the right of the heating table.

![Temperature Graph](image)

**Figure 5.7:** Wafer table heat-up. The target temperature is 80 °C.

5.4 Wafer Table

During assembly the wafer is placed on a table. This table fulfills two functions: firmly holding the wafer in place and heating of the wafer.

5.4.1 Heating

The heater can deliver 200 W and has a maximum operating temperature of 300 °C. The heater consists of a heating disc (DBK HT03) and a custom control unit. The heating disc operates on mains power.

The heater control unit is build around *Microchip PIC18F14K50* 8-bit microcontroller. Since the thermal capacitance of the table is quite high, processing speed is not an issue. Heating power is regulated through a galvanically separated phase-fired controller (PFC). The wafer table’s heater controller is connected to the I²C peripherals network (section 5.3.4). Heat-up is rather slow, but once the target temperature is reached, very consistent (fig. 5.7).
Table 5.1: Values chosen for determining the NTC parameters

<table>
<thead>
<tr>
<th>T/°C</th>
<th>R/Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>29287</td>
</tr>
<tr>
<td>25</td>
<td>10000</td>
</tr>
<tr>
<td>100</td>
<td>868.37</td>
</tr>
<tr>
<td>140</td>
<td>329.98</td>
</tr>
</tbody>
</table>

Table 5.2: Equation (5.23) constants obtained for the sensor used

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_0$</td>
<td>$9.114 640 93 \times 10^{-4}$</td>
</tr>
<tr>
<td>$A_1$</td>
<td>$2.580 338 75 \times 10^{-4}$</td>
</tr>
<tr>
<td>$A_2$</td>
<td>$-3.090 185 54 \times 10^{-7}$</td>
</tr>
<tr>
<td>$A_3$</td>
<td>$1.179 888 96 \times 10^{-7}$</td>
</tr>
</tbody>
</table>

Temperature Measurement

Temperature feedback is provided by a negative-temperature-coefficient (NTC) thermistor (Becker, Green, and Pearson, 1946) that is inserted into a vertical channel reaching into the table. The model used is an Epcos B57560G1103F005.

The resistance $R_T$ of NTCs at a temperature $T$ follows the equation

$$ R_T = R_R \cdot e^{B \left( \frac{1}{T} - \frac{1}{T_R} \right)} $$

with $R_R$ being the rated resistance, $T_R$ being the rated temperature, and $B$ being an NTC specific constant (Epcos, 2009b). As an approximation we have used a modified version of the Steinhart-Hart equation (Stehnhart and S. R. Hart, 1968) to calculate the temperature ($T$) of the thermistor

$$ \frac{1}{T} = A_0 + \sum_{i=1}^{3} A_i \cdot (\ln R_T)^i. $$

From the thermistor’s data-sheet (Epcos, 2009a) we have obtained pairs of $R_T$ and $T$ for various temperatures (table 5.1). We have selected values that cover the range of interest for our application. From these we obtain the constants $A_0$ through $A_3$; they are listed in table 5.2.

The resistance is measured using the internal analog-to-digital converter (ADC) of the microcontroller. To prevent the interconnect from influencing the measured value four-wire Kelvin resistance measurement is employed. To increase accuracy the measurement is oversampled 64 times.
5.4.2 Holding

Groves around the table surface are connected to the vacuum system (fig. 5.8). When the vacuum is applied, the wafer is firmly held in place. Since both the wafer and the table are flat, no additional sealing is required. A thin rim and notch serve as alignment help. They do not extend beyond the height of the mounted wafer as they would otherwise interfere with the substrate during mounting.

5.5 Substrate Holders

The robotic manipulator moves the substrates, and later the substrates with the chips attached, from one place to another. For this purpose there are substrate holders attached to the end-effector of the robot. Apart from holding the substrates, the holders provide an electrical connection to the heaters inside the substrate. They also feature retractable vacuum needles that lift the chips out of the wafer (see section 3.2, section 4.3.5, and, in particular, fig. 4.8).

The three holders required for our application are placed along a straight line (see fig. 5.9). The distance between the holders is adjustable to accommodate for different wafer layouts. To hold the substrates firmly in place each substrate holder is equipped with a rubber suction cup.

Figure 5.8: CAD rendering of the wafer table vacuum groves and channels. The tabletop is transparent in this rendering.
5.5 Substrate Holders

Figure 5.9: Substrate holders. The eccentric is marked orange; the motor driving it is black. The vacuum connections for substrate holding and suction pipes are marked yellow and blue, respectively.

5.5.1 Retractable Suction Needles

The suction needles are mounted on a linear slide. They have an inner diameter of 450 μm and an outer diameter of 600 μm. The retraction movement is provided by an elongated eccentric. A single eccentric is used for the three individual holders. A geared 8 mm motor drives the eccentric.

A spring pushes an arm attached to the linear slide against the eccentric. The spring also ensures compliance of the suction needles as they are pressed against the chip during pickup. The precise height of the vacuum needles can be set using an adjusting screw. Since the needles reach through the substrate during the first part of the assembly process, they also serve as additional substrate alignment pins.

5.5.2 Substrate Heating

Heating for regular flip-chip soldering is commonly achieved by heating the chip-handling probe and/or substrate chuck (i.e., in our case the substrate holders). Heating the chip in this way restrains free motion of the chip and inhibits self-alignment of the chip to the substrate. Alternatively, the complete system is often heated in a furnace.

We have developed a method that heats the substrate locally at the desired spot while precisely controlling the temperature. This is achieved by embedding a Joule
heater into the substrate. Additional sensors are not required because the change of the resistance of the heating, which reflects the change in temperature, is closely monitored. Because the temperature is determined inside the substrate it provides accurate feedback of the solder’s temperature. Since the heating is integrated into the substrate, it does not interfere with other components. The heater is described in detail in chapter 6.

The in-substrate heater requires electrical connections for both heating and temperature sensing. These are provided by the substrate holders. A connector placed on the individual substrates is connected to its counterpart that is embedded into the substrate holder.

5.6 Vacuum

Various parts of the system rely on vacuum for holding or fixating components. A small pump is providing a vacuum of −87 kPa relative to atmospheric pressure for the process. A total of seven valves controls the vacuum at:

- the wafer holding and preheating table
- each of the three substrate holders
- each of the three pairs of needles used to separate the MEMS chips form the wafer.

The vacuum valves are controlled by digital outputs of the low-level controller.
5.7 Cameras

Our system uses two identical cameras (IDS UI-1226-LE-M), one for finding the alignment marks of the wafer and one for recording the MEMS chip self-alignment. They are connected to the process controller using an USB. The cameras have been equipped with a custom lighting system consisting of a ring of eight LEDs each. The LEDs are driven by a small custom interface board that is connected to the camera's internal I²C-bus. This way we can control the individual brightness of each LED from our camera drivers. A simple light-guide leads the light to desired spot (fig. 5.11). The LEDs are powered through the cameras USB connection. To stay within the camera's 150 mA current budget, the interface board is designed to be highly efficient.

5.8 Process control

The process control software runs on an “off-the-shelf” Personal Computer. The software consists of several interacting modules. The program is written in the Python programming language (Rossum, 2012) and relies heavily on the Qt toolkit (Qt library 4.8 Documentation 2012) for displaying GUI elements and inter-module communication. For accessing the Qt library from Python, the PyQt4 bindings are used (PyQt 4.9.5 Reference Guide n.d.).
5 System Components

Figure 5.12: Screenshot of the process controller GUI while soldering.

5.8.1 Graphical User Interface

The operator interacts with a GUI that is part of the process controller program. The GUI reflects the modular structure of the control software (fig. 5.12). Most of the implemented modules are not required for regular operation. The central module of the GUI is the wafer display.

5.8.2 Wafer display

The wafer display is generated from the MEMS chip coordinates supplied by the MEMS manufacturer. Given the coordinates a picture is dynamically generated. Furthermore confirmation of the state of each MEMS chip is incorporated. Possible states are: empty for chips that have already been removed from the wafer, broken for those chips that have been detected to be malfunctioning in KGD testing, and finally present for chips available to packaging. The operator can select which chips are to be assembled next. In the wafer display in fig. 5.12 (bottom center) broken chips are marked red, empty positions in the wafer are white.
6 Substrate Heating

6.1 Introduction

Solder-bump-based flip-chip processes such as Parallel C4 require temporary melting of the solder alloy. After cooling, a solid connection between substrate and chip is formed. Depending on the application, a desired feature of the C4 process is the fact that the chip will self-align to the substrate if allowed. The self-alignment is brought about by the surface forces of the liquid solder. (L. F. Miller, 1969b)

In general, flip-chip applications impose the restriction that the electrical connections are physically inaccessible in the assembled state. Consequently, the connections must be heated indirectly by heating the chip, the substrate, or both.

This chapter focuses on the heating process. To ensure reliable connections, precise control of the soldering temperature profile is often required. Short heating times are desired to reduce oxidation (Kuhmann et al., 1998), phase formation (Pahl et al., 2001) and, depending on the application, the risk of damaging the device. However, a certain time above liquidus is required to ensure sufficient wetting, to guarantee the formation of an appropriate intermetallic layer, and to prevent flux entrapment.

Furthermore, the appropriate distribution of heat is of critical importance. The required temperature must be reached for all contact pads but should not be excessively exceeded anywhere. Finally, the heating system should impose as few restrictions on the design of the device as possible. It should not cause contamination of the assembly, and both the equipment cost and the variable costs should be as low as possible.

We present a method that fulfills the above criteria. A Joule heater is embedded into the substrate. It provides rapid and local application of heat at the land location. Since common substrate manufacturing techniques can be used for the production of the heater, this process introduces little or no variable costs. Our heater provides temperature feedback, allowing for the heat to be applied in a closed loop fash-
ion enabling tight temperature control and steep heating rates. The temperature feedback requires no additional sensor. Finally, due to the small thermal mass that is heated, the method is highly energy efficient.

6.1.1 State of the Art

Heating methods for flip chip can be categorized as those that selectively heat a specific area of the substrate and those that heat the complete substrate. While this chapter focuses on the former case, we will briefly present a nonlocal heating method since its use is widespread. The heat transport mechanism employed can have far-reaching implications on the process. Conductive heating methods generally restrain the self-alignment feature of the C4 process.

Most commercial flip-chip bonders provide a mechanism to control the temperature of both the chip handling tool and the substrate chuck. Often, a combination of radiant heating and nitrogen cooling of the handling tool and chuck is used to ensure homogeneous heating as well as tight control of heating and cooling rates (Pahl et al., 2001; Meyen et al., 1979). Since the handling tool conductively heats the chip, its free motion is inhibited. The molten solder cannot self-align the chip to the substrate pads.

Another common method is reflow soldering the chip to the substrate after the chip has been loosely placed. Here, varying compositions of radiant and convection heating are often employed (Zarrow, 1988). Alternatively pure radiant heating (Mayer, Paul, and Baltes, 1997) or pure convection heating is often employed as originally proposed by L. F. Miller (1969a) in his C4 patent. Reflow soldering methods offer no spatial control of the heating but achieve largely homogeneous heat distribution given sufficient heat exposure durations (Mahaney, 1993). The components are typically exposed to high temperatures (typically 20°C to 40°C above the solder’s melting point) for a longer duration (on the order of several minutes) compared with other methods. Since reflow soldering generally does not feature local temperature measurement, it relies on empirical methods for achieving the desired soldering temperatures in all places. An extended heat exposure duration is required to ensure that all components reach the necessary temperatures.

By transmitting the heat via a laser beam, heat can be precisely applied locally. The laser is pointed at the contact pads through a translucent substrate. In (Kordás
et al., 2006), it is stressed that pointing the laser beam through the component is not an option because the beam would be scattered by the metal patterns. Hurtony, Balogh, and Gordon (2009) use a laser to heat the chip.\footnote{Hurtony, Balogh, and Gordon (2009) tried pointing a laser through translucent substrate but found that heating the chip gave better results.} Apart from the difficulty of conveying the laser to the correct spot, the high cost is a major disadvantage of laser soldering.

A method relying on ultrasonic vibration to generate the required heat is presented in (J. H. Kim, J. Lee, and Yoo, 2005). Since the chip is subjected to both pressure and acceleration, this method is infeasible for many MEMS applications. Furthermore, the pressure causes local deformation of organic substrates.

Another local approach is induction heating, in which an eddy current is induced in the solder. Due to the resistance of the solder alloy, it is Joule-heated. The amount of heat generated in an individual solder ball is highly dependent on the solder volume; small volumes create little heat. Induction heating is one of the few methods that do not make use of a heat transport mechanism to apply heat to the solder. (Li et al., 2008)

A localized heating method for polymer MEMS packaging based on resistive (Joule) heating has been presented by Su and Liwei Lin (2005). Micro-heaters made from aluminum thin films are either permanently or temporarily placed between or onto the components that are to be bonded. The microheaters are heated for 0.25 s. In (Cheng, Liwei Lin, and Najafi, 2000) a similar approach is applied for silicon-to-glass fusion bonding and silicon-to-gold eutectic bonding. The change in resistance of the heater material is used for calculating the local temperature.

### 6.1.2 System in Package

This chapter presents a heating method that is especially relevant for solder-bump flip-chip bonding of system-in-package modules. SiP modules combine several chips or components in a single package. These modules are not necessarily assembled at the same time or even using the same process. The high temperatures required during C4 can adversely affect sensitive components or connections created during previous assembly steps (see section 2.1.4).
It can be important that not all parts of the package are exposed to the same amount of heating. Instead, selectively heating the chips can be preferred. However, the different parts on the module are closely spaced. The risk of a conductive heating system to physically interfere with other parts on the module is high.

Our application is a case where selective heating is desired, but conductive methods would likely interfere with components already mounted on the substrate. Therefore, we would have chosen one of the radiant heating methods. However that would have implied that we have to enclose our setup to protect users from eyesight-damaging radiation. We saw this as a major restriction for our test setup where we expected frequent operator interaction.

6.1.3 General Approach to Localized Closed-Loop Heating

Our heating method integrates heating as well as temperature sensing into the substrate. Both functions are achieved by a single wire that can be produced in the same manner that is routinely employed for providing electrical connections on substrates. The heat is conducted by the substrate to the land location. Our heating and sensing method is similar to those employed by (Su and Liwei Lin, 2005; Cheng, Liwei Lin, and Najafi, 2000) where the heating is embedded in a polymer or silicon dioxide. The heating systems presented there are not used to heat electrical contact pads and can, therefore, be placed at the surface of the substrate. To prevent shorting, our Joule heater must be separated by a dielectric from the contact pads it is meant to heat. The heater is placed underneath the pads. Furthermore, instead of solely using the temperature feedback for monitoring, we use it to create a high-frequency feedback loop. The heating is, therefore, conducted in a closed-loop, temperature-controlled fashion.

Our heating method provides localized, temperature-controlled, and fast heating. It imposes little restrictions on device design, consists of low-cost compact equipment, and is energy efficient.

6.2 Principle of Operation

Our approach consists of three parts: heating, temperature monitoring, and control. The heating is implemented using a Joule heater with the heating elements
embedded into the substrate. The temperature-dependent change of resistance of these heating elements is analyzed to monitor the temperature. If no reference resistance/temperature combination is known, this monitoring method only provides differential measurements. A second method then must be employed to obtain the reference point for the differential readings.

Control is provided by electronics separate from the substrate. Since the heating is embedded, the substrate must carry some form of (temporary) electrical junction that can be connected to the control electronics. In the FemtoTools force sensor application, a connector on the PCB is inserted into the substrate holder (see also section 5.5.2). This connector is later reused for regular sensor operation.

6.2.1 Heating

A wire with resistance $R_h$ is embedded into the substrate. Since the energy converted into heat is proportional to the resistance of the wire ($P = I_h^2 \cdot R_h$), it is desirable to maximize the wire’s resistance ($R_h$). The resistance of the wire is dependent on the specific resistance of its material ($\rho$), the length of the wire ($l$), and the wire’s cross sectional area ($A$)

$$R_h = \rho \cdot \frac{l}{A}. \tag{6.1}$$

To minimize costs, a material is used that is already employed in the substrate’s electrical connection. Therefore, we are limited to minimizing the wire cross section ($A$) and maximizing the length of the wire ($l$) (i.e., by laying out the wire in tight meanders).

6.2.2 Continuous Temperature Monitoring

The specific resistance ($\rho$) of metals typically varies with temperature ($T$). Here, this effect is used to determine the temperature of the heating wire. This way, the need for a separate temperature sensor is avoided.\(^2\)

For a limited temperature range, the temperature dependence of the specific

---

\(^2\) We assume that the temperature is homogeneous along the heating wire. This is the case as long as the wire cross section is fairly constant and the wire is a good thermal conductor.
resistance can be approximated by
\[ \rho(T) = \rho(T_0) \left(1 + \alpha(T - T_0)\right) \] (6.2)

where \( T_0 \) is an arbitrarily chosen reference temperature and \( \alpha \) is the material-dependant temperature coefficient of electrical resistance. Simultaneously, the material of the wire expands (again approximately) according to
\[ l(T) = l(T_0) \left(1 + a(T - T_0)\right) \] (6.3)

where \( a \) is the temperature coefficient of linear expansion. The above applies both to the expansion in the direction of the wire (length \( l \)) as well as to the expansion of the conductor cross section (\( A \)) in squared form.\(^3\) We assume that \( l \) and \( A \) are unknown, due to manufacturing variations. By combining eqs. (6.2) and (6.3) with eq. (6.1) we obtain the temperature dependence for the resistance of the wire (\( R_h \)) as
\[ R_h(T) = R_h(T_0) \frac{1 + \alpha(T - T_0)}{1 + a(T - T_0)}. \] (6.4)

This leads us to the temperature as a function of resistance
\[ T(R_h) = T_0 + \frac{R_h - R_{h,0}}{\alpha R_{h,0} - a R_h} \quad \text{with} \quad R_{h,0} = R_h(T_0). \] (6.5)

6.2.3 Initial Temperature Measurement

It must be assumed that the wires inside the substrate are subject to manufacturing variations that result in the resistance of the heating wire to differ between parts. Therefore, it is necessary to individually determine the initial resistance of the heating wire (\( R_{h,0} \)) at a known temperature \( T_0 \).

If it cannot be guaranteed that the devices arrive at the assembly machine with a specific temperature, \( T_0 \) has to be measured individually, as well. An infrared thermometer calibrated to the emissivity of the substrate provides almost instant surface temperature readings.

Measuring the initial resistance (\( R_{h,0} \)) can be done using the same equipment that is already required during the continuous temperature measurement.

---

\(^3\) The adjoining substrate material has the same temperature as the wire. In the case of FR-4, it
Figure 6.1: Optical micrograph of the substrate. At the top of the picture we can see the heating wire meander shining through the epoxy resin. The heating meanders are roughly placed around the landing location of the chip to ensure a more even heating. The land location can be recognized by seven contact pads.

Table 6.1: Material constants in our application

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical resistance coefficient</td>
<td>$a_{\text{Cu}}$</td>
</tr>
<tr>
<td>Linear expansion coefficient</td>
<td>$a_{\text{Cu}}$</td>
</tr>
<tr>
<td>Emissivity of FR-4</td>
<td>$\varepsilon_{\text{FR-4}}$</td>
</tr>
<tr>
<td>Approximate resistance of heating</td>
<td>$R_h(T = 25 \degree C)$</td>
</tr>
</tbody>
</table>

6.3 Implementation and Application

In our application the substrate is an organic four-layer FR-4 PCB. The PCB is 1.57 mm thick. The copper heating wire is part of the two interior layers of the substrate (see fig. 6.1). Table 6.1 lists the relevant material properties. At a temperature of 25 $\degree$C the wire has a resistance of approximately 450 m$\Omega$. Copper’s temperature coefficient of electrical resistance ($a_{\text{Cu}}$) is much larger than copper’s coefficient of thermal expansion ($a_{\text{Cu}}$). Therefore, we can neglect the effect of $a_{\text{Cu}}$ and use a simplified form of eq. (6.5) to calculate the temperature:

$$T(R_h) \approx T_o + \frac{R_h - R_{h,0}}{aR_{h,0}}.$$

also has a similar coefficient of thermal expansion (table 2.2). The stress generated inside the substrate is similar to that of established methods such as hand soldering.

4 This allows us to change the division by $aR_{h,0} - aR_h$ into a multiplication by $\frac{1}{aR_{h,0}}$. $R_h$ is constant for each substrate (while it is connected to the controller electronics). This significantly reduces the computation demands of our algorithm (see section 6.3.3).
Figure 6.2: Cross section of sample # 37 reflowed using our heater. The FT-S260 MEMS chip (bottom) has been attached to the FR-4 substrate (top). Three heating wire cross sections can be seen inside the substrate. Between substrate and chip three C4 joints are depicted. Eutectic 58Bi–42Sn solder (Indalloy 281 in Indium 5.7LT solder paste) has been used.

Figure 6.3: The infrared thermometer array (black pipes) is measuring the reference temperatures $T_o$ of three substrates held by the substrate holders.
We mostly use Indium 5.5L T low-temperature solder paste containing Indalloy 42 (eutectic 46Bi-34Sn-20Pb, melting point 96 °C) for the work leading to this thesis (see section 4.2.1). For the tests presented in section 6.4, typical temperatures suitable for the more commonly used eutectic tin–bismuth solder (melting point: 138 °C) were chosen. The low melting point and ductile nature of both of these solders help to reduce stress in C4 applications. In our packaging application, seven 380 µm × 380 µm pads with a minimum pitch of 400 µm are bonded. A cross section of an assembled device is depicted in fig. 6.2. For the initial reference temperature ($T_0$) measurement we use three Melexis MLX90614 infrared thermometers (10° field of view, 5.5 µm to 14 µm optical filter, see fig. 6.3).

Custom electronics were designed to provide the closed-loop heating solution. It is beneficial to place the electronics as close as possible to the point of assembly. Since in parallel C4 the substrate is moved instead of the chip, the electronics had to be placed on the end effector of the robotic manipulator. This requires a compact and lightweight design. Figure 6.4 shows a stack of three heating controller boards placed upon the robotic manipulator. Figure 6.5 depicts simplified schematics of the electronics and the relevant part of the substrate. The substrate exposes junctions that are electrically linked to the heating. These can be connected to the control electronics.
**Figure 6.5:** Simplified schematics. Both the potential over \( R_i \) and \( R_h \) are measured using the four-wire Kelvin method. The values are amplified (in. amp.) and digitized (ADC) to be then processed by a microcontroller (\( \mu \)C). The microcontroller controls the output of the current source (\( I_h \)).

**Figure 6.6:** Simplified controller diagram. Initially, the infrared sensor is used to set \( \Delta T' = \tilde{T} - \Delta T_o \) (dash-dotted control loop). Once the infrared sensor is no longer pointing at the substrate, \( \Delta T \) is the set-point for the temperature regulator. The regulator outputs the desired heating current (\( \tilde{I}_h \)) which is fed to the current regulator. The heating current (\( I_h \)) and voltage drop over the wire (\( U_h \)) are used to calculate the wire resistance (\( R_h \)) and the temperature difference (\( \Delta T \)) in relation to \( T_o \).
6.3 Implementation and Application

Table 6.2: Measurement resolution for voltage (a) and current (b) digitalization

<table>
<thead>
<tr>
<th>a) Range (V)</th>
<th>Res. (mV)</th>
<th>b) Range (A)</th>
<th>Res. (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>0.0366</td>
<td>0.0</td>
<td>0.0916</td>
</tr>
<tr>
<td>0.4125 ... 1.0501</td>
<td>0.0732</td>
<td>1.0313 ... 2.6252</td>
<td>0.1831</td>
</tr>
<tr>
<td>0.8438 ... 2.6252</td>
<td>0.1831</td>
<td>2.1095 ... 6.5629</td>
<td>0.4578</td>
</tr>
<tr>
<td>2.0626 ... 6.0</td>
<td>0.3662</td>
<td>5.1566 ... 15.0</td>
<td>0.9156</td>
</tr>
</tbody>
</table>

6.3.1 Measurement of Heating Current and Wire Resistance

To calculate the resistance of the heating wire, both the current flowing through the wire \(I_h\) as well as the voltage drop \(U_h\) over the wire \(R_h\) must be measured. To obtain accurate values, a Kelvin measurement setup is used. The precision resistor \(R_I\) in fig. 6.5 is used to determine the current flowing through the heating. The heating voltage drop \(U_h\) is measured on the substrate to ensure that the voltage drops of the connecting wires are not taken into account.

The potentials over \(R_h\) and \(R_I\) are then amplified by instrumentation amplifiers. The voltage over \(R_I\) needs stronger amplification because a small sensing resistor is chosen to prevent it from heating up. The amplified values are then digitized by analog-to-digital converters (ADCs). The sampling of both values takes place at exactly the same time. The conversion results are fed to a microcontroller (μC).

Measurement Resolution

Since the heating current \(I_h\) varies with the amount of heating applied, the amplification of the instrumentation amplifiers can be varied to guarantee good measurement resolution over a wide range of currents (see table 6.2).

Temperature Measurement When Not Heating

When the heating is not active, no current \(I_h\) flows, and, therefore, the resistance \(R_h\), and, thus, temperature \(\Delta T\) cannot be determined. To overcome this limitation, short current pulses are used to periodically determine the current value of \(R_h\).
The pulses are set to a duration and frequency that ensure negligible heating (less than 2 mW average power for the tested device).

### 6.3.2 Heating Power Regulation

In our application, the amount of heat generated is controlled by a regulated current source. It provides a heating current \( I_h \) in the range of 0 A to 5 A at a voltage \( U_S \) of up to 5 V. This creates a maximal total heating power of 25 W depending on the resistance of the heating wire \( R_h \). In the test application, a maximum of 17.1 W was achieved.

Because of the relatively large current required, a switching rather than a linear current regulation was chosen.\(^5\) While leading to more complex electronics, this has the advantage of drastically reducing energy losses and, by removing the need for heat sinks, reducing weight. This in turn is beneficial when attaching the control electronics onto the actuator, close to the substrate.

Directly driving the heater using the switched signal would lead to high levels of *electromagnetic interference* (EMI) with the wires between substrate and electronics acting as antennas. Therefore, a synchronous buck converter setup that uses inductors and capacitors to smoothen the output is employed.

### 6.3.3 Heating Control

Control is entirely digital. We employ a Microchip **PIC18F26150** 8-bit microcontroller operating at 48 MHz for all calculations. The microcontroller’s processing power places constraints on the control algorithm that can be implemented. (See table 6.3 for the processing time various operations require.) An upgrade to a faster microcontroller will allow increased performance both in terms of temperature accuracy and in terms of heating rate. The heating controller is part of our peripherals network (section 5.3.4).

Control of the heating is realized in two nested control loops (see fig. 6.6). The inner loop takes care of regulating the current running through the heating wire, while the outer loop regulates the temperature of the wire. Additionally, an infrared

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\(^5\) The current source is regulated with 7 bit resolution at 375 kHz pulse-width modulation (PWM) frequency.
### Table 6.3: PIC 18F26J50 microcontroller timing (HiTech C version 9.80, 48 MHz)

<table>
<thead>
<tr>
<th>Description</th>
<th>Duration / µs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>General</strong></td>
<td></td>
</tr>
<tr>
<td>LED on–off–on</td>
<td>0.13</td>
</tr>
<tr>
<td>Temperature from resistance</td>
<td>327.41</td>
</tr>
<tr>
<td>Temperature from $1/R$</td>
<td>159.21</td>
</tr>
<tr>
<td>ADC launch</td>
<td>1.42</td>
</tr>
<tr>
<td>ADC readout</td>
<td>1.95</td>
</tr>
<tr>
<td>Data conversion (&quot;measure_convert()&quot;)</td>
<td>236.33</td>
</tr>
<tr>
<td>State-machine disconnected</td>
<td>14.98</td>
</tr>
<tr>
<td>State-machine connected</td>
<td></td>
</tr>
<tr>
<td>- Current controller</td>
<td>350.00</td>
</tr>
<tr>
<td>- Temperature controller</td>
<td>435.00</td>
</tr>
<tr>
<td><strong>Floating Point</strong></td>
<td></td>
</tr>
<tr>
<td>Get through function call</td>
<td>2.83</td>
</tr>
<tr>
<td>Assignment</td>
<td>0.61</td>
</tr>
<tr>
<td>Constant Subtraction (in place &quot;− =&quot;)</td>
<td>63.65</td>
</tr>
<tr>
<td>Multiplication (in place &quot;* =&quot;)</td>
<td>108.48</td>
</tr>
<tr>
<td>Division (in place &quot;/ =&quot;)</td>
<td>159.67</td>
</tr>
</tbody>
</table>
sensor measures $T_o$ which is the reference temperature linked to $R_{h,o}$. Once $T_o$ has been determined, the infrared sensor is removed from the control loop. The current control loop runs at 500 Hz while the temperature control loop runs at 100 Hz.

There is a short propagation delay between the heating wire reaching a certain temperature and the heat spreading to the solder pads on the substrate’s surface. That delay is not relevant to the control loop, as the temperature of the heating wire can be measured with virtually no delay.

6.4 Results

6.4.1 Temperature Measurement Accuracy

We first analyze the temperature monitoring accuracy because the later sections build on that. The measurement noise is nearly normally distributed (fig. 6.7). The standard deviation is dependent on the output power. It decreases from about 1°C at 45 mW to about 0.5°C at 1.3 W output power. As previously described in section 6.2.3 an initial resistance ($R_{h,o}$) measurement is carried out to calibrate the heating for an individual heating wire. This measurement determines the relationship between $R_{h,o}$ and the reference temperature $T_o$. It is affected by the same noise as subsequent regular measurements. The error for the reference resistance $R_{h,o}$ biases all temperature measurements based on it. To minimize this bias, the reference resistance is measured using short high-current spikes (see section 6.3.1)
so that the temperature error introduced by it also has a standard deviation of 0.5 °C. The added standard deviation of the reference point and individual (high-power) measurements amounts to approximately 0.7 °C. We can deduce that 99.99% of temperature measurements have an error due to measurements noise of less than 2.72 °C.

The above analysis is purely based on the measurement noise. Additionally, we have compared the temperatures calculated from the change in heating wire resistance to the surface temperature of the substrate by means of one of our infrared thermometers (see fig. 6.8). To ensure constant emissivity ($\epsilon_{FR4}$), temperature measurements were conducted without actually assembling a chip to the heated
substrate. There is excellent agreement between the calculated temperatures and those measured by the infrared thermometer as long as the temperature is fairly stable. The deviation is 2°C over a temperature range of 140°C. This error can be attributed to inexact material constants. In particular, the emissivity of the substrate has not been measured exactly but obtained from the literature (Mahaney, 1993). Another cause for a slight temperature drop is convection and emission of heat on the substrate surface.

### 6.4.2 Heating Speed

Heating up to 164°C (a temperature suitable for eutectic tin-bismuth solder) takes about 5 s for the tested substrates (fig. 6.8 and fig. 6.9). As noted before, we observe close correlation of the surface temperature of the substrate and the temperature of the heating wire in fig. 6.8. Large temporal temperature gradients at the Joule heating are damped while the heat is diffused to the surface (see $t = [0, 5] \text{s}$ in fig. 6.8). The conductive heat flow is proportional to the spatial temperature gradient. The local temperature at the heating wires intentionally overshoots to help fast heating of the surface by maintaining a gradient while the surface temperature approaches the desired temperature. Care must be taken to give the heater enough time to spread and prevent burning of the substrate directly at the heating wires.

When the heater is turned off (at 20 s in fig. 6.8), the temperature decays exponentially to ambient temperature following Newton’s law of cooling.

While fig. 6.9 may suggest otherwise, the maximum power is applied from $t = 0.27 \text{s}$ to $t = 1.465 \text{s}$. It is limited by the current output of 5 A. However, as the resistance $R_h$ increases due to heating, the output voltage and power increase ($P = I_h^2 \cdot R_h$). For the given substrate and electronics, improved heating times can be achieved only by a larger overshoot of the wire temperature or slightly quicker initial heating.

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6 The differential temperature profile measured inside the substrate ($\Delta T(t)$) is not noticeably affected when a 6.36 μg MEMS chip is being bonded. This is due to the chip’s small heat capacity and the diminutive increase in heat transferring surface area.

7 When the temperature changes quickly, the heat conductance from the inside to the outside of the substrate takes a certain amount of time, causing differences in temperature. See also section 6.4.2.
Figure 6.9: Temperature and power versus time ($t$). Again, the desired temperature difference is set to $\Delta T = 140 \, ^{\circ}C$ at $t = 0$. Initially high power heats up the device. But already after 1.465 s the power can be successively reduced to 2 W to keep the temperature at a steady level of 140 \, ^{\circ}C.
We have also tested heating to 265°C to verify the applicability for the widely used tin-silver-copper (SAC) solders. In this case, heating up takes about 7.5 s.

6.4.3 Surface Temperature Distribution

Figure 6.10 displays the heat distribution at the substrate surface (without a chip attached). The area where the meanders are located (see fig. 6.1) is fairly evenly heated with a maximum variation of about 5 °C. Outside of this area, the temperature decays roughly exponentially toward ambient temperature. Approximately 5 mm from the heater, the temperature difference is halved. Optical analysis has shown negligible warpage of the substrate due to the local heating.

6.5 Conclusion

We presented a heating method that is spatially selective, tightly temperature controlled, and fast. We also provided testing results verifying the viability of our approach.

Using our method, the chip’s free movement is in no way impeded by the heater, thus permitting self-alignment of chip and substrate. Access to the chip remains unobstructed, allowing for online visual inspection of such an alignment procedure. This allows us to track the alignment of the MEMS chips to the substrate. The unobstructed access also allows for online infrared temperature measurements. Furthermore, the apparatus does not need to be enclosed in a safety housing to protect the operator from (infrared) radiation. The heating takes up no space except for the control electronics that can be freely placed within reasonable limits. Subsequently, the heating can easily be integrated into other process steps. Also, since it cannot physically interfere with other parts, the heating system does not impose any restrictions on component placement.

While the application of heat is not as selective as it is when applied by a laser, we demonstrated that the spatial distribution is fairly isolated. Using thinner substrates will lead to even more selective heating as well as smaller differences between surface temperature and heating temperature. Furthermore, if required, the precision can be increased by reducing the conductivity of the substrate by adding holes.

Our method provides tight temperature control and very low heat propagation
Figure 6.10: Temperature distribution on the substrate surface. The circles to the left of the substrate mark the contact pads that will be connected to the MEMS chip (see also fig. 6.1). The image was captured with an SDS Infrared Hotfind D camera. Above the infrared photograph of the substrate, the temperature profile along the axis laid onto the photograph is depicted. The photograph and plot are aligned.
delay. This offers room for reduction of the time and temperature above liquidus. Further research will be required to determine how far we can reduce the temperature as well as time above liquidus without impacting solder connection reliability. The rapid heating and fairly short heat exposure time decrease oxidation and inter-metallic phase formation. Furthermore, combined with the limited extent of the high-temperature area, it reduces the risk of damaging adjacent components.

Compared to other methods, the maximum heating temperature is minimally reduced if the substrate material constitutes the limiting factor. This is because the temperature inside the substrate is slightly higher than that at the solder connection. In practice, this will not impose a restriction. The size and number of connections per chip is not inherently limited. In fact, more and larger connections will provide better heat transport to the chip’s pads. The amount of power available may need to be increased for large chips. This can easily be achieved by revising the control electronics. Higher heating power and a faster microcontroller will also allow for even steeper heating curves. Using multiple sets of control electronics, it is possible to heat several substrate regions simultaneously.

Rapid heating is achieved at low energy input. This leads to favorable operating costs and low environmental impact. Further cost savings are offered by the much lower equipment costs compared with other selective heating solutions. Our method can be used to reheat the solder connection should rework be required.

Currently, our implementation suffers from the limited processing power of the microcontroller. By upgrading the microcontroller and incorporating some other modifications to the control electronics, it will be possible to achieve even faster heating, more precise temperature measurement and control at reduced weight of the control electronics. Given these upgrades the heating power that can be induced into the substrate is limited only by the substrate's ability to diffuse the heat without starting to burn. Owing to the online temperature measurement the system can be safely be operated close to this point.

Our approach may prove interesting not only for the application at hand but for other applications as well. For example, in adhesive flip-chip applications it can be beneficial to use this method for thermal polymer curing when UV curing is difficult to apply.

Fluxless soldering is of special interest for MEMS applications featuring miniature structures which are destroyed or rendered useless by liquids (such as, e.g., comb
drives). Both the flux itself and flux removal solutions can destroy such devices (see section 3.4). Steeper heating rates lead to reduced oxidation. Given a heat-up time of below 5 s it is possible to perform fluxless soldering in air after PADS pretreatment of the solder (Koopman, Bobbio, et al., 1993). Our method can provide the required heating rate and may thus find application in these settings. For solders with melting points beyond around 140 °C the control electronic implementation would need to be revised to provide the required output power.

Our heating method is most suited for applications where free motion of the chip, tight temperature control, unobstructed access to the chip, easy integration, the ability to rework, close spacing of components, careful handling of the chip, selective or rapid application of heat are major concerns. These requirements are common to but not limited to S1Ps. Our approach offers the additional benefit of low cost and low energy consumption and thus small environmental impact.
7 Modeling of Chip Alignment Motion

The literature contains several similar models that try to predict the dynamics of solder self-alignment. However, we will show in the following section that, while these models succeed at modeling the general pattern of the motion, a clear understanding of the parameters has not yet been established. The complex interactions of solder, under bump metallurgy, oxidation, flux solvent evaporation, flux activation, and the resulting wetting are not captured by current models.

In our analysis, we frequently rely on the Surface Evolver software. It utilizes a gradient descent model to minimize the energy of a surface (Brakke, 1992). The calculated surface shapes have been found to closely resemble experimental results (Moon et al., 1996; Chenxi Wang and Chunqing Wang, 2010).

When calculating forces, we apply the principle of virtual work. Josell et al. (2002) have used similar equations within Surface Evolver to calculate alignment forces for 63Sn–37Pb solder. They have compared the results to experimental data and found that the two closely matched.

7.1 State of the Art

A basic model for the dynamics of the self-alignment mechanism in flip-chip soldering was developed in (Patra and Y. C. Lee, 1991a). It is assumed that a centering force $F_c$ as well as a damping force $F_d$ are acting upon the chip of mass $m$ causing an acceleration $\ddot{x}$

$$m \cdot \ddot{x} = F_c(x) - F_d(x, \dot{x}).$$  \hspace{1cm} (7.1)

$F_c$ is the result of an offset $x$ causing a deformation of the solder’s meniscus. This deformation results in an increase of the solder’s surface energy ($E_s$). $F_c$ is dependent on the surface tension $\gamma$ and the alignment offset $x$. The viscous damping force $F_d$, on the other hand, is dependent on the flow inside the solder joint which is induced by $\dot{x}$.
Table 7.1: Derived material properties from (Landry, Patra, and Y. C. Lee, 1991). Values calculated by us are starred, while those directly extracted from the paper are not.

<table>
<thead>
<tr>
<th>Case</th>
<th>Temp.</th>
<th>ω</th>
<th>ω₃</th>
<th>h*</th>
<th>γ*</th>
<th>μ*</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>in K</td>
<td>in s⁻¹</td>
<td>in s⁻¹</td>
<td>in μm</td>
<td>in N m⁻¹</td>
<td>in mPa s</td>
</tr>
<tr>
<td># 1</td>
<td>473</td>
<td>26.62</td>
<td>1.31</td>
<td>1160</td>
<td>0.074</td>
<td>143.2</td>
</tr>
<tr>
<td># 2</td>
<td>473</td>
<td>45.4</td>
<td>0.83</td>
<td>859</td>
<td>0.178</td>
<td>75.1</td>
</tr>
</tbody>
</table>

7.1.1 Experimental Data in the Literature: Landry, Patra, and Y. C. Lee

Landry, Patra, and Y. C. Lee (1991) have subsequently fitted two sets of experimental data to a simplified version of this model. The centering force $F_c$ is assumed to follow Hooke’s law with

$$F_c(x) = -\frac{dE_s}{dx} = -C_c \cdot x. \quad (7.2)$$

Similarly Couette flow with a profile $u(z)$, boundary conditions $u(\phi) = 0$ and $u(h(x)) = \dot{x}$, and a constant solder height $h$ is assumed for the viscous damping force $F_d$ (which is pointed in the opposite direction of $\dot{x}$)

$$F_d(x, \dot{x}) = -\mu \cdot \frac{A}{h} \cdot \dot{x} = -C_d \cdot \dot{x}. \quad (7.3)$$

Here, $\mu$ is the viscosity of the solder and $A$ is the contact area of the pads. Combining eqs. (7.1) to (7.3) results in the differential equation

$$m \cdot \ddot{x} + C_d \cdot \dot{x} + C_c \cdot x = 0. \quad (7.4)$$

For an underdamped case, the solution to this equation is (ibid.)

$$x(t) = x_m e^{-\omega_d t} \cos(\omega t + \phi) \quad \text{with}$$

$$\omega_d = \frac{C_d}{2m},$$

$$\omega^2 = \omega_o^2 - \omega_d^2,$$

$$\omega_o^2 = \frac{C_c}{m}. \quad (7.5)$$

Assuming a perfectly cylindrical shape for the solder meniscus and $N_p$ pads, we can calculate (Veen, 1999)

$$\mu = \frac{C_d h}{N_p \pi r^2} \quad \text{and} \quad \gamma = \frac{C_c h}{N_p r \pi}. \quad (7.6)$$
7.2 Factors Influencing Solder Self-Alignment

Table 7.1 lists \( \omega \) and \( \omega_d \) for cases 1 and 2 from (Landry, Patra, and Y. C. Lee, 1991). We have derived the material constants that would explain the observed behavior: First, we have calculated the height \( h^* \) for an assumed surface tension of 0.4 N m\(^{-1}\) (see table 7.2) using the Surface Evolver software. Using this height, we calculated the material properties resulting from eqs. (7.5) and (7.6). In table 7.1, the calculated values are starred, while the ones directly obtained from the paper are not.

As previously pointed out in (Josell et al., 2002) the surface tension does not match the values reported in the literature for solders similar to the 63Sn–37Pb used here (see table 7.2). Furthermore, the calculated material properties are highly inconsistent between the two cases (Veen, 1999). Finally, the calculated viscosity cannot be linked to that of solder.

7.1.2 Experimental Data in the Literature: W. Lin and Y. C. Lee

W. Lin and Y. C. Lee (1999) have also tracked the solder self-alignment movement. The pads were square with 1 mm edge length and Ti, Cu metallization. The joint height \( h \) was 350 \( \mu\)m. Eutectic Sn-Pb solder was used in an 1.7 % formic acid vapor environment. At the start of the experiments, the pads were completely wetted, but the solder was solid. The pads were misaligned by about 10 \( \mu\)m. (ibid.)

Instead of the oscillatory movement predicted by the above model, an over-damped behavior, in which 90 % of the alignment takes place in about 10 s, was observed. Lin and Lee explain that by the changing surface conditions during the melting process. The primary reason for these is the lower centering force due to the presence of oxides. (ibid.)

7.2 Factors Influencing Solder Self-Alignment

While similar models roughly match experimental data in the case of nonsolder liquid self-alignment (J.-M. Kim, Shin, and Fujimoto, 2004; Lambert et al., 2010), the above examples show that for solder self-alignment this is not the case. During solder self-alignment, many processes take place. In the following sections we will consider some of the effects that are unique to solder self-alignment.

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Table 7.2: Surface tension and viscosity of several solder alloys as reported in the literature.
7.2 Factors Influencing Solder Self-Alignment

7.2.1 Oxidation

Solder tends to oxidize, even more so at raised temperatures (Kuhmann et al., 1998). The same is true for the contact pads depending on the metallization used. Oxides in turn prevent the solder from wetting the pads. In the case of solder paste, it also prevents coalescence of the individual solder balls contained in the paste. Apart from that, the oxide layer is a rather stiff shell around the solder particles, which significantly affects their rheological behavior. (Mannan et al., 2000)

7.2.2 Flux

Flux is used to first reduce and subsequently to prevent solder and pad oxidation. Typically flux is formulated so that it is activated at a temperature below the melting point of the solder. It removes the oxidation and builds a thin protective coating around the solder and pads. Flux activity increases significantly at higher temperatures (MacKay and Voss, 1985). Flux consists of an unactivated vehicle (often rosin), solvents, and activators. The exact composition is proprietary (MacKay, 1993). While the viscosity of flux at room temperature is available from manufacturers, it is not known at soldering temperatures. Furthermore, due to the evaporation of the solvents and chemical reactions, the viscosity can be expected to change significantly with time.

Experiments have shown that the surface tension of Sn–Pb alloys is reduced by more than 10% when it is covered by organic flux. This reduction is desired as it improves wetting. (Howie and Hondros, 1982)

In the experiments of Landry, Patra, and Y. C. Lee (1991) the substrate pads were coated with 20 \( \mu \text{m} \) of organic flux. Since the authors point out that the experiments had to be conducted within 4 min to suppress effects caused by flux evaporation, flux seems to have had a significant influence on the tests. (ibid.)

7.2.3 Flow Profile

Given the solder density \( \rho \), the time \( t_1 \) until an almost linear solder flow velocity distribution is established is (Lu and Bailey, 2005)

\[
 t_1 = \frac{8h^2 \rho}{\pi^2 \mu}. \tag{7.7}
\]
7 Modeling of Chip Alignment Motion

Using a coupled model of solder motion (within the individual solder connections) and chip, motion Lu and Bailey have shown that the assumption of Couette flow eq. (7.3) can significantly underestimate damping (Lu and Bailey, 2005). Lambert et al. (2010) have subsequently provided an analytical approximation of the coupled model.

Owing to the rather large meniscus height in the experiments by Landry, Patra, and Y. C. Lee (1991), the time \( t_I \) is on the order of seconds, which is much longer than the oscillation period (table 7.1). The damping can, therefore, be expected to be significantly higher than predicted by the uncoupled model.

7.2.4 Wetting

During the wetting process, parts of the \( \text{UBM} \) dissolve into the solder (and vice versa) and an intermetallic phase is built up. Because of the formation of the intermetallic phase, the rheological properties of the solder deviate. The wetting speed is temperature dependent (Kang et al., 2005). Wetting takes place only after the oxidation is (partially) removed. As wettability improves, the molten solder-pad contact angle \( \theta \) decreases. Chen, Fennell, and Baldwin (2000) conclude that wetting initially dominates solder self-alignment.

7.2.5 Solder Paste

Solder pastes consist of approximately equal volumes of small (depending on the type 2 \( \mu \text{m} \) to 180 \( \mu \text{m} \) diameter) solder particles and flux. During heat-up, first the solvents evaporate. This causes the solder balls to come in contact with each other while the flux is being expelled (Mannan et al., 2000). When all solvents have evaporated, approximately 75% of the paste’s volume consist of solid solder. Since the maximum packing rate for spheres is around 64%, the paste becomes a solid at this point. (Genovese, 2012)

Slightly below the melting point of the solder, the flux is activated and the solder oxides are reduced. When the solder balls finally melt, they start to coalesce. This process is limited by the oxide layer on the solder, and the rate of oxide reduction. It was found to happen in the order of seconds—several orders of magnitude slower than what would be expected in the absence of oxides. (Mannan et al., 2000)
7.2.6 Summary

While the models found in the literature seem to generally describe the motion of the chips during self-alignment, they do not take into account the effects described above. This can generally be compensated for by using modified viscosity ($\gamma$) and surface tension ($\mu$) parameters. The degree to which the parameters need to be modified depends on the effects present. Of the effects described above, the oxide layer around the solder appears to be the fundamental reason for the retarded self-alignment reported in the literature.

7.3 Model

Our process is affected by several of the effects described in the previous section: we use a solder paste, our solder is partially oxidized, and the self-alignment process occurs simultaneously with the melting of the solder and wetting of the pads.

7.3.1 Kinetic Model

In our case, movement is not restricted to one direction. Thus, we simulate the movement in a two-dimensional plane. Analogous to eq. (7.1), we assume that centering forces and damping forces act upon our chip. Since our pad layout (fig. 7.1) is asymmetrical, we take the individual forces $\vec{F}_{c,i}$ and $\vec{F}_{d,i}$ acting on the $N_p$ pads into account. Given the pad offset $\vec{p}_i$ (fig. 7.1) we obtain the resulting force
\[ \vec{F} \text{ and the resulting torque } \tau \text{ as} \]

\[ \vec{F} = \sum_{i=1}^{N_p} \vec{F}_{c,i} - \vec{F}_{d,i} \quad (7.8) \]

\[ \tau = \sum_{i=1}^{N_p} \vec{p}_i \times (\vec{F}_{c,i} - \vec{F}_{d,i}) \quad (7.9) \]

We do not take into account the comparatively small twist-restoring torques of the individual solder connections. From the total force \( \vec{F} \) and torque \( \tau \), we calculate the translational (\( \ddot{x} \)) and angular (\( \ddot{\alpha} \)) acceleration

\[ m \cdot \ddot{x} = \vec{F} \quad \text{and} \quad I \cdot \ddot{\alpha} = \tau. \quad (7.10) \]

Given an initial offset \( (\dot{x}_0, \dot{\alpha}_0) \), and velocity \( (\ddot{x}_0, \ddot{\alpha}_0) = (\ddot{o}, \ddot{o}) \), we can calculate the offset \( (\ddot{x}(t), \ddot{\alpha}(t)) \) at time \( t \) by means of integration.

### 7.3.2 Centering Force

Our chip’s pads have a slightly elongated rectangular shape (fig. 7.1). For reasons of simplification, we model them as having the same square dimension as the

\[ \text{Figure 7.2: Centering force versus pad offset. The curve for the analytical model is not marked.} \]

Surface Evolver results for movement along the pad edges is marked with a dot (*) and the result for diagonal movement are marked with a cross (+). (Model parameters: see table 7.3, \( V = 5.49 \times 10^6 \text{ m}^3 \).)
substrate’s pads ($c = 380 \mu$m). Since we are analyzing fairly large offsets of the chip (up to half the edge length of the pad), we cannot apply the linearization of the centering force from eq. (7.6). Instead, we assume that the meniscus forms a parallelepiped, with the solder pad on the substrate forming the base. The free surface energy $E_{S,i}$ of the solder–atmosphere interface $S_{s,a,i}$ of a single pad $i$ then is (Tsai, Hsieh, and Yeh, 2007)

$$E_{S,i} = \int_{S_{s,a,i}} \gamma \, dS = 2\gamma c \left( \sqrt{h^2 + x_{i,o}^2} + \sqrt{h^2 + x_{i,1}^2} \right).$$  \hspace{1cm} (7.11)

Assuming a constant meniscus height $h$, we obtain the centering force by differentiation

$$-F_{c,i,j}(\tilde{x}) = \frac{dE_{S,i}}{dx_j} = \frac{2\gamma}{\sqrt{x_{i,j}^2 + h^2}} x_{i,j}. \hspace{1cm} (7.12)$$

Benchmarking the approximation using Surface Evolver, we have found that

$$\tilde{F}_{c,i}(\tilde{x}) = -\frac{2\gamma}{\sqrt{\tilde{x}_i^2 + h^2}} \tilde{x}_i \hspace{1cm} (7.13)$$

is a fairly good match, while eq. (7.12) significantly overestimates the centering force for diagonal offsets larger than 100 $\mu$m. The resulting forces are depicted in fig. 7.2 alongside results from the Surface Evolver benchmark for offsets along the pad edge and for diagonal offsets. Our approximation produces the same results for both cases. The values resulting from eq. (7.13) are within 20% of the benchmark for the relevant offset ($\tilde{x}$) range.

For the benchmark, we have chosen a solder contact angle of $\theta = 25^\circ$ for the pads (Mei et al., 1997) and complete nonwettability of the passivated areas around the pads. Our approximation from eq. (7.13) does not take the contact angle into account. For large contact angles and large offsets, this can cause significant errors. Figure 7.3 shows that, in these cases, the shape of the contact area is significantly altered and that the height $h$ is increased. Equations (7.11) to (7.13) no longer apply. While, for a diagonal shift, the contact shape would remain roughly square, $c$ is reduced. The resulting effect can be observed in fig. 7.2 when, for $\|\tilde{x}\| = 100 \mu$m, the centering force starts descending.

### 7.3.3 Damping Force

For our application, the time until an almost linear flow profile is established eq. (7.7) is in the order of milliseconds. This is much shorter than the observed alignment
duration. We therefore assume Couette flow analogous to eq. (7.3).

7.3.4 Oxide and Solder Paste

Our simulation starts at the state where the solvent has been (mostly) evaporated from the solder paste. The paste has become hard (section 7.2.5). To model the stiff oxide shell (section 7.2.1) and the inability of the paste to flow, we start the simulation with a very high initial viscosity of 100 Pa s. We then let the viscosity linearly approach the nominal value of the solder over a period \( t_i \).

7.3.5 Wetting

To simulate the progressive wetting of the pads (section 7.2.4), we also let the edge length \( c \) linearly approach its real value from 0 over the period \( t_i \).

7.4 Simulation

Measured and estimated parameters for our case study can be found in table 7.3. For the surface tension \( \gamma \) we have started with the theoretical value for 46Bi–32Sn–22Pb
Table 7.3: Parameters of the simulation

<table>
<thead>
<tr>
<th>measured values</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder density</td>
<td>$\rho$</td>
</tr>
<tr>
<td>Edge length</td>
<td>$c$</td>
</tr>
<tr>
<td>Chip mass</td>
<td>$m$</td>
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</table>

<table>
<thead>
<tr>
<th>estimated values</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Meniscus height</td>
<td>$h$</td>
</tr>
<tr>
<td>Moment of inertia</td>
<td>$I$</td>
</tr>
<tr>
<td>Dynamic viscosity of solder</td>
<td>$\mu$</td>
</tr>
<tr>
<td>Surface tension of solder</td>
<td>$\gamma$</td>
</tr>
<tr>
<td>Contact angle (only used by Surface Evolver)</td>
<td>$\theta$</td>
</tr>
</tbody>
</table>

From Table 7.2 and reduced it by 7.6% since the theory used in (Prasad and Mikula, 1999) seems to produce values that are too high (see the values for 4Bi–58Sn–38Pb in the same table). To account for the presence of flux, we have reduced the obtained value by another 10%. We have not taken into account a possible temperature dependence of the surface tension. Based on the viscosities listed in Table 7.2 and the Arrhenius law given in (Plevachuk, Sklyarchuk, Eckert, et al., 2008), we have roughly estimated the viscosity $\mu$ at $T = 413$ K.

We have implemented the model described above as a numerical simulation using discrete time steps of $10^{-7}$ s. The equations of motion are implemented using the Verlet Velocity algorithm. In lack of a detailed understanding of both aspects, we have implemented the decrease of the viscosity (caused by the oxide shells around the solder particles being reduced and the solder melting, see section 7.3.4) and the increase of the solder contact area (caused by the wetting progress, see section 7.3.5) to progress in parallel.

Without taking the influences of oxide, melting, wetting, and solder paste into account, our simulation predicts an oscillatory motion with frequencies in the range of several hundred Hz.
7.5 Alignment Tracking

We have optically recorded the motion of the chip at 52.2 Hz. The resolution of the optical system is 37.5 μm. From the recorded data, the motion of the chip and, as a reference, of the substrate has been extracted using CSEM’s custom tracking software (Wyss and Glock, 2010). Using subpixel sampling the measurement resolution has been enhanced beyond the optical resolution. For nonmoving parts we observe a standard deviation of 1.3 μm and 0.031° for lateral and angular measurements, respectively. Figure 7.4 depicts the motion for a typical sample as well as simulation results for identical initial offsets.

The alignment duration supports the assumption that the process is limited by the oxide reduction and wetting speed rather than the viscosity of the solder. This finding is also supported by the large effect of the soldering temperature on the alignment speed we have observed.

We attribute the slightly irregular chip movement to nonsimultaneous melting and wetting of all pads. Sometimes we have even observed an initial rotation of the chip. We can produce the same result in our simulation if we offset the start time for individual pads by small amounts. We use the controlled and fast heater described in chapter 6. Because of the way the heating meanders are embedded in the substrate, it can be expected that the lower pads in fig. 7.1 are heated slightly faster than the upper ones (see also the temperature distribution in fig. 6.10).

Table 7.4 lists the durations of alignment motions. The times are given for traveling from 5% to 95% of the total distance (i.e., the central 90%). Times for the central 80%, 70%, 60%, 50%, and 40% are also given. It can be deducted that most of the motion happens within a short period of time. That timespan starts after oxide removal and ends when the chip is nearly aligned to the substrate.
Figure 7.4: Motion tracking and simulation results. At the bottom, a typical recorded alignment motion is depicted. At the top, the simulated motion using identical initial offset is shown. For the simulation, the duration of the initial parameter adaption $t_i$ has been set to 1.2 s. The adaption process starts at $t = -0.05$ s (not shown) and ends at $t = 1.05$ s after the chip has reached its final position.
Table 7.4: Alignment durations (all in s) for various samples. The durations are measured for the
time it took to travel from 5% to 95% (10% to 90%, etc.) of the total distance.

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8 Assembly Results

We have packaged several batches of FemtoTools FT-260 devices using the parallel C4 process. The devices have been functionally tested by FemtoTools, and they perform as desired. The selected low-temperature solder guarantees a level of shear stress that does not impact the performance of the sensor.

One of the critical points of this application is the flux reaching the comb drive, leading to the destruction of the device (see section 4.1.2). This has not been observed for any of the manufactured devices.

8.1 Solders

We initially selected 46Bi–34Sn–20Pb solder for our application (section 4.2.1). At first, we used Indalloy 42 in the Indium 5.5LT solder paste carrier (Indium, 2008a). Later, we switched to the improved (Scalzo, 2012b) Indium 5.7LT solder paste (Indium, 2008b). We have also run assembly tests with eutectic tin-bismuth (58Bi–42Sn, melting point: 138 °C) solder pastes. We used the Indium 5.7LT solder paste with Indalloy 281 as well as Felder GmbH IsoCream EL 42/58 (Felder, 2011). Our results indicate that these solders work well with our method, too. We have not functionally tested devices assembled using eutectic tin-bismuth solder, however. It can be expected that the higher melting point leads to increased stress in the MEMS device. Whether the stress reaches levels that impact the sensor operation remains to be verified.

While the flux contained in the other pastes is classified as ROLO (IPC, 2008), the flux in the Felder paste is classified as ROL1. Fluxes of type ROLO can contain up to 0.05 % (by weight) halides; those of type ROL1 may contain up to 0.5 % halides. In fact, the Indium solder pastes are specified as halogen-free and as having a halide content of 0 %. The flux used in the Felder paste can, therefore, be expected to reduce oxides more actively. Table 8.1 lists important properties and parameters
Table 8.1: Solders used. The element percentages are relative to the metal part of the paste. All percentages are by weight. Soldering temperature (S. T.) and preheat temperature (P.-h. T.) are the values we usually use for our application.

<table>
<thead>
<tr>
<th>Solder make</th>
<th>Paste make</th>
<th>Flux type*</th>
<th>Alloy (eutectic)</th>
<th>Metal in %</th>
<th>S. T. in °C</th>
<th>P.-h. T. in °C</th>
<th>Lot</th>
</tr>
</thead>
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<td>Bi–Sn–Pb</td>
<td>84</td>
<td>145</td>
<td>80</td>
<td>PS49920</td>
</tr>
<tr>
<td>Indalloy 281</td>
<td>Ind. 5.7LT</td>
<td>ROL0</td>
<td>Bi–Sn</td>
<td>84</td>
<td>165</td>
<td>125</td>
<td>PS49915</td>
</tr>
<tr>
<td>Fel. IsoCream EL 42/58</td>
<td>ROL1</td>
<td>Bi–Sn</td>
<td>85</td>
<td>165</td>
<td>125</td>
<td>165682/08/12</td>
<td></td>
</tr>
</tbody>
</table>

* According to IPC (2008).

Figure 8.1: Cross section of solder connection (sample # 2, 0.26 mg of Indalloy 42 in Indium 5.5LT paste were used for seven connections).

of the used solders.

8.2 Solder Joint Analysis

8.2.1 Cross Sections

We have done several cross sections through the solder connections to analyze both the wetting behavior of the solder and the pad–pad alignment (see also fig. 6.2). Generally, we observe good wetting (see fig. 8.1) with the chip pads sometimes showing very small deficiencies at the very edge.

In early testing we often encountered solder voids (see fig. 8.2, Dudek et al., 2010). We identified them as flux entrapment voids. Voiding occurred frequently
for solder masses of more than 450 µg per assembly. Originally, the problem was attributed to the fast heating and short soldering time. It was assumed that the flux did get expelled from the solder in time. However, at the time we used expired (by more than two years) Indalloy 42 / LT5.5 solder paste. Old paste can contain more oxides, which will be reduced to gases during soldering (Scalzo, 2012b). These gases can then form voids. We have not observed strong voiding with fresh paste.

8.2.2 Solder Connection Strength

We have shear tested the devices using a Norson Dage 4000 bond tester. The results of our tests are listed in table 8.2. The connections have always failed at the chip pads. For this reason, when calculating the shear stress, we use the surface area of these pads ($7 \times 360 \mu m \times 400 \mu m = 1.1008 \text{ mm}^2$). All tests were conducted at about 22 °C temperature and with a shear speed of 300 µm s$^{-1}$.

Comparison of Results

In the 46Bi–34Sn–20Pb solder tests, we have obtained a maximum shear stress of 12.6 N mm$^{-2}$, while, with 58Bi–42Sn solder, the maximum shear stress we have observed was 36.2 N mm$^{-2}$.

The results for 58Bi–42Sn solder are in line with those found in the literature for similar solders. Tomlinson and Fullylove (1992) list an ultimate shear strength between 19.6 N mm$^{-2}$ and 25.3 N mm$^{-2}$ for 57Bi–43Sn solder on copper pads at
8 Assembly Results

**Table 8.2**: Shear-test results. All tests were done at a shear speed of 300 µm s⁻¹. For samples #1 to #32 the probe blade was set to a height of 100 µm above the substrate, for the remaining tests to 75 µm above the substrate. The amount of solder is the total amount per chip (seven pads).

<table>
<thead>
<tr>
<th>Sample number</th>
<th>Solder paste</th>
<th>Solder amount in mg</th>
<th>Soldering temp. in °C</th>
<th>Wafer temp. in °C</th>
<th>Soldering duration in s</th>
<th>Shear strength in N mm⁻²</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.26</td>
<td>145</td>
<td>80</td>
<td>15</td>
<td>12.6</td>
</tr>
<tr>
<td>5</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.30</td>
<td>145</td>
<td>80</td>
<td>5</td>
<td>11.9</td>
</tr>
<tr>
<td>8</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.31</td>
<td>145</td>
<td>80</td>
<td>5</td>
<td>11.1</td>
</tr>
<tr>
<td>10</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.54</td>
<td>145</td>
<td>80</td>
<td>30</td>
<td>10.9</td>
</tr>
<tr>
<td>11</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.37</td>
<td>145</td>
<td>80</td>
<td>30</td>
<td>10.3</td>
</tr>
<tr>
<td>14</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.48</td>
<td>145</td>
<td>80</td>
<td>30</td>
<td>11.2</td>
</tr>
<tr>
<td>15</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.46</td>
<td>145</td>
<td>80</td>
<td>30</td>
<td>9.0</td>
</tr>
<tr>
<td>18</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.65</td>
<td>145</td>
<td>80</td>
<td>30</td>
<td>9.5</td>
</tr>
<tr>
<td>19</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.63</td>
<td>145</td>
<td>80</td>
<td>30</td>
<td>10.0</td>
</tr>
<tr>
<td>20*</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.65</td>
<td>145</td>
<td>80</td>
<td>15</td>
<td>5.0</td>
</tr>
<tr>
<td>26</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.22</td>
<td>145</td>
<td>80</td>
<td>5</td>
<td>12.5</td>
</tr>
<tr>
<td>30</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.21</td>
<td>145</td>
<td>80</td>
<td>30</td>
<td>11.4</td>
</tr>
<tr>
<td>32</td>
<td>Ind. 42 / 5.5LT</td>
<td>0.24</td>
<td>145</td>
<td>80</td>
<td>30</td>
<td>10.1</td>
</tr>
<tr>
<td>35</td>
<td>Ind. 42 / 5.7LT</td>
<td>0.28</td>
<td>130</td>
<td>25</td>
<td>15</td>
<td>7.1</td>
</tr>
<tr>
<td>37</td>
<td>Ind. 281 / 5.7LT</td>
<td>0.28</td>
<td>165</td>
<td>125</td>
<td>15</td>
<td>23.0</td>
</tr>
<tr>
<td>38</td>
<td>Ind. 281 / 5.7LT</td>
<td>0.31</td>
<td>165</td>
<td>125</td>
<td>15</td>
<td>25.9</td>
</tr>
<tr>
<td>41</td>
<td>Fel. EL 42/58</td>
<td>0.26</td>
<td>165</td>
<td>125</td>
<td>15</td>
<td>25.3</td>
</tr>
<tr>
<td>42</td>
<td>Fel. EL 42/58</td>
<td>0.28</td>
<td>165</td>
<td>125</td>
<td>15</td>
<td>31.7</td>
</tr>
<tr>
<td>43</td>
<td>Fel. EL 42/58</td>
<td>0.28</td>
<td>165</td>
<td>125</td>
<td>15</td>
<td>36.2</td>
</tr>
</tbody>
</table>

* Debris between chip and substrate.
20 °C. On the other hand, Grimmer (2012b) of Felder GmbH notes that the EL42/58 solder paste was tested to withstand at least 48 N mm⁻².

We have found no information for the shear strength of 46Bi–34Sn–20Pb in the literature. A lower shear strength than 58Bi–42Sn is expected—if only for the significantly lower melting point. Another, or additional, explanation for the significantly lower shear resistance of the tertiary alloy would be the lower soldering temperature. The same solder paste carrier is used for Indalloy 42 and Indalloy 281 solder. However, the carrier has been formulated for Indalloy 281 and its melting point of 138 °C. The flux is activated at around 100 °C (Scalzo, 2012a), above the melting point of Indalloy 42, but below our soldering temperature of 145 °C. Still, flux activity increases with temperature and the flux will, therefore, reduce oxidation quicker when used at a higher temperature. Furthermore, in the case of 58Bi–42Sn, we raise the temperature beyond the activation point before melting the solder (see sections 4.3.4 to 4.3.6, temperatures are adapted to account for the higher melting point of the 58Bi–42Sn alloy as per table 8.1). In summary, the disparate soldering temperatures may play a role in the ultimate shear strength difference between the eutectic Bi–Sn–Pb and Bi–Sn–Pb alloys. If however, the soldering temperature of the Bi–Sn–Pb solder is raised, some of the alloy’s advantages are lost. Also, the (preheating) temperature cannot be increased beyond the flux activation point prior to soldering.

The Felder EL 42/58 solder paste seems to provide slightly higher shear force resistance than the Indalloy 281 / 5.7LT counterpart. This could be explained by a more active flux (see section 8.1). We do not have collected sufficient amounts of data though to assert a difference with any certainty, though.

Breaking Chips

The force sensor chip has an open, ‘U’-like shape. Because of that, the joint failure is always accompanied by the chip breaking apart. Figure 8.3 shows one of the few chips that have not flown away during shear testing. The destruction of the chip

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1 Similar measurements are also presented in (Mei et al., 1997).

2 This is rather uncommon.
inevitably reduces the maximum shear force. The force-curve in fig. 8.4 suggests the same effect. Shortly before the chip is completely detached, a first break of one or several solder connections occurs. After that, the remaining pads have to handle the complete shear force.

Soldering Duration

Interestingly, we could not find an influence of the soldering duration on the solder connection strength for the values we tested. Even with only 5 s soldering duration (the time spent at the soldering temperature), which amounts to a time above the solder’s melting point of about 16 s (for 46Bi–34Sn–20Pb), connections of good quality are formed. This comes as a surprise because both solder manufacturers recommend much longer soldering durations (Indium, 2008b; Felder, 2011).
8.2.3 Summary

The maximum shear force measurements, good electrical connections and cross-sections (see section 8.2.1) demonstrate good wetting of the contact pads. According to Goldmann (1969) the geometry of the pads should be optimized so that “fractures are evenly divided between the” solder–substrate and solder–chip interfaces. In our application the fracture generally occurs along the chip's pads. Even though the contact area of the chip’s pads is slightly larger than that of the substrate’s pads (0.1444 mm² versus 0.144 mm²), this is an indication for the bond being weaker on the chip side. This assumption is supported by the poorer wetting of the chip pads we have observed in the cross sections. Most likely a modified chip UBM can lead to improved results. Nonetheless, our method already creates very good solder connections. The shear results are in line with the results reported in the literature for comparable solders and would likely be even better with a solid chip that does not break during testing.

8.3 Alignment

It needs to be stressed that the C4 process aligns the chip's and substrate's pads to each other. This is not equivalent to aligning the chip to the substrate, though. While the pads on the chip are placed very precisely, this is not the case for the PCB substrate. The copper layers of the PCB are commonly aligned to the substrate's edges with a tolerance of 150 μm. However, increased precision can be obtained at higher cost. When we evaluate parallel C4’s alignment accuracy we measure the alignment to the substrate's top copper layer.

The final alignment has been analyzed optically using a digital camera attached to a Nikon SMZ745T stereo microscope. Due to the way the microscope is constructed the image plane is tilted. We try to mechanically compensate for that. Furthermore, to guarantee exact distance measurements, we create an affine transformation between the image coordinates and physical coordinates. We calculate this transformation on the basis of the known PCB via locations by means of least-square fitting (Elonen, 2007; Spät, 2004). This way, we can cancel out rotation, shear, and scaling effects that result from the inaccurate manual placement of the parts onto the microscope's table as well as effects that result from variations in zoom. The
Figure 8.5: Map of chip positions relative to the desired position. The origin is at the center of the land location. The x-axis is pointing in the desired direction of the probe tip. The numbers denote the samples. Samples assembled using the same solder paste are shown in identical colors. The arrows indicate the chip orientation; however, the angular error is amplified by a factor of 90 (i.e., an arrow pointing in a horizontal direction designates a $1^\circ$ deviation from the x-axis). Dust was detected at the land location of sample #29 prior to the assembly.
resolution of the optical system is about 6 µm. The feature coordinates are manually determined in the camera images. Figure 8.5 shows a map of our alignment measurements. The median of our measurements deviates by (0.95 µm, 11.78 µm) and 0.056° from the expected origin and angle. The standard deviations of the chip origin and angle are (11.97 µm, 11.80 µm) and 0.28°, respectively. The chip and substrate features are not always easy to recognize in the camera images. Some error has to be expected from the manual analysis of the pictures.

Using the methods described in section 7.5 we have also recorded and analyzed the movement of most of the chips during alignment. The paths the chips have
followed during self-alignment are depicted in fig. 8.6. We attribute the irregular movement to the nonsimultaneous wetting of the individual pads and the non-symmetrical layout of the pads.

In our tests, we identified two major reasons for misalignment: too little wetting and too much wetting. Too little wetting is typically caused either by using an insufficient amount of solder or by insufficient oxide removal. The latter can be addressed by using different fluxes, modifying the UBM, or cleaning procedures. We have also observed excessive wetting. This occurs on the PCB substrates, where the passivation layer is not directly adjacent to the pads. The solder-resist passivation layer is applied late in the PCB manufacturing process. The alignment tolerance between copper layer and solder resist mask varies, but 100 μm is not uncommon. This tolerance has to be compensated for by enlarged gaps in the solder resist. Within these gaps, the solder can spread to the sides of the substrate’s pads (fig. 8.7). Also the solder easily spreads onto the part of the wire leading to the pad that is not covered by solder resist.

Our excellent optical alignment measurement results are supported by what we seen in the cross-sections: we have never found strongly misaligned solder connections.
Table 8.3: Process-step durations. The individual times include the manipulator’s movement from the previous step.

<table>
<thead>
<tr>
<th>Operation</th>
<th>Duration (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manual mounting (per device)</td>
<td>10</td>
</tr>
<tr>
<td>Measure reference temperature</td>
<td>2.4</td>
</tr>
<tr>
<td>Pickup</td>
<td>7.5</td>
</tr>
<tr>
<td>Assembly (5 s soldering)</td>
<td>20</td>
</tr>
<tr>
<td>Assembly (15 s soldering)</td>
<td>33</td>
</tr>
<tr>
<td>Assembly (30 s soldering)</td>
<td>50</td>
</tr>
<tr>
<td>Manual unmounting (per device)</td>
<td>10</td>
</tr>
</tbody>
</table>

8.4 Cycle Time

Table 8.3 lists the durations for the individual process steps. The time for an individual step is measured from the end of the previous step to the end of the current step. This includes the manipulator’s movement from the previous step to the current one. All measurements have been done while using 46Bi–34Sn–20Pb solder. In the table, values for the actual assembly step with soldering times of 5 s, 15 s and 30 s are included. The soldering times are measured from the time the desired soldering temperature is reached (here: 145 °C) to the time the heating is turned off. The assembly process step ends when the temperature drops 6 °C below the solder melting point (here: 92 °C). The total process time for our semi-automatic process implementation varies between 90 s to 120 s per batch or 30 s to 40 s per device.

As we have pointed out in section 4.3, several of the steps would be removed or optimized in an industrial application. Individual reference temperature measurement would not be required and heating could start right after pickup without having to move to the camera station first. The manual steps would be replaced by much faster, parallel, and automatized counterparts. In section 6.4.2 we have described the heating and cooling behaviour of the system (see also fig. 6.8). Cooling takes much longer than heating. This could be improved by forced cooling as it is common for other systems. By applying all of the above measures process times of 15 s beyond the soldering time should easily be achievable.

Even larger throughput improvements can obviously be achieved by increasing the amount of parallelization. Combining the changes described above with an
increased parallelization of only 16 devices per batch would already lead to process times around 2 s per device.
9 Summary: Conclusions and Outlook

9.1 Conclusions

This thesis presents parallel c4, a method providing high-throughput and precise-placement packaging of mems at low cost. The method requires only limited changes to existing mems designs. By building on c4 technology, many of the potential advantages are offered to the mems designer: chip-scale package (CSP), stacking of mems and electronics chips, improved electrical and thermal performance, and integrated mechanical fixation are just some of them. Parallel c4 relies on process parallelization to achieve high throughput and on self-alignment to achieve alignment precision. This approach obviates the need for an expensive manipulator.

The method features properties that may prove beneficial to new designs. Contrary to regular flip-chip approaches, the mems chip is handled from a single side only. This gives the chip designer the option of placing fragile structures on most of the underside of the chip. Due to the parallel processing of the assembly, high throughput can be achieved at relatively low handling acceleration. This can be desirable for very sensitive devices.

Because of tooling requirements, the cost of a machine implementing the parallel c4 method will highly depend on the amount of parallelization chosen. The manufacturer can select the appropriate amount of parallelization to match the desired throughput. This significantly reduces the cost for producing small- to medium-size batches as found in specialized devices or experimental setups.

9.1.1 Contributions

At the core of this thesis is the parallel c4 packaging method. As pointed out above, it provides a low-cost packaging method for large as well as small batch sizes. For large batch sizes, it also provides high throughput. We have demonstrated the
excellent alignment capabilities of parallel c4.

We have presented the self-alignment dynamics models found in the literature and extended them to take flux solvent evaporation, oxide reduction, and wetting into account in a wholesale manner. We have compared the results of a simulation based on the new model to tracking data from our application. In doing so, we provided an in-depth analysis of solder self-alignment dynamics. We have been able to show that oxides and their reduction dominate the timescale of the alignment process in our case study.

When the surface force of the liquid solder is not sufficient to lift the chips out of the wafer, the reach-through chip-handling system based on suction needles provides an effective solution. It also allows the application of parallel c4 in cases where the land location solder pads are not the highest elements on the substrate (e.g., in certain cases of 2D SIP).

We have presented a novel localized heating system for soldering. It is temperature controlled but requires no separate sensor. Also, it can provide steep heating ramps. Since it is embedded into the substrate, it can easily be adapted to a specific application without generating tooling costs. Part costs are also minuscule as the same processes used for manufacturing the substrate are employed for the creation of the heater. Thanks to the direct heating from withing the substrate, the method is very energy-efficient and has low environmental impact. Our shear testing and cross-section analysis have shown that good solder connections can be created at short soldering times and steep heating rates.

For MEMS, classical chip singulation methods often are not appropriate. They produce debris that could damage the MEMS. Also, conventional use of dicing tape often is not an option. Therefore, MEMS are often capped prior to singulation. Our method allows for singulation of the chip by etching. Deep etching processes are commonly employed in MEMS, and, therefore, the etching does not add an extra process step. Using etching for singulation leaves the chip surrounded by a gap. It is no longer in a defined position. The parallel c4 method is tolerant to that and can compensate the location uncertainty through its self-alignment mechanism. It provides an automated parallel packaging method for nonfixed chips without the need for individual chip localization.

A robot software stack was developed in the course of our parallel /c4 application. It uses a simple, yet effective approach to separate different functions of the software.
This guarantees reliable real-time operation. It is based solely on open-source software. The IndustryPack subsystem and driver development done in the course of this thesis are being merged into the Linux kernel.

9.2 Outlook

9.2.1 Industrial adoption

Quick widespread adoption of this method is, however, questionable. If not required to do so, large packaging companies will shy away from replacing their proven technologies by this one. This is not least the case because of the need to reobtain certification for use in certain applications such as medical, military or space. The certification process is both expensive and time consuming.

A more likely scenario is gradual adoption of parallel c4 for new designs on the basis of its technical merits. Our approach solves the problem of cost-efficient packaging of devices that have been singulated by etching and are not located in an exactly defined position. Also, new designs become possible through our one-sided handling.

9.2.2 Future research

We have analyzed the dynamics of solder self-alignment and developed a model that explains the observed behaviour. Further research targeted at the various factors influencing the self-alignment will, however, be required to obtain a thorough understanding of the interaction of these factors. So far we have packaged three devices per batch. While we have no doubts that parallel c4 is capable of much higher levels of parallelization, this will need to be verified in applications.
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