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Role of impurities and p-n junction formation in CdTe thin film solar cells

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Role of impurities and p-n junction formation in CdTe thin film solar cells

A dissertation submitted to
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for the degree of
Doctor of Sciences

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Abstract

Photovoltaics (PV) based on CdTe thin films offer one of the most cost-effective options for the production of solar electricity. Cost reduction of CdTe PV could be possible by substituting the commonly used rigid glass substrates with flexible metal foil to enable roll-to-roll production. However, the use of metal foil substrates is not compatible with the conventional CdTe solar cell structure (“superstrate configuration”) where light enters through the substrate into the finished device, therefore limiting the choice of substrates to transparent materials. To render the use of opaque substrates possible the conventional device structure must be inverted. In spite of various efforts, solar cell efficiencies in the inverted structure (“substrate configuration”) have previously remained below 8%. This was caused by the limited electronic properties of the CdTe layer and p-n junction, getting adversely affected by uncontrolled diffusion of impurities between different layers. In this thesis processes for the growth of CdTe solar cells in substrate configuration are presented which control impurity distribution in the solar cell and enable certified record efficiencies of 13.5%, 11.5%, and 10.9% on glass, flexible molybdenum foil, and flexible steel foil substrates, respectively. A novel concept for doping of the CdTe layer in substrate configuration is introduced. The controlled doping of the recrystallized CdTe layer with sub-monolayer amounts of copper results in hole densities of $\sim 10^{14}$ cm$^{-3}$, and leads to a pronounced improvement of the collection of photo-generated charge carriers. A process for the p-n junction formation in substrate configuration is developed, where both the CdTe and CdS layers are subjected to separate CdCl$_2$ treatments. The CdCl$_2$ treatment of the CdS layer leads to its recrystallization, and enhances minority carrier lifetime in the CdTe layer by an order of magnitude to $>2$ ns due to passivation of grain boundary and interface defects. Chlorine segregates at the CdTe/CdS interface and sulfur diffuses along CdTe grain boundaries, which can occur by an elemental exchange with oxygen. Sulfur segregates within <10 nm from the CdTe grain boundaries without significant formation of a tellurium rich CdS$_x$Te$_{1-x}$
alloy. The process presented in this thesis enables substrate configuration solar cells with comparable electronic properties as in superstrate configuration; however, the efficiency of 15.6% achieved in superstrate configuration with a low temperature process ($\leq 450 \, ^\circ\text{C}$) is still superior to the efficiency of devices in substrate configuration. The difference in efficiency mainly arises from more pronounced parasitic absorption in the thicker CdS layer used in substrate configuration devices. It is proposed that the reduction of CdS layer thickness requires the formation of a $\text{CdS}_x\text{Te}_{1-x}$ alloy at the p-n junction. This could be achieved by the addition of sodium, which is found to lead to massively enhanced CdS-CdTe interdiffusion. The process for substrate configuration solar cells offers new opportunities to overcome persistent challenges in CdTe PV and paves the way for industrialization of CdTe solar modules on flexible metal foil.
Zusammenfassung (In German)

CdTe Dünnfilmphotovoltaik ist eine der erfolgreichsten Technologien zur Produktion von kostengünstigem Solarstrom. Weitere Kostensenkung der CdTe Dünnfilmphotovoltaik könnte dadurch ermöglicht werden, dass die normalerweise verwendeten starren Glas-Substrate durch flexible Metallfolien ersetzt werden um eine Rolle-zu-Rolle Produktion zu erlauben. Die Verwendung von Metall-Substraten ist jedoch nicht kompatibel mit der herkömmlichen CdTe Solarzellenstruktur ("Superstrat Konfiguration"), bei der Licht durch das Substrat in die Solarzelle eindringt und daher nur transparente Substrate zulässt. Um die Verwendung von lichtundurchlässigen Substraten zu ermöglichen, muss die herkömmliche Solarzellenstruktur invertiert werden. Trotz verschiedener Bemühungen, ist die Effizienz von Solarzellen in der invertierten Struktur ("Substrat Konfiguration") in vorangegangenen Versuchen unter 8% geblieben. Dies ist auf die geringe elektronische Qualität der CdTe-Schicht und des p-n Übergangs zurückzuführen, was durch die unkontrollierte Diffusion von Verunreinigungen zwischen verschiedenen Schichten verursacht wurde. In dieser Arbeit werden Prozesse für die Herstellung von CdTe Solarzellen in Substrat Konfiguration präsentiert, die die Verteilung von Verunreinigungen in der Solarzelle kontrollieren und zertifizierte Rekordeffizienzen von 13.5% auf Glas-Substrat, 11.5% auf flexiblen Molybdän-Substrat und 10.9% auf flexiblen Stahl-Substrat ermöglicht haben. Ein neues Konzept für die Dotierung der CdTe-Schicht in Solarzellen in Substrat Konfiguration wird eingeführt. Die kontrollierte Dotierung der rekristallisierten CdTe-Schicht mit Kupfer-Mengen im Sub-Monolagenbereich hat Lochdichten in der CdTe-Schicht von \( \sim 10^{14} \text{ cm}^{-3} \) zur Folge, was dazu führt, dass photogenerierte Ladungsträger deutlich besser eingesammelt werden. Ein Prozess für die Bildung des p-n Übergangs wurde entwickelt, in der sowohl die CdTeals auch die CdS-Schicht einer CdCl\textsubscript{2} Behandlung unterzogen werden. Die CdCl\textsubscript{2} Behandlung der CdS-Schicht führt zu ihrer Rekristallisation und verbessert die Lebensdauer der Minoritätsladungsträger in der CdTe-Schicht um eine Größenordnung auf >2
ns durch die Passivierung von Korngrenzen- und Grenzflächendefekten. Chlor seg-
regiert an der CdTe/CdS Grenzfläche und Schwefel diffundiert entlang der CdTe Korn-
grenzen, was durch einen Elementaustausch mit Sauerstoff stattfinden kann. Schwei-
fel segregiert <10 nm entfernt von den CdTe Korngrenzen, wobei keine nachweisbare
Menge einer Tellur-reichen CdS$_{x}$Te$_{1-x}$ Verbindung entsteht. Der entwickelte Prozesses
ermöglicht die Herstellung von CdTe Solarzellen in Substrat Konfiguration mit ähnlichen
elektronischen Eigenschaften wie in Superstrat Konfiguration. Die in Superstrat Konfig-
uration mit einem Tieftemperaturprozess ($\leq$ 450 °C) erreichte Effizienz von 15.6% ist
jedoch weiterhin höher als die Effizienz der Solarzellen in Substrat Konfiguration. Der
Unterschied in der Effizienz ist größtenteils auf die stärkere parasitäre Absorption in der
in Substrat Konfiguration verwendeten dickeren CdS-Schicht zurückzuführen. Um die
CdS-Schichtdickenreduzierung zu ermöglichen, könnte die Bildung einer CdS$_{x}$Te$_{1-x}$
Verbindung am p-n Übergang notwendig sein. Dies könnte durch die Zugabe von Na-
trium erreicht werden, wodurch die Vermischung der CdS- und CdTe-Schichten deutlich
verstärkt wird. Der entwickelte Prozess für die Herstellung von Solarzellen in Substrat
Konfiguration bietet neue Möglichkeiten, langjährige Probleme der CdTe Dünnschicht-
photovoltaik zu lösen und ebnet den Weg für die Industrialisierung von CdTe Solarmod-
ulen auf flexibler Metallfolie.
Chapter 1

Introduction

1.1 Photovoltaics

Renewable energies have gained increasing interest due to the potential to replace a significant part of the electricity generated by other sources, such as fossil fuels or nuclear energy. In 2012, renewables supplied more than 20% of the global electricity [1]. One of the technologies for the production of renewable energy is photovoltaics (PV), where sunlight is directly converted into electricity. Currently, only a small part of the electricity is produced by PV. However, the installed capacity is growing at high pace. The world's cumulative PV capacity installed at the end of 2012 amounted to 102 GW-peak (GW$_p$), of which 31 GW$_p$ was newly installed in the year 2012 [2]. In 2011 and 2012, PV was the number-one newly installed electricity generation source in Europe and in 2012 PV covered about 2.4% of the electricity demand in Europe [2].

Currently, the PV market is dominated by solar cells based on silicon wafers. Emerging PV technologies based on various thin films have the potential to significantly reduce the cost of solar electricity. Potential materials include Cu(In,Ga)Se$_2$ (CIGS) [3,4], Cu$_2$ZnSn(S,Se)$_4$ (CZTS) [5], CdTe [6,7], CH$_3$NH$_3$PbI$_3$ [8,9], silicon [10], as well as dye-sensitized [11], and organic materials [12]. Each of these materials has certain advantages. CIGS has the advantage of very high efficiency of up to 20.8%, even surpassing the efficiency record of the current market leader polycrystalline silicon [13]. Organic PV can potentially become a very cheap technology, providing that efficiencies are further enhanced. Fast efficiency improvements of solar cells based on the perovskite layer CH$_3$NH$_3$PbI$_3$ indicate prospects of very high efficiency with this technology. CdTe
is an attractive material for production of low cost thin film solar modules and combines low costs with high efficiencies up to 19.6% on the cell level and 16.1% on the module level [14, 15]. CdTe PV is the second largest commercial PV technology after conventional crystalline silicon solar cells. In the following, properties and processing of CdTe thin film solar cells are described.

1.2 CdTe thin film solar cells

1.2.1 Device structure

CdTe thin film solar cells are multilayer structures consisting of semiconductor and metal layers. The charge separating p-n junction is formed by a p-type CdTe layer and typically a n-type CdS layer between two contacting layers. One of the contacts needs to be transparent to allow sunlight to enter the solar cell. Figure 1.1a shows the cross-section of the conventional CdTe solar cell structure, which has been mainly followed over the past 40 years and was first described by Adirovich et al. in 1969 [6,16]. In this “superstrate configuration”, light enters through the substrate into the solar cell, limiting the choice of substrates to transparent materials. This is well compatible to the use of rigid glass substrates. However, the choice of flexible substrates is quite limited in this configuration and flexible polyimide film is one of the few materials with suitable properties. Polyimide is temperature stable up to about 450 °C, has relatively good transparency, and high efficiencies were achieved on conventional thin PI [17, 18]. On experimental clear polyimide film efficiencies up to 13.8% were achieved [18, 19], but the large volume cost of this special substrate is currently not known.

The limitation of sufficient substrate transparency can be overcome by growing solar cells in “substrate configuration”, where – in comparison to the conventional superstrate configuration – the complete deposition order is reversed and light does not pass through the substrate (Figure 1.1b). This configuration allows the use of opaque substrates like metal foils and a photograph of CdTe solar cells on a flexible metal foil is shown in Figure 1.2. The growth of solar cells on flexible substrates is expected to lead to a significant price reduction of CdTe PV by implementing high-throughput roll-to-roll manufacturing. Furthermore, the growth in substrate configuration offers more control of p-n junction properties as recrystallization of CdTe and p-n junction forma-
1.2. CdTe thin film solar cells

Figure 1.1: Scanning electron micrograph and schematic of the cross-section of a CdTe solar cell in the conventional superstrate configuration (a) and the substrate configuration (b). The yellow arrows show the direction of illumination.

...tion with CdS can be decoupled. In spite of these advantages, the solar cell efficiency record in substrate configuration at the beginning of this thesis was 7.8% [20], which was significantly lower than the corresponding former record in superstrate configuration of 16.5% [21]. The reversal of deposition order does not allow simple transfer of the process from one configuration to the other. The diffusion of impurities and chemical reactions between the layers change upon reversal of deposition order. Detrimental impurity diffusion from the last deposited layer can be easily controlled; however, upon reversal of deposition order this layer is deposited first. Therefore, the layer has to withstand the subsequent deposition steps, leading to excessive diffusion of impurities from this layer into the upper part of the solar cell. On the other hand, a beneficial diffusion from one of the first deposited layers will be suppressed upon reversal of deposition order. The uncontrolled impurity diffusion in substrate configuration solar cells has previously resulted in inferior electronic properties of the absorber and p-n junction. In this thesis a novel process for the growth of CdTe solar cells in substrate configuration is presented, which controls impurity distribution in this configuration and enables 13.6% and 11.5% efficiency on glass and metal foil substrates, respectively.
1.2.2 Layer properties and processing

In this section the properties and growth processes of the different layers in CdTe solar cells are described using the conventional superstrate configuration.

1.2.2.1 Substrate and electrical front contact

Solar cells are deposited on a substrate, which has to withstand temperatures during subsequent processing steps. Mostly glass is employed as substrate, while low temperature growth processes ($\leq 450$ °C) also enable the growth on flexible polyimide film. The sodium content in the glass substrate is an important parameter as it significantly influences CdTe solar cell growth (cf. Chapter 3).

The first layer to be deposited in superstrate configuration is the electrical front contact (FC). Usually, transparent conductive oxides (TCOs) are used as FC. TCOs are highly doped large band gap oxide semiconductors which have both high transparency for incoming photons as well as good electrical conductivity for lateral charge transport. Typical materials are Fluorine doped SnO$_2$ (FTO) [22], tin doped indium oxide (ITO) [23], ZnO:Al [17], or Cd$_2$SnO$_4$ [21]. The layer can be deposited by different methods including sputtering [17,21], chemical vapor deposition [24], or spray deposition [25]. To achieve highest efficiency, a highly resistive and transparent (HRT) layer such as intrinsic SnO$_2$ [26], ZnO [17,27], or ZnSnO$_6$ [21] is deposited on top of the TCO. The
1.2. CdTe thin film solar cells

HRT layer allows reduction of CdS layer thickness, enabling less parasitic absorption and therefore higher short circuit current density ($J_{sc}$) [17].

1.2.2.2 CdS layer

A n-type semiconducting layer is deposited as the n-part of the p-n junction on the TCO stack. High-efficiency CdTe solar cells generally use a CdS based semiconductor as n-type layer [21], which can be deposited for example by chemical bath deposition (CBD) [21,28], CSS [29,30], high vacuum evaporation (HVE) [17,31], or sputtering [27]. CdS can be grown in wurtzite or zincblende structure, it has a band gap of ~2.4 eV, and intrinsically grows as n-type semiconductor [32, 33]. During solar cell processing the addition of chlorine during the CdCl$_2$ treatment can additionally contribute to n-type doping [34]. The use of CdS has the advantages of reduced interface defect states at the p-n junction and proper energy band alignment with the CdTe layer [35]. However, because of the relatively narrow energy band gap and because of a high recombination rate of carriers in the window layer, the CdS layer causes photocurrent loss. To reduce this loss, the CdS layer is made as thin as possible. The use of a thin CdS layer can lead to incomplete coverage of the CdS layer due to grain growth during the CdCl$_2$ treatment, leading to pinhole formation and locally occurring weak diodes. The use of the aforementioned HRT layer improves PV properties of these diodes [17]. To further reduce optical losses, alternative n-type materials are under investigation, for example Cd$_{1-x}$Zn$_x$S [36] or ZnO$_{1-x}$S$_x$ [37].

1.2.2.3 CdTe layer

CdTe is a II-VI compound semiconductor with a band gap of 1.49 eV [38] and an absorption coefficient above 10$^4$ cm$^{-2}$ [39], making it an ideal semiconductor as absorber layer in solar cells and reaching a theoretical maximum efficiency of about 30%. CdTe grows in zincblende structure and can be grown with both n- and p-type conductivity [33]. In solar cells, p-type CdTe is used and the acceptor doping is mainly achieved by copper doping, which diffuses from the back contact (BC) into the CdTe layer [40]. Acceptor doping is furthermore influenced by the heat treatment in the presence of CdCl$_2$ and oxygen [34,41,42]. One of the advantages of the CdTe technology is the simple phase diagram of CdTe and its congruent evaporation characteristics. This fa-
cilitates stoichiometric growth at high deposition rates and allows the utilization of a variety of different deposition techniques [43]. These techniques can be divided into high-temperature deposition methods (substrate temperature $\geq 550 \, ^\circ \text{C}$) like close space sublimation (CSS) [21] or vapor transport deposition [44] as well as low temperature deposition methods (substrate temperature $\leq 450 \, ^\circ \text{C}$) like sputtering [27], electrodeposition [45], and HVE [17,46].

The polycrystalline nature of the CdTe film has an impact on device performance. Grain boundaries (GBs) can induce trap states, and therefore have to be appropriately passivated [47]. When GBs are passivated, polycrystalline CdTe solar cells even outperform their single crystalline counterpart. According to a model by Visoly-Fisher et al. [48] this can be explained by the active participation of GBs in charge separation and transport, which is caused by local downward band bending close to the GBs.

1.2.2.4 CdCl$_2$ treatment

Very important for device performance is an annealing treatment of the CdS/CdTe layer stack in a chlorine and oxygen containing ambient at around 400-450 $^\circ \text{C}$ and its beneficial impact on the cell performance is widely accepted in the field of CdTe solar cells [26, 49–51]. Mostly, CdCl$_2$ is used as supply of chlorine, but also other chlorine containing chemicals, such as Freon were successfully used [52]. Several investigations on the impact of the CdCl$_2$ treatment on the structural properties were carried out [53]. In low temperature grown CdTe, the CdCl$_2$ treatment leads to recrystallization, grain growth and reduction of stacking faults in the CdTe layer [53, 54], so that CdCl$_2$ treated CdTe layers grown with various techniques have similar grain size upon CdCl$_2$ treatment. The treatment furthermore leads to interdiffusion of the CdS and CdTe layers [53]. This can reduce the number of defect states at the CdS/CdTe interface due to reduced lattice mismatch and is often reported to be important for high device performance [21, 55–57]. However, CdS-CdTe interdiffusion can also result in excessive consumption of the CdS layer, leading to weak diodes [58]. While these structural effects are enhanced by the presence of chlorine, a CdCl$_2$ treatment is also required in high-temperature grown solar cells, where it does not lead to significant structural changes [59]. This suggests that chlorine additionally has an effect on the electronic properties, which is discussed in Section 1.2.3.
1.2. CdTe thin film solar cells

1.2.2.5 Electrical back contact

The last layer to be deposited is the electrical BC. The BC should give a good electrical contact to the CdTe layer and enable high lateral conductivity. Lateral conductivity is provided by a metal layer like gold or molybdenum. Good electrical contact to the CdTe layer is challenging due to the formation of a Schottky barrier at the CdTe/metal interface, caused by the high electron affinity of the CdTe layer and Fermi level pinning at the CdTe/metal interface. Therefore interlayers like Cu₂Te [60], ZnTe:Cu [61], Sb₂Te₃ [62], antimony [62], As₂Te₃ [63], or MoOₓ [64] are used. Generally, highest efficiencies are achieved by the addition of copper during BC processing. The role of copper is discussed in Section 1.2.3.

1.2.3 Impurities

Several impurities are intentionally added during CdTe solar cells processing, namely chlorine, oxygen, sulfur and copper. Processes for highest efficiency solar cells involve the incorporation of all of these impurities.

Chlorine is incorporated during the CdCl₂ treatment, leading to a concentration of \( \sim 8 \times 10^{18} \text{ cm}^{-3} \) in the CdTe layer [59] and preferential segregation at the GBs of the CdTe layer [65]. The CdCl₂ treatment has been found to lead to improved minority carrier lifetime (MCLT) in the CdTe layer [66, 67]. GB co-passivation with chlorine and copper can contribute to this [68]. The CdCl₂ treatment has also been reported to enhance p-type conductivity [41, 42]. This is not obvious, because chlorine is a n-dopant in CdTe, but the enhanced p-type conductivity can be explained by the formation of chlorine A-centers [69].

The CdCl₂ treatment is generally performed in an oxygen containing ambient. In some processes, oxygen is additionally added during the growth of the CdS and/or CdTe layers, e.g. when grown using CSS. Oxygen addition during CSS growth decreases grain size due to increased nucleation rate, which can be important for a good CdS coverage [21, 70]. Oxygen has been reported to enhance p-type doping in CdTe solar cells [71] and CdTe thin films [72]. Furthermore, MCLT in the CdTe layer [73] has been found to increase due to addition of oxygen during the growth of the CdTe layer. Oxygen addition can furthermore have an impact on CdS-CdTe interdiffusion [74, 75].
During the CdCl$_2$ treatment, also sulfur is introduced into the CdTe layer, which diffuses from the CdS layer into the CdTe layer and forms a CdS$_x$Te$_{1-x}$ alloy at the interface. The effects of this alloy are discussed in Section 1.2.2.4.

As mentioned above, highest efficiencies in superstrate solar cells are achieved with copper added to the BC. Copper reduces the energy barrier at the CdTe/BC interface [76, 77]. Additionally, copper partly diffuses into the CdTe layer upon annealing at typically 200-250 °C, increasing MCLT and doping density in the CdTe layer [40, 78]. However, because copper is a mobile element, it can contribute to performance degradation of the solar cell [60, 79]. Therefore, processes are developed which exclude the addition of copper. Solar cells without addition of copper may, however, be more susceptible to effects of uncontrolled impurities [79] and it is difficult to exclude copper impurities in CdTe solar cells due to impurities arising e.g. from impure CdCl$_2$.

Additionally to the deliberately added impurities, sodium can diffuse from the glass substrate into the layers of the solar cell during processing and significantly affect solar cell properties as discussed in detail in Chapter 3.

### 1.2.4 Substrate configuration solar cells

In substrate configuration solar cells, the complete layer order is reversed. Several groups have tried to adapt the CdTe solar cell growth process from superstrate to substrate configuration with the goal to produce cells on flexible metal foil and/or to take advantage of improved opportunities to enhance and investigate p-n junction properties [20, 31, 80–96]. At the beginning of the thesis, efficiencies were below 8%. In the following some of the approaches to develop substrate configuration solar cells are shortly described. An overview on the development effort on CdTe solar cells on flexible metal foil until 2011 can also be found in [96].

Glass or metal foil substrates were used. Generally, molybdenum is used as BC metal because of its good thermal and chemical stability and its relatively high work function. Many investigations on substrate configuration solar cells focused on the BC buffer layer. Various materials were used as BC buffer layers, including ZnTe:Cu [80, 84], Sb$_2$Te$_3$ [91, 95], MoO$_x$ [80, 91], Cu$_x$Te [80, 84], and antimony [95]. Often, copper is added to the BC.

Various methods were used to grow the CdTe and CdS layers. The CdCl$_2$ treatment,
1.2. CdTe thin film solar cells

which is performed in superstrate configuration on the CdS/CdTe layer stack is performed in various ways in substrate configuration devices. For example a CdCl₂ treatment only after CdTe was tested [80, 82–84, 91], a CdCl₂ treatment of the CdTe/CdS layer stack [20], or a CdCl₂ treatment after both CdTe and CdS [80, 83, 88, 91]. Also a post processing annealing either after finishing the cell growth or after CdS layer deposition at relatively low temperatures around 200 to 250 °C was reported to be beneficial for device performance [80, 84].

1.2.5 Achieved laboratory efficiencies

This section and the next section are in part based on the following publication:

Table 1.1 shows the PV parameters of a selection of high-efficiency CdTe solar cells achieved in different laboratories. Information on the work of other research groups in the field of CdTe PV can be found in [30, 97–103]. In the conventional superstrate configuration on glass substrates CdTe solar cells with efficiency above 15% have been achieved with various methods including high (≥ 550 °C) and low (≤ 450 °C) temperature processes. Similar V_{oc} and FF are achieved with the different methods, indicating that good electronic quality of the CdTe layer can be achieved with various growth processes for the CdTe layer. The differences in J_{sc} originate from different transparency of the window layer stack. In 2001, NREL achieved 16.5% efficiency [21, 104], which remained the benchmark for about 10 years. Between 2011 and 2013, the record efficiency was improved several times by the companies First Solar and GE Global Research. Currently, the record value for CdTe solar cells is 19.6% [14]. This rapid advancement was mainly achieved by minimizing optical losses in the window layers in order to improve the J_{sc} of the solar cells [105]. The reported fast improvements in efficiency as well as the recently announced solar technology partnership between First Solar R&D and GE Global Research [106] provide good reasons that efficiencies above 20% might soon be possible. Furthermore, the high PV parameters (V_{oc}=903 mV, J_{sc}=28.6 mA·cm⁻² and FF=82.5%) achieved on different devices indicate prospects of even higher efficiencies.

Besides the development of CdTe solar cells on rigid glass substrate described above,
some deposition methods have been used to develop solar cells on flexible and lightweight substrates. Solar cells with efficiency up to 13.8% were achieved on flexible polyimide film in superstrate configuration [18, 19] and an 8.0% efficient mini-module was presented [107]. For high temperature grown CdTe solar cells, flexible glass can be used and efficiencies up to 14.0% were achieved [108]. An alternative approach is to reverse the layer order and to produce CdTe solar cells in substrate configuration, which allows the use of opaque substrates like flexible metal foil. In this thesis, CdTe solar cells in substrate configuration with efficiencies up to 13.6% and 11.5% on glass and flexible metal foil are presented, respectively. The configuration furthermore has a large potential to further improve efficiency.

1.2.6 Industrialization

Several companies are commercializing CdTe PV technology. Table 1.2 shows a selection of companies as well as their achieved module efficiencies. Information on other companies can be found in [112–114]. Modules with efficiencies up to 16.1% have been reported [14] and efficiencies above 17% can be expected in the near future without disruptive technology changes by implementing the recent improvement in solar cell efficiency [105]. Commercially available CdTe modules exhibit efficiencies around 10-13%.

With a module production of more than 1.8 GW, in 2012, CdTe PV technology has the second largest market share after conventional crystalline silicon modules [115]. The modules are almost entirely produced by the company First Solar, making it the third largest PV company in terms of production output in 2012 [115]. Other companies so far have reported annual production capacities below 100 MW.

In the third quarter of 2013, First Solar produced CdTe solar modules at 0.59 $/W, [116], which is among the lowest costs of all PV technologies. A clear differentiator between wafer based and thin film PV technologies is the energy payback time. Among all currently commercially relevant PV technologies, CdTe solar modules have the shortest energy payback time [117]. The energy return on investment of CdTe PV exceeds that of oil-fired electricity [118] and its compliance with environmental and safety standards is demonstrated by several studies [119].

All companies listed in Table 1.2 produce CdTe solar modules in superstrate configura-
1.2. CdTe thin film solar cells

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Substrate</th>
<th>Laboratory</th>
<th>Method</th>
<th>$\eta$ (%)</th>
<th>$V_{oc}$ (mV)</th>
<th>$J_{sc}$ (mA cm$^{-2}$)</th>
<th>FF (%)</th>
<th>$A$ (cm$^2$)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Superstrate</td>
<td>Glass</td>
<td>GE</td>
<td>CSS$^2$</td>
<td>19.6*</td>
<td>857</td>
<td>28.6</td>
<td>80.0</td>
<td>1.04</td>
<td>[14]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FSLR</td>
<td>VTD$^2$</td>
<td>19.0*</td>
<td>872</td>
<td>28.0</td>
<td>78.0</td>
<td>0.48</td>
<td>[7]</td>
</tr>
<tr>
<td></td>
<td>NREL</td>
<td>CSS$^2$</td>
<td></td>
<td>16.5*</td>
<td>845</td>
<td>25.9</td>
<td>75.5</td>
<td>1.03</td>
<td>[21]</td>
</tr>
<tr>
<td>Delaware</td>
<td>VTD$^2$</td>
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<td></td>
<td>16.4</td>
<td>835</td>
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<td>82.5</td>
<td>0.36</td>
<td>[109]</td>
</tr>
<tr>
<td>Calyxo</td>
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<td></td>
<td></td>
<td>16.2*</td>
<td>836</td>
<td>26.7</td>
<td>72.7</td>
<td>0.4</td>
<td>[110]</td>
</tr>
<tr>
<td>Florida</td>
<td>CSS$^2$</td>
<td></td>
<td></td>
<td>15.8*</td>
<td>843</td>
<td>25.1</td>
<td>74.5</td>
<td>1.05</td>
<td>[24]</td>
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<td>Parma</td>
<td>CSS$^2$</td>
<td></td>
<td></td>
<td>15.8</td>
<td>862</td>
<td>25.5</td>
<td>72</td>
<td>1</td>
<td>[46]</td>
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<tr>
<td>Empa</td>
<td>HVE$^1$</td>
<td></td>
<td></td>
<td>15.6</td>
<td>834</td>
<td>24.7</td>
<td>75.9</td>
<td>0.15</td>
<td>[17]</td>
</tr>
<tr>
<td>FSLR</td>
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<td></td>
<td></td>
<td>14.8*</td>
<td>903</td>
<td>23.3</td>
<td>70.3</td>
<td>0.48</td>
<td>[7]</td>
</tr>
<tr>
<td>Superstrate</td>
<td>Flex.</td>
<td>NREL</td>
<td>CSS$^2$</td>
<td>14.0</td>
<td>841</td>
<td>25.0</td>
<td>66.7</td>
<td>N/A</td>
<td>[108]</td>
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<tr>
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<td>Glass</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Superstrate</td>
<td>PI</td>
<td>Empa</td>
<td>HVE$^1$</td>
<td>13.8</td>
<td>846</td>
<td>22.3</td>
<td>73.4</td>
<td>0.15</td>
<td>[18]</td>
</tr>
<tr>
<td></td>
<td>film</td>
<td>Toledo</td>
<td>Sputter$^1$</td>
<td>10.5</td>
<td>768</td>
<td>19.5</td>
<td>69.8</td>
<td>N/A</td>
<td>[111]</td>
</tr>
<tr>
<td>Substrate</td>
<td>Glass</td>
<td>Empa</td>
<td>HVE$^1$</td>
<td>13.6</td>
<td>852</td>
<td>21.2</td>
<td>75.3</td>
<td>0.3</td>
<td>[93]</td>
</tr>
<tr>
<td></td>
<td>NREL</td>
<td>CSS$^2$</td>
<td></td>
<td>11.0*</td>
<td>833</td>
<td>21.8</td>
<td>60.5</td>
<td>0.43</td>
<td>[80]</td>
</tr>
<tr>
<td>Substrate</td>
<td>Metal</td>
<td>Empa</td>
<td>HVE$^1$</td>
<td>11.5*</td>
<td>821</td>
<td>22.0</td>
<td>63.9</td>
<td>0.52</td>
<td>[93]</td>
</tr>
<tr>
<td></td>
<td>foil</td>
<td>Toledo</td>
<td>HVE$^1$</td>
<td>7.8</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>0.05</td>
<td>[20]</td>
</tr>
</tbody>
</table>

**Table 1.1:** Selection of high-efficiency CdTe solar cells achieved in different laboratories. PI: Polyimide; GE: GE Global Research; FSLR: First Solar R&D; CSS: Close Space Sublimation; (AP)VTD: (Atmospheric pressure) vapor transport deposition; HVE: High vacuum evaporation; ED: Electrodeposition; Sputter: Sputtering; $^1$ low temperature ($\leq 450$ °C); $^2$ high temperature ($\geq 550$ °C); * certified efficiency.

on glass substrates. An exception is the company Xunlight 26 Solar, which is developing CdTe solar modules on flexible polyimide substrate as well as (semi-)transparent CdTe solar modules [112].

### 1.2.7 Open research questions

This section gives a short and selective overview of open research questions in the field of CdTe solar cells.
Chapter 1. Introduction

<table>
<thead>
<tr>
<th>Laboratory</th>
<th>Method</th>
<th>( \eta )</th>
<th>( V_{oc} ) (V)</th>
<th>( J_{sc} ) (A)</th>
<th>FF (%)</th>
<th>( A ) (m²)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASP</td>
<td>N/A</td>
<td>11.1 (t,p)</td>
<td>59</td>
<td>1.92</td>
<td>70.9</td>
<td>0.72</td>
<td>[120]</td>
</tr>
<tr>
<td>Antec Solar</td>
<td>CSS</td>
<td>10.0 (t,p)</td>
<td>95</td>
<td>1.25</td>
<td>61.0</td>
<td>0.72</td>
<td>[121]</td>
</tr>
<tr>
<td>Calyxo</td>
<td>APVTD</td>
<td>13.4* (ap,c)</td>
<td>0.828**</td>
<td>22.9**</td>
<td>70.3</td>
<td>0.6637</td>
<td>[122]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11.8 (t,p)</td>
<td>63.6</td>
<td>2.06</td>
<td>64.9</td>
<td>0.72</td>
<td>[123]</td>
</tr>
<tr>
<td>First Solar</td>
<td>VTD</td>
<td>16.1* (t,c)</td>
<td>68.7</td>
<td>2.25</td>
<td>74.8</td>
<td>0.72</td>
<td>[14]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12.9 (t,p)</td>
<td>60.5</td>
<td>2.11</td>
<td>72.5</td>
<td>0.72</td>
<td>[124]</td>
</tr>
<tr>
<td>GE Energy</td>
<td>CSS</td>
<td>11.5 (t,p)</td>
<td>95.0</td>
<td>1.25</td>
<td>69.5</td>
<td>0.72</td>
<td>[125]</td>
</tr>
</tbody>
</table>

Table 1.2: Selection of companies, which commercialize CdTe solar modules. ASP = Advanced Solar Power (Hangzhou); CSS: Close Space Sublimation; (AP)VTD: (Atmospheric pressure) vapor transport deposition; * certified efficiency; ** PV parameters per cell (\( J_{sc} \) in mA·cm\(^{-2}\)); (c) champion efficiency; (p) production efficiency (extracted from product data sheet); (t) total area efficiency; (ap) aperture area efficiency

Replacement of the rigid glass substrate by flexible substrates, which could allow roll-to-roll production is investigated by several research groups [18, 93, 108, 111]. This is done in superstrate configuration on flexible PI film or flexible glass. An alternative way is to reverse the deposition order, which enables the use of a variety of substrates including flexible metal foil.

Another investigated subject is the increase of window layer transmittance, while maintaining good p-n junction properties. This involves thinning of the CdS, HRT, and TCO layers and the use of alternative materials with wider band gap [17, 21, 37, 126]. The recent results of GE Global Research and First Solar R&D, reaching \( J_{sc} \) above 28 mA·cm\(^{-2}\) with a nearly rectangular external quantum efficiency (EQE) while maintaining very high \( V_{oc} \) and FF [7], show that it is possible to significantly improve window layer transmittance without adverse effects on p-n junction properties.

High-efficiency solar cells mostly apply CdTe layers with \(~3-10\ \mu\text{m}\) thickness, even though only 1 \(\mu\text{m}\) of CdTe is required to absorb 92% of the incoming sunlight with energy larger than the band gap. To overcome potential limitations by the tellurium supply [127, 128], several research groups are currently aiming at reducing CdTe layer thickness without adverse effects on device performance [129, 130].

The largest potential for further efficiency improvements is by increasing \( V_{oc} \) beyond
present values of \( \sim 860 \) mV. The \( V_{oc} \) is \( \sim 200 \) mV lower than that of single-crystalline GaAs solar cells in spite of a comparable band gap [131]. Improvement in \( V_{oc} \) is possible by improving doping in the CdTe layer or by improving MCLT [131, 132]. Various approaches are currently being tested to improve MCLT and doping density in the CdTe layer beyond present values of \( \sim 1 \) ns and \( \sim 10^{14} \text{ cm}^{-3} \), respectively [131–134] and recently up to 903 mV was reached by improving MCLT [7]. Even though these solar cells currently still have limited \( J_{sc} \) and FF, the results show that CdTe PV is not fundamentally limited at \( \sim 860 \) mV. To significantly enhance efficiency, both MCLT and doping density have to be enhanced [131, 132].

The goal of enhancing \( V_{oc} \) brings up further research questions under investigation: Which parameters are influencing MCLT and doping density? How can these parameters be improved beyond state-of-the art? What is the role of impurities and what is the precise defect structure of the CdTe layer? What is the role of GBs in doping, MCLT and carrier collection?

Another area of intensive research is the BC. BCs combining very good contact properties and long-term stability are being developed [22, 62].

### 1.3 Aim of the thesis

The aim of the thesis is the development of low temperature grown CdTe solar cells and the inversion of the conventional device structure. The thesis focuses on the investigation of the properties of the semiconductor layers, the p-n junction and the impurity distribution in the solar cell, as well as on their effects on electronic properties and photovoltaic performance.
Chapter 2

Solar cell processing and characterization

2.1 Sample preparation

2.1.1 CdTe solar cells in superstrate configuration

CdTe solar cells in the conventional superstrate configuration were grown using a low temperature process, which is described in the following.

2.1.1.1 Substrate and front contact

Unless otherwise noted, low alkaline content Corning 7059 borosilicate glass (BSG) or Corning 1737 aluminosilicate glass was used as substrate. Substrates were cleaned using hand washing with water and soap followed by an ultrasonic bath in acetone, isopropanol, and deionized water and dried with N$_2$. Al/Ni pads were deposited by electron beam evaporation on the edges of the substrate to facilitate contacting of the TCO. A double layer FC consisting of ZnO:Al and intrinsic ZnO (i-ZnO) was deposited by rf-sputtering in a vacuum chamber by AJA international, Inc. with 4 inch ceramic targets and typical base pressure of $\sim 5 \times 10^{-7}$ mbar. Deposition parameters for the ZnO:Al were 200 W rf-power, 20 sccm flow of argon, 0.3 sccm flow of O$_2$/Ar mixture (3% O$_2$), substrate temperature 300 °C, 30 minutes deposition. Deposition parameters for the i-ZnO HRT were 150 W rf-power, 20 sccm flow of argon, 7 sccm flow of O$_2$/Ar
mixture (3% O\(_2\)), substrate temperature 300 °C, 10-30 minutes deposition, leading to ZnO:Al and i-ZnO thicknesses of 1 µm and 150-400 nm, respectively.

2.1.1.2 CdS and CdTe layer

CdS and CdTe layers were deposited by evaporation from the compounds in a vacuum chamber with a base pressure of typically 5\(\times\)10\(^{-7}\) mbar. A CdS layer with a thickness of typically 130 nm was deposited at a substrate temperature of 160 °C using growth rates of ~2 Å/s, followed by vacuum annealing at 420 °C for 30 minutes. For highest efficiency devices, thinner CdS layers were used. Without breaking the vacuum, 4-6 µm of CdTe was deposited at a substrate temperature of 350 °C and growth rates of typically 15-20 Å/s.

2.1.1.3 CdCl\(_2\) treatment

A layer of CdCl\(_2\) with a thickness of 400 nm was evaporated at 5-10 Å/s in vacuum (typical pressure 5\(\times\)10\(^{-6}\) mbar) from the compound on the CdTe layer. Subsequently, the sample was annealed in air or O\(_2\)/Ar mixture (30% O\(_2\)), typically at 420 °C for 25 minutes. Residual CdCl\(_2\) was removed with deionized water, followed by drying with N\(_2\).

2.1.1.4 Back contact and copper doping

A Cu/Au electrical BC was applied on the CdTe. CdTe was etched with diluted bromine in methanol (0.07%, 4 seconds) and cleaned in isopropanol. 2.5 nm of copper and 60-80 nm of gold were applied by vacuum evaporation through a mask at ≤ 10\(^{-5}\) mbar, defining cell area of 0.15 cm\(^2\). Finally, the finished devices were annealed at 215 °C for 20 minutes in air. In selected cases, an anti-reflection (AR) coating (~100 nm of MgF\(_2\)) was applied on the glass side of the substrate.

2.1.2 CdTe solar cells in substrate configuration

The developed process for the growth of CdTe solar cells in substrate configuration is described in the following.
2.1. Sample preparation

2.1.2.1 Substrate and back contact

Solar cells were grown on Corning 7059 BSG. Substrates were cleaned using hand washing with water and soap followed by an ultrasonic bath in soap water and deionized water and dried with N\textsubscript{2}. For the growth of solar cells on flexible metal foils, molybdenum foil (50 µm thickness), or steel foil substrates (30 µm thickness) were used. They were washed with a sponge using soap and water and ultrasonic bath in deionized water. On steel foil, best results were obtained when applying a Ti/TiN impurity diffusion barrier layer with a thickness of 60/230 nm by pulsed DC sputtering.

As electrical BC a molybdenum layer was deposited by DC sputtering at a base pressure of about $1 \times 10^{-7}$ mbar. Three consecutive layers of molybdenum were deposited using the following parameters: 1200 W, 17 sccm argon flow, 90 s; 1200 W, 38.5 sccm argon flow; 500 W, 46 sccm argon flow, resulting in a total molybdenum thickness of about 600 nm. As BC buffer layer ~150 nm of MoO\textsubscript{3} was evaporated from the compound at typical base pressure of $1 \times 10^{-6}$ mbar. The MoO\textsubscript{3} layer reacts to MoO\textsubscript{2} during solar cell processing [92]. In most cases a tellurium capping layer with a thickness of ~50 nm was deposited to protect the MoO\textsubscript{3} during transfer through air into the CdTe evaporation chamber. The tellurium layer re-evaporates upon heating before CdTe deposition [92].

2.1.2.2 CdTe layer, annealing treatment and doping

CdTe with a thickness of 4-6 µm was deposited by HVE (typical base pressure $5 \times 10^{-7}$ mbar) from the compound at a substrate temperature of 350 °C at 15-20 Å/s. A CdCl\textsubscript{2} treatment of the CdTe layer (called CdTe treatment) was performed by deposition of 400 nm of CdCl\textsubscript{2} in high vacuum from the compound followed by annealing at typically 435 °C for 25 minutes in an O\textsubscript{2}/Ar mixture typically containing 40% of O\textsubscript{2}. Samples were cleaned with DI water and dried with N\textsubscript{2}. The CdTe layer was doped by depositing copper by HVE at a pressure $\leq 10^{-5}$ mbar followed by annealing to promote diffusion of copper into CdTe. The annealing was done at 400 °C for 20 minutes in an O\textsubscript{2}/Ar mixture containing 40% of O\textsubscript{2}. Unless otherwise noted, the evaporated copper layer had an equivalent thickness of 1.2 Å, which corresponds to $1 \times 10^{15}$ copper atoms cm\textsuperscript{-2}. Copper was evaporated at a rate of ~0.03 Å/s and the copper thickness was controlled with a quartz crystal microbalance, which was calibrated by evaporating 50 nm of copper on a glass slide at a rate of ~0.03 Å/s and measuring the resulting thickness with a
2.1.2.3 CdS layer and annealing treatment

CdS was grown using CBD in a water bath at 70 °C from a precursor solution of cadmium acetate (0.0016 mol/l), ammonium hydroxide (1.48 mol/l) and thiourea (0.022 mol/l) in deionized water. Typical reaction time was 18 minutes, resulting in a CdS layer with ~60 nm thickness. A CdCl$_2$ treatment of the CdS layer (called CdS treatment) was performed by vacuum evaporation of 100 nm of CdCl$_2$ followed by annealing at temperatures between 360 and 400 °C for 25 minutes in an O$_2$ containing ambient (mostly 50% O$_2$). Unless otherwise noted, a second CdS layer was subsequently deposited by CBD as described above.

2.1.2.4 Front contact

A double layer FC consisting of i-ZnO and ZnO:Al was deposited in the vacuum system described in Section 2.1.1.1 without intentional substrate heating. Deposition parameters for the i-ZnO were 150 W rf-power, typically 12 minutes deposition, 45 sccm flow of argon, 16 sccm flow of O$_2$/Ar mixture (3% O$_2$). Deposition parameters for the ZnO:Al were 200 W rf-power, 10-25 min deposition, 20 sccm flow of argon, 0.29 sccm flow of O$_2$/Ar mixture (3% O$_2$) leading to i-ZnO and ZnO:Al thicknesses of about 250 nm and 350-900 nm, respectively. Mostly, a metallic Ni/Al grid with thicknesses of 50/2000 nm was applied by electron beam evaporation at evaporation rates of ~5/20 Å/s for improved FC conductivity. In most cases, nominally 85 nm of MgF$_2$ was deposited at a rate of ~5 Å/s as AR coating by electron beam evaporation. The cell area was defined by mechanical scribing and cells were mostly scribed to nominally 0.3 cm$^2$ or 0.57 cm$^2$ (when a grid was applied) and to nominally 0.15 cm$^2$ in earlier devices when no grid was applied.

2.1.2.5 Post-processing annealing

The completed solar cells were annealed at 190-250 °C (mostly 210 °C) in air for 10 minutes and cooled down rapidly to room temperature. This post-processing annealing was introduced, but its effect is not analyzed in detail in the present thesis and its effect
2.1. Sample preparation

is therefore shortly discussed in the following.

Depending on other processing conditions (e.g. the annealing conditions during the CdS treatment), the post-processing annealing had very different effects on device performance and could lead to an increase or a decrease in device performance. The effect of this post processing on the solar cells presented in this thesis were not as significant as in the devices discussed by Dhere et al. [80], likely because in the present solar cells an additional CdCl$_2$ treatment is used after the CdS layer deposition. Also without the post-processing annealing, efficiencies up to 13.2% were achieved. However, highest cell efficiency was obtained with this annealing step. The post processing annealing is believed to result in a redistribution of copper atoms and/or formation of certain copper related defects.

2.1.3 CdTe thin films on glass

CdTe thin films for resistivity and Hall effect measurements were prepared by depositing CdTe layers with a thickness of ~5 µm on Corning 7059 BSG. Copper doped samples were subsequently annealed with CdCl$_2$ and doped with copper as described in Section 2.1.2.2.

Arsenic doped samples were prepared by placing as-deposited CdTe thin films on BSG and CdTe thin films on BSG/Mo/MoO$_x$ together with pieces of arsenic (4-1000 mg) in a glass ampoule, followed by evacuation and sealing. All arsenic doped samples discussed in this thesis were annealed at 500 °C for 18 hours to allow evaporation and incorporation of arsenic into the CdTe layer. If an additional CdCl$_2$ treatment and copper doping were performed, standard treatments as described in Section 2.1.2.2 were done after arsenic doping.

The electrical contacts to CdTe thin films were made by vacuum evaporation of gold through a mask. For resistivity measurements line contacts with distances between 0.2 and 2 mm were used and for Hall effect measurements point contacts in van der Pauw geometry were employed.
2.2 Characterization

2.2.1 Structural characterization

2.2.1.1 Electron microscopy and X-ray spectroscopy

Structural properties of layers and solar cells were analyzed by scanning electron microscopy (SEM) using a Nova NanoSEM 230, Philips XL30 ESEM-FEG, or Hitachi S-4800. Typically 5 kV accelerating voltage was used. Samples for cross-section SEM were prepared by breaking and in some cases (Chapter 3) etching in bromine methanol solution. Carbon coating was applied to reduce sample charging. Elemental composition analysis was conducted using energy dispersive X-ray spectroscopy (EDX) at a relatively low accelerating voltage of 5 kV to minimize the excitation volume.

The microstructure of the double layer CdS in substrate configuration solar cells was investigated by scanning transmission electron microscopy (STEM). STEM analysis was performed on a JEOL 2200FS TEM/STEM operated at 200 kV. Samples for STEM were prepared by mechanical polishing of cross-sections followed by argon ion milling using a Fischione TEM ion mill 1050 employing the liquid nitrogen cooling option.

2.2.1.2 Ex-situ and in-situ X-ray diffraction

Crystal phases were analyzed by ex-situ X-ray diffraction (XRD) measurements using a Siemens Diffractometer D5000 in $\Theta$ - 2$\Theta$ mode operated at 40 kV and 37 mA. To investigate the phase of a thin CdS layer or the surface region of the CdTe layer in substrate configuration, grazing incidence XRD (GIXRD) measurements were carried out using a fixed grazing incidence angle of 3°. CdS-CdTe intermixing is investigated at relatively large angles of 60° to 80° in order to maximize the possibility of detecting a potential tellurium rich CdS$_{2x}$Te$_{1-x}$ phase close to the CdTe surface.

In-situ XRD patterns during the annealing treatment of the CdS layer in substrate configuration were recorded using a PANanalytical Xpert Pro MPD X-ray diffractometer. 2$\Theta$ scans were recorded with fixed grazing incidence angle of 3°. XRD patterns of a solar cell processed up to the first CdS layer were recorded at temperatures between 150 °C and 450 °C (10 °C steps, 1.5 °C/min ramping speed) in an ambient containing 50% of O$_2$. The experiment was performed both with and without a CdCl$_2$ layer (100 nm) on
the CdS.

### 2.2.2 Elemental distribution and concentration

#### 2.2.2.1 Secondary ion mass spectroscopy

Depth dependent elemental distribution was investigated by secondary ion mass spectroscopy (SIMS) with a TOF-SIMS\textsuperscript{5} from ION-TOF using dual beam depth profiling. For the depth profiles with high mass resolution and low lateral resolution Bi\textsuperscript{+} ions with energy of 25 keV and a current of 1-1.3 pA were used as primary ions and an area of (100 µm)\textsuperscript{2} was analyzed. For the investigation of electropositive ions, sputtering was done using O\textsuperscript{2+} (2 kV, 400 nA) and positive secondary ions were detected. For the investigation of electronegative ions, sputtering was done using Cs\textsuperscript{+} (2 kV, 120 nA) and negative secondary ions were detected. In both cases, an area of (300 µm)\textsuperscript{2} was sputtered for 2 s after each analysis step.

SIMS measurements in Chapter 3: For better visibility, SIMS data has been shifted so that the ZnO layer, as observed from the upcoming O\textsuperscript{−} (negative ions) or the upcoming Zn\textsuperscript{+} (positive ions) signal, coincides for the different samples.

SIMS measurements in Chapter 5: Mechanical lift-off was achieved after gluing the solar cell on a glass slide. Sulfur signal in the BC region is not shown because of an overlap with \textsuperscript{16}O\textsuperscript{2} and a large oxygen signal. The sputter time of the sample without CdS treatment was compressed by about 10\% to account for different sputter velocities.

SIMS measurements in Chapter 6: Quantification of SIMS copper counts in CdTe was done by comparing the normalized copper SIMS signal (\textsuperscript{63}Cu\textsuperscript{+}/\textsuperscript{114}Cd\textsuperscript{+}) in the absorber with the normalized copper SIMS signal of a CdTe thin film on glass/Mo with a known copper concentration. The copper concentration in the CdTe thin film was determined using inductively coupled plasma mass spectrometry (ICPMS).

To investigate lateral impurity distribution arising from the polycrystalline nature of the CdTe layer, SIMS was used in imaging mode (Chapter 5). For SIMS chemical imaging the lateral resolution was tuned to 400 nm (Full width at half maximum, FWHM) whereas the technique has the capability of a lateral resolution of about 100-200 nm [135]. The aforementioned settings were used with the following changes: Primary Bi\textsuperscript{+} ions had a current of 0.15 pA and an area of (20 µm)\textsuperscript{2} with 128×128 pixel was analyzed. 0.2 s
sputtering time with Cs$^+$ was used after each analysis step. For the evaluation 1000 consecutive scans were added for one 2D image after dynamic drift correction. 2D plots were cut to a size of (15 µm)$^2$ for 3D evaluation. Sulfur and chlorine counts between 2 and 8 (sulfur) and between 15 and 100 (chlorine) are shown. Mass resolution in imaging mode is not sufficient to distinguish between $^{32}\text{S}$ and $^{16}\text{O}_2$, however, high-mass resolution mode (Figure 5.4e) reveals, that influence of elements other than $^{32}\text{S}$ are small (3-4%) compared to the sulfur signal. The chlorine concentration within the CdTe grains was quantified by comparing the chlorine SIMS signal within the grain with the quantified chlorine SIMS counts at the GBs. The chlorine SIMS counts at the GBs were quantified by comparison with the concentration determined from atom probe tomography (APT) after weighting with the apparent GB width measured with the two methods. Quantification of non-imaging chlorine SIMS counts was done by normalization to the average grain/GB concentration, which was estimated using the determined chlorine concentration values in the grains and at the GBs and assuming cubic grains with 2.5 µm grain size.

### 2.2.2.2 Inductively coupled plasma mass spectroscopy

For quantification of copper traces in copper doped, CdCl$_2$ treated CdTe thin films on glass/Mo, an Agilent 7500ce ICPMS apparatus was used, performing external calibration from certified single elemental standards (1 mg/ml). Only high purity PE-LD or Teflon vessels were employed during sample preparation and measurement. For the analysis, approximately 25 mg of the absorber were scratched with the tip of a glass pasteur pipette from the Mo layer and dissolved in 10 ml 65% nitric acid. Afterwards, the acidic solution was adjusted to a final volume of 50 ml with deionized water. For quality assurance, a reference material (NIST SRM 1643e) and spiking of known copper concentrations to the measurement solution was conducted, resulting in recoveries not lower than 90%.

### 2.2.2.3 Atom probe tomography

To investigate impurity distribution in the vicinity of CdTe GBs, APT measurements were performed. Sample preparation was completed via standard lift-out techniques [136], using an FEI Helios 600i and an Omniprobe micromanipulator at EMEZ followed by
2.2. Characterization

mounting to Si microtip substrates supplied by Cameca. Annular milling and low-kV cleaning steps were applied to achieve apex radii of <100 nm and remove residual Ga implantation. Data collection was completed on a Cameca LEAP 4000X-HR with 160 kHz laser pulse repetition rate and a specimen temperature of 65 K, ensuring field evaporation parameters were held consistent during the analysis. Data reconstruction and evaluation was completed with IVAS 3.6.6 (Cameca). Peak overlap between $^{32}$S and $^{16}$O$_2$ exists, but the potentially sulfur related peaks are attributed to $^{32}$S because the presence of sulfur in CdTe and its accumulation at the GBs was already proven by SIMS measurements and because no $^{16}$O was detected.

2.2.2.4 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) measurements were performed in a Quantum2000 from Physical Electronics using a monochromatized Al K$_\alpha$ source (1486.6 eV). All measurements were done in the fixed analyzer transmission mode. A pass energy of 58.7 eV and an energy step width of 0.125 eV were used. Binding energy ($E_B$) was calibrated to Au 4f$_{7/2}$ = 83.96 eV. No ion or electron neutralizers were used. Depth information was obtained by sputtering the sample gently in steps of 30 seconds with Ar$^+$-ions using an acceleration voltage of 500 V. All spectra were evaluated with the CasaXPS software package (Version 2.3.16dev85) [137], further a Shirley background correction and a Gauss-Lorentzian product were used for peak fitting. Elemental concentrations were calculated taking into account the Scofield factors, the asymmetry function and the transmission function [138]. Errors given in $E_B$ are the standard deviation of a minimum of 10 measurement points within a layer.

2.2.3 Electrical characterization

2.2.3.1 Current-voltage and spectral response

The performance of the processed solar cells was evaluated using current density-voltage ($J$-$V$) and EQE measurements.

$J$-$V$ characteristics of solar cells in substrate configuration were measured in a steady-state sun-simulator under simulated standard-test conditions (25 °C, 1000 Wm$^{-2}$, AM 1.5G illumination). For solar cells in superstrate configuration, a halogen lamp was
used for early devices, while a combination of a halogen lamp and LED was used in later devices [18]. The irradiation power is calibrated with a crystalline silicon reference cell. Spectral mismatch correction was performed using EQE measurements. The PV parameters $V_{oc}$, $J_{sc}$ and FF and the resulting efficiency are extracted.

The spectrally resolved response of the solar cells was measured using EQE measurement. EQE was measured with a lock-in amplifier. A chopped white light source (900 W, halogen lamp, 360 Hz) and a dual grating monochromator generated the probing beam. A certified mono-crystalline Si cell from Fraunhofer ISE was used as the reference cell. Cell temperature was controlled at 25 °C with peltier cooling and white light bias was applied. The absorber band gap was determined from EQE measurements by plotting $(h\nu \text{EQE})^2$ against $h\nu$ in the region of the cut-off wavelength and extrapolating to the x-axis. The error in the determination of the absorber band gap from the EQE measurements is approximately 0.003 eV. The measured absorber band gap is additionally influenced by other parameters like MCLT which change collection of charge carriers generated deep inside the absorber by photons with energy close to the absorber band gap.

$J-V$ and EQE characteristics shown in Figure 8.2 and the corresponding PV parameters in Table 8.2 were independently measured and certified by Fraunhofer ISE, Freiburg, Germany.

### 2.2.3.2 Capacitance measurements

Capacitance-voltage ($C-V$) measurements of solar cells were performed with an Agilent E4980A precision LCR meter at a frequency of 300 kHz, an oscillating voltage of 50 mV, and bias voltages between -1.5 and +0.5 V. Assuming the solar cell to be a plate capacitor with a one-sided n$^+$-p junction the apparent acceptor concentration $N_a$ of the p-doped side can be written as [139,140]

$$N_a(x) = \frac{-2}{q\epsilon_0\epsilon_r A^2} \left( \frac{d(1/C^2)}{dV} \right)^{-1}$$

(2.1)

with the apparent profiling depth $x = \epsilon_0\epsilon_r A/C$, the elemental charge $q$, the vacuum permittivity $\epsilon_0$, the relative permittivity $\epsilon_r = 10$ and the area of the solar cell $A$. To extract the apparent hole density and space charge region (SCR) at 0 V a constant temperature of 25 or 30 °C was used. A varying temperature, e.g. between 203 and 343 K (typically
2.2. Characterization

20 K step size) was used to extract the apparent shallow acceptor concentration, which was evaluated from the minimum of the apparent acceptor concentration.

Admittance spectroscopy (AS) measurements were performed to investigate the energy distribution of defect states within the energy band gap in the CdTe layer of solar cells [141, 142]. The frequency dependent capacitance was measured with an Agilent E4980A precision LCR meter at varying frequency between 100 Hz and 2 MHz without applied bias at temperatures between 193 K and 303 K (10 K step size). Evaluation was done following [141]. The key is that the contribution of defects to the capacitance due to charging and discharging depends on the applied frequency and temperature. Depending on the energy position in the valence band and attempt to escape frequency of the defect, the defect can follow the applied frequency. Variation of frequency and temperature therefore allow to deduce the energy spectrum of defects within the energy gap.

2.2.3.3 Time-resolved photoluminescence

Time-resolved photoluminescence (TRPL) was used to measure MCLT in the CdTe layer of the solar cells. TRPL was measured with a near infrared compact fluorescence lifetime spectrometer C12132 by Hamamatsu using a YAG excitation laser with a wavelength of 532 nm, a spot size of 3 mm and an excitation power of 42.4 mW (Chapter 6) or 8.2 mW (Chapter 5) and a repetition rate of 15 kHz. The system had a time resolution of approximately 0.2 ns. The detection wavelength was set to the photoluminescence (PL) maximum at 825 nm (substrate configuration) or 835 nm (superstrate configuration) and light was detected using a photomultiplier tube. MCLT was evaluated using deconvolution and fitting of the initial section of the PL decay with a single exponential function [73].

Figure 2.1 shows the impact of variation of laser energy by three orders of magnitude on the MCLT. MCLT is constant for high laser energy, while a lower laser energy results in longer measured MCLT. High laser powers were used in the presented experiments to be in the region of constant MCLT and to characterize the recombination properties in the CdTe layer in the presence of a p-n junction [143].
2.2.3.4 Electron beam-induced current

Electron beam-induced current (EBIC) measurements were performed to identify the position of efficient charge carrier collection in the solar cell. EBIC measurements were performed in a FEI Strata 235 Dual Beam focused ion beam and secondary electron microscopy at accelerating voltage of 25 kV and spot size 3 without applied bias at the cell. The current was measured with a SR570 Preamplifier from SRS at a gain of $10^7$. Samples were prepared by mechanical cleaving and electrical contacts to the FC and BC were made with silver paste and indium wires.

2.2.3.5 Resistance and Hall effect measurements

In-plane resistivity of CdTe thin films was measured at room temperature in the dark using a Keithley 2400 Source Meter. The contact resistance was separated from bulk resistance using the transmission-line method by altering the contact distance from 0.2 mm to 2 mm. The contact resistance was found to be smaller than 7% of the total resistance at 2 mm contact distance.

To investigate carrier density and type as well as carrier mobility in CdTe thin films on glass, Hall effect measurements were performed. Measurements were made with a HMS 3000 Hall effect measurement system at room temperature in the dark using van der Pauw geometry. The given error is the standard deviation of the mean of more than 10 measurements.
2.2. Characterization

2.2.4 SCAPS simulations

The 1-D solar cell simulation software SCAPS (version 3.1.02) [144] was used for simulations of $J-V$ and EQE measurements (Chapter 6). The SCAPS definition file CdTe-base.def (22.5.2009) was used for simulation of the optimally doped sample with the following modifications: CdTe and CdS layer thicknesses were set to 5 µm and 100 nm, ZnO electron affinity was set to 4.4 eV instead of using the value of SnO$_x$, and hole capture cross-section of the donor-type mid-gap defect in CdTe was set to $1 \times 10^{-13}$ cm$^2$. A series resistance of 3 Ω cm$^2$ was included and reflection was reduced to 6%. To simulate the relatively deep acceptor-type defect states of copper in CdTe, the shallow acceptor concentration in CdTe was set to zero and an acceptor-type defect with energy of 220 meV above the valence band (Cu$^{+}$ [145]) was introduced. Acceptor-type defect concentration was set to $6.5 \times 10^{14}$ cm$^{-3}$ and hole and electron cross-sections of $1 \times 10^{-15}$ cm$^2$ were used. The concentration was chosen to result in a hole density of $3.8 \times 10^{14}$ cm$^{-3}$ in the CdTe layer outside the SCR consistent with the value determined by Hall effect measurements. The cell without copper doping was simulated by using the aforementioned values with the concentration of the acceptor-type defect set to zero. Furthermore, the majority carrier barrier height at the electrical BC was set to 0.7 eV instead of the default value of 0.4 eV.

For simulation of the sample with excessive copper doping, the aforementioned values of the optimally doped sample were used but the concentration of the acceptor-type defect was increased to $1 \times 10^{15}$ cm$^{-3}$. Furthermore, a compensating donor-type defect was introduced with concentration of $9 \times 10^{14}$ cm$^{-3}$, energy of 380 meV below the conduction band [Cu$^{+}$, [145]], and electron and hole capture cross-sections of $1 \times 10^{-11}$ cm$^2$ and $2 \times 10^{-14}$ cm$^2$, respectively.

The energetic position of the acceptor-type defect Cu$_{Cd}$ is under debate. Proposed values range between 150 and 350 meV above the valence band. The value from Wei et al. of 220 meV is used for the simulations [145].
Chapter 3

Effect of sodium on structural and electronic properties

This chapter is in part based on the following publication:

3.1 Introduction

Alkaline metals are highly mobile elements with small activation energies (<1 eV) for diffusion in CdTe [146]. Sodium is present in significant amounts in glass substrates and can diffuse into the active layers of the solar cell depending on the processing temperatures and barrier layer properties. Sodium can act as a shallow acceptor in CdTe with low activation energy of 59 meV [147], which can result in an increased acceptor concentration and $V_{oc}$ [131]. Still, highest efficiency CdTe cells are obtained on glass with low sodium content, e.g. BSG [21]. CdTe solar cells on low cost soda-lime glass (SLG) usually require an appropriate barrier layer to block sodium diffusion from the glass substrate, but during a complete growth process, sodium can still diffuse through the barrier layer [148]. Significant amounts of sodium are commonly observed in CdTe solar cells on glass [59, 149]. Despite the high importance, only few published studies describe the effect of sodium on CdTe solar cells. Dhere et al. [150] observed that the
presence of a NaF layer on CdS increases the grain size of CdTe layers when grown in helium ambient, while the effect is less pronounced when CdTe was deposited in the presence of oxygen. Durose et al. [151] found grain growth of CdS layers deposited by CBD on FTO when heated in the presence of NaCl. They reported an effect of “weakening the grain boundary interfaces” of CdTe. A strong decrease in cell performance was found when sodium was added, while it was suggested that impurity diffusion from glass substrates was beneficial [151].

This chapter describes the influence of sodium on the structural and PV properties of low temperature processed CdTe solar cells in superstrate configuration and shows the reasons for detrimental effects of sodium on the solar cell performance. The performance of the TCO ZnO:Al as barrier against sodium diffusion from SLG was evaluated and was found to be sufficient for low temperature processed CdTe solar cells.

### 3.2 Microstructure of CdTe and CdS

Vacuum evaporated CdTe is deposited with an average grain size of about 0.5 µm, which increases upon recrystallization during the subsequent CdCl$_2$ treatment. The influence of sodium on the microstructure of CdTe upon CdCl$_2$ treatment was evaluated by depositing a thin layer of NaF with varying thickness between 0 and 12 nm on top of CdTe before the CdCl$_2$ treatment and was investigated by top-view SEM of finished solar cells (Figure 3.1a,b). CdTe grain size increases with increasing amount of sodium present during recrystallization, in line with the observations of Dhere et al. [150]. An increase in average CdTe grain size from 4.1±0.5 µm for the baseline sample without added sodium to 6.5±0.5 µm was observed when 12 nm NaF was included in the CdCl$_2$ treatment. Such an increase in grain size can have positive effects on device performance, but in the present case the increase in grain size was accompanied by a widening of the GBs. Wide GBs and round grain edges in CdTe were observed, most probably because of a change in CdTe surface energy due to the presence of sodium during recrystallization. The surface energy is minimized by these microstructural features. The modification of GBs can lead to conducting shunt paths through the CdTe layer, which electrically shorten the solar cells resulting in a lower parallel resistance, as observed in $J-V$ measurements (Section 3.8).

SEM cross-section images were used to determine the influence of sodium on the mi-
3.2. Microstructure of CdTe and CdS

crostructure of CdS (Figure 3.1c-f). The baseline cell, CdCl$_2$ treated without added sodium (Figure 3.1c), has a uniform small grained CdS layer almost completely covering the TCO layer, while CdS is strongly recrystallized even when only 1.5 nm NaF is used (Figure 3.1e). The CdS film has transformed into distributed large droplet-like CdS grains. Sodium therefore appears to similarly affect the surface energy of CdS and CdTe, leading to the formation of rounded grains. The formation of droplet-like CdS is especially undesired as it leaves regions where no CdS layer exists and in these places CdTe or Te-rich CdS$_x$Te$_{1-x}$ directly forms the p-n junction with the TCO. These p-n junction have inferior properties from PV point of view [17]. As depicted in Figure 3.1d, the addition of 12 nm of NaF results in completely consumed CdS due to excessive CdS-CdTe intermixing (Section 3.4). Furthermore, SEM cross-section images also show the widening of GBs in the absorber and near to the TCO.

![Figure 3.1: a,b) SEM top-view images of the morphology of CdCl$_2$ treated CdTe layers without NaF (a) and in the presence of 12 nm of NaF (b). c-e) SEM cross-section images of CdTe solar cells CdCl$_2$ treated with 0 nm (c), 12 nm (d), and 1.5 nm (e) of NaF. An EDX line scan of sulfur (f) parallel to the ZnO interface shows that the round grains are CdS or sulfur-rich CdS$_x$Te$_{1-x}$.](image-url)
3.3 Influence on spectral response

EQE measurements showed enhanced response in the blue wavelength region for the cells CdCl$_2$ treated in the presence of sodium (Figure 3.2a, Arrow 1). The enhanced response results from consumption of CdS during cell processing, which reduces parasitic absorption, and therefore more photo-generated carriers are contributing to the current. The nearly rectangular shape of the EQE curve indicates that the addition of a thin layer of 1.5 nm NaF leads to almost complete consumption of CdS. Such CdS consumption during CdCl$_2$ annealing treatment is commonly observed due to CdS-CdTe intermixing [50,58]. Excessive intermixing can result in direct connections between the absorber and the TCO electrical FC, giving rise to inferior p-n junction properties, which reduce $V_{oc}$ and FF [58,152]. XRD and SIMS measurements confirm that the excessive consumption of CdS observed by EQE for CdCl$_2$ treated samples in the presence of sodium originates from enhanced CdS-CdTe intermixing (Section 3.4).

EQE in the long wavelength region (> 550 nm) decreases with increasing amount of NaF which can be caused by lower collection efficiency (Figure 3.2a, Arrow 2). This assumption is confirmed by a reduced SCR width as observed with $C-V$ measurements at room temperature (Table 3.1). A reduced SCR can be caused by an increased acceptor concentration of the absorber when sodium replaces cadmium atoms [147]. A strongly increased apparent acceptor concentration due to the addition of NaF was measured by $C-V$ measurements (Figure 3.2b). Nevertheless, the apparent hole density is lower than expected if all sodium was electrically active as shallow acceptor because of the spontaneous creation of compensating donors, which is known to limit shallow acceptor concentration in CdTe [33]. Furthermore, the consumption of CdS might have an influence on the SCR as it results in ZnO/CdTe junctions in parallel to CdS/CdTe junctions, which have different band alignments. The SCR width of the ZnO/CdTe junction has been measured to be smaller than the SCR width of the CdS/CdTe junction [17]. The different microstructure of the CdTe layer might also indirectly influence acceptor concentration in the CdTe layer by changing diffusion of copper into the CdTe layer during back contact processing, which significantly influences acceptor doping of the CdTe layer (Chapter 6).

The addition of small amounts of sodium did not significantly affect the long wavelength cut-off at about 850 nm corresponding to the minimum band gap of the absorber (Figure 3.2a & Table 3.1) because it is governed by the miscibility gap of the CdS-CdTe
system [153]. Only for the largest sodium contents, a slightly larger band gap, corresponding to smaller sulfur content was measured (Table 3.1). This is due to complete CdS-CdTe interdiffusion, as measured by XRD and SIMS for the largest sodium content. In this case the minimum absorber band gap is not governed by the miscibility gap, but by the limited availability of sulfur from CdS.

![Figure 3.2](image_url)

**Figure 3.2:** a) EQE measurements of solar cells processed in the presence of different amounts of NaF. b) Depth dependent apparent acceptor concentration as determined by C-V measurements at room temperature.

### 3.4 CdS-CdTe intermixing

XRD measurements of finished cells are shown in Figure 3.3a. Magnification of the CdTe related peaks revealed a change in the lattice constant in the absorber material due to the addition of NaF. This is shown in Figure 3.3b for the CdTe 331 peak. With increasing NaF thickness, the CdTe 331 peak intensity decreases, while a peak at slightly larger angle appears with increasing intensity. This can indicate a change in strain in the CdTe or an enhanced CdS-CdTe intermixing. SIMS measurements confirmed the enhanced CdS-CdTe intermixing (see below); hence it can be concluded that the additional XRD-peak corresponds to CdS$_x$Te$_{1-x}$. The change in XRD peak position corresponds to a change in lattice constant from 6.476 Å to 6.464 Å and 6.461 Å from the sample without addition of NaF to the 1.5 nm and 12 nm NaF sample, respectively. Using the Vegard’s law, the sulfur content of the probed CdS$_x$Te$_{1-x}$ layers
Table 3.1: PV parameters and parallel resistance $R_P$ of solar cells which were CdCl$_2$ treated with different amounts of NaF and of a device on SLG. SCR width at room temperature and minimum absorber band gap $E_G$ as determined from $C$-V and EQE measurements, respectively are also shown. *: short annealing treatment (10 instead of 25 minutes). No AR coating was applied.

could be determined to be 1.8% and 2.3% for the 1.5 nm and 12 nm NaF sample, respectively [154]. A similar change in XRD peak position was observed for all CdS$_{x}$Te$_{1-x}$ diffraction peaks. Table 3.2 shows the sulfur content of CdS$_{x}$Te$_{1-x}$ as determined from different XRD peaks. Very similar sulfur contents were observed for the different diffraction peaks, indicating that CdS-CdTe intermixing is independent of grain orientation. A slight change in $x$ from the sample with 1.5 nm to 12 nm of NaF shows that the sulfur content close to the BC changes. This does not contradict the finding that the minimum absorber band gap is not changed, as it is determined by the sulfur content close to the CdS/CdTe interface while XRD probes the absorber close to the BC. Texture of CdTe was also influenced by the presence of NaF, but no clear trend was found.

SIMS measurements were performed to evaluate the influence of sodium on the sulfur distribution in the CdS/CdTe layer stack. While CdCl$_2$ treated cells without additional sodium show a relatively small intermixed region (Figure 3.3c), the addition of only 1.5 nm of NaF expands the intermixed region throughout the absorber. Cells treated with 12 nm of NaF exhibit a complete interdiffusion of CdS and CdTe and homogeneously distributed sulfur in the absorber. This shows that the presence of sodium during CdCl$_2$ treatment leads to strongly enhanced CdS-CdTe intermixing.
Figure 3.3: a) XRD overview spectra of finished cells. The peaks corresponding to Te rich \( \text{CdS}_x \text{Te}_{1-x} \) and \( \text{ZnO} \) 002 (*) are labeled. b) XRD measurements of the \( \text{CdTe} \) 331-peak. XRD data is normalized to the same area under the XRD pattern. c) SIMS measurements of the sulfur distribution in samples which were \( \text{CdCl}_2 \) treated in the presence of different amounts of NaF.

3.5 Alternative sodium source

Experiments were also performed with NaCl replacing NaF in order to exclude the possibility of fluorine to be responsible for the observed effects. The experiments showed a similarly enhanced consumption of CdS and grain growth of CdTe. Therefore, it is concluded, that these structural changes are indeed caused by the presence of sodium.
Chapter 3. Effect of sodium on structural and electronic properties

<table>
<thead>
<tr>
<th>NaF thickness (nm)</th>
<th>S content (%) in CdS$<em>x$Te$</em>{1-x}$ from different XRD peaks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td>1.9 1.8 1.9 1.8 1.9 2.0</td>
</tr>
<tr>
<td>12</td>
<td>2.2 2.3 2.2 2.3 2.3 2.4</td>
</tr>
</tbody>
</table>

Table 3.2: Sulfur content of the intermixed CdS$_x$Te$_{1-x}$ phase as determined from different XRD diffraction peaks and calculated with the Vegard’s law. The 111 orientation is not included as the corresponding small angle prohibited reliable determination of the sulfur content.

3.6 Impact of CdCl$_2$ annealing conditions on recrystallization

A change in recrystallization during the CdCl$_2$ treatment - as observed for samples processed with addition of sodium - can also occur by changing CdCl$_2$ treatment conditions. This is illustrated in the following by the example of varying CdCl$_2$ treatment temperature between 400 and 460 °C. No sodium is added to the samples discussed in this section.

The impact of CdCl$_2$ treatment temperature on CdTe grain size is evaluated by the use of top-view SEM images (not shown). Increase of temperature from 400 to 420 and 440 °C leads to an increase of average grain size from 3.2±0.1 to 3.7±0.2 and 4.5±0.4 µm, respectively. The error gives the standard deviation of the average grain size per image after evaluation of three SEM images per temperature.

XRD measurements were performed to investigate the impact of CdCl$_2$ annealing temperature on CdS-CdTe interdiffusion (Figure 3.4a). Devices which were CdCl$_2$ treated at the temperature optimized for high performance (420 °C) only exhibit a very small shoulder at the large angle side of the XRD peak corresponding to 511 CdTe. Increase in CdCl$_2$ treatment temperature to 460 °C leads to a clearly enhanced CdS-CdTe intermixing. This is confirmed by EQE measurements (Figure 3.4b). Reduction of CdS thickness due to diffusion of sulfur into the CdTe layer is visible in the increased EQE in the short wavelength region (Arrow 1). The formation of a Te rich CdS$_x$Te$_{1-x}$ phase is visible in the shift in cut-off wavelength (Arrow 2), corresponding to a change in ab-
sorber band gap due to diffusion of sulfur into CdTe. The change in band gap indicates that sulfur concentration in these samples is not limited by the solubility of sulfur in CdTe but by kinetic reasons. Also the formation of a small amount of sulfur rich CdTe is indicated by the slightly reduced EQE in the wavelength region between 520 and 550 nm for an increase in CdCl$_2$ treatment temperature from 400 to 420 °C (indicated by 3).

Figure 3.4: XRD (a) and EQE (b) measurements of solar cells, which were CdCl$_2$ treated at different temperatures. XRD data is normalized to the same area under the XRD pattern.

3.7 ZnO:Al as diffusion barrier on soda-lime glass

ZnO:Al has been found to be a barrier against sodium diffusion in CIGS solar cells grown in superstrate configuration [155]. Here the effectiveness of ZnO:Al/i-ZnO is tested for low temperature grown CdTe solar cells. The performance of ZnO:Al as diffusion barrier against sodium diffusion from SLG was examined by the growth of CdTe solar cells on ZnO:Al layers with thicknesses of 1.5 µm and 250 nm while keeping an i-ZnO thickness of 100 nm in both cases. In this case, no NaF layer is applied.

Sodium distribution in CdTe solar cells was measured by SIMS. A significantly lower sodium content in CdTe was measured for cells grown on the thick ZnO:Al layer (Figure 3.5a). This is caused by the superior diffusion barrier properties of the thicker ZnO:Al due to both the increased thickness as well as the larger grain size compared to
Chapter 3. Effect of sodium on structural and electronic properties

the thin ZnO:Al (Figure 3.6). The grain size is an important parameter as it determines the GB density and GBs are easier and preferred diffusion pathways in polycrystalline materials. The measured potassium signal (not shown here) is similar in the samples with the different ZnO:Al thicknesses, indicating that potassium diffusion from the glass is negligible.

Figure 3.5: a) SIMS measurements of the sodium distribution in CdTe solar cells with two different ZnO:Al thicknesses on SLG. b) EQE measurements of CdTe solar cells with different ZnO:Al thicknesses on SLG.

Figure 3.6: SEM cross-section images of cells processed with 1.5 µm (a) and 250 nm (b) of ZnO:Al thickness on SLG.

Top-view SEM images of the CdTe solar cells on thick and thin ZnO:Al on SLG are shown in Figure 3.7a and b, respectively. The CdTe GB properties depend on the thickness of the ZnO:Al layer causing different sodium contents in the CdTe. Widened
GBs can be observed for cells grown on thin ZnO:Al, while CdTe grains are compact when grown on thick ZnO:Al, furthermore showing that a sufficiently thick ZnO:Al layer is able to suppress sodium diffusion. The average CdTe grain size on thin ZnO:Al is about 20% larger than on thick ZnO:Al due to the different sodium concentrations. This difference is less pronounced than when sodium was added as a layer of NaF prior to CdCl$_2$ on BSG (Figure 3.1) due to the difference in how sodium is provided. Furthermore, the sodium content in these experiments could be lower than in the case when 12 nm of NaF was added.

EQE measurements (Figure 3.5b) show an enhanced response in the blue wavelength region for cells grown on thin ZnO:Al due to enhanced CdS-CdTe intermixing, which is caused by sodium diffusion from the glass substrate. The slightly lower response in the long wavelength region for the cells grown on the thick ZnO:Al results from the lower transmission of the thick ZnO:Al layer. The minimum absorber band gap does not change significantly, similar to the experiments where NaF was deliberately added.

SEM cross-section images (Figure 3.6) revealed distributed CdS islands when cells are grown on thin ZnO:Al. The thick ZnO:Al layer is able to effectively suppress sodium diffusion from SLG and therefore the formation of CdS islands, which has been shown to result from a large sodium content available during CdCl$_2$ treatment (Section 3.2).

![Figure 3.7: SEM top-view images of CdTe solar cells processed with 1.5 µm (a) and 250 nm (b) of ZnO:Al thickness on SLG.](image)

In conclusion, due to sodium diffusion through thin ZnO:Al, similar effects were observed on this sample as if sodium was deliberately added as NaF precursor. On the other hand, cells grown on thick ZnO:Al show comparable properties as when grown on low sodium content glass, proving the effectiveness of ZnO as barrier layer for low
3.8 Cell performance

Solar cell performance strongly deteriorated when the CdCl$_2$ treatment was performed in the presence of sodium. This is because of excessive CdS consumption and increased shunting in the cell and can also be influenced by increased voltage dependent collection. Increased shunting is indicated by lower parallel resistance (Table 3.1), which is attributed to the modified structure and widened GBs in the absorber layer. Only for the thinnest NaF layer applied an increase in $J_{sc}$ could be observed because of higher response in the blue wavelength region, while it considerably decreased for larger amounts of sodium. $V_{oc}$ and especially FF strongly decreased with increasing amount of sodium due to the lower parallel resistance and because of the excessive CdS-CdTe intermixing. An amount of only 0.75 and 1.5 nm of NaF decreased cell performance significantly from 14.0% to 12.4% and 9.4%, respectively (Table 3.1). Assuming that all sodium was incorporated and homogeneously distributed in CdTe, the solar cells treated with 0.75 nm of NaF would have a sodium concentration of $5 \times 10^{18}$ cm$^{-3}$, but the incorporated concentration might be considerably smaller as parts of the NaF can remain at the surface of CdTe. Sodium concentrations of $1 \times 10^{17}$ to $1 \times 10^{18}$ cm$^{-3}$ in CdTe and more than $1 \times 10^{19}$ cm$^{-3}$ in CdS in finished CdTe solar cells have previously been measured by quantitative SIMS [59, 149]. This indicates that, depending on the growth conditions, the amounts of sodium in finished CdTe solar cells might be on the same order as applied in this study. Therefore, special care has to be taken to avoid sodium contamination, which can always occur during cell processing either due to diffusion from the glass substrate or as contamination from other sources like impure CdCl$_2$ [156]. By avoiding sodium contamination, excessive CdS-CdTe intermixing and recrystallization as well as the formation of shunting paths can be prevented and CdS thickness can be reduced without adverse effects on FF and $V_{oc}$.

The results of this chapter show that both the addition of sodium and the use of higher temperatures during the CdCl$_2$ treatment enhance the recrystallization of the CdS/CdTe layer stack. This suggests, that the effect of sodium addition on the device properties might depend on the applied CdCl$_2$ treatment conditions. Table 3.1 shows the PV parameters of a device, where NaF with a layer thickness of 3 nm was applied, but which
was annealed for a shorter time of only 10 minutes instead of 25 minutes. In this case, the applied NaF layer has a reduced effect on cell performance. Similar results are obtained when the CdCl$_2$ annealing temperature is reduced. These results show, that the detrimental effects of sodium can partly be overcome by adapting the CdCl$_2$ treatment conditions; however, highest efficiencies were obtained without application of NaF and using CdCl$_2$ treatment conditions optimized for samples without addition of sodium. The results also show, that depending on the sodium content in the solar cell, which is influenced by the substrate, underlying layers as well as processing temperatures, the optimized CdCl$_2$ treatment conditions can be different and therefore have to be adapted when changing one of the previously mentioned parameters.

Sodium contamination from the substrate can be reduced by using low alkaline BSG or by the inclusion of a diffusion barrier layer, but these methods increase production costs. A more economical method for minimizing sodium diffusion from the glass substrate is to reduce the substrate temperatures during CdTe solar cell processing. Low temperatures intrinsically reduce diffusion as the diffusion constant follows an Arrhenius characteristic with exponential dependence on the temperature. Furthermore, as shown in Section 3.7, the use of a sufficiently thick and large grained ZnO:Al layer can effectively suppress sodium diffusion from the glass substrate. The use of low deposition temperatures as well as the barrier function of ZnO:Al enabled the growth of CdTe solar cells on low cost SLG without additional barrier with efficiencies up to 13.5% [without AR coating, Table 3.1] in spite of a large sodium content in the glass substrate. The high $V_{oc}$ of 853 mV obtained on SLG is another indication that sodium can increase acceptor concentration in CdTe.

### 3.9 Mechanism

A mechanism is proposed to explain the pronounced impact of sodium on the CdS-CdTe intermixing. Sodium is known to enhance oxygenation of CIGS [157] and other materials [158]. In CdTe the addition of sodium during the CdCl$_2$ treatment, which is performed in an oxygen containing ambient (here: air) could therefore also enhance oxygenation of the CdTe layer. This is confirmed by SIMS measurements of finished solar cells, revealing average O$_2$ counts within the CdTe layer of 2.5, 8 and 23 for samples processed without, with 1.5 nm and with 12 nm of NaF, respectively. The
results shown in Figure 5.4 suggest that oxygen acts as exchange partner for sulfur to diffuse into the CdTe layer. Furthermore, oxygen has been reported to reduce the eutectic temperature of the system CdTe-CdCl$_2$ [159], which may lead to liquid phase recrystallization. It is therefore proposed that sodium added during the CdCl$_2$ treatment promotes oxygenation, which in turn enhances recrystallization and facilitates diffusion of sulfur into the CdTe layer.

### 3.10 Conclusions and outlook

The effect of sodium on CdTe solar cells has been investigated. Sodium present during the CdCl$_2$ treatment was found to lead to increased grain size of the absorber but also to a widening of GBs, which results in electrical shunting of solar cells. CdS-CdTe intermixing and CdS island formation is significantly enhanced in the presence of sodium. Addition of sodium leads to a reduced SCR width and an increased apparent acceptor concentration in CdTe. In spite of the doping effects by the addition of sodium, cell performance deteriorated due to excessive CdS-CdTe intermixing and shunting. A mechanism for the sodium enhanced CdS-CdTe interdiffusion is proposed, which is based on sodium enhanced oxygenation, which in turn facilitates sulfur diffusion into the CdTe layer. A sufficiently thick and large grained ZnO:Al TCO was found to effectively suppress sodium diffusion from SLG. This enables the growth of CdTe solar cells with efficiencies up to 13.5% (without AR coating) on low cost SLG without additional diffusion barrier by using a low temperature process, which minimizes sodium diffusion. These results show that high-efficiency CdTe solar cells on SLG can be developed at low temperatures ($\leq 450$ °C), that impurities like sodium play an important role and that ZnO can be used as effective diffusion barrier.

While the present results show that sodium addition in solar cells with optimized CdS-CdTe intermixing is detrimental, it could be beneficial in solar cells with insufficient CdS-CdTe intermixing. In Chapter 8 insufficient CdS-CdTe intermixing is proposed as the reason for the thick CdS layer required in substrate configuration. Therefore application of sodium in substrate configuration can be considered as an approach to reduce CdS layer thickness (cf. Section 4.8).
Chapter 4

p-n junction formation in substrate configuration

This chapter is in part based on the following publication:

Parts of the results of this chapter were obtained during the Master thesis of Rafael Schmitt [160].

4.1 Introduction

An important processing step for the growth of CdTe solar cells is the p-n junction formation between the CdTe absorber layer and the CdS window layer. In superstrate configuration, the p-n junction is formed during the CdCl$_2$ treatment of the CdS/CdTe layer stack, which also leads to the recrystallization of the CdTe and CdS layers [76]. While this process is well established, the best p-n junction formation process for substrate configuration CdTe solar cells is under debate [80,91]. Various approaches were used for substrate configuration, e.g. a CdCl$_2$ treatment only after CdTe [82, 84, 91], a CdCl$_2$ treatment of the CdTe/CdS layer stack [20], or a CdCl$_2$ treatment after both CdTe and CdS [84, 88, 91]. Recently, experiments on solar cells with efficiency around
10% have led to the conclusion that a CdCl$_2$ treatment of the CdS (in the following called CdS treatment) degrades solar cell performance [80]. However, in this chapter it is shown that the CdS treatment is needed to obtain efficiencies above 13% and the impact of this annealing treatment on the phase and microstructure of the CdS layer is investigated. It is furthermore shown that addition of a second CdS layer after the CdS treatment further improves $V_{oc}$ and FF. Different ways to reduce parasitic absorption in these CdS layers without deterioration of p-n junction properties are discussed. While this chapter focuses on the effect of the CdS treatment on the structural properties of the CdS layer, Chapter 5 focuses on its effects on impurity distribution and MCLT in the CdTe layer.

### 4.2 CdCl$_2$ treatment of the CdS layer

Figure 4.1 shows top-view SEM micrographs of CdS layers which were deposited on the CdCl$_2$ treated and copper doped CdTe layer of solar cells in substrate configuration and annealed under different conditions. Table 4.1 shows the PV parameters of the corresponding finished devices. As-deposited CdS grown by CBD covers the CdTe layer with nanocrystalline sized grains (Figure 4.1a). Upon CdS treatment at 400 °C in an ambient containing 50% of O$_2$, the microstructure of the CdS layer significantly changes (Figure 4.1b): Grain size increases and pinholes are formed in the CdS layer. In spite of the pinhole formation in the CdS layer, the efficiency of the solar cells increases due to improvements in all PV parameters, especially $V_{oc}$ and FF. The corresponding $J$-$V$ and EQE measurements are shown in Figure 4.2. EQE in the long wavelength region is improved and voltage dependent carrier collection is reduced upon CdS treatment.

### 4.3 Double CdS layer

Even though the CdS treatment increases efficiency, the pinholes in the CdS layer which occur upon annealing treatment can be detrimental to device performance due to the direct contact between CdTe and ZnO. In order to cover the pinholes and to enable a covering CdS layer, a second CdS layer is grown after the annealing treatment. Complete coverage upon addition of a second CdS layer is confirmed by SEM (Figure 4.1c).
4.4 Impact of oxygen

Figure 4.1: Top-view SEM images of CdS layers prepared under different conditions on CdTe. Preparation conditions are shown in Table 4.1. All images except for (c) show the morphology of the first CdS layer without addition of a 2nd CdS while (c) shows the morphology after deposition of a second CdS layer.

Even though deposition of a second CdS layer leads to increased parasitic absorption and therefore a reduced $J_{sc}$, with the application of the second CdS layer $V_{oc}$ and FF are further increased (Table 4.1 & Figure 4.2). $V_{oc}$ well above 800 mV and FF above 70% are obtained, leading to an increased efficiency of 12.2%.

4.4 Impact of oxygen

The oxygen content during the CdS treatment was varied and its influence on the CdS morphology and the device performance was investigated. The oxygen content has
Chapter 4. p-n junction formation in substrate configuration

<table>
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<th>Process</th>
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<th>2\textsuperscript{nd} CdS</th>
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<th>$J_{sc}$ (mA·cm(^{-2}))</th>
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<td>59.8</td>
</tr>
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Table 4.1: PV parameters of CdTe solar cells processed with different CdS annealing conditions.

Figure 4.2: $J$-$V$ (a) and EQE (b) measurements of CdTe solar cells prepared with different p-n junction formation processes. Processing parameters of process a,b and c as well as the corresponding PV parameters are given in Table 4.1

A strong influence on the CdS morphology and enhanced grain growth and pinhole formation is indicated upon changing the oxygen content from 50\% to 30\% or 80\% (Figure 4.1d,e). The efficiency is reduced to below 10\% due to a reduction of $V_{oc}$ and FF. Solar cells processed without oxygen addition during the CdS treatment have further reduced performance (7.5\% efficiency). This shows, that oxygen content during the annealing treatment has to be well controlled in order to achieve a good morphology of the CdS with minimal pinhole density and to obtain high efficiencies.
4.5 Impact of CdCl$_2$

Grain growth is a typical influence of the CdCl$_2$ treatment and can lead to pinhole formation. In an attempt to avoid pinhole formation, a sample was identically processed as the device with 12.2% efficiency but without addition of CdCl$_2$ during the annealing of the CdS. SEM images confirm that this significantly reduces pinhole formation in the CdS layer (Figure 4.1f). In spite of the improved coverage, a low $V_{oc}$ of ~700 mV and a low FF of ~60% are obtained, yielding an efficiency of only 8.7%.

It is possible that the annealing conditions during the CdS treatment (temperature, oxygen content) need to be adapted for an annealing step without CdCl$_2$. Therefore, several samples with varying annealing conditions of the CdS without addition of CdCl$_2$ were produced. The highest obtained efficiency for a solar cell where the CdS was annealed without addition of CdCl$_2$ is 11.1% (799 mV, 61.2% FF, 22.8 mA·cm$^{-2}$). This is obtained by reducing oxygen content to 10% while the temperature is kept at 400 °C. The lower oxygen content is expected to reduce oxygenation of the CdS, while a reduced oxygen content is not needed when CdCl$_2$ is used, which protects the CdS layer from oxygenation [161]. The efficiencies of cells processed without addition of CdCl$_2$ during the annealing treatment of the CdS always remained significantly lower than what is achieved with addition of CdCl$_2$, especially due to a low FF<65% in samples without addition of CdCl$_2$. Therefore, it is concluded, that addition of CdCl$_2$ during the annealing treatment of the CdS is important for good device performance, especially to obtain high FF. Even when no CdCl$_2$ is added to the aforementioned samples, a small amount of CdCl$_2$ due to residuals in the annealing oven cannot be excluded. A sample similarly processed as the aforementioned sample with 11.1% efficiency shows significantly lower efficiencies (~4%) when the CdS annealing treatment is performed after removing all residual CdCl$_2$ from the annealing oven. This further emphasizes the importance of the presence of CdCl$_2$ during the annealing treatment of the CdS and the positive impact of CdCl$_2$ addition on MCLT will be shown in Chapter 5.

To investigate the influence of the presence of CdCl$_2$ on the crystallographic phase of CdS, in-situ XRD measurements of a solar cell processed up to the CdS with and without using CdCl$_2$ were performed (Figure 4.3). In the presence of CdCl$_2$ the phase of the CdS layer changes from cubic to hexagonal while the phase change does not occur when no CdCl$_2$ is present even when higher than usual annealing temperatures are used. The results could suggest that recrystallization of the CdS layer to hexagonal
phase is important to obtain high-efficiency solar cells. This is further discussed below. In-situ XRD shows that above 400 °C various oxides are formed. The shift of the CdS 111 phase towards smaller angles upon annealing is attributed to oxygen loss from the hydro-oxygenated CBD grown CdS. The reduction of oxygen content in the CdS layer upon CdS treatment is confirmed with SIMS and XPS measurements (Chapter 5).

The in-situ XRD results furthermore show, that the phase change of the CdS, which accompanies the improved device performance already occurs at around 330 °C, which is significantly lower than typical CdCl$_2$ treatment temperatures of 400-420 °C commonly applied for CdTe solar cells in superstrate configuration.

![In-situ XRD patterns during the CdCl$_2$ treatment of CdS (a) and while annealing without the presence of CdCl$_2$ (b). CdS was deposited on a Glass/Mo/MoO$_x$/CdTe layer stack.](image)

**Figure 4.3:** In-situ XRD patterns during the CdCl$_2$ treatment of CdS (a) and while annealing without the presence of CdCl$_2$ (b). CdS was deposited on a Glass/Mo/MoO$_x$/CdTe layer stack.

### 4.6 CdS recrystallization with reduced pinhole formation

Solar cells were produced, where the CdS layer was CdCl$_2$ treated at 360 °C, a temperature at which the in-situ XRD measurement suggests phase change of the CdS
layer from cubic to hexagonal. Ex-situ XRD measurements confirm the expected CdS phase change (Figure 4.4). Furthermore, Figure 4.5a shows that the relatively low temperature of 360 °C enables an improved coverage of the CdTe layer with hexagonal CdS compared to the application of an annealing treatment at 400 °C. Top-view SEM images do not reveal a significant change in morphology of the CdS layer upon CdCl\textsubscript{2} treatment of the CdS at 360 °C compared to the as-deposited CdS layer (Figure 4.1a). However, STEM reveals grain growth of the CdS layer upon CdCl\textsubscript{2} treatment at 360 °C (Figure 4.5b). The STEM image shows the double CdS layer between the CdTe absorber and the ZnO FC. The CdCl\textsubscript{2} treated CdS layer exhibits grain size up to several 100 nm while the additional CdS layer exhibits nanocrystallites as commonly observed for CBD grown CdS.

**Figure 4.4:** GI\textit{X}RD pattern of an as-deposited CdS layer grown on Glass/Mo/MoO\textsubscript{x}/CdTe layer stack and after an annealing treatment at 360 °C in the presence of CdCl\textsubscript{2} and 50% O\textsubscript{2}.

Figure 4.6 shows the \textit{J-V} and EQE characteristics of a solar cell where the CdS treatment is performed at 360 °C. The improved coverage enables high \( V_\text{oc} = 841 \text{ mV} \) and FF=76.2%. An efficiency of 13.2% is obtained with \( V_\text{oc} \) and FF as high as the internal record efficiency cell in superstrate configuration (Chapter 8). It is also notable, that the rollover, which is generally very pronounced for CdTe solar cells in substrate configuration, is not observed for the cell with CdS bi-layer, even though some other nominally identically processed samples showed a small rollover.

Even though the modified annealing treatment partly solves the structural problems of pinhole formation in the CdS, the second CdS layer is still required for highest \( V_\text{oc} \).
Figure 4.5: a) Top-view SEM image of a CdS layer deposited on the CdTe layer and annealed in the presence of CdCl$_2$ at 360 °C in an ambient containing 50% O$_2$. The image shows the first CdS layer without application of a second CdS layer. b) Bright field STEM image of the double layer CdS in a CdTe solar cell. The first CdS layer (CdS-1) is CdCl$_2$ treated at 360 °C and the second CdS (CdS-2) is as-deposited CBD grown CdS.

J-V and FF. Figure 4.6 shows $J$-$V$ and EQE measurements of a cell without second CdS. Remarkable $V_{oc}$ and FF are reached; however, the values are still lower compared to cells with CdS bi-layer. This indicates that the CdS treatment still leads to the formation of small pinholes, which are not clearly visible with SEM.

4.7 Discussion

The presence of CdCl$_2$ during the annealing treatment of the CdS was found to be crucial for highest performance and in-situ XRD reveals that the presence of CdCl$_2$ is needed to obtain a phase change of the CdS layer upon annealing. Furthermore, all high-efficiency devices which were investigated by XRD had hexagonal CdS. This could hint towards the important role of the hexagonal phase of CdS. However, XRD measurements of a high-efficiency superstrate cell measured from the back contact indicated that this device contains cubic CdS. These results indicate that another ef-
4.8 Towards thinner CdS layer

The results of high $V_{oc}$ and FF of the solar cell with CdS bi-layer and the high $J_{sc}$ of the cell with single CdS layer (Figure 4.6) suggest that efficiencies well above 14% should be achievable. However, the increase in $J_{sc}$ by omitting the second CdS layer was accompanied by a decrease in $V_{oc}$ and FF so far and the highest efficiency reached without addition of a second CdS layer is 13.3%. This emphasizes the importance to understand the reason for the currently needed thick CdS layer and to develop processes which enable the reduction of CdS thickness without loss in $V_{oc}$ and FF. Different approaches to accomplish this are discussed in the following.

**Figure 4.6:** $J-V$ (a) and EQE (b) measurements of solar cells processed with a CdS treatment at 360 $^\circ$C with single and double CdS layer. The inset shows the PV parameters of the corresponding devices.

Fect accompanies the phase change of CdS. In Chapter 5 the beneficial effect of the CdS treatment on the MCLT in the CdTe layer upon modification of CdTe GBs and the CdTe/CdS interface with sulfur and chlorine impurities is shown.
4.8.1 Sulfurization of the CdTe layer

In Chapter 5, the positive effect of the CdS treatment on MCLT in the CdTe layer is shown. These results motivate to develop processes, which enable a similar increase of MCLT without the drawback of parasitic absorption in the CdS layer. One of the tested approaches to achieve this is the sulfurization of the surface of the CdTe layer after copper doping in a two zone tube furnace using elemental sulfur. Sulfur is transported by N\textsubscript{2} carrier gas from one temperature zone to the sample in a second temperature zone. Best obtained efficiency is 9.6% (674 mV, 64% FF, 22.2 mA·cm\textsuperscript{-2}) by using T\textsubscript{Sulfur}=230 °C and T\textsubscript{Substrate}=320 °C, followed by a CdCl\textsubscript{2} treatment and deposition of one CdS layer. A constant EQE at high value (~90%) in the wavelength region between 550 and 800 nm is observed for this sample, indicating an improved MCLT compared to samples without sulfur diffusion into the CdTe layer (no CdCl\textsubscript{2} treatment after deposition of the CdS layer). This result is a confirmation of the importance of sulfur in passivating defects at GBs and surface of the CdTe layer (see Chapter 5). In spite of these positive signs, the efficiency remained below the efficiency of devices processed with the baseline process, possibly owing to contamination from the sulfurization furnace, which is usually used for processing CZTS absorbers. Possibly, the use of other chemicals, like H\textsubscript{2}S might enable improved results.

4.8.2 Reduction of thicknesses of each CdS layer

An obvious way to reduce parasitic absorption in the CdS layers is to deposit either of the CdS layers with reduced layer thickness. The PV parameters of devices with different CdS layer thicknesses are shown in Table 4.2. As expected, reduction of CdS layer thickness leads to an increase in $J_{sc}$ and an improved response in the short wavelength region is confirmed by EQE (not shown). However, to obtain highest $V_{oc}$ and FF relatively thick CdS layers are required. The data furthermore suggests, that reduction of the second CdS layer thickness is more promising than reduction of the first CdS layer thickness. This is consistent with the aforementioned results: Omitting the first CdS layer together with its annealing treatment leads to a significant reduction of performance to about 7% while relatively high efficiencies were also achieved without addition of the second CdS layer.
4.8. Towards thinner CdS layer

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<th>2nd CdS layer</th>
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Table 4.2: PV parameters of solar cells processed with different CdS layer thicknesses. The deposition time during growth of CdS using CBD is given as a measure for CdS thickness. 20 minutes deposition corresponds to a CdS thickness of approximately 70 nm.

4.8.3 Suggested future experiments

Additional to the aforementioned approaches, the following concepts are suggested in order to reduce CdS layer thickness:

The XPS measurements shown in Chapter 5 indicate that a cadmium, oxygen and chlorine containing layer is formed at the surface of the CdS layer upon CdS treatment and it is discussed that one role of the deposition of the second CdS layer is to remove this layer from the surface. Therefore, replacement of the deposition of the second CdS layer with a partial electrolyte treatment, e.g. in thiourea solution, is suggested. Even though initial experiments were not yet successful in the here presented solar cells, further investigations in this direction are recommended.

In Chapter 8, the absence of an intermixed CdS$_x$Te$_{1-x}$ layer is discussed as a possible reason for the thicker CdS layer necessary in substrate configuration. This motivates to develop processes, which enable an intermixed CdS$_x$Te$_{1-x}$ layer at the CdTe surface and the aforementioned sulfurization of the surface of the CdTe layer could be a route to accomplish this. Another concept could be to treat the CdTe and CdS layers together to obtain an intermixed layer; however, this did not yet lead to very high efficiencies. An alternative way could be the use of co-evaporated CdS$_x$Te$_{1-x}$ close to the CdTe surface or an additional CdTe/CdS stack at the junction, on which a CdCl$_2$ treatment
is performed. Considering the suggested role of oxygen to act as exchange partner for sulfur (cf. Chapter 5), enhanced oxygenation of the surface of the CdTe layer, e.g. by application of NaCl during the copper diffusion treatment or CdTe treatment should be considered (cf. Chapter 3). Furthermore, other ways to obtain an inverted n-type surface of the CdTe layer, e.g. by indium or aluminium doping of the surface of the CdTe layer can be considered.

Another reason for the required large CdS thickness could be an insufficient n-type doping density in the CdS layer. SIMS measurements reveal a higher copper concentration in the CdS layer of substrate configuration solar cells than of superstrate configuration (cf. Chapter 6). Copper can form acceptors in CdS [33], which could lead to inferior n-type doping in the CdS layer. Enhanced n-type doping density of the CdS layer could therefore lead to improved results.

4.9 Conclusions and outlook

In conclusion, the influence of different processing conditions during an annealing treatment after deposition of the CdS layer on its microstructure and phase and on the device properties is investigated. The presence of CdCl$_2$ during the annealing treatment of the CdS is important for a phase change of the CdS layer to hexagonal phase and for high-efficiency solar cells. The beneficial effect of this treatment on the MCLT in the CdTe layer will be shown in Chapter 5. Performing the CdS treatment at 360 $^\circ$C leads to a phase change of the CdS with reduced effects on the CdS coverage. The addition of a second CdS layer after the annealing treatment of the first CdS layer improves $V_{oc}$ and FF but increases parasitic absorption. Reduction of CdS layer thickness without loss in $V_{oc}$ or FF could enable solar cells with efficiency well beyond 14% and various concepts to improve the $J_{sc}$ by reduction of CdS layer thickness without deterioration of p-n junction properties are discussed.
Chapter 5

Tailoring impurity distribution for enhanced minority carrier lifetime

This chapter is in part based on the following publication:


Parts of the results of this chapter were obtained during the Master thesis of Rafael Schmitt [160].

5.1 Introduction

Passivation of GBs and interfaces in order to suppress recombination and to improve MCLT is essential for the functionality of devices based on polycrystalline materials. Improvement of MCLT is believed to be a very promising way to bring CdTe solar cells to the next efficiency level. Recently, the persistent challenge of limited $V_{oc}$ was overcome and solar cells with $V_{oc}$ up to 903 mV were achieved, even though with limited $J_{sc}$ and FF [7]. The improved $V_{oc}$ was achieved by enhancing MCLT, suggesting this approach to be most promising for pushing the $V_{oc}$ towards 1 V. This emphasizes the importance to identify the parameters, which significantly influence MCLT.

Based on experiments on CdTe solar cells in the conventional superstrate configu-
ration [6], it was found, that the addition of oxygen during the growth of the CdTe layer increases MCLT [73]. The controlled addition of copper can increase MCLT, whereas excessive amounts of copper decrease MCLT ([78, 162] & Chapter 6). The CdCl₂ treatment, which is commonly performed on the CdS/CdTe layer stack improves MCLT [66, 67] and leads to increase of grain size, incorporation of chlorine and inter-diffusion of the CdS and CdTe layers [53]. Several simultaneously occurring effects prevent separation of their impact on MCLT for CdTe solar cells grown in superstrate configuration. Experiments on layer stacks indicated that the CdCl₂ treatment of the CdTe without the presence of sulfur increases MCLT and sulfur diffusion additionally increases MCLT [66]. However, no solar cells could be processed with these layer stacks.

This drawback can be overcome by growing CdTe solar cells in substrate configuration, which offers advanced opportunities to improve and investigate the CdTe/CdS junction properties. Chapter 4 presents the developed p-n junction formation process for substrate configuration solar cells and the effects of the CdS treatment on the structural properties of the CdS layer. In this chapter, the effects of the p-n junction formation on the MCLT in the CdTe layer are presented and it is shown that the CdS treatment is essential for good device performance because it significantly enhances MCLT. The CdS treatment leads to sulfur diffusion along CdTe GBs and a modification of the electronic properties of the CdTe/CdS interface upon chlorine segregation at this interface.

5.2 Electronic properties

Figures 5.1a and b show the influence of the CdS treatment and other processing steps on the $J-V$ and EQE characteristics of the solar cells. The corresponding PV parameters are listed in Table 5.1. As shown in Chapter 4, the solar cell performance significantly increases due to the CdS treatment. The solar cell conversion efficiency increases from ~7% to >13% and all PV parameters are improved. Voltage dependent carrier collection is reduced and EQE is improved, especially in the long wavelength region, which can be due to an improved MCLT. The beneficial effect of the CdS treatment on PV performance, voltage dependent carrier collection and EQE in the long wavelength region was proven in several experiments.

TRPL measurements were performed to investigate the influence of the CdS treatment
5.2. Electronic properties

Figure 5.1: Influence of different processing conditions on $J$-$V$ (a), EQE (b), TRPL (c) and normalized PL (d) characteristics. Description of the processes A-D and the corresponding PV parameters and MCLT are listed in Table 5.1.

on the MCLT (Figure 5.1c & Table 5.1). MCLT increases at least by an order of magnitude from <0.2 ns (detection limit of the TRPL system) to 2.39 ns upon CdS treatment. The pronounced positive effect of the CdS treatment on the MCLT was reproducibly observed several times. Metzger et al. found an improvement in $V_{oc}$ by about 140 mV for an improvement in MCLT by an order of magnitude [73]. In the present measurements improvement in $V_{oc}$ by 177 mV is observed, indicating that the improved performance mainly arises from the longer MCLT. Figure 5.1d shows the PL spectra of the corresponding cells. The maximum of the PL spectrum does not change upon CdS treatment; however, the width of the PL signal increases slightly, which might correspond to a small change of absorber band gap close to the CdTe/CdS junction.
Table 5.1: Influence of different processing conditions on PV parameters and MCLT as determined by J-V and TRPL measurements, respectively. PV parameters of the best cell and average PV parameters (with standard deviation) of the five best cells of a sample are given.

<table>
<thead>
<tr>
<th>Process</th>
<th>CdTe treat.</th>
<th>Copper doping</th>
<th>CdS treat.</th>
<th>$\eta$ (%)</th>
<th>$V_{oc}$ (mV)</th>
<th>$J_{sc}$ (mA·cm$^{-2}$) (%)</th>
<th>FF (%)</th>
<th>MCLT (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>13.6</td>
<td>850</td>
<td>21.4</td>
<td>74.6</td>
<td>2.39</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(13.4±0.2)</td>
<td>(850±2)</td>
<td>(21.4±0.1)</td>
<td>(73.8±1.1)</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>6.8</td>
<td>673</td>
<td>18.1</td>
<td>55.7</td>
<td>&lt;0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(6.6±0.2)</td>
<td>(665±7)</td>
<td>(18.2±0.4)</td>
<td>(54.6±1.9)</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>yes</td>
<td>no</td>
<td>yes</td>
<td>0.6</td>
<td>323</td>
<td>3.5</td>
<td>53.4</td>
<td>1.78</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(0.4±0.2)</td>
<td>(315±32)</td>
<td>(2.2±0.8)</td>
<td>(53.4±4.0)</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>no</td>
<td>yes</td>
<td>yes</td>
<td>10.1</td>
<td>728</td>
<td>20.5</td>
<td>67.5</td>
<td>1.79</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(9.9±0.1)</td>
<td>(726±5)</td>
<td>(20.3±0.2)</td>
<td>(67.4±0.7)</td>
<td></td>
</tr>
</tbody>
</table>

The impact of the CdS treatment on the MCLT and device performance is compared with the effects of other processing steps, which are expected to influence MCLT based on the knowledge gained from experiments on solar cells in superstrate configuration, namely the copper doping and the CdCl$_2$ treatment of the CdTe (called CdTe treatment). As shown in Chapter 6, substrate configuration CdTe solar cells processed without copper doping have significantly reduced PV parameters and also reduced MCLT (Figure 5.1); however, the reduction in MCLT is not sufficient to explain the reduced PV performance. Low performance arises from the absence of p-type doping of the CdTe layer, resulting in negligible electric field close to the CdTe/CdS junction (see Chapter 6). Omitting the CdTe treatment reduces the $V_{oc}$, resulting in about 10% efficiency and leads to a small reduction in MCLT. Interestingly, the CdS treatment is more important for good device performance and for long MCLT in the CdTe layer than the CdTe treatment (Table 5.1). The beneficial effect of the CdS treatment in the presented process was established by several experiments and the samples processed without CdS treatment had a lower efficiency than the sample without CdTe treatment. PL measurements on the sample without CdTe treatment (Figure 5.1d) show a clear shift of band gap towards longer wavelength because the CdS treatment is performed on the non-recrystallized CdTe, which leads to amplified sulfur diffusion into the CdTe layer,
resulting in a CdS\textsubscript{x}Te\textsubscript{1−x} alloy close to the junction [91]. In superstrate configuration, formation of a CdS\textsubscript{x}Te\textsubscript{1−x} alloy is often associated with good device performance. In substrate configuration, process A, which enabled best solar cell performance does not lead to a clear shift in PL peak, indicating that high $V_{oc}$ and FF can also be achieved with negligible formation of a Te rich CdS\textsubscript{x}Te\textsubscript{1−x} alloy. This is further supported by GIXRD measurements (Figure 5.2). No formation of a Te rich CdS\textsubscript{x}Te\textsubscript{1−x} alloy is detected upon CdS treatment, which is expected to appear as a shoulder or an additional peak at the large angle side of the CdTe peak (compare e.g. Chapter 3). The present TRPL study clearly shows that the CdS treatment is the most important processing step for enhancing MCLT. Often, the product of the mobility and the lifetime is used as a measure to characterize the quality of electronic materials [163]. In the present case, the minority carrier mobility is assumed to be independent of the applied chemical treatments, making the MCLT a good measure for the electronic quality (cf. Metzger et al. [73]).

As shown in Chapter 4, addition of CdCl\textsubscript{2} and oxygen during the CdS treatment is important for good device performance. In the following, the impact of addition of these impurities on MCLT is shown. Omitting CdCl\textsubscript{2} during the CdS treatment significantly reduces MCLT in the CdTe layer, resulting in a MCLT of 0.59 ns. Omitting oxygen has a weaker effect, leading to a MCLT of 1.38 ns. This shows that the presence of CdCl\textsubscript{2} during the CdS treatment is essential to significantly improve MCLT in the CdTe layer, and the necessity of CdCl\textsubscript{2} addition was proven by several experiments.

TRPL of CdTe solar cells is generally measured in the presence of a p-n junction, which

**Figure 5.2:** GIXRD measurements of CdTe solar cells processed up to the first CdS layer – either with or without performing a CdS treatment. The GIXRD measurement around the peak corresponding to 422 CdTe is shown.
can significantly complicate the analysis of the data as the drift field of the p-n junction can contribute to the separation of the carriers. However, it was shown by simulations and experiments that TRPL measurements at sufficiently high injection levels allow deducing the recombination properties in spite of complications introduced by the p-n junction [73, 143]. Even though this is currently under discussion [83, 164] the following experiment shows, that under the conditions chosen in the presented measurements, the presence of the p-n junction does not have a major influence on the measurements. Copper doping has a small influence on MCLT, whereas the electric field close to the CdTe/CdS interface dramatically changes as shown in Chapter 6 by EBIC measurements. Furthermore, an enhanced electric field induced by the p-n junction is expected to decrease measured MCLT [143], whereas the measurements show a small increase in MCLT upon controlled copper doping.

Generally, the improved MCLT can arise from reduced recombination in the CdTe grains and at GBs or at the CdTe/CdS interface. In the following, the influence of the CdS treatment on the impurity distribution in the CdTe layer is shown, followed by the influence on the CdTe/CdS interface. On all samples discussed in the remainder of this chapter, a CdTe treatment and copper doping was performed.

### 5.3 Impurity distribution

#### 5.3.1 Secondary ion mass spectroscopy

Potential changes in the CdTe bulk and GBs due to the CdS treatment are limited because CdTe recrystallizes in the previous CdTe treatment in the presence of chlorine and oxygen at higher temperatures. The only additionally introduced element is sulfur. As shown above, the presence of CdCl$_2$ is essential for long MCLT and as shown in Chapter 4 CdCl$_2$ acts as recrystallization flux of the CdS layer, enhancing diffusion of sulfur into the CdTe layer.

With the goal to investigate if sulfur diffuses into CdTe upon the CdS treatment, SIMS measurements on cells processed up to the first CdS layer both with and without CdS treatment were performed (Figure 5.3). However, SIMS depth profiles recorded during sputtering through the CdS layer into the CdTe layer (Figure 5.3c) can be distorted from forward-sputtering of sulfur atoms into CdTe. Still, it allows the deduction of changes in
the impurity distribution within the CdS layer. Chlorine and tellurium content in the CdS layer increase, whereas oxygen content decreases. Chlorine and oxygen preferentially segregate at the CdTe/CdS interface and surface of CdS after the CdS treatment. Assuming that chlorine mainly interacts with the cadmium atom, segregation of chlorine on the surface of the CdTe layer would also be expected upon CdTe treatment. The absence of chlorine segregation at the surface of CdTe in the sample without CdS treatment (Figure 5.3a) can be explained considering the influences of the CBD of the CdS layer, which can remove excess chlorine from the surface of CdTe. Changes in the CdS bulk, e.g. chlorine doping can have a minor additional effect on the device performance; however, these changes do not influence the MCLT in the CdTe layer.

**Figure 5.3:** a,b) SIMS depth profiles of solar cells processed up to the first CdS layer recorded during sputtering from the FC towards the BC. The samples are processed without CdS treatment (dashed: a) and with CdS treatment (solid: b). c) shows a schematic of the measurement mode and the green arrows indicate the direction of sputtering.

To enable investigation of the sulfur distribution in the CdTe layer, SIMS measurements were performed after mechanical lift-off and sputtering from the BC towards the FC (Figure 5.4). A clear increase in sulfur signal in the CdTe layer is observed due to the CdS treatment, with the signal rising towards the CdS layer. Oxygen signal follows the opposite trend: it rises towards the FC before the CdS treatment, whereas it is constant after the CdS treatment. This indicates an elemental exchange between oxygen and sulfur within the CdTe layer.

In order to investigate if sulfur diffuses along GBs or penetrates into the CdTe grains, the method of TOF-SIMS chemical imaging [135] is introduced to CdTe solar cell research as a tool to investigate impurity segregation near the GBs. SIMS chemical images of
Chapter 5. Tailoring impurity distribution for enhanced minority carrier lifetime

**Figure 5.4:** a,b) SIMS depth profiles of finished solar cells recorded during sputtering from the BC to the FC after mechanical lift-off. The samples are processed without CdS treatment (dashed: a) and with CdS treatment (solid: b). c,d) Sulfur (c) and oxygen (d) signal of samples without (dashed) and with (solid) CdS treatment are shown in a linear scale. e) Mass spectrum around the mass of $^{32}\text{S}$ and $^{16}\text{O}_2$ within the CdTe layer (sputter time 200-1800 s) of measurement (b). f) shows a schematic of the measurement mode and the blue arrows indicate the direction of sputtering.

A solar cell processed with CdS treatment are obtained with a lateral resolution of approximately 400 nm. Sputtering from the BC to the FC after mechanical lift-off enables the 3D investigation of the impurity distribution (Figure 5.5). Segregation of chlorine at
the GBs of the CdTe layer is observed - consistent with previous measurements e.g. by energy-filtered transmission electron microscopy [65]. Even though chlorine preferentially segregates at GBs, it is also present within the grains as seen from the mass spectrum extracted from within a single CdTe grain (Figure 5.5). This is confirmed for several CdTe grains. The upcoming sulfur signal close to the FC clearly correlates with the position of high chlorine signal, indicating that sulfur preferentially diffuses along the GBs into the CdTe layer. The SIMS chemical imaging measurement furthermore confirms the data of Figure 5.4b (after averaging over the lateral distribution).

Even though SIMS chemical imaging shows a clear segregation of chlorine and sulfur close to the GB region, the apparent width of the impurity distribution around GBs is governed by the lateral resolution of the characterization method, excluding quantitative extraction of the impurity distribution around the GBs. Therefore APT was applied to further resolve the local distribution of impurities.

5.3.2 Atom probe tomography

APT has already been used to study local atomic distributions in CIGS [165] and CZTS [166] solar cells and one report describes the impurity distribution around the GBs of CdTe solar cells in superstrate configuration [167]. Here, APT measurements are performed on the CdTe layer in a substrate configuration solar cell subjected to a CdS treatment. Figure 5.6a shows an APT reconstruction of a GB region and Figure 5.6b shows the corresponding 1D-profile of the impurity distribution across the GB after averaging over the indicated volume. The GB type is not known. Chlorine segregation at the GB is confirmed. An upper limit of the FWHM of the chlorine distribution around the GB of 7 nm is measured. Though ions are subject to local magnification effects during field-evaporation, which can overestimate an interface dimension [168], this width can also suggest a near-GB excess of the impurity atoms. Sulfur segregation at the GB is likewise observed, consistent with SIMS chemical images. Chlorine and sulfur concentrations at the GB of 1.4 at% and 0.3 at% are measured, respectively. Mass spectra within the bulk of the CdTe grains revealed no sulfur or chlorine related peaks above the background, suggesting their maximum concentration to be ~0.05 at%; however, SIMS chemical imaging reveals a non-zero concentration of chlorine within the CdTe grains. A chlorine concentration of approximately $6 \times 10^{17}$ cm$^{-3}$ within the CdTe grains is obtained (cf. Section 2.2.2.1). This is in reasonable agreement with published
Figure 5.5: SIMS chemical images of the lateral chlorine (red) and sulfur (green) distribution in the CdTe layer and its evolution while sputtering through the sample (left). Yellow color arises from color mixing of the red chlorine signal and the green sulfur signal. z-axis gives approximate values. On the right side, a SIMS image in the CdTe close to the FC (top) and BC (bottom) is shown. The blue signal shows the chlorine line profile along the vertical blue straight line. The mass spectrum within a CdTe grain is shown (binning 0.02 amu).

solubility values of chlorine in CdTe around $1 \times 10^{17}$ cm$^{-3}$ [169]. Solubility of sulfur in CdTe is around 5% at typical CdCl$_2$ treatment temperatures [153] and can therefore not explain segregation of sulfur at GBs. In this case, GB segregation arises from the
preferred diffusion along GBs compared to diffusion into CdTe bulk. Using sulfur diffusivity values in CdTe bulk published by Lane et al. [170], a decrease in sulfur content to 50% and to 5% of the GB value is expected within ~3 nm and ~10 nm from the GB, respectively. This is in good agreement with the presented APT measurement, which reveals that sulfur is mostly at the GBs of CdTe without significant diffusion into the bulk. In comparison, growth processes in superstrate configuration commonly lead to sulfur diffusion during a recrystallization treatment of the CdTe bulk, facilitating sulfur diffusion into CdTe grains, which leads to the formation of a CdS$_{x}$Te$_{1-x}$ alloy [53]. A significantly wider sulfur distribution around GBs than in the present study of substrate configuration devices was also observed in a previous APT study of CdTe solar cells in superstrate configuration [167]. On the other hand, the two APT studies reveal a similar chlorine distribution around the GB [167].

The different origins of the segregation of chlorine and sulfur at the GBs might also explain the slightly different shape of the chlorine and sulfur concentration profile around the GB (Figure 5.6b), with sulfur having a slightly larger FWHM of 9 nm. The exact shape of impurity distribution around GBs is important, because GBs can actively participate in carrier separation and collection and appropriate interface engineering is important for the functionality of the devices [47,48,171].

### 5.3.3 X-ray photoelectron spectroscopy

Additionally to impurity diffusion along the GBs of CdTe, modification of the CdTe/CdS interface can also influence MCLT. The results of this chapter show that the presence of chlorine during the CdS treatment is essential for long MCLT and SIMS measurements revealed segregation of chlorine at the CdTe/CdS interface upon CdS treatment. However, it is not a priory clear if chlorine is electronically active and bound to cadmium and tellurium atoms. Bonding of cadmium and tellurium to the electronegative atom chlorine is investigated with XPS measurements and the results are discussed in the following.

The elemental depth profiles as measured with XPS are shown in Figure 5.7a and b. Before CdS treatment an oxygen concentration of ~4 at% in the CdS layer is observed, which arises from the deposition of CdS using a chemical bath. Consistent with SIMS measurements (Figure 5.3), oxygen content in the CdS layer decreases and tellurium and chlorine content increase upon CdS treatment. Chlorine and oxygen preferentially
Figure 5.6: a) APT measurement in the region of a GB of the CdTe layer in a solar cell, on which a CdS treatment was applied. The GB is visualized in red by the 0.7 at% chlorine isoconcentration surface. Tellurium and sulfur atoms are visualized as dark blue and green dots, respectively. b) 1D-profile of the elemental distribution across the GB (bin size 1 nm) in the region indicated by the cyan box in (a). The inset shows the mass spectrum around the mass of several CdCl-isotopes within a region of grain 1 and within the GB (inside the chlorine isosurface, offset vertically by 20 counts).

Segregate at the CdS surface whereas sulfur concentration decreases at the CdS surface. After CdS treatment tellurium and chlorine content in the CdS layer are ~2 at% and 1-2 at%, respectively. Decrease of oxygen content in the CdS layer occurs in spite
5.3. Impurity distribution

Figure 5.7: *a,b) Depth dependent elemental distribution across the CdTe/CdS interface before (a) and after (b) the CdS treatment as measured with XPS. c) Binding energy of cadmium and tellurium as a function of the sputter time in the sample before (dashed) and after (solid) CdS treatment. $E_B$ of Te 3d$_{5/2}$ in the sample without CdS treatment is shown for sputter depth with tellurium signal above 1 at%. The XPS measurements were repeated and similar results were obtained.*

of an oxygen containing ambient during the CdS treatment. The reason for the loss of oxygen is not clear at the moment, however, the observation was confirmed with SIMS (Figure 5.3) as well as in-situ XRD measurements (Figure 4.3) and is in agreement with previous investigations of air annealing of CdS films [172]. The increase in chlorine and oxygen content as well as the decrease of sulfur suggest, that a cadmium, oxygen and chlorine containing layer is formed at the surface of the CdS layer upon CdS treatment. It is possible, that this layer is not present in the final solar cell because another deposition of CdS by chemical bath is performed after the CdS treatment (see Section 4.3). In
CIGS solar cells, the CBD of CdS can lead to a removal of O\textsubscript{Se} interface acceptors by replacement with S\textsubscript{Se} [157]. Similarly, the replacement of oxygen with sulfur can occur in the present case and this could also be one role of the deposition of the second CdS layer, which is further discussed in Section 4.8.3.

Before CdS treatment a $E\textsubscript{B}$ of Cd 3d\textsubscript{5/2} of 405.26 ± 0.01 eV and 404.90 ± 0.01 eV are measured in the CdS and CdTe layer, respectively – consistent with literature values [173]. The increases in $E\textsubscript{B}$ of Te 3d\textsubscript{5/2} from the CdTe-layer (572.19 ± 0.01 eV) to the CdTe/CdS interface can be explained by an increase in oxygen concentration. Upon CdS treatment $E\textsubscript{B}$ of Cd 3d\textsubscript{5/2} decreases in the CdS layer (405.13 ± 0.01 eV). It furthermore exhibits a depth dependent increase by up to 0.1 eV at the CdTe/CdS interface, which indicates bonding to chlorine [173]. Also Te 3d\textsubscript{5/2} shows a slightly higher $E\textsubscript{B}$ at the CdTe/CdS interface after the CdS treatment, consistent with bonding to chlorine [173]. Chlorine can passivate defect states at the CdTe/CdS interface, similar to what has been found for Te core GBs in CdTe by the use of first-principle calculations [68]. Chlorine segregation at the CdTe/CdS interface was also observed in superstrate configuration CdTe solar cells and a correlation with improved cell performance was found [79].

5.4 Discussion

5.4.1 Impact of sulfur at CdTe grain boundaries

Sulfur at CdTe GBs can passivate defects, explaining the measured improvement in MCLT. This is consistent with observations on CdTe single crystals and nanoparticles. Kang et al. reported on surface passivation of single crystal CdTe and an increased MCLT by a sulfur treatment, which dissociates native oxides and neutralizes dangling bonds at the surface [174]. CdTe/CdS core-shell nanoparticles exhibited a longer MCLT [175] and a higher PL quantum yield [176] than CdTe nanoparticles owing to passivation of the core nanocrystal surface. Previous first-principle studies on the passivation of CdTe GBs in solar cells focused on the effect of co-passivation with copper and chlorine [68], whereas the here presented results show, that the effect of sulfur should also be taken into account. Sulfur only segregates at the CdTe GBs close to the FC (Figure 5.5). In agreement, a TRPL measurement of a solar cell, which was pro-
cessed with treatments and copper doping, revealed a MCLT in the CdTe layer close to the BC of <0.2 ns as measured after mechanical lift-off and illumination from the back side. This shows that the MCLT is depth dependent, in agreement with a spatially resolved TRPL study on cross-sections of CdTe solar cells in superstrate configuration [67].

5.4.2 Mechanism of impurity diffusion

Based on the XPS and SIMS measurements (Figure 5.3 & 5.4 & 5.7), a mechanism for the diffusion and exchange of elements during the CdS treatment is proposed. SIMS measurements strongly suggest, that sulfur diffuses into the CdTe by exchange with oxygen. This observation is supported by the similar chemical nature of the two elements. After CdS treatment, tellurium diffuses from the CdTe layer into the CdS layer and might be replaced with chlorine atoms as indicated by a small increase in chlorine signal in the CdTe layer upon CdS treatment (Figure 5.4). The increase in average chlorine concentration in the CdTe layer is estimated to be ~$3 \times 10^{18}$ cm$^{-3}$ (cf. Section 2.2.2.1), which is in reasonable agreement with the loss in tellurium concentration in the CdTe layer of $7 \times 10^{18}$ cm$^{-3}$ as estimated by using the tellurium concentration in the CdS layer and the thicknesses of the CdS and CdTe layer. In the CdS layer, the oxygen concentration before CdS treatment is approximately equal to the sum of the tellurium and chlorine concentration after CdS treatment, indicating that chlorine and tellurium might replace oxygen in the CdS layer. To conclude, exchange of several elements between the different layers is happening during the CdS treatment and the initial oxygen content in the CdS and CdTe layer might be crucial in determining diffusion of other impurities into these layers, which can occur by exchange with oxygen, while oxygen can leave the sample into the ambient.

Previous studies reported that oxygen addition during the growth of CdTe increases p-type doping in the CdTe layer [71]. It was also found, that MCLT in the CdTe layer improves due to oxygen addition [73], but the oxygen amount in the final device was not investigated. The present study shows that the amount of added oxygen does not necessarily correlate with the oxygen content in the CdTe layer of the finished solar cell as exchange of sulfur and oxygen in CdTe can occur and oxygen content in CdS and CdTe can decrease upon an annealing treatment even in an oxygen containing ambient. It is suggested that the presence of oxygen in the CdTe layer of the final
device is not beneficial for improved MCLT, but that the addition of oxygen during the
growth of CdTe increases MCLT because it facilitates sulfur diffusion along the CdTe
GBs by exchange with oxygen. This is consistent with a study by Zhao et al. [75],
where an increased formation of \( \text{CdS}_x\text{Te}_{1-x} \) due to oxygen addition during the growth
of CdTe was reported. In the solar cells presented in this thesis, no oxygen is added
during the growth of the CdTe layer, but the oxygen amount in the CdTe layer before the
CdS treatment can be influenced by the MoO\
\[x\]
 based BC, which is reduced from MoO\[3\] to MoO\[2\] during processing [92] as well as the presence of oxygen in the annealing
ambient during the CdTe treatment and copper doping process.

5.5 Conclusions and outlook

The results presented in this Chapter show that the CdTe/CdS junction formation pro-
cess developed for substrate configuration solar cells significantly improves MCLT in
the CdTe layer and performance of the solar cell by passivation of GB and interface
defects. This is achieved by a CdCl\[2\] treatment after deposition of the CdS layer, which
leads to sulfur diffusion along CdTe GBs and sulfur segregation within <10 nm from
the GBs. Furthermore, chlorine segregates at the GBs and at the CdTe/CdS interface,
where it can bond to cadmium and tellurium. Various changes in the elemental distribu-
tion in the CdTe/CdS layer stack upon CdS treatment are measured and a mechanism
based on the exchange of elements between the different layers is proposed. Insight
is given into the role of oxygen during the growth of CdTe solar cells, as oxygen con-
tent might determine the degree of impurity diffusion by acting as exchange partner
with sulfur, tellurium and chlorine. In future work, the contribution of recombination at
the CdTe/CdS interface and the CdTe GBs might be separated by the use of different
excitation wavelengths as proposed by Kanevce et al. [177] or by employing spatially
resolved TRPL measurements on cross-sections of solar cells [67]. The results give
guidance for knowledge based efficiency improvements of CdTe solar cells, for exam-
ple by enhancing MCLT through sulfurization of the CdTe GBs and surface with sulfur
containing chemicals other than CdS (see Section 4.8.1). This is especially well appli-
cable to solar cells in substrate configuration and might help to skip the use of CdS in
order to significantly reduce window layer absorption and to improve \( J_{sc} \). Furthermore,
the results might help in developing processes, which further improve MCLT in order to
overcome persistent challenges and to improve $V_{oc}$ towards 1 V.
Chapter 6

Copper doping

This chapter is in part based on the following publications:


6.1 Introduction and effect of copper in superstrate configuration

One of the major challenges of CdTe solar cell research is the achievement of a high hole density in the CdTe layer by means of controlled acceptor doping [131, 178]. It is impeded by the spontaneous formation of compensating donors, a phenomenon commonly observed in the field of II-VI semiconductors [33]. For example, first principle calculations suggest that copper dopants in CdTe can occupy the Cd atomic site acting as an acceptor as well as interstitial positions acting as a donor [145]. Originally, copper has been added to the BC of CdTe solar cells in superstrate configuration with the purpose to improve the contact properties to CdTe by forming a degenerate semiconductor layer, e.g. in the form of Cu$_x$Te, ZnTe:Cu, HgTe:CuTe doped graphite paste.
or As$_2$Te$_3$:Cu [21, 60, 63, 76, 179]. Figure 6.1a shows that the addition of a sufficiently large amount of copper to the BC of superstrate configuration solar cells significantly increases device performance. Figure 6.1b shows, that the temperature during an annealing after copper deposition has to be well controlled to obtain high $V_{oc}$ and FF. In these samples, Cu/Au is used as electrical BC. These results can be explained by the necessity to precisely control the amount of copper diffusing into the CdTe layer during BC annealing. The diffusion of copper into the CdTe layer has been found by SIMS measurements [180] and it was increasingly recognized that copper not only has an impact on BC formation, but that it also increases acceptor concentration and affects carrier lifetime [40, 78]. Figure 6.1a also shows the impact of copper thickness applied at the BC on the SCR of the solar cell. Increasing the amount of copper added to the BC decreases the SCR. This can be explained by the formation of Cu$_{Cd}$ acceptor type defects in the CdTe layer.

![Graphs](image)

**Figure 6.1:**  
*a*) Impact of copper thickness applied at the BC of superstrate configuration solar cells on the efficiency and SCR as determined by $J$-$V$ and $C$-$V$ measurements at room temperature, respectively.  
*b*) Dependence of $V_{oc}$ and FF on the applied temperature during BC annealing.

In substrate configuration copper is commonly added to the devices using the same approach as developed for devices in superstrate configuration, i.e. the use of a copper containing layer with an equivalent copper thickness of several nanometers in the electrical BC structure [84,88,91]. However, this approach is not suitable, because high temperature steps during subsequent device fabrication lead to excessive diffusion of the mobile copper into the adjacent layers, deteriorating their electronic properties.
results in performance degradation of the devices and low reproducibility and the highest achieved efficiency with copper added to the BC is 11.3% [80, 91]. Attempts have also been made to apply copper at different processing steps by dipping the cell into warm CuCl solution, however efficiencies remained around 7% [87].

Previously presented approaches did not prove suitable to achieve desired bulk doping of the CdTe layer in substrate configuration and hence the cell efficiencies remained low. In this chapter, a novel process is introduced for the controlled doping of the CdTe layer by means of vapor deposition of copper after the recrystallization treatment of the CdTe layer and subsequent annealing. A small amount of copper with the equivalent thickness of less than a monolayer is deposited on top of the recrystallized CdTe layer and diffusion into CdTe is promoted by annealing at 400 °C. The process is depicted in Figure 6.2 and the process used for superstrate configuration is shown for comparison. The copper deposition position, the deposited amount and the subsequent annealing temperature differ in the two processes.

Figure 6.2: Schematic of the copper doping process in substrate (a) and superstrate (b) configuration. Back contact (BC), CdTe, CdS and front contact (FC) layers are indicated.
6.2 Copper doping of CdTe thin films

The effect of copper doping on the resistivity and hole density of CdTe layers on glass after CdCl\textsubscript{2} treatment was investigated (Figure 6.3a). Adding 0.8×10\textsuperscript{15} cm\textsuperscript{-2} copper atoms (sub-monolayer with equivalent thickness of 1 Å) to a 5 µm thick CdTe layer results in an abrupt decrease in resistivity by three orders of magnitude and an increase in hole density from <1×10\textsuperscript{12} cm\textsuperscript{-3} to 3.8×10\textsuperscript{14} cm\textsuperscript{-3} (inset of Figure 6.3a). Addition of more copper leads to a small increase in CdTe resistivity accompanied by a decrease in hole density owing to the formation of compensating donor-type defects. This demonstrates that the hole density in polycrystalline CdTe can be maximized by carefully controlling the concentration of the dopant.

6.3 Copper doping of substrate configuration solar cells

6.3.1 Copper distribution

The copper distribution in CdTe solar cells in substrate configuration with 5 µm thick absorber doped using 1.0×10\textsuperscript{15} cm\textsuperscript{-2} copper atoms was investigated by SIMS measurements (Figure 6.4a). Accumulation of copper at the BC/CdTe interface and in the n-type CdS is observed. The copper concentration in the polycrystalline CdTe is found to be (5 ± 3)×10\textsuperscript{17} cm\textsuperscript{-3} (cf. Section 2.2.2.1), in agreement with measurements of devices in superstrate configuration [59, 180]. The inset of Figure 6.4a shows that copper is present in the CdTe layer and the mass of \textsuperscript{63}Cu\textsuperscript{+} is clearly distinguishable from \textsuperscript{126}Te\textsuperscript{2+}. A SIMS measurement of a CdTe solar cell without copper addition was performed for comparison, revealing four copper-related SIMS counts within the CdTe layer, which is about 20 times less than in the copper doped device. This shows, that the copper signal in the CdTe layer is well above the noise level of the instrument.

6.3.2 Carrier collection

To study the depth-dependent collection efficiency of the solar cells EBIC measurements were performed (Figure 6.5a,b). In a copper free cell, the only carriers that are efficiently collected are those generated close to the electrical BC. Upon optimum cop-
6.3. Copper doping of substrate configuration solar cells

![Figure 6.3: Influence of copper doping on resistivity of CdCl$_2$-treated CdTe thin films on glass (a) and efficiency (b) as well as MCLT (c) of CdTe solar cells in substrate configuration as determined by J-V and TRPL measurements, respectively. The inset shows the carrier density and mobility of CdTe thin films on glass as determined by Hall effect measurements. The regions of doping and compensation are indicated.](image)

per doping, the effective carrier collection is observed in a region close to the CdS. Effective carrier collection is desirable in a region where carriers are generated by the incoming sunlight. Over 90% of the usable sunlight is absorbed in the first micrometer of the CdTe layer near the interface to the n-type CdS layer. As such, copper doping shifts the region of effective carrier collection to the region of carrier generation, result-
Chapter 6. Copper doping

**Figure 6.4:** SIMS measurement of the depth dependent copper distribution in completed solar cells in substrate (a) and superstrate (b) configuration. The substrate configuration device is doped with copper using $1.0 \times 10^{15}$ cm$^{-2}$ (equivalent to 1.2 Å layer thickness) copper atoms deposited on the CdTe layer. The superstrate configuration device is doped by deposition of 2.5 nm of copper followed by an annealing at 215 °C. The inset of (a) shows the mass spectrum around the mass of $^{63}\text{Cu}^+$ in the CdTe layer from sputter cycle 500 to 1000.

...ing in a dramatic increase in efficiency from less than 1% to over 12% (Figure 6.3b). All PV parameters are improved and EQE increases from ~10% to ~90% (Figure 6.6a,b). The EQE of the copper free cell exhibits highest values for photons with wavelength of 800-850 nm, which have a higher probability to penetrate deeper into the CdTe layer towards the region of effective carrier collection.

## 6.3.3 Simulations

The 1-D simulation software SCAPS [144] was used to investigate the influence of doping on $J-V$ and EQE characteristics (Figure 6.6c,d). EQE simulation of a solar cell without acceptor doping of the absorber confirms the experimentally obtained curve for the cell without copper addition. For the simulation of the copper doped device, acceptor-type defects with a concentration of $6.5 \times 10^{14}$ cm$^{-3}$ were introduced into CdTe in order to obtain a hole density of $3.8 \times 10^{14}$ cm$^{-3}$ consistent with Hall effect measurements (cf. Section 2.2.4). This results in a change in the EQE as observed upon copper addition.
6.3. Copper doping of substrate configuration solar cells

Figure 6.5: a,b) EBIC measurements of CdTe solar cells processed without copper (a) and with $1 \times 10^{15}$ cm$^{-2}$ copper atoms deposited on the CdTe layer with subsequent annealing at 400 °C (b). EBIC signal is normalized to 100%. For better visualization, EBIC signal below 30% is not shown. Grain contrast arises from topography due to cleaving of the sample. The profiles on the left show the horizontally averaged EBIC signal (black, collection). Furthermore, a schematic of the depth dependent carrier generation under normal operation in sunlight is shown (red, generation). c,d) Proposed energy band diagrams for CdTe solar cells without (c) and with optimum copper doping (d). Conduction band energy $E_C$, valence band energy $E_V$ and built-in voltage $V_{bi}$ are indicated.

To reproduce the observed behavior of the $V_{oc}$ completely, the valence band energy barrier at the BC/CdTe interface is increased in the simulation of the sample without acceptor doping. This is motivated by the reported observation that copper reduces this barrier [76, 181] and by the SIMS measurement shown in Figure 6.4a, which indicates that copper accumulates at the BC/CdTe interface.

6.3.4 Excessive copper doping

Excessive copper doping leads to a decrease of all PV parameters and a reduced EQE in the long wavelength region (Figure 6.6a,b). The net hole density is reduced (inset of Figure 6.3a) and the MCLT decreases as confirmed with TRPL measurements
Figure 6.6: a,b) $J$-$V$ (a) and EQE (b) measurements of CdTe solar cells processed without copper, with optimum copper ($8 \times 10^{14} \text{ cm}^{-2}$ copper atoms) and with excessive copper ($2.4 \times 10^{15} \text{ cm}^{-2}$ copper atoms). Efficiencies $\eta$ of the corresponding cells are given in the inset. c,d) Simulations of $J$-$V$ (c) and EQE (d) characteristics of CdTe solar cells with undoped (no acceptors), doped ($6.5 \times 10^{14} \text{ cm}^{-3}$ acceptors) and compensated ($1 \times 10^{15} \text{ cm}^{-3}$ acceptors and $0.9 \times 10^{15} \text{ cm}^{-3}$ donors) absorber. The undoped sample is simulated both with standard (0.4 eV, dashed line) and with increased (0.7 eV, solid line) valence band energy barrier at the BC/CdTe interface.

(Figure 6.3c). In simulations, an increase of the acceptor-type defect concentration to $1 \times 10^{15} \text{ cm}^{-3}$ together with the introduction of compensating donor-type defects with a concentration of $9 \times 10^{14} \text{ cm}^{-3}$ reproduce $J$-$V$ and EQE characteristics of the sample with excess copper (Figure 6.6c,d). The results support an explanation of the reduced device performance with excessive copper doping by the formation of deep donors, which act as recombination centers and reduce the net hole density.
6.3. Copper doping of substrate configuration solar cells

6.3.5 Solar cell performance

The controlled doping of CdTe has enabled the achievement of unprecedented efficiencies up to 13.6% for CdTe solar cells in substrate configuration on glass substrates. \( J-V \) and EQE measurements of the solar cell are shown in Figure 6.7. Several samples with efficiencies above 13% were produced and Table 6.1 shows the PV parameters of a selection of cells, demonstrating the good reproducibility of the process.

<table>
<thead>
<tr>
<th>Solar Cell</th>
<th>( \eta ) (%)</th>
<th>( V_{oc} ) (mV)</th>
<th>( J_{sc} ) (mA·cm(^{-2}))</th>
<th>FF (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>13.6</td>
<td>852</td>
<td>21.2*</td>
<td>75.3</td>
</tr>
<tr>
<td>B</td>
<td>13.4</td>
<td>841</td>
<td>21.7*</td>
<td>73.4</td>
</tr>
<tr>
<td>C</td>
<td>13.2</td>
<td>841</td>
<td>20.6</td>
<td>76.2</td>
</tr>
<tr>
<td>D</td>
<td>13.0</td>
<td>842</td>
<td>20.3</td>
<td>76.1</td>
</tr>
</tbody>
</table>

Table 6.1: Efficiency and PV parameters of a selection of CdTe solar cells in substrate configuration on glass, which were produced using the presented process. Each sample was processed separately. Two of the samples have an optimized AR coating (marked with *), explaining the slight variation in \( J_{sc} \).

Figure 6.7: \( J-V \) (a) and EQE (b) measurements of the record efficiency solar cell with 13.6%. PV parameters are shown in Table 6.1 (Solar cell A).
6.3.6 Stability

Copper is known to influence stability of CdTe solar cells [60, 63, 79, 182]. It was found that excess copper at the BC reduces device stability as it can diffuse towards the p-n junction [60, 79]. In the case of the presented copper doping method, a controlled amount of copper is added close to the FC. This approach is expected to avoid excessive copper diffusion from the BC towards the p-n junction, which could translate to improved device stability. After storage of the record efficiency sample at room temperature under indoor illumination for more than 6 months, the efficiency of the best cells was unchanged at 13.6%, indicating good stability of the cells. Standardized stability tests of encapsulated cells for long durations are the subject of further investigations within an ongoing PhD thesis.

6.4 Discussion

The results show, that the electronic properties of CdTe and the efficiency of the solar cells are enhanced by carefully controlling copper doping of the CdTe. These observations can be explained by the amphoteric doping behavior of copper in CdTe. Copper addition up to an optimum amount increases acceptor concentration, e.g. due to the formation of CuCd. Further increase in copper concentration decreases hole density and MCLT owing to the formation of compensating donor-type defects, e.g. Cu, [145]. The formation of defects upon excessive copper doping is also indicated by AS measurements (Figure 6.8a). Whereas the device with optimum amount of copper shows a small AS signal at relatively low energy, a large signal at higher energy arises for devices doped with excessive amounts of copper. It should be noted that the absolute energetic position of the signal varied upon repetition of the experiment and is therefore not discussed. However, the general trend of an increased defect density and energy upon excessive copper doping is observed several times.

The measured copper concentration in the doped polycrystalline CdTe of $(5 \pm 3) \times 10^{17}$ cm$^{-3}$ is three orders of magnitude higher than the measured hole density of $3.8 \times 10^{14}$ cm$^{-3}$. Part of the difference is attributed to the fact that the CuCd acceptor has a large activation energy. However, according to numerical simulations only $6.5 \times 10^{14}$ cm$^{-3}$ copper atoms are required to obtain the measured hole density assuming the ener-
Figure 6.8: a) AS measurements of devices doped with optimum amount of copper and with excessive amounts of copper. b) Ionization degree of acceptors with activation energy $E_a$ and concentration $N_a$ as calculated using SCAPS simulations. The white rectangle indicates the region where solar grade copper doped CdTe layers are suspected.

generic depth of the copper related acceptor level to be 220 meV (see Section 2.2.4). A detailed investigation of the degree of acceptor ionization and its dependence on the acceptor ionization energy and concentration was performed using SCAPS simulations and the results are shown in Figure 6.8b. The degree of ionization of the acceptor varies depending on its activation energy and concentration; however, it remains above 20% in the region where solar grade copper doped CdTe layers are suspected. Therefore, the main part of the difference between the measured copper concentration and hole density cannot be explained by partial ionization arising from the energetic depth of the acceptor. The difference is mainly attributed to the preferential accumulation of copper at GBs, which is reported to be energetically favored [68]. The use of advanced characterization techniques such as APT and SIMS chemical imaging was tested to investigate the potential GB segregation of copper. However, the combination of very low copper concentration as well as the peak overlaps of $^{63}\text{Cu}^+$ and $^{65}\text{Cu}^+$ with $^{126}\text{Te}_2^{2+}$ and $^{130}\text{Te}_2^{2+}$, respectively, restricted the investigation of potential copper segregation at GBs with these methods. An investigation of copper distribution within the polycrystalline CdTe layer therefore remains to be done by other characterization methods such as electron energy loss spectroscopy.

Copper doping changes the position of effective carrier collection as measured with
EBIC. This is explained with the energy band diagrams in Figure 6.5c,d. A copper free cell has a SCR that extends over the whole ~5 µm absorber as confirmed with C-V measurements. The low acceptor concentration leads to a small band bending and small electric field close to the CdS layer – the result being that carriers are collected less efficiently even in the SCR. Only close to the electrical BC, Fermi level pinning at the BC/CdTe interface can cause sufficient band bending to allow efficient collection of carriers. Doping CdTe with $1 \times 10^{15}$ cm$^{-2}$ copper atoms results in a SCR of about 1.8 µm (from C-V measurements) and causes sufficient band bending close to the CdS to generate a strong electric field, leading to effective carrier collection (Figure 6.5b).

In Section 6.3.3 the impact of copper doping on performance is explained by the dual role of copper on CdTe acceptor doping and reduction of valence band energy barrier at the BC/CdTe interface. Initially, other potential mechanisms were also investigated to explain the impact of copper doping on performance, especially in view of the accumulation of copper in the CdS layer and at the BC interface as measured with SIMS (Figure 6.4). These considerations are discussed in the following.

To investigate the influence of copper impurities in the CdS layer, the impact of copper doping on the performance of solar cells processed without CdS was compared with its impact on the performance of solar cells processed with CdS layer. In devices processed without CdS layer, a clear beneficial effect of copper doping is observed with efficiency rising from ~0.1% to ~4% with a strong increase in $J_{sc}$ upon addition of less than 1 Å of copper and a deterioration of efficiency to below 2% upon addition of more than 2 Å of copper. Even though the results are on a low efficiency level due to the inferior i-ZnO-CdTe junction properties [17], similar trends are observed as for solar cells employing a CdS layer, supporting that the observed changes in performance mainly arise from effects of copper in the CdTe layer, rather than its effect in the CdS layer.

To investigate if the low $J_{sc}$ in undoped devices can be explained by a large valence band energy barrier at the BC/CdTe interface, temperature dependent $J-V$ measurements of devices doped with different amounts of copper were performed and the temperature dependent $J_{sc}$ values were extracted. Using the theory of thermionic emission over a potential barrier [183] allows only a poor fit of the extracted values and results in energy barrier heights of ~10 and ~100 meV for copper free and copper containing cells, respectively. These values are well below commonly observed values for Schottky barriers. This, as well as the increase of the energy upon copper addition show, that a Schottky barrier at the BC is not responsible for the low $J_{sc}$ in copper free devices.
The dual role of copper on the BC properties and the CdTe acceptor doping is further investigated by comparing the influence of copper doping in substrate and superstrate configuration solar cells. Figure 6.9a,b shows $J-V$ characteristics of CdTe solar cells without copper, with copper amounts below optimum and with optimum amount of copper for both device configurations. While undoped and optimal doped solar cells show $J-V$ characteristics, which are similar for the two device configurations, the $J-V$ characteristics of devices containing copper amounts below optimum significantly vary for the two configurations. In substrate configuration the $J_{sc}$ is close to the $J_{sc}$ of optimally doped solar cells, while the $V_{oc}$ is well below the value of the device with optimum amount of copper. In superstrate configuration, the opposite trend is observed. These observations can be explained considering the different positions of copper addition (Figure 6.2). Small amounts of copper in substrate configuration will mainly increase the hole density in the CdTe layer, while small amounts of copper in superstrate configuration will mainly reduce the energy barrier at the BC. The $J-V$ characteristics can be well reproduced with SCAPS simulations by changing these parameters and the results are shown in Figure 6.9c,d.

The results show that substrate and superstrate configuration solar cells need different copper addition methods to achieve good electronic properties. Comparison of the resulting copper distributions (Figure 6.4) shows that both methods lead to accumulation of copper at the BC/CdTe interface and in the CdS as well as a small copper concentration in the CdTe layer. While the amount of copper at the electrical BC and in the CdS layer differs in the two configurations, the copper concentration in the CdTe layer is similar, supporting the importance of the precise control of copper amount in the CdTe layer in order to maximize its hole density. The precise control of the copper concentration in the CdTe layer of superstrate configuration solar cells can be achieved by the control of BC annealing temperature (Figure 6.1b & [78]). In substrate configuration this approach is not possible because the BC is deposited before deposition of the CdTe layer. Therefore, copper concentration in solar cells in substrate configuration in the presented process is controlled by the added amount of copper.

During development of the presented process, copper addition at several processing stages was tested: at the BC, on the CdTe layer (before or after the CdTe treatment), on the CdS layer (before or after CdS treatment). Highest efficiencies are achieved with copper addition on the CdTe layer after its recrystallization treatment. It is suggested that this position of copper addition is advantageous compared to addition at other pro-
Chapter 6. Copper doping

Figure 6.9: a,b) $J$-$V$ measurements of solar cells in substrate (a) and superstrate (b) configuration processed using 0/0.1/1.0Å equivalent and 0/2/32Å of copper, respectively. c,d) SCAPS simulations using different valence band energy barriers at the BC/CdTe interface $\Phi$ and acceptor concentrations $N_a$ to reproduce the measurements of (a) and (b). Simulation parameters in [132].

Processing steps, even though it cannot be excluded, that adaptation of processing conditions could also enable high efficiencies with copper added at a different processing stage. Advantages of performing the copper doping after recrystallization of the CdTe layer are discussed in the following. Chlorine incorporated into the CdTe grains during the CdCl$_2$ treatment of the CdTe can act as a donor [34] compensating the copper induced increase in hole density when copper doping is done before the CdCl$_2$ treatment. This is supported by the fact that highest efficiencies in superstrate configuration are also achieved by addition of copper after the CdCl$_2$ treatment of the CdTe.
advantage can be the presence of oxygen during the copper diffusion treatment. During process development, the addition of oxygen during the copper diffusion treatment was found to be beneficial for device performance. Oxygen is known to enhance p-type doping [71] and can generate cadmium vacancies [34], enhancing the formation of Cu$_{Cd}$ acceptors in favor of donor type Cu$_i$. Furthermore, oxygenation of the CdTe surface, which can happen during the copper diffusion treatment can be important for p-n junction formation by facilitating sulfur diffusion from the CdS into the CdTe layer (see Chapter 5).

6.5 Conclusions and outlook

To conclude, a novel concept for the controlled doping of the CdTe layer of substrate configuration devices is introduced. The precisely controlled copper doping of CdTe results in reduced compensation of acceptors, increased hole density, improved MCLT, and a pronounced improvement of the collection of photo-generated charge carriers in CdTe close to the CdTe/CdS junction and enables CdTe solar cells in substrate configuration with efficiencies up to 13.6%. The dual role of copper on the hole density in the CdTe layer and the valence band energy barrier at the BC/CdTe interface is discussed. Furthermore, the amphoteric behavior of copper is suggested as the reason for the necessity to precisely control copper concentration in the CdTe. The developed process for substrate configuration solar cells offers new opportunities in CdTe PV research to increase $V_{oc}$ towards 1 V through further improved doping procedures. Substrate configuration growth allows better control of p-type doping of the absorber in the absence of the n-type CdS layer and decouples doping processes from the p-n junction formation, which is a significant advantage over superstrate configuration (cf. Chapter 3). Attempts to further increase hole density are discussed in Chapter 7.
Chapter 7

Towards further increased hole density

Parts of the results of this chapter were obtained during the Master thesis of Michael Wyss and the Master project of Elias Rehmann [184, 185].

7.1 Introduction

A way to overcome persistent challenges of limited $V_{oc}$ in high-efficiency CdTe solar cells is the increase of hole density in the CdTe layer from present values of $\sim 1 \times 10^{14}$ cm$^{-3}$ towards $1 \times 10^{17}$ cm$^{-3}$ [131]. The p-type conductivity in state-of-the-art CdTe solar cells is mainly established by copper doping (Chapter 6) and also the CdCl$_2$ treatment, which introduces chlorine and oxygen impurities can influence the p-type conductivity in the CdTe layer [34, 69, 72, 186]. Extrinsic dopants from group I and group V of the periodic system have been used to generate p-type conductivity in CdTe crystals [33, 146]. Some of these dopants were also tested in CdTe solar cells, even though with limited success [178].

In this chapter, experiments on solar cells in superstrate and substrate configuration as well as CdTe thin films on glass are discussed, which target the improvement of hole density in the CdTe layer beyond the values presented in Chapter 6 in order to increase the $V_{oc}$ towards 1 V. The experiments were successful to increase the hole density in the CdTe layer of solar cells as measured with $C-V$ measurements and in CdTe layers
as measured with Hall effect measurements. Hole densities up to $5.7 \times 10^{16}$ cm$^{-3}$ are achieved; however, the high hole densities did not lead to high-efficiency solar cells. The reason for the limited success of additional doping of the CdTe layer for performance improvement in CdTe solar cells is discussed and ways to overcome the limitations are suggested.

### 7.2 Superstrate configuration

Doping of the CdTe layer of superstrate configuration solar cells with extrinsic impurities from group I and group V of the periodic system is investigated. The extrinsic dopants are typically applied by vapor deposition of Å to few nanometer thickness before, during or after CdCl$_2$ treatment. Some of the dopants increase hole density as confirmed by $C$-$V$ measurements and as an example the effects of sodium doping are discussed in detail in Chapter 3. Nevertheless, none of the methods lead to an improvement in performance compared to the baseline process.

$C$-$V$ measurements were performed to investigate the doping density and SCR in CdTe solar cells. Figure 7.1a shows the $C$-$V$ measurement of a high efficiency solar cell. The extracted apparent shallow acceptor concentration, apparent hole density at RT and SCR are $3.7 \times 10^{13}$ cm$^{-3}$, $1.2 \times 10^{14}$ cm$^{-3}$ and 1.5 µm, respectively. $C$-$V$ measurements were performed on various samples, which were processed as described in Section 2.1.1 with the following variations:

- Addition of different amounts of NaF, NaCl, LiCl or Sb.
- Addition of different amounts of Cu or Ag to the BC.
- Variation of CdTe and CdS thickness.
- Variation of CdCl$_2$ treatment duration, temperature, CdCl$_2$ amount and oxygen content in the annealing ambient.
- Variation of CdTe deposition temperature.

The large number of $C$-$V$ measurements of differently processed samples motivate to investigate correlations between electronic properties and device performance. In
7.3 Doping of CdTe thin films and substrate configuration solar cells

Figure 7.1b the $V_{oc}$ of these devices is plotted against the apparent hole density. Apparent hole density varies by about 2 orders of magnitude. No clear correlation between $V_{oc}$ and apparent hole density is observed. Highest $V_{oc}$ of $\sim 850 \text{ mV}$ is achieved with apparent hole densities between $7 \times 10^{13} \text{ cm}^{-3}$ and $1 \times 10^{15} \text{ cm}^{-3}$, while samples with apparent hole density above $1 \times 10^{15} \text{ cm}^{-3}$ tend to have a reduced $V_{oc}$. The apparent shallow acceptor concentration from low temperature $C$-$V$ measurements is evaluated and the $V_{oc}$ is plotted against this value. Again, no correlation is found. This indicates that another effect is dominating the performance in the investigated devices, which could possibly be the MCLT. Future investigations should focus on the simultaneous improvement of hole density and MCLT.

![Graph](image)

**Figure 7.1:** a) Depth dependent apparent acceptor concentration as determined by a $C$-$V$ measurement of a high-efficiency solar cell in superstrate configuration. b) Apparent hole density/apparent shallow acceptor concentration as determined from $C$-$V$ measurements versus $V_{oc}$ of the corresponding devices.

7.3 Doping of CdTe thin films and substrate configuration solar cells

Arsenic impurities in CdTe generate relatively shallow acceptor states and the energetic depth of As$_{Te}$ acceptors in CdTe was reported to be around 100 meV [187,188]. Arsenic has already been used for p-type doping of CdTe solar cells [189]. In the experiments
explained in the following, arsenic doping of CdTe thin films on glass is done by annealing the sample together with arsenic pieces in a closed glass ampoule. The effect of arsenic doping on the hole density in the CdTe layer (measured by Hall effect) is studied together with the effects of the CdCl₂ treatment and copper doping. Table 7.1 shows the highest achieved hole densities and the corresponding processes. Hole density up to $5.7 \times 10^{16}$ cm$^{-3}$ is reached by doping the CdTe layer with arsenic without addition of copper. The corresponding samples, which are identically processed but additionally doped with copper exhibit hole densities, which are almost an order of magnitude lower than in the reference without copper doping. At first glance, these results appear to contradict the results of Chapter 6. However, the opposite effects of copper can be explained considering the amphoteric behavior of copper in CdTe and the dependence of defect formation energies on Fermi level position. In lowly doped CdTe formation of the acceptor Cu$_{Cd}$ is preferred, while in highly doped CdTe formation of the donor Cu$_{i}$ is preferred [190]. Table 7.1 shows that the hole density changes with time, but also in the relaxed state relatively high hole densities are obtained.

Arsenic incorporation into the CdTe layer is investigated by SIMS measurements (not shown). Arsenic accumulates at the surface of the CdTe layer and arsenic counts within the main part of the CdTe layer are below the detection limit of the system. Considering relative sensitivity factors of Cu$^{+}$- and As$^{-}$-detection with SIMS [191] and the results on quantitative SIMS presented in Chapter 6, an upper limit of the arsenic concentration of $4 \times 10^{17}$ cm$^{-3}$ is estimated. This value is about an order of magnitude above the measured hole density. Even though presence of arsenic in the main part of the CdTe film could not be proven, arsenic concentration in the CdTe layer can be large enough to explain the measured hole density.

Solar cell were processed using CdTe layers identically prepared as those, which led to hole densities above $1 \times 10^{16}$ cm$^{-3}$ (Table 7.1). Performance of the samples is very low, with $V_{oc}$ only up to 532 mV. Still, $J_{sc}$ values above 20 mA·cm$^{-2}$ are obtained without copper doping, confirming the increased hole density upon arsenic doping (cf. Chapter 6). Additional copper doping leads to $V_{oc}$ up to 669 mV. The results show that even though arsenic doping increases hole density in the CdTe layer, the increased hole density does not yet lead to improved performance. Furthermore, the results confirm the importance to add copper even in highly doped CdTe films and the reason for this could be related to its additional effect on the BC properties as discussed in Chapter 6. It is suggested that the overall low performance of the arsenic doped samples arises from
7.4. Discussion

In state-of-the-art solar cells, copper doping is important for highest device performance. The results shown in this chapter indicate that copper doping can pin carrier density at present values around $1 \times 10^{14}$ cm$^{-3}$ which can be related to the amphoteric behavior of copper in CdTe. In order to further increase hole density in CdTe solar cells, it might be necessary to adapt the copper doping process to the additionally introduced dopant or even to avoid copper doping. Considering the dual role of copper discussed in Chapter 6 on acceptor doping in the CdTe layer and the BC properties, this requires the search for an alternative route to reproduce its effect on BC properties. This could be done by changing the BC material or introducing other impurities, which have a similar effect as copper on the BC formation but without its amphoteric behavior on the hole density in the CdTe layer. Copper can also contribute to GB passivation [68]. This effect could possibly be reached by adapting the conditions of the CdCl$_2$ treatments (Chapter 5). Adapting all the aforementioned properties will require extensive development work and this could be the reason why an appropriate method for increasing doping

<table>
<thead>
<tr>
<th>Process</th>
<th>$N_{\text{Quenched}}$ (cm$^{-3}$)</th>
<th>$N_{\text{Relaxed}}$ (cm$^{-3}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>as measure w/o Cu</td>
<td>with Cu</td>
</tr>
<tr>
<td>As (mg)</td>
<td>CdCl$_2$ treatment</td>
<td></td>
</tr>
<tr>
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<td>no</td>
<td>$5.7 \times 10^{16}$</td>
</tr>
<tr>
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<td>yes</td>
<td>$4.4 \times 10^{16}$</td>
</tr>
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<td>yes</td>
<td>$2.1 \times 10^{16}$</td>
</tr>
<tr>
<td>20</td>
<td>no</td>
<td>$1.6 \times 10^{16}$</td>
</tr>
</tbody>
</table>

Table 7.1: Achieved hole densities in CdTe thin films on glass as measured with Hall effect measurements and the corresponding process. Hole density is given for the quenched state (within few hours after post-processing annealing) and in the relaxed state (after at least 2 weeks of storage). Samples which were processed identically but with additional copper doping are shown for comparison.

the segregation of arsenic at the surface of the CdTe layer (measured with SIMS), which deteriorates p-n junction properties. To overcome this, processes should be developed which enable homogeneous distribution in the CdTe layer without accumulation at the surface of the CdTe layer, for example by using co-evaporation of CdTe and arsenic.
density for $V_{oc}$ beyond $\sim$860 mV is not yet known in the scientific community. However, the suggested approaches could be helpful to achieve this goal.

### 7.5 Conclusions and outlook

The apparent hole density in solar cells in superstrate configuration was varied by two orders of magnitude. No correlation between apparent hole density and $V_{oc}$ could be found. Arsenic doping of CdTe thin films increases hole density to beyond $1 \times 10^{16}$ cm$^{-3}$ when no copper is present. Additional copper doping in these highly doped films reduces hole density, the opposite of the effect of copper in lowly doped CdTe (cf. Chapter 6). These observations are explained by the amphoteric behavior of copper in CdTe and the dependance of defect formation energy on Fermi level position. The tested approaches to dope the CdTe layer did not enable an increased $V_{oc}$. To enable an improved $V_{oc}$ by increasing hole density in the CdTe layer several steps of the process need to be adapted and possible routes to achieve this are discussed.
Chapter 8

Achieved efficiencies and comparison of device configurations

8.1 Solar cell performance

In superstrate configuration efficiencies up to 15.6% and 13.5% are achieved on BSG and SLG using a low temperature process. Figure 8.1 shows the $J$-$V$ and EQE measurements of the record efficiency device and Table 8.1 shows the corresponding PV parameters.

Table 8.1 additionally shows PV parameters of devices with high $V_{oc}$, $J_{sc}$ and FF as well as of a device which combines high $V_{oc}$ and FF. Comparable $V_{oc}$ and FF values are achieved as the record cells grown at high temperature (Section 1.2.5), showing that very good electronic properties are also possible with a low temperature process. Only the $J_{sc}$ differs, which mainly arises from a different transmission of the window layer stack (TCO and CdS).

Efficiencies up to 13.6% are achieved in substrate configuration on glass substrates. The corresponding $J$-$V$ and EQE characteristics as well as PV parameters are shown in Chapter 6. $V_{oc}$ of 852 mV (cf. Chapter 6), $J_{sc}$ of 23.1 mA·cm$^{-2}$ (cf. Chapter 4) and FF of 76.2% (cf. Chapter 6) are achieved on separate devices. High efficiency is confirmed by external calibration measurements at Fraunhofer ISE. 13.5% efficiency is certified and the corresponding $J$-$V$ and EQE measurements are shown in Figure 8.2. The performance significantly exceeds the former highest certified efficiency of 11.0% for CdTe solar cells in substrate configuration on glass [80].
Figure 8.1: IV (a) and EQE (b) characteristics of the internal record efficiency solar cell in superstrate configuration with 15.6 % efficiency.

<table>
<thead>
<tr>
<th>Sample</th>
<th>η</th>
<th>V&lt;sub&gt;oc&lt;/sub&gt;</th>
<th>J&lt;sub&gt;sc&lt;/sub&gt;</th>
<th>FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>High η</td>
<td>15.6</td>
<td>834</td>
<td>24.7</td>
<td>75.9</td>
</tr>
<tr>
<td>High V&lt;sub&gt;oc&lt;/sub&gt;</td>
<td>13.9</td>
<td>862</td>
<td>22.1</td>
<td>72.8</td>
</tr>
<tr>
<td>High J&lt;sub&gt;sc&lt;/sub&gt;</td>
<td>13.6</td>
<td>817</td>
<td>25.0</td>
<td>66.4</td>
</tr>
<tr>
<td>High FF</td>
<td>14.8</td>
<td>842</td>
<td>22.7</td>
<td>77.5</td>
</tr>
<tr>
<td>High V&lt;sub&gt;oc&lt;/sub&gt; and FF</td>
<td>15.0</td>
<td><strong>856</strong></td>
<td>22.9</td>
<td><strong>76.7</strong></td>
</tr>
<tr>
<td>SLG substrate</td>
<td>13.5</td>
<td>853</td>
<td>21.3</td>
<td>74.4</td>
</tr>
</tbody>
</table>

Table 8.1: PV parameters of the internal record efficiency devices in superstrate configuration on BSG and SLG as well as of solar cells with high V<sub>oc</sub>, J<sub>sc</sub> and FF.

8.2 Solar cells on flexible metal foil

One of the big advantages of substrate configuration is the possibility to grow solar cells on flexible metal foil substrates. As a proof of concept the developed process was applied on metal foils and certified efficiencies of 11.5% and 10.9% on molybdenum and steel foil substrates were achieved, respectively. The corresponding PV parameters and J-V and EQE characteristics are shown in Table 8.2 and Figure 8.2, respectively. The performance greatly exceeds the previous record efficiency of 7.8% [20], proving that highly efficient flexible CdTe solar cells on non-transparent substrates are possible. The
remaining gap between efficiencies on glass and on metal foil substrates are expected to be closed by adapting processing temperatures to the changed thermal mass of the substrate and by reducing impurity diffusion from the steel foil substrate through the application of improved diffusion barrier layers.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>( \eta )</th>
<th>( V_{oc} )</th>
<th>( J_{sc} )</th>
<th>FF</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass</td>
<td>13.5 ± 0.4</td>
<td>855 ± 4</td>
<td>21.8 ± 0.6</td>
<td>72.5 ± 0.7</td>
<td>0.270 ± 0.003</td>
</tr>
<tr>
<td>Molybdenum foil</td>
<td>11.5 ± 0.4</td>
<td>821 ± 4</td>
<td>22.0 ± 0.6</td>
<td>63.9 ± 0.6</td>
<td>0.524 ± 0.007</td>
</tr>
<tr>
<td>Steel foil</td>
<td>10.9 ± 0.4</td>
<td>785 ± 4</td>
<td>21.8 ± 0.6</td>
<td>63.9 ± 0.6</td>
<td>0.576 ± 0.007</td>
</tr>
</tbody>
</table>

Table 8.2: Efficiency and PV parameters of substrate configuration CdTe solar cell on different substrates as certified by Fraunhofer ISE.

Figure 8.2: \( J-V \) (a) and EQE (b) measurements of CdTe solar cell in substrate configuration on different substrates as certified by Fraunhofer ISE. The corresponding PV parameters and efficiency are shown in Table 8.2

8.3 Comparison of device configurations

In this chapter, similarities and differences of the properties of substrate and superstrate configuration CdTe solar cells are explained and discussed, with a focus on the p-n junction.
8.3.1 Structural properties

In both configurations the CdTe layer is grown with the same method of HVE and is subsequently annealed in the presence of CdCl₂. The CdTe layer grows in zincblende structure and the CdCl₂ treatment leads to similar grain growth and reduction of texture in both configurations [91].

At Empa the CdS layer in superstrate configuration is grown by HVE, while the CdS layer in substrate configuration is grown by CBD. The CdS layer in superstrate configuration consists of large grained CdS with grain sizes of several 100 nm due to the CdCl₂ treatment (Figure 3.1 & [58]). In substrate configuration the CdS layer consists of a double layer, with the first (CdCl₂ treated) layer having grain sizes up to more than 100 nm and the second CdS layer having nanocrystalline grains.

In superstrate configuration, the CdS and CdTe layers intermix during the CdCl₂ treatment as observed by several research groups using XRD [53]. On the other hand, GIXRD measurements of substrate configuration solar cells revealed no detectable formation of a CdSₓTe₁₋ₓ phase upon CdS treatment (Figure 5.2). This difference is further discussed in Section 8.3.4.

8.3.2 Impurities

Figure 8.3 shows a SIMS measurement of a solar cell in superstrate configuration. The corresponding measurement - also measured during sputtering from the BC to the FC - of a substrate configuration device is shown in Figure 5.4b. Sulfur shows comparable relative depth dependency in both configurations, with the signal rising towards the FC. However, the absolute sulfur amount significantly differs in the two configurations. The superstrate device has approximately two orders of magnitude higher sulfur signal than the substrate configuration device. This is due to a pronounced difference in sulfur diffusion from the CdS into the CdTe layer as further discussed in Section 8.3.4. Chlorine and oxygen also have a similar depth dependent distribution in both configurations with higher signals close to the BC and in the CdS layer. However, the amount of chlorine and oxygen in the main part of the absorber of the superstrate configuration solar cell is approximately two and six times higher than in substrate configuration, respectively. The higher chlorine signal in superstrate configuration might be related to the higher sulfur content in the CdTe layer. Considering, that chlorine preferentially segregates in
the CdS layer as compared to the CdTe layer, a preferred segregation in CdS$_x$Te$_{1-x}$ as compared to CdTe is possible. The higher chlorine signal in the CdS layer than in the CdTe layer are most probably not arising from matrix effects in the SIMS as quantitative SIMS has shown similar results [192]. The different oxygen amount can be related to the different processes. In superstrate configuration oxygen is supplied during the CdCl$_2$ treatment, while in substrate configuration the last annealing step in oxygen containing ambient at temperatures above 300 °C is the CdS treatment, which has been found to lead to a decrease in oxygen content in both the CdS and CdTe layer (cf. Chapter 5).

The similarities and differences of copper distribution in the two configurations as well as its origins and effects on device performance are discussed in detail in Chapter 6. The main difference is the copper content at the BC.

To conclude, adaptation of processing conditions from superstrate to substrate configuration has resulted in similar impurity distributions in the two configurations, while the main differences are the degree of sulfur diffusion into the CdTe layer and the copper content at the BC.

![Graph showing SIMS measurement](image)

**Figure 8.3:** SIMS measurement of a CdTe solar cells in superstrate configuration. The corresponding measurement of a substrate configuration device is shown in Figure 5.4b.
**8.3.3 Electronic properties and solar cell performance**

To compare acceptor doping and MCLT of the CdTe layer in the two configurations, temperature dependent $C-V$ measurements as well as TRPL measurements were performed. Figure 8.4a shows a $C-V$ measurement of a high-efficiency solar cell in substrate configuration, revealing an apparent shallow acceptor concentration, apparent hole density at RT and SCR of $3.3 \times 10^{13}$ cm$^{-3}$, $1.1 \times 10^{14}$ cm$^{-3}$ and $1.8$ µm, respectively. These values are very similar to the values measured in a high-efficiency solar cell in superstrate configuration (cf. Chapter 7). Figure 8.4b shows TRPL measurements of high-efficiency solar cells in both configurations. The measured TRPL decay is similar in the two configurations. These measurements show, that similar electronic properties are obtained in the two configurations.

In substrate and superstrate configuration 13.6% and 15.6% efficiency are achieved, respectively. In both configurations similar $V_{oc}$ and FF are obtained, while the $J_{sc}$ differs. The difference in $J_{sc}$ is explained below with the help of EQE measurements. The $V_{oc} = 852$ mV and FF = 75.3% of the substrate configuration device are especially noteworthy as they almost reach the values of the record efficiency cell in superstrate configuration ($V_{oc} = 857$ mV, FF = 80.0% [14]), while earlier substrate configuration devices have especially suffered from low FF values, mostly below 60% [82, 96]. This shows that the CdTe/CdS junction and electrical BC of devices in substrate configuration can be produced with a quality comparable to the record superstrate device.

In the following, similarities and differences of $J-V$ characteristics of substrate and superstrate configuration devices are investigated in more detail by comparing the record efficiency solar cell in substrate configuration with the sample "high $V_{oc}$ and FF" from Table 8.1. The $J-V$ characteristics are normalized to the same $J_{sc}$ to enable comparison of the shape of the curves (Figure 8.5a). In spite of the similar FF, there are small differences in the shape of the curves. The more obvious difference occurs in the region above ~0.7 V. The substrate configuration device has a more pronounced rollover in the region beyond $V_{oc}$ and a corresponding higher apparent series resistance. This difference is attributed to small remaining differences in BC barrier height [95]. An additional small difference in $J-V$ characteristics becomes apparent when investigating the region of small bias voltage in detail (inset of Figure 8.5a). The substrate configuration device has less voltage dependent collection than the superstrate configuration device. The dark $J-V$ characteristic (shifted to the normalized $J_{sc}$ value) of the superstrate con-
8.3. Comparison of device configurations

Figure 8.4: a) Depth dependent apparent acceptor concentration as determined by a \(CV\) measurement of a high-efficiency solar cell in substrate configuration. The corresponding measurement of a superstrate configuration device is shown in Figure 7.1a. b) TRPL measurements of high-efficiency solar cells in substrate and superstrate configuration.

The difference in voltage dependent collection is attributed to the better coverage of the CdS layer in substrate configuration devices. Inferior coverage leads to local ZnO/CdTe diodes connected in parallel to the main CdS/CdTe diodes. ZnO/CdTe diodes show more pronounced voltage dependent collection [17]. The CdS double-layer deposition process developed for substrate configuration enables very good coverage, because the second CdS layer is not subjected to a recrystallization treatment. On the other hand the CdS layer in superstrate configuration recrystallizes during the CdCl\(_2\) treatment, which is optimized to suffice several criteria including recrystallization of the CdTe layer and p-n junction formation. Figure 3.1c shows that the optimized process leads to
a small amount of pinhole formation in the CdS layer. Please note, that the difference in voltage dependent collection is not only attributed to the difference in absolute CdS layer thickness. This is confirmed by investigating superstrate configuration solar cells with very thick CdS layer (~250 nm), still showing more pronounced voltage dependent collection than the substrate configuration devices.

Figure 8.5: Normalized $J$-$V$ (a) and EQE (b) characteristics of solar cells in substrate and superstrate configuration.

Figure 8.5b shows EQE measurements of the substrate configuration record and the device “high $V_{oc}$ and FF” from Table 8.1, revealing two differences. The difference in the wavelength region below ~500 nm (indicated by “1”) is caused by the difference in CdS layer thickness. This difference is even more pronounced when using the 15.6% record efficiency superstrate device for comparison (Figure 8.1b), which employs a thinner CdS layer. The difference in CdS layer thickness is the main reason for the different $J_{sc}$ in the two configurations and approaches to reduce CdS layer thickness in substrate configuration without loss in $V_{oc}$ and FF are discussed in Section 4.8. Another difference in EQE is visible in the cut-off wavelength region (indicated by “2”), corresponding to the absorber band-gap, which can be found by plotting $h\nu$ EQE$^2$ against $h\nu$ and extrapolation to the x-axis (inset of Figure 8.5b). A difference of ~0.02 eV is visible. Such a difference is observed for numerous substrate and superstrate configuration devices. For confirmation, EQE measurements of high-efficiency superstrate and substrate configuration devices are added into the inset of Figure 8.5b. The same devices are used as those for the discussion of the voltage dependent carrier collection (inset
8.3. Comparison of device configurations

of Figure 8.5a).

8.3.4 p-n junction formation

In CdTe solar cells the p-n junction is formed by depositing CdS and CdTe layers and annealing the layers in the presence of CdCl$_2$. This generally leads to the formation of a CdS$_x$Te$_{1-x}$ alloy at the interface. The formation of this alloy is often reported to be important for device performance due to reduced structural defects arising from reduced lattice mismatch at the CdS/CdTe interface between the CdS and CdTe layer [21, 55–57]. Substrate configuration solar cells with comparable $V_{oc}$ and FF as in superstrate configuration were produced by the use of the presented process. Therefore, investigation of the p-n junction properties can contribute to the understanding of the role of the CdS$_x$Te$_{1-x}$ alloy.

One of the main differences between substrate and superstrate configuration devices is the degree of sulfur diffusion into the CdTe layer. Sulfur diffusion into the CdTe layer is much more pronounced in superstrate than in substrate configuration. This is consistently observed with EQE (Figure 8.5b) and SIMS measurements (Figure 8.3). It is also confirmed by comparing the APT results presented in Chapter 5 with an APT measurement reported in literature [167]. Also GIXRD measurements revealed no visible CdS$_x$Te$_{1-x}$ formation upon CdS treatment (Chapter 5). Only the modification of the CdTe GBs with sulfur in a region <10 nm from the GBs is observed (Chapter 5). This shows, that very high $V_{oc}$>850 mV and FF>75% are achievable with negligible formation of a tellurium rich CdS$_x$Te$_{1-x}$ alloy. However, the results also show, that in these devices such high $V_{oc}$ and FF are only achievable with relatively thick CdS layer, which limits the $J_{sc}$ in these devices. It is proposed that negligible sulfur diffusion into the CdTe layer and the required CdS layer thickness to achieve high $V_{oc}$ and FF in these devices are correlated and the reason for this is explained in the following.

The formed CdS$_x$Te$_{1-x}$ phase is expected to be n-type, because of the following reasons. CdS is more easily doped n-type than CdTe [33]. Similar to results on other ternary II-VI compounds, this also enhances the n-type dopability of the alloy as compare to pure CdTe [33, 193]. The n-type doping of the CdS$_x$Te$_{1-x}$ alloy can be obtained by native defects (sulfur vacancies) and can be additionally enhanced by the presence of the n-type dopant chlorine in the region of high sulfur content, namely at the
CdTe/CdS interface and the CdTe GBs (cf. Chapter 5). Therefore, a CdS$_x$Te$_{1-x}$ phase present at the CdTe/CdS interface and at the absorber GBs can act as the first part of the n-type side of the p-n junction. In this way, the p-n junction can be formed between CdTe and tellurium rich CdS$_x$Te$_{1-x}$ as also proposed in [194]. This layer is absent (or at least very thin) in the substrate configuration devices and might not allow homogeneous coverage of the CdTe layer. Pinholes in the CdS layer in substrate configuration can therefore lead to local CdTe-ZnO junctions, which have inferior p-n junction properties. Therefore, the formation of a homogeneously covering inverted CdTe surface, e.g. by formation of a CdS$_x$Te$_{1-x}$ alloy could be a promising way to reduce CdS thickness. A similar concept was recently successfully applied in CIGS solar cells [4]. Application of a KF post deposition treatment leads to a copper depleted surface, which enables cadmium to diffuse into the CIGS layer and can lead to an inverted CIGS surface. This enabled reduction of CdS layer thickness. Generation of an inverted CdTe surface is especially well applicable to solar cells in substrate configuration, but should also be possible in superstrate configuration. Possible concepts to obtain an inverted surface are discussed in Section 4.8.

Not only the final sulfur content in the CdTe layer is different in the two configurations, but also the mechanism to obtain sulfur diffusion into the CdTe layer is different. In superstrate configuration devices sulfur diffuses into the CdTe layer due to CdS-CdTe interdiffusion when the layer stack is annealed. In the developed substrate configuration process, the layers are treated separately, which does not lead to significant CdS-CdTe intermixing. Therefore, another mechanism to obtain sulfur diffusion along GBs of the CdTe layer is required and the results shown in Chapter 5 suggest, that sulfur in substrate configuration devices diffuses into the CdTe layer due to elemental exchange with oxygen.

### 8.4 Conclusions and outlook

Efficiencies up to 15.6% and 13.6% are achieved in superstrate and substrate configuration, respectively. Similar high $V_{oc}$ and FF are obtained, which are also comparable to the record efficiency devices. 13.5% certified efficiency is reached in substrate configuration and application of the process on flexible metal foil substrates has resulted in certified efficiencies of 11.5% and 10.9% on molybdenum foil and steel foil substrates,
respectively. Comparable electronic properties are achieved in substrate configuration as in superstrate configuration and similar impurity distributions are obtained. The main differences between substrate and superstrate configurations are a different degree of CdSₙTe₁₋ₓ formation and required CdS thickness to reach high \( V_{oc} \) and FF. The results give indications, that the formation of a tellurium rich CdSₓTe₁₋ₓ alloy in the p-n junction region is beneficial for enabling thinner CdS layer. This give guidance to reduce CdS layer thickness in CdTe solar cells in order to reduce parasitic absorption and improve \( J_{sc} \) of the devices.
Chapter 9

Conclusions and outlook

This thesis investigates low temperature (≤450 °C) grown CdTe solar cells in superstrate and substrate configuration. Extrinsic p-type doping of the CdTe layer with sodium is examined in superstrate configuration solar cells. Due to sodium addition, apparent hole density in the CdTe layer is enhanced to above $10^{15}$ cm$^{-3}$ and grain size of the CdTe layer increases to ~6 µm. In spite of these positive effects, efficiency strongly decreases because the addition of sodium leads to excessive CdS-CdTe interdiffusion. Also when sodium is not intentionally added during the CdTe solar cell growth, it can diffuse from the glass substrate into the solar cell. It is shown, that sodium diffusion from the glass substrate is effectively suppressed by the use of a sufficiently thick and large grained ZnO:Al layer as diffusion barrier. This facilitates 13.5% efficiency (without AR-coating) on low-cost SLG without additional diffusion barrier layer. The use of BSG and a thin CdS layer enable efficiencies up to 15.6%, showing that high efficiencies are achievable with a low temperature process.

A novel process for the growth of CdTe solar cells in substrate configuration is developed which controls impurity distribution in the solar cell and enables certified record efficiencies of 13.5%, 11.5%, and 10.9% on glass, flexible molybdenum foil, and flexible steel foil substrates, respectively. The p-n junction formation in this configuration involves separate CdCl$_2$ treatments of the CdTe and the CdS layer. Subsequent addition of another CdS layer improves $V_{oc}$ and FF, but reduces $J_{sc}$ due to increased parasitic absorption. The CdCl$_2$ treatment of the first CdS layer improves device performance from ~7% to >13% and enhances MCLT in the CdTe layer by an order of magnitude to >2 ns due to passivation of GB and interface defects. The CdS layer recrystallizes, resulting in hexagonal phase and grain size on the order of 100 nm. Chlorine segre-
gates at the CdTe/CdS interface and at GBs in the CdTe layer, and bonding of chlorine to cadmium and tellurium is indicated. The CdCl$_2$ treatment of the CdS layer leads to sulfur diffusion along CdTe GBs and segregation within <10 nm from the GBs without significant formation of a tellurium rich CdS$_x$Te$_{1-x}$ alloy. Sulfur diffusion can occur by an elemental exchange with oxygen. The results suggest that the initial oxygen content in the CdS and CdTe layers can influence impurity diffusion as oxygen can act as exchange partner facilitating diffusion of other impurities into these layers. A novel concept is introduced to dope the CdTe layer in substrate configuration solar cells. After its recrystallization, sub-monolayer amounts of copper are evaporated on the CdTe layer followed by an annealing treatment at 400 °C. The controlled doping leads to hole densities of $\sim 10^{14}$ cm$^{-3}$, reduced valence band energy barrier at the BC/CdTe interface, and significantly enhanced collection of photo-generated charge carriers. The necessity to precisely control the quantity of copper in the CdTe layer of solar cells is explained by the amphoteric behavior of copper impurities in CdTe. The amphoteric behavior can also be a limiting factor to obtaining higher hole density in state-of-the-art CdTe solar cells. Hole densities above $1 \times 10^{16}$ cm$^{-3}$ are achieved in arsenic doped CdTe thin films on glass without copper doping. In spite of these high hole densities, the $V_{oc}$ in the corresponding solar cells could not be improved.

Differences and similarities between substrate and superstrate configuration solar cells are investigated. MCLT of more than 2 ns and apparent hole densities of $\sim 10^{14}$ cm$^{-3}$ are obtained in both configurations, leading to similar $V_{oc}$ and FF. However, substrate configuration devices still have $\sim 2$% lower efficiency than low temperature grown superstrate configuration solar cells, arising from a difference in $J_{sc}$ by $\sim 3$ mA·cm$^{-2}$. The lower $J_{sc}$ in substrate configuration devices is mainly caused by parasitic absorption in the thicker CdS layer. An additional difference between substrate and superstrate configuration devices is the degree of CdS$_x$Te$_{1-x}$ formation which is much more pronounced in superstrate configuration. Furthermore, substrate configuration devices have a stronger rollover, which is attributed to the BC properties, and an improved voltage dependent carrier collection, which is attributed to the CdS layer coverage.

Insights are gained into the role of impurities and the p-n junction formation in CdTe solar cells. Various impurities are involved in the growth of CdTe solar cells, added either intentionally or unintentionally, namely chlorine, oxygen, sulfur, copper, and sodium. Chlorine and sulfur can passivate defects at CdTe GBs and the CdTe/CdS interface. Oxygen can act as an exchange partner for other impurities, in particular to facilitate
sulfur diffusion along GBs of the CdTe layer. The controlled addition of copper enhances hole density, MCLT and reduces the BC energy barrier. Sodium can diffuse from the glass substrate and significantly enhances CdS-CdTe intermixing. In substrate configuration high $V_{oc}$ > 850 mV and FF > 75% are obtained without significant formation of a tellurium rich CdS$_x$Te$_{1-x}$ layer. It is suggested that the formation of this alloy might be important to form a p-n junction between p-type CdTe and n-type tellurium rich CdS$_x$Te$_{1-x}$ in order to significantly reduce CdS layer thickness and to improve $J_{sc}$ of the devices.

The process for the growth of CdTe solar cells in substrate configuration offers new opportunities to overcome technological challenges and to answer scientific questions of CdTe PV. One of the advantages of substrate configuration is the easier accessibility of the p-n junction region, offering advanced opportunities to improve and investigate the CdTe/CdS junction properties. Furthermore, recrystallization and doping of the CdTe layer are decoupled from p-n junction formation, allowing better control of p-type doping of the absorber in the absence of the n-type CdS layer. Another advantage of the possibility to grow high-efficiency solar cells in both configurations is the potential to gain scientific insights into the role of various processing steps, impurities and chemical reactions in CdTe solar cells by comparing results in both configurations.

Future work should focus on the development of substrate configuration CdTe solar cells. The most promising way to enhance efficiency of these solar cells is through the improvement of $J_{sc}$ by reduction of CdS layer thickness. Therefore, reduction of CdS layer thickness while maintaining high $V_{oc}$ and FF should be targeted, for example by formation of a CdS$_x$Te$_{1-x}$ alloy. As explained above, the required thickness of the CdS layer could be related to the insufficient CdS$_x$Te$_{1-x}$ formation at the CdTe/CdS interface. For example, the use of co-evaporated CdS$_x$Te$_{1-x}$ close to the CdTe surface could be tested. Considering the suggested role of oxygen acting as an exchange partner with sulfur, enhanced oxygenation of the CdTe layer followed by sulfur diffusion could be tried. Furthermore, sodium could be applied to enhance CdS-CdTe interdiffusion. An alternative option could be the generation of an inverted n-type surface of the CdTe layer by indium or aluminium doping. If CdS layer thickness is successfully reduced and $J_{sc}$ of 24 or 26 mA·cm$^{-2}$ without loss in $V_{oc}$ and FF would be possible, substrate configuration solar cells with ~15 or ~16% efficiency could be obtained, respectively. Another way to enhance $J_{sc}$ could be the application of alternative window layers with a larger band gap. Further efforts could focus on the improvement of FF to ~80%. To achieve this,
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series resistance has to be reduced, possibly by replacement of the MoO₃ based BC material with other materials. The efficiency gap between substrate configuration solar cells on different substrates should be closed. To achieve this, processing temperatures during the growth on metal foil should be adapted and improved diffusion barrier layers should be developed. Furthermore, the process can be applied to other substrates, such as flexible aluminum foil or polyimide film.

Additional work could focus on the improvement of \( V_{oc} \). Considering that all record efficiency CdTe solar cells of the last 20 years exhibit \( V_{oc} \) of ~850 mV this could be a challenging task. However, the recently achieved \( V_{oc} \) above 900 mV (even though with limited \( J_{sc} \) and FF) shows that the \( V_{oc} \) of CdTe solar cells is not fundamentally limited at ~850 mV [7]. It is proposed that to increase \( V_{oc} \) towards 1 V, CdTe solar cell research has to go several steps back and replace some of the impurities with others having similar effects. The use of chlorine, copper, sulfur, and oxygen impurities has enabled the successful story of CdTe PV. However, the use of some of these impurities could also limit the performance to present values. It is difficult to state, which of these impurities has to be replaced, and which way could finally lead to an enhanced \( V_{oc} \), but four possible routes are presented in the following and the requirements on process adaptation are shortly discussed.

1. The amphoteric behaviour of copper could limit the hole density in CdTe PV to present values, and therefore its replacement with other p-type dopants like arsenic should be tried. However, copper also influences the BC and can contribute to GB passivation. Therefore, replacement of copper with arsenic might simultaneously require the use of other BC materials, and the adaptation of the CdCl₂ treatment conditions.

2. There are reports that chlorine limits the performance by the formation of deep defects in the CdTe layer [195,196]. Replacement of chlorine requires another approach to passivate GBs, and a TRPL study of CdTe/CdS layer stacks doped with different impurities or prepared under different conditions could identify suitable alternatives. At the same time, the possible role of chlorine as an n-type dopant in the surface and GB region of the CdTe layer might have to be replaced by another n-dopant like indium. Furthermore, in low temperature grown CdTe solar cells another way has to be found to enable recrystallization of the CdTe layer.

3. The formation of a CdTe p-n homojunction can be targeted, which could lead to a higher \( J_{sc} \) and \( V_{oc} \). A p-n homojunction could, for example, be obtained by doping of
the CdTe layer with copper to form a p-doped layer and subsequent inversion of the top part of the CdTe layer by in-diffusion of indium. Omitting the CdS layer requires other ways to passivate the CdTe surface and GBs, possibly by the use of other sulfur containing chemicals. The effectiveness of those can also be investigated by a TRPL study.

4. Approach 1 and 3 could be combined: A homojunction is formed, where the CdTe layer is p-doped with arsenic and the top part of the CdTe layer is inverted with indium. This might require all the adaptations listed in approach 1 and 3.

Each of these suggested routes requires extensive development work. Considering that the $V_{oc}$ limitation in record efficiency devices has already existed for many years it is likely that several steps in CdTe solar cell processing have to be simultaneously adapted, because many of the straightforward approaches were probably already tested.
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Abbreviations

AR  Anti-reflection
APT  Atom probe tomography
AS  Admittance spectroscopy
BC  Back contact
BSG  Borosilicate glass
CBD  Chemical bath deposition
CIGS  Cu(In,Ga)Se$_2$
$C$-$V$  Capacitance-voltage
CSS  Close space sublimation
CZTS  Cu$_2$ZnSn(S,Se)$_4$
$E_B$  Binding energy
EBIC  Electron beam induced current
EDX  Energy dispersive X-ray spectroscopy
$\eta$  Efficiency
EQE  External quantum efficiency
FC  Front contact
FF  Fill factor
FTO  Fluorine doped SnO$_2$
FWHM  Full width at half maximum
GB  Grain boundary
GIXRD  Grazing incidence X-ray diffraction
HRT  Highly resistive and transparent
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>HVE</td>
<td>High vacuum evaporation</td>
</tr>
<tr>
<td>ICPMS</td>
<td>Inductively coupled plasma mass spectroscopy</td>
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<tr>
<td>ITO</td>
<td>tin doped indium oxide</td>
</tr>
<tr>
<td>i-ZnO</td>
<td>Intrinsic ZnO</td>
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<tr>
<td>$J$-$V$</td>
<td>Current density - voltage</td>
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<tr>
<td>$J_{sc}$</td>
<td>Short circuit current density</td>
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<tr>
<td>MCLT</td>
<td>Minority carrier lifetime</td>
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<tr>
<td>PL</td>
<td>Photoluminescence</td>
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<tr>
<td>PV</td>
<td>Photovoltaic</td>
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<tr>
<td>SCR</td>
<td>Space charge region</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning electron microscopy</td>
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<tr>
<td>SIMS</td>
<td>Secondary ion mass spectroscopy</td>
</tr>
<tr>
<td>SLG</td>
<td>Soda-lime glass (float glass)</td>
</tr>
<tr>
<td>STEM</td>
<td>Scanning transmission electron microscopy</td>
</tr>
<tr>
<td>TCO</td>
<td>Transparent conductive oxide</td>
</tr>
<tr>
<td>TRPL</td>
<td>Time resolved photoluminescence</td>
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<tr>
<td>$V_{oc}$</td>
<td>Open circuit voltage</td>
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<tr>
<td>$W_p$</td>
<td>Watt-peak</td>
</tr>
<tr>
<td>XPS</td>
<td>X-ray photoelectron spectroscopy</td>
</tr>
<tr>
<td>XRD</td>
<td>X-ray diffraction</td>
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**Book chapter**


**Patent application**