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# High-Power DC-DC Converter Technologies for Smart Grid and Traction Applications

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*A mis padres  
Julieta y Fernando.*



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# Abstract

Electric transformers, either utilized in electric power systems or within a power electronics-based converter, are fundamental components of modern highly-efficient energy supply chains, as they provide the voltage adaptation between networks with different voltage levels. In traction applications for example, the power for the drive system is provided through a single-phase Medium Voltage (MV) catenary line, whereas the traction machine is fed by a Low Voltage (LV) three-phase inverter. It is therefore necessary to step this MV down to the required LV level through a Low Frequency (LF) transformer which needs to be carried by the driving locomotive. Since the performance of these traction solutions is tightly linked to the weight of the energy supply system, which is to a large extent determined by the step-down and isolation transformer, lower weight energy supply concepts for modern traction solutions are highly desirable and cannot be fulfilled by classical concepts.

In electric power systems, transformers also perform the fundamental task of adapting the voltage between the generation, transmission and distribution levels. In modern electric power systems, high flexibility in power delivery is becoming mandatory, as new types of sources, e.g. renewable energy generators, and dynamic loads are integrated into the power grid. Given the dynamic behavior of these sources/loads, a smart energy routing concept, i.e. a Smart Grid, which ensures a stable and reliable operation of the network is required. This task of fast and active response to variations in the grid conditions cannot be met by standard LF transformers, as they are intrinsically passive components.

These limiting factors for future traction solutions and Smart Grid implementation can be overcome by integrating more controllable components within these supply chains. In the case of traction applications, this would mean the integration of the isolation stage within the converter system in order to enable the operation of this component at higher frequencies, and therefore a reduction in its weight. Considering Smart Grids energy routing solutions, the main requirement is the flexibility in power delivery, which results in the partial or total processing

of the transformer's power by controllable active devices, i.e. power semiconductor switches, in order to actively adapt the operating point of the transformer to the grid conditions. The integration of power semiconductor switches together with an isolation transformer is often referred to as Solid-State Transformer (SST), where numerous options for the realization of this component have been considered. A three-stage approach comprising an active front-end rectifier, a high-power DC-DC conversion stage performing the isolation and voltage adaptation at higher frequencies and finally a load-end inverter represents the most attractive solution given its modularity and low coupling between the different power conversion stages. Within this three-stage SST concept, the key component is the high-power DC-DC conversion stage, as it is now responsible for the isolation and voltage adaptation at higher frequency levels.

This thesis deals with the conception and design of one cell of such DC-DC converter stage (2 kV/400 V, 166 kW, 20 kHz). The first topic to be addressed is the requirement of soft-switching modulation and the respective DC-DC converter topologies which enable this type of switching transitions. Furthermore, the performance of the semiconductor switches on the MV side of the DC-DC converter under these soft-switching modulation schemes is experimentally analysed, whereby models for the analytical estimation of the switching losses are presented. Moreover, on the LV side of the converter, alternative bridge arrangements comprising combinations of MOSFET and IGBT switches in order to maximize the efficiency of the system are considered. The optimized design of the key component within the DC-DC converter, the Medium Frequency (MF) transformer, is presented for two types of transformers with different core materials and cooling concepts, where the trade-offs between these two types are clearly visualized. For each of these parts of the DC-DC converter, i.e. the MV side bridge, the LV side bridge and the MF transformer, a detailed description of the constructed prototypes' mechanical arrangement is presented at the end of the respective chapters.

In order to test the designed systems, a back-to-back arrangement was constructed based on two fully-rated bidirectional DC-DC converters. With this setup, the testing of the system within standard laboratory conditions can be achieved, obtaining experimental data and verification of the proposed converter design.



# Kurzfassung

Transformatoren sind wichtige elektrische Komponenten, die für den Einsatz in elektrischen Verteilnetzen oder in leistungselektronischen Konvertern unerlässlich sind, da sie als Bindeglieder zwischen Netzen verschiedener Spannungslevel agieren.

Beispielsweise in Antriebssystemen hoher Leistung muss der Transformator die hohe Speisespannung, die vom Netz zur Verfügung gestellt wird, auf ein niedrigeres Spannungsniveau heruntersetzen um die Maschine versorgen zu können. Bei Traktionsanwendungen spielt das Gewicht des Antriebs eine wichtige Rolle und da dieses Gewicht zu einem grossen Teil vom Transformator bestimmt wird, ist es notwendig, Möglichkeiten zu entwickeln, die eine leichte und kleine Baugrösse des Transformators erlauben.

Auch in elektrischen Verteilnetzen erfüllen Transformatoren den Zweck, die Spannungen von Netzen verschiedener Spannungsniveaus anzupassen. Moderne leistungselektronische Systeme erfordern einen hohen Grad an Flexibilität, um der sich ständig ändernden Nachfrage nach Blind- und Wirkleistung nachzukommen, insbesondere weil die Anzahl neuer Energiequellen im Netz, z.B. regenerativer Energieerzeuger, zunimmt. Das elektrische Verteilnetz, das dadurch ein sehr dynamisches Verhalten aufweist, benötigt daher ein intelligentes Konzept, vielfach als Smart Grid bezeichnet, um einen stabilen und zuverlässigen Betrieb zu garantieren. Diese Aufgabe kann mit niederfrequenten (50Hz) Transformatoren nicht gewährleistet werden, da diese Komponenten rein passiv sind. Eine hohe Dynamik kann für diese Systeme dadurch erreicht werden, dass steuerbare (aktive) Komponenten verwendet werden. Für Antriebssysteme bedeutet dies, dass die Transformation der Spannung mittels eines leistungselektronischen Konverters vorgenommen wird, was eine höhere Betriebsfrequenz und dadurch ein geringeres Gewicht des Transformators erlaubt. Auch die hohe geforderte Dynamik des Leistungsflusses in Smart Grids kann durch einen leistungselektronischen Konverter erreicht werden, der den benötigten Blind- und Wirkleistungsbedarf des Netzes über den Transformator durch aktives Schalten steuert. Die Kombination aus aktiven

Schaltern mit einem isolierenden Transformator wird oft als Solid-State Transformator bezeichnet, für den es mehrere Realisierungsmöglichkeiten gibt. Ein dreistufiges System, bestehend aus aktivem eingangsseitigem Gleichrichter, einem DC-DC Konverter und einem ausgangsseitigen Wechselrichter, erlaubt einen hohen Grad an Modularität und stellt eine geringe Kopplung zwischen den einzelnen Stufen sicher. Der DC-DC Wandler erfüllt dabei die Aufgabe der galvanische Trennung und der Spannungsübersetzung bei hoher Schaltfrequenz, was eine kleine Baugröße des Transformators erlaubt.

Diese Arbeit beschreibt den analytischen Entwurf, den Aufbau und die experimentelle Verifikation eines Moduls des für die beschriebenen Anwendungen essentiell wichtigen DC-DC Konverters (2kV/400V, 166kW, 20kHz). Als erstes werden mehrere Topologien und Modulationsverfahren der aktiven Schalter beschrieben, die ein weiches, d.h. verlustarmes Schalten der Leistungshalbleiter ermöglichen. Die analytischen Modelle werden dabei experimentell auf der Mittelspannungsseite des Konverters validiert. Auf der Niederspannungsseite des Konverters werden mehrere Realisierungsmöglichkeiten bestehend aus Kombinationen von IGBTs und MOSFETs vorgestellt, implementiert und messtechnisch miteinander verglichen.

Für den Transformator, der das Herzstück des Konverters darstellt, werden zwei Realisierungen, die sich hinsichtlich der Materialien und Kühlkonzepte unterscheiden, gezeigt und deren Eigenschaften einander gegenübergestellt.

Der mechanische Aufbau der Niederspannungsseite, des mittelfrequenten Transformators und der Mittelspannungsseite, wird detailliert zum Schluss der jeweiligen Kapitel beschrieben. Für die messtechnische Validierung des Gesamtsystems werden zwei Konvertersysteme antiparallel geschaltet um eine Zirkulation des Leistungsflusses zu ermöglichen. Dies erlaubt den Nennleistungsbetrieb des Konverters unter Laborbedingungen und damit die experimentelle Verifikation der theoretisch ermittelten Konvertermodelle.

# Abbreviations

2D	...	Two Dimensional
3D	...	Three Dimensional
AC	...	Alternating Current
ADC	...	Analog to Digital Converter
DAB	...	Dual Active Bridge
DC	...	Direct Current
DUT	...	Device Under Test
DSP	...	Digital Signal Processor
CAD	...	Computer Aided Design
FEM	...	Finite Element Method
FS	...	Field Stop
FPGA	...	Field Programmable Gate Array
HC-DCM-SRC	...	Half-Cycle Discontinuous Conduction Mode Series Resonant Converter
IC	...	Integrated Circuit
IGBT	...	Insulated Gate Bipolar Transistor
ISOP	...	Input Series Output Parallel
MAF	...	Moving Average Filter
MF	...	Medium Frequency
MOSFET	...	Metal Oxide Field Effect Transistor
MV	...	Medium Voltage
NPC	...	Neutral Point Clamped
NPT	...	Non Punch Through
LF	...	Low Frequency
LV	...	Low Voltage
PCB	...	Printed Circuit Board
PWM	...	Pulse Width Modulation
QZCS	...	Quasi Zero-Current Switching
RMS	...	Root Mean Square
SRC	...	Series Resonant Converter

SOC	...	Start of Conversion
SST	...	Solid-State Transformer
TCM	...	Triangular Current Mode
TCM-DAB	...	Triangular Current Mode Dual Active Bridge
ZCS	...	Zero-Current Switching
ZVS	...	Zero-Voltage Switching

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# 1

## Introduction

Standard LF transformers represent the core component around which our current electric power systems are built. They enable the selection of appropriate voltage levels for each stage of the electric power delivery chain, starting from MV at the generation stage, high voltage transmission, back to MV for distribution and finally LV in order to be safely used by the end consumers. These transformers are properly matched to the traditional electric power system, where a central generation together with an exclusively unidirectional power flow are among the main characteristics.

In modern electric power systems, as envisioned by the Smart Grid concept [1, 2], the integration of renewable energy generation is a key element not only at large scales as in the case of on- and off-shore wind generation for example, but also at the consumer end, where the recent improvements, cost reductions and attractive policies have made the installation of photovoltaic solutions interesting. The integration of these now highly distributed energy generation systems into the grid introduces new challenges concerning the control of the power flow and ultimately for the stability of the network, since renewable energy sources have an intrinsically high dynamic behavior which is tightly linked to unforeseeable weather conditions. These new challenges in control of power delivery are no longer fulfilled by standard LF transformers, since no means for actively controlling the power flow are provided by these components.

Moreover, the fixed operating frequency of our current electric power systems restricts the degrees of freedom available for the optimization of the required isolation transformers. In cases where tight volume/weight budgets are found, such as for rolling stock applications, this fixed and

low operating frequency leads to heavy, large-sized and low-efficient designs. In order to improve the performance of these traction solutions, a concept with a higher operating frequency isolation transformer is highly desirable.

In order to propose and analyse the possible concepts for next generation traction energy supply chains and future Smart Grid flexible energy routing solutions, first the basics of classical transformers will be discussed where the main challenges in the state-of-the-art technology will be highlighted. Furthermore, previously proposed solutions for Smart Grid and traction applications will be comprehensively reviewed and classified, leading to the selection of the specifications of the converter described in this thesis.

## 1.1 Transformer Basics

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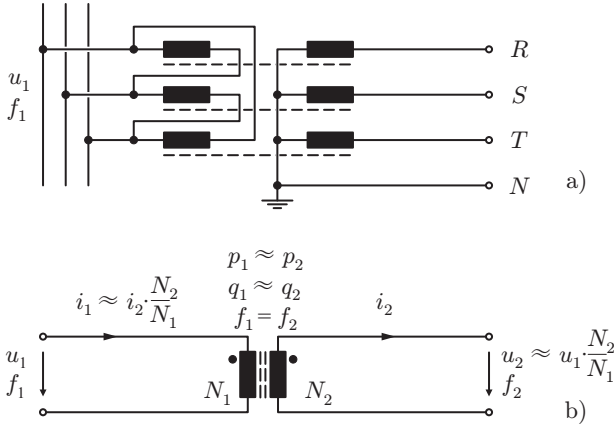
Classical transformers are constructed with iron-based core materials such as silicon steel. Around these cores, a primary winding and a secondary winding are wound with a certain number of turns<sup>1</sup>. These windings are constructed with highly conductive metals, typically copper or aluminum. To complete the construction, an insulation material is utilized which ensures safe galvanic isolation between these two windings, which is for this type of transformers either mineral oil or a dry-type resin. This isolation layer also serves as cooling medium in order to extract the losses generated by the operation of the core and winding [3].

The operating frequencies of these classical transformers is 50/60 Hz for power distribution applications and also for a number of traction electrification lines [4]. Due to historical reasons related to the available electrical machine technology at the times these railway networks were constructed, a lower operating frequency of  $16\frac{2}{3}$  Hz is found in traction railways systems of Germany, Switzerland, Austria, Sweden and Norway [4]. These transformers, employed either in distribution or traction systems, connect an MV grid which ranges typically from 10 to 25 kV to a LV grid with voltages lower than a kilovolt [2].

A typical representation of a three-phase (distribution) transformer is shown Fig. 1.1-a), whereby a delta connection is found at the primary (MV) side and a star connection is utilized at the secondary (LV)

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<sup>1</sup>Historically the primary winding has been related to the higher-voltage winding while the lower-voltage winding is related to the secondary side of the transformer.



**Figure 1.1:** Transformer basics: a) Three-phase transformer representation with delta connection on primary side and star connection on secondary side. b) Ideal single-phase transformer circuit utilized to visualize the key features of a classical transformer.

side. Assuming individual magnetic cores, each of the phases of this transformer can be analysed with its single-phase equivalent circuit as presented in Fig. 1.1-b). Here, the main features of a classical transformer can be identified:

- Ideally fixed voltage transfer ratio given by

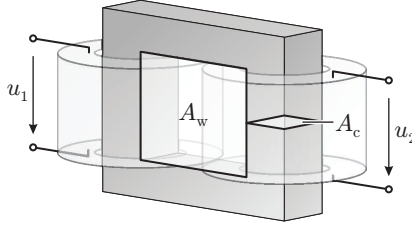
$$u_2 = u_1 \cdot \frac{N_2}{N_1}. \quad (1.1)$$

In a more realistic case, this transfer ratio is influenced by the transformer's leakage inductance and by the operating point of the transformer.

- Ideally fixed current transfer ratio given by

$$i_1 = i_2 \cdot \frac{N_2}{N_1}. \quad (1.2)$$

This transfer ratio is influenced mainly by the magnetizing inductance of the transformer and can be assumed approximately constant for most transformer designs.



**Figure 1.2:** Definition of core cross-section  $A_c$  and winding window area  $A_w$  used to study the scaling laws present in transformer design.

- Fixed active power transfer: Assuming no losses in the transformer, the active power sourced to the primary winding is equal to the power delivered to the secondary winding, i.e.

$$p_2 = p_1. \quad (1.3)$$

- Fixed reactive power transfer: Neglecting leakage and magnetizing effects, the reactive power delivered to the primary winding will be transferred equally to the secondary, leading to:

$$Q_2 = Q_1. \quad (1.4)$$

- Equal primary and secondary operating frequencies:

$$f_2 = f_1. \quad (1.5)$$

Based on the electrical specifications of the transformer, the required core cross-section  $A_c$  and winding window area  $A_w$  as defined in Fig. 1.2 are found [3],

$$A_c = \frac{1}{\sqrt{2}\pi} \frac{U_1}{f \cdot B_{\max}} \frac{1}{N_1} \quad (1.6)$$

$$A_w = \frac{2I_1}{k_w J_{\text{rms,max}}} N_1, \quad (1.7)$$

whereby  $B_{\max}$  is the maximum magnetic flux density in the core,  $f$  is the operating frequency,  $k_w$  is the winding window's filling factor,

greatly affected by the amount of required insulation, and  $J_{\text{rms,max}}$  is the maximum allowed current density in the transformer winding, defined by the windings' cooling system heat extraction capabilities.

Among the main advantages of classical transformers are their relatively low costs due to the simple construction, highly reliable and robust operation, with a lifetime in the tens of years' range and high efficiencies usually higher than 98 % for distribution transformers.

Due to their passive nature, however, several weaknesses of classical transformers can be pointed out such as voltage drop under load conditions, no load losses due to continuous AC magnetization of their iron core, sensitivity to harmonics and disturbances in the grid or load sides, sensitivity to DC components present in the exciting voltages which can cause saturation of the magnetic core and no intrinsic protection against overload or over-currents. In addition, fire danger and environmental concerns due to the utilization of high amounts of insulating oil are becoming important matters.

A final aspect to be analysed is the achievable size of these transformers, which is related to the previously defined core cross-section and winding window area in the form of the area product

$$A_c \cdot A_w = \frac{\sqrt{2}}{\pi} \frac{P_T}{fk_w J_{\text{rms,max}} B_{\text{max}}}, \quad (1.8)$$

where  $P_T$  is the transformer's nominal power.

From (1.8) it can be seen that the area product is proportional to the power  $P_T$  processed by the transformer and inversely proportional to the operating frequency  $f$ . Moreover, it can be seen that the material properties, namely the filling factor  $k_w$ , the maximum current density  $J_{\text{rms,max}}$  and the maximum flux density  $B_{\text{max}}$  are also inversely proportional to the transformer's area product, meaning that an increase in any of these parameters would result in a decrease of the transformer volume and therefore in a more compact design.

With a selected set of material properties, i.e. fixed filling factor  $k_w$ , maximum current density  $J_{\text{rms,max}}$  and maximum flux density  $B_{\text{max}}$ , the frequency is the main determining factor for the size of the transformer for a given power level. In case of distribution and traction transformers, the low aforementioned frequencies lead to large and heavy transformer designs. The possibilities for reduction in size of the transformer are then given only by the previously discussed material properties.

A flexible selection of the transformer's operating frequency cannot

be achieved in classical distribution/traction transformers given their direct connection to electrical networks with tight operating parameters. It is therefore necessary to integrate the transformer stage within an electric circuit capable of increasing the fixed operating frequency given by the electrical network. The electric circuits capable of providing this functionality are based on actively controlled power electronic semiconductor devices arranged in bridge configurations.

Moreover, by utilizing power semiconductor devices in order to link two electrical networks, a large number of functionalities can be gained with respect to traditional transformers, such as active secondary voltage control, active input current control, reactive power compensation and over-voltage and over-current protection, among others.

The utilization of a combination of power semiconductor devices for linking two electrical networks which integrate a transformer operated at higher frequencies is referred to as *Solid-State Transformer* (SST) [5]. A historical background of the SST development for traction applications is provided in Appendix A.

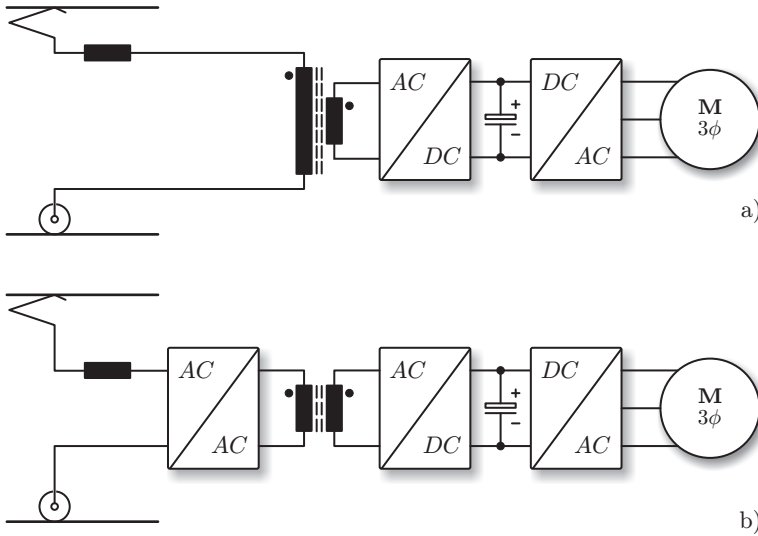
The aim of this thesis is to conceptualize, design and experimentally test a DC-DC converter cell of a fully-rated SST, whereby the proper selection of the specifications and the topology of this SST will be decided upon the review of SST applications in traction and Smart Grids. This review will be performed in the following sections.

## 1.2 Traction Applications

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The power required by locomotives utilized in traction applications is fed by overhead catenary lines, which, due to the long distances, are typically operated in the MV range, e.g. at 15 kV or 25 kV in Europe [4]. Additionally, due to historical technological limitations, the operating frequency is very often as low as  $16\frac{2}{3}$  Hz and 50 Hz in other cases. On the other hand, the power taken from this catenary line needs to be transferred to the electric machines driving the locomotive. These machines are typically of LV type ( $< 1$  kV), meaning that, in order to be supplied from the MV catenary line, the voltage fed to the LV machines needs to be stepped down by a transformer.

In Fig. 1.3-a), the classical approach for voltage step-down in locomotives is presented. It comprises a front-end LF transformer connected on its secondary side to an active rectifier. This rectifier performs the power factor correction of the input current and regulates the DC-link



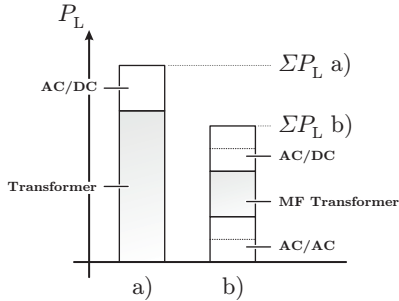
**Figure 1.3:** Electrical energy supply chain for locomotives in traction applications: a) Traditional LF front-end voltage step-down and isolation solution with active rectifier. b) Solution incorporating SST technology with integrated MF voltage adaption and isolation.

voltage to the value required by the inverter stage, which finally supplies the locomotive's machine.

In this scheme, given the operation of the isolation transformer with LF, low transformer power densities are achieved, resulting in bulky and heavy solutions with power density values in the 2 to 4 kg/kVA range [6]. This low power density and hence heavy weight is detrimental to the performance of the traction system, since weight is typically minimized in any traction solution.

Moreover, in an effort to increase the system's power density, the transformers are designed to operate at high current and flux density levels, thus increasing its losses and consequently reducing the traction system's efficiency, which can reach values in the 90 to 95 % range [6].

In order to overcome the aforementioned limitations of traditional traction solutions, the next generation locomotive scheme, as presented in Fig. 1.3-b), has been proposed. The key modification with respect to the traditional approach is the integration of the isolation stage within



**Figure 1.4:** Share of losses in the energy supply chain for the traditional (cf. Fig. 1.3-a)) and SST-based (cf. Fig. 1.3-b)) traction solutions.

the conversion chain, i.e. building an SST. In order to achieve this, the MV catenary line is directly connected to a power electronics-based front-end AC-AC converter. This AC-AC stage converts the LV AC voltage on the MV AC side to a MF AC voltage which is used to feed a transformer. Given the operation at higher frequencies, the size and consequently the weight of the isolation stage can be considerably reduced as explained in the previous section. Additionally, given the freedom in the selection of the MF transformer's operating frequency, the input AC-AC stage and the transformer can be optimized in order to meet with specific weight/efficiency requirements, thus additionally enabling an increase in the system's efficiency with respect to the standard approach (cf. Fig. 1.3-a)).

Fig. 1.4 qualitatively shows the share of losses of the two presented traction supply chain concepts. In the standard approach (cf. Fig. 1.4-a)), the losses are composed of the transformer and the rectifier losses<sup>2</sup>. A big portion of these losses are found in the step-down transformer due to its comparatively low efficiency, while the rectifier stage contributes with a smaller portion to the overall losses.

The potentially reached losses in the SST-based solution are presented in Fig. 1.4-b). As mentioned earlier, a reduction in losses in the transformer can be achieved given the possibility for optimization through the selection of the operating frequency. This reduction overcomes the additional losses introduced by the input AC-AC stage, thus

<sup>2</sup>The losses in the inverter stage driving the machine are not considered since they are equal for both solutions.



resulting in an overall more efficient and lighter solution.

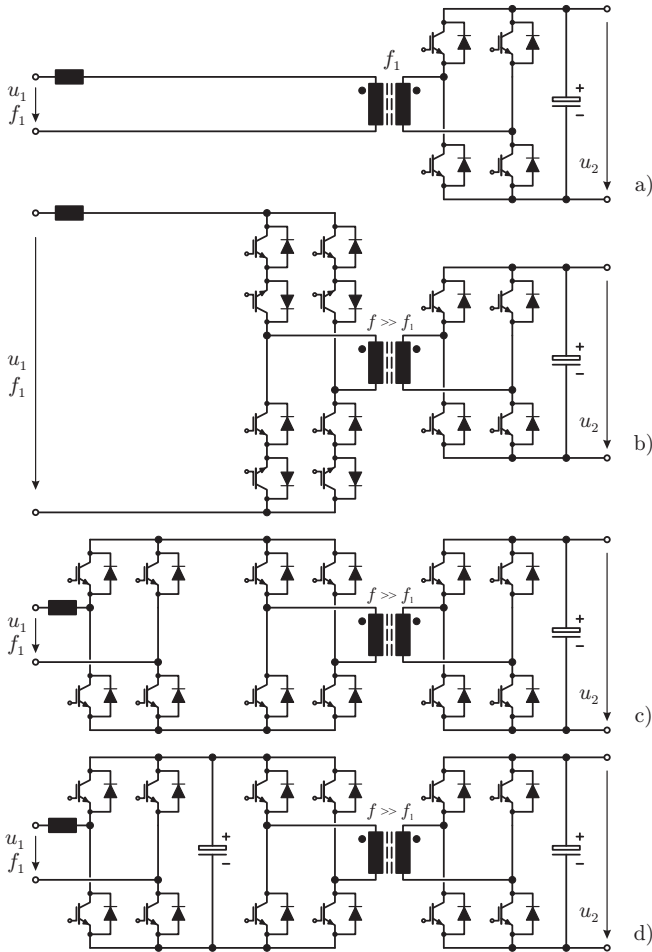
A detailed schematic view (the partitioning of the high input voltage to several series connected converter cells is not considered) of the standard and next generation locomotive solutions is shown in Fig. 1.5. The standard solution presented in Fig. 1.5-a) comprises a LF transformer fed from the catenary line with voltage  $u_1$  and frequency  $f_1$ . The active rectifier connected on the secondary side of the transformer performs the power factor correction at the input side while providing a regulated LV DC output voltage. This robust and reliable solution has been extensively used and represents the classic traction energy supply scheme [4].

In Fig. 1.5-b), the input voltage  $u_1$  is fed to a direct matrix-type converter, comprising bidirectional semiconductor devices, which transforms the LF input voltage into an MF voltage which is fed to the isolation transformer. On the secondary side of the transformer, a rectifier operated at MF provides the regulated DC-link voltage  $u_2$ . It should be noted that this approach performs the conversion of LF to MF in a single-stage and has been reported in literature previously [7–11].

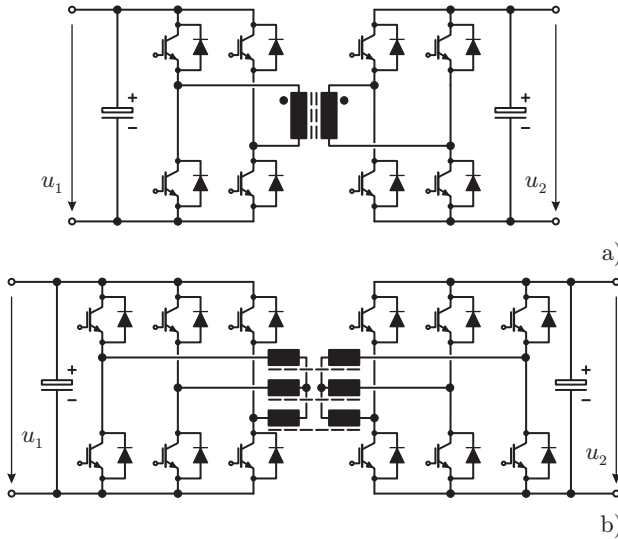
The indirect version of the matrix-based approach shown in Fig. 1.5-b) is presented in Fig. 1.5-c). Here, the input rectifier performs a synchronous rectification, providing a positive voltage to the full-bridge driving the MF transformer. This concept strictly adds one conversion stage to the supply chain but avoids the utilization of a DC-link capacitor on the MV side.

The fully indirect conversion chain comprising a MV DC-link is presented in Fig. 1.5-d). In this case, the input rectifier provides an ideally constant voltage to the full-bridge driving the MF transformer. With this solution, a better utilization of the transformer is reached, since a square-shaped voltage is always supplied to the windings, thus reaching at every switching cycle the nominal values of current and flux density. The price is the addition of the MV side DC-link capacitor which compromises the converter's power density. Nevertheless, the inherently modular construction achieved with this approach proved attractive for several implementations [12–16], whereby the solution presented in [17] has been commissioned for the Swiss Federal Railway system.

The DC-DC stage shown in Fig. 1.5-d) can be built with a single-phase transformer as shown in Fig. 1.6-a) or with a three-phase converter, as presented in Fig. 1.6-b). This last case may result attractive in order to reduce the size of passive components such as the DC-link



**Figure 1.5:** Energy supply chains for traction applications: a) Traditional LF front-end isolation and voltage step-down with active rectifier on LV side; b) Integrated MF isolation with matrix-type front-end AC-AC converter; c) Integrated MF isolation with synchronous rectifier front-end and time varying MV DC-link voltage; d) Integrated MF isolation with PWM rectifier front-end and MV DC-link.



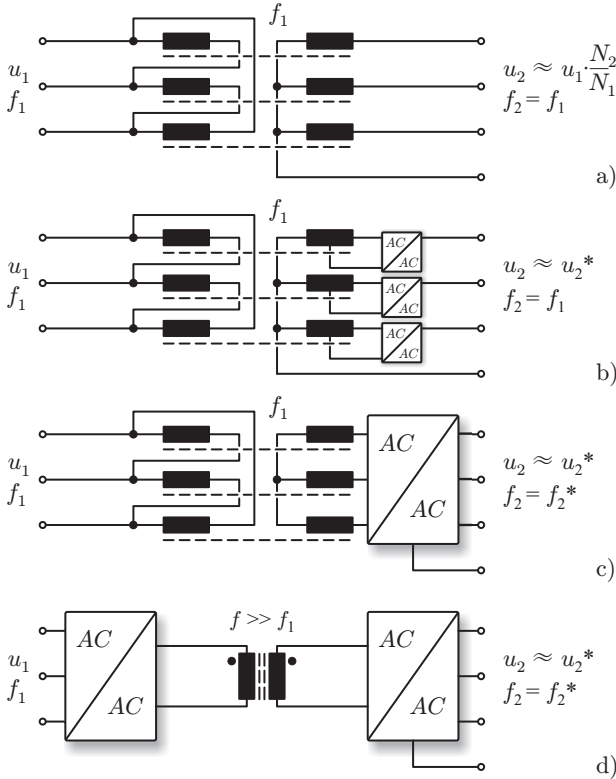
**Figure 1.6:** Possible implementations of the DC-DC converter stage: a) Single-phase Dual Active Bridge (DAB); b) Three-phase DAB.

capacitors. However, a comparison of the single- and three-phase approaches has not been presented previously in literature for traction solutions.

It should be noted that in the solutions presented in Fig. 1.5 which comprise an MF AC-link, the main challenges are now placed on the construction and optimization of the MF transformer and its driving power electronic bridges. Consequently, the trade-offs in the design and synthesis of these components represents the main research challenge in the case of SSTs for traction solutions.

## 1.3 Smart Grid Applications

As mentioned earlier, a transformer which can provide the flexibility in power delivery, namely secondary side voltage control, primary side power-factor correction/reactive power compensation and short circuit current protection, is required for the implementation of future Smart Grids [1, 2]. In order to achieve this flexible and dynamic behavior in the



**Figure 1.7:** Standard and Smart Grid oriented transformers: a) Standard three-phase LF transformer; b) LF transformer with secondary side voltage regulation provided by partial power converters; c) LF transformer with secondary side voltage regulation provided by full-power AC-AC converter; d) Integration of the isolation stage within a fully-rated SST.

transformer’s operation, at least a portion of the power flow through the transformer needs to be processed by actively controlled components, i.e. by power semiconductor devices. Fig. 1.7 shows the possible concepts which enhance the operation of the traditional transformer with additional features.

In order to clearly visualize the achievable functionality and performance of the different possible concepts, Fig. 1.7-a) shows the standard

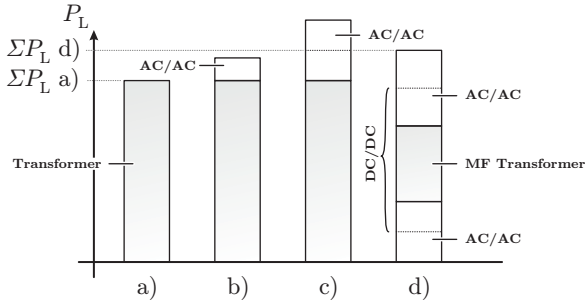
three-phase, primary delta, secondary star-connected transformer. This transformer, as mentioned above, is characterized by a secondary voltage tightly linked to the primary voltage ( $u_2 = u_1 \frac{N_2}{N_1}$ ), equal primary and secondary side frequencies,  $f_2 = f_1$ , no active short circuit protection features and comparatively large size due to the low operating frequency. In contrast, the solution presented in Fig. 1.7-b) provides controllability in the output voltage  $u_2$  by including power electronic AC-AC converters at the secondary side, which process a portion of the power transferred by the LF transformer. Possible implementations of these fractional-power converters are presented in Appendix B.

If controllability over the whole voltage range and independence between the primary and secondary frequencies is required, the solution presented in Fig. 1.7-c) can be utilized. Here, a full-scale AC-AC converter is placed at the secondary side of the transformer, achieving full controllability of the output voltage while being able to actively shape the input currents in order to meet the grid's reactive power requirements. This solution however, relies on a standard LF transformer for isolation and voltage step-down purposes.

In addition to flexibility in power delivery, a reduction in size/weight may be advantageous in applications with tight volume/weight budgets. This reduction is achieved by introducing an additional degree of freedom in the transformer's design: the operating frequency. As previously stated, given that electric power systems are characterized by a fixed operating frequency, the means to achieve this freedom in the transformer's frequency selection is the integration of the transformer with active power electronic bridges, i.e. building an SST solution. This described scheme is presented in Fig. 1.7-d). Here, an AC-AC converter is fed by the MV AC grid, converting this LF voltage into an MF voltage which excites the transformer. On the secondary side, a second AC-AC converter is utilized to convert the MF waveforms back into LF three-phase voltages to be fed to the load.

The operation at higher frequencies is translated into a reduction in size/weight of the transformer, whereby the freedom in the selection of the operating frequency enables the optimization of the transformer design for a specific target. In this case however, two fully-rated AC-AC converters are responsible for the processing of the full transformer power, thus a highly efficient operation of these components becomes mandatory.

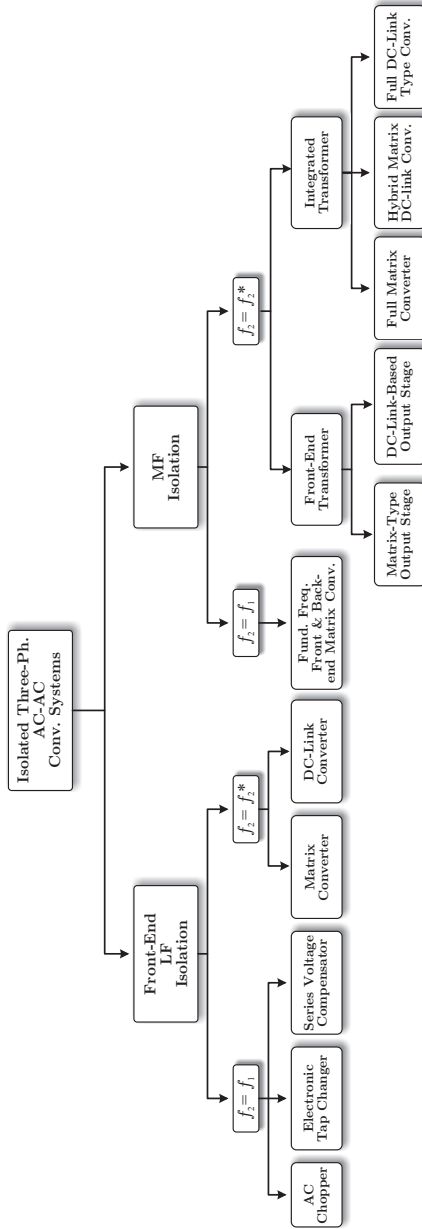
In order to qualitatively analyze the trade-offs in the inclusion of



**Figure 1.8:** Loss distribution in the different stages of the concepts shown in Fig. 1.7.

active power electronic circuits to the transformer, Fig. 1.8 shows the contribution of losses of each component for all transformer options presented in Fig. 1.7. In the standard solution, only the LF transformer losses are encountered, which for distribution transformers typically represents 1 to 2% of the transformer's transferred power, i.e. an efficiency of 98 to 99% [3]. If the partial power solution presented in Fig. 1.7-b) is implemented, the losses of the AC-AC conversion stage are added to the transformer losses, as represented in Fig. 1.8-b). With a full-scale AC-AC converter interfaced to the MV grid through a LF transformer (cf. Fig. 1.7-c)), the losses in the full-scale AC-AC system are added to the transformer losses, leading to a solution with lower efficiency but higher controllability when compared to the option presented in Fig. 1.8-b). The loss contributions for the SST-based solution are presented in Fig. 1.8-d). Here, in addition to the transformer losses, the losses in the power electronic bridges represented by the front- and load-end AC-AC converters are encountered. It should be noted however that the transformer losses can be reduced due to the flexibility in the frequency selection, which enables an optimization of this component e.g. for maximum efficiency at a given volume. In order to be a real replacement for standard grid transformers, the aforementioned solutions must be able to offer comparable efficiency values as traditional transformers, which represents a major challenge given the inclusion of additional conversion stages which are operated at MV and higher frequencies.

For the construction of isolated three-phase AC-AC conversion systems several options with different functionalities, as the ones shown



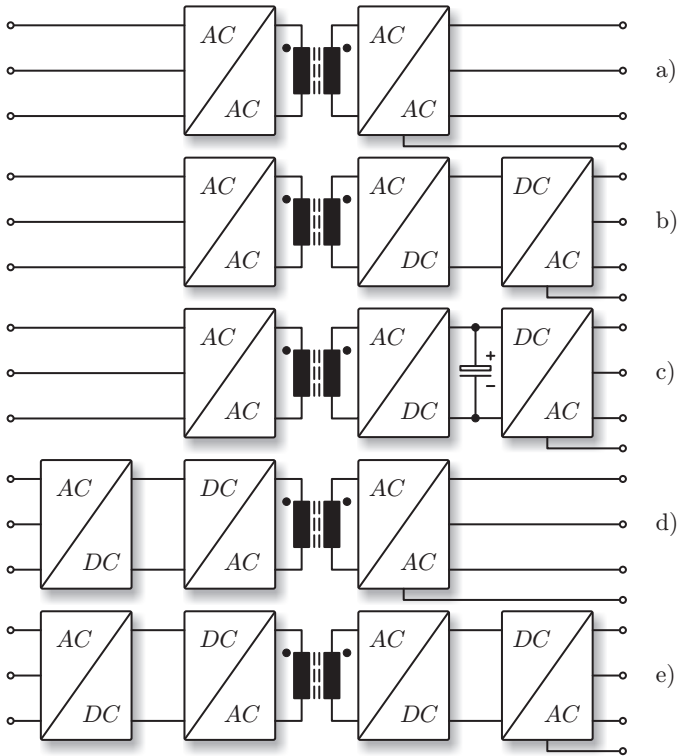
**Figure 1.9:** Classification of three-phase isolated AC-AC conversion systems ( $f_2^*$  denotes an output frequency, which can be selected independent of the input frequency  $f_1$ ).

in Fig. 1.7, are available. A comprehensive classification of these options is shown in Fig. 1.9. The first conceptual differentiation is made when selecting the operating frequency of the transformer, where the front-end LF and MF isolation are found. On the LF isolation side, a division between systems with and without capability of secondary side frequency adjustment is found. The first of this type of converters is the AC chopper, which is able to regulate output voltage without independent selection of frequency [18–20]. The electronic tap changer, as the name points out, is based on a tapped transformer where the switching between different taps is done with power electronic circuitry [21]. With this concept, the output voltage can be actively regulated therefore compensating for disturbances from the primary side. The last concept in this category is the series voltage compensator [21, 22]. This circuit is able to control the output voltage within a certain range depending on the amount of power the respective converter system is designed for. Other concepts which are able to control the output frequency while implementing a front-end LF transformer can be categorized in matrix-type and DC-link-based converters. Further details and topologies utilizing front-end LF isolation can be found in Appendix B.

Advanced concepts for isolated three-phase AC-AC converter systems comprising a MF isolation, i.e. SST concepts, can be also subdivided into output frequency-controllable and non-controllable concepts. Systems unable to control the output frequency can be found in the form of fundamental frequency front- and back-end matrix-based converters. For the output frequency-controllable concepts, the transformer can also be placed at the front-end while still being operated at higher frequencies, as is the case in [23, 24], which incorporates a matrix-type output stage.

Alternatively, the transformer can be integrated into the energy supply chain, leading to the last category of isolated AC-AC three-phase conversion systems. Here, the main categorization consist of the modularity level in the direction of the power flow. The non-modular structure consists of a single-stage concept, where the voltage from the three-phase grid is directly transformed into MF by a direct matrix-type structure on both sides of the MF transformer. Several realizations based on this concept can be found in literature [25–28]. Other concepts are comprising matrix-type structures on one side of the MF transformer while utilizing a DC-link-based arrangement on the LV side, leading to hybrid structures [10]. The fully-modular arrangement is represented

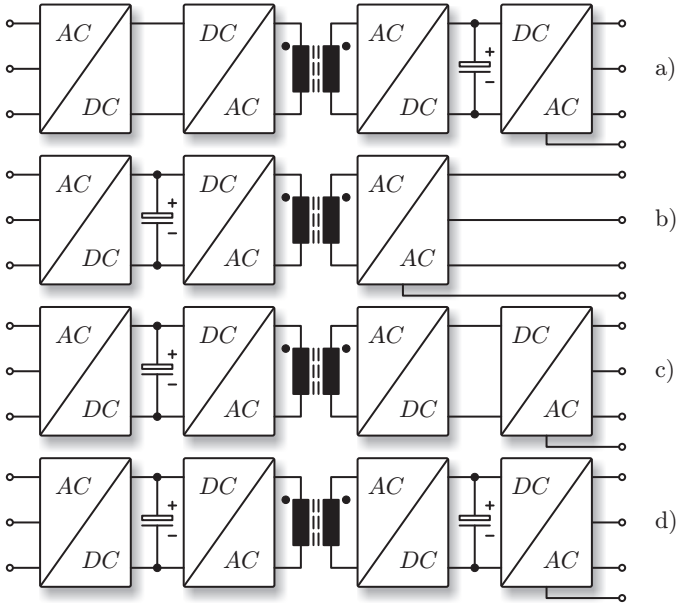




**Figure 1.10:** Possible full-scale three-phase to three-phase SST concepts: a) MV side direct matrix converter / LV side direct matrix converter; b) MV side direct matrix converter / LV side indirect matrix converter; c) MV side direct matrix converter / LV side DC-link-based converter; d) MV side indirect matrix converter / LV side direct matrix converter; e) MV side indirect matrix converter / LV side indirect matrix converter. For further topologies see Fig. 1.11.

by the MV and LV side DC-link-based structures, where the power flow is processed in three stages: AC-DC rectification, DC-DC conversion and finally DC-AC inversion [29, 30]

This last group, denominated as integrated transformer type, has gained intense attention due to its potential benefits in efficiency and power density, leading to a vast number of proposed converter units. In

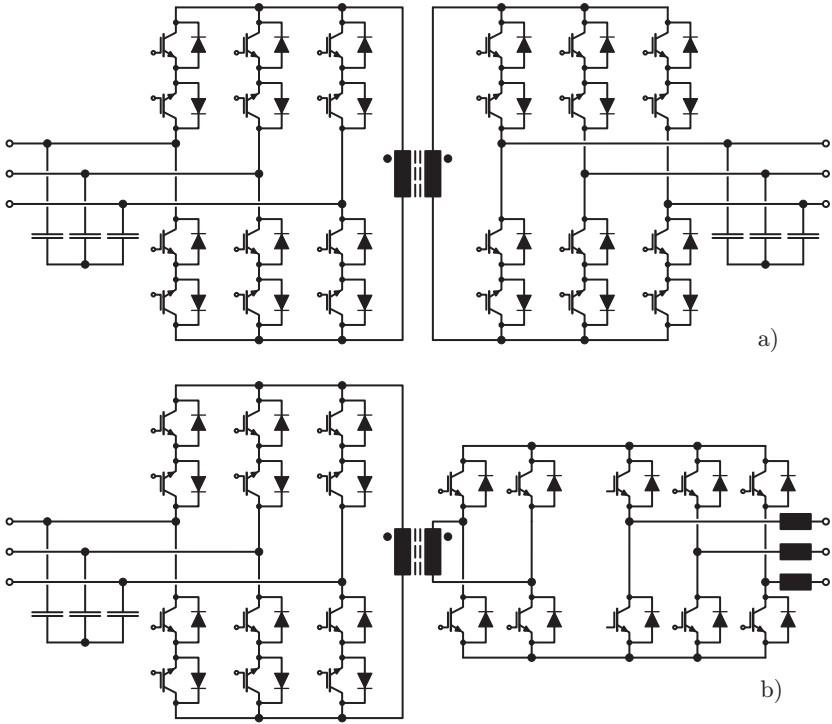


**Figure 1.11:** a) MV side indirect matrix converter / LV side DC-link-based converter; b) MV side DC-link-based converter / LV side direct matrix converter c) MV side DC-link-based converter / LV side indirect matrix converter; d) MV side DC-link-based converter / LV side DC-link-based converter. For further topologies see Fig. 1.10.

order to classify these proposed systems, an identification of the level of modularity is required in three different axes: 1) in the power flow direction; 2) concerning the realization of the three-phase property and 3) concerning the connection to the MV level, which is also beneficial for characterizing the complexity of the converter system. This classification regarding modularity level is described in the following.

### 1.3.1 Modularization of SSTs

The first selection in the construction of the SST is dedicated to how the power is processed along the supply chain. Several options are available, starting from single-stage to three-stage fully-modular options, all of which will be discussed in the following.

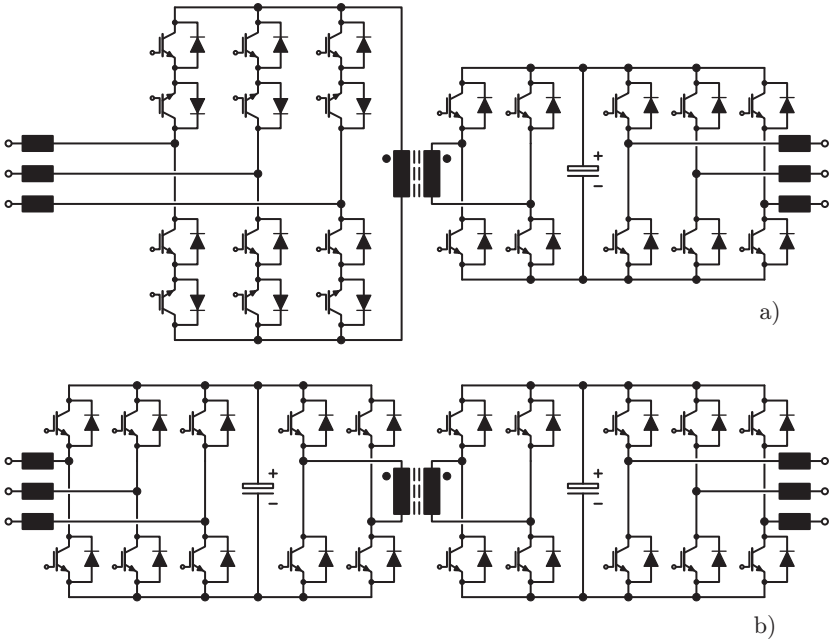


**Figure 1.12:** Possible full matrix-type SST concepts: a) MV side direct matrix converter / LV side direct matrix converter; b) MV side direct matrix converter / LV side indirect matrix converter.

### Modularization in Power Flow Direction

All different options for modularization in the power flow direction are presented in Figs. 1.10 and 1.11 and they comprise all possible combinations starting from direct three-phase matrix conversion, to indirect three-phase matrix conversion and finally DC-link-based converters. These types of conversion systems can be either on the LV or on the MV side of the SST, completing a total of nine options.

The circuit diagrams of four of these concepts are schematically presented (not taking into account the partitioning of the MV level to several series connected converter cells) in Figs. 1.12 and 1.13. In Fig. 1.12-



**Figure 1.13:** Possible DC-link-based SST concepts: a) MV side direct matrix converter / LV side DC-link; b) MV side DC-link / LV side DC-link.

a), the schematic representation of a single-stage direct matrix-type converter is shown. This concept utilizes six four-quadrant switches on the MV and the LV side. Since each of these switches comprises two IGBTs, a total of 24 devices is necessary in order to build this single-stage approach, which has been proposed in literature [25–28].

The first step in modularization is represented by the exchange of the direct matrix converter for an indirect type, as shown in Fig. 1.12-b). Here, similar functionality as with the direct matrix-type structure can be achieved while utilizing two semiconductor devices less.

Adding a DC-link on one of the converter’s sides represents the next step in modularization in the direction of the power flow. The version with MV side direct matrix-type converter and LV DC-link-based arrangement is shown in Fig. 1.13-a). This structure requires the same amount of semiconductor devices as the indirect matrix-type

structure, with the addition of a DC-link capacitor on the LV side. This capacitor effectively achieves a decoupling of the LF AC side from the MF AC side, which is beneficial for the design and optimization of the complete converter system.

The final step in modularization of the SST in the power flow direction is a fully-modular three-stage approach, where independent rectification, DC-DC conversion and inversion stages are utilized as shown in Fig. 1.13-b). This solution utilizes a total of 20 semiconductor devices, four less than the single-stage direct matrix-type system. Additionally, this approach allows the optimization of each converter stage in an individual manner, thus ensuring that an optimized/application-specific design is achieved. Moreover, the major challenge in the construction of this type of converter structure is now limited to the DC-DC conversion stage, where the operation at higher frequencies combined with the MV level represents a major research challenge.

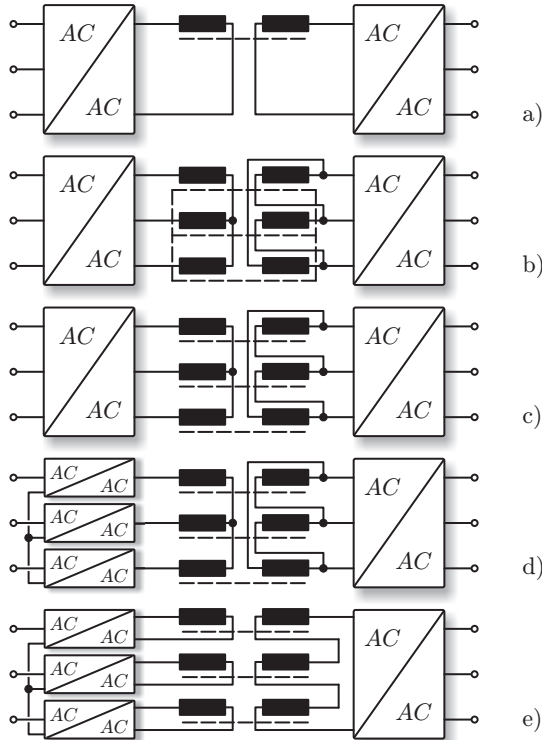
In the previous examples, the three-phase grid is interfaced with a three-phase integrated converter, either of matrix or of DC-link type. This solution, however, can be modified in order to, for example, utilize an independent converter for each of the phases, thus achieving a phase-modular structure in terms of the connection to the three-phase grid, which is covered in the next section.

### **Modularization in the Connection to Three-Phase Systems**

Another axis of modularization potential is represented by the different strategies to connect to the three-phase system, which could be either on the MV or LV grid side or on the transformer side. The different options for modularization in this axis are presented in Figs. 1.14 and 1.15 whereby, in order to simplify the classification, only direct matrix converter systems are considered, i.e. no modularization in the power flow direction is shown.

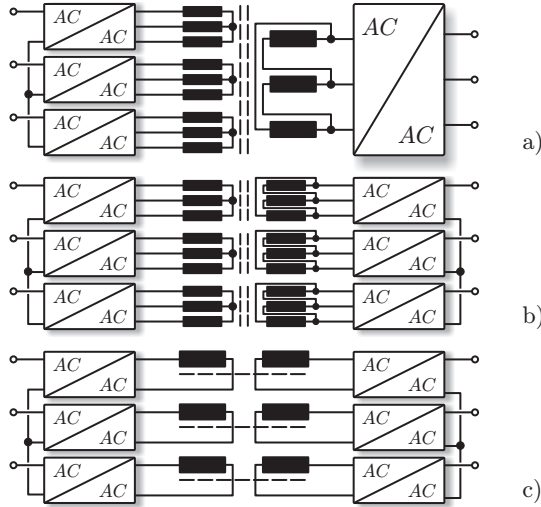
The lowest modularization level is represented by a solution which fully integrates the MV and LV side three-phase system while the MF AC-link is done with a single-phase transformer, as shown in Fig. 1.14-a). This isolation transformer can be also built as a three-phase system, whereby the respective magnetic circuit can be either integrated, i.e. a single multi-limb magnetic core could be employed (cf. Fig. 1.14-b)) or independent magnetic circuits could be utilized as shown in Fig. 1.14-c).

The first step of modularization on the LF sides (input and output side) is shown in Fig. 1.14-d), whereby the MV side converter has



**Figure 1.14:** Direct matrix-type three-phase SST topologies showing different degrees of phase modularity; a) Three-phase integrated MV and LV side LF interfaces and single-phase MF transformer; b) as a) but three-phase magnetically-integrated MF transformer; c) as b) but independent magnetic circuits (cores) of the three-phase transformer phases; d) as c) but phase-modular MV side LF AC interface; e) as d) but individual single-phase transformers connected to the MV side phase modules and series connection of the transformer secondary windings forming a single-phase output connected to a LV side converter stage as shown for a). For further topology variations see Fig. 1.15.

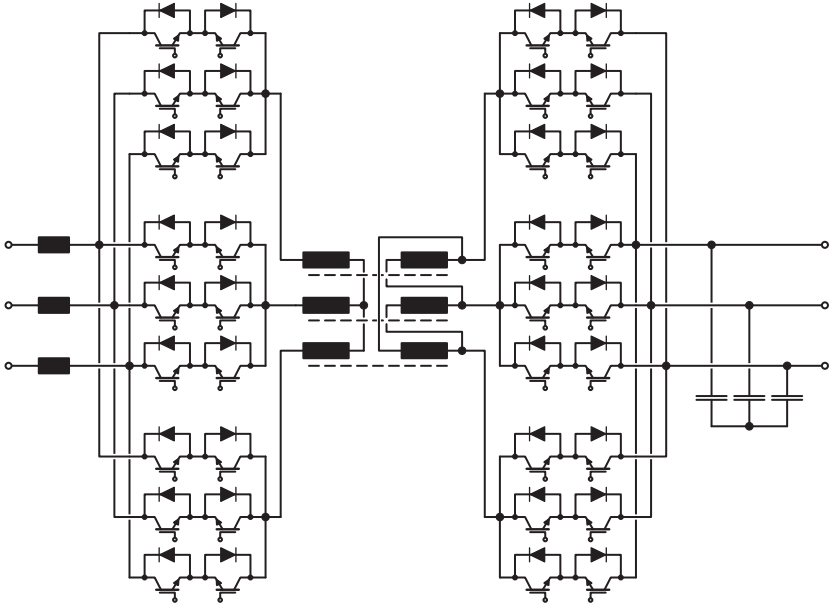
been split into three independent single-phase converters each of them connected to one of the phases of the three-phase network. Each of



**Figure 1.15:** a) as Fig. 1.14-e) but three-phase output of the MV side phase modules and magnetically fully-integrated transformer arrangement with three sets of three-phase MV windings and a single three-phase LV winding; b) Phase-modular MV and LV side converter interfaces with converter phase modules connected through individual three-phase transformers; c) as b) but single-phase instead of three-phase transformers. For further topology variations, see Fig. 1.14.

these converters feeds a winding of a magnetically independent three-phase transformer. A special case is found when the LV side windings of the transformer in Fig. 1.14-d) are connected in series, leading to a single-phase transformer seen from the LV side as shown in Fig. 1.14-e).

The solutions presented so far utilize a single-phase transformers or a single three-phase transformer arrangement, where the magnetic circuits are either integrated or independent. The next step is to construct independent transformers fed by independent converter modules. The solution in Fig. 1.14-e) can be extended with independent three-phase windings on the MV side magnetically coupled to a three-phase winding arrangement on the LV side, as shown in Fig. 1.15-a). The fully-modular structures, i.e. LF MV and LV phase-modular and independent transformers, are shown in Figs. 1.15-b) and c) for the three-

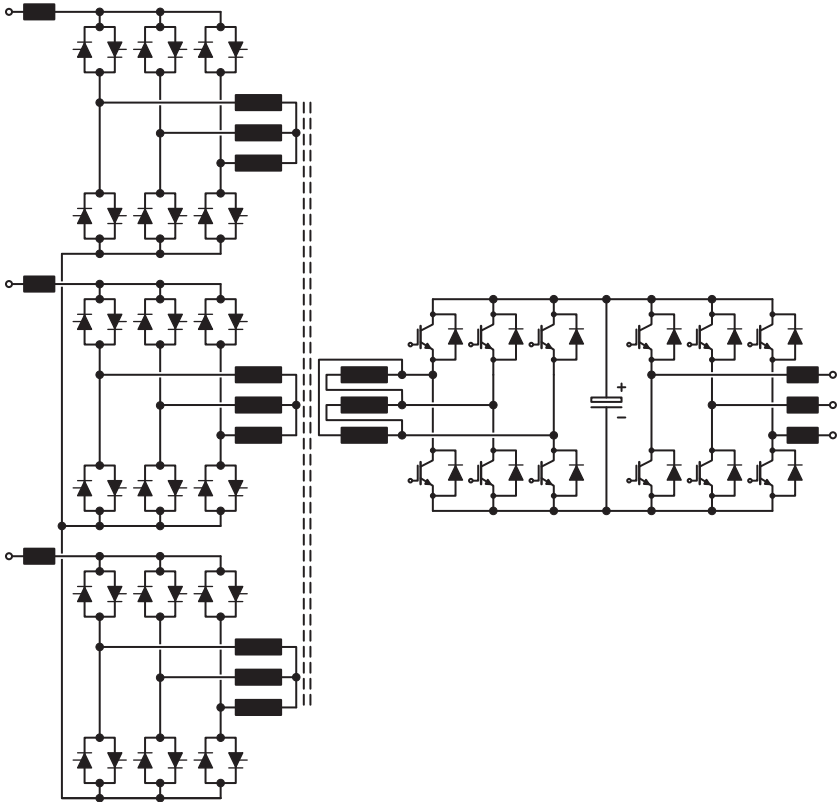


**Figure 1.16:** Direct matrix-type, three-phase integrated MV and LV side LF interfaces and three-phase MF transformer with individual magnetic cores of the phases (cf. Fig. 1.14-c) [8].

phase and single-phase transformer solutions respectively. These last levels of high modularity result beneficial in high power solutions, as each component can be independently designed to meet specific requirements.

Two examples of the aforementioned phase-modular solutions are presented in Figs. 1.16 and 1.17, for the fully-three-phase-integrated solution from Fig. 1.14-c) (with magnetically independent phases) and the MV side modular three-phase magnetically integrated solution from Fig. 1.15-a). The fully-integrated solution comprises bidirectional switches which directly connect the MV and LV LF sides to the MF transformer, realizing the conversion of energy in a single-stage. This solution however, requires the implementation of four-quadrant switches, thus requiring a high number of semiconductor devices. The solution





**Figure 1.17:** Phase-modular MV side and three-phase integrated LV side LF interface and MV side phase-modular three-phase magnetically integrated MF transformer (cf. Fig. 1.15-a) [31].

in Fig. 1.17 incorporates a MV side modular magnetically integrated three-phase transformer, whereby the LV side converter comprises two-level three-phase integrated bridges on both MF and LF sides (the LV side rectifier stage provide the commutation voltage for the MV side thyristor bridges).

The means to split the converter into power conversion stages and the different concepts utilized to connect to three-phase systems on the MF and LF sides have been clarified. It is now necessary to study the

possibilities available to deal with the MV level. The desire to operate at higher frequencies while still reaching high efficiency values presents a key challenge within the realization of SSTs. The different options available to deal with the MV level will be covered in the next section as a final axis of the different modularization options.

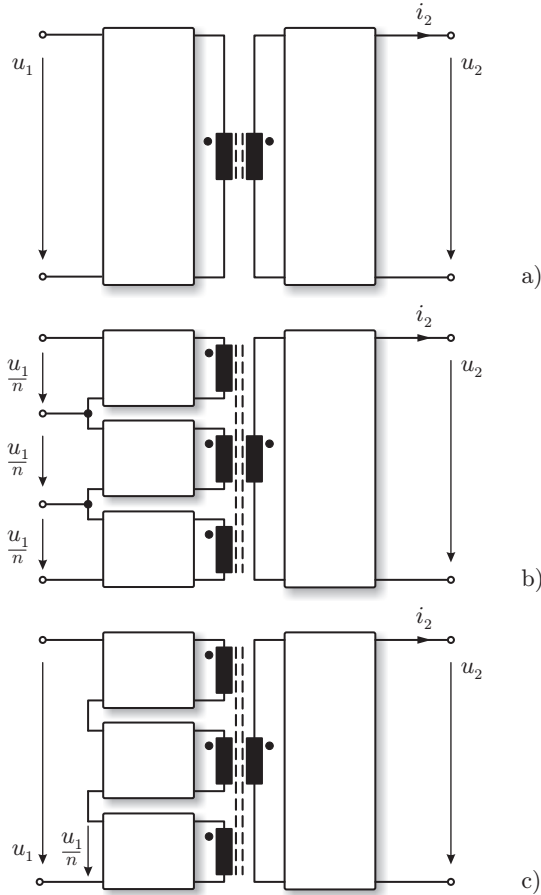
### **Modularization in the Connection to the MV Level**

The last step in modularization of the SST topology is required in order to deal with the voltage levels encountered in these applications, which typically reach up to the tens of kilovolts. The current semiconductor technology does not provide single devices designed for these voltage levels. For this reason, advanced converter structures able to block these high voltages while operating at higher frequencies and reaching high efficiency levels become mandatory.

Figs. 1.18 and 1.19 present the main options for modularization in the voltage direction. It should be noted that this modularization can be performed either on the DC or AC side of the converter in case a multi-stage solution is implemented. The first option, in Fig. 1.18-a) is a fully-integrated solution, which comprises power semiconductor bridge legs of the type shown in Fig. 1.20-a). The MV side voltage can be subdivided into lower voltage DC-links whereby the respective semiconductor devices are of the LV class. The first of these options is shown in Fig. 1.18-b). This solution would result from the implementation of the bridge legs as shown in Fig. 1.20-b) on the MV AC side, whereby the intermediate levels of the DC-link voltage are available at the input. In case the MV side converter is built with a cascaded concept, as the bridge shown in Fig. 1.20-c) and Fig. 1.21, the structure shown in Fig. 1.18-c) is suitable. Here, the MV side converter relies on a series connection of independent partial voltages in order to deal with the voltage level, while the LV side is still constructed with a single bridge.

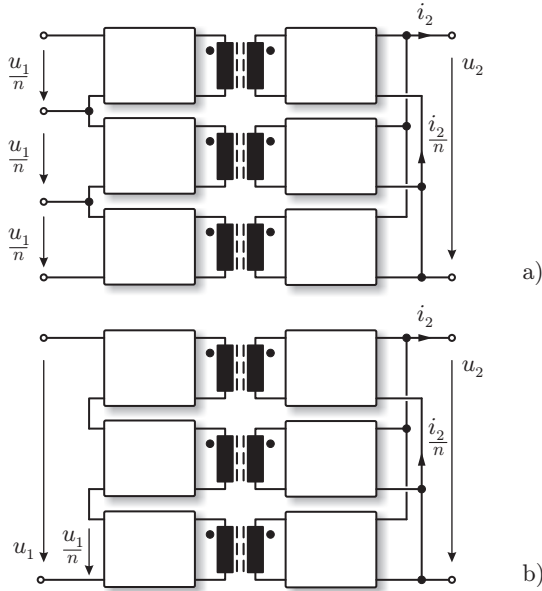
The two fully-modular approaches, comprising series connection on the MV side and parallel connection on the LV side are presented in Fig. 1.19. Depending on the type of bridge leg arrangement utilized on the MV side, the intermediate DC-link levels will be available (cf. Fig. 1.19-a)) or unavailable (cf. Fig. 1.19-b)).

It is important to remark that the construction of the SST utilizing one of the aforementioned strategies is mandatory in order to deal with the MV level while reaching the high efficiency goal. This in-



**Figure 1.18:** Schematic representation of the modularization in voltage direction: a) Non-modular MV and LV sides; b) Modular series-connected MV side with access to intermediate levels and non-modular LV side; c) Modular series-connected MV side with internal intermediate levels and non-modular LV side. For further topology variations see Fig. 1.19

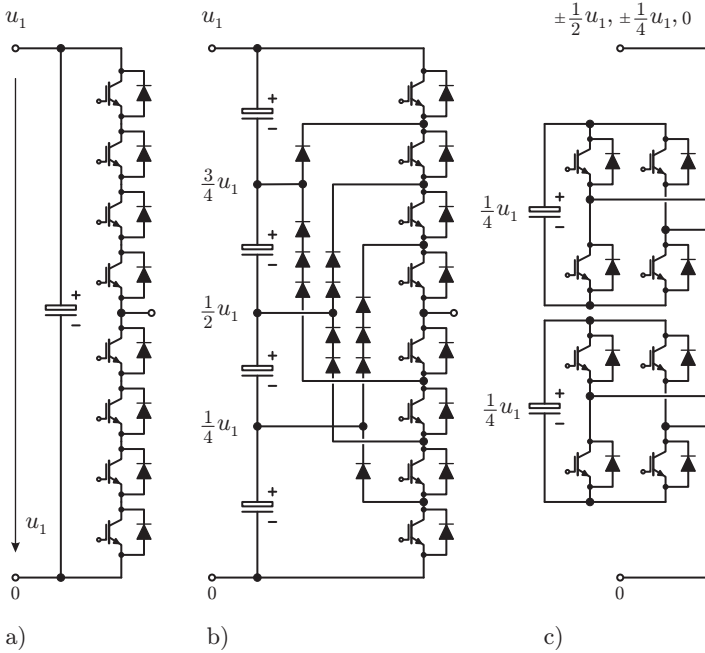
creased complexity brings new challenges in the construction of SSTs such as optimum number of series-connected converter modules [32], common-mode currents, and mixed MV DC and MF AC electric field



**Figure 1.19:** Schematic representation of the modularization in voltage direction: a) Modular series-connected MV side with access to intermediate levels and modular parallel connected LV side; b) Modular series-connected MV side with independent intermediate levels and modular parallel connected LV side. For further topology variations see Fig. 1.18

stress on insulation materials [33]. This last topic is one of the keys for the successful deployment of SST technologies in the aforementioned application fields.

The numerous degrees of freedom for modularization available in the SST lead to a vast amount of possible arrangements depending on the different levels of modularization in the three discussed modularization axes: Degree of Power Conversion Partitioning; Degree of Phase Modularity and Number of Levels or Series/Parallel Connected Cells. Since the level of modularity in each of these different directions is independent, these three axes can be considered to be orthogonal to each other, enabling a representation as shown in Fig. 1.22. Here, each element rep-

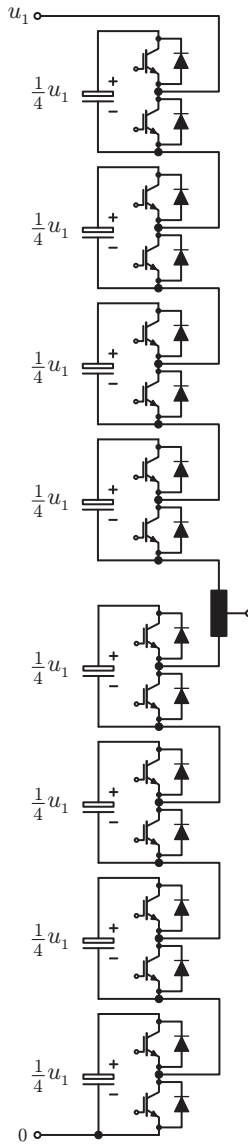


**Figure 1.20:** Bridge leg arrangements utilized to deal with the MV level: a) Series connection of devices; b) Series connection in multilevel arrangement; c) Multi-cell arrangement.

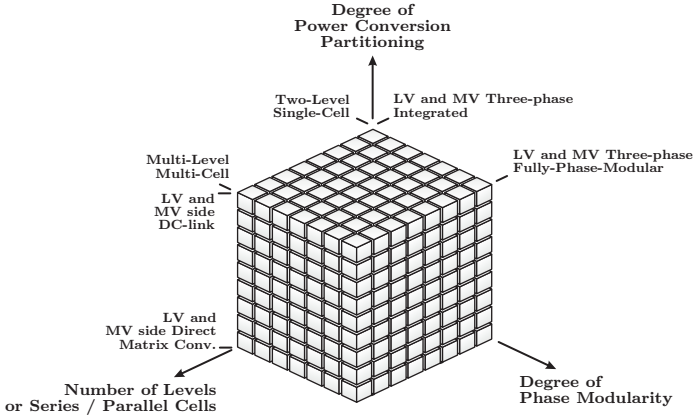
resents a specific design with a certain amount of modularization in each of the axes.

For example, an element close to the origin would represent a low level of modularity in all axes, i.e. a direct matrix-type structure on the MV and LV sides without series connection on the MV side and fully-integrated three-phase LF interfaces. On the other hand, an element distant from the origin would represent a highly modular structure, i.e. a multi-stage power conversion system with series connection of converter cells on the MV side, parallel connection on the LV side and independent modules interfacing to each of the three phases on the MV and the LV side. In similar way, other concepts can be conceived, with different levels of modularization in each of the different axes.

Fig. 1.22 qualitatively shows the large amount of options available for the construction of the SST for Smart Grid applications. This clas-



**Figure 1.21:** Modular-multilevel arrangement.



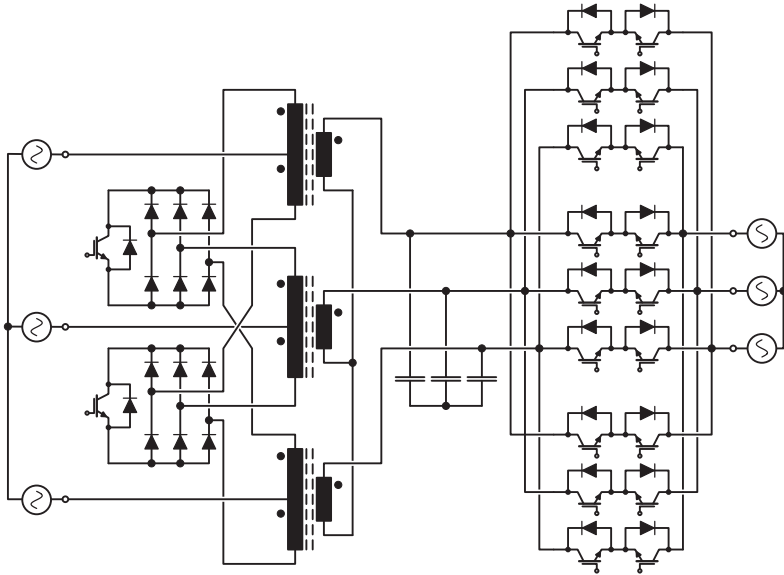
**Figure 1.22:** Three degrees of modularity: Degree of Power Conversion Partitioning; Degree of Phase Modularity and Number of Levels or Series/Parallel Connected Cells. Together these three modularity axes are defining a fine mesh of options from which the SST can be constructed.

sification based on the level of modularity will be now utilized to classify the previously reported solutions for three-phase AC-AC interfaces which ultimately leads to the selection of the topology and the specifications for the project developed in this thesis.

### 1.3.2 Previously Reported SST Structures for Smart Grid Applications

A number of concepts with various levels of modularity in the different aforementioned directions have been studied in previous research projects. In the following, a selection of these concepts which have been recently proposed will be briefly discussed together with their respective schematic representations.

Belonging to the front-end transformer/matrix-type output stage category, the converter shown in Fig. 1.23 and discussed in detail in [23] achieves the MF operation of the transformer by connection of two three-phase short circuit switches (formed by a three-phase diode rectifier and a DC-side switch) to the three winding terminals of independent center-tapped transformers. The IGBT switches are realizing alterna-



**Figure 1.23:** Front-end transformer MF AC-link concept with direct output matrix-type converter presented in [23].

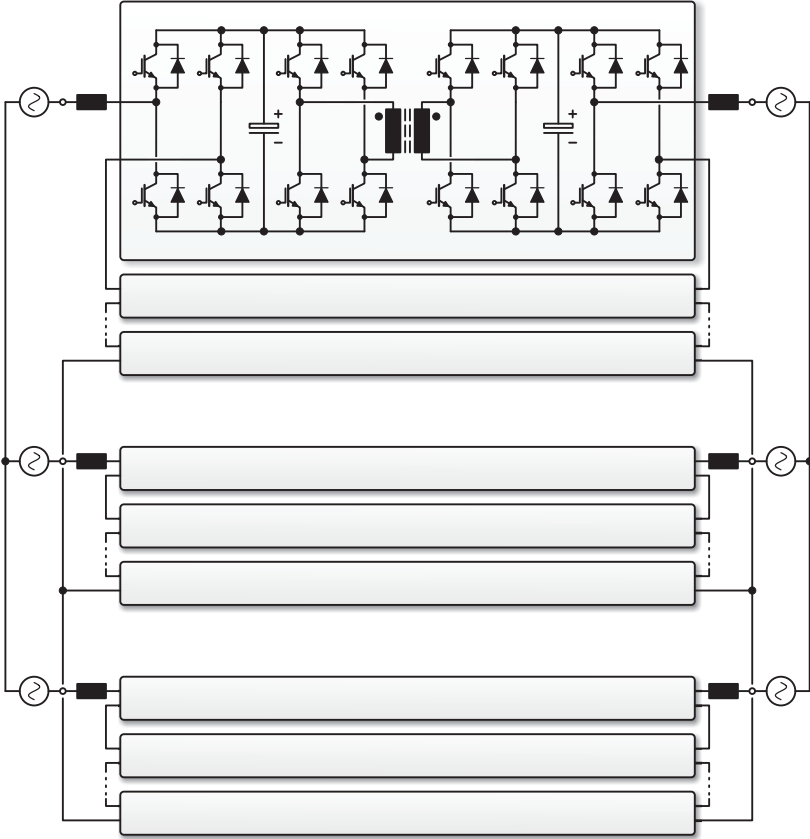
tive star-point connections of these transformers at higher frequencies, thus selecting the polarity of the voltage applied to the secondary of the transformer by turning the upper or lower IGBT on. On the secondary side, a direct matrix-type converter links the converter to the LV side LF grid.

A structure comprising full modularity in the power flow direction, phase modularity and series connection of cells was presented in [29] (cf. Fig. 1.24). This fully-modular arrangement subdivides the complete complex converter structure into standardized units, which allows to independently design and optimize the different converter modules.

An advanced SST structure utilizing SiC devices on the MV side was mentioned in [34] and is depicted in Fig. 1.25. This converter implements an indirect matrix-type conversion on the MV and LV sides. Additionally, as can be seen, full modularity in the three-phase connection and in the cascading of converter cells is performed in order to deal with the selected voltage levels.

Fig. 1.26 presents a phase-modular concept with MV side cascaded

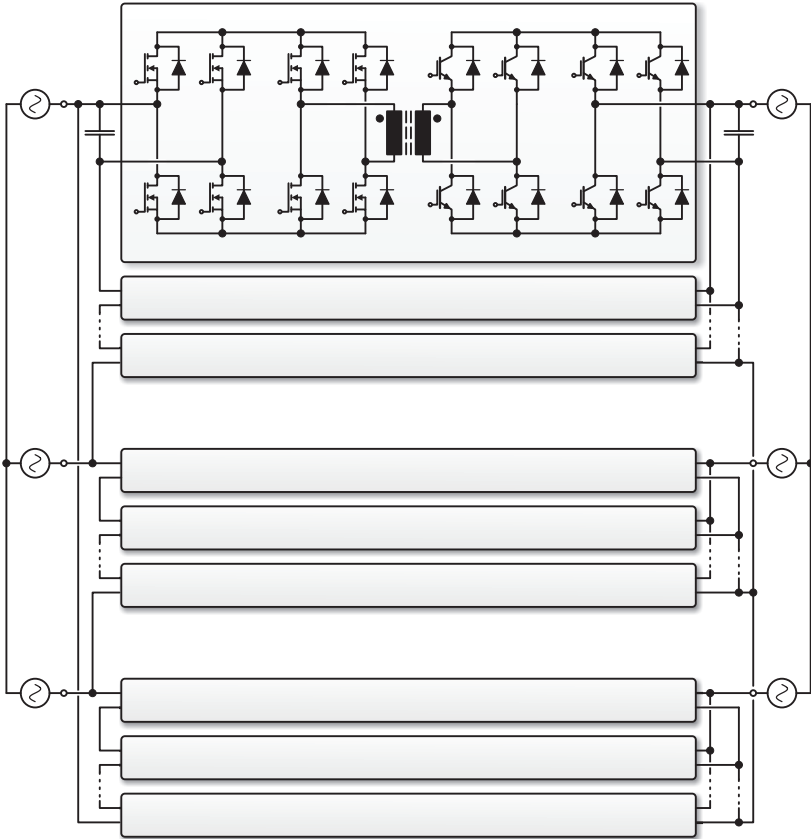




**Figure 1.24:** Fully-modular multi-cell structure as presented in [29].

cells and magnetically independent transformers with electrically integrated three-phase LV side MF and LF AC connections [35]. Given the lower voltage level on the LV side, this structure relies on the availability of single power semiconductor devices in this voltage range, which simplifies the construction of the LV side power electronic bridges.

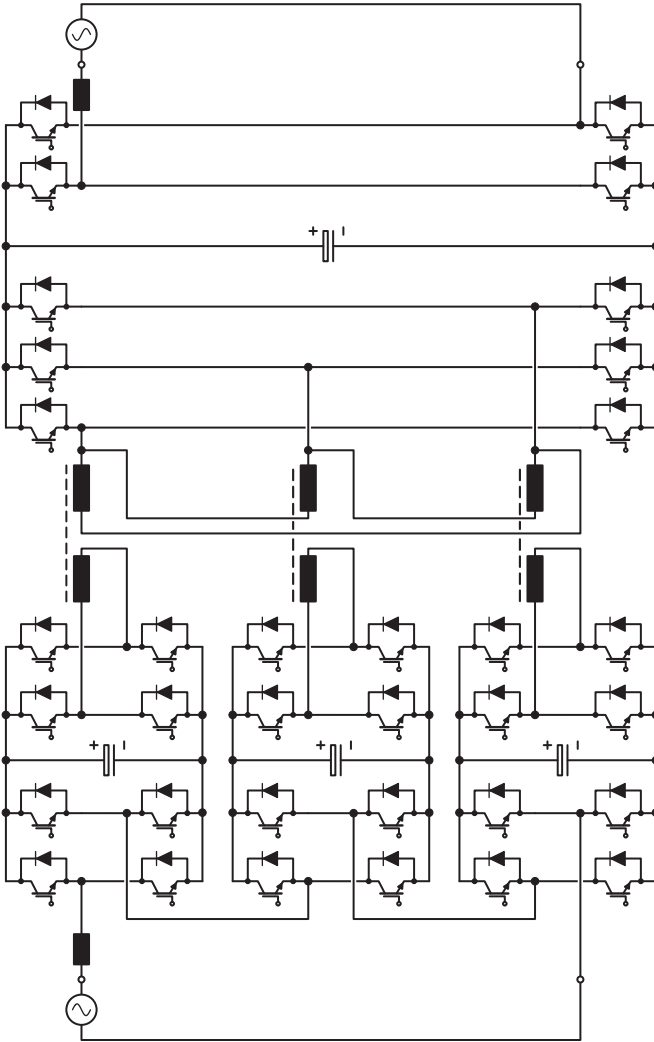
In order to deal with higher voltages while keeping a low component count, the concept presented in Fig. 1.27 and proposed in [36] utilizes gate turn-off devices on the MV side. These semiconductor



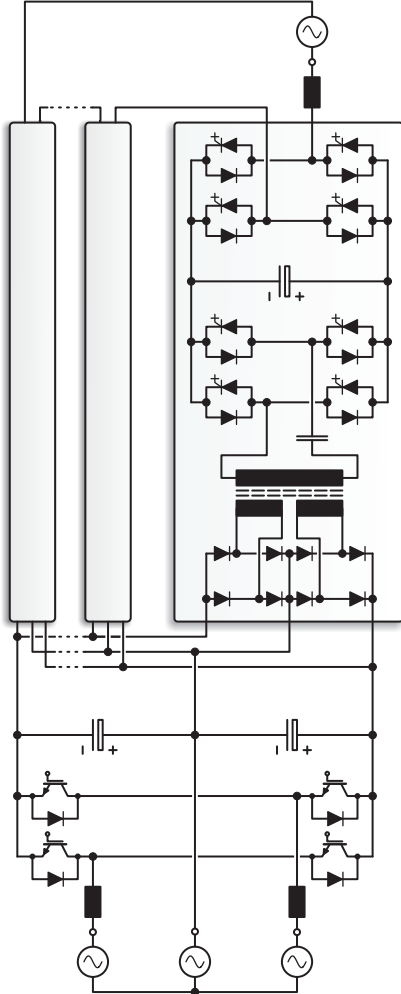
**Figure 1.25:** Indirect matrix-type, phase-modular multi-cell structure mentioned in [34].

devices, however, are characterized by a slow switching performance, which compromises the flexibility on the selection of the transformer's operating frequency. Additionally, this DC-link-based structure is constructed with a series connection at the MV side and a three-phase integrated LV side concept.

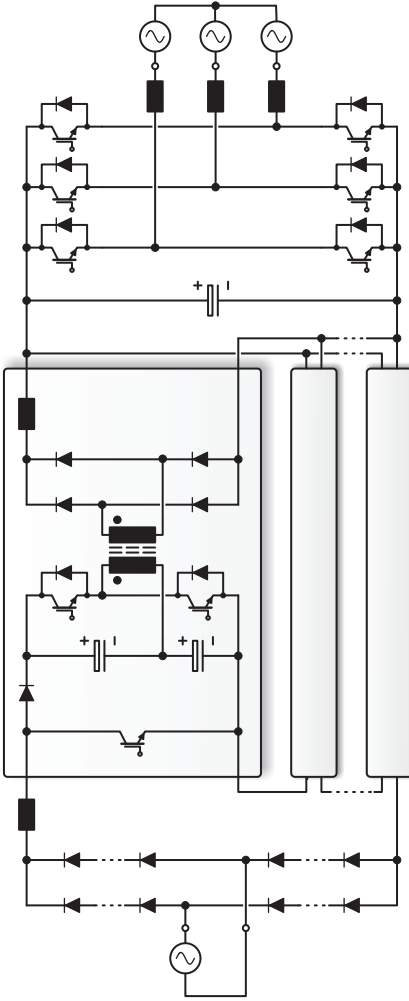
Further structures with unidirectional power transfer capability have also been proposed, as is the case for the converter in Fig. 1.28 which was presented in [37]. This converter is characterized by a multi-cell



**Figure 1.26:** DC-link-based single-phase SST, with MF-side phase-modular, magnetically independent three-phase transformer and three-phase integrated (transformer and converter) LV side rectifier stage, presented in [35].



**Figure 1.27:** Unidirectional SST with DC-link-based cascaded and phase-modular MV side and three-phase integrated IV side; independent single-phase transformers of the individual cells with parallel connected secondary side rectifier stages [36]; representation of MV side limited to one phase.



**Figure 1.28:** Unidirectional SST with single diode bridge rectifier input stage with series-connected diodes and following multi-cell current shaping and isolation stage with parallel connected output rectifiers supplying the DC-link of a three-phase integrated LV side mains interface, as presented in [37]; representation of MV side limited to one phase.

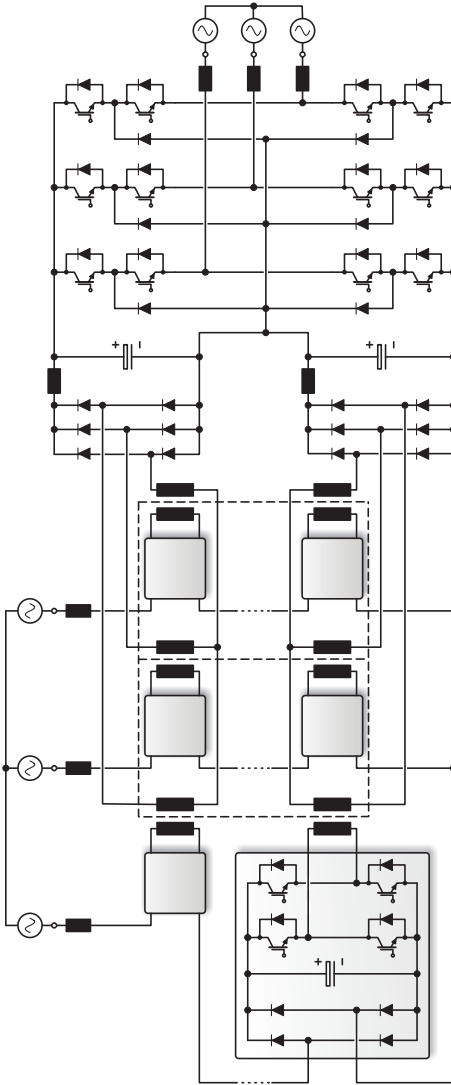
boost-type input stage based on a full-wave diode rectifier. The boost converters are arranged into modules whereby their isolated DC sides are connected in parallel and feeding a three-phase two-level inverter linked to the LV side network. It should be noted that this unidirectional structure reduces considerably the complexity of the system when compared to the discussed fully-bidirectional structures.

The magnetic integration of a three-phase transformer results attractive due to the potential reduction of required magnetic core material. This is the case for the concept proposed in [38] and shown in Fig. 1.29. This modular arrangement connects to the MV side through a series connection of modules, i.e. a multi-cell structure. Each of the MV side modules feeds an individual winding of a three-phase/magnetically-integrated transformer. On the LV side, two full-wave diode bridges feed two series-connected DC-links which form part of a three-level Neutral Point Clamped (NPC) structure utilized to link to the LV grid with a three-phase integrated bridge.

Similar to the previous concept, the MV side modules can be replaced by matrix-type bridges in order to eliminate one conversion stage, as presented in Fig. 1.30 and studied in [39]. Here, at the input side, four-quadrant switches in full-bridge configuration are utilized to feed a three-phase magnetically integrated transformer with MF excitation. A single three-phase secondary winding linked to a three-phase integrated active rectifier bridge supplies a DC-link connected to a two-level inverter linked to the LV side grid.

Another type of three-stage, phase-modular and multi-cell arrangement with magnetically integrated three-phase transformer is presented in Fig. 1.31. This structure, proposed in [38], utilizes a multi-winding transformer with combination of star and delta connections on the secondary sides. It should be noted however, that the magnetic integration of the three-phase transformer results in a complex magnetic circuit, where the coupling between the different transformer windings must be carefully accounted for.

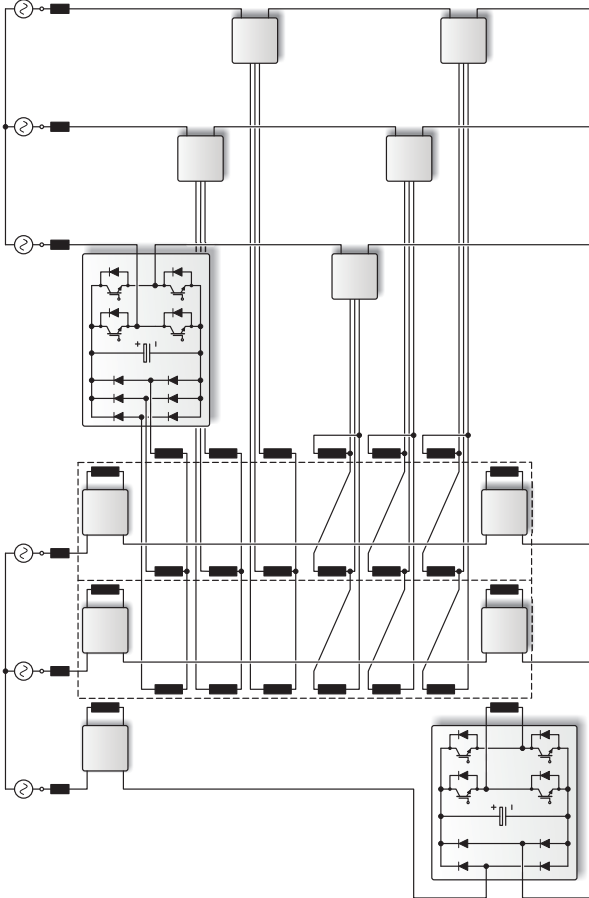
A highly modular structure able to interface three three-phase grids is presented in Fig. 1.32. This structure was developed in a large scale European project [40] studying flexible AC conversion systems for future electric power distribution. The core component in this arrangement is a back-to-back full-bridge-based module which interfaces on the one side the LF grid and on the other side performs the switching at MF which feeds the isolation transformer. As can be seen, this con-



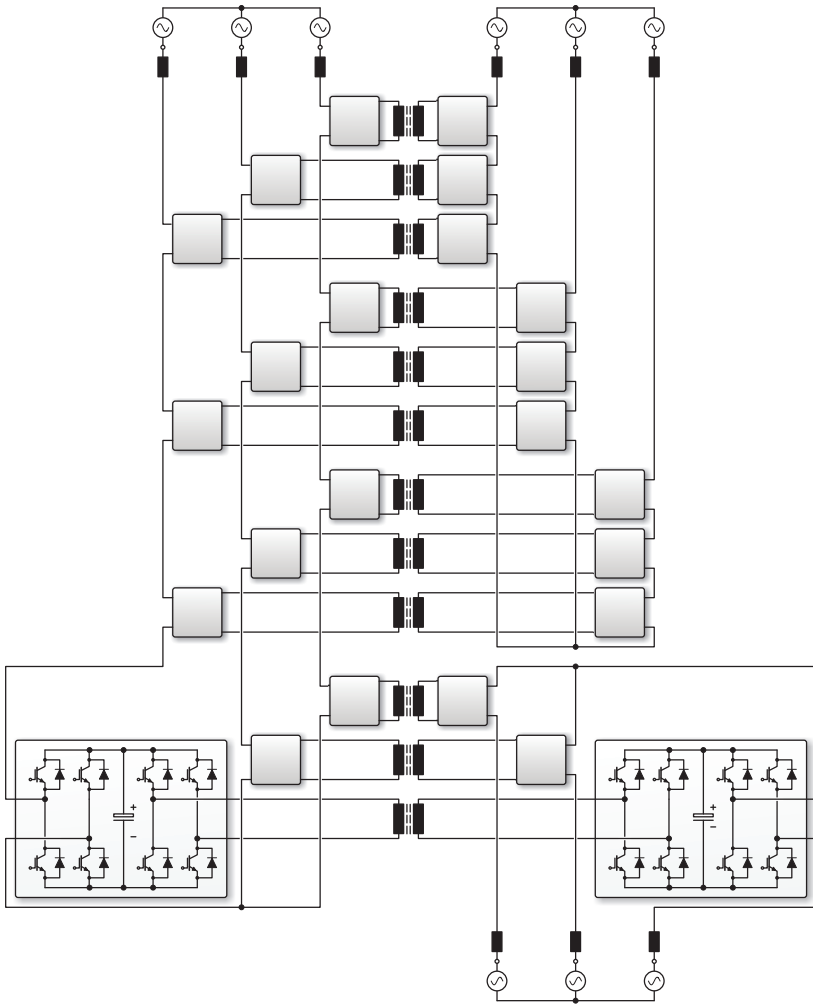
**Figure 1.29:** DC-link-based three-stage converter with cascaded MV side arrangement and integrated three-phase LV side. The transformer consists of a three-phase magnetically integrated construction [38].







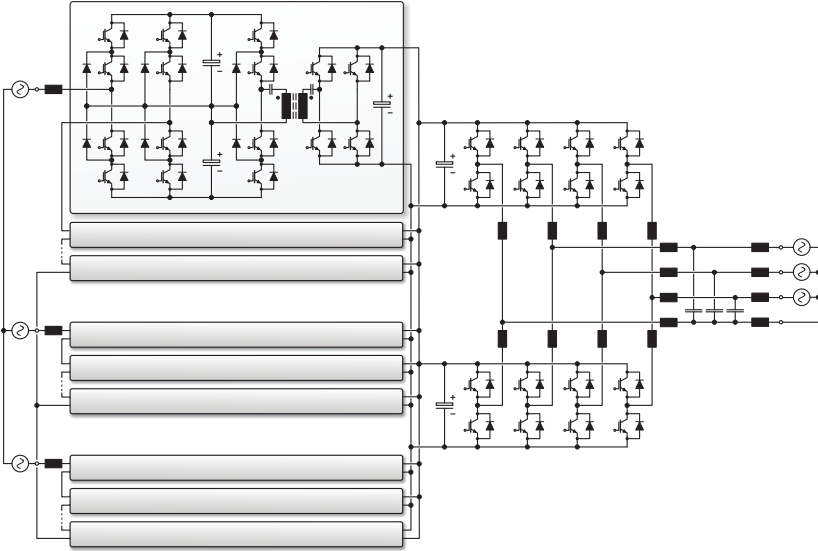
**Figure 1.31:** DC-link-based modular cascaded MV and LV side SST with three-phase magnetically integrated three-phase MF AC-link [38].



**Figure 1.32:** Fully-phase-modular arrangement with cascaded input and output sides, independent single-phase transformers and an additional three-phase output [40].

verter structure is realized with full modularity in all aforementioned modularization axes.

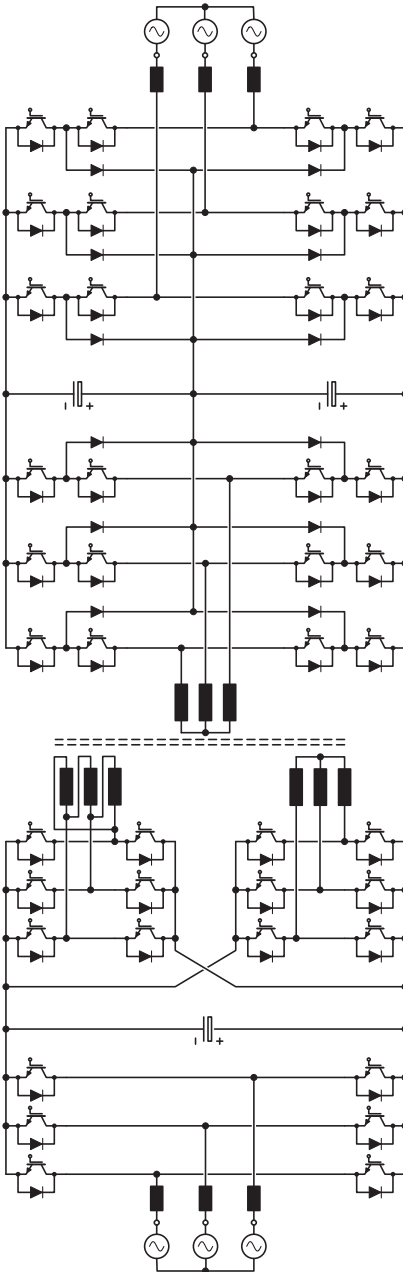
The converter presented in Fig. 1.33, denoted as MEGALink [41] is



**Figure 1.33:** SST (MEGALink) with DC-link-based cascaded and phase-modular MV side where the converter cell DC-links are connected to DC-DC converter stages comprising single-phase transformers; the transformer secondary windings are connected via individual rectifier stages in parallel to the DC-link of the LV three-phase integrated inverter stage interfacing to the LF three-phase grid [41].

based on a series connection at the MV side and DC-link-based power conversion chains on the MV and LV side. On the LV side, two parallel three-phase integrated two-level bridges are utilized in order to link to the three-phase grid. The DC-DC stages consist of a series resonant structure and are parallel connected on the LV side, where they are connected to the aforementioned two-level inverters.

The converter shown in Fig. 1.34 realizes the link to the MV side grid with a multilevel NPC-based arrangement comprising SiC semiconductor devices [42, 43]. The MF conversion is performed by a three-phase magnetically integrated transformer with two secondary windings connected in star and delta respectively. Active rectifiers transform this MF waveforms from the transformer's secondary to a single LV DC-link feeding a two-level, three-phase inverter.



**Figure 1.34:** Three-stage DC-link-based approach with integrated MV and LV side three-phase arrangements and integrated three-phase MF AC-link [42, 43].

With the comprehensive review of previously proposed concepts and their different modularity levels, a discussion of the most suitable structure and specifications of an SST concept to be researched in this thesis will be presented in the next section.

## 1.4 DC-DC Converter Topology and Specifications Selection

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The previous sections demonstrated the tendency towards the modularization of the power conversion chain in SSTs. As mentioned earlier, a high degree of modularity in the power conversion direction enables the optimized design of the different stages involved in the energy conversion: rectification, isolated DC-DC conversion, and inversion. Among these different stages, the DC-DC conversion stage presents the major challenges due to the combination of high-power, MV, and MF. Moreover, this stage is now responsible for the galvanic isolation between the MV and the LV side, thus the MF transformer represents a key component within the conversion chain. For these reasons, the focus of this thesis will be placed on three-stage DC-link-based SSTs and specifically on the high-power DC-DC conversion stage.

Traction and Smart Grid applications require components able to process powers in the MW range. Therefore, in order to attractively compete with the existing technologies, the total conversion system developed in this thesis is aimed for 1 MW of transferred power. Moreover, in order to reach a high power density in the converter design while exploring the behavior of magnetic components at higher frequency levels, an operating frequency of 20 kHz is selected. It should be noted that this frequency may not be considered high in lower power applications. Therefore, this frequency range is often referred to as MF and so will it be along this thesis.

In order to connect to the MV grid while operating at the selected frequency, a modularization in the voltage direction of the converter must be considered. This modularization can be done in the LF AC MV side or at the MV DC-link of the converter. Since the analysis of the LF AC side converters (rectifier and inverter) is out of the scope of this thesis, a series connection is considered for the MV side DC-link.

Given typical voltage levels in the MV and LV range [2], a MV side DC-link of 12 kV is considered together with a 1.2 kV LV DC-link. The means to deal with these voltage levels, i.e. the modularity level in the voltage direction will be decided once the possibilities for the construction of the DC-DC converter regarding topologies and modulation schemes are analyzed.

The selected DC-DC converter specifications are presented in Table. 1.1.

**Table 1.1:** Targeted specifications of the high-power DC-DC converter researched in this thesis.

Parameter	Value
Nominal power	1 MW
Operating frequency	20 kHz
MV side voltage	12 kV
LV side voltage	1.2 kV

## 1.5 Thesis Outline

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In the following chapters, the details about the design of the high-power DC-DC converter as specified in the previous section will be presented. In Chapter 2, the possible bridge configurations and soft-switching modulation schemes suitable for high-power DC-DC conversion will be studied in detail, leading to the final DC-DC converter module structure and the reference design values for the circuit parameters and waveforms of the converter system.

With these values defined, the analysis and design of the MV side power electronic bridge is initiated in Chapter 3. As a start, the theoretical background describing the behavior of IGBTs under soft-switching conditions is outlined. Extensive experimental analysis is later carried out in order to verify the proposed analytical loss models for IGBTs under soft-switching, namely ZCS, conditions. The chapter is finalized with a description of the final MV side bridge mechanical design, comprising heat sink dimensioning, power circuit layout, capacitor selection and gate driver concept, among others.

Possible bridge structures for the LV side power electronics are presented in Chapter 4. Here, alternative mixed-bridge structures comprising IGBTs and MOSFETs in a full-bridge configuration are presented. Experimental verification of the achieved reduction in overall losses gained by utilizing these bridges is presented. The chapter concludes with the details about the mechanical arrangement of the built LV side power electronic bridges, where details about the heat sink design/selection, circuit layout, capacitor selection and gate driver circuitry are presented.

The key component within the high-power DC-DC converter is the MF transformer, whereby the details regarding its design are presented in Chapter 5. This chapter starts with a literature search which

is aimed to identify the most utilized transformer concepts in this power/frequency range. This literature search leads to the selection of the suitable transformer concepts, which are optimized in this chapter following the proposed optimization procedure. The mechanical construction together with an extensive experimental verification of these optimized transformer designs concludes the chapter.

Chapter 6 addressed the DC magnetization phenomenon of transformers due to the non-ideal behavior of semiconductor devices. A comprehensive classification of previously proposed approaches to deal with this phenomenon is presented, leading to the detailed description of a novel concept utilized in this project: the "Magnetic Ear". Experimental verification utilizing the proposed flux density transducer is carried out, whereby the capability of this transducer and its respective feedback loop to ensure an unbiased operation of the transformer (DC flux density component controlled to zero) is shown.

The design of two converters with equal terminal specifications, i.e. equal power and MV/LV voltage levels but different modulation schemes, is described in Chapters 3, 4 and 5. In Chapter 7 the final assembly of these converters and their respective control boards are shown. Finally, back-to-back high-power testing of the two converters is carried out in order to experimentally verify the design of these systems.



## 1.6 List of Publications

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### Conference Papers

- ▶ G. Ortiz, C. Gammeter, J. W. Kolar, **Mixed MOSFET/IGBT Bridge for Highly-Efficient Medium-Frequency Dual-Active Bridge Converter in Solid-State Transformers**, Proceedings of the 14th IEEE Workshop on Control and Modelling for Power Electronics (COMPEL 2013), Salt Lake City, USA, June 23-26, 2013. → Best Paper Award.
- ▶ G. Ortiz, M. Leibl, J. W. Kolar, O. Apeldoorn, **Medium Frequency Transformers for Solid-State-Transformer Applications - Design and Experimental Verification**, Proceedings of the 10th IEEE International Conference on Power Electronics and Drive Systems (PEDS 2013), Kitakyushu, Japan, April 22-25, 2013. → *Best Paper Award*.
- ▶ G. Ortiz, L. Fässler, J. W. Kolar, O. Apeldoorn, **Application of the Magnetic Ear for Flux Balancing of a 160kW/20kHz DC-DC Converter Transformer**, Proceedings of the 28th Applied Power Electronics Conference and Exposition (APEC 2013), Long Beach, California, USA, March 17-21, 2013. → *Best Poster Award*.
- ▶ J. Huber, G. Ortiz, F. Krismer, N. Widmer, J. W. Kolar, **Pareto Optimization of Bidirectional Half-Cycle Discontinuous-Conduction-Mode Series-Resonant DC/DC Converter with Fixed Voltage Transfer Ratio**, Proceedings of the 28th Applied Power Electronics Conference and Exposition (APEC 2013), Long Beach, California, USA, March 17-21, 2013.
- ▶ G. Ortiz, D. Bortis, J. W. Kolar, O. Apeldoorn, **Soft-Switching Techniques for Medium-Voltage Isolated Bidirectional DC / DC Converters in Solid-State Transformers**, Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON 2012), Montreal, Canada, October 25-28, 2012. → *Best Presentation Award*.
- ▶ B. Cougo, J. W. Kolar, G. Ortiz, **Strategies to Reduce Copper Losses in Connections of Medium-Frequency High-**

- Current Converters**, Proceedings of the 37th Annual Conference of the IEEE Industrial Electronics Society (IECON 2011), Melbourne, Australia, November 7-10, 2011.
- ▶ **G. Ortiz**, J. Mühlethaler, J. W. Kolar, "**Magnetic Ear**"- **Based Balancing of Magnetic Flux in High-Power Medium Frequency Dual Active Bridge Converter Transformer Cores**, Proceedings of the 8th International Conference on Power Electronics (ECCE Asia 2011), The Shilla Jeju, Korea, May 30-June 3, 2011.
  - ▶ **G. Ortiz**, A. Müsing, J. Biela, D. Bortis, J. W. Kolar, **A 180MW, 450kV Solid State Modulator Based on Press-Pack IGBT Technology**, Proceedings of the IEEE International Power Modulator and High Voltage Conference (IPMHVC 2010), Atlanta, USA, May 23-27, 2010.
  - ▶ **G. Ortiz**, J. Biela, J. W. Kolar, **Optimized Design of Medium Frequency Transformers with High Isolation Requirements**, Proceedings of the 36th Annual Conference of the IEEE Industrial Electronics Society (IECON 2010), Phoenix, USA, November 7-11, 2010.
  - ▶ **G. Ortiz**, D. Bortis, J. Biela, J. W. Kolar, **Optimal Design of a 3.5kV/11kW DC-DC Converter for Charging Capacitor Banks of Power Modulators**, Proceedings of the IEEE Pulsed Power Conference (PPC 2009), Washington D.C., USA, June 28-July 2, 2009.
  - ▶ A. Müsing, **G. Ortiz**, J. W. Kolar, **Optimization of the Current Distribution in Press-Pack High-Power IGBT Modules**, Invited Paper, Proceedings of the International Power Electronics Conference (ECCE Asia 2010), Sapporo, Japan, June 21-24, 2010.
  - ▶ **G. Ortiz**, J. Biela, D. Bortis, J. W. Kolar, **1 Megawatt, 20kHz, Isolated, Bidirectional 12kV to 1.2kV DC-DC Converter for Renewable Energy Applications**, Proceedings of the International Power Electronics Conference (ECCE Asia 2010), Sapporo, Japan, June 21-24, 2010.  
→ *Best Paper Award*.

- ▶ D. Bortis, J. Biela, G. Ortiz, J. W. Kolar, **Design Procedure for Compact Pulse Transformers with Rectangular Pulse Shape and Fast Rise Times**, Proceedings of the IEEE International Power Modulator and High Voltage Conference (IPMHVC 2010), Atlanta, USA, May 23-27, 2010.

## Journal Papers

- ▶ G. Ortiz, L. Fässler, J. W. Kolar, O. Apeldoorn, **Flux Balancing of Isolation Transformers and Application of the Magnetic Ear for Closed-Loop Volt-Second Compensation**, IEEE Transactions on Power Electronics: Special Issue on High-Frequency-Link Power Conversion Systems, Vol. 29, No. 8, pp. 4078-4090, August 2014.
- ▶ J. W. Kolar, G. Ortiz, **Aktive Verteiltransformatoren - Funktion und Einsatzbereiche in künftigen Smart Grids**, Bulletin SEV/VSE, Jg. 104, Nr. 4, S. 34-40, April 2013.
- ▶ G. Ortiz, H. Uemura, D. Bortis, J. W. Kolar, O. Apeldoorn, **Modeling of Soft-Switching Losses of IGBTs in High-Power High-Efficiency Dual-Active-Bridge DC/DC Converters**, IEEE Transactions on Electron Devices, Vol. 60, No. 2, pp. 587-597, February 2013.
- ▶ G. Ortiz, D. Bortis, J. Biela, J. W. Kolar, **Optimal Design of a 3.5-kV/11-kW DC-DC Converter for Charging Capacitor Banks of Power Modulators**, IEEE Transactions on Plasma Science, vol. 38, no. 10, pp. 2565-2573, October 2010.

## Patents

- ▶ G. Ortiz, J. W. Kolar, **Method for Operating a Converter Bridge**.
- ▶ G. Ortiz, L. Fässler, J. W. Kolar, **Messverfahren und Messvorrichtung zur Induktivitätsmessung bei der Messung einer magnetischen Flussdichte I**.
- ▶ G. Ortiz, L. Fässler, J. W. Kolar, **Messverfahren und Messvorrichtung zur Induktivitätsmessung bei der Messung einer magnetischen Flussdichte II**.

- ▶ J. W. Kolar, G. Ortiz, F. Krismer, **Electrical Converter and Method for its Operation**.
- ▶ J. W. Kolar, J. Mühlethaler, G. Ortiz, **Vorrichtung zur Messung der Flussdichte im Magnetkreis von Mittelfrequenz-Hochleistungstransformatoren**.

## Tutorials and Workshops

- ▶ J. W. Kolar, G. Ortiz, **Solid-State Transformer Concepts in Traction and Smart Grid Applications**, Tutorial at the 39th Annual Conference of the IEEE Industrial Electronics Society (IECON 2013), Vienna, November 10-13, 2013.
- ▶ J. W. Kolar, G. Ortiz, **Solid-State Transformer Concepts in Traction and Smart Grid Applications**, Tutorial at the 4th International Symposium on Power Electronics for Distributed Generation Systems (PEDG 2013), Rogers, Arkansas, USA, July 8-11, 2013.
- ▶ J. W. Kolar, G. Ortiz, **Solid-State Transformer Concepts in Traction and Smart Grid Applications**, Tutorial at the Applied Power Electronics Conference and Exposition (APEC 2013), Long Beach, California, USA, March 17-21, 2013.
- ▶ G. Ortiz, J. Huber, J. W. Kolar, **Intelligent Solid-State Transformers (SSTs) - MEGACube and MEGALink**, ECPE Workshop "Power Electronics in the Electrical Network (Renewables, Energy Storage, Grid Stability)", Kassel, Germany, March, 12-13 2013.
- ▶ J. W. Kolar, G. Ortiz, **Solid-State Transformer Concepts in Traction and Smart Grid Applications**, Tutorial at the 15th International Power Electronics and Motion Control Conference (ECCE Europe 2012), Novi Sad, Serbia, September 4-6, 2012.
- ▶ J. W. Kolar, G. Ortiz, **Intelligent Solid-State Transformers (SSTs) - A Key Building Block of Future Smart Grid Systems**, Tutorial at the 19th China Power Supply Society Conference (CPSSC 2011), Shanghai, China, November 18-21, 2011.

- ▶ G. Ortiz, J. Mühlethaler, J. W. Kolar, **Magnetic Saturation of High Power Medium Frequency Transformers due to Semiconductor On-State Voltage Drop and Switching Time Tolerances**, ECPE Workshop "Parasitic Effects in Power Electronics", Berlin, Germany, 23-24 February, 2011.
- ▶ G. Ortiz, J. Biela, J. W. Kolar, **"MegaCube" – 1MW Ultra Compact/Efficient Isolated 20kHz Bidirectional 12kV/1.2kV DC/DC Converter**, ECPE Workshop "Power Electronics for Energy Efficiency Buildings, Lighting and Home Appliances", RWTH Aachen, Germany, April 15-16, 2010.



# 2

## Topologies and Modulation Schemes

Isolated DC-DC conversion starts by transforming a constant DC voltage into an AC waveform applied to a transformer primary winding, which is magnetically closely coupled to a secondary winding, enabling a highly efficient electromagnetic power transfer. The conversion of this DC into AC voltage is done through arrangements of power semiconductor devices and passive components in bridge configurations. Several bridge arrangements have been considered in the literature for various isolated DC-DC conversion applications, as described in Chapter 1. Focusing on high-power/MF DC-DC conversion, however, the options for bridge structures must be narrowed down mainly due to the following aspects:

1. **Bidirectionality:** In order to be a replacement for LF transformers, SSTs must be able to provide bidirectional power flow, hence their DC-DC stages must be built with active switches on the MV and LV sides. This feature is especially critical in traction solutions since regenerative braking capability is highly desirable.
2. **Isolation:** The requirement of isolation restricts the bridge arrangements only to those which can generate pure AC excitation, resulting in the simplest case in symmetrical bridge configurations.
3. **MV Capability:** In order to deal with the MV level, bridge structures capable of withstanding higher DC voltage levels, e.g. multilevel arrangements, are favored specially for the MV side.
4. **Modulation Flexibility:** As will be experimentally shown in Chapter 3, the combination of MV and MF demands the use

of modulation schemes capable of achieving soft-switching transitions for the semiconductor devices. This constraint is achievable as long as enough degrees of freedom in the bridge components' design and/or flexible modulation schemes are available.

These aspects are taken into account when analyzing suitable bridge structures for the MV as well as for the LV side of the DC-DC stage in the next sections.

## 2.1 Suitable Bridge Structures

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Four bridge structures are considered for the construction of the power electronic bridges; these are: 1) half-bridge with series output capacitor; 2) half-bridge with split DC-link; 3) Full-bridge and 4) NPC (multilevel) bridge. These configurations differ in complexity, namely component count, and functionality, as will be discussed in the following.

### 2.1.1 Half-Bridge with Series Output Capacitor

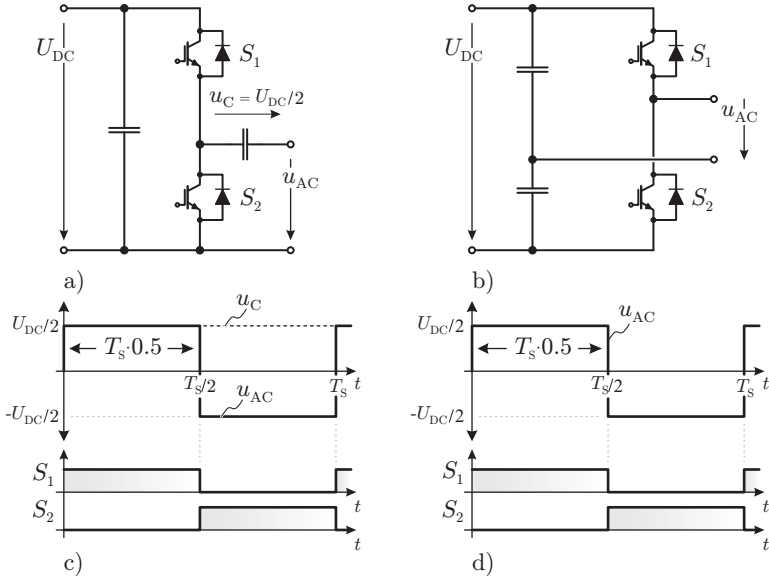
This topology comprises two power semiconductor devices in half-bridge configuration connected to a single DC-link capacitor. Since this structure is incapable of generating pure AC signals on its output, an additional DC-blocking capacitor has to be added to the output, resulting in the structure presented in Fig. 2.1-a). In order to generate a symmetric AC output, switches  $S_1$  and  $S_2$  are operated with 50% duty cycle, as shown in Fig. 2.1-c). This naturally results in a DC voltage across the series output capacitor of  $u_C = U_{DC}/2$ . Given the limited number of active devices, this topology can only generate two output voltage levels and therefore presents reduced modulation scheme possibilities.

The simplicity and low component count of this structure makes it attractive for industry applications as in [17, 44]. Here, the output capacitor was used as part of an LLC filter connected to the MF transformer.

### 2.1.2 Half-Bridge with Split DC-link

An alternative structure with same output voltage waveform is the half-bridge with a split DC-link configuration, shown in Fig. 2.1-b). In this structure, the AC output is generated by dividing the DC-link into





**Figure 2.1:** Half-bridge-based structures capable of bipolar AC voltage generation, i.e. two output voltage levels  $U_{DC}/2$  and  $-U_{DC}/2$  available for  $u_{AC}$ . In a) a half-bridge with series output capacitor configuration is presented while b) presents an alternative half-bridge structure with split DC-link. In c) and d) the respective and idealized gate signals (no interlock delay time considered) are presented.

ideally identical and equally charged (to  $U_{DC}/2$ ) capacitors. One of the output terminals of the bridge corresponds to this mid-point connection of the DC-link capacitors. The output signal is generated by operating switches  $S_1$  and  $S_2$  with 50% duty cycle, obtaining the output voltage displayed in Fig. 2.1-d).

This half-bridge structure has also been adopted by main traction companies [6, 14, 45] due to its low complexity. In all these cases, the lack of flexibility in the modulation, in order to achieve soft-switching commutations, is counteracted by utilization of resonant structures, as will be discussed in Section 2.3.

### 2.1.3 Full-Bridge

The next step in bridge structures is presented by the full-bridge configuration. In this case, four semiconductor devices are arranged as shown in Fig. 2.2-a). The additional bridge leg included in this configuration enables a flexible selection of the duty cycle  $D$  at which the full-bridge operates. This duty cycle is controlled by appropriate adjustment of the semiconductors' switching instants, as shown in Fig. 2.2-c). A free-wheeling interval, where the bridge applies zero volts on its output terminals, results from the controllable duty cycle. This additional degree of freedom proves beneficial for implementation of soft-switching modulations schemes, as will be discussed later in this chapter.

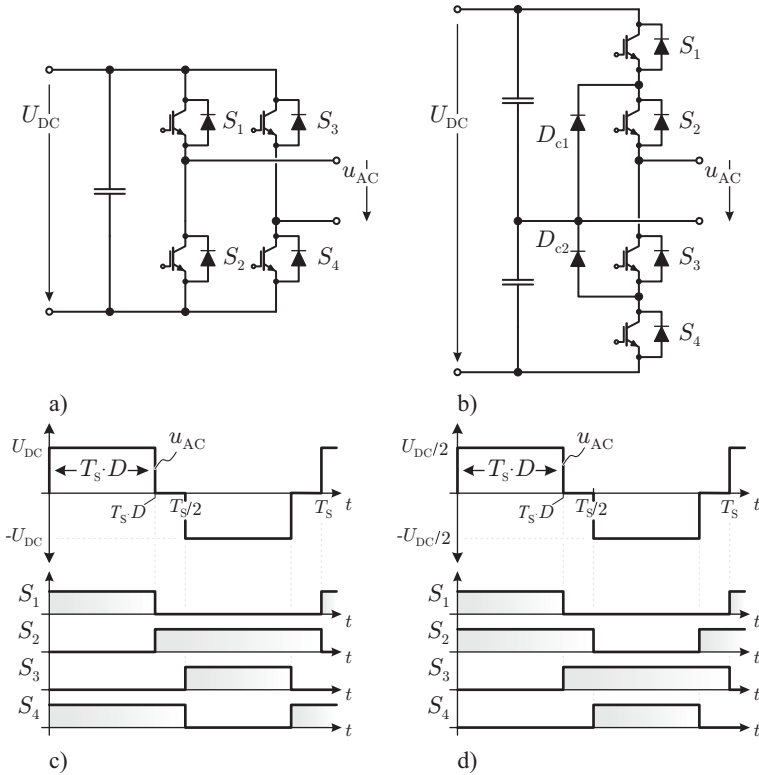
This bridge structure has been very often utilized in traction system developments [12, 13] and also in SST concepts for Smart Grid applications [46–48].

### 2.1.4 NPC (Multilevel)

The NPC bridge leg gave origin to a new breed of power electronic circuits: the multilevel converters. These converters enable the construction of power electronics circuits able to deal with higher voltages, e.g. in the MV range, while still utilizing low voltage devices [49]. Among these multilevel converters, the NPC structure, initially proposed in [50], has been well accepted in industry, where some of the main variable speed drive manufacturers have adopted it as their main solution for MV drives up to several MVAs [51, 52].

The NPC half-bridge leg is also utilized in DC-DC conversion by considering the arrangement shown in Fig. 2.2-b), as proposed in [53]. The basic structure consists of four series-connected devices,  $S_1$  through  $S_4$  and two equally charged (to  $U_{DC}/2$ ) DC-link capacitors in series. During blocking state, diodes  $D_{c1}$  and  $D_{c2}$  ensure that  $S_1$  and  $S_4$  do not block more than  $U_{DC}/2$ , hence enabling the use of lower voltage semiconductors with MV DC-links.

Additionally, the NPC half-bridge structure shown in Fig. 2.2-b) is able to generate a three-level output voltage with adjustable duty cycle  $D$  by controlling the semiconductor devices with the gate signals shown in Fig. 2.2-d). This NPC half-bridge is only able to apply a maximum voltage of  $U_{DC}/2$  on its output (cf. Fig. 2.2-d)), hence for the same transferred power, the current peak value would be twice, in comparison to the full-bridge structure.



**Figure 2.2:** Full-bridge and NPC half-bridge structures capable of unipolar voltage generation (shown in a) and b) respectively), i.e. 3 output levels are available for  $u_{AC}$  as presented together with the respective gate signals in c) and d).

## 2.2 Converter Module Structure Selection

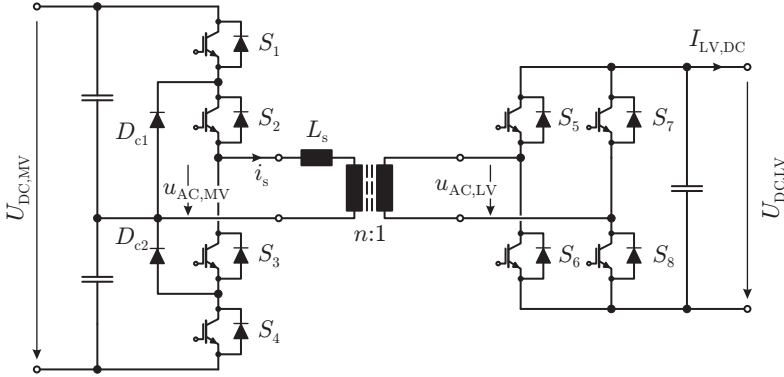
The four presented power electronic bridges would fulfil the requirements for bidirectionality and pure AC voltage output. Among these, however, the NPC half-bridge is favored for the MV side given its capability of dealing with higher DC voltages while still utilizing relatively LV-rated devices. In addition, the NPC half-bridge arrangement as presented in Fig. 2.2-b) is able to generate three output voltage levels (cf. Fig. 2.2-d)), hence complying with the requirement of higher modula-

tion scheme flexibility, a specially critical feature for the MV side semiconductors since soft-switching modulation schemes are mandatory in order to reduce the semiconductors' switching losses (cf. Section 3.3).

As specified earlier, a total MV side voltage of 12 kV is required, which is reached by series connection of converter modules. It is therefore necessary to determine the number of series-connected modules in order to select the appropriate semiconductor technology for the MV side bridge. A low number of modules would be beneficial in order to increase the systems' reliability, assuming that a lower number of modules results in low component count and hence in higher reliability. In order to achieve a low number of modules however, a high voltage blocking capability of each single component would be mandatory, compromising the converter's efficiency if the selected switching frequency is maintained. In case the switching frequency would be reduced in order to reduce the converter's losses, the power density would be compromised. As a consequence, the total number of modules, and hence the voltage blocking capability per MV side switch, results in a trade-off between the complexity of the system and some of its key features such as power density and efficiency. Once the possible soft-switching schemes available for the MV side semiconductors have been analyzed, the decision on the number of modules and therefore on the MV side switch technology will be made.

On the other hand, given the selected voltage level of 1200 V on the LV DC side, it is possible to utilize LV rated devices for the LV side bridge in a full-bridge structure, while the total 1200 V DC voltage is reached by proper series connection of converter modules, similar to the MV side.

The final module structure with the NPC half-bridge leg on the MV side and the full-bridge on the LV side is depicted in Fig. 2.3. The definitive values of the MV side and LV side DC voltages,  $U_{DC,MV}$  and  $U_{DC,LV}$ , will be decided upon the level of modularity, namely the number of modules, that the final converter will be based on. The next section is dedicated to the study of possible soft-switching, namely Zero-Voltage Switching (ZVS) and Zero-Current Switching (ZCS), modulation schemes suitable for high-power DC-DC conversion, which will justify the selection of the semiconductors' voltage level on the MV side and ultimately the number of modules the complete converter will be based on.



**Figure 2.3:** High-power DC-DC converter comprising a NPC half-bridge leg on the MV side and a full-bridge on the LV side. The values for the DC side voltages,  $U_{DC,MV}$  and  $U_{DC,LV}$ , and hence the blocking capability of the single semiconductor devices will be decided once the total number of modules is determined.

## 2.3 Soft-Switching Modulation Schemes

In order to achieve a reasonable level of modularity while still reaching a high efficiency and power density on the DC-DC converters, soft-switching modulation schemes suitable for semiconductor devices in the MV range are desirable and often mandatory. In this voltage and frequency range, IGBTs are the dominating technology due to their good switching performance in comparison to other bipolar power switches. Nevertheless, their minority carrier-based characteristic and the requirement of large n-drift regions in order to block high voltages results in a large amount of charge which is stored during the conduction phase of the semiconductor. This stored charge needs to be evacuated, in the form of a tail current, during the turn-off transition of the device [54]. For this reason, ZVS strategies, do not significantly contribute to the reduction of turn-off losses in IGBTs if snubber capacitors are avoided [55].

It is therefore necessary to consider other types of soft-switching strategies, for reducing the IGBTs' turn-off losses. Since in these devices the turn-off losses are linked to the amount of switched current during

the turn-off process, it is interesting to consider modulation schemes where the amount of switched current during turn-off is minimized or even reduced to zero, finally resulting in a ZCS transition.

Two topologies which allow ZCS modulation schemes are considered: 1) Half-Cycle Discontinuous Conduction Mode Series Resonant Converter (HC-DCM-SRC) and 2) Triangular Current Mode Dual Active Bridge (TCM-DAB). These two topologies differ greatly concerning their basic operation principle, resulting in considerably different features and performances. In order to later quantify the effectiveness of both ZCS modulation strategies, these two converter types will be analyzed in the following.

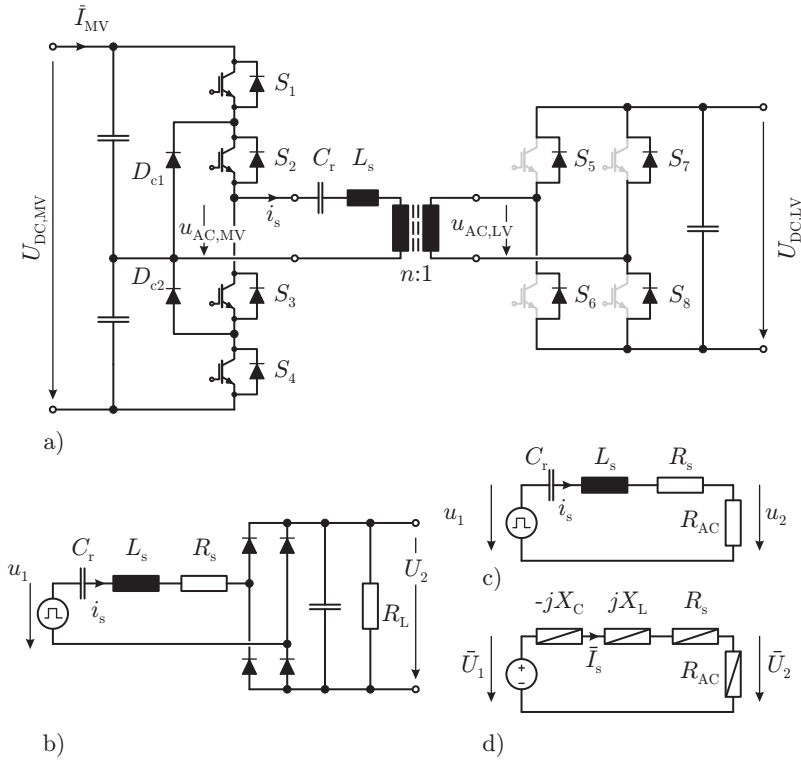
### 2.3.1 Half-Cycle Discontinuous Conduction Mode Series Resonant Converter (HC-DCM-SRC)

Consider the structure presented in Fig. 2.3, where in addition to the inductance  $L_s$ , a capacitor  $C_r$  is placed in series, as shown in Fig. 2.4-a). This combination of a capacitor and an inductor builds a resonant circuit in series to the transformer, hence the complete structure is referred to as Series Resonant Converter (SRC) [56].

The basic principle of this type of converter is to operate the half-bridge which feeds the power actively, thus applying an AC voltage of defined frequency and duty cycle to the transformer, while the rectifying bridge is left uncontrolled, i.e. only diodes are in operation. Under these conditions, the circuit in Fig. 2.4-a) can be simplified as shown in Fig. 2.4-b), for power flow from the MV side to the LV side. Here, the MV side circuit and the transformer are represented by an AC source  $u_1$ , whereby for the NPC half-bridge this amplitude corresponds to  $U_1 = U_{DC,MV}/(2n)$  with  $n$  being the transformer's turns ratio. Additionally, the series resistance  $R_s$ , responsible for the total conduction losses of the circuit, is included in the diagram.

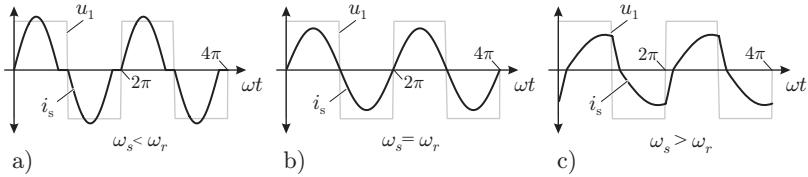
Depending on the ratio between the switching frequency of the converter and the resonant frequency of the resonant tank formed by the series inductor  $L_s$  and series capacitor  $C_r$ , the operating modes of the SRC can be classified into: 1) sub-resonant; 2) resonant and 3) super-resonant, as shown in Fig. 2.5.

In sub-resonant mode, the converter's switching frequency is lower than the resonant tank's resonance frequency. This causes zero current intervals of the waveform  $i_s$  and/or operation of the converter in Dis-



**Figure 2.4:** SRC circuit representations. The complete circuit presented in a) can be simplified to the one shown in b) by considering the MV side bridge and the transformer as single voltage source. On the LV side, the bridge is represented only the rectifying diodes. In order to perform a classical fundamental AC analysis, the complete converter is further simplified to the one shown in c), leading to the fundamental impedance model shown in d).

continuous Conduction Mode (DCM) since, always only one half-cycle of the resonant pulse is conducted until the rectifier diodes on the LV side (provided that the series resonant capacitor voltage is lower than the reflected LV side DC-link voltage [57]) enter blocking state and no current is further conducted until the next half-cycle is initiated. It should be noted that in this operating mode, the switching of the semi-



**Figure 2.5:** Operating modes of the SRC: a) Sub-resonant  $\rightarrow$  converter's switching frequency lower than the resonant frequency of the resonant tank; b) Resonant  $\rightarrow$  converter's switching frequency equal to resonant frequency of the resonant tank; c) Super-resonant  $\rightarrow$  converter's switching frequency higher than the resonant frequency of the resonant tank.

conductors on the powering bridge is done in ZCS conditions, as shown by  $u_1$  in Fig. 2.5-a).

Resonant operating mode is found when the converter's switching frequency is equal to that of the resonant tank. In this limiting case, the power electronic bridge is switched exactly at the zero crossing events of the current  $i_s$ , therefore reaching ZCS transitions for the MV side semiconductors, as shown by  $u_1$  in Fig. 2.5-b).

At super-resonant operation, the converter's switching frequency is higher than the resonant tank's frequency. As shown in Fig. 2.5-c), under this condition the MV side semiconductors do not operate under ZCS, rendering this case less attractive for high-power DC-DC conversion.

The static behavior, namely the transfer ratio  $U_R = U_2/U_1$  between the input and output voltage for the three described operating modes will be now investigated. Assuming that the LV DC side capacitor in Fig. 2.4-b) is large enough in order to neglect the voltage ripple on  $U_2$ , the complete circuit can be represented by its AC fundamental equivalent, as shown in Fig. 2.4-c) and described in [56] where the equivalent AC resistance  $R_{AC}$  is related to the load resistance  $R_L$  through

$$R_{AC} = \frac{8}{\pi^2} R_L. \quad (2.1)$$

With this equivalent circuit, classical AC analysis techniques can be used in order to study the SRC converter. This analysis is valid for switching frequencies above the resonance frequency  $\omega_r$  of the resonant



tank [56]. For switching frequencies below  $\omega_r$ , the rectifying diodes do not operate continuously as shown in Fig. 2.5-a), therefore introducing a non-linearity in the circuit operation which cannot be studied with the classic AC analysis concept.

Since only the fundamental component of  $u_1$  is considered, the impedance model shown in Fig. 2.4-d) is valid. With this circuit, the complex transfer ratio  $\bar{U}_R$  between voltages  $\bar{U}_1$  and  $\bar{U}_2$  can be calculated from

$$\bar{U}_R = \frac{\bar{U}_2}{\bar{U}_1} = \frac{R_{AC}}{R_{AC} + R_s + j \cdot (X_L - X_C)}, \quad (2.2)$$

with

$$X_L = \omega_s L_s \quad (2.3)$$

$$X_C = \frac{1}{\omega_s C_r}. \quad (2.4)$$

In order to generalize the analysis, a per unit system will be utilized with the following power and frequency base values

$$P_N = P_2 = \frac{|\bar{U}_2|^2}{2R_{AC}} \quad (2.5)$$

$$\omega_N = \omega_r = \frac{1}{\sqrt{L_s C_r}}, \quad (2.6)$$

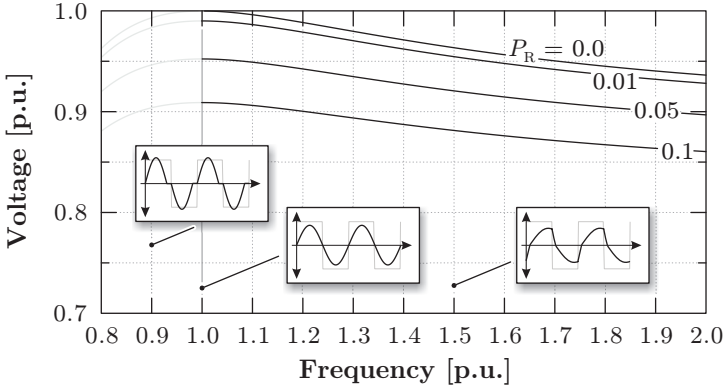
respectively.

It is therefore possible to express the ratio between losses in the series resistance  $R_s$  and the VAR rating of the series inductor  $L_s$  with respect to the base power  $P_N$

$$P_R = \frac{P_s}{P_N} = \frac{|\bar{I}_s|^2 \cdot R_s}{2P_N} \quad (2.7)$$

$$Q_R = \frac{Q_L}{P_N} = \frac{|\bar{I}_s|^2 \cdot X_L}{2P_N}, \quad (2.8)$$

where the current  $\bar{I}_s$  is calculated from



**Figure 2.6:** Dependence of the input/output voltage transfer ratio magnitude  $|\bar{U}_R|$  of the SRC on the normalized frequency  $\omega_R$  for different values of  $P_R$  and constant  $Q_R = 0.5$ .

$$\bar{I}_s = \frac{\bar{U}_2 \left( \frac{1}{\bar{U}_R} - 1 \right)}{R_s + j \cdot (X_L - X_C)}. \quad (2.9)$$

Additionally the ratio  $\omega_R$  between the frequency  $\omega_s$  of the voltage  $u_1$  and the base frequency  $\omega_N$  is expressed as

$$\omega_R = \frac{\omega_s}{\omega_N}. \quad (2.10)$$

By combining equations (2.1) through (2.9), the transfer ratio  $\bar{U}_R$  between input and output voltages  $\bar{U}_1$  and  $\bar{U}_2$  in dependence of the introduced normalized quantities is found:

$$\bar{U}_R = \frac{\bar{U}_2}{\bar{U}_1} = \frac{\omega_R^2}{\omega_R^2 (P_R + 1) + j \cdot Q_R (\omega_R^2 - 1)}. \quad (2.11)$$

It is now interesting to utilize the expression in (2.11) in order to analyze the dependence of the transfer ratio  $\bar{U}_R$  with respect to the normalized parameters  $\omega_R$ ,  $P_R$  and  $Q_R$ , which are intrinsically related to the converter's switching frequency, conduction losses and dimensioning of reactive components respectively.

Fig. 2.6 shows the dependency of the magnitude of  $\bar{U}_R$  with respect to the normalized frequency  $\omega_R$  for different values of  $P_R$  and for a

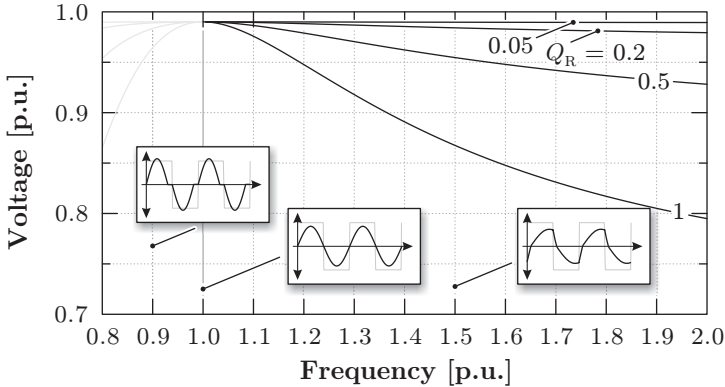
constant  $Q_R = 0.5$ . This value of  $Q_R$  is rather conservative and was selected based on practical realizations. For example, in the hardware implementation of this project, a value of  $Q_R = 0.082$  was reached (cf. Chapter 7) while higher values can be found in e.g. [58] ( $Q_R = 0.14$ ) or in [59] ( $Q_R = 0.32$ ). The effect of lower values of  $Q_R$  in the transfer ratio  $\bar{U}_R$  will be analyzed in more detail later in this section. It should be noted that, as explained earlier, the expression in (2.11) is only valid for values of  $\omega_R \geq 1.0$ , i.e. for switching frequencies above the resonance frequency of the resonant tank (cf. (2.10)).

As shown in Fig. 2.6, for any value of  $P_R$ , the voltage transfer ratio's magnitude  $|\bar{U}_R|$  decreases for increasing frequency. This feature was demonstrated in [56] and is often utilized in order to regulate the output voltage by adjusting the converter's switching frequency.

At  $\omega_R = 1.0$ , i.e. when the converter's switching frequency is equal to the resonant tank's resonance frequency, the highest value for  $|\bar{U}_R|$  is found for any value of  $P_R$ . Moreover, when  $P_R = 0$ , meaning that the series resistance  $R_s$  is negligible or that the output power is zero, leading to zero current through the tank and therefore to no losses in  $R_s$ , a unity transfer ratio is reached, i.e.  $|\bar{U}_2| = |\bar{U}_1|$ .

In a practical case, however, the series resistance  $R_s$  has a non-zero value and therefore the value of  $P_R$  is higher than zero, resulting in a drop of the voltage transfer ratio when non-zero power is transferred, as shown in Fig. 2.6 for  $P_R > 0$ . Nevertheless, when  $P_R = 0.1$ , meaning that 10 % of the output power is being dissipated in the series resistance  $R_s$ , the voltage transfer ratio remains over 0.9. In a more realistic case, the value of  $P_R$  at nominal power would be in the range of  $P_R = 0.01$  in order to ensure a high converter efficiency. As a consequence, considering a highly-efficient design and when operated at resonance frequency, the SRC features a voltage transfer ratio  $|\bar{U}_R| \approx 1.0$  independent of the transferred power.

In order to investigate the behavior of the voltage transfer ratio concerning variations in  $Q_R$ , Fig. 2.7 shows its dependence with respect to the normalized frequency  $\omega_R$  for different values of  $Q_R$  and constant  $P_R = 0.01$ . Above resonance frequency ( $\omega_R > 1.0$ ), increasing the value of  $Q_R$  increases the sensitivity of the voltage transfer ratio with respect to the frequency, which could be used to adjust the gain of the system in case a variable frequency control is desired. As explained earlier, however, in this super-resonant condition, the semiconductors do not operate under ZCS, thus this operating mode will not be further



**Figure 2.7:** Dependence of the input/output voltage transfer ratio  $|\bar{U}_R|$  of the SRC on the normalized frequency  $\omega_R$  for different values of  $Q_R$  and constant  $P_R = 0.01$ .

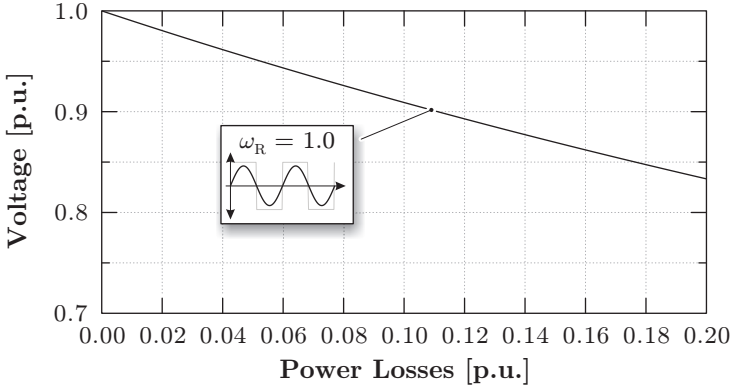
analyzed.

At switching frequency equal to resonance frequency, i.e.  $\omega_R = 1.0$ , the transfer ratio is determined by the value of  $P_R$ , which was fixed to  $P_R = 0.01$  for Fig. 2.7, regardless of the value of  $Q_R$ . This phenomenon can be also seen in (2.11), where by inserting  $\omega_R = 1.0$ , the complete expression is simplified to

$$\bar{U}_R = \frac{\bar{U}_2}{\bar{U}_1} = \frac{1}{P_R + 1}. \quad (2.12)$$

The expression in (2.12) reveals another feature of the SRC: regardless of the specific values of the series inductor  $L_s$  and capacitor  $C_r$ , when operated at resonant frequency, the voltage transfer ratio  $|\bar{U}_R|$  is only determined by the value of  $P_R$ , i.e. by the series resistance  $R_s$  and the amount of transferred power. This phenomenon is quantitatively depicted in Fig. 2.8 where the voltage transfer ratio is shown in dependence of the ratio  $P_R$  for  $\omega_R = 1.0$ . As can be seen, the voltage transfer ratio stays above 0.9 for values of  $P_R$  below 0.1. As mentioned earlier, however, in a realistic case, only 1 to 2% of losses would be allowed in the series resistance  $R_s$  at nominal power, leading to values of  $P_R$  well below 2% and therefore to a transfer ratio close to unity.

The previous studies utilized AC analysis tools in order to elaborate the expression in (2.11), which describes the voltage transfer ratio of



**Figure 2.8:** Dependence of the input/output voltage ratio  $|\bar{U}_R|$  of the SRC on the conduction losses to output power ratio  $P_R$  for  $\omega_R = 1.0$ . At this frequency the transfer ratio does not depend on  $Q_R$  (cf. (2.12)).

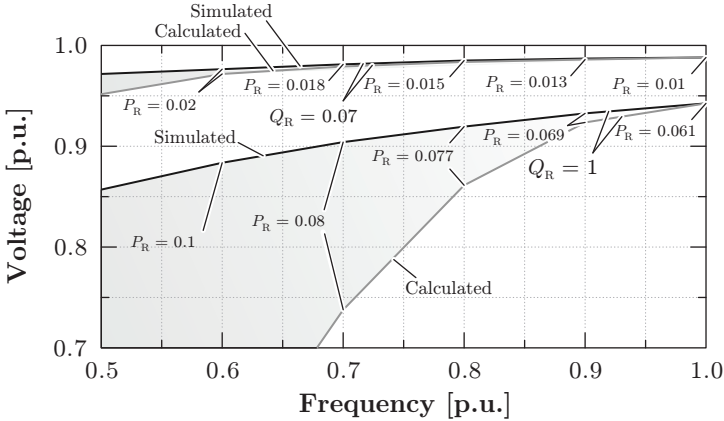
the SRC for operation at super-resonance. Since at sub-resonant conditions these tools are no longer valid, a series of simulations utilizing Gecko Research simulation software [60] with values for the normalized quantities in the ranges

$$\begin{aligned}\omega_R &= \{0.5 \dots 1.0\} \\ P_R &= \{0.01 \dots 0.1\}\end{aligned}$$

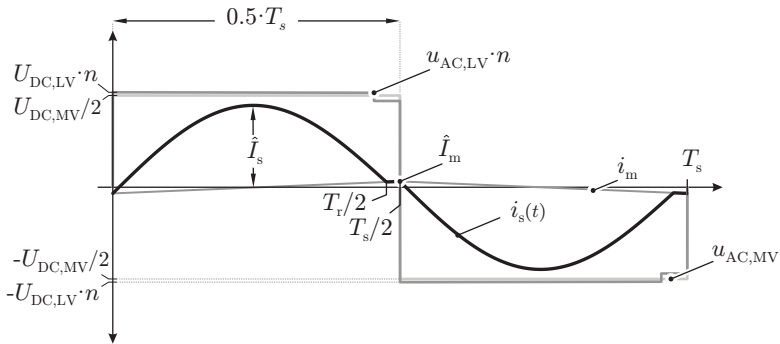
were conducted. Two values for  $Q_R$  were selected:  $Q_R = 0.07$  and  $Q_R = 1$  following typical values of practical realizations as stated earlier.

The results of these simulations are presented in Fig. 2.9, whereby the respective analytical values are also shown. As can be seen, close to resonant operation, simulated and calculated results agree very well. At lower operating frequencies however, the calculated values differ significantly from the simulations, proving that the AC analysis is not valid in this range. In addition, the simulated results show that the SRC also achieves a high transfer ratio  $|\bar{U}_R|$  at sub-resonant operation for the lower value of  $Q_R = 0.7$  even at frequencies as low as  $\omega_R = 0.5$  (switching frequency two times lower than resonance frequency).

Before a final time domain expression for the current through the transformer can be provided, one additional aspect must be considered



**Figure 2.9:** Dependence of the input/output voltage transfer ratio  $|\bar{U}_R|$  of the SRC on the normalized frequency in the sub-resonant range  $\omega_R = \{0.5 \dots 1.0\}$  obtained through comprehensive simulation with values of  $P_R$  in the range  $P_R = \{0.01 \dots 0.1\}$  and for  $Q_R = 0.07$  and  $Q_R = 1$ .



**Figure 2.10:** Operation of the HC-DCM-SRC with increased magnetizing current in order to achieve soft-switching transitions, as explained in Chapter 3.

in the analysis of the SRC: the utilization of the magnetizing current  $i_m$  in order to achieve soft-switching transitions in the driving IGBTs (cf. Chapter 3). The utilization of this degree of freedom, however, modifies the current waveform through the transformer, as shown in

Fig. 2.10, whereby the resonant pulse is now superimposed with the magnetizing current  $i_m$ . As soon as the resonant pulse is over, the rectifying diodes on the LV side (for power transfer from MV to LV side) no longer conduct, originating a time interval (between  $T_s/2$  and  $T_r/2$  in Fig. 2.10) where only a linearly increasing magnetizing current flows through the MV side switches.

It is now interesting to find an expression for the current through the transformer  $i_s$  for a given power level and a given magnetizing current in order to later dimension the semiconductor devices and the transformer copper conductors. For this, first the expression for the transformer current  $i_s$  during one switching period is found

$$i_s(t) = \begin{cases} \hat{I} \sin(\omega_r t) + \frac{4\hat{I}_m}{T_s} t - \hat{I}_m & 0 \leq t < \frac{T_r}{2} \\ \frac{4\hat{I}_m}{T_s} t - \hat{I}_m & \frac{T_r}{2} \leq t < \frac{T_s}{2} \\ -\hat{I} \sin(\omega_r(t - \frac{T_s}{2})) - \frac{4\hat{I}_m}{T_s}(t - \frac{T_s}{2}) + \hat{I}_m & \frac{T_s}{2} \leq t < \frac{T_s}{2} + \frac{T_r}{2} \\ -\frac{4\hat{I}_m}{T_s}(t - \frac{T_s}{2}) + \hat{I}_m & \frac{T_s}{2} + \frac{T_r}{2} \leq t < T_s, \end{cases} \quad (2.13)$$

where  $\hat{I}_s$  is the peak resonant current value through the transformer and  $\hat{I}_m$  is the peak magnetizing current at the end of one half switching cycle (cf. Fig. 2.10). The average current  $\bar{I}_{MV}$  at the MV side DC-link is calculated from

$$\bar{I}_{MV} = \frac{1}{2} \left( \frac{2}{T_s} \int_0^{T_s/2} i_s(t) \cdot dt \right) = \hat{I}_s \cdot \frac{T_r}{\pi T_s}, \quad (2.14)$$

where the  $\frac{1}{2}$  is introduced in order to account for the NPC half-bridge construction on the MV side.

With the expression in (2.14), the power supplied at the MV side DC-link,  $P_T = U_{MV} \cdot \bar{I}_{MV}$ , can be calculated, whereby solving for the peak current  $\hat{I}_s$  corresponds to

$$\hat{I}_s = \frac{P_T}{U_{MV}} \cdot \frac{T_s}{T_r} \pi. \quad (2.15)$$

From (2.15), the peak current  $\hat{I}_s$  can be calculated for a given power  $P_T$  and a given set of circuit parameters. Together with the expression in (2.13), this value of peak current  $\hat{I}_s$  is used to calculate the values for RMS and average current in the semiconductor devices and the transformer windings in the subsequent chapters.

The aforementioned features render the SRC operated in sub-resonant mode very attractive for high-power DC-DC applications, since no feedback loops are required in order to maintain a good regulation of the output voltage, while ensuring that all switching transitions are performed under ZCS conditions. Given the operation of this SRC under discontinuous current over one half switching cycle, it is often referred to as HC-DCM-SRC [61].

The first practical utilization of the HC-DCM-SRC was reported in [58] for transferring energy through the joints of robot arms. Also in this publication, the dynamic behavior of the converter was analyzed utilizing a simple equivalent circuit, where the transient behavior of the currents and voltages can be analyzed.

The first application for SSTs in traction was reported by ABB in [12] where mainly the ZCS behavior of the utilized IGBT switches was investigated. Bombardier and Alstom Transport also reported the utilization of this converter in [45] and [13] respectively, where other aspects such as isolation, electromagnetic compatibility, control schemes and mechanical arrangement were covered. Siemens in collaboration with their University Partner reported the utilization of this topology for their traction solutions in [14, 44] covering a broad range of topics such as ZCS behavior of the IGBTs, optimized frequency selection, MF transformer design and test bench concept, among others.

More recently, ABB published results on a fully-operational prototype comprising the complete traction solution, which was commissioned for the Swiss Federal Railways in 2012 [17, 59, 62]. Other recent publications [15, 63] further analyzed the ZCS behavior of the IGBTs and the optimization of the system.

The HC-DCM-SRC has been considered for Smart Grid applications in [64, 65] where also a three-phase variation was studied.

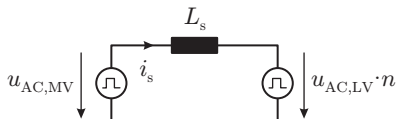
The main drawback of the HC-DCM-SRC is its incapability of controlling the power throughput since, in order to operate in DCM while achieving ZCS, the active bridge must be operated without duty cycle control. This disadvantage restricts the utilization of the HC-DCM-SRC to applications where tight input/output voltage ranges are required or where the voltage regulation can be done by other stages of the SST. In applications where these requirements are not fulfilled, other converters which achieve ZCS transitions while being able to actively control the power flow result more attractive, as will be discussed in the next section.



### 2.3.2 Triangular Current Mode Dual Active Bridge (TCM-DAB)

In case power transfer control is required while still keeping ZCS transitions at least for the MV side of the converter, the DAB presents an interesting option. The first form of DAB converter was introduced for direct AC-AC conversion already in the seventies in order to link two AC networks through a flexible interface [66] (cf. Appendix A). For DC-DC conversion, the DAB operated only with phase-shift modulation was proposed in [67] and is characterized by two AC voltage sources interfaced by an inductor and a transformer.

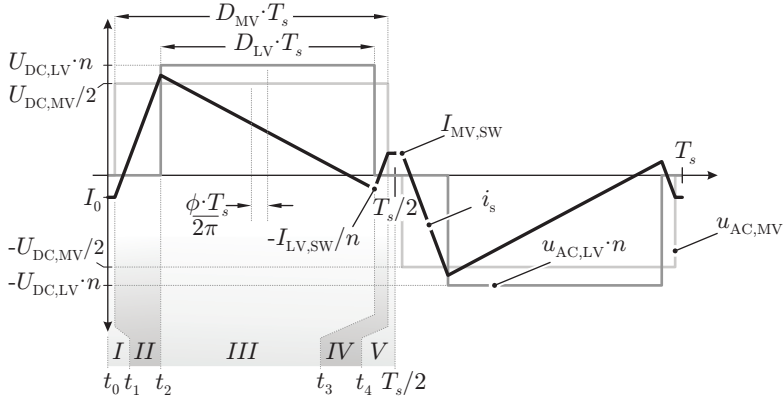
In its original conception, the DAB consisted of two full-bridge structures (cf. Fig. 2.2-a)) on the MV and the LV side. However, the DAB can be also built with an NPC half-bridge structure on the MV side (cf. Fig. 2.3), given its capability to control the duty cycle of the output voltage. This arrangement, besides the possibility of phase-shifting the voltage waveforms of the LV and MV sides, is able to freely adjust the duty cycles of the MV and LV side voltage waveforms, as explained in Section 2, resulting in a total of three degrees of freedom for the control of the DAB: the phase-shift  $\phi$ ; the MV side duty cycle  $D_{MV}$  and the LV side duty cycle  $D_{LV}$ .



**Figure 2.11:** Equivalent DAB circuit considering an ideal transformer. The MV and LV side converters have been condensed into AC voltage sources supplying square-shaped voltage sources.

One of these control parameters, often the phase-shift  $\phi$ , is adjusted in order to transfer the required amount of power, while the MV and LV side duty cycles are available for optimization of other converter features. As an example, in [68], the exact values for these three control parameters which minimize the converter's RMS currents were found, leading to various operating modes for the different power/voltage levels.

Considering applications with semiconductor devices in the MV range, it results attractive to utilize the additional degrees of freedom



**Figure 2.12:** Current and voltage waveforms for a DAB operated under TCM and power transfer from MV to LV side. Here, the general case for this type of modulation, with non-zero switched current is presented.

of the DAB in order to achieve soft-switching transitions, namely ZCS, at least for the MV side semiconductors. This behavior can be achieved by implementing a TCM modulation scheme in the DAB, as proposed in [69]. This type of modulation consists of shifting all current switching events to the LV side converter, where semiconductors with better switching performance can be utilized.

In order to describe the operating principle of this modulation, consider the simplified circuit of the DAB shown in Fig. 2.11, where the MV and LV power electronic circuits have been replaced by ideal three-level, voltage sources applying square-shaped voltages  $u_{AC,MV}$  and  $u_{AC,LV} \cdot n$  to the transformer terminals. The difference between these two voltages appears across the series inductor  $L_s$  whereby, together with the value of this inductor, they define the slope of the current  $i_s$ .

The general case for the voltage and current waveforms in TCM are presented in Fig. 2.12 for power transferred from the MV to the LV side. In this waveform, the general case with non-zero current being switched on both sides, i.e. on the MV and the LV side, corresponding to  $I_{MV,SW}$  and  $I_{LV,SW}$ , is presented. The case when exact ZCS transitions are desired will be treated as a special condition after the general solution is found.

The following detailed description, based on the time intervals de-

defined in Fig. 2.12 is valid for the first half-cycle:

► **Interval I**

Both MV and LV side bridges apply zero voltage on their respective outputs, leading to a complete freewheeling state where the current  $i_s$  remains constant and equal to  $I_0$  as at the end of the previous switching cycle.

► **Interval II**

The MV side converter applies positive voltage  $U_{DC,MV}/2$  on its output while the LV side bridge is kept in freewheeling state. The full MV side voltage is therefore applied to the inductor, causing the current  $i_s$  to linearly increase.

► **Interval III**

The LV side is switched and applies  $U_{DC,LV}$ , i.e. a positive voltage on its output, leading to  $U_{DC,LV} \cdot n$  at the MV side of the transformer. Accordingly, now the difference of the voltages applied from the MV and the LV side,  $U_{DC,MV}/2$  and  $U_{DC,LV} \cdot n$ , occurs across the inductor. Since the aim of this modulation is finally to achieve ZCS on the MV side, during this time interval the current must change its slope in order to approach zero before the switching event occurs on the MV side. This change in sign of the slope results in the following restriction for the transformer's turns ratio  $n$ :

$$U_{DC,LV} \cdot n > U_{DC,MV}/2 \quad \Rightarrow \quad n > \frac{U_{DC,MV}}{2 \cdot U_{DC,LV}}. \quad (2.16)$$

This condition is necessary but not sufficient for ZCS. The precise values of all remaining converter design and control parameters must be determined in order to ensure ZCS transitions.

► **Interval IV**

The LV side is switched back to freewheeling whereby the MV side is left applying full voltage on its output, increasing linearly the value of the current  $i_s$ .

► **Interval V**

The MV side bridge is switched to freewheeling, applying zero volts on its output. Since now both MV and LV bridges apply zero volts, the current remains constant until the end of the positive

semi-cycle when the analogous process is initiated for the negative semi-cycle.

The behavior of the current  $i_s$  during the previously described time intervals is represented by piecewise linear functions containing the different initial values for each time interval and the corresponding current slopes defined by the applied voltages and the value of the series inductor  $L_s$ . The time instants  $t_0$  through  $t_4$  introduced in Fig. 2.12 are utilized to describe the current  $i_s$  in each of these time intervals

$$i_{s1}(t) = I_0 \quad (2.17)$$

$$i_{s2}(t) = i_{s1}(t_1) - \frac{U_{\text{DC,MV}}}{2} \frac{1}{L_s} \cdot (t - t_1) \quad (2.18)$$

$$i_{s3}(t) = i_{s2}(t_2) + \left( U_{\text{DC,LV}} \cdot n - \frac{U_{\text{DC,MV}}}{2} \right) \frac{1}{L_s} \cdot (t - t_2) \quad (2.19)$$

$$i_{s4}(t) = i_{s3}(t_3) - \frac{U_{\text{DC,MV}}}{2} \frac{1}{L_s} \cdot (t - t_3) \quad (2.20)$$

$$i_{s5}(t) = i_{s4}(t_4). \quad (2.21)$$

Since pure AC excitation is assumed on the transformer terminals, the current  $i_s$  has a symmetrical behavior during the positive and negative semicycles, which is expressed by

$$i_{s1}(t_0) = -i_{s5}(T_s/2), \quad (2.22)$$

from where the value of the current  $I_0$  at the beginning of the positive switching period is found:

$$I_0 = \frac{1}{4} \cdot \frac{U_{\text{MV}}(t_4 - t_1) - 2n \cdot U_{\text{LV}}(t_3 - t_2)}{L_s}. \quad (2.23)$$

In addition, the time values  $t_0$  through  $t_4$  are depending on the control signals  $\phi$ ,  $D_{\text{MV}}$  and  $D_{\text{LV}}$  through

$$t_0 = 0 \quad (2.24)$$

$$t_1 = \frac{T_s}{2} \left( \frac{1}{2} - D_{MV} \right) \quad (2.25)$$

$$t_2 = t_1 + \left( \frac{D_{MV} - D_{LV}}{2} - \frac{\phi}{2\pi} \right) \cdot T_s = \frac{T_s}{2} \left( D_{LV} + \frac{\phi}{\pi} - \frac{1}{2} \right) \quad (2.26)$$

$$t_3 = t_2 + D_{LV} \cdot T_s = \frac{T_s}{2} \left( \frac{1}{2} + D_{LV} - \frac{\phi}{\pi} \right) \quad (2.27)$$

$$t_4 = t_1 + D_{MV} \cdot T_s = \frac{T_s}{2} \left( \frac{1}{2} + D_{MV} \right), \quad (2.28)$$

where  $T_s = 1/f_s$  corresponds to the switching period.

With the definitions for the currents made in (2.17) - (2.21) in each of the time intervals and the relations between time instants  $t_0$  through  $t_4$  and the DAB's control signals, the following piecewise linear function, which describes the behavior of the current  $i_s$  through the transformer for the considered operating mode during the positive half-cycle, is assembled

$$i_s(t) = \begin{cases} \frac{U_{MV}(t_4-t_1)-2n \cdot U_{LV}(t_3-t_2)}{4L_s} & t_0 \leq t < t_1 \\ \frac{U_{MV}(t_4+t_1)-2n \cdot U_{LV}(t_3-t_2)}{4L_s} - \frac{U_{MV}}{2L_s} \cdot t & t_1 \leq t < t_2 \\ \frac{U_{MV}(t_4+t_1)-2n \cdot U_{LV}(t_3+t_2)}{4L_s} + \frac{2n \cdot U_{LV}-U_{MV}}{2L_s} \cdot t & t_2 \leq t < t_3 \\ \frac{U_{MV}(t_4+t_1)+2n \cdot U_{LV}(t_3-t_2)}{4L_s} - \frac{U_{MV}}{2L_s} \cdot t & t_3 \leq t < t_4 \\ -\frac{U_{MV}(t_4-t_1)-2n \cdot U_{LV}(t_3-t_2)}{4L_s} & t_4 \leq t < \frac{T_s}{2}. \end{cases} \quad (2.29)$$

With the expression in (2.29) and the defined time instants  $t_0$  through  $t_4$ , the current  $i_s$  is described as a function of the operating voltages  $U_{MV}$  and  $U_{LV}$ , transformer turns ratio  $n$ , series inductance  $L_s$  and the DAB control signals  $\phi$ ,  $D_{MV}$  and  $D_{LV}$ .

The goal is now to find the expressions of these three control signals which result in the desired power transfer  $P_T$  and switched currents on the MV and LV sides:  $I_{MV,SW}$  and  $I_{LV,SW}$  respectively. In order to calculate the power transferred from the MV to the LV side, the average value  $I_{LV,DC}$  of the LV side rectified current (cf. Fig. 2.3) is determined,

$$I_{LV} = \frac{2n}{T_s} \int_{t_2}^{t_3} i_s(t) \cdot dt = \frac{1}{2} \cdot \frac{nT_s D_{LV} U_{MV} \phi}{\pi L_s}; \quad (2.30)$$

the total power transferred to the LV side DC-link then results as

$$P_T = I_{LV} \cdot U_{LV} = \frac{1}{2} \cdot \frac{nT_s D_{LV} U_{MV} U_{LV} \phi}{\pi L_s}. \quad (2.31)$$

On the other hand, the required values of switched currents  $I_{MV,SW}$  and  $I_{LV,SW}$  are translated into the following restrictions (cf. Fig. 2.12):

$$i_s(t_4) = I_{MV,SW} \quad (2.32)$$

$$i_s(t_3) = -I_{LV,SW}/n. \quad (2.33)$$

The expressions in (2.31), (2.32) and (2.33) constitute a system of three equations where the values for the control signals  $\phi$ ,  $D_{MV}$  and  $D_{LV}$  are unknowns. Solving these equations for the control parameters and disregarding physically non-meaningful solutions gives

$$\phi = \frac{2\pi P_T L_s (2n \cdot U_{LV} - U_{MV})}{A \cdot U_{MV}} \quad (2.34)$$

$$D_{LV} = \frac{A}{T_s U_{LV} n (2n \cdot U_{LV} - U_{MV})} \quad (2.35)$$

$$D_{MV} = \frac{2(2I_{MV,SW} L_s (2n \cdot U_{LV} - U_{MV}) + A)}{T_s U_{MV} (2n \cdot U_{LV} - U_{MV})}, \quad (2.36)$$

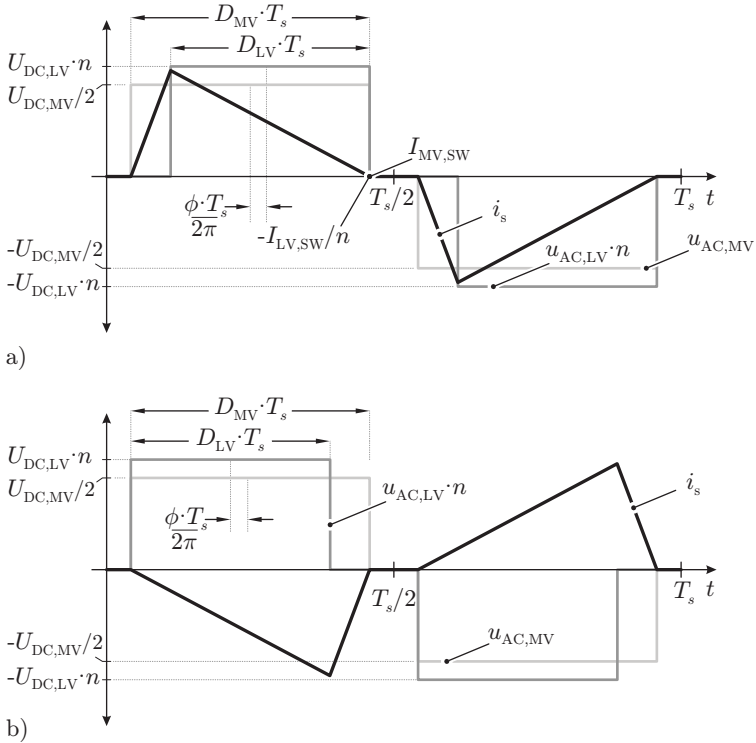
where

$$A = 2I_{LV,SW} U_{LV} L_s + \sqrt{2U_{LV} L_s (2I_{LV,SW}^2 U_{LV} L_s + 2P_T T_s U_{LV} n^2 - P_T T_s U_{MV} n)}. \quad (2.37)$$

These expressions constitute the solution for arbitrary values of switched currents  $I_{MV,SW}$  and  $I_{LV,SW}$ . The special case of pure ZCS is defined as

$$I_{MV,SW} = 0 \quad (2.38)$$

$$I_{LV,SW} = 0. \quad (2.39)$$



**Figure 2.13:** Current and voltage waveforms for DAB operated under TCM and pure ZCS operation; a) Power transfer from MV to LV side; b) Power transfer from LV to MV side.

This case is shown in Fig. 2.13-a) for power transfer from MV to LV side, whereby the new simplified equations for the control signals  $\phi$ ,  $D_{MV}$  and  $D_{LV}$  are

$$\phi = \frac{\sqrt{2}\pi P_T L_s (2n \cdot U_{LV} - U_{MV})}{(\sqrt{U_{LV} L_s P_T T_s n (2n \cdot U_{LV} - U_{MV})}) \cdot U_{MV}} \quad (2.40)$$

$$D_{LV} = \frac{\sqrt{2U_{LV} L_s P_T T_s n (2n \cdot U_{LV} - P_T T_s U_{MV})}}{T_s U_{LV} n (2n \cdot U_{LV} - U_{MV})} \quad (2.41)$$

$$D_{MV} = \frac{2\sqrt{2U_{LV} L_s P_T T_s n (2n \cdot U_{LV} - P_T T_s U_{MV})}}{T_s U_{MV} (2n \cdot U_{LV} - U_{MV})}. \quad (2.42)$$

The TCM-DAB converter is able to operate in bidirectional power transfer mode. Until now only the case with power transfer from the MV to the LV side was analyzed. In Fig. 2.13-b), the current shape for power transfer in the reverse direction, i.e. from the LV to the MV side, is presented. It should be noted that the aforementioned set of equations for the calculation of  $\phi$ ,  $D_{LV}$  and  $D_{MV}$  for the pure ZCS as well as for non-zero switched current are still valid, i.e. only an inversion of the sign of  $\phi$ , meaning a change in the sign of  $P_T$  is required in order to reverse the power direction.

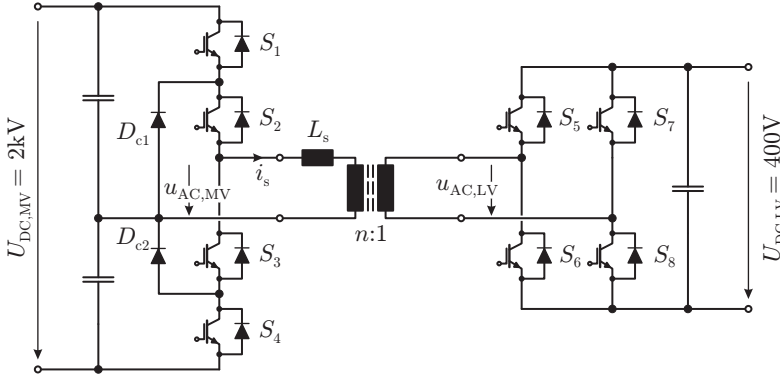
It may result intuitive to select the case of pure ZCS instead of the non-ZCS or Quasi ZCS (QZCS) operation since switching losses are generally intuitively related to the amount of switched current. As will be shown in the next chapter however, QZCS helps achieve soft turn-on transitions for the MV and the LV side semiconductors thus helping to improve the converter's efficiency. In order to quantify this improvement, the precise values of module power/and voltage levels, which lead to specific semiconductor technologies, must be defined and will be discussed in the next section.

## 2.4 Converter Module Power/Voltage Rating Selection

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As mentioned earlier, the total number of modules results in a trade-off between the complexity of the system and some of its key features such as power density and efficiency. Since a switching frequency of  $f_s = 20$  kHz is aimed for, 1.7 kV power semiconductors are selected for the MV side NPC half-bridge leg, since, by employing the presented soft-switching techniques, this desired switching frequency can be reached without compromising the converter's efficiency/power density, as will be shown





**Figure 2.14:** High-power DC-DC converter comprising a NPC half-bridge on the MV side and a full-bridge on the LV side. Typically capacitors (not shown in the figure) are additionally connected in series to the MV and LV windings in order to operate the magnetic core under balanced conditions (cf Chapter 6).

in Chapter 7 of this thesis. With this blocking capability, converter modules with an MV side DC-link voltage of  $U_{DC,MV} = 2\text{kV}$  can be built, whereby each semiconductor device blocks 1kV. This way, the number of series-connected modules is fixed to 6 with a power per module of  $P_N = 1\text{ MW}/6 = 166\text{ kW}$ .

In case of the LV side, lower-voltage semiconductor devices are available for the construction of the described full-bridge structure. Semiconductor devices of the 600 V class are considered since switch technologies in this voltage level are characterized by outstanding conduction and switching capabilities, whereby majority and minority carrier-based semiconductor technologies (MOSFETs and IGBTs respectively) coexist in this range, widening the range of available switch options. For these reasons, a full-bridge structure with  $U_{DC,LV} = 400\text{ V}$  DC-link voltage comprising 600 V semiconductor devices is selected for the LV side power electronics.

The complete 166 kW converter module comprising a  $U_{DC,MV} = 2\text{kV}$  MV side DC-link, a  $U_{DC,LV} = 400\text{ V}$  LV side DC-link and the linking MF transformer is presented in Fig. 2.14. A total number of 6 units is required to achieve the initially specified 1 MW converter. These 6 converter modules are connected in series on the MV side,

building up the total  $U_{\text{DC,MV,T}} = 12 \text{ kV}$ , as shown in Fig. 2.15. The total  $U_{\text{DC,LV,T}} = 1.2 \text{ kV}$  voltage level on the LV side is achieved through a combination of series and parallel connection, as can be also seen in Fig. 2.15.

Each converter module of the structure presented in Fig. 2.15 can be subdivided into three main parts: the MV side NPC half-bridge; the LV side full-bridge and the MF transformer. These three parts of the converter module will be independently treated in the following chapters, where all modelling and design details will be covered, once the reference specifications for HC-DCM-SRC and TCM-DAB operation are defined in the next section.

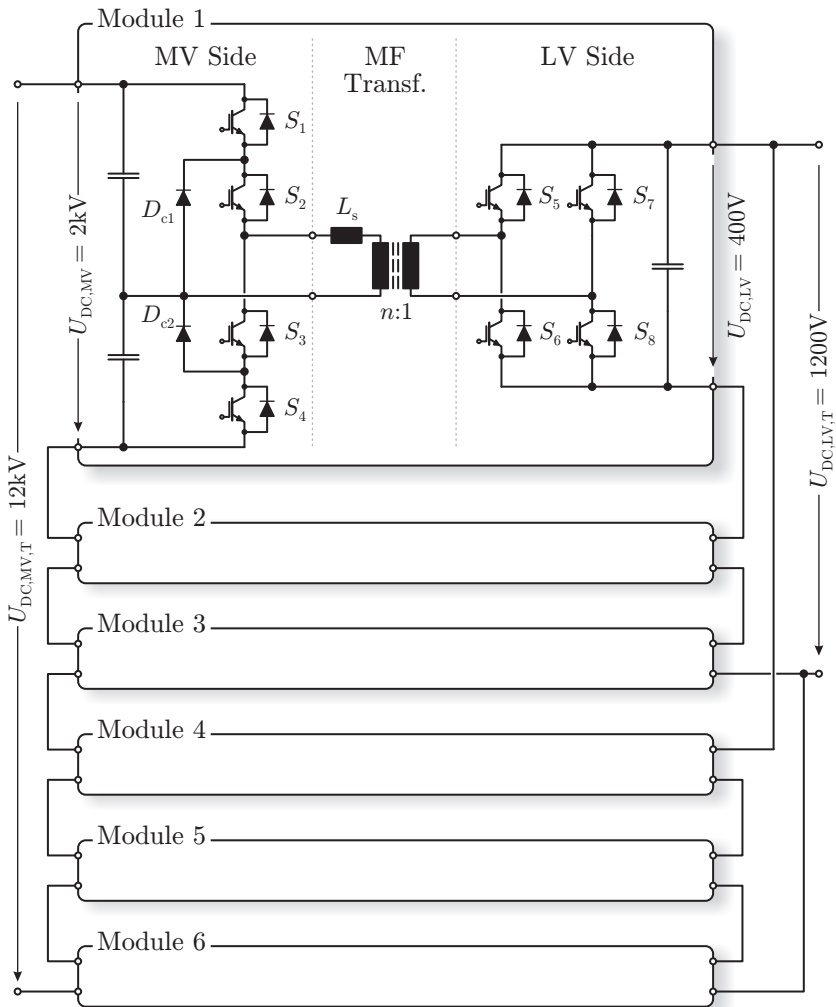
### 2.4.1 Converter Module Specifications

In order to proceed with the design of each of the aforementioned converter module parts, the reference specifications for the two alternative converter types must be defined.

The specified nominal power, switching frequency and voltage levels are shown in Table. 2.1 for both of these converters. In the case of the HC-DCM-SRC, the turns ratio is defined, as described earlier in this chapter, by the input to output voltage transfer ratio, i.e.  $n = N_{\text{MV}}/N_{\text{LV}} = U_{\text{MV}}/U_{\text{LV}} = 5 : 2$ . The series inductance must be in this case minimized in order to improve the converter's dynamic performance [58]. Together with the series resonant capacitor  $C_r$ , this inductor defines the value of the resonant frequency  $f_r$ . For the calculation of the reference values shown in Table. 2.1, the resonant frequency is chosen equal to the switching frequency, i.e.  $f_r = f_s$ .

For the TCM-DAB, the turns ratio is a free parameter. Due to practical construction issues which will be covered in Chapter 5, it is convenient to select the turns ratio of the transformer equal to  $n = N_{\text{MV}}/N_{\text{LV}} = 3 : 1$  in order to simplify the transformer construction. With this value selected, the value of series inductance must not exceed  $L_s = 11 \mu\text{H}$  in order to be able to transfer nominal power while keeping a safe operational margin. The peak current values for the TCM-DAB are calculated considering pure ZCS.

The specifications presented in Table 2.1 are reference values utilized to initiate the modules' design and will vary as new considerations are taken into account during the description of the practical realization. Other values specific for each converter module part, such as semicon-



**Figure 2.15:** Full-scale 1 MW modular converter comprising six series connected modules on the MV side which are parallel-/series-connected on the LV side. Each module is designed for 166 kW/20 kHz linking a 2 kV MV DC-link to a 400 V LV DC-link.

**Table 2.1:** Reference values for the design of the HC-DCM-SRC and TCM-DAB converters.

Parameter	HC-DCM-SRC	TCM-DAB
Nominal power $P_N$	166 kW	
Operating frequency $f_s$	20 kHz	
MV side voltage $U_{MV}$	2 kV	
LV side voltage $U_{LV}$	400 V	
Turns ratio $n = N_{MV}/N_{LV}$	5 : 2	3 : 1
Series inductance $L_s$ (MV side)	<i>min.</i>	11 $\mu$ H
Resonant frequency $f_r$	20 kHz	–
MV side peak current $\hat{I}_{s,MV}$	273 A	354 A
LV side peak current $\hat{I}_{s,LV}$	684 A	1063 A

ductors' or capacitors RMS current values, will be presented once the respective components' selection is covered in the next chapters.

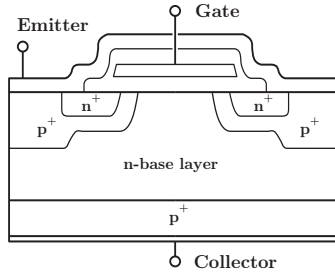
# 3

## Medium Voltage Side Power Electronics

In the previous chapter, modulation schemes that achieve ZCS transitions, at least on the MV side of the DC-DC converter were introduced. It is now necessary to estimate the reduction in switching losses achieved for the MV side IGBTs with these modulation schemes in order to design the complete MV side power electronic unit, i.e. to dimension its critical components such as, power switches and heat sink cooling system, among others.

The losses associated with ZCS transitions are related to the dynamic behavior of the semiconductor switching device. During its conduction phase, a bipolar power switch builds up a large amount of charge in order to become conductive and hence to reduce the associated conduction losses (conductivity modulation). The instantaneous value of this charge is dynamically related to the current conducted through the semiconductor device during its conduction phase and is responsible for the switching losses encountered when the device transitions from conducting to blocking state, as this charge must be evacuated when the semiconductor device enters the blocking state (tail current of IGBTs).

The data required to estimate the dynamic behavior of this charge for arbitrary current shapes is not available in standard component's datasheets, as it partly constitutes technological information of the semiconductor manufacturers. It is therefore necessary to assess these effects through an experimental approach, whereby a theoretical basis for the proposed models is first laid out. With an understanding of the internal dynamic processes taking place in the semiconductor de-



**Figure 3.1:** IGBT cross-section. The n-base layer is responsible for blocking the voltage during the off state of the device. Also in this region, the charge required to build a low resistive current path is stored during the on-state of the device.

vice, several improvements can be proposed to the standard modulation schemes presented in Chapter 2. Finally, the obtained experimental values for switching and conduction losses are utilized in order to design the respective MV side power electronics circuits.

### 3.1 Semiconductor Stored Charge Dynamics

High voltage bipolar semiconductor devices, as previously mentioned, store large amounts of charge during their conduction phases. This charge, if not allowed to recombine internally, is translated into switching losses when the device is taken back to the blocking state. Since this stored charge is directly related to the dissipated energy during the switching process, it is useful to analyze the behavior of the charge  $Q$  stored in the switch during its conduction phase. In order to perform this analysis, first the minority carrier (hole) concentration  $p_0$  in the n-base layer, shown in the cross-sectional view of the IGBT in Fig. 3.1, needs to be studied. Consider the following expression which describes the relation between the carrier concentration  $p_0$  and the hole current density (diffusion current)  $J_{p0}$  [70]

$$p_0(t) = \frac{L_a}{2qD_p} \tanh\left(\frac{W_N}{L_a}\right) J_{p0}(t) \quad (3.1)$$

$$L_a = \sqrt{\tau D_a}, \quad (3.2)$$

where  $L_a$  is the ambipolar-diffusion length,  $D_p$  is the hole diffusion constant in the n-base layer,  $W_N$  is the thickness of the n-base layer,  $q$  is the electron charge,  $\tau$  is the recombination time constant and  $D_a$  is the ambipolar-diffusion constant. Within the n-base layer, the carrier distribution decays exponentially due to recombination [70], hence

$$p(x, t) = p_0(t) \cdot e^{-\frac{x}{L_a}}. \quad (3.3)$$

Integrating (3.3) over the n-base layer and multiplying by the elementary electric charge  $q$  and the device area  $S$ , gives the total charge  $Q$  in the n-base layer,

$$Q(t) = qS \int_0^{W_N} p(x, t) \cdot dx \quad (3.4)$$

$$= qS \cdot L_a \cdot p_0(t) \cdot \left(1 - e^{-\frac{W_N}{L_a}}\right). \quad (3.5)$$

This charge  $Q$  recombines in a lossless manner as long as the collector-emitter voltage  $U_{CE}$  remains close to zero. If a positive collector-emitter voltage  $U_{CE}$  is applied to the device before total recombination is achieved, the remaining charge will be removed from the n-base layer by an external current, causing switching losses in the semiconductor. In high voltage devices, the n-base layer width  $W_N$  is made large in order to withstand the blocking voltage. From (3.5) it can be seen that a large n-base layer directly increases the amount of stored charge  $Q$  in the device, hence increasing the switching losses. Additionally, in high voltage devices, the carrier lifetime  $\tau$  is made long in order to decrease the on-state voltage, which increases the amount of stored charge. In some applications, however, lifetime control can be applied in order to decrease the lifetime  $\tau$ , i.e. reducing switching losses, but with increased on-state voltage and hence higher conduction losses.

In order to calculate the instantaneous value of stored charge  $Q$  for an arbitrary current  $i_s$ , the following equation, i.e. the time-dependent ambipolar-diffusion equation is used [70]

$$\frac{dp(x, t)}{dt} = -\frac{p(x, t)}{\tau} + D_a \frac{d^2 p(x, t)}{dx^2}, \quad (3.6)$$

which is valid while the collector-emitter voltage  $U_{CE}$  is constant and

$\approx 0$  V. By differentiating (3.4) with respect to time and combining with (3.6) the following expression is obtained

$$\begin{aligned} \frac{dQ(t)}{dt} &= qS \int_0^{W_N} \left( -\frac{p(x,t)}{\tau} + D_a \frac{d^2 p(x,t)}{dx^2} \right) dx \\ &= -qS \frac{L_a}{\tau} \cdot p_0(t) \cdot \underbrace{\left( 1 - e^{\left(-\frac{W_N}{L_a}\right)} \right)}_{\frac{Q(t)}{\tau}} + qS \frac{D_a}{L_a} p_0(t) \left( 1 - e^{\left(-\frac{W_N}{L_a}\right)} \right). \end{aligned} \quad (3.7)$$

The first term on the right-hand-side of (3.7) is equal to  $Q/\tau$ . By inserting (3.1) in (3.7) the following expression is found

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} + qS \frac{D_a}{L_a} \frac{L_a}{2qD_p} \tanh\left(\frac{W_N}{L_a}\right) \left( 1 - e^{\left(-\frac{W_N}{L_a}\right)} \right) J_{p0}(t). \quad (3.8)$$

The hole current density  $J_{p0}$  is proportional to the total current density  $J_s$  through the switch [71],

$$J_{p0}(t) = J_s(t) \cdot K_{p0} = \frac{K_{p0}}{S} \cdot i_s(t), \quad (3.9)$$

where  $i_s$  is the instantaneous current through the switch and  $K_{p0}$  is the proportional constant relating the total current density  $J_s$  to the diffusion current density  $J_{p0}$ . This constant depends on the switch technology, whereby the expressions for the Field Stop (FS) and Non Punch Through (NPT) technologies can be found in [71]. Inserting (3.9) into (3.8) yields

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} + q \frac{D_a}{L_a} \underbrace{\frac{L_a}{2qD_p \tanh\left(\frac{W_N}{L_a}\right) \left( 1 - e^{\left(-\frac{W_N}{L_a}\right)} \right) K_{p0}}}_{k_s} \cdot i_s(t). \quad (3.10)$$

The constant (non-time dependent) part of the second term on the right hand side of (3.10) is condensed into the term  $k_s$  (with  $0 < k_s < 1$ ),



which is a proportionality parameter tightly related to the device construction and operating junction temperature  $T_j$ . Finally, the expression for the dynamic behavior of the stored charge  $Q$  in the semiconductor device for an arbitrarily shaped current  $i_s$  is found as

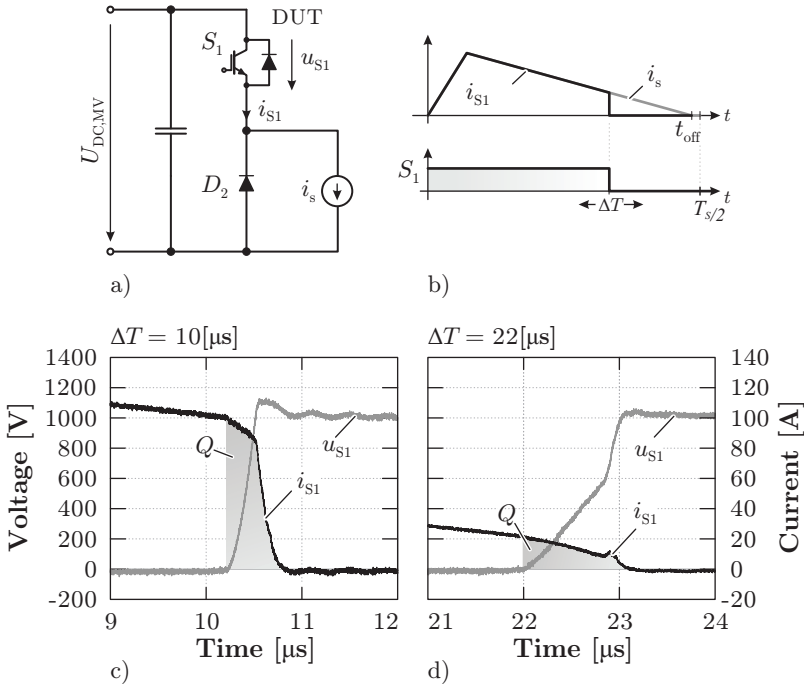
$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} + k_s \cdot i_s(t). \quad (3.11)$$

As can be seen, (3.11) provides a simple expression for the dynamic behavior of the stored charge  $Q$  in the semiconductor device, whereby only parameters  $\tau$  and  $k_s$  are required in order to describe this behavior. These parameters, however, are usually confidential information from the semiconductor manufactures and therefore cannot be directly extracted from the device's datasheet, for example. For this reason, parameters  $\tau$  and  $k_s$  were determined for 1.7 kV FS and NPT IGBTs by performing the experiment described in the following.

Consider the circuit depicted in Fig. 3.2-a) where an IGBT-based bridge leg is presented. Here, a current source generates the triangular current  $i_s$  shown in Fig. 2.13-a) whereby switch  $S_1$  is turned on at  $t = 0$ , the beginning of the switching period, and turned off at  $t = \Delta T$ . By increasing stepwise the value of  $\Delta T$  from  $\Delta T = 0$  to  $\Delta T = t_{\text{off}}$ , as shown in Fig. 3.2-b), the current turned off by device  $S_1$  is modified. By measuring the current  $i_{S_1}$  through  $S_1$  and integrating  $i_{S_1}$  over the switching process for each value of  $\Delta T$ , the charge stored in the device during the conduction phase is constructed. This experiment was also performed for a resonant structure [72].

The aforementioned test was realized with two bridge legs based on 1.7 kV FS (FF150R17KE4) and NPT (IXGN100N170) IGBTs operating at 20 kHz with a DC-link voltage of  $U_{\text{MV,DC}} = 1$  kV. The voltage and current waveforms of  $S_1$  using the FS IGBT for  $\Delta T = 10 \mu\text{s}$  and  $\Delta T = 22 \mu\text{s}$  are shown in Figs. 3.2-c) and d) respectively. Here, the area considered for the measurement of the stored charge is highlighted.

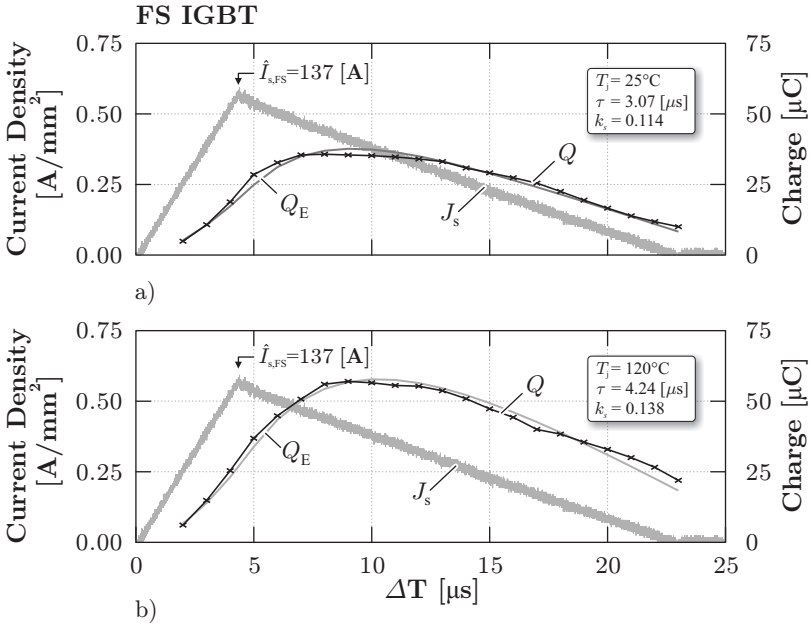
According to their respective datasheets, the utilized FS and NPT IGBTs are rated for 150 A and 95 A respectively. Given these different nominal current ratings, the described experiment was performed considering equal peak current densities  $J_s$  in both devices. Therefore, the chip areas were measured, whereby values of  $S_{\text{FS}} = 228 \text{ mm}^2$  and  $S_{\text{NPT}} = 152 \text{ mm}^2$  were obtained for the FS and NPT IGBT respectively. With peak currents of  $\hat{I}_{s,\text{FS}} = 137 \text{ A}$  and  $\hat{I}_{s,\text{NPT}} = 91 \text{ A}$  in the FS and NPT IGBTs respectively, a peak current density of  $\hat{J}_s = 0.6 \text{ A/mm}^2$



**Figure 3.2:** In order to measure the semiconductor’s stored charge, the circuit depicted in a) was used. The triangular current shape shown in b) is generated by the current source in a) and is used to measure the stored charge in the IGBT under test (DUT). Two values of switched current and the respective measurement of the evacuated charges are shown in c) and d).

is reached for both cases. As can be seen, these peak currents are in good agreement with the nominal current rating given in the respective devices’ datasheets.

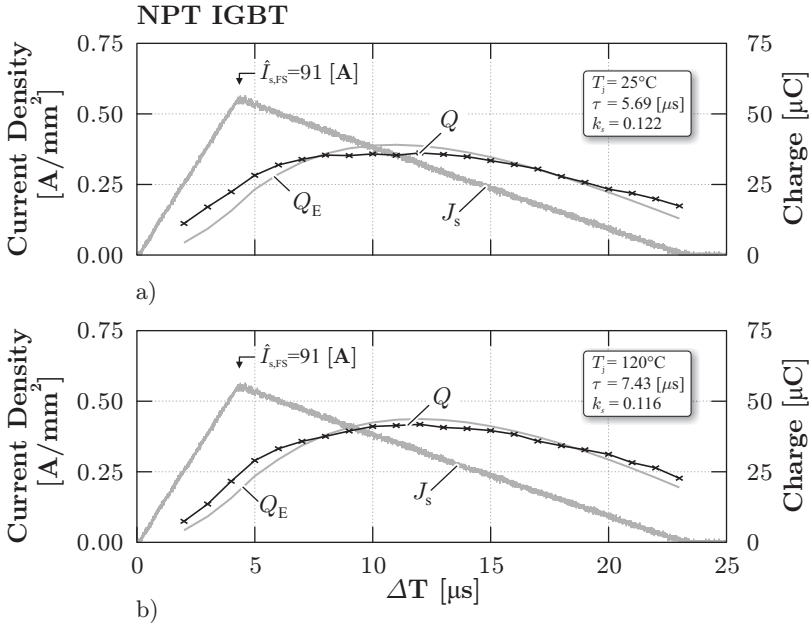
The results for the measured behavior of the charge  $Q$  in the FS and NPT IGBTs are presented in Figs. 3.3 and 3.4 respectively. These tests were done for junction temperatures of  $25^\circ C$  and  $120^\circ C$  (which were adjusted by controlling the semiconductors’ heat sink temperature) whereby single pulse tests with short pulse durations were utilized in order to avoid self heating of the devices. In each case, the measured



**Figure 3.3:** Experimentally measured stored charge behavior in a FS IGBT at a) 25 °C and b) 120 °C for TCM modulation. The dynamic charge behavior was also analytically calculated with (3.11) and the shown fitted values for  $\tau$  and  $k_s$ , leading to the waveforms of estimated charge  $Q_E$ .

behavior of  $Q$  was used to estimate the values of  $\tau$  and  $k_s$  in (3.11) in order to analytically describe the dynamic behavior of the charge. These parameters were extracted using the least squares method, whereby the obtained values are summarized in Table 3.1 and the resulting analytically estimated charge behavior  $Q_E$  is also presented in Figs. 3.3 and 3.4.

In case of the FS IGBT (cf. Fig. 3.3), the dynamic behavior of  $Q$  can be clearly seen. For a converter, this means that the switching losses in the IGBT do not depend exclusively on the instantaneous value of the switched current. This means, for example, that by switching the peak current of  $\hat{I}_{s,FS} = 137$  A at  $t = 4$  μs, less charge is removed, hence lower switching losses are generated, in comparison to switching at  $t = 10$  μs, when the value of the switched current is considerably lower. Moreover,



**Figure 3.4:** Experimentally measured stored charge behavior in an NPT IGBT at a) 25 °C and b) 120 °C for TCM modulation. The dynamic charge behavior was also analytically calculated with (3.11) and the shown fitted values for  $\tau$  and  $k_s$ , leading to the waveforms of estimated charge  $Q_E$ .

at time  $t = 23 \mu\text{s}$  when the current reaches zero, a considerable amount of charge remains stored in the device, thus turning  $S_1$  off in ZCS conditions wouldn't result in zero switching losses. In other cases, e.g. in inverter applications with relatively low switching frequencies, the conduction phase is usually long enough (e.g. 3 to 4 times the time constant  $\tau$ ) and therefore the static behavior of the charge

$$Q(t) = \tau \cdot k_s \cdot i_s(t) \quad (3.12)$$

is reached. In this case, the stored charge, hence switching losses, are proportional to the switched current, as commonly stated in IGBT datasheets.

In Fig. 3.3-b), the behavior of  $Q$  for a junction temperature  $T_j$  of 120 °C is shown, whereby a considerable sensitivity of the amount of

stored charge with respect to temperature is visible. This is confirmed by the values of  $\tau$  and  $k_s$  estimated in this case, which are both higher in comparison to the values obtained with operation at 25 °C as expected for this type of IGBT technology [73]. It should be noted that for both temperature values, an accurate fitting of (3.11) is achieved, thus for this device the analytical description proves useful to estimate the charge behavior in the device.

In comparison to the FS device, it can be observed that the NPT switch features a larger recombination time constant  $\tau$  (cf. Fig. 3.4) for both tested junction temperatures, as expected for this type of switch technology [73]. Moreover, it can be seen that the sensitivity to operation at higher temperatures is lower for this type of IGBT, which is also in agreement with the expected behavior. It should be noted that, similar to the FS IGBT, (3.11) with the fitted values of  $\tau$  and  $k_s$  also in this case very well represents the behavior of  $Q$  in the NPT device during its conduction phase. However, the accuracy of this equation is lower than in the case of the FS switch, as can be seen by the behavior of  $Q_E$  in Figs. 3.4-a) and b). This difference can be explained by a light dependency of the parameter  $K_{p0}$  on the conducted current  $i_s$ , as described in [70, 74].

**Table 3.1:** Extracted parameters for the 1.7 kV FS and NPT IGBTs at junction temperatures of  $T_j = 25^\circ\text{C}$  and  $T_j = 120^\circ\text{C}$ .

Switch Technology	Temperature $T_j$	$\tau$	$k_s$
FS	25 °C	3.07 $\mu\text{s}$	0.114
FS	120 °C	4.24 $\mu\text{s}$	0.138
NPT	25 °C	5.96 $\mu\text{s}$	0.122
NPT	120 °C	7.43 $\mu\text{s}$	0.116

Table 3.1 summarizes the extracted parameters of the two analyzed IGBTs at  $T_j = 25^\circ\text{C}$  and  $T_j = 120^\circ\text{C}$ . It can be observed that the FS device features a faster time constant at both measured temperatures. This makes the FS IGBT more suitable for ZCS modulation schemes, where fast recombination of the internal charge is a key feature to reach low switching losses and hence high efficiency. On the other hand, the NPT IGBT shows a lower sensitivity to temperature and therefore it would be attractive for applications where a high operating temperature of the IGBT's junction is necessary in order to reduce the heat sink

size and therefore increase power density. In the following, only the FS IGBT will be considered in the verification of the proposed ZCS techniques.

The aforementioned analysis of the stored charge in FS and NPT IGBTs provides the basis for modelling the ZCS losses in this type of semiconductor devices. This model represents the last missing element within the converter model which would enable an overall converter optimization, i.e. a Pareto front analysis [75]. Moreover based on the previous study of the IGBTs stored charge, a first observation regarding soft switching techniques in high voltage semiconductors can be made: the shape of the current during the conduction phase considerably influences the remaining stored charge that needs to be evacuated from the switch when entering the blocking state in case of high switching frequencies. Therefore, it is desirable to conveniently shape this current in order to minimize the ZCS losses, as reported in previous publications on the HC-DCM-SRC (cf. Fig. 2.4-a)) whereby the main approaches are reviewed in the next section.

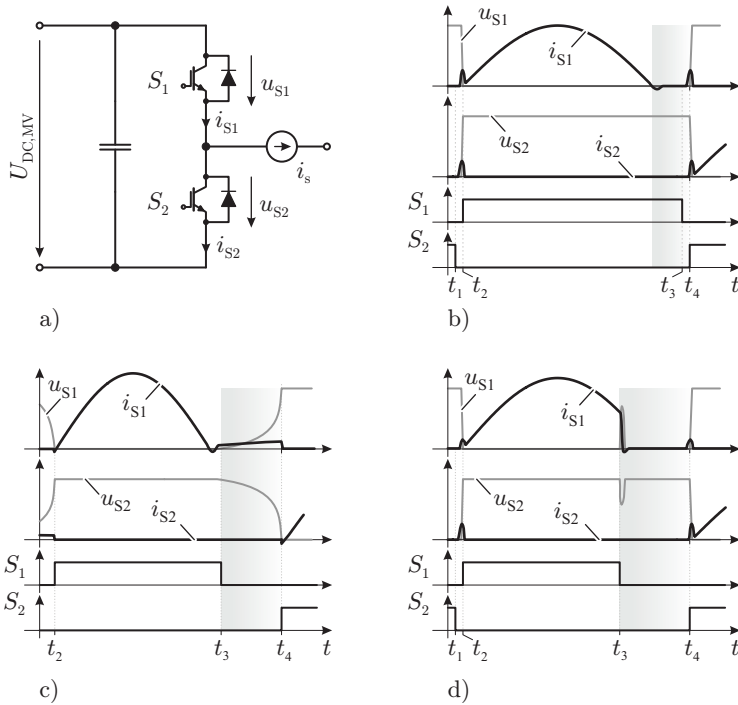
## 3.2 Previously Proposed ZCS Techniques for Resonant Converters

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Consider the bridge leg presented in Fig. 3.5-a) where the current source  $i_s$  represents the resonant tank together with the rest of the HC-DCM-SRC circuit (cf. Fig. 2.4-a)). This current source generates the sinusoidal pulses shown in Figs. 3.5-b), c) and d) used to analyze three of the main previously proposed enhancements in the ZCS modulation scheme for this converter structure: Interlock delay time (cf. Fig. 3.5-b)); Increased magnetizing current (cf. Fig. 3.5-c)) and Residual current switching (cf. Fig. 3.5-d)).

### 3.2.1 Interlock Delay Time

As described in the previous chapter, by operating in sub-resonant mode, the resonant converter offers the possibility to introduce an interlock time in the conduction of  $S_1$  between the zero crossing of the current and the turn-on event of  $S_2$ , as depicted in Fig. 3.5-b). This interlock delay time provides additional time for the IGBT to recom-



**Figure 3.5:** Previously reported enhancements to the ZCS HC-DCM-SRC: a) IGBT phase leg; b) Interlock delay time introduced; c) Increased magnetizing current; d) Residual current switching.

bine its carriers in a lossless manner, thus the switching losses generated when  $S_2$  is turned on are considerably reduced. It should be noted that, as seen in [12, 15, 59], no significant reverse recovery effects of the LV side diodes are encountered when the current reaches zero due to the relatively small voltage step the rectifying diodes are subject to, which only corresponds to the series capacitor voltage at the end of the sine pulse.

### 3.2.2 Increased Magnetizing Current

In the HC-DCM-SRC, the bridge providing the power also needs to provide the magnetizing current of the isolation transformer. This means that when the resonant pulse is finished, the magnetizing current continues flowing through the previously conducting IGBTs, non-linearly increasing the IGBT voltage (due to the non-linear collector-emitter capacitance), as shown in Fig. 3.5-c). Therefore, if the magnetizing current is made high enough, it can be used to extract stored charge from the IGBT, as described in [14, 15]. It should be noted that, if enough time is provided to change the voltage of the parasitic capacitances of  $S_1$  and  $S_2$ , the turn on process of  $S_2$ , after the non-linear increase of the blocking voltage (cf. Fig. 3.5-c)), is done under ZVS conditions, thus a considerable reduction in switching losses can be achieved.

### 3.2.3 Residual Current Switching

As reported in [12, 15], the switch  $S_1$  in Fig. 3.5-a) can be turned off before the resonant pulse has reached zero current. This way, the charge stored in the IGBT can be removed by the series inductor and, under certain conditions, ZVS can be achieved for the turning-on IGBT. In order to achieve this, the series inductor  $L_s$  must store enough energy to charge/discharge the respective capacitances of  $S_1$  and  $S_2$ .

A large series inductor, however, is undesirable in this converter since it affects the converter's dynamic performance [58]. For this reason, turning  $S_1$  off, as shown in Fig. 3.5-d), does not result in a traditional inductive switching. Here, as explained in [12], the current reverses its direction in the switched-off IGBT before the maximum blocking voltage is reached, thus its antiparallel diode conducts and the voltage in the device is reduced to zero until the complementary switch  $S_2$  is turned on (cf. Fig. 3.5-d)). As also shown in [12], only minor ringing due to the reverse recovery of this diode is obtained during the IGBT turn-off given that this process is done at nearly zero voltage.

Nevertheless, this type of switching strategy has been utilized for reducing the switching losses in previous implementations [12, 15] due to the additional time that can be provided for carrier recombination (shaded area in Fig. 3.5-d)).



### 3.2.4 Applications to the TCM-DAB Converter

The aforementioned enhancements to the ZCS modulation for the HC-DCM-SRC suggest the use of similar techniques for the TCM-DAB. However, the inclusion of an additional interlock delay time into the control of the TCM-DAB is not straightforward. This is due to the reverse recovery of the rectifier diodes on the LV side. In the HC-DCM-SRC, the series inductor value  $L_s$  is typically kept as low as possible in order to improve the converter's dynamic response [58]. This results in a large resonant capacitor  $C_r$  value, thus the peak voltage of this component is low in comparison to the DC-link voltages. The peak resonant capacitor voltage must be blocked by the diodes of the rectifier bridge after their respective conduction phases are finalized, therefore, since this voltage step is relatively low, the reverse recovery effects are negligible, as reported in [12, 14, 15].

On the other hand, in the TCM-DAB, this voltage step is considerably larger as it corresponds to the MV side applied voltage times the turns ratio of the transformer, resulting in large oscillations of the transformer voltages due to the reverse recovery of the rectifier diodes. Therefore, other strategies to provide longer recombination time need to be implemented in the case of the TCM-DAB.

Since the value of the series inductor  $L_s$  in case of the TCM-DAB is considerably higher than in the case of the HC-DCM-SRC, also the stored energy in this component is considerably higher. This means that, by adjusting the control signals of the TCM-DAB such that a high enough current is switched, the stored charge of the switching device can be completely removed and additionally ZVS of the complementary switch can be achieved. This can be done without reducing the magnetizing inductance value, as in the HC-DCM-SRC, and therefore without increasing the reactive power in the circuit. This operating mode corresponds to the one described in Section 2.3.2 with non-zero switched current, i.e. the general case for the TCM operating mode of the DAB (cf. Section 2.3.2).

## 3.3 Proposed Enhancements to the TCM-DAB

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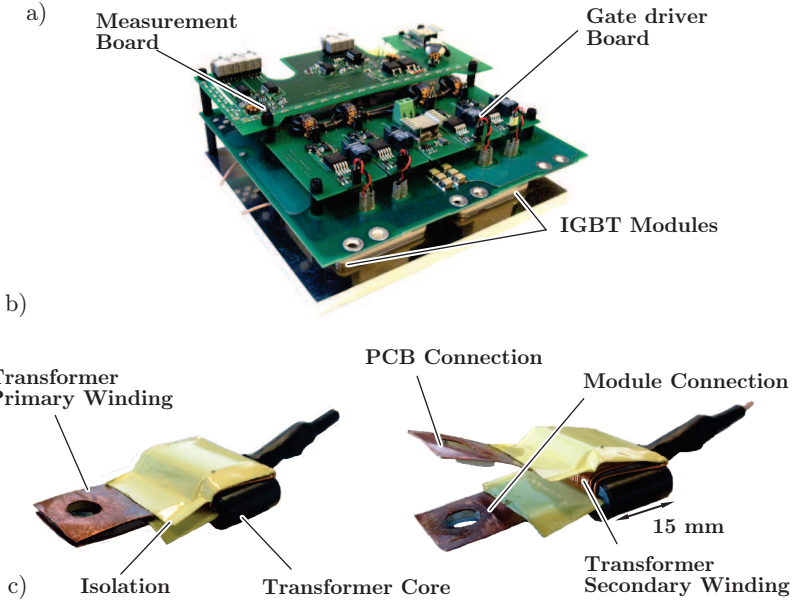
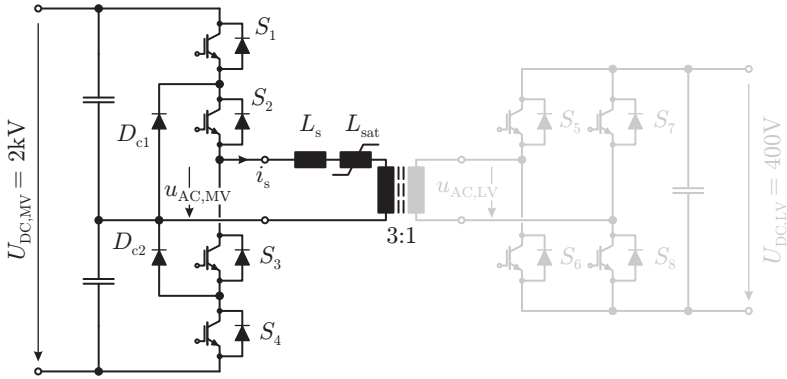
As discussed in the previous sections, there are two main strategies that can help to reduce switching losses in the MV side semiconductors. The

first one is related to the time provided for the recombination of the charge that the IGBT stores during its conduction phase by introducing a time interval before the semiconductor has to block voltage where the current is considerably lower than the peak current. The second one is the reduction or total elimination of turn-on losses by achieving ZVS in the turning-on device. The means to implement these strategies will be discussed in this section together with their experimental verification.

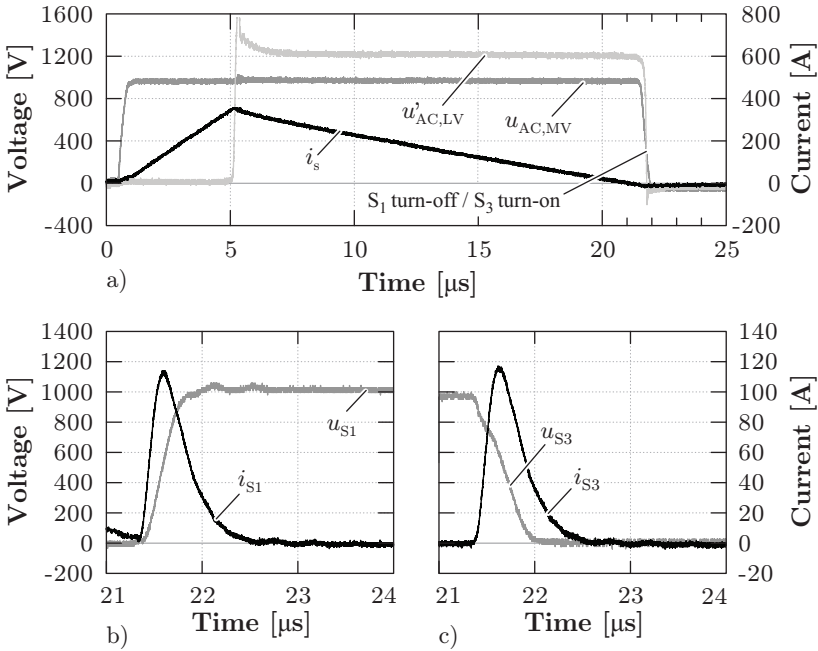
### 3.3.1 Standard ZCS Modulation

In order to benchmark the proposed modulation strategies for the TCM-DAB, first the switching losses for pure ZCS modulation (cf. Fig. 2.13), i.e. the special case when  $I_{MV,SW} = 0$  and  $I_{LV,SW} = 0$ , were measured. These measurements were performed with the aforementioned 1.7 kV FS IGBT module (FF150R17KE4) building a 2 kV NPC half-bridge-based bridge (with super-fast recovery clamping diodes (DSDI 60)) as shown in Fig. 3.6-a) which was designed and utilized during all the following tests at a nominal power of 166 kW and a switching frequency of 20 kHz. The hardware realization of this bridge is shown in Fig. 3.6-b). The non-linear inductor  $L_{sat}$  shown in Fig. 3.6-a) will be used in the third part of this section to shape the current in order to reduce the switching losses of the MV side switches. The transformer turns ratio is  $N_{MV}/N_{LV} = 3 : 1$  and the LV side bridge is a 400 V full-bridge structure utilized to generate the desired current waveforms. The planar current transformers (based on ferrite cores originally used as common-mode chokes for planar cables) shown in Fig. 3.6-c) together with passive voltage probes were used to measure the currents and voltages of switches  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$  (cf. Fig. 3.6-a)).

The turn-off and turn-on process of the complementary switches  $S_1$  and  $S_3$  are used hereinafter to exemplify the ZCS process and the further proposed enhancements. It should be noted, however, that in order to comprehensively analyze the switching losses, all switching events were measured and used to calculate the total losses of the NPC half-bridge. The switching process of devices  $S_1$  and  $S_3$  at the end of one half switching cycle is shown in Figs. 3.7-b) and c) respectively. Here it can be seen that since  $S_1$  was conducting the current during the positive semi-cycle, it contains a considerable amount of stored charge, which is removed when  $S_3$  is turned on causing turn-off losses in  $S_1$  as well as considerable turn-on losses in  $S_3$ .

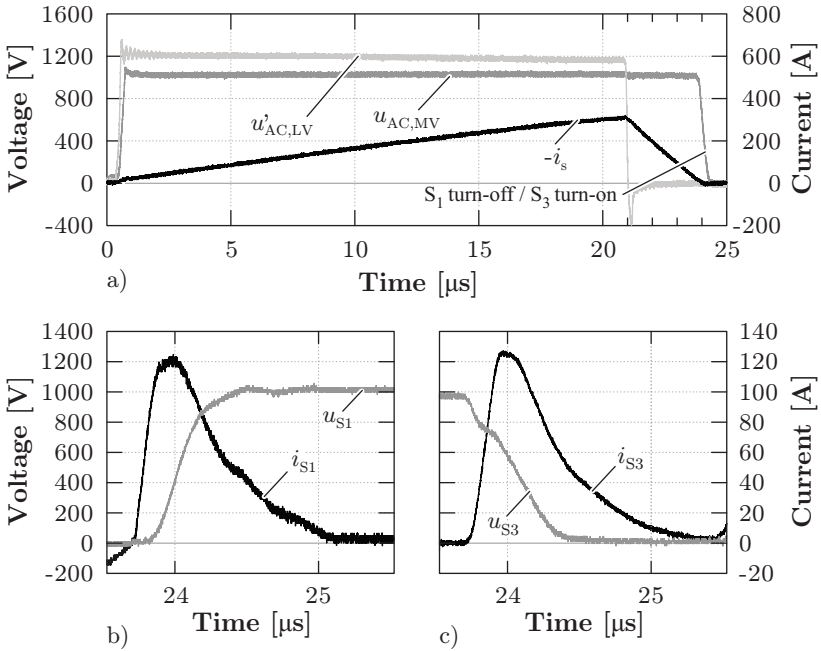


**Figure 3.6:** DAB converter used to test the 1.7kV FS IGBT: a) NPC half-bridge-based bridge linked to the LV side full-bridge through a transformer; b) Hardware realization of the MV side 2kV NPC half-bridge; c) Current transformers utilized to measure the IGBT modules' currents during the switching events.



**Figure 3.7:** Main waveforms for standard ZCS with TCM-DAB and power transfer from MV to LV side: a) AC-link waveforms for one half switching period; b) Voltage and current of  $S_1$  during the switching interval at the end of the semi-cycle; c) Voltage and current of  $S_3$  during the switching interval at the end of the semi-cycle.

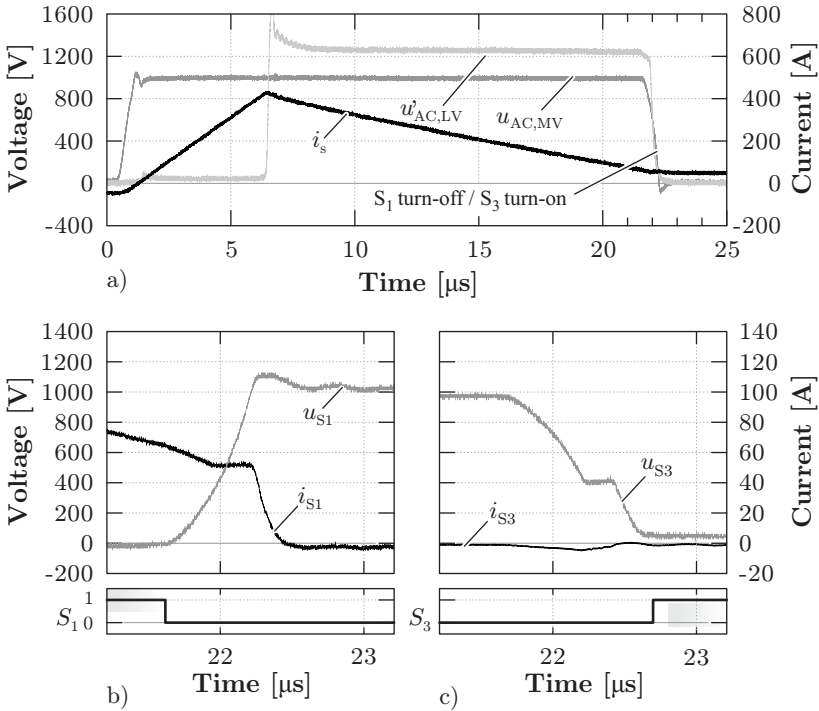
The current and voltage waveforms in the transformer for power flowing from the LV to the MV side are shown in Fig. 3.8-a), where the phase-shift and duty cycles of the LV and MV side bridges have been adjusted to reverse the power flow while still achieving ZCS on the MV side, as described in the previous chapter. The switching behavior of switches  $S_1$  and  $S_3$  is shown in Figs. 3.8-b) and c) respectively where it should be noted that for this power flow direction, the respective antiparallel diodes of each switch conduct the triangular current and are therefore responsible for the generated switching losses. As can be seen, the turn-on process of  $S_3$  generates losses in the antiparallel diode of  $S_1$ , as this last device was previously conducting the full current and



**Figure 3.8:** Main waveforms for standard ZCS with TCM-DAB and power transfer from LV to MV side: a) AC-link waveforms for one half switching period; b) Voltage and current of  $S_1$  during the switching interval at the end of the semi-cycle; c) Voltage and current of  $S_3$  during the switching interval at the end of the semi-cycle.

thus still contains a considerable amount of stored charge. The current peak in Figs. 3.8-b) and c) representing the evacuation of the charge stored in the antiparallel diode of  $S_1$  flows through  $S_3$  during its turn-on process, thus causing turn-on losses also in this device (cf. Fig. 3.8-c)).

The waveforms shown in Figs. 3.7 and 3.8 suggest the use of a non-ZCS, i.e. residual current switching modulation scheme, allowing a certain amount of current to be switched-off by  $S_1$ . This way, the stored charge is evacuated through the load, and the voltage across  $S_3$  is decreased before its gate signal is applied, resulting in ZVS of  $S_3$ . This type of modulation corresponds to the general case for the TCM-DAB described in Section 2.3.2, when the value of the switched current



**Figure 3.9:** Main waveforms for ZVS of the TCM-DAB and power transfer from MV to LV side: a) AC-link waveforms for one half switching period; b) Voltage and current of  $S_1$  during the switching interval at the end of the semi-cycle; c) Voltage and current of  $S_3$  during the switching interval at the end of the semi-cycle.

$I_{MV,SW}$  is higher than zero, thus allowing soft ZVS transitions.

### 3.3.2 Modified ZVS Modulation

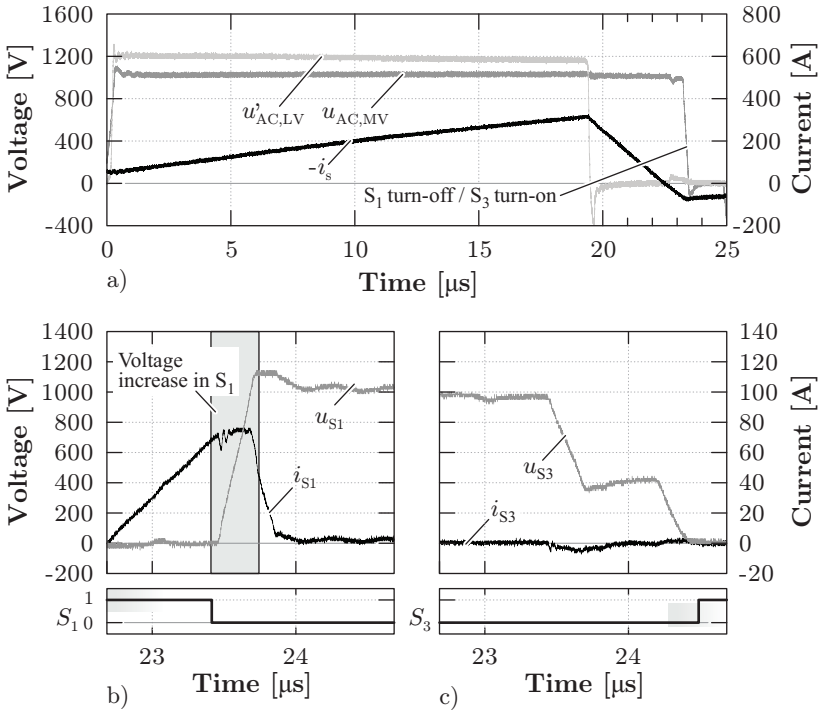
The operation under ZVS was studied for the converter displayed in Fig. 3.6 (without the saturable inductor  $L_{sat}$ ). The waveforms for power transfer from MV to LV side are shown in Fig. 3.9-a), where the duty cycles and the phase shift of the converter have been adjusted in order to switch a current of  $I_{MV,SW} = 50$  A. In this case,  $S_1$  is turned off before

the current reaches zero, thus losing ZCS, as shown in Fig. 3.9-b). Since the current is not zero when  $S_1$  is turned off, its voltage increases before the gate signal is applied to the complementary switch  $S_3$ . This means that  $S_3$  is turned on with ZVS and no current peak must be conducted during its turn-on process (cf. Fig. 3.9-c)) in contrast to the switching process shown in Fig. 3.7-c), thus reducing the turn-on losses of  $S_3$  to a negligible value. It should be noted that during interlock delay time interval, before switch  $S_3$  is turned on, the voltage  $u_{S_3}$  in this device stays in an intermediate value which is defined by the capacitive network built by parasitic capacitances of the bridge semiconductors, as detailed in [76].

In Fig. 3.10-a) the operation for power transfer from the LV to the MV side is shown with a modification in the modulation scheme which allows a soft-switching transition of  $S_1$  and  $S_3$  by keeping the gate signal of  $S_1$  on until the reverse recovery charge of its respective antiparallel diode has been evacuated. This modification corresponds to selecting a non-zero value for  $I_{MV,SW}$  and reversing the power flow direction in the TCM-DAB by adjusting the phase shift  $\phi$ . The result of this modification on the switching performance of  $S_1$  and  $S_3$  is shown in Figs. 3.10-b) and c). As previously explained, the current reverses its direction in the antiparallel diode of  $S_1$  before turn-on of  $S_3$ , thus the voltage across  $S_1$  is increased within the reverse recovery interval, as highlighted in Fig. 3.10-b), and not by the turn-on process of switch  $S_3$ . Therefore, the turn-on losses in  $S_3$  are reduced considerably as shown in Fig. 3.10-c), whereby, as explained earlier, an intermediate voltage level is blocked by device  $S_3$  before its turn-on signal is applied and the voltage decreases to zero.

Taking all switching processes into account, the switching losses in all switches and diodes of the MV side bridge were measured under ZVS operation for different switched currents, at 25 °C and 120 °C and for power transfer in both directions. In Fig. 3.11-a), the results for nominal power transfer ( $P_T = 166$  kW) from the MV to the LV side are presented. Here, an optimum can be found around 40 A of switched current for operation at 120 °C, reaching a reduction of 40 % in the total switching losses. Above this current value, no further reduction of the turn-on losses is achieved whereas the turn-off losses are increased, consequently the overall switching losses are also increased.

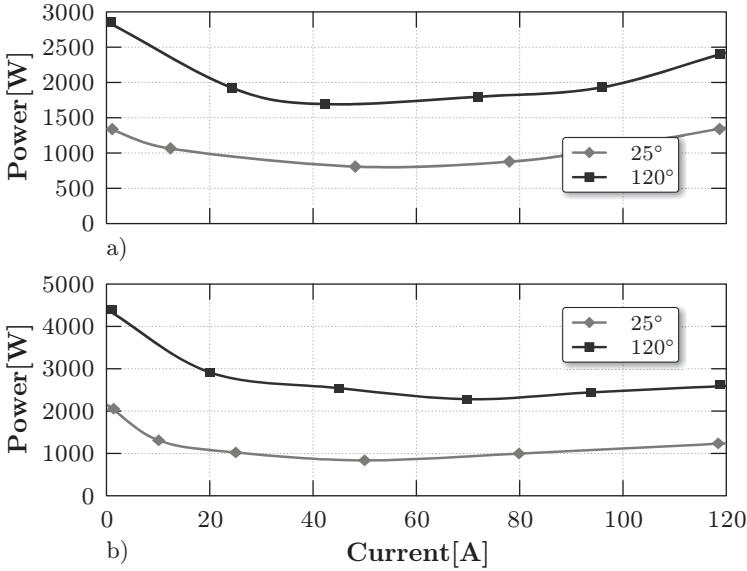
The results for nominal power flow from the LV to the MV side ( $P_T = 166$  kW) are shown in Fig. 3.11-b). It can be seen that the



**Figure 3.10:** Main waveforms for ZVS of the TCM-DAB and power transfer from LV to MV side: a) AC-link waveforms for one half switching period; b) Voltage and current of  $S_1$  during the switching interval at the end of the semi-cycle; c) Voltage and current of  $S_3$  during the switching interval at the end of the semi-cycle.

switching losses have an optimum value around 70 A of switched residual current for operation at 120 °C, where a 48% reduction with respect to the operation with pure ZCS is achieved. It can be seen that if higher currents are switched off, no further reduction of turn-on losses is achieved whereas the turn-off losses are increased.



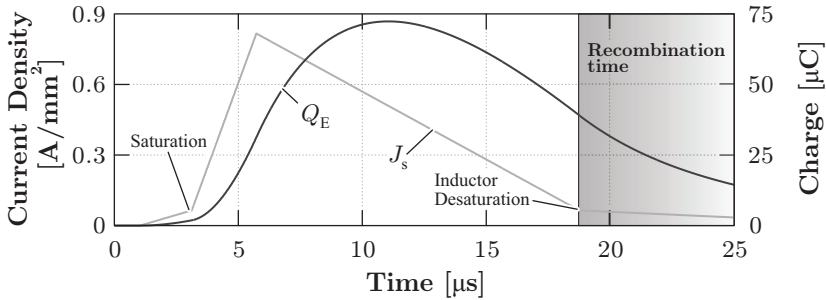


**Figure 3.11:** Optimal residual switched current for switching loss minimization: a) Power transfer from MV to LV side ( $P_T = 166$  kW); b) Power transfer from LV to MV side ( $P_T = 166$  kW).

### 3.3.3 Saturable Inductor Current Shaping

By inserting a saturable inductor  $L_{\text{sat}}$  (cf. Fig. 3.6) in series to the series inductor  $L_s$ , the current through the transformer, and consequently through the switches, can be shaped conveniently in order to stay at a low value for a portion of the switching period right before the devices are taken to blocking state, as shown in Fig. 3.12 where a simulation of the stored charge behavior for the FS IGBT operated at 120°C is presented. When compared to the amount of charge removed in normal ZCS mode (cf. Fig. 3.3-b)), an improvement is achieved since less charge must be evacuated when the voltage is re-applied. This new current shape is merged with the previously introduced ZVS modulation, thus combining the features of long recombination time and ZVS.

For the analyzed converter, a saturable inductor with a saturation current of 35 A was used. While keeping this saturation current constant, the inductance value was modified, whereby three different values

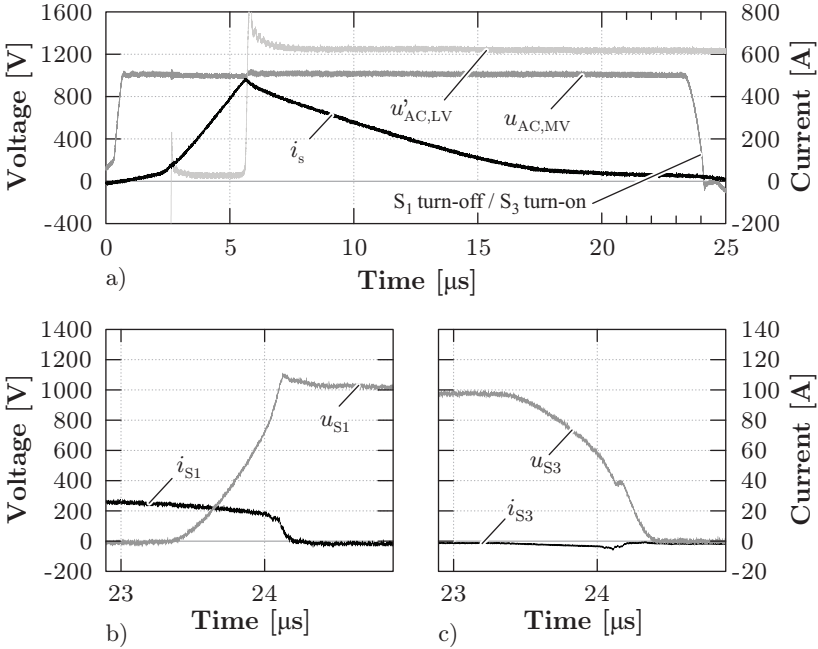


**Figure 3.12:** IGBT simulated charge profile for saturable inductor current shaping considering the FS IGBT at  $120^\circ\text{C}$  ( $\tau=4.24\ \mu\text{s}$  and  $k_s = 0.138$ ).

were tested:  $40\ \mu\text{H}$ ,  $70\ \mu\text{H}$  and  $100\ \mu\text{H}$  (non-saturated values). When saturated, the inductance value reaches  $1\ \mu\text{H}$ , which together with the (non-current dependant) inductance  $L_s$  results in a total series inductance of  $4.7\ \mu\text{H}$ . The resulting current waveform for power transfer from the MV to the LV side, i.e. IGBTs conducting the current, are shown in Fig. 3.13 for a saturable inductor value of  $L_{\text{sat}} = 100\ \mu\text{H}$ . As can be seen from Fig. 3.13-a), the saturable inductor introduces a time interval before the bridge is taken to freewheeling where the current is comparatively low, thus allowing  $S_1$  and  $S_2$  to recombine a large amount of the charge generated during the conduction phase. In addition, a certain amount of current is turned-off by  $S_1$  (cf. Fig. 3.13-b)), thus ZVS for achieved in  $S_3$  as shown in Fig. 3.13-c) and described in the previous section.

The waveforms corresponding to power from the LV to the MV side and a saturable inductor  $L_{\text{sat}} = 100\ \mu\text{H}$  are shown in Fig. 3.14-a) whereby the diodes of the MV side bridge benefit from the additional time for recombination. In order to achieve soft-switching, the current is allowed to reverse its direction through the antiparallel diode of  $S_1$  within the reverse recovery interval of the diode, thus voltage is built up across  $S_1$ , achieving ZVS in  $S_3$  (cf. Fig. 3.14-c)).

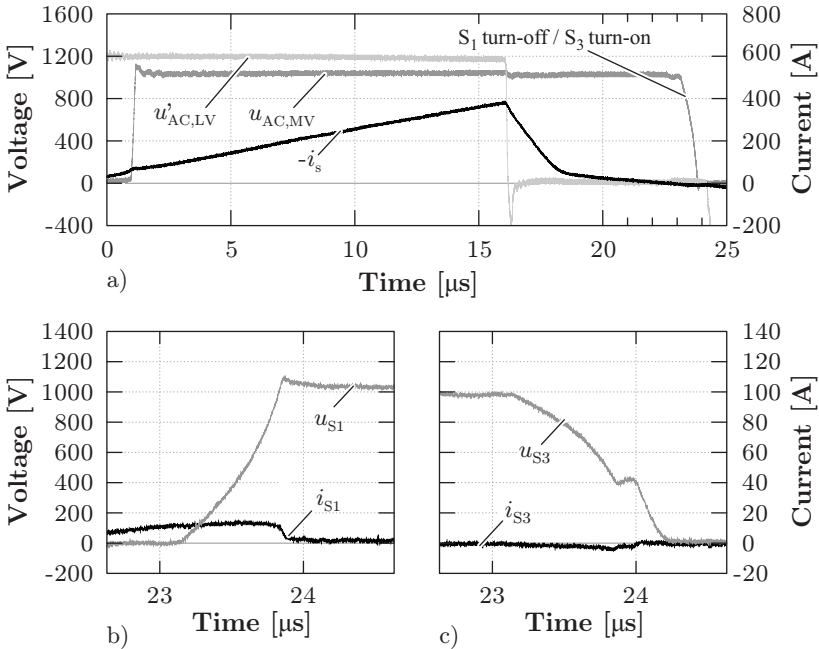
It should be noted that the addition of the saturable inductor  $L_{\text{sat}}$  to the circuit introduces time intervals, as long as this inductor is not saturated, where relatively low power is transferred from the MV to the LV side. Since the required power to be transferred remains constant, this results in an increased peak current through the circuit, and thus



**Figure 3.13:** Main waveforms of the TCM-DAB with  $100 \mu\text{H}$  saturable inductor,  $4.7 \mu\text{H}$  series inductor and power transfer from MV to LV side: a) AC-link waveforms for one half switching period; b) Voltage and current of  $S_1$  during the switching interval at the end of the semi-cycle; c) Voltage and current of  $S_3$  during the switching interval at the end of the semi-cycle.

in higher conduction and switching losses on the LV side. In order to reduce the impact of the saturable inductor inclusion, the voltages on the MV and LV side are conveniently modified with respect to the traditional modulation in order to rapidly bring the saturable inductor into saturation at the beginning of each half switching period. This can be seen in Fig. 3.13-a) before  $t = 2.5 \mu\text{s}$ , when the full difference between  $u_{LV,AC}$  and  $u_{MV,AC}$  is applied to the inductor. The result is a moderate increase of the peak current through the circuit resulting in a corresponding moderate increase of the conduction and switching losses, as will be quantitatively analyzed in Section 3.3.4.

The aforementioned tests were performed for the three values of the

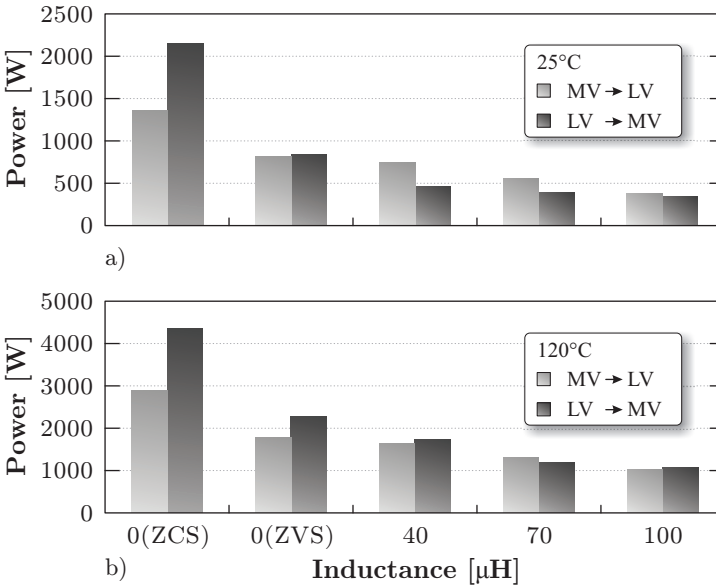


**Figure 3.14:** Main waveforms TCM-DAB with  $100\ \mu\text{H}$  saturable inductor,  $4.7\ \mu\text{H}$  series inductor and power from LV to MV side: a) AC-link waveforms for one half switching period; b) Voltage and current of  $S_1$  during the switching interval at the end of the semi-cycle; c) Voltage and current of  $S_3$  during the switching interval at the end of the semi-cycle.

saturable inductor,  $120\ ^\circ\text{C}$  and  $25\ ^\circ\text{C}$  junction temperature and power flow in both directions. The results for these tests are analyzed and compared with the standard ZCS and the analyzed ZVS modulation in the next section.

### 3.3.4 Switching Loss Reduction Summary and Impact on Converter Performance

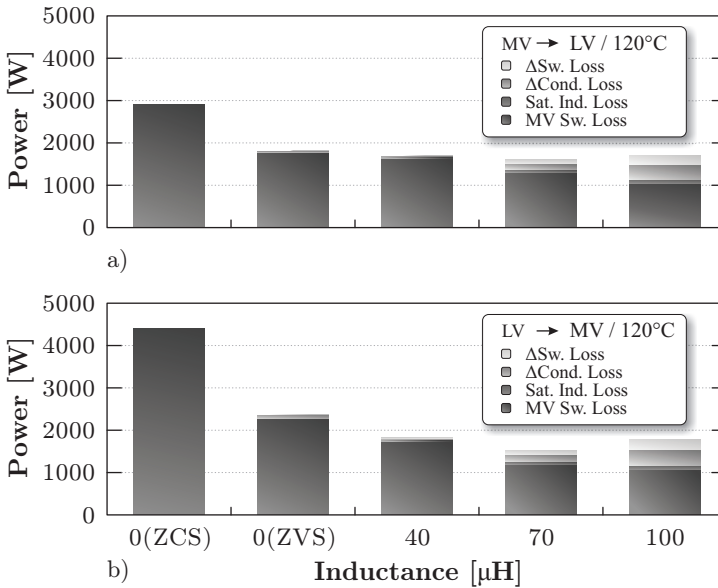
A summary of the previously described switching loss reduction strategies is provided in Fig. 3.15 for power transfer in both directions and at  $25\ ^\circ\text{C}$  and  $120\ ^\circ\text{C}$  junction temperature. As can be seen, a considerable



**Figure 3.15:** Summary of reduction in switching losses of the MV side switches with the presented soft-switching strategies and power transfer of 166 kW: a) Junction temperature of 25 °C; b) Junction temperature of 120 °C.

loss reduction can be achieved by combining ZVS techniques together with the saturable inductor. In the best case, with a 100 μH saturable inductor, the switching losses are more than four times lower for operation at 25 °C and more than three times lower when operating at 120 °C.

However, the introduction of the saturable inductor to shape the current through the switches increases the conduction losses in the whole converter and switching losses on the LV side. Moreover, the saturable inductor generates by itself additional losses which should be added to the total converter losses. In Fig. 3.16, the aforementioned additional losses are added to the switching losses of the MV side switches shown in Fig. 3.15 for the different strategies (note that these are the additional conduction and switching losses and not the total conduction and switching losses). As can be seen, for power flow in both directions, the use of a 70 μH saturable inductor is advantageous with respect to the



**Figure 3.16:** Impact of the modified current waveforms on the converter performance for a junction temperature of  $120^\circ\text{C}$ . The losses in the saturable inductor plus the additional conduction and LV side switching losses are included: a) Power transfer from MV to LV side; b) Power transfer from LV to MV side.

$100\ \mu\text{H}$  inductor, as the additional losses introduced by the modified current shape overcome the reduction in switching losses on the MV side in the latter case. This means that for this application, the use of a  $70\ \mu\text{H}$  saturable inductor would result in the lowest losses in the overall converter.

With the proposed models and extracted experimental loss values for the MV side semiconductors, the remaining components of the MV side bridge, e.g. gate driver, heat sink and capacitor banks among others, are designed as presented in the next sections for both the HC-DCM-SRC and the TCM-DAB.

## 3.4 Design and Construction of the NPC Half-Bridges

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The estimation of the ZCS losses in the 1.7 kV IGBTs performed in the previous section determines the key missing component of the loss contributions of the MV side NPC half-bridge. With this estimations and the developed models for estimation of the dynamic charge behavior, the further steps in the design of the MV side components, such as heat sink dimensioning, semiconductor layout, power busbar and gate driver design, can be completed.

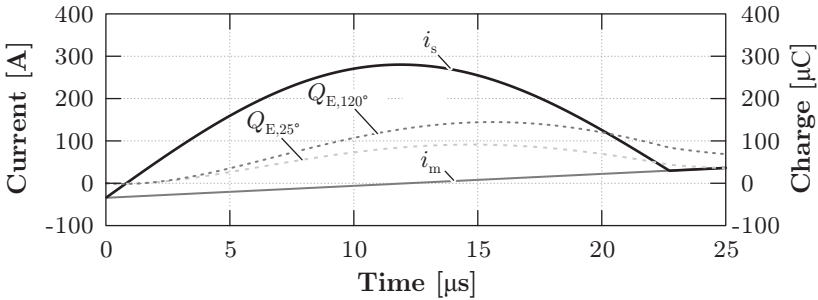
### 3.4.1 IGBT Module Selection and Loss Calculation

The measurement of the ZCS losses of the 1.7 kV FS IGBT in the previous section was performed on the FF150R17KE4 IGBT module from Infineon, which belongs to the IGBT 4 semiconductor technology generation. In order to utilize the previous measurements of switching losses for the dimensioning of the final NPC half-bridge of the MV side, an IGBT module of the same technology generation was selected.

From the available options of IGBT modules with this technology, the dual (or half-bridge) arrangement is advantageous as the internal module layout already ensures low parasitic inductances of the power and gate drive paths, resulting in a more straightforward design. In order to reduce the overall losses and hence to increase the efficiency, the module with highest current rating (available at this time) within this semiconductor family was selected, corresponding to the FF450R17ME4 1700 V/450 A EconoDUAL IGBT module. Three of these modules are utilized to build the complete NPC half-bridge, whereby the antiparallel diodes of two of the IGBTs are used as the clamping diodes of the NPC structure, as will be shown later when the assignment of the different modules is explained.

The switching losses in the HC-DCM-SRC are not available since only the TCM-DAB was utilized to study the ZCS loss behavior. For this reason, the procedure presented in [77], which utilizes the value of estimated charge  $Q_E$  at the end of one half switching period, was utilized in order to calculate these losses.

To obtain the value of  $Q_E(T_s/2)$ , first the current waveform conducted by the semiconductor device must be defined. Here, a resonant frequency of 22 kHz was selected whereby a magnetizing current  $i_m$



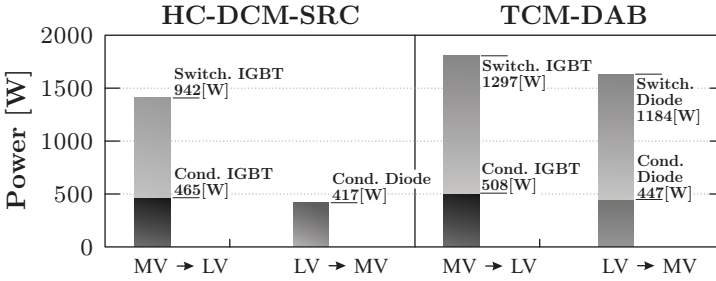
**Figure 3.17:** Theoretical charge profile for HC-DCM-SRC based on (3.11). The charge was estimated for 25 °C and 120 °C ( $Q_{E,25^\circ}$  and  $Q_{E,120^\circ}$  respectively) with the IGBT parameters from the FS IGBT presented in Table 3.1.

with peak value  $\hat{I}_m = 40$  A at the switching instant is added to the resonant pulse in order to ensure soft-switching transitions (cf. Section 2.3.1). With these parameters, the peak current in the resonant tank corresponds to  $\hat{I}_s = 284.3$  A. The current waveform  $i_s$  and the resulting charge profiles for 25 °C and 120 °C operating temperature are presented in Fig. 3.17, whereby only 120 °C junction temperature is considered for the loss calculation. These losses amount to 942 W for all 4 semiconductor devices of the NPC half-bridge.

In order to complete the calculation of losses for the MV side NPC half-bridges, the conduction losses are calculated based on the current waveforms shown in Figs. 3.13 and 3.14 for the TCM-DAB and with the current waveform from Fig. 3.17 for the HC-DCM-SRC together with the output characteristic extracted from the device’s datasheet.

The summary of the losses for both converters and also for both power flow directions at nominal power is shown in Fig. 3.18. The measured switching losses in the TCM-DAB are included. As can be seen, for power transfer from MV to LV side, in both converters the switching losses contribute to the largest portion of the overall losses, which is expected due to the combination of MV and MF. It should be noted that no switching losses are added for the HC-DCM-SRC when powering from the LV to the MV side since during this time only the diodes on the MV side are operated and virtually no reverse recovery effects are encountered due to the slow current slope of the resonant pulse.





**Figure 3.18:** Calculated values for conduction and switching losses in the MV side bridge of the HC-DCM-SRC and TCM-DAB converters for dimensioning of the cooling system.

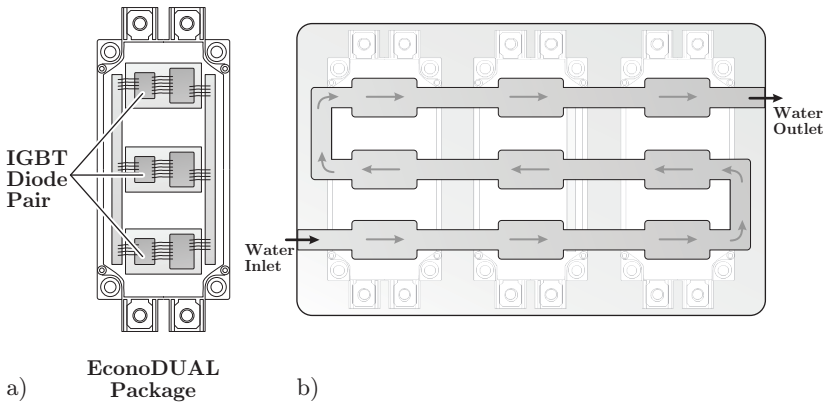
With these values for the losses in both converters, the next step in the module construction can be initiated: The heat sink design.

### 3.4.2 Heat Sink Design

In worst case, the HC-DCM-SRC MV side bridge generates 2744 W of losses. A commercial solution was adopted for the heat sink of this bridge in order to realize a simple and robust design. In this case, the MQT1914 water-cooled heat sink from MaxQ Technology was considered. This heat sink can dissipate up to 3000 W and is originally designed for three phase inverters built with three EconODUAL IGBT modules and is therefore suited for the construction of the MV side NPC half-bridge.

Due to the higher power required to be dissipated (3980 W in worst case), the heat sink for the MV side bridge of the TCM-DAB followed a custom design. In Fig. 3.19-a), a representation of the utilized IGBT module is presented. Here, the arrangement of the IGBT-diode pairs is displayed, whereby three of these pairs can be identified in the module package. Given this internal power module arrangement, it would result convenient to design a water-cooled heat sink which directly extracts the losses from the locations where these three IGBT-diode pairs are found. The concept of the designed heat sink is presented in Fig. 3.19-b). Here, the IGBT-diode pairs are directly cooled by enlarged cavities, reducing the thermal resistance of the module's baseplate to the water.

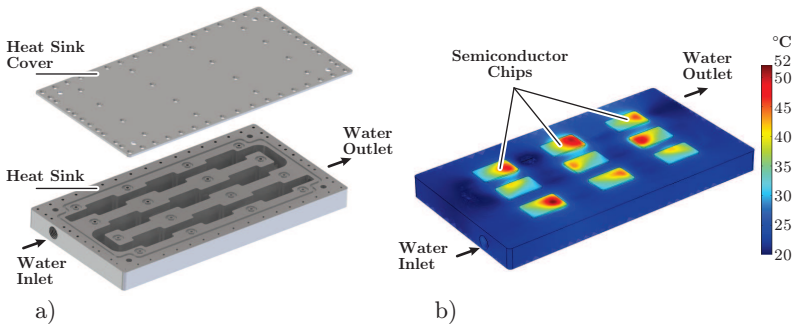
A CAD drawing of the constructed heat sink is shown in Fig. 3.20-a), where the cavities for the efficient cooling of the 9 IGBT-diode pairs



**Figure 3.19:** Water-cooled heat sink concept for TCM-DAB converter. Each of the selected IGBT modules consists of 3 IGBT-diode pairs as shown in a). The respective heat sink is designed for three of the aforementioned IGBT modules, where the water circulation shown in b) is specially designed in order to directly extract the heat from these IGBT-diode pairs.

can be observed together with the water inlet and outlet. The heat sink consists of two pieces, one for the mounting of the IGBT power modules and a sealing cover. The inlet and outlet are built with a conic national pipe thread for secure sealing of the cooling fluid.

A fluid-dynamic/thermal simulation was performed with COMSOL Multiphysics in order to estimate the temperature rise of the designed cooling system. The result of this simulation is shown in Fig. 3.20-b). In this simulation, solid copper pieces generating in total the maximum losses encountered in the MV side TCM-DAB bridge were used in order to study the surface temperature of the heat sink under nominal conditions. The water stream speed was found by matching the system's impedance (found through simulations) to the pump's characteristic, leading to a water speed of 4.56 m/s at the heat sink's inlet. Under these conditions, the maximum heat sink surface temperature rise is  $\Delta T = 32^\circ\text{C}$ . With the value of junction to heat sink thermal resistance (considering thermal paste) extracted from the IGBT module's datasheet, a total temperature rise of  $91^\circ\text{C}$  is reached in each IGBT chip. If a  $20^\circ\text{C}$  water temperature is considered, this temperature rise



**Figure 3.20:** a) CAD drawing of the designed heat sink and its respective cover. A FEM simulation comprising the fluid dynamics as well as the thermal properties was conducted and the results are shown in b).

would result in a total of  $111\text{ }^{\circ}\text{C}$  of the semiconductor's junction, which is well below the recommended limit of  $150\text{ }^{\circ}\text{C}$ .

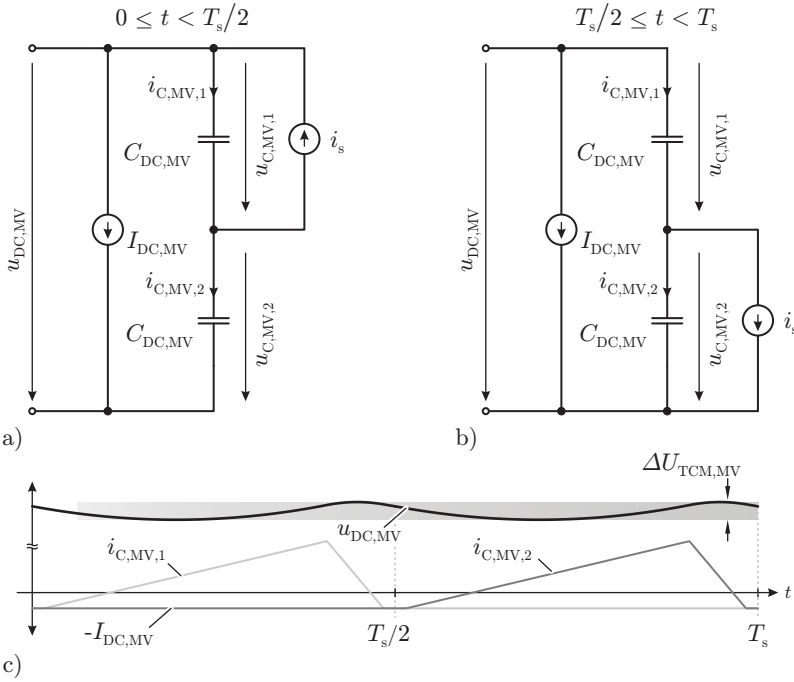
### 3.4.3 DC-link Capacitor Selection

The DC-link capacitor selection is based on two main specifications: capacitance value, for minimum voltage ripple, and RMS current rating. In order to calculate the value of capacitance required for fulfilling a maximum voltage ripple, here defined as 1%, consider the circuits shown in Figs. 3.21-a) and b) valid for the HC-DCM-SRC as well as for the TCM-DAB. Here, the current source  $i_s$  represents the current through the transformer, which flows through the upper capacitor during the first half-cycle (cf. Fig. 3.21-a)) and through the lower capacitor during the second half-cycle<sup>1</sup> (cf. Fig. 3.21-b)). On the other hand, the current source  $I_{DC,MV}$  represents the load at the DC side of the NPC half-bridge, sinking constant current.

As an example, Fig. 3.21-c) qualitatively shows the capacitor currents  $i_{C,MV,1}$  and  $i_{C,MV,2}$  as well as DC-link voltage ripple  $u_{DC,MV}$  for the TCM-DAB converter during one switching period when pure ZCS is achieved.

With the presented equivalent circuits, the currents  $i_{C,MV,1}$  and

<sup>1</sup>These shown equivalent circuits are valid as long as pure ZCS is achieved in the TCM-DAB and 50% duty cycle is utilized the case of the HC-DCM-SRC.



**Figure 3.21:** Equivalent circuit for calculation of the required MV side DC-link capacitance. a) Shows the circuit during the first half-cycle while b) shows the circuit during the second half-cycle. The respective capacitor voltage and capacitor currents for the TCM-DAB MV side DC-link in c) when pure ZCS is achieved.

$i_{C,MV,2}$  in the upper and lower capacitor respectively can be expressed by

$$i_{C,MV,1}(t) = \begin{cases} i_s(t) - I_{DC,MV} & 0 \leq t < T_s/2 \\ -I_{DC,MV} & T_s/2 \leq t < T_s \end{cases} \quad (3.13)$$

$$i_{C,MV,2}(t) = \begin{cases} -I_{DC,MV} & 0 \leq t < T_s/2 \\ -i_s(t) - I_{DC,MV} & T_s/2 \leq t < T_s \end{cases} \quad (3.14)$$

and the respective capacitor voltages are

**Table 3.2:** Selected capacitors and achieved voltage ripple and current rating in MV side of the HC-DCM-SRC and TCM-DAB converter DC-link.

Parameter	HC-DCM-SRC	TCM-DAB
Maximum voltage ripple (pk-to-pk)	1 %	1 %
Required capacitance	45.7 $\mu\text{F}$	62.3 $\mu\text{F}$
Maximum RMS current	75.38 A	112.8 A
Manufacturer	WIMA	EPCOS
Selected capacitor	DCP4P051007G	B32778G1206
Maximum DC voltage	1100 V	1100 V
Capacitance per capacitor	10 $\mu\text{F}$	20 $\mu\text{F}$
Maximum RMS curr. per cap.	9.5 A	15 A
Total N° of paralleled caps.	16	9
Total capacitance $C_{\text{DC,MV}}$	160 $\mu\text{F}$	180 $\mu\text{F}$
Maximum total RMS current	152 A	135 A
Achieved voltage ripple (pk-to-pk)	0.33 %	0.4 %

$$u_{\text{C,MV},1}(t) = \frac{1}{C_{\text{DC,MV}}} \int_0^t i_{\text{C,MV},1}(t_u) \cdot dt_u \quad (3.15)$$

$$u_{\text{C,MV},2}(t) = \frac{1}{C_{\text{DC,MV}}} \int_0^t i_{\text{C,MV},2}(t_u) \cdot dt_u. \quad (3.16)$$

The total DC-link voltage  $u_{\text{DC,MV}}$  is found:

$$u_{\text{DC,MV}}(t) = u_{\text{C,MV},1}(t) + u_{\text{C,MV},2}(t). \quad (3.17)$$

By replacing the respective HC-DCM-SRC and TCM-DAB current waveforms, the maximum and minimum values of the DC-link voltage  $u_{\text{DC,MV}}$  can be found. With the expressions for these maximum and minimum voltages, the relation between the peak-to-peak voltage ripples  $\Delta U_{\text{SRC,MV}}$  and  $\Delta U_{\text{TCM,MV}}$  for the HC-DCM-SRC and TCM-DAB and the DC-link capacitance  $C_{\text{DC,MV}}$  can be calculated, leading to the values of capacitance that fulfil the 1 % voltage ripple:  $C_{\text{SRC,MV}} = 45.7 \mu\text{F}$  and  $C_{\text{TCM,MV}} = 62.3 \mu\text{F}$  for the HC-DCM-SRC and the TCM-DAB respectively.

As stated earlier, the DC-link capacitors possess a defined current rating tightly linked to their operating frequency. Foil capacitors ex-

hibit a good compromise between compactness, current carrying capability and reliability. For this reason, they are exclusively considered in this case for MV side DC-link. Since the current rating of capacitors is highly dependent on specific material properties and dielectric construction, no analytical formulae is available for the estimation of their current limit. Therefore, an extensive search of suitable DC-link capacitors over the available manufacturers' portfolio was performed, whereby the maximum current was extracted from the respective datasheets.

This search lead to the selected capacitors shown in Table 3.2, which fulfil both the required capacitance value and maximum RMS current.

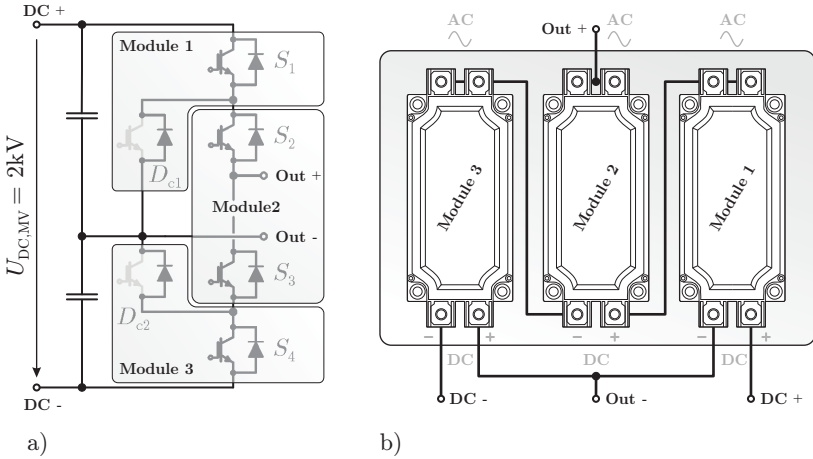
As can be seen from Table 3.2 for the TCM-DAB, the maximum RMS current presents a very stringent requirement, in case of the TCM-DAB, as this specification is closely met while the capacitance requirement is largely over-dimensioned. On the other hand, the HC-DCM-SRC is over-dimensioned in both aspects whereby the selection of the capacitance was also related to the realization of the mechanical assembly.

### 3.4.4 NPC Half-Bridge Arrangement and Copper Busbar Design

The interconnection of the IGBT modules must be carefully realized in order to reduce undesired phenomena related to parasitic inductances during the switching transitions. In the NPC half-bridge, the current of the outer switches  $S_1$  and  $S_4$  in Fig. 2.3 is commutated to their respective clamping diodes  $D_{c1}$  and  $D_{c2}$  when a positive current is turned off by these switches. It is therefore convenient to pair these IGBT and clamping diodes in a module in order to reduce the parasitic inductance of the commutation path. Fig. 3.22-a) shows this arrangement where switch  $S_1$  is coupled with diode  $D_{c1}$  inside module 1, and  $S_4$  and  $D_{c2}$  are coupled in module 3. The inner switches  $S_2$  and  $S_3$  are then arranged in module 2.

This module arrangement results in the interconnections of the three modules as shown in Fig. 3.22-b), whereby 5 copper busbars are required in order to realize the shown connections. These busbars are shown in Fig. 3.23.

The DC-link power terminals are presented in Fig. 3.23-a) and are utilized as input terminals and additionally as part of the DC-link capacitor bank together with the mid-point busbar. The mid-point con-



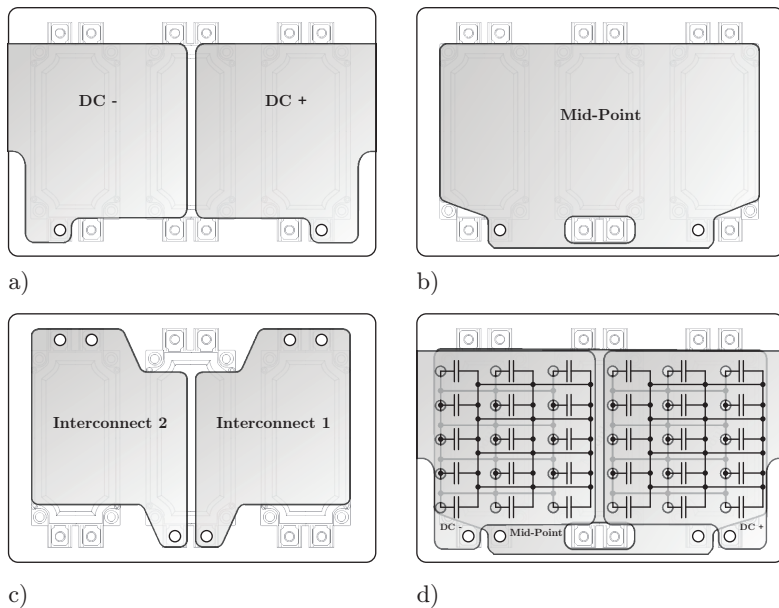
**Figure 3.22:** a) Assignment of the IGBT modules to switch pairs of the MV side NPC half-bridge. This assignment ensures that all commutations occur within the IGBT modules. The interconnections between these IGBT modules when placed on the heat sink are shown in b).

nection, corresponding also to the negative output terminal, is done through the busbar shown in Fig. 3.23-b), which interconnects the negative terminal of module 1 to the positive terminal of module 3. This copper busbar is also used to connect the mid-point terminals of the DC-link capacitors.

The connection between the AC output of module 1 and the positive DC terminal of module 2 is done through the busbar Interconnect 1 while the connection between the AC output of module 3 and the negative DC terminal of module 2 is done through the busbar Interconnect 2, as shown in Fig. 3.23-c). All busbars are built with 0.5 mm copper plates.

The arrangement of the DC-link capacitors is presented in Fig. 3.23-d). Here, the upper busbars are the DC-link positive and negative terminals while the next layer in the stack corresponds to the mid-point busbar.

The assembly process of the capacitor bank is shown in Fig. 3.24. In Fig. 3.24-a), the capacitors are arranged in the required layout and the positive and negative busbars, previously laser cut with all the

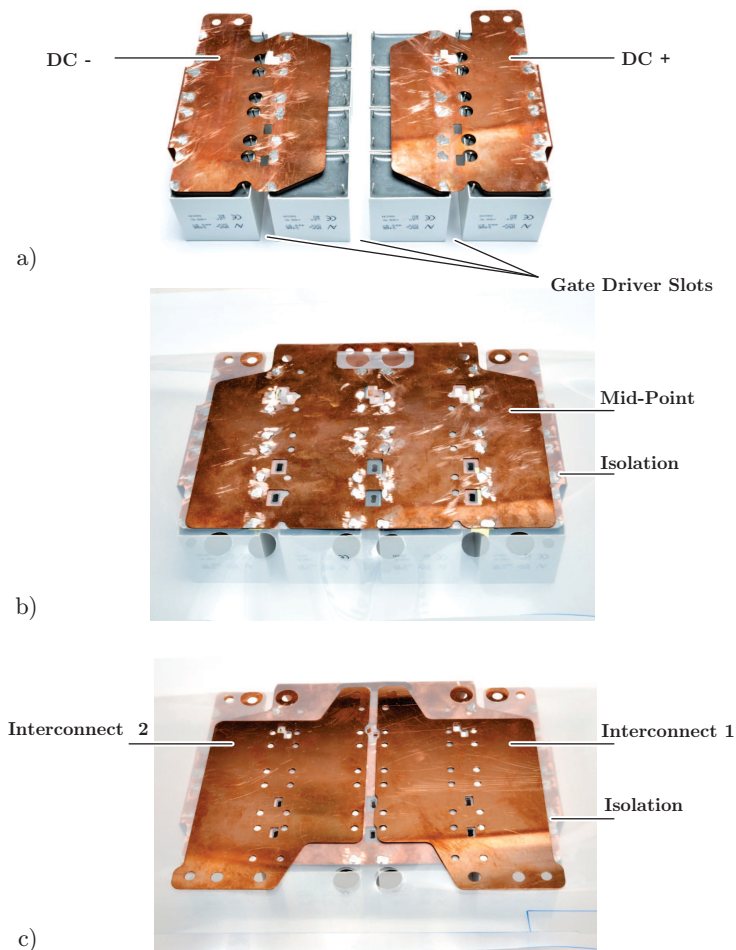


**Figure 3.23:** Power busbars design: a) Positive and negative DC-link busbars; b) Mid-point busbar; c) Interconnection busbars between outer and middle switches; d) Arrangement of DC-link capacitors between mid-point and positive/negative busbars.

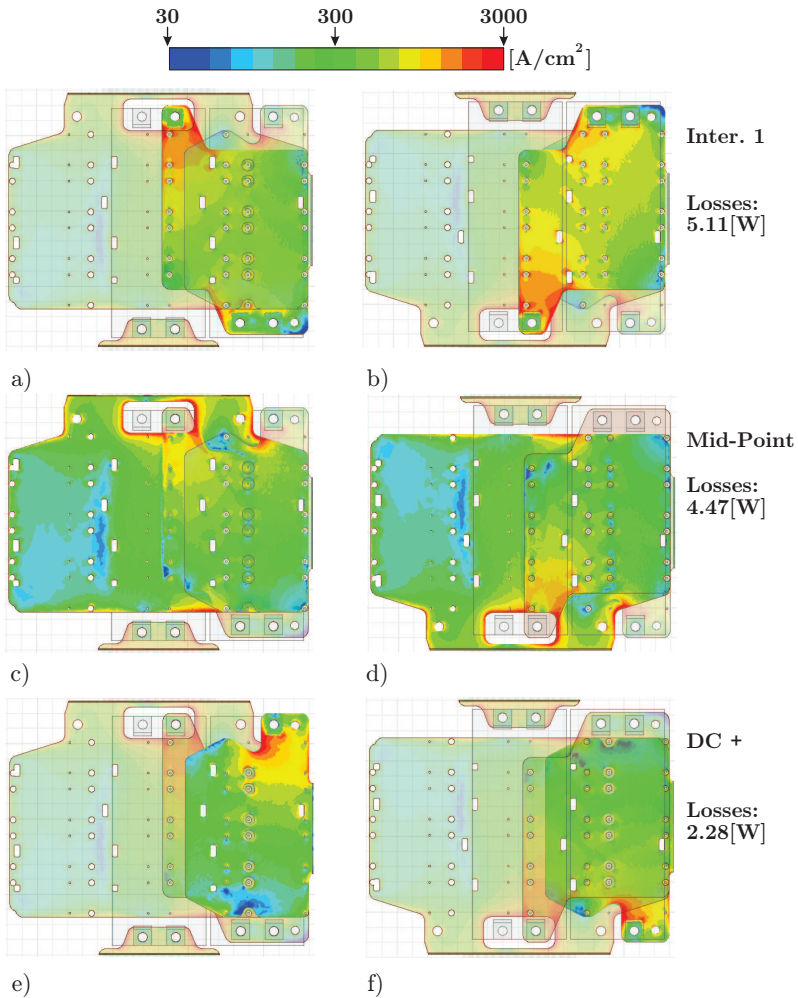
required terminal perforations, are soldered to the respective capacitor pins. Here, also the spacing left for the insertion of the IGBT gate driver is shown. The next layer corresponds to a mylar foil providing the isolation between the DC-side busbars and the next busbar in the stack: the mid-point busbar. In Fig. 3.24-b), this isolation layer and the soldered mid-point busbar are displayed. The last pieces in the capacitor bank assembly are the interconnecting busbars 1 and 2, which are isolated from the mid-point busbar with an additional layer of mylar foil, as shown in Fig. 3.24-c).

It should be noted that these busbars are operated under high currents and at MF level, thus high frequency effects such as skin and proximity are expected to affect their current distribution. In order to analyze this phenomena, FEM simulations utilizing ANSYS Maxwell





**Figure 3.24:** Mechanical assembly of the TCM-DAB MV side capacitor bank. The HC-DCM-SRC capacitor bank was assembled utilizing the same concept. In a), the positive and negative DC terminals are soldered to the respective capacitors. A layer of isolation and the mid-point busbar are added in b) while c) shows the interconnecting busbars after the last layer of isolation has been placed.



**Figure 3.25:** FEM simulations for estimation of current densities and losses in the power busbars: a) Top view of interconnection 1 busbar; b) Bottom view of interconnection 1 busbar; c) Top view of mid-point busbar; d) Bottom view of mid-point busbar; e) Top view of positive busbars; f) Bottom view of positive busbars;

**Table 3.3:** MV side busbars (Interconnect 1, Mid-point and DC+) RMS current for the HC-DCM-SRC and the TCM-DAB converters.

Parameter	HC-DCM-SRC	TCM-DAB
RMS Current	191.9 A	213.8 A

simulation software were performed. The simulation considers the conduction of a sinusoidal current with the nominal RMS value through all busbars involved in conduction of a positive current from the plus DC-link capacitors into the transformer, i.e. busbars Interconnect 1, Mid-Point and DC+ in Fig. 3.23. The values for RMS current in these busbars are shown in Table 3.3. Since it represents a worst case scenario, the RMS value of the current in the TCM-DAB was utilized in order to conduct the simulation, corresponding to 213.8 A. The results for the current distribution and the simulated loss values are presented in Fig. 3.25 for the top and bottom faces of each of the involved busbars. As expected, the highest current concentration, reaching  $3000 \text{ A/cm}^2$ , is found close to the connection to the IGBT modules in all cases.

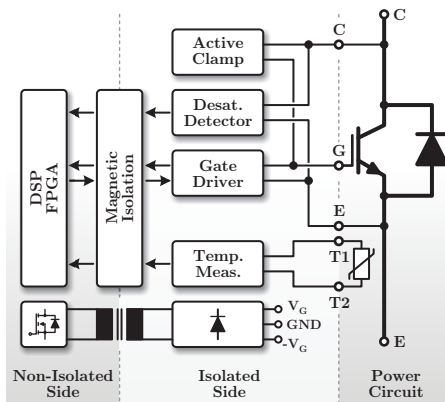
The total losses were calculated based on the simulated current densities, giving a total of 13.2 W for all five power busbars, thus no significant temperature rise is expected.

It should be noted that the arrangement of the power modules as well as the design of all interconnecting busbars is valid for the HC-DCM-SRC and for the TCM-DAB converters since the power and voltage ratings are equal in both cases, thus the values for RMS currents are comparable, as seen in Table 3.3.

### 3.4.5 Gate Driver

The 1.7 kV IGBT modules constitute the key components within the MV side power electronic bridges. For this reason, a gate driver circuit, comprising e.g. feedback signals, protection features and temperature measurement, results very attractive in order to ensure the reliable operation of the power electronic bridge.

Fig. 3.26 shows a block diagram of the gate driver utilized to control all MV side IGBT modules. The gate of the IGBT switch is controlled through a dedicated power stage with independent gate resistors for turn-on and turn-off transitions. A desaturation circuit is incorporated



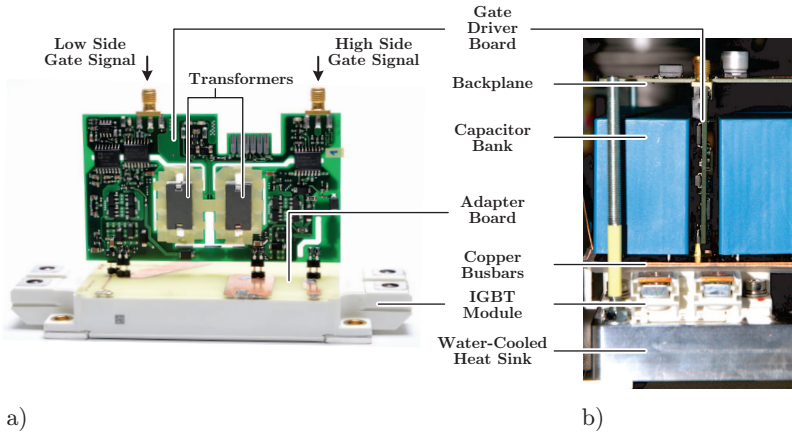
**Figure 3.26:** Block diagram of the gate driver for IGBT modules comprising active clamping; desaturation detection, gate driver power stage, temperature measurement and galvanic isolation from the non-isolated side.

in order to detect over-currents in the switch by measuring the collector-emitter voltage during the on-state of the device. Furthermore, an active clamping circuit is utilized in order to avoid overvoltages in the device during the turn-off process of the switch. The utilized IGBT module incorporates a temperature probe inside the module. This temperature sensor consists of a temperature-dependent resistor, thus the resistance value is converted into a voltage signal by dedicated circuitry.

The gate driver has as input the gate signal and a reset signal utilized in case a fault has been detected and the converter needs to return to normal operation. The feedback signals are a trip flag in case a desaturation has been detected and a ready signal indicating that the driver is in nominal operation. All signals are galvanically isolated through a core-less magnetic isolator.

The complete isolated side of the gate driver is powered through an H-bridge transformer driver feeding a planar transformer built in the gate driver's PCB. The secondary side is then rectified generating the required voltages on the isolated side of the gate driver.

The assembled gate driver PCB is shown in Fig. 3.27-a). This PCB comprises the high side and low side gate drivers, both with the aforementioned functionality. Also in this figure, the planar PCB-integrated transformers utilized to supply the isolated side of the gate driver can



**Figure 3.27:** a) Assembled gate driver and respective adapter board for gate and temperature measurement signals re-routing. In b) the fitting of the gate driver between the DC-link capacitors is displayed.

be seen. The gate signals are provided through independent coaxial inputs and isolated through dedicated gate driver ICs.

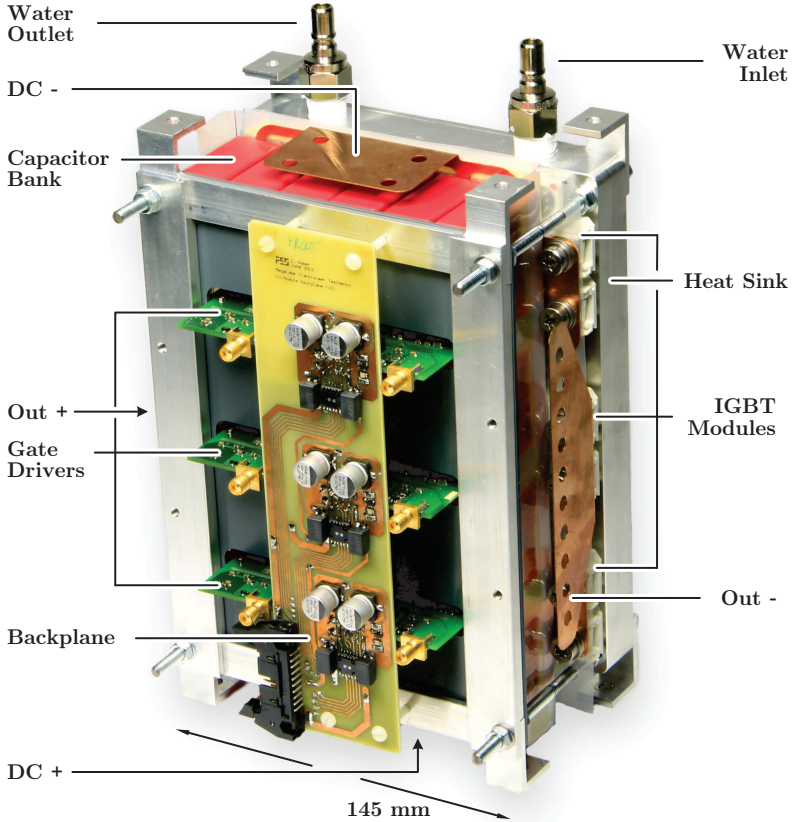
A vertical connection of the gate driver to the IGBT module was selected in order to achieve a compact assembly of the MV side power electronics units. The connection of the gate driver board is done through an adapter board utilized to shift the position of the gate and temperature measurements pins, thus increasing the flexibility in the module's construction.

The complete stack of the MV side bridges is shown in Fig. 3.27-b), comprising from top to bottom: Interconnecting backplane; capacitor bank, copper busbars, IGBT modules and water-cooled heat sinks. The presented gate driver unit is vertically inserted between the DC-link capacitors whereby perforations in the copper busbars were considered in order to connect the gate driver board to the IGBT module's gate and sensing pins.

### 3.4.6 Final Assembled HC-DCM-SRC Module

The final construction of the MV side HC-DCM-SRC converter module is presented in Fig. 3.28. As can be seen, all three IGBT modules are

controlled by their respective gate drivers inserted between the capacitor bank. A single backplane PCB board is utilized in order to route all feedback signals and power supply connections to the gate driver boards. The DC connections are done through the top and bottom faces of the module while the output AC terminals are arranged on both sides of the module. The commercial heat sink where all IGBT modules are attached to is used as basis for ensuring mechanical stability of the module. The TCM-DAB MV side converter module follows a similar construction whereby the backplane integrates conversion to optical signals, as will be shown in Chapter 7.



**Figure 3.28:** Final assembly of the HC-DCM-SRC MV side NPC half-bridge. Concerning labels, DC+, DC-, Out+ and Out-, refer to Fig. 3.22.





# 4

## Low Voltage Side Power Electronics

As discussed in Chapter 2, the LV side bridge of the high-power DC-DC converter comprises a 400 V DC-link. This convenient voltage level was mainly chosen in order to enable the utilization of two mature power semiconductor technologies which are suitable for this voltage level: IGBTs and MOSFETs.

A straightforward solution would comprise exclusively IGBTs, given their high reliability and large safe operating areas while trading efficiency due to their higher switching losses. This is the case for the HC-DCM-SRC, where along the project a simple and robust construction was followed and, additionally, no high currents need to be switched and therefore no considerable benefits would be obtained from a MOSFET-based implementation. In the case of the TCM-DAB, however, the capability of power flow control offered by this topology is achieved by adjusting the converter's duty cycle, which inherently results in high currents being switched off by the LV side full-bridge. For these reasons, an implementation with MOSFET technology of this converter topology would result attractive as the introduction of higher conduction losses is counteracted by a strong reduction in switching losses when compared to a pure IGBT implementation. Furthermore, the current waveforms in each of the switches in the TCM-DAB converter's LV side full-bridge suggest the use of alternative bridge configurations, as will be shown in the first section of this chapter which is exclusively dedicated to the possible bridge arrangements of the TCM-DAB's LV side bridge.

The final construction of the LV side full-bridges of the both HC-

DCM-SRC and TCM-DAB converters will be presented at the end of the chapter.

## 4.1 TCM Modulation Waveforms on LV Side

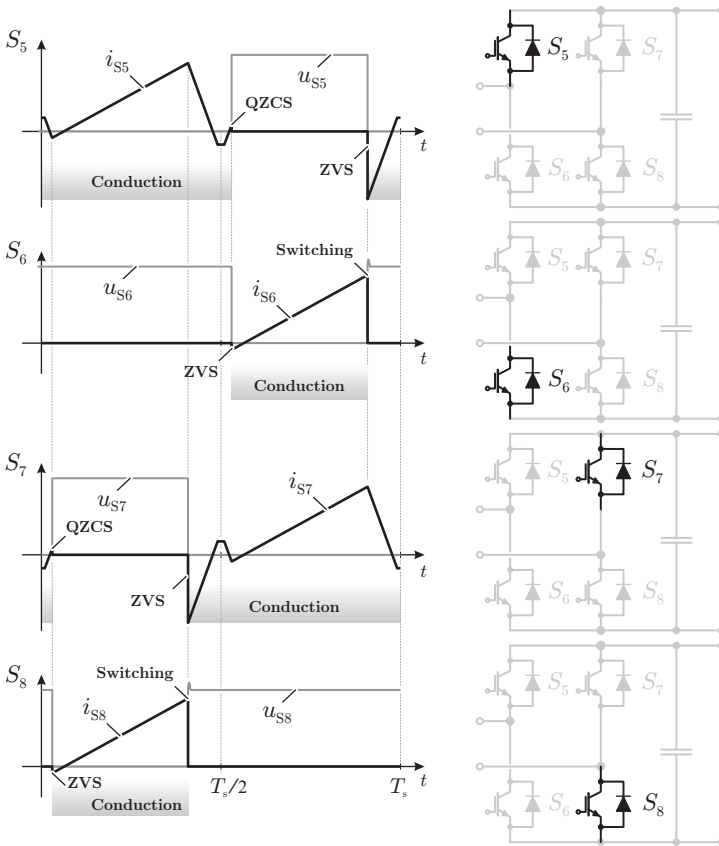
The currents and voltages of the LV side switches of the TCM-DAB converter for power from LV to MV side (cf. Fig. 2.13) during one switching period are presented in Fig. 4.1. These waveforms correspond to the general case of the TCM-DAB, i.e. when QZCS is encountered.

At the beginning of the first half cycle,  $S_7$  turns off a small amount of current (QZCS) which is utilized to achieve ZVS transition in  $S_8$  and therefore reducing the switching losses in this last device. At the end of the LV side's duty cycle,  $S_8$  turns off the full current which is commutated to  $S_7$ , enabling ZVS in this last device. The second half cycle is analogous, whereby first  $S_5$  is operated with QZCS and  $S_6$  is turned on with ZVS. Later this device switches off the full current which is commutated to  $S_5$ , achieving ZVS. It should be noted that  $S_5$  and  $S_7$  conduct a small amount of negative current before their QZCS transitions take place. This current is required in order to achieve QZCS on the MV side NPC half-bridge (cf. Section 2.3.2).

As can be seen from Fig. 4.1, different current waveforms are conducted and switched off by the devices of the LV side full-bridge, whereby the aforementioned behavior can be summarized as follows:

- ▶ Devices  $S_5$  and  $S_7$ , the high side switches, are turned on with ZVS, turned off with QZCS and conduct during a comparatively longer portion of the switching cycle.
- ▶ Devices  $S_6$  and  $S_8$ , the low side switches, are turned on with ZVS, are required to turn-off the peak current and conduct during a comparatively shorter period of the switching cycle.

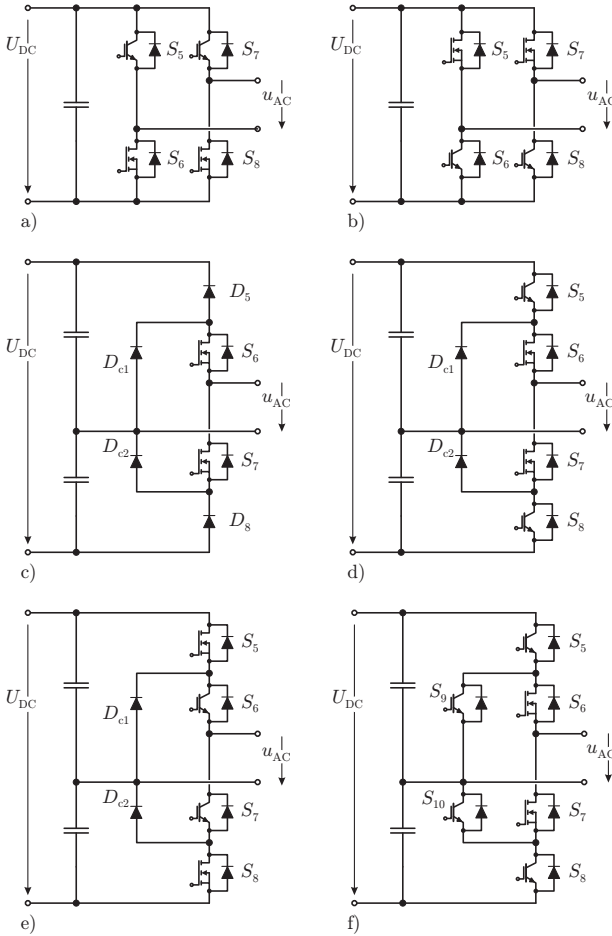
When aiming for a highly-efficient system, these switching transitions and current waveforms suggest the use of semiconductor devices with good switching performance, e.g. MOSFETs, for the low side switches  $S_6$  and  $S_8$  and semiconductor devices with good conduction performance, e.g. IGBTs, for the high side (QZCS operated) switches, i.e. a mixed-bridge. The different options for combining these semiconductor devices into a full-bridge together with the hardware realizations and experimental results will be discussed in the next section.



**Figure 4.1:** Current waveforms through all LV side full-bridge switches. The high side switches  $S_5$  and  $S_7$  are operated in ZCS while the low side switches  $S_6$  and  $S_8$  are operated with ZVS.

## 4.2 Mixed MOSFET/IGBT Bridges

As previously mentioned, a convenient combination of MOSFETs and IGBTs in a full-bridge configuration operated under TCM modulation scheme consists of IGBTs on the high side and MOSFETs for the low side, as shown in Fig. 4.2-a). The modulation scheme described in Section 4.1 can be modified in order to invert the operation of the high



**Figure 4.2:** Options for combination of MOSFETs and IGBTs in a TCM-operated full-bridge for reduction of overall losses: a) MOSFETs on the low side; b) MOSFETs on the high side; and NPC half-bridge variations: c) Unidirectional; d) Bidirectional with asymmetric loss generation, rectifier-enhanced; e) Bidirectional with asymmetric loss generation, inverter-enhanced; f) Bidirectional with symmetric loss generation.

side and low side switches, i.e. in order to operate the low side switches  $S_6$  and  $S_8$  with ZCS while allowing the high side switches  $S_5$  and  $S_7$  to perform the current turn-off. In this case, the arrangement shown in Fig. 4.2-b) would enable a reduction of the overall bridge losses.

This mixed-bridge structure and other variations have been previously reported in literature [78–82] mainly for inverter (hard-switched) applications. However, the combination of the TCM modulation scheme together with the presented mixed-bridge, which enables QZCS operation of IGBTs while the current turn-off is performed only by MOSFETS, has not been previously reported.

The NPC half-bridge topology described in Section 2.1.4 is also a suitable LV side structure for the generation of the TCM waveforms and it is therefore interesting to analyze the different options of mixed-bridge implementations with this arrangement. These options are shown in Figs. 4.2-c), d), e) and f).

If only rectification is required, i.e. power flow from the AC to the DC side, the configuration shown in Fig. 4.2-c) presents a valid solution. In this circuit, only the inner switches  $S_6$  and  $S_7$  are used to switch current while the rectifier diodes are used to feed the current into the DC-link. It should be noted that with this arrangement however, two out of the four switching transitions within a switching period are done with pure ZCS (no QZCS), thus increasing the losses in this type of bridge.

In the case when bidirectional power flow is required, the bridges in Figs. 4.2-d), e) and f) can be used. When operated in rectifier mode, the configuration in Fig. 4.2-d) performs all peak current turn-off events with MOSFETS  $S_6$  and  $S_7$  (thus achieving ZVS) while the IGBTs  $S_5$  and  $S_8$  operate in QZCS mode. If power is transferred from the DC to the AC side, the outer IGBTs  $S_5$  and  $S_8$  are required to turn-off the peak current, thus losing QZCS and increasing the switching losses. On the other hand, if reduction in switching losses is required for inverter operation (power from the DC to the AC side), the arrangement in Fig. 4.2-e) could be used. Here, for the outer switches  $S_5$  and  $S_8$ , MOSFETS are employed as they must switch off the peak current while the inner IGBTs  $S_6$  and  $S_7$  are operated in ZVS/QZCS mode. In rectification mode, however, the peak current must be switched off by the inner IGBTs, thus increasing the switching losses. In these two last arrangements, the asymmetric generation of switching losses results in different nominal power ratings of the switches depending on power flow

direction, if the same junction temperature is assumed in all cases.

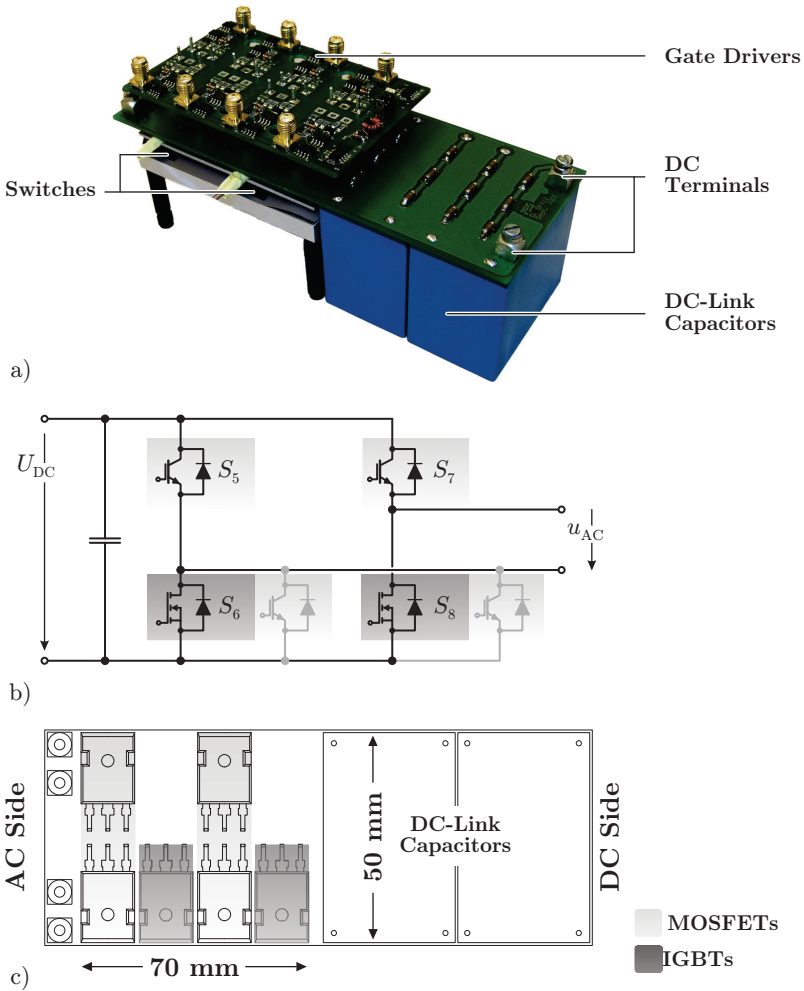
In order to achieve a loss reduction independent of the power flow direction, the bridge presented in Fig. 4.2-f) can be used. This bridge replaces the clamping diodes by active IGBT switches, thus commonly known as Active Neutral Point Clamped (ANPC) bridge [83]. With this structure, the current turn-off can always be performed by the inner switches  $S_6$  and  $S_7$ , independent of the power flow direction, thus enabling the use of MOSFETs in this case and IGBTs for all other switches. The result is a symmetric loss generation with switching of current performed by the MOSFETs while achieving QZCS in all IGBTs.

In order to quantify the improvement achieved by the combination of MOSFETs and IGBTs in a mixed full-bridge configuration, the arrangement shown in Fig. 4.2-a) was built considering a  $U_{DC} = 400$  V LV side DC-link operated at  $f_s = 20$  kHz with a duty cycle corresponding to 20  $\mu$ s on-time per half-cycle. The peak current to be switched is 1000 A.

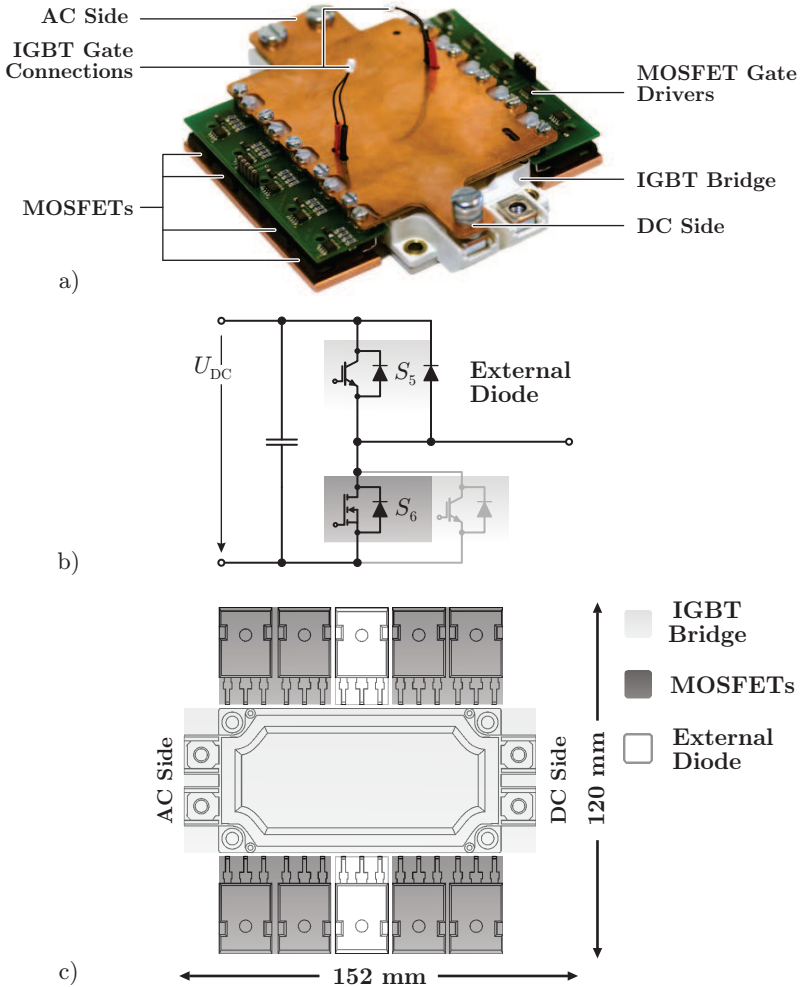
Two concepts were considered for the bridge construction: A single devices-based arrangement with discrete MOSFETs and IGBTs and a modular construction whereby the MOSFETs are arranged around an IGBT module.

The single devices-based bridge hardware realization is shown in Fig. 4.3-a). In this case, the utilized MOSFET is a IPW60R041C6 650 V/77 A CoolMOS from Infineon while the IGBT is a IKW75N60T 600 V/75 A device also from Infineon. These current ratings make it possible to build a mixed full-bridge able to switch 80 A current peak. Fig. 4.3-b) shows the full-bridge built based on these devices. As can be seen, in parallel to the low side MOSFETs, there are parallel-connected IGBTs which will be later used to further reduce the losses of this bridge, as will be shown in Section 4.3. The layout of the components in the printed circuit board displayed in Fig. 4.3-a) is presented in Fig. 4.3-c). The goal of this discrete component construction is the reduction of parasitic effects related to interconnection inductances. In order to switch the 1000 A peak current however, several of these bridges would be necessary, increasing the complexity of the system. For this reason, a second mixed-bridge modular construction is also considered.

The hardware realization of the modular mixed-bridge configuration is depicted in Fig. 4.4-a). The utilized IGBT is in this case the



**Figure 4.3:** Laboratory prototype arrangement for a single device-based realization of the different switches (discrete MOSFETs and IGBTs) full-bridge: a) Picture of the hardware realization; b) Circuit view of the bridge shown in a); c) Components' layout for the realized hardware shown in a). The MOSFETs and IGBTs are placed in close vicinity in order to reduce the value of the parasitic inductance of the interconnections.



**Figure 4.4:** Laboratory prototype arrangement for a module-based mixed-bridge-leg (discrete MOSFETs arranged around an IGBT module) full-bridge: a) Picture of the hardware realization; b) Circuit view of the bridge-leg shown in a); c) Components' layout for the realized hardware shown in a). A total of 8 MOSFETs are placed around the IGBT module whereby external diodes are also incorporated in order to reduce the effects of fast transients caused by the MOSFETs' switching.



Infineon FF600R06ME3 600 V/600 A half-bridge module. In order to match the IGBT module's current rating, designed for 500 A peak, 8 IPW60R041C6 CoolMOS MOSFETs were connected in parallel in order to build  $S_6$  (cf. Fig. 4.4-b)). As with the single devices-based mixed-bridge, the low side switch of the IGBT module is only utilized in Section 4.3 for further loss reduction. In this case only a bridge leg was built, which was used to realize all experimental tests. Two of these half-bridges would be then required to build the complete mixed-bridge. The mechanical layout of the IGBT module and the MOSFETs is shown in Fig. 4.4-c) (DC-link capacitors not shown). In addition to the IGBT module and MOSFETs, external diodes were placed in order to deal with the fast transients generated by the MOSFETs' switching. The modular bridge arrangement has the advantage that only 4 of this mixed half-bridge configurations shown in Fig. 4.4-a) would be necessary to reach the required current rating.

Switching loss measurements at 120 °C junction temperature were performed on the IGBTs and MOSFETs for both constructions. These measurements combined with the datasheet values for the output characteristics of the devices were utilized to compare the performance of the bridges with respect to full MOSFET and full IGBT realizations (considering the same devices as with the respective mixed bridges). The results are summarized as follows:

Single devices-based bridge (Fig. 4.3-a)):

- ▶ Full MOSFET: 512 W
- ▶ Full IGBT: 320.5 W
- ▶ Mixed-bridge: 250.1 W

Module-based bridge (Fig. 4.4-a)):

- ▶ Full MOSFET: 2500 W
- ▶ Full IGBT: 1802 W
- ▶ Mixed-bridge: 1220 W

As can be seen, a reduction of the losses by a factor 2 compared to the full MOSFET construction is achieved for both single device- and module-based constructions when considering the proposed mixed-bridge arrangement, rendering this concept suitable for high-power DC-DC converters operated with TCM modulation schemes. These results

will be summarized in Section 4.4 together with the outcome of a further loss reduction strategy introduced in the next section.

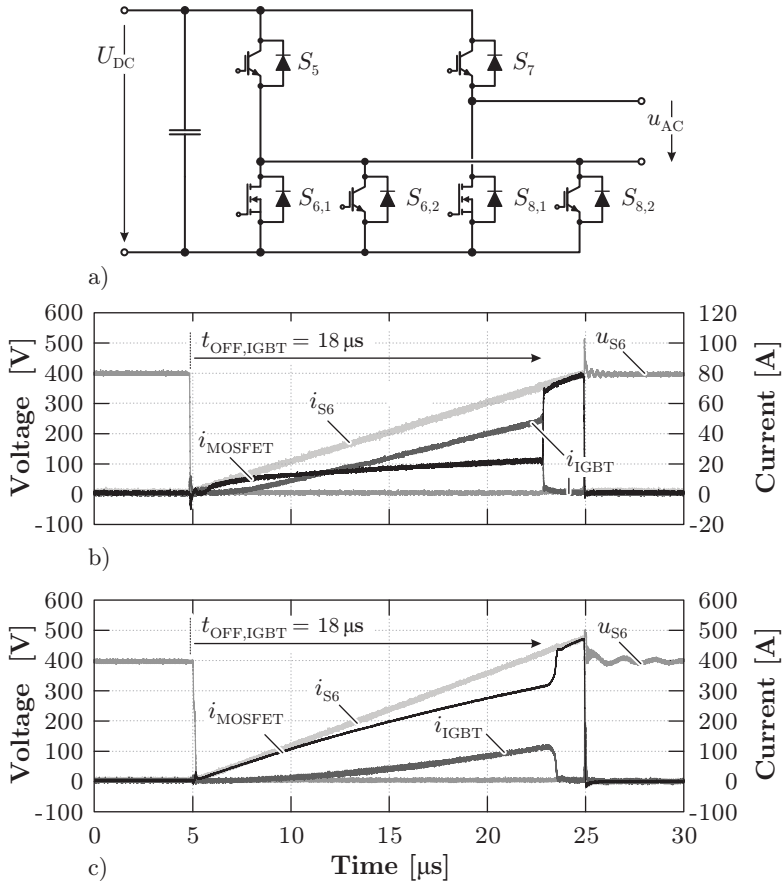
### 4.3 Conduction/Switching Enhancement through MOSFET-IGBT Parallel Connection

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In order to further improve the performance of the presented mixed-bridge under TCM modulation, the MOSFETs of this bridge can be assisted by parallel connected IGBTs which support the conduction phase of the MOSFETs, providing an additional low resistive path for the current, thus reducing the overall conduction losses. This solution is often called hybrid switch and has been previously proposed in [84–86] for inverter solutions, whereby all switches in the bridge are composed of parallel connected IGBTs and MOSFETs. The resulting bridge with the IGBT-assisted conduction is shown in Fig. 4.5-a).

The experimental prototype bridges presented in Section 4.2 already include the additional parallel-connected IGBTs introduced in Fig. 4.5-a), hence the experimental testing of this concept at 120 °C junction temperature was also performed. The operation of the mixed-bridge with hybrid switch is explained with Fig. 4.5-b), where the experimental waveform for one operating point of the single devices-based bridge is presented. This figure shows the current waveform of the hybrid switches in Fig. 4.5-a), corresponding to devices  $S_6$  and  $S_8$  in Fig. 4.1.

In the following, switches  $S_{6,1}$  and  $S_{6,2}$  will be used to explain the bridge's operation, whereby the behavior of  $S_{8,1}$  and  $S_{8,2}$  is analogous. At the beginning of the switching cycle ( $t = 5 \mu\text{s}$  in Fig. 4.5-b)), both the MOSFET  $S_{6,1}$  and the IGBT  $S_{6,2}$  are turned on. Assuming  $S_7$  was previously in on-state from the freewheeling interval, the output current flows through both the IGBT and the MOSFET, providing two parallel paths for the current, leading to reduced conduction losses. Before the end of the respective duty cycle (20  $\mu\text{s}$  in Fig. 4.5-b)), the IGBT is turned off, thus the load current is entirely commutated to the MOSFET. Virtually no losses are generated during this commutation since the MOSFET is in on-state, keeping the IGBT's blocking voltage close to zero. At the end of the duty cycle, the MOSFET performs the turn-off of the current, thus generating comparatively low switching losses.



**Figure 4.5:** a) Mixed full-bridge comprising IGBTs in parallel with the low side MOSFETs in order to reduce the conduction losses of the bridge; b) Experimental waveform of the hybrid switch in the single devices-based prototype with an IGBT turn-off at  $t_{OFF,IGBT} = 18 \mu$ s; c) Experimental waveform of the hybrid switch in the module-based prototype with an IGBT turn-off at  $t_{OFF,IGBT} = 18 \mu$ s;

The result of the aforementioned switching strategy for the hybrid switch is the optimal utilization of the available semiconductor devices, whereby mainly the IGBT is utilized for the conduction of current and

the MOSFET is in charge of the current switch-off.

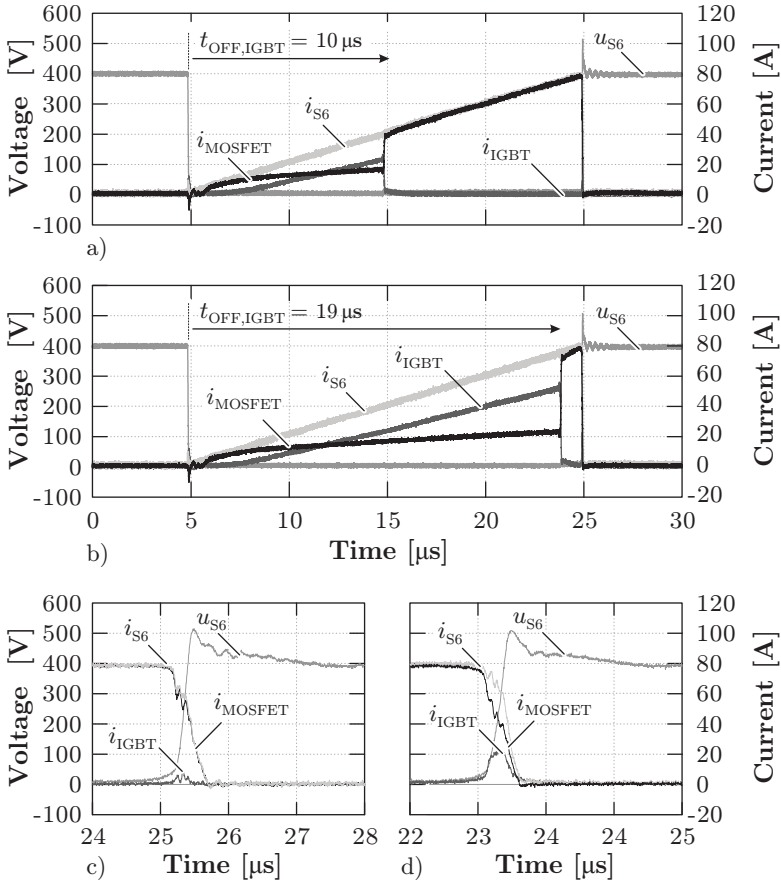
The module-based mixed-bridge comprising the introduced hybrid switch was also tested under these conditions, the results of this test are displayed in Fig. 4.5-c). In this case, the parasitics present in the IGBT-MOSFET connection result in an unfavorable current sharing, as will be explained later in this section.

The selection of the point time at which the IGBT turns off affects the sharing of losses in the parallel connected MOSFET and IGBT. This phenomenon is explained through Fig. 4.6. If  $t_{\text{OFF,IGBT}}$  is selected short, as presented Fig. 4.6-a) for  $t_{\text{OFF,IGBT}} = 10 \mu\text{s}$ , the MOSFET would conduct for a comparatively long portion of the switching cycle, leading to higher conduction losses due to the higher on-state resistance in comparison to the IGBT. On the other hand, if  $t_{\text{OFF,IGBT}}$  is made long, as shown in Fig. 4.6-b) for  $t_{\text{OFF,IGBT}} = 19 \mu\text{s}$ , the best utilization of the switches' conduction potential is achieved, whereby the MOSFET only conducts the full load current during a small portion of the duty cycle.

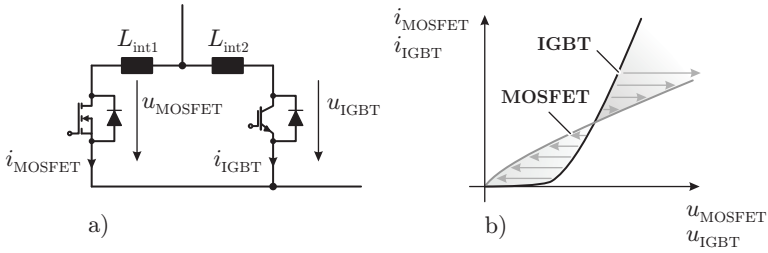
In this last case however, switching losses are encountered in the IGBT due to the limited time available for recombination of its internal charge carriers, as explained in Section 3.1 for the MV side semiconductors. This effect is seen in Fig. 4.6-d) where a detailed view of the MOSFET turn-off process for the case presented in Fig. 4.6-b) is depicted. As can be seen, a visible current spike through the IGBT is present during the turn-off process of the MOSFET, leading to switching losses in the IGBT. It should be noted that this current spike in the IGBT is not present when observing Fig. 4.6-c), corresponding to the detailed MOSFET's switching process for the conditions presented in Fig. 4.6-a).

As a consequence, the selection of  $t_{\text{OFF,IGBT}}$  is a trade-off between MOSFET conduction losses and IGBT switching losses and its optimized value results from the minimization of the overall losses of the mixed-bridge.

Since the modelling of the IGBT's internal charge dynamics requires semiconductor parameters not available in the device's datasheet, this optimization was experimentally performed for the single devices- and module-based bridges by measuring the total conduction and switching losses of both MOSFETs and IGBTs while increasing stepwise the value of  $t_{\text{OFF,IGBT}}$  starting from  $t_{\text{OFF,IGBT}} = 0$ . In case of the single devices-based bridge, the optimal timing is  $t_{\text{OFF,IGBT}} = 19 \mu\text{s}$  (for 80 A peak)



**Figure 4.6:** Trade-off encountered with the selection of  $t_{\text{OFF,IGBT}}$ . When selected short as in a), the MOSFET conduction losses are increased while the IGBT's switching losses are reduced, as seen in c) where a detailed view of the switching process of a) is shown. On the other hand, if  $t_{\text{OFF,IGBT}}$  is chosen large as in b), the conduction losses of the MOSFETs become considerable and switching losses are encountered in the IGBTs, as shown by the current spike in the IGBT's current in d).



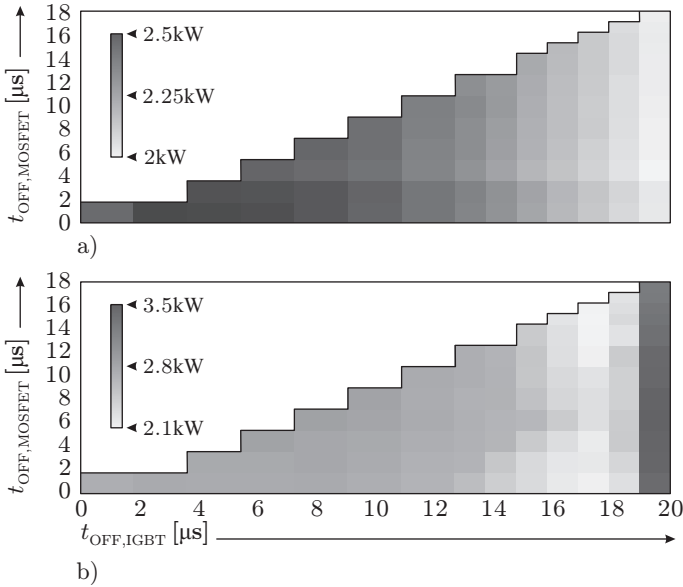
**Figure 4.7:** Effect of parasitic inductance in the interconnection of the IGBT and the MOSFET shown in a). The output characteristics of the MOSFET and the IGBT shown in b) together with the parasitic inductance deteriorate the performance of the hybrid switch and result in an uneven current sharing between the two devices.

leading to total losses of 170.9 W. In case of the module-based bridge, the optimal timing is  $t_{\text{OFF,IGBT}} = 17 \mu\text{s}$  resulting in 1173 W of losses (for 500 A peak) .

As shown in Fig. 4.5-c), the current sharing between the MOSFET and the IGBT presents slow dynamics. This phenomenon is related to parasitic inductances in the interconnection between the MOSFET and the IGBT, as analyzed in [84]. Fig. 4.7 can be used to explain this effect. The output characteristics of the MOSFET and IGBT show that as long as the current is low, it is conducted by the MOSFET, since it offers lower impedance for the current (cf. Fig. 4.7-b)). As the current increases, the voltage drop in the MOSFET becomes higher than in the IGBT, thus the current starts to commute to the IGBT as seen at the beginning of the conduction phase of the single devices-based bridge (cf. Fig. 4.5-b)). However, the parasitic inductances  $L_{\text{int1}}$  and  $L_{\text{int2}}$  in the interconnection of the MOSFET and IGBT increase the time required to commute the current from the MOSFET to the IGBT, given the relatively small voltage applied to them, which is only the difference between the IGBT and MOSFET forward voltage drops.

In order to overcome this problem, a delay  $t_{\text{ON,MOSFET}}$  in the turn-on signal of the MOSFET is introduced, leaving only the IGBT conducting for a portion of the duty cycle. This way, the MOSFET is only turned on when the IGBT offers a lower impedance path for the current, improving the current sharing between these two devices.

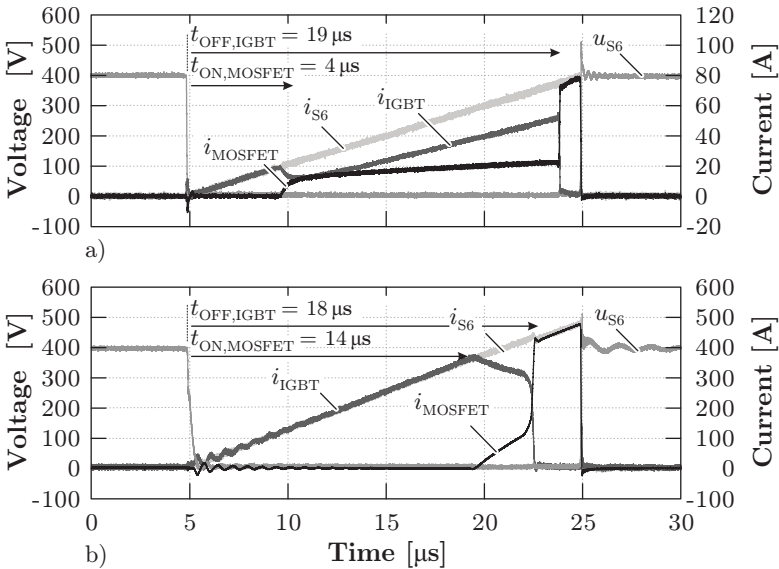
The delay  $t_{\text{ON,MOSFET}}$  introduces a new degree of freedom in the



**Figure 4.8:** 2D optimization for the switching times  $t_{\text{OFF,IGBT}}$  and  $t_{\text{ON,MOSFET}}$ , aiming for minimization of overall bridge losses: a) Single devices-based bridge; b) Module-based bridge.

operation of the hybrid switch, whereby a 2D optimization ( $t_{\text{OFF,IGBT}}$  and  $t_{\text{ON,MOSFET}}$ ) is required in order to find the values of these two variables which minimize the total losses of the bridge. This optimization was performed for both single devices- and module-based mixed-bridges by stepwise modifying the values of  $t_{\text{OFF,IGBT}}$  and  $t_{\text{ON,MOSFET}}$  while measuring all switching and conduction losses. The results of this sweep are found in Fig. 4.8-a) and b) for the single devices- and module-based bridges respectively. Here, the values for losses are scaled in order to reach the desired 1000 A peak current with both bridges.

For the single devices-based bridge, the optimized timings correspond to  $(t_{\text{OFF,IGBT}}, t_{\text{ON,MOSFET}}) = (19 \mu\text{s}, 4 \mu\text{s})$ . The good current sharing already available in this bridge due to the comparatively small parasitic components leads to a small value  $t_{\text{ON,MOSFET}}$ . On the other hand, the high value of  $t_{\text{OFF,IGBT}}$  is related to a fast recombination process in the IGBT.

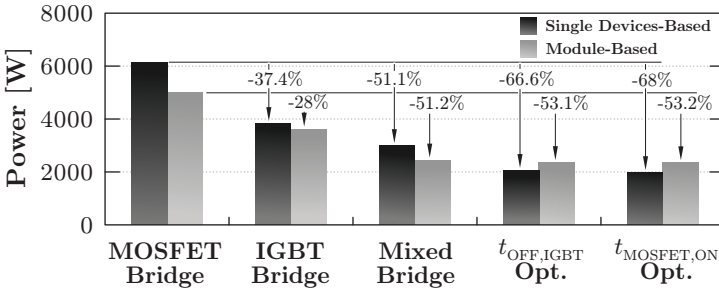


**Figure 4.9:** Waveforms for the a) single devices-based and b) module-based bridges with their respective optimized switching times  $t_{\text{OFF,IGBT}}$  and  $t_{\text{ON,MOSFET}}$ .

For the module-based bridge the optimal switching times correspond to  $(t_{\text{OFF,IGBT}}, t_{\text{ON,MOSFET}}) = (18 \mu\text{s}, 14 \mu\text{s})$ . The value of  $t_{\text{ON,MOSFET}}$  is comparatively large due to the larger parasitic inductances encountered in this construction, given the larger dimensions of the bridge (cf. Fig. 4.4). As a consequence, in order to achieve a current sharing that ensures minimal losses, the conducted current of the IGBT is increased by increasing the value of  $t_{\text{ON,MOSFET}}$ . It should also be noted that the value of  $t_{\text{OFF,IGBT}}$  is smaller in comparison to the single devices-based construction, phenomena possibly related to the longer recombination time constant of the module's semiconductors in comparison to the discrete IGBTs of the single devices-based arrangement.

The final waveforms for the aforementioned optimized values of  $t_{\text{OFF,IGBT}}$  and  $t_{\text{ON,MOSFET}}$  are shown in Figs. 4.9-a) and b) for the single devices- and module-based bridges respectively. The results of this optimization compared to the other presented realizations are discussed in the next section.





**Figure 4.10:** Summary of the obtained losses for the different considered full-bridges and the reduction reached with the introduced combination of IGBTs and MOSFETs in mixed-bridge and hybrid switch arrangements.

## 4.4 Summary and Comparative Evaluation

The analyzed mixed MOSFET/IGBT full-bridges possess different current ratings due to the utilized components in each realization. In order to compare the single device- and module-based constructions with respect to losses, the obtained results are scaled in order to reach the desired current rating (cf. Table 2.1) with both concepts.

Fig. 4.10 shows a summary of these scaled loss values for the different bridge realizations and switching time optimizations discussed in the previous sections. Taking a full MOSFET realization (all four switches of the full-bridge implemented with MOSFETs) as reference system, a loss reduction higher than 50% is obtained for the module- as well as for the single devices-based construction by implementing the mixed-bridge presented in Fig. 4.2-a). In the single devices-based realization (cf. Fig. 4.3), the adjustment of the switching times ( $t_{OFF,IGBT}$  and  $t_{ON,MOSFET}$ ) leads to a total reduction of 68% with respect to the full MOSFET realization.

In the module-based mixed-bridge (cf. Fig. 4.4) the additional loss reduction achieved with the introduction of the hybrid switch is comparatively low with respect to the single devices-bridge arrangement. This is due to the large value of the interconnecting inductances  $L_{int1}$  and  $L_{int2}$  in this construction, which does not allow an effective utilization of the MOSFET and IGBT conduction capabilities.

## 4.5 Design and Construction of the LV Side Full-Bridges

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The construction of the LV side bridges follows different design targets for the HC-DCM-SRC and the TCM-DAB converters. For the HC-DCM-SRC an approach comprising robust and reliable IGBT switches and other of-the-shelf components was preferred. On the other hand, for the TCM-DAB other switch technologies, e.g. MOSFETs were considered in order to increase the converter's efficiency. This concept leads to the construction of several customized parts, as will be discussed in the next subsections.

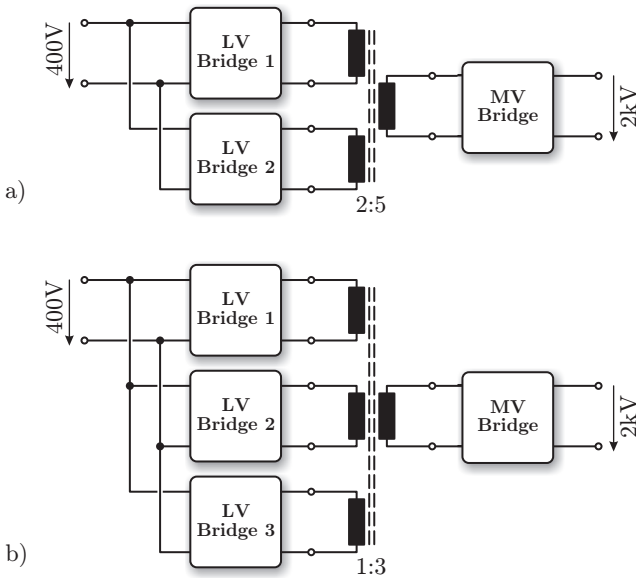
For these reasons, in contrast to the MV side NPC half-bridge, considerable differences are found in the design of the HC-DCM-SRC and TCM-DAB LV side bridges, and therefore the design steps described in the following, comprising semiconductor selection, heat sink design/selection, DC-link capacitor selection and mechanical arrangement, will be mostly independently treated for the two analyzed converters.

### 4.5.1 Semiconductor Selection

Different semiconductor devices are utilized in both designed converters given the different targeted goals. In case of the HC-DCM-SRC, a reliable and robust design comprising only IGBT switches is preferred while higher switching losses, i.e. lower efficiency, are accepted. On the other hand, in order to modularize the design, the same semiconductor package as in the MV side bridge, the EconoDUAL package, is preferred. For these reasons, the highest current rated 600 V IGBT modules in EconoDUAL package were considered. Among this group, the 600 A Infineon FF600R06ME3 power module was readily available and was therefore selected for the construction of the HC-DCM-SRC LV side full-bridge.

In order for the losses in the IGBT modules to stay within the specified values, two identical IGBT-based full-bridges were built for the LV side of the HC-DCM-SRC converter, i.e. four FF600R06ME3 half-bridge modules. It should be noted that, given the output characteristic of IGBTs, no considerable reduction in losses is achieved by paralleling IGBT modules.

In case of the TCM-DAB, the high switched currents suggest the use

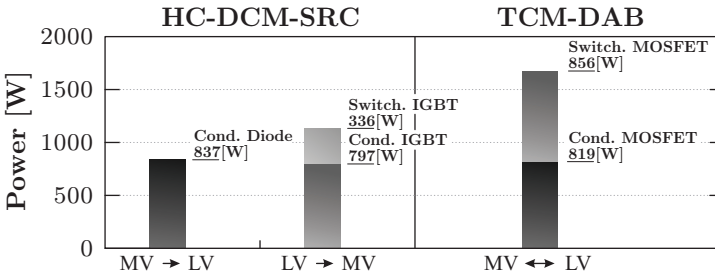


**Figure 4.11:** Splitting of bridges on the LV side of the a) HC-DCM-SRC and b) TCM-DAB converters.

other semiconductor technologies, e.g. MOSFETs, in order to increase the converter's efficiency. The mixed-bridge described in the previous section comprises the IPW60R041C6 650 V/77 A CoolMOS which features a  $41\text{ m}\Omega$  on-state resistance and is built with TO-247 packages. Newer semiconductor devices are readily available which feature on-state resistances as low as  $19\text{ m}\Omega$ , therefore competing in current rating with IGBT switches in the same package (TO-247).

For this reason, a redesign of the bridges presented in Section 4.2 comprising only the STY112N65M5 650 V/96 A MOSFET from ST was considered. This device features a  $19\text{ m}\Omega$  on-state resistance and therefore the utilization of a mixed-bridge in order to reduce the conduction losses by implementing IGBT switches would only result in a marginal improvement in the converter's efficiency and was finally discarded for the construction of the TCM-DAB's LV side bridge.

In order to deal with the high switched/conducted currents, several devices were connected in parallel. Given the resistive behavior of MOSFETs, this parallel connection greatly favors the reduction of con-



**Figure 4.12:** Calculated/measured values for conduction and switching losses in the LV side bridge of the HC-DCM-SRC and TCM-DAB converters for dimensioning of the cooling system.

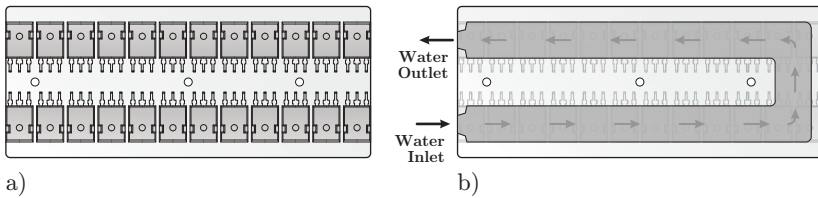
duction losses. Furthermore, in order to modularize the design, the LV side bridge consists of three identical full-bridges whereby each switch consists of six paralleled STY112N65M5 MOSFETs.

Fig. 4.11 shows the aforementioned bridge arrangement with two IGBT-based full-bridges for the LV side of the HC-DCM-SRC (cf. Fig. 4.11-a)) and three MOSFET-based full-bridges for the TCM-DAB converter (cf. Fig. 4.11-b)).

With the selected semiconductor devices and the amount of devices utilized in both LV side bridges, the bridge losses can be calculated in order to proceed with the further steps in the converter design. In the case of the IGBT module for the HC-DCM-SRC, datasheet parameters were extracted for conduction and switching losses. In this case, given the lower blocking capability and therefore the faster recombination time, no dynamic effect of the charge was assumed, whereby the datasheet values for turn-off losses were considered.

In case of the TCM-DAB, the switching losses were experimentally measured. For the conduction losses, the on-state resistance value at  $110^\circ$  was utilized. These calculations led to the loss values presented in Fig. 4.12 for nominal transferred power (166 kW).

The largest share of losses in the HC-DCM-SRC corresponds to conduction for both power flow directions, given the low switched currents and the relatively good switching performance of the selected 600 V IGBTs in comparison to the semiconductors on the MV side. In case of the TCM-DAB, the loss sharing is symmetric with respect to power flow direction due to the utilization of MOSFETs. This converter presents



**Figure 4.13:** Water-cooled heat sink concept for the TCM-DAB’s LV side. The array of MOSFETs is arranged as shown in a), whereby the water channel in the aluminum heat sink is positioned directly under the semiconductor packages as shown in b).

higher overall losses mainly due to the high switched currents in spite of the use of MOSFETs for its construction.

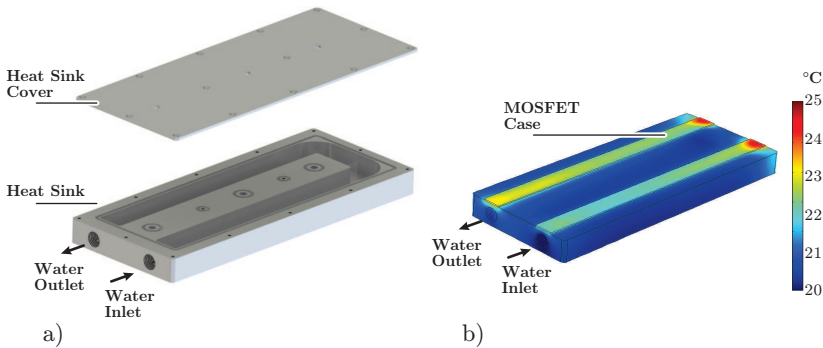
With the estimated values for losses in both converters, the further steps in the bridges’ design will be presented, starting with the heat sink dimensioning.

### 4.5.2 Heat Sink Design

Since the LV side bridge of the HC-DCM-SRC comprises IGBT modules on EconoDUAL package, as in the MV side, the same commercial heat sink, i.e. the MQT1914 water-cooled heat sink from MaxQ Technology, is utilized in order to further simplify the converter’s design. As stated earlier, this heat sink is designed to extract up to 3 kW of losses from the IGBT modules and is therefore well suited for the HC-DCM-SRC’s LV side bridge.

For the TCM-DAB converter, given the utilization of several paralleled MOSFETs in TO-247 package, custom made water-cooled heat sinks were designed in order to conveniently accommodate these devices. Each of the three TCM-DAB LV side full-bridges consists of total of 24 devices. These devices were placed on a cold plate as shown in Fig. 4.13-a), whereby the heat sinks are designed to extract one third of the total losses, i.e. 558 W. The water channel inside this heat sink is displayed in Fig. 4.13-b). As can be seen, this channel is placed directly underneath the MOSFET’s case, thus achieving an efficient heat extraction from the semiconductor’s junction.

A CAD drawing of the designed LV side heat sink is presented in

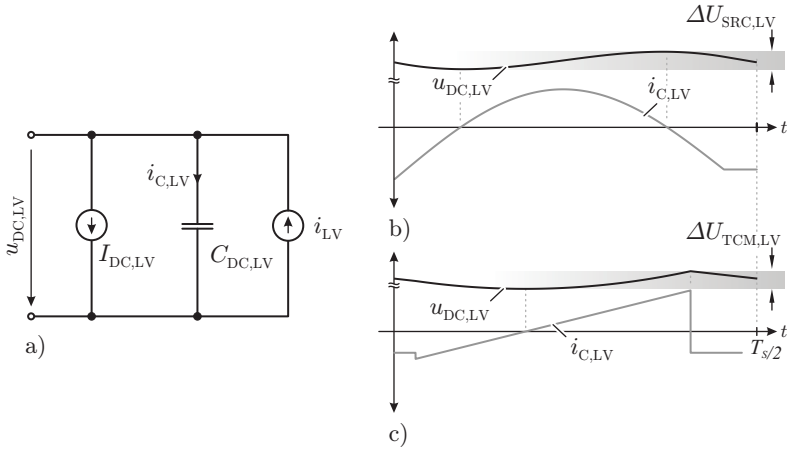


**Figure 4.14:** a) CAD drawing of the designed TCM-DAB LV side heat sink and its respective cover. A FEM simulation comprising the fluid dynamics as well as the thermal physics was conducted and the results are shown in b).

Fig. 4.14-a) which was utilized to conduct a fluid dynamics/thermal FEM simulation with COMSOL multiphysics, with the results shown in Fig. 4.14-b). Here, the MOSFET cases were replaced by metal stripes generating in total 558 W of losses while the cooling fluid speed was calculated for an inlet temperature of 20 °C based on the simulated heat sink's impedance and the pump characteristic. As can be seen, the heat sink's hotspot is found at the right-most semiconductor devices (cf. Fig 4.13-b) due to their comparatively larger distance to the water channel. It should be noted, however, that the water to hotspot temperature rise reaches only 5 °C in worst case. With this temperature rise and a total power dissipation per switch of 23.3 W (558 W/24), a maximum temperature rise from cooling fluid to junction of  $\Delta T = 23.3$  °C is expected, reaching a maximum junction operating temperature of  $T_j = 43.3$  °C considering the aforementioned cooling fluid inlet temperature of 20 °C.

### 4.5.3 DC-link Capacitor Selection

For the selection of the LV side capacitors, a similar analysis as the one presented for the MV side NPC half-bridge is utilized, which is valid for the HC-DCM-SRC as well as for the TCM-DAB converters. The respective equivalent circuit is presented in Fig. 4.15-a) whereby the full-bridge generating current  $i_{LV}$ , i.e. the rectified AC-link current,



**Figure 4.15:** a) Equivalent circuit for calculation of required LV side DC-link capacitance. The respective capacitor voltage and current for the HC-DCM-SRC and the TCM-DAB LV side DC-link capacitors are shown in b) and c).

is replaced by a current source and the DC side current is assumed constant and equal to  $I_{DC,LV}$ . With these definitions, the LV side DC-link voltage  $u_{DC,LV}$  is calculated as follows:

$$u_{DC,LV}(t) = \frac{1}{C_{DC,LV}} \int_0^t i_{C,LV}(t_u) dt = \frac{1}{C_{DC,LV}} \int_0^t (i_{LV}(t_u) - I_{DC,LV}) dt \quad (4.1)$$

where  $C_{DC,LV}$  corresponds to the LV side DC-link capacitance.

The capacitor current  $i_{C,LV}$  for the HC-DCM-SRC during the positive half-cycle is shown in Fig. 4.15-b) and in c) for the TCM-DAB converter. The rectified current  $i_{C,LV}$  of the HC-DCM-SRC converter corresponds to the complete sine pulse while in the case of the TCM-DAB this current corresponds to the Interval III of the triangular current conduction (cf. Fig. 2.12). The peak value of current in the HC-DCM-SRC and in the TCM-DAB converters is 711 A and 1216 A respectively.

In order to reach a 1 % peak-to-peak voltage ripple in  $u_{DC,LV}$  capacitance values of  $C_{MV, SRC} = 667 \mu\text{F}$  and  $C_{MV, TCM} = 676 \mu\text{F}$  are required for the HC-DCM-SRC and the TCM-DAB respectively.

The RMS current rating is the next key feature the DC-link capaci-

**Table 4.1:** Selected capacitors and achieved voltage ripple and current rating in LV side of the HC-DCM-SRC and TCM-DAB converter DC-link.

Parameter	HC-DCM-SRC	TCM-DAB
Required capacitance	188 $\mu\text{F}$	243 $\mu\text{F}$
Maximum RMS current	274 A	331 A
Voltage ripple (pk-to-pk)	1 %	1 %
Capacitor manufacturer	VISHAY	EPCOS
Capacitor model	MKP18486154	B32774D42
Maximum voltage	450 V	450 V
Capacitance per capacitor	15 $\mu\text{F}$	22 $\mu\text{F}$
Maximum RMS curr. per cap.	10 A	9 A
Total N <sup>o</sup> of paralleled caps.	32	44
Total Capacitance $C_{\text{DC,LV}}$	480 $\mu\text{F}$	968 $\mu\text{F}$
Maximum total RMS current	320 A	396 A
Achieved voltage ripple (pk-to-pk)	0.4 %	0.25 %

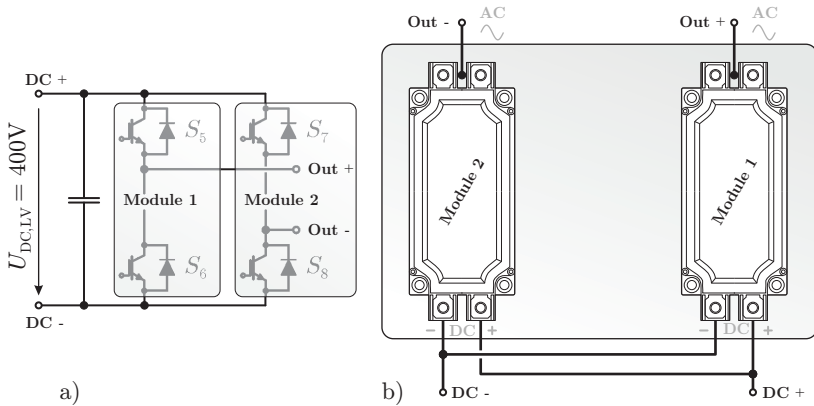
tors are required to fulfil. In order to achieve the required RMS current rating, several capacitors, in this case restricted to foil capacitors, are connected in parallel. An exhaustive search among foil capacitors manufacturer's portfolio led to the selection shown in Table 4.1. Here it can be seen that the RMS current rating results in a more stringent requirement as it determines in both cases the required number of capacitors and therefore the total capacitance whereby the voltage ripple remains well below the specified 1 %.

#### 4.5.4 Full-Bridge Power Circuit Design

Given the considerable differences in the construction of the HC-DCM-SRC and the TCM-DAB converter's LV side bridges, several differences can be found in their power circuit arrangement and therefore this topic will be independently presented for these two converters.

Each of the two full-bridges utilized in the HC-DCM-SRC consists of two half-bridge IGBT modules. The construction of this bridge is therefore straightforward since these modules are originally designed to operate in this configuration, reducing potential overvoltages during the switching transients. Fig. 4.16-a) shows the LV side full-bridge circuit and the assignment of modules to both bridge legs. The selected water-cooled heat sink for these semiconductors is designed to cool three of



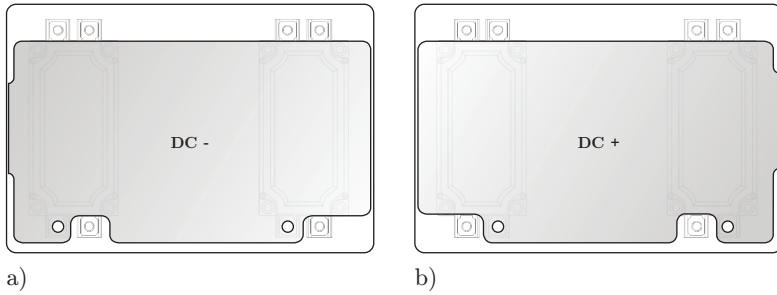


**Figure 4.16:** a) Assignment of the IGBT modules to switch pairs of the LV side HC-DCM-SRC full-bridge. The interconnections between these IGBT modules when placed on the heat sink are shown in b).

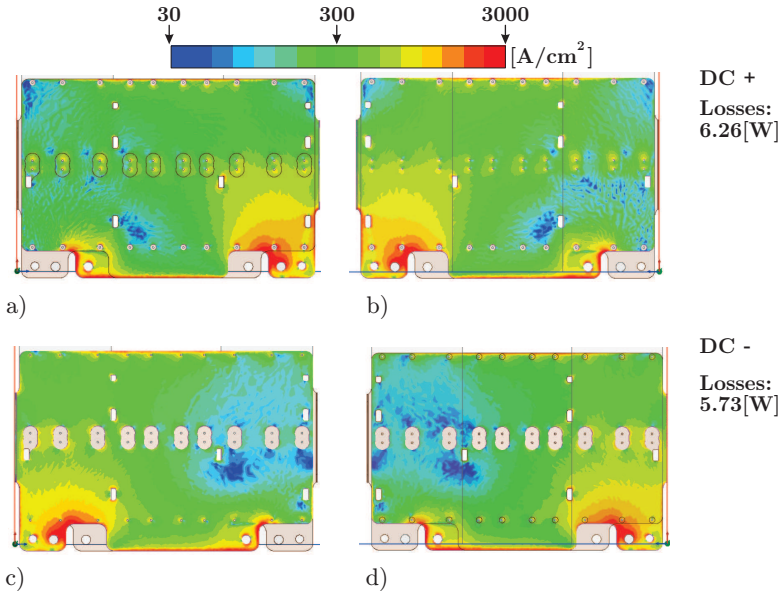
these modules, whereby in this case the two outer-most positions are used, as shown in Fig. 4.16-b). Here, also the required interconnecting busbars can be identified, which consist namely of the positive and DC-link busbars and the output terminals of the bridge, as presented in Fig. 4.17. The two DC-link busbars, consisting of 0.5 mm laser-cut copper plates, are also utilized as part of the capacitor bank, where the capacitors are directly soldered to these busbars in a similar way as shown in Fig. 3.24 for the MV side bridges.

Due to the high currents and MF level, FEM simulations were conducted in order to quantify the losses in the LV bridge busbars and to visualize the current density distribution caused by high frequency effects. The simulation consists of imposing a rectified sinusoidal current with peak value value of the sine wave at nominal power for HC-DCM-SRC, which amounts to 479.87 A. The results of this simulation, performed in ANSYS Maxwell, are displayed in Fig. 4.18. As expected, in all cases the highest current densities, with a peak value close to  $3000 \text{ A/cm}^2$  are found in the vicinity of the modules' terminals. With the presented current distribution, a total of 6.26 W and 5.73 W are generated as losses in the positive and negative DC-link busbars respectively, thus no further cooling of these parts is considered.

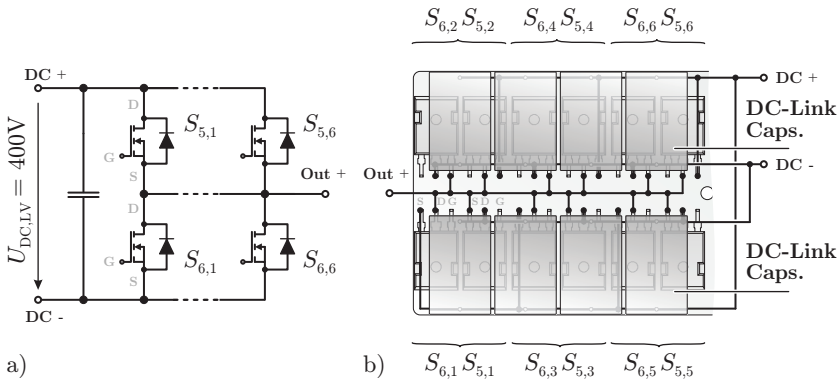
In the TCM-DAB LV side bridge, each switch within the three re-



**Figure 4.17:** HC-DCM-SRC busbar design. These busbars consist of the required interconnection of the positive and negative DC-link voltages to the IGBT modules and DC-link capacitors.



**Figure 4.18:** FEM simulations for estimation of current densities and losses in the power busbars: a) Top view of positive busbar; b) Bottom view of positive busbar; c) Top view of negative busbar; d) Bottom view of negative busbar.

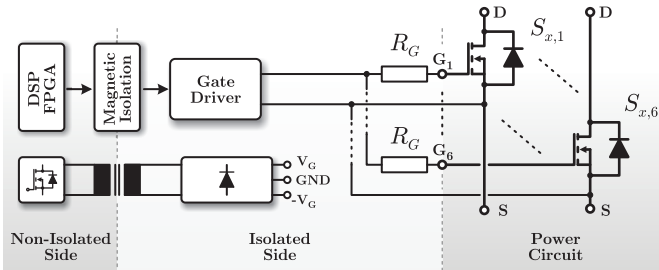


**Figure 4.19:** Arrangement of the MOSFET switches in bridge configuration. In a), one leg of the full-bridge is shown, whereby each switch in this half-bridge consists of six paralleled MOSFET switches. The arrangement on the heat sink is presented in b), whereby low side and high side switches are placed next to each other in order to reduce the effects of parasitic inductances during the switching transients.

quired MOSFET-based full-bridges consists of six parallel connected devices, as represented by one of the bridge legs in Fig. 4.19-a), whereby the mechanical layout of this bridge leg is presented in Fig. 4.19-b). In order to minimize the effects related to parasitic inductances in the commutation path, the arrangement consists of placing the high side and low side devices next to each other. Additionally, in order to further minimize parasitic effects, the DC-link capacitors are placed directly on top of the semiconductors, as can be seen in Fig. 4.19. This power circuit was accommodated on a two layer PCB with 0.1 mm copper thickness. The main advantage of the layout presented in Fig. 4.19-b) is the independence of the DC busbar connections, directly on the bottom of the DC-link capacitors, and the AC side connections, which run through the middle of the assembly utilizing both PCB layers. The result is a maximal utilization of the available copper layers on the PCB.

#### 4.5.5 Gate Driver

Given the similarity in the construction of the HC-DCM-SRC MV and LV side bridges, an identical gate driver circuit was used in for the LV



**Figure 4.20:** Gate driver concept for the TCM-DAB MOSFET bridges. A single gate driver is used to drive the six paralleled devices with independent gate resistors in order to improve the transient current sharing among the paralleled devices.

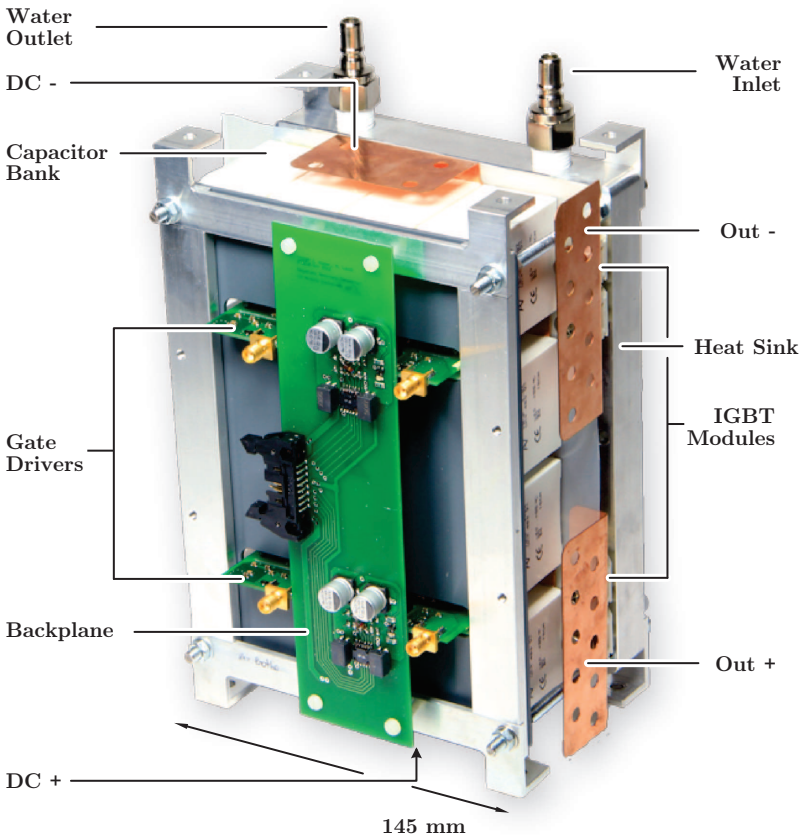
side semiconductors of this converter. In order to utilize the clamping circuit which ensures operation within safe voltage levels, however, minor modifications corresponding to replacement of the transient voltage suppression diodes for lower voltage-rated devices were implemented due to the lower operating voltage.

The block diagram of the TCM-DAB gate driver circuit is presented in Fig. 4.20. The gate signal generated in the DSP is isolated by a coreless magnetic isolator and fed to the gate driver IC. The isolated power supply comprises an H-bridge transformer driver feeding the primary side of a PCB integrated transformer connected on its secondary side to a rectifier circuit which generates the required positive and negative gate voltages.

This gate driver circuit is utilized to control all six paralleled devices which build each switch of the LV side TCM-DAB bridge. The output of the gate driver is connected to independent and identical gate resistors used to driver each of the six MOSFETs, as shown in Fig. 4.20.

#### 4.5.6 Final Assembled LV Side Full-Bridges

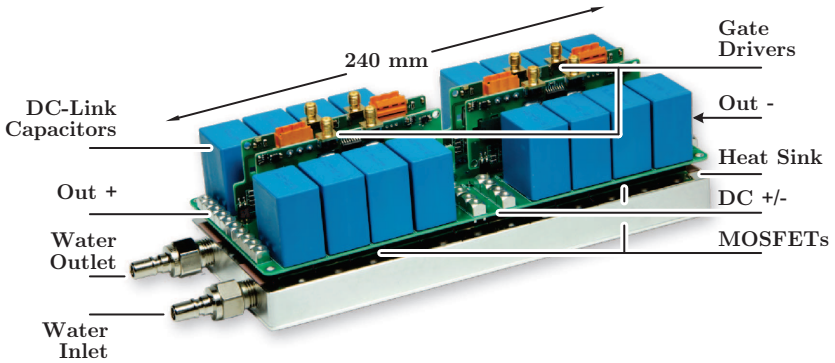
The final assembled HC-DCM-SRC LV side bridge is shown in Fig. 4.21. As can be seen, a compact construction was achieved for this module, reaching a power density of 25 kW/liter. The construction resembles that of the HC-DCM-SRC MV side bridge (cf. Fig. 3.28): top water-cooling inlet and outlet, top/bottom DC-link connections, compact ca-



**Figure 4.21:** Picture of the realized LV side IGBT-based HC-DCM-SRC bridge. Concerning terminals Out+, Out-, DC+ and DC-, refer to Fig. 4.16-a).

capacitor bank, vertically inserted gate drivers and common signal distribution backplane. The main difference is presented by the output AC terminals which are in this case placed on the same side of the module.

The assembled LV side full-bridge of the TCM-DAB converter, featuring a power density of 27 kW/liter, is presented in Fig. 4.22. All 24 semiconductor devices are placed on the customized water-cooled heat sink. The high current PCB performs the interconnections between



**Figure 4.22:** Picture of the realized LV side MOSFET-based TCM-DAB bridge. Concerning terminals Out+, Out-, DC+ and DC-, refer to Fig. 4.19-a).

the different power components, namely the DC-link capacitors, the power semiconductors and the DC and AC terminals. Additionally, the vertically inserted gate driver board can be seen.

# 5

## Medium Frequency Transformer

As mentioned in the introduction, electric transformers, either utilized in electric power systems or in a power electronics-based converter, are fundamental components within modern high-efficient energy supply chains. Two important specifications of these transformers are their VA (power) rating and operating frequency, since combined with the available magnetic core materials and copper conductor technology, they strongly influence the two key features of a transformer: its efficiency and power density.

SSTs constitute a new application area where transformers are utilized in MF range ( $> 1$  kHz) while processing large amounts of power ( $> 100$  kW). From the transformer's perspective, for a given operating frequency, higher power leads to an increased size. However, the combination of higher frequencies and larger dimensions results in strong parasitic effects in the core material, copper conductors and, in some cases, in the cooling system. If not properly accounted for, these effects increase the losses of the transformer, decreasing its efficiency and ultimately compromising its reliability. Moreover, for a given efficiency, higher power density leads to higher loss density, thus efficient transformer cooling concepts become mandatory.

In this chapter, MF transformer technologies will be studied starting from a review of previously reported MF transformer realizations, leading to the concepts adopted in this thesis for the HC-DCM-SRC and the TCM-DAB converter. An optimization procedure which outputs the optimum transformer design for a given set of constant parameters is also proposed, leading to the construction of these two transformer prototypes, whereby their mechanical assembly is extensively covered.

## 5.1 Transformer Types and Review of Previously Reported Designs

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Typically when designing lower power inductive components, a vast variety of core shapes and sizes are available to start the design. When considering higher power components, however, the core sizes and shapes are considerably limited due to the larger required dimensions, specially of the magnetic cores.

A revision of the previously proposed MF transformer concepts shows that they can be summarized in three main types: Coaxial, Shell-Type and Core-Type. These three transformer types are presented in Fig. 5.1 whereby the four main parts, core; primary winding; secondary winding and isolation, in each transformer type are identified.

The main features of these three transformer types together with the previously reported realizations will be discussed in the following.

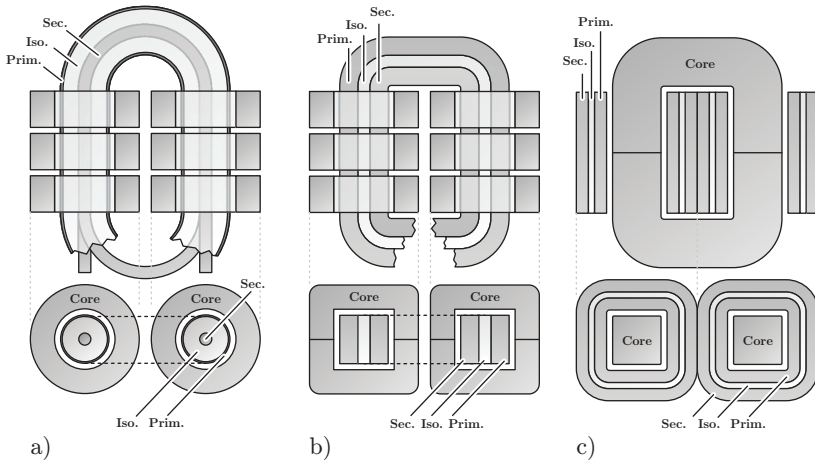
### 5.1.1 Coaxial Winding Transformer

The coaxial transformer type is based on a coaxial cable where the outer and inner conductors are used as the transformer windings, as can be seen in Fig. 5.1-a). Typically ring-shaped magnetic cores are implemented since they possess a favorable geometry for this type of transformer. The main advantage of this type of transformer construction is the reduced and easily analytically calculated value of leakage inductance due to the coaxial concept and the inherently interleaved construction. Moreover, the coaxial concept ensures smooth electric fields within the isolation medium, thus achieving a reliable isolation performance.

The main drawback of this construction is the limitation of the achievable turns ratio given the incapability of independently selecting the number of primary and secondary turns.

This transformer concept for high-power DC-DC conversion was initially reported in [87] for a power rating of 50 kW and an operating frequency of 50 kHz. Later in [88], a detailed analysis of the high frequency effects affecting the copper losses in the coaxial cable was performed on a 120 kW/20 kHz prototype. ABB reported the construction of a high-power MF transformer with a coaxial winding construction first in [12] where a solution for the limitation of the transformer's turns ratio selection was proposed. Later in [89], a detailed description of this





**Figure 5.1:** Transformer topologies typically considered for the design of high-power MF transformers: a) Coaxial winding transformer. Based on coaxial cable whereby the primary and secondary windings are implemented using the inner and outer conductor of the coaxial cable. b) Shell-type transformer consisting of an E-shaped core with concentric primary and secondary windings. c) Core-type transformer consisting of two U-shaped cores with the windings arranged around the core legs.

350 kW/10 kHz transformer prototype construction was presented, comprising loss calculations, mechanical arrangement and isolation testing among others. More recently, in [90] a detailed analytical calculation of the parasitic components up to the megahertz range in a 30 kW/20 kHz prototype was presented.

### 5.1.2 Shell-Type Transformer

The shell-type MF transformer structure is based on an E-shaped magnetic core as presented in Fig. 5.1-b). The primary and secondary windings are concentrically arranged around the middle leg of the transformer core, achieving a compact transformer construction. This standard transformer structure can be very often found in LF distribution transformers [3].

The main advantages of this transformer construction are the relatively large number of available core sizes and copper conductors suitable for the transformer's assembly. Additionally, due to the concentric winding construction, typically low leakage inductances can be achieved, which is specially critical if the transformer is to be used in a resonant-type structure. Moreover, the analytical calculation of this leakage inductance can be easily done due to the regular geometry and hence well-defined magnetic fields inside the transformer's winding window. Furthermore, the primary and secondary windings' turns can be independently chosen as opposed to the coaxial concept, achieving a higher flexibility in the selection of these parameters.

This transformer construction for high-power DC-DC conversion has been reported in several publications. In [91] a compact 50 kW/50 kHz prototype is thoroughly described with special attention on the thermal management of the transformer. Further details of this transformer and the complete DC-DC system are found in [92, 93]. The highest power MF transformer prototype found in literature was presented in [13], where a 500 kW/8 kHz prototype was experimentally tested. This switching frequency was selected in order to avoid acoustic noise emissions in the audible range, as vibrations and magnetostriction, and hence the audible noise, in transformers is generated a twice the operating frequency [94].

The next reported shell-type, high-power transformer prototype was presented in [95] where an oil insulated concept was proposed. Here, also a deep analysis of the transformer's thermal behavior was presented for the 170 kW/4 kHz prototype. A deep analysis and optimization of MF transformers was realized in [96], resulting in an optimal design of a shell-type, natural convection-cooled 25 kW/2 kHz transformer prototype, which is part of the UNIFLEX European project [30]. Given the natural convective cooling selected in this case, this transformer exhibits a relatively low power density. The same authors analyzed in [63] two transformer prototypes, one of them shell-type, for a total power of 400 kW and an operating frequency of 1 kHz. Here, a comprehensive optimization procedure and the resulting two-dimensional performance plots, in shape of Pareto-front were presented. With this rather low switching frequency, however, no high-frequency related issues, such as asymmetric current sharing (which will be covered later in this chapter) are expected.

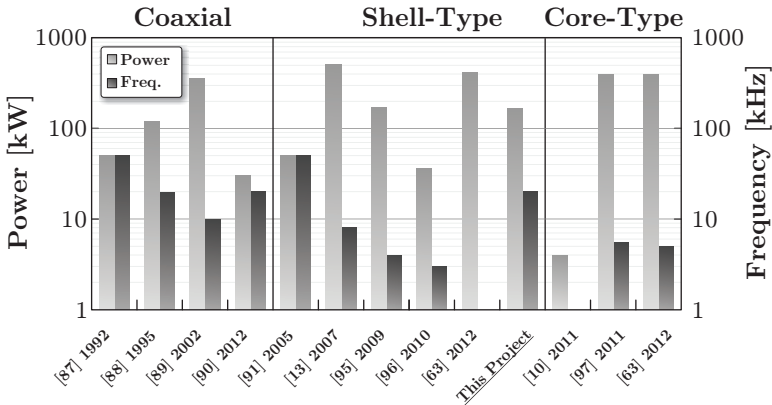
### 5.1.3 Core-Type Transformers

The core type transformer arrangement consists of two U-shaped magnetic cores whereby the windings are typically concentrically arranged around each of the core legs. This transformer arrangement is presented in Fig. 5.1-c) and, as can be seen, represents the analogous construction with respect to the shell-type arrangement. In this case, if the windings are concentrically arranged, the calculation of the leakage inductance can be done as with the shell-type arrangement. In other cases however, if the primary and secondary windings are placed on different legs of the core, the analytical calculation of the leakage inductance, and therefore its minimization, becomes highly complex.

This transformer concept has been reported in literature, whereby in [10], a downscaled prototype of 4 kW and 400 Hz was realized. A high-power prototype was reported in [97], reaching 400 kW and operated at 5.6 kHz. The windings of this transformer prototype are arranged independently on each core leg, i.e. no concentric winding was considered. Additionally, the windings are built with hollow aluminum conductors, whereby the inner channel serves as water pipe for cooling of the windings, enabling considerably high current densities to be reached. The complete arrangement is oil-immersed, thus also a high isolation level is reached. The latest MF transformer comprising the core-type arrangement was reported in [63]. This prototype was designed for 400 kW power level and 5 kHz operating frequency and is based on nanocrystalline core material.

A summary of all aforementioned transformer designs together with their power/frequency levels is presented in Fig. 5.2 and they are also chronologically arranged for each transformer type. As can be seen, the coaxial concept was initially favored due to the capability to accurately control its parasitic components and due to the potential to reach high isolation levels. The constructed prototypes range from 30 to 350 kW with frequencies in the range between 10 and 50 kHz. Later, the shell-type arrangement was favored, becoming the mainly considered concept as can be seen in Fig. 5.2. It is interesting to observe that in this case as well as for the coaxial winding concept, the power level of the designed transformers is decreasing, starting with ambitious frequency goals as high as 50 kHz and settling down in frequencies as low as 4 kHz.

The latest considered arrangement is the core-type construction. The two highest power level prototypes considering this prototype are



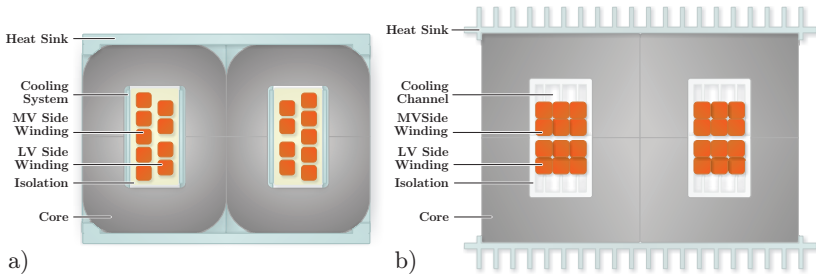
**Figure 5.2:** Summary of constructed transformer prototypes found in literature grouped according to transformer concept and showing the aimed power/frequency levels.

largely similar in terms of power and frequency specifications, as can be seen in Fig. 5.2.

The revision of the previously presented transformer concepts also enables the identification of the different available core materials, conductor types, insulation media and cooling concepts.

The two mainly utilized core materials are amorphous and nanocrystalline, both with high saturation flux densities higher than  $B_{\text{sat}} = 1.2 \text{ T}$ . These core materials have considerably high costs when compared to ferrite, therefore ferrite is also considered in the design of the transformers in this project. The preferred conductor type is the litz wire due to its superior high frequency performance, which typically enables a reduction in losses when compared to foil conductors. When considering isolation, several strategies have been followed. In case of the coaxial windings concepts for example, the isolation is provided by the coaxial cable, which typically is made of PTFE (teflon). Other concepts consider oil isolation due to its comparatively high reliability. Finally, tape isolation as done with electrical machines has also been utilized.

The increase in switching frequency is aimed to reduce the size of the transformer. If the efficiency is kept at the same level, a higher power density results in higher generated losses per unit volume, and hence in



**Figure 5.3:** Cross-sectional views of the designed transformers for the a) HC-DCM-SRC and the b) TCM-DAB converter.

higher heat fluxes through the transformer boundaries. In order to keep the transformer's operating temperatures within safe limits, advanced cooling concepts are often mandatory. In this respect, the three main utilized approaches are passive convective cooling, forced convective cooling and water-cooling. The utilization of different cooling concepts influences the transformer's power density, as will be empirically shown in the next sections where a water-cooled and a forced air-cooled solution are introduced and optimized.

## 5.2 Optimization of the MF Transformer

As seen in the previous section, the shell-type transformer represents the mainly considered concept due to its comparatively compact design and the flexibility in the selection of its components. For this reason, for the high-power DC-DC converter designed in this project, shell-type transformers were considered for both the HC-DCM-SRC and the TCM-DAB. These two transformers however, differ in their selected core material, isolation medium and cooling concept. The cross-sectional views of the considered transformers can be seen in Fig. 5.3.

For the HC-DCM-SRC system, a compact, high-power density design is aimed for. For this reason, nanocrystalline core material and water-cooling are selected. As can be seen from Fig. 5.3-a), in the shell-type structure the LV side winding is placed around the middle leg of the transformer. A layer of isolation based on mica tape is placed between the LV winding and the MV winding. This material can isolate up to 13.8 kV and is originally designed for isolation of medium voltage

electrical machines [98]. In addition to this isolation layer, the windings are initially covered with a semi-conductive tape in order to even out the electric field within the isolation.

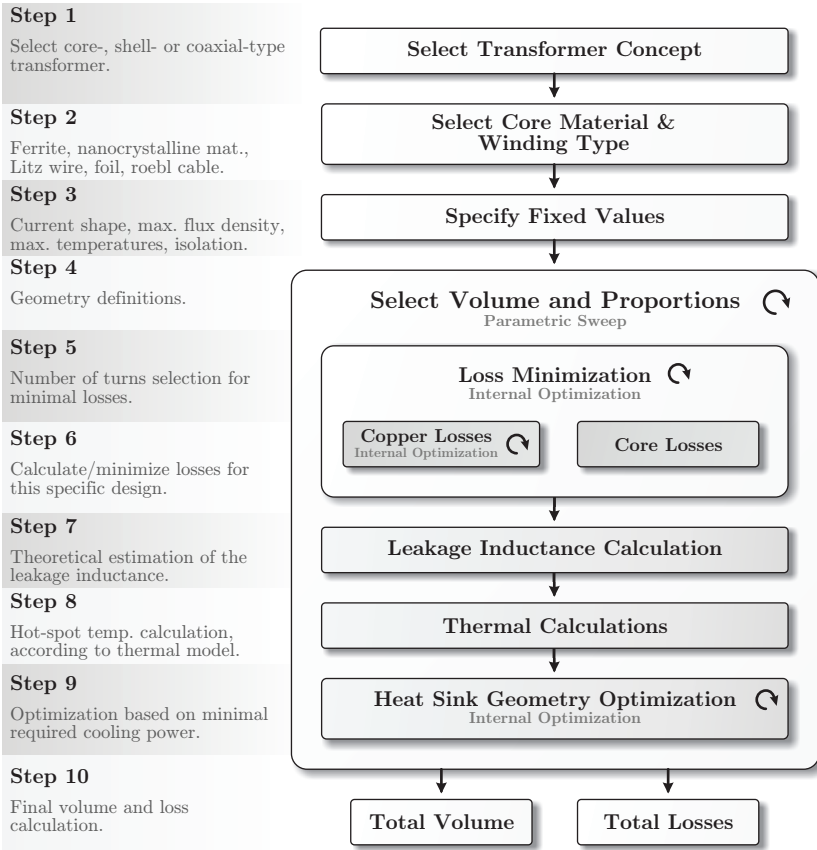
The cooling concept is based on aluminum pieces conducting the heat to top/bottom water-cooled heat sinks, similar to the concept utilized in [91]. Further details about the cooling concept will be shown in the next section together with the complete mechanical construction of the nanocrystalline transformer whereby the specific selection of winding turns, core size and others will result from an optimization process.

In case of the TCM-DAB transformer, a ferrite-based construction was preferred in order to achieve a comparatively lower cost solution. The isolation concept is based on a PTFE (teflon) bobbin where the windings are placed. The cooling concept is forced air-cooling for both the winding and the cores, as seen in Fig. 5.3-b). Here, the air channel adjacent to the MV and LV windings is displayed, achieving the heat removal from these windings. The top and bottom heat sinks are utilized in order to cool the ferrite cores. Further details about the selected cooling system and its performance will be shown in the next section. As with the nanocrystalline transformer, the precise number of turns and core dimensions and other transformer parameters will be given as a result of the optimization process described in the following.

## 5.2.1 Optimization Procedure

The implemented optimization procedure is presented in Fig. 5.4. The first step in the transformer design process is the selection of the transformer type, where, as stated earlier, the commonly utilized concepts are presented in Fig. 5.1. The following step is the selection of the employed materials and followed by step 3 where the electrical/magnetic/thermal properties, e.g. the current shape and RMS values, the core's saturation flux density and the maximum operating temperatures, among others, are defined.

In step 4, the parametric sweep of the transformer geometry, defined by proportions between its main dimensions and the total allowed boxed volume  $V_{\text{box}}$  which completely encloses the transformer, is performed. These proportions, related to the dimensions presented in Fig. 5.5, are defined as follows:

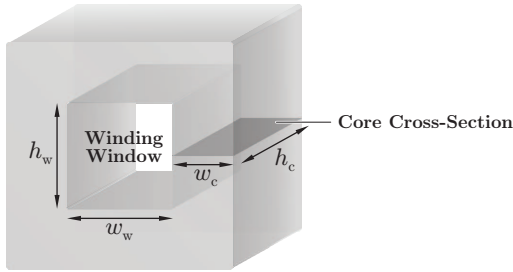


**Figure 5.4:** Optimization procedure's flowchart presenting the steps considered to find the optimized MF transformer design.

$$p_c = \frac{h_c}{w_c} \quad (5.1)$$

$$p_w = \frac{h_w}{w_w} \quad (5.2)$$

$$p_{wc} = \frac{h_w w_w}{h_c w_c}. \quad (5.3)$$



**Figure 5.5:** Definition of basic core dimensions based on the core window size and core cross-section.

Moreover, the boxed volume  $V_{\text{box}}$  can be defined for the shell-type transformer based on the dimensions displayed in Fig. 5.5

$$V_{\text{box}} = 2 \cdot (2w_c + w_w) \cdot (2 \cdot w_w + h_c) \cdot (2 \cdot w_c + h_w) \quad (5.4)$$

assuming that the ends of the windings at the front and back of the transformer extend the transformer length for  $w_w$  on each side.

The expressions in (5.1) through (5.4) are enough to completely define the transformer dimensions. The three proportions  $p_c$ ,  $p_w$  and  $p_{wc}$  are utilized as free parameters in the transformer design together with the enclosing box volume  $V_{\text{box}}$  of the transformer. Further proportions related to the design of the cooling system will be defined once the thermal model is derived.

With the geometry of the transformer defined, the number of turns that minimizes the total transformer losses is searched for by sweeping discrete values of  $N_{LV}$  in the range  $1 \rightarrow 10$  (with  $N_{MV} = N_{LV} \cdot n$ ). Within this step, a minimization of the copper losses is performed based on the analytical expression presented in [99] whereby the core losses are calculated based on the approach presented in [100] for non-sinusoidal flux density waveforms and the Steinmetz parameters provided by the core manufacturer. In case of the copper losses, the litz wire parameters, namely its number of strands  $n_s$  and the strand diameter  $d_s$  are internally optimized for minimum losses within the manufacturing possibilities of the litz wire provider.

The following step in the optimization process consists of the estimation of the transformer's leakage inductance. This estimation is based on the calculation of the magnetic energy stored between the





following.

The litz wire has an internal thermal resistance  $R_{Cu1}$  and is also responsible for the generation of the losses calculated in step 6. It should be noted that the thermal resistance of the litz wire in the radial direction, as is the case for  $R_{Cu1}$ , is considerably higher than the copper thermal resistance [102], given by the construction of the litz wire which is based on multiple strands isolated from each other with a low thermally-conductive isolation layer. Additionally, the copper's thermal resistance is treated as a distributed loss generator with total generated losses of  $P_{cu,N}$ , which results in the temperature rise being half of an equivalent thermal resistance with no heat generation and with total conducted power of  $P_{cu,N}$  [103]. The next resistances along the copper-generated heat flux are the isolation resistance  $R_{I1}$ , the cooling plate's thermal resistance  $R_{P1}$  and the C-shaped pieces' thermal resistance  $R_{C3}$ . This series connection of resistances is lumped into a single total resistance  $R_{T1}$ . The analogous thermal analysis can be done for the total resistance  $R_{T2}$  on the LV side winding. In this case, slight modifications in thermal resistances are found due to the difference in the winding arrangement and in the total generated losses in the LV winding.

From a thermal point of view, the transformer possess two symmetry axes as shown in Fig. 5.6-a). This allows to reduce the thermal model of the C-shaped pieces to two resistances defined by the different cross-sections found in each part of the heat path. The goal of these C-shaped pieces is to carry the copper's and core's heat to the top and bottom water-cooled heat sinks.

For the derivation of the core's thermal network, consider the scheme presented in Fig. 5.6-b). Analogously as with the thermal resistance of the litz wire, the nanocrystalline core's thermal resistance  $R_{K,N}$  is responsible for the conduction of the distributed losses  $P_{K,N}$  in the core to the cooled surfaces. These losses are conducted into node  $M_1$  and  $M_2$  for the outer and inner cores respectively. From there, the equal path through resistances  $R_{C1}$  and  $R_{C2}$  into the heat sink is followed.

All the aforementioned thermal resistances are calculated based on the materials' respective thermal conductivities, presented in Table 5.1, the transformer proportions and the following cooling system proportions (cf. Fig. 5.6-b):

**Table 5.1:** Thermal conductivities utilized in the thermal model of the MF transformers.

Material	Thermal Conductivity
Nanocrystalline (parallel to tape)	8.35 Wm/K
Ferrite	4 Wm/K
Litz wire (radial direction)	0.8 Wm/K
Mica tape	0.2 Wm/K
Aluminum	237 Wm/K

$$p_C = \frac{h_1}{h_c} \quad (5.5)$$

$$p_{wi} = \frac{h_2}{w_w/2}. \quad (5.6)$$

With this description of the thermal network and the respective thermal resistances defined, the copper and core's hotspot temperature found as

$$T_{M1} = (P_{K,N} + P_{Cu1,N}) \cdot (R_{C1} + R_{C2} + R_{HW}) + T_W \quad (5.7)$$

$$T_{K,N} = \frac{R_{K,N}}{2} \cdot P_{K,N} + T_{M1} \quad (5.8)$$

$$T_{Cu1,N} = \left( \frac{R_{Cu1,N}}{2} + R_{I1} + R_{P1} + R_{C3} \right) \cdot P_{Cu1,N} + T_{M1}, \quad (5.9)$$

whereby  $T_{M1}$  corresponds to the temperature in node  $M_1$ ,  $T_{K,N}$  corresponds to the core's hotspot temperature,  $T_{Cu1,N}$  is the litz wire's hotspot temperature and  $T_W$  is the water temperature.

From here, the heat is conducted away by the cooling fluid, whereby the maximum thermal resistance of heat sink to the water  $R_{HW}$  is calculated in order not to exceed the maximum temperatures in the litz wire and core material as specified in step 3 of the optimization process. This thermal resistance is calculated following the approach presented in [103] for internal fluid flows.

The thermal model for the ferrite air-cooled transformer is derived from Fig. 5.6-c). Here, the thermal paths for the core and litz wires can be independently analyzed considering that no thermal coupling is

found between these two parts given the low thermal conductivity of the utilized isolation bobbin. For this same reason, the top and bottom halves of the transformer can be independently analyzed. For the litz wire, a simple thermal network consisting on the litz wire's thermal resistance  $R_{Cu,F}$  and its thermal resistance to air,  $R_{CuA}$ , are utilized. It should be noted that, as with the nanocrystalline transformer, the resistance  $R_{Cu,F}$  is treated with half its value given the distributed loss generation [103].

In case of the ferrite core, the core's leg thermal resistance  $R_{K1,F}$  is utilized whereby for the limb, a resistance  $R_{K2,F}$  is considered. The heat is conducted through these thermal resistances into the top air-cooled heat sink.

With this description, the following set of equations describes the litz wire's and the core's hotspot temperatures:

$$T_{Cu,F} = P_{Cu,F} \left( \frac{R_{Cu,F}}{2} + R_{CuA} \right) + T_A \quad (5.10)$$

$$T_{K1,F} = P_{K1,F} \cdot \frac{R_{K1,F}}{2} + R_{HA} \cdot (P_{K2,F} + P_{K1,F}) + T_A, \quad (5.11)$$

whereby  $T_{Cu,F}$  is the litz wire's hotspot temperature,  $T_{K1,F}$  is the core's hotspot temperature and  $T_A$  is the ambient air temperature.

All the required thermal resistances are calculated based on the material's thermal properties (cf. Table 5.1) and defined proportions and volumes, whereby the following air-cooling system proportions are defined:

$$p_{ch} = \frac{h_3}{h_w/2} \quad (5.12)$$

$$p_{hs} = \frac{h_4}{2 \cdot w_c + h_c}. \quad (5.13)$$

As a final result of this step in the optimization process, the required minimum heat sink to water thermal resistance  $R_{HW}$ , litz wire to air thermal resistance  $R_{CuA}$ , and air-cooled heat sink to air thermal resistance  $R_{HA}$  which all together ensure safe operating temperatures in the nanocrystalline and ferrite transformer concepts are given as outputs for the next optimization step which minimizes the cooling system power.

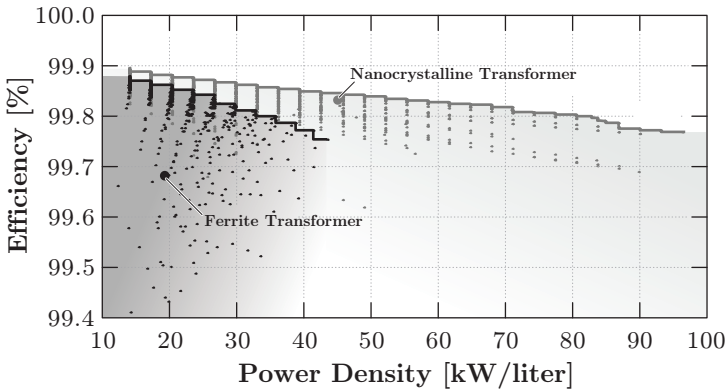
**Table 5.2:** Parameter sweep utilized in the optimization procedure presented in Fig. 5.4.

Parameter	Nanocrystalline	Ferrite
Boxed volume $V_{\text{box}}$	1 $\rightarrow$ 12 liter	1 $\rightarrow$ 12 liter
Core cross-section proportion $p_c$	1.875 $\rightarrow$ 7.5	2 $\rightarrow$ 3.4
Core window area proportion $p_w$	1 $\rightarrow$ 4	1 $\rightarrow$ 1.8
Area ratio $p_{wc}$	0 $\rightarrow$ 1	0 $\rightarrow$ 1
C-piece size $p_C$	0.1 $\rightarrow$ 0.15	–
Winding cooler size $p_{wi}$	0.1 $\rightarrow$ 0.15	–
Air channel ratio $p_{ch}$	–	0.1 $\rightarrow$ 0.3
Air heat sink ratio $p_{hs}$	–	0.1 $\rightarrow$ 0.3
Maximum litz wire temperature	130 °C	130 °C
Maximum core temperature	130 °C	130 °C
Water/air temperature	20 °C	40 °C

The last step in the transformer’s design process consists of the optimization of the water-cooled heat sink and forced air-cooled heat sink in case of the nanocrystalline and ferrite transformers respectively. Here, the required cooling system thermal resistances  $R_{CuA}$  and  $R_{HA}$  are synthesised. Two degrees of freedom are available in the design of these heat sinks: the pump/fan power and the heat sink geometry. Following the approach presented in [104], these heat sinks can be designed to achieve the desired thermal resistances while minimizing the required pump/fan power. This power is later added to the total losses of the system in order to obtain the final value of efficiency achieved with the specific design.

The aforementioned optimization process was executed with the values of proportions and volumes shown in Table. 5.2, where also the maximum allowed temperatures which are part of the fixed values given in step 3 are presented.

The resulting efficiency-power density Pareto-fronts for both designed transformers are shown in Fig. 5.7. The nanocrystalline concept performs always better than the air-cooled version, but at low power densities the difference in efficiency decreases. Considering the cost of the nanocrystalline cores and the higher effort for a water-cooling system, the air-cooled system might be the better choice for high efficiency applications. The highest power density of each Pareto-front (about 97 kW/liter for the nanocrystalline transformer and about 43 kW/liter

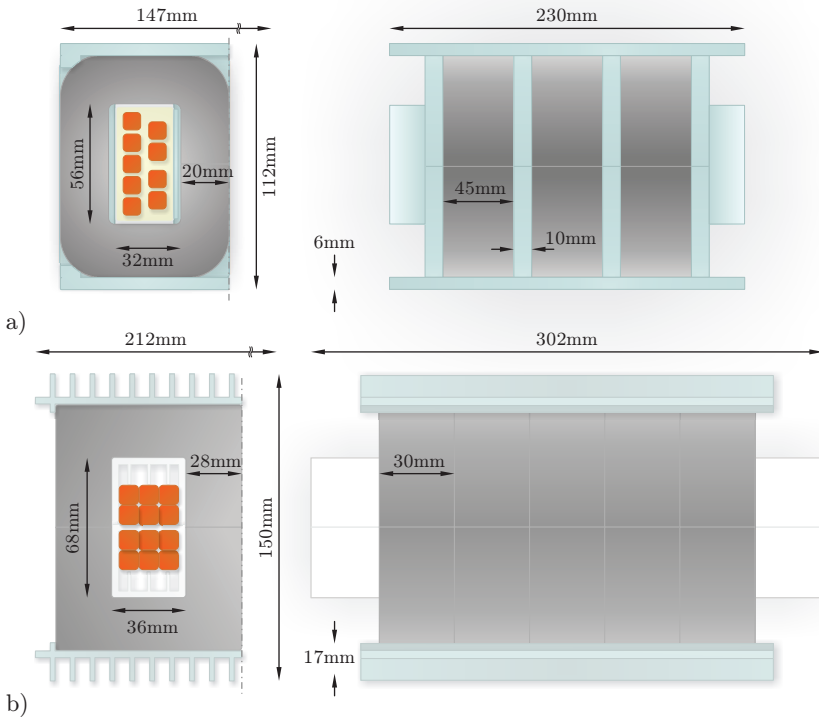


**Figure 5.7:** Resulting Pareto-fronts for the designed nanocrystalline and ferrite transformers.

for the ferrite transformer), i.e. the design which exhibits the lowest volume is achieved at the thermal limit, imposed by the ambient temperature and the maximum hotspot temperatures. It is shown that power densities beyond 43 kW/liter are only achievable using the water-cooled concept.

The theoretical values of efficiency and power density obtained with the aforementioned optimization procedure for both designed prototypes are also highlighted in Fig. 5.7. In the case of the air-cooled concept, the limited availability of core geometries and litz wires results in the shown sub-optimal design. On the other hand, nanocrystalline cores are typically tailored for a specific application and therefore it is possible to construct a core with the optimal dimensions resulting from the optimization procedure, thus the real design is close to the Pareto-optimum, as can be seen in Fig. 5.7.

Another reason for the sub-optimal constructed prototypes is the practical issues related to their mechanical construction. In order to visualize these limitations, several details about the mechanical assembly and experimental testing of the prototypes will be presented in the following.



**Figure 5.8:** Optimized transformers' final dimensions: a) Nanocrystalline transformer design built with Vitroperm 500F core material; b) Ferrite transformer constructed with N87 core material.

## 5.2.2 Optimized Transformers' Parameters

The dimensions of the final optimized transformer designs are shown in Figs. 5.8-a) and b) for the nanocrystalline and ferrite transformers respectively. The nanocrystalline transformer design comprises six pairs of U-cores with Vitroperm 500F nanocrystalline core material and the respective four C-shaped cooling pieces (cf. Fig. 5.8). These U-cores were tailored by the core manufacturer (Vacuumschmelze) in order to meet the specific design requirements.

Both MV and LV windings are built with a litz wire composed of 9500 strands with a thickness of  $71\ \mu\text{m}$  each. In the MV winding, one litz wire with a total of five turns is utilized while for the LV winding, two paralleled litz wires each with two turns are utilized. Each of these LV windings is driven by a dedicated full-bridge, as described in Chapter 4.

The ferrite transformer is built with the U96/76/30 N87 ferrite cores from EPCOS. A total of 10 core pairs are utilized to build the required E-shaped core. The MV and LV windings are constructed with the same litz wire as the nanocrystalline transformer. In this case, the MV winding is constructed with 6 turns while the LV winding comprises 3 parallel litz wires with two turns each, achieving the desired  $n = 1 : 3$  turns ratio.

## 5.3 MF Transformers' Assembly Details

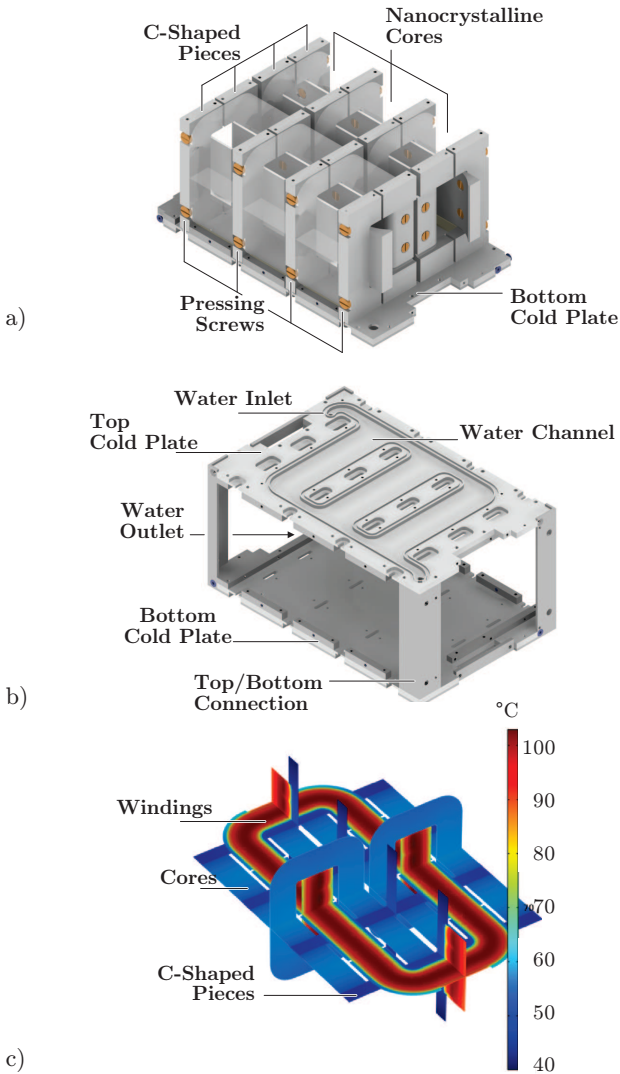
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The optimization procedure presented in the previous section led to two 166 kW/20 kHz designs where the main differences are the employed core material and the cooling concept. These different strategies lead to considerable differences in the performance of the two designed systems. Moreover, the mechanical construction of both transformers also possess considerable differences, which will be detailed in this section. Additionally, the thermal model verification and further details about the mechanical arrangement of the designed prototypes will be also presented together with the final views of the designed MF transformers.

### 5.3.1 Nanocrystalline Transformer Prototype

A detailed 3D CAD drawing of the nanocrystalline transformer's cooling system is shown in Fig. 5.9-a). Here it can be seen that the transformer consists of six pairs of U-cores arranged in E-shape. The heat-extracting C-shaped pieces are placed in between these cores and also at the two extremes in order to equally cool all transformer cores. These C-shaped pieces are pressed against the winding by screws on the side of the assembly, as depicted in Fig. 5.9-a). The heat from these C-shaped pieces is conducted into the top/bottom heat sinks, which can be seen in Fig. 5.9-b). Here the designed water channel which ensures an efficient cooling of the aluminum plate is presented. These top and bottom heat sinks are connected through a dedicated aluminum piece. This





**Figure 5.9:** Nanocrystalline transformer's cooling system details: a) C-shaped cooling pieces for core and winding heat extraction; b) Top/bottom water-cooled heat sinks; c) COMSOL thermal simulation.

way the inlet and outlet water connections are on the same side of the transformer.

### Thermal Model Verification

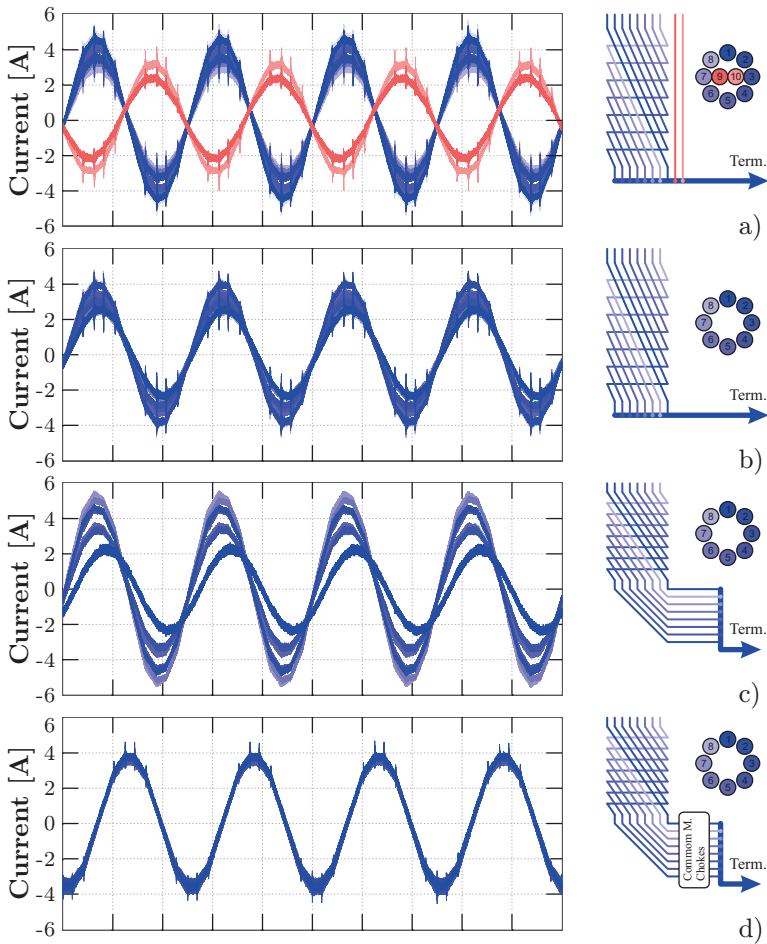
A thermal simulation with the presented transformer cooling system was conducted in COMSOL multiphysics with the results shown in Fig. 5.9-c). As can be seen the hotspot temperature is always found in the winding, as expected due to the high thermal resistance of the required isolation layer. This hotspot temperature, however, is lower than the accepted maximum winding temperature of 130 °C, validating the proposed transformer's thermal design.

### Copper Losses Verification

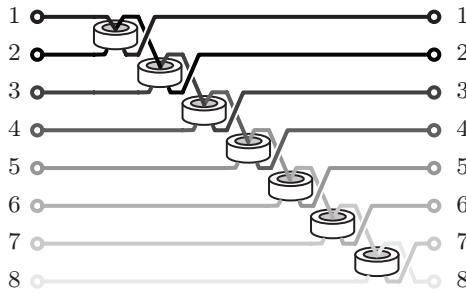
The utilized litz wire is based on 10 sub-bundles with 950 strands each. The first test performed on the nanocrystalline transformer consist of measuring the current in each of these bundles in order to quantify the impact of the transformer's size on the current distribution in the bundles. In all cases the current was fed from the MV side with a short circuited LV side winding, i.e. only the stray inductance of the transformer limits the conducted current. Also the aluminum cooling system was removed in this case. On the MV side a current of 25 A RMS is fed and the current in each litz wire bundle is measured with a Rogowski coil while the total losses in the winding are measured with the Yokogawa WT3000 precision power analyzer. The resulting current sharing for different termination strategies is presented in Fig. 5.10.

For the first test, a termination of the litz wire which ensures same length of all bundles was adopted (cf. Fig. 5.10-a). The litz wire was delivered by the manufacturer with two middle non-interchanged bundles (in red) surrounded by 8 bundles with interchanged positions (in blue) as shown in Fig. 5.10-a). The measured currents can also be seen in Fig. 5.10-a) together with the schematic view of the litz wire and its respective termination arrangement. As can be seen, the non-interchanged litz wire bundles in the middle result in negative circulating currents, increasing the losses in the complete litz wire whereby the AC to DC resistance ratio, representing the impact of high frequency effects on the litz wire, is  $R_{AC}/R_{DC} = 3.01$ .

As a second test, the middle non-interchanged conductors were removed while keeping the remaining 8 bundles. The current sharing



**Figure 5.10:** Analysis of the current sharing in litz wire bundles; a) With middle non-interchanged bundles and symmetric termination; b) Without middle non-interchanged bundles and symmetric termination; c) Without middle non-interchanged bundles and unsymmetrical termination; d) Without middle non-interchanged bundles, unsymmetrical termination and equalizing common-mode chokes (cf. Fig. 5.11).



**Figure 5.11:** Arrangement of common-mode chokes to equalize the currents in the litz wire bundles.

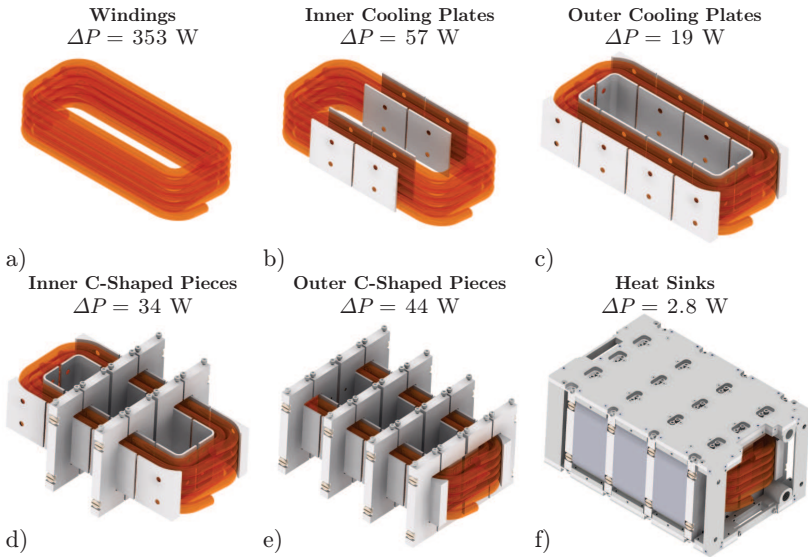
in this case is considerably improved as can be seen in Fig. 5.10-b) whereby the AC to DC resistance ratio is reduced to  $R_{AC}/R_{DC} = 1.95$ , proving the importance of a symmetrically built litz wire at this frequency/dimensions range.

For practical reasons, the connection of the litz wires to the power electronic switches is realized by spreading the litz wire bundles into copper plates which are later connected to the power semiconductors. The impact of the asymmetry introduced by this connection is shown in Fig. 5.10-c). No significant difference is found in the AC to DC resistance ratio with respect to the symmetric termination. In this case, this ratio has a value of  $R_{AC}/R_{DC} = 1.98$ .

In order to force a symmetric behavior of the currents in the bundles, the arrangement of common-mode chokes (Vitroperm 500F ring cores from Vacuumschalze) as shown in Fig. 5.11 are placed on the litz wire bundles, resulting in a symmetrization of the currents in the bundles as seen in Fig. 5.10-d). In spite this symmetric current distribution the AC to DC resistance ratio is still  $R_{AC}/R_{DC} = 1.94$ , i.e. no considerable improvement in losses was achieved<sup>1</sup>.

The cooling system utilized in this transformer is potentially subject to high magnetic fields and therefore to induced currents. These induced current could cause losses in the aluminum cooling plates used

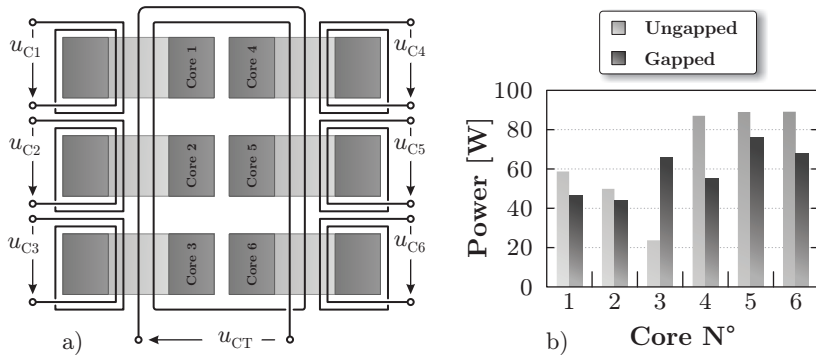
<sup>1</sup>The losses in the common-mode chokes were calculated based on the measured magnetic flux density obtained through the measurement of the induced voltage in one auxiliary turn placed around a common-mode choke. The resulting core losses are about 5 mW per core and are therefore neglected in the total losses of the litz wire.



**Figure 5.12:** Step-by-step assembly of the nanocrystalline transformer's cooling system and its respective measured losses: a) MV and LV side windings; b) Inner winding cooling plates; c) Outer winding cooling plates; d) Attachment of the inner C-shaped pieces; e) Attachment of the outer C-shaped pieces; f) Complete assembly comprising top/bottom heat sinks.

for the heat extraction (cf. Figs. 5.6-a) and b)). In order to quantify the losses in each part of the cooling system, the increase in losses  $\Delta P$ , starting with the bare winding, was measured utilizing a high precision power analyzer (Yokogawa WT3000) and an external 25 A RMS / 20 kHz current source. Even though this current is considerably lower than the nominal transformer current, the linearity of the system is utilized in order to estimate the losses at nominal transferred power. This way, the incremental increase of the losses was measured and therefore the contribution of each of the cooling system's parts to the total losses could be identified. The different parts of the aluminum cooling system can be seen in Fig. 5.12 whereby the loss share of each part is:

- Winding, Fig. 5.12-a) (no cooling system): 353 W



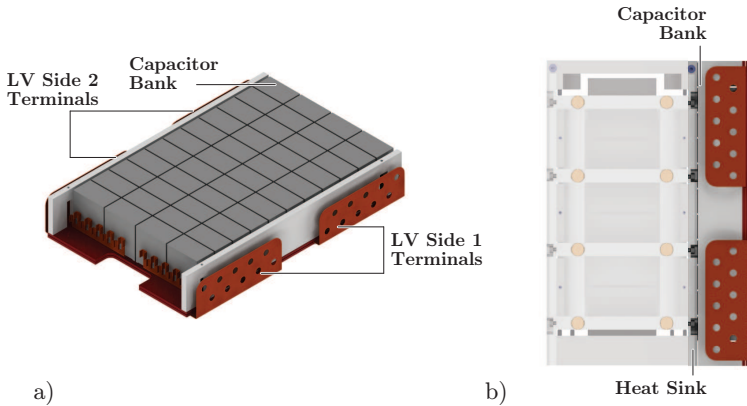
**Figure 5.13:** Arrangement of the nanocrystalline cores in order to independently measure the voltages induced in test windings placed around the 6 cores. In b) the measured losses for gapped and ungapped arrangement are presented.

- ▶ Inner cooling plates, Fig. 5.12-b): 56.97 W
- ▶ Outer cooling plates, Fig. 5.12-c): 18.82 W
- ▶ Inner heat conducting plates, Fig. 5.12-d): 34.28 W
- ▶ Outer heat conducting plates, Fig. 5.12-e): 44.30 W
- ▶ Top/bottom water-cooled heat sinks, Fig. 5.12-f): 2.83 W.

As can be seen, a large share of losses, in total 157 W, is generated in the C-shaped aluminum pieces. These losses were not accounted for during the optimization of the transformer, since no high magnetic fields were expected in these regions. This phenomena and its accurate modelling should be matter for future research on MF transformers.

### Core Losses Verification

The core losses were measured in the complete nanocrystalline transformer as well as in the individual cores by magnetizing the transformer from the LV winding with open MV winding. A test winding was placed around each of the cores as shown in Fig. 5.13-a) in order to independently measure the core losses in each of the stacked cores. The initial measurement was performed with ungapped cores, i.e. top and bottom U-cores pressed together without gap spacing. The results of this



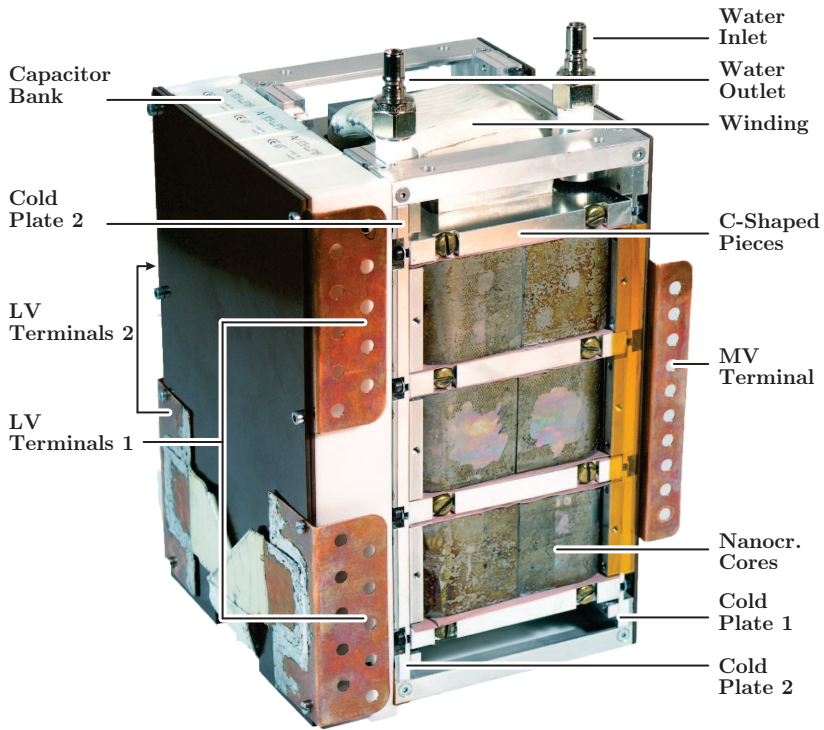
**Figure 5.14:** Nanocrystalline transformer (for the HC-DCM-SRC) resonant capacitor arrangement: a) Capacitor bank and respective terminals; b) Attachment to the water-cooled heat sink in order to ensure safe operating temperatures.

test are presented in Fig. 5.13-b). The total core losses are considerably higher than the calculated ones. This phenomenon has been reported previously for tape-wound cut-cores [105, 106], as the ones utilized in this transformer prototype. The reason for this increase in losses is mainly due to the flux lines around the air gap which orthogonally cross the tape layers generating eddy currents and therefore higher losses. During the testing process, a high sensitivity of the core losses to the alignment of the core pairs was detected, causing increases in up to 30 % of core losses with a minimum core misalignment.

Additionally, the undefined air-gap results in uneven flux densities in the different cores due to the different reluctances in the magnetic path, which can be observed in Fig. 5.13-b) due to the uneven generated losses in the different cores. In order to account for this problem, a 0.1 mm air-gap was introduced in between the core pairs. This way, the total core losses were reduced by 12 % while improving the loss distribution, and therefore the thermal behavior, of the cores as shown in Fig. 5.13-b).

### Resonant Capacitor Integration

The final step of the nanocrystalline transformer construction is the design of the resonant capacitor bank. The leakage inductance measured



**Figure 5.15:** Final mechanical assembly of the nanocrystalline transformer utilized in the HC-DCM-SRC DC-DC converter prototype.

from the LV side reaches  $0.4 \mu\text{H}$  whereby a resonant frequency  $f_r$  close to  $20 \text{ kHz}$  is desired. Utilizing the expression (2.6) of Chapter 2, the required capacitor value

$$C_r = \frac{1}{(2\pi f_r)^2 L_s} = 158.31 \mu\text{F} \quad (5.14)$$

is found.

This capacitor value was realized with 44 paralleled KEMET C4A-TGBW 4330 A3EJ  $450 \text{ V}/3 \mu\text{F}$  capacitors, reaching a total capacitance of  $132 \mu\text{F}$ .

It should be noted that this resonant capacitor must be able to



deal with the total transformer RMS current at 20 kHz. With this capacitance value, the achieved resonance frequency is  $f_r = 21.9$  kHz, ensuring sub-resonant operation of the HC-DCM-SRC.

The mechanical arrangement of the capacitor bank is presented in Fig. 5.14-a). In order to realize a compact transformer design, this capacitor bank possess equal length and width as the transformer's heat sinks. This way, the top face of the capacitors can be attached to the cover of one water-cooled heat sink, as shown in Fig. 5.14-b), thus effectively extracting heat from the resonant capacitor bank and ensuring its operation within safe temperature values.

### Final Mechanical Assembly

The final assembled nanocrystalline transformer is presented in Fig. 5.15. As can be seen, the magnetic cores are placed in between the C-shaped cooling pieces utilized to extract the heat from the cores and winding as explained earlier. These C-shaped pieces conduct the heat to top/bottom water-cooled heat sinks, whereby the water inlet and outlet is conveniently positioned at the top of the assembly. The power terminations for the MV side are placed on one of the transformer's faces, whereas for the LV side, these terminals are placed on top of the capacitor bank.

Finally, adding the copper, core and cooling system losses measured previously, this 166 kW/20 kHz nanocrystalline, water-cooled transformer achieves a 99.4% efficiency at rated power with a power density of 32.7 kW/liter.

### 5.3.2 Ferrite Transformer Prototype

The designed ferrite transformer is based on 10 pairs of U-cores with N87 core material arranged in E-structure. The cooling concept in this case is forced air-convection with the thermal model proposed in Fig. 5.6-c). In order to force the air stream through the winding and the top/bottom heat sinks, an air channel was constructed with the two selected 120 mm fans attached to the front, as presented in Fig. 5.16-a). This air-channel is built with a bottom aluminum plate and a PVC isolated top cover, utilized to mount the power electronics bridges shown in Chapters 3 and 4 for the TCM-DAB converter.

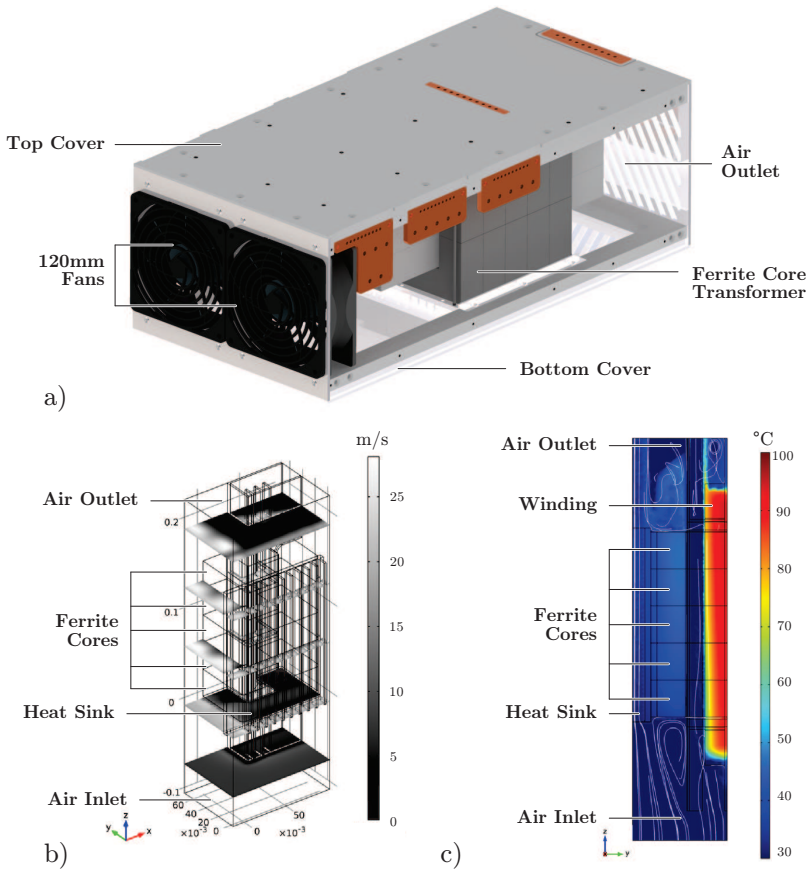
#### Thermal Model Verification

The ferrite transformer's air channel was simulated in order to study its aerodynamic behavior. It should be noted from Fig. 5.6-c) that the transformer has a one quarter symmetry and therefore only this piece was considered in the simulation, as presented in Fig. 5.16-b). The goal of this study is to obtain the impedance of the system in order to accurately find the operating point of the frontal fans, and therefore the value of volumetric air flow required for the thermal simulation.

With the fan's operating point defined, the corresponding thermal simulation comprising heat conduction in solids and heat conduction in fluids was conducted with the results shown in Fig. 5.16-c). As can be seen, the windings' litz wire presents the highest operating temperature, which in any case stays below the allowed 130 °C maximum.

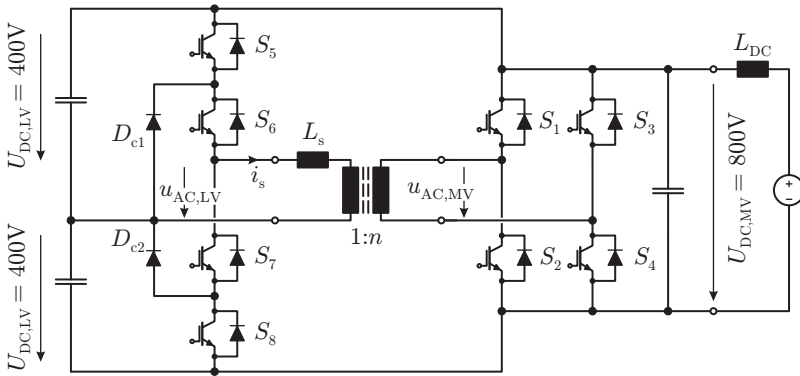
#### Transformer's Continuous Thermal Test

In order to thermally test the transformer before the complete converter is assembled, a back-to-back test bench with power recirculation was constructed. The schematic representation of this test bench is shown in Fig. 5.17. The circuit is based on a full-bridge structure based on 1.7 kV IGBTs on the MV side and an NPC half-bridge-based structure comprising 600 V IGBTs on the LV side. Both bridges are powered by a single 800 V power supply only supplying the losses of the system. It should be noted that from the MV side the voltage applied on the transformer terminals is  $\pm 800$  V instead of the nominal  $\pm 1000$  V as with the original converter. This reduced applied voltage is translated into a reduction of the total transferred power, which in this setup reaches a

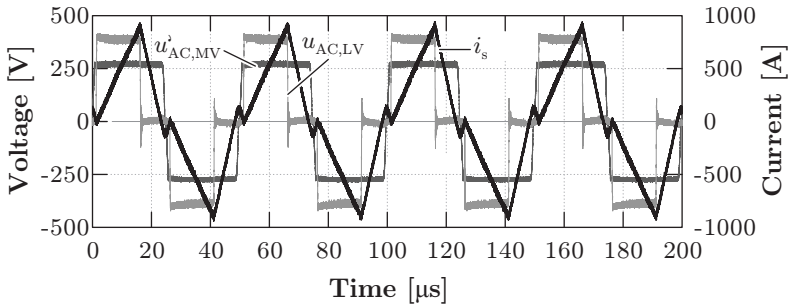


**Figure 5.16:** Ferrite transformer's cooling system details: a) Air channel enclosure comprising two frontal 120 mm fans in order to extract the core and litz wire losses according to the thermal design shown in Fig. 5.6-c); b) Aerodynamic simulation performed in order to analyze the performance of the selected 120 mm fans; c) Aerodynamic simulation coupled with thermal simulation showing the validity of the proposed thermal model.

maximum of 130 kW while still keeping ZCS transitions. This power is further reduced if QZSC transitions are implemented in order to achieve



**Figure 5.17:** Back-to-back testbench utilized to test the thermal behavior of the ferrite transformer.

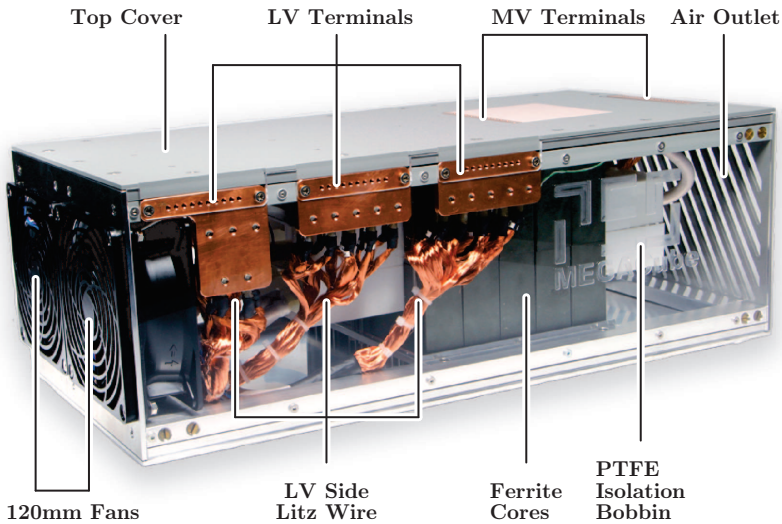


**Figure 5.18:** Experimental testing of the ferrite transformer under nominal current conditions and 100 kW transferred power.

soft switching in all utilized semiconductors.

The power electronic bridges in this case were based on IGBT modules and their construction is analogous to the MV and LV side bridges presented for the HC-DCM-SRC converter in Chapters 3 and 4 respectively.

The continuous operation of the test bench presented in Fig. 5.17 was up to 100 kW of circulating power with nominal RMS current through the winding. The result of this test is shown in Fig. 5.18 where the voltages and the current in the transformer are shown with

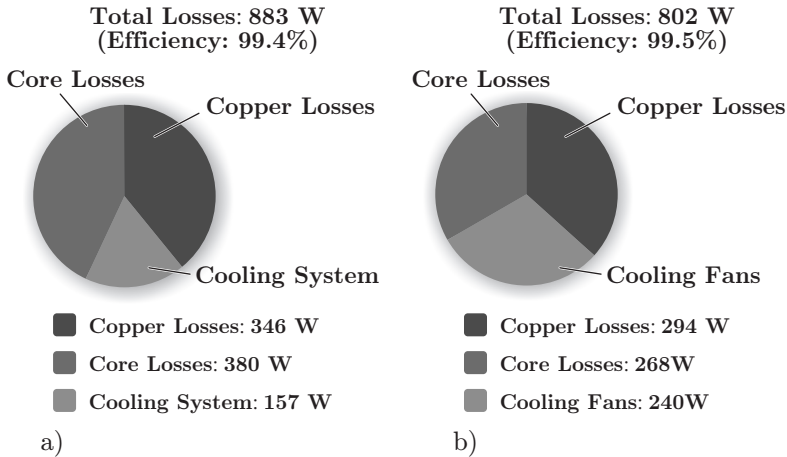


**Figure 5.19:** Final assembly of the ferrite transformer within the designed air channel.

the MV side voltage reflected to the LV side. This test was conducted while measuring the transformer's litz wire and core's temperature until thermal steady state was reached after about 45 min of uninterrupted operation. The core's maximum temperature measured at the center of its middle leg reached  $72^{\circ}\text{C}$  while the litz wire's surface temperature reached  $61^{\circ}\text{C}$ . Even though a measurement of the litz wire's hotspot is not practically achievable, the aforementioned maximum temperature value is assumed to be within the specified limits, therefore validating the proposed thermal model and the further conducted thermal simulations.

### Final Mechanical Arrangement

The ferrite transformer's final mechanical assembly is presented in Fig. 5.19. Here, in addition to the air channel described earlier, the litz wire terminations arranged at the sides of the transformer are also displayed. It should be noted that the LV winding is based on three parallel litz wires independently driven by the MOSFET-based bridges presented in Chapter 4 and therefore three identical LV terminations



**Figure 5.20:** Summary of transformer losses for a) nanocrystalline transformer and b) ferrite transformer. Both transformers are designed for 166 kW rated power and for 20 kHz operating frequency.

were constructed. On the MV side, the terminations are placed on the surface of the top cover and are realized by copper plates running through this cover. The complete assembly is cooled by the two frontal 120 mm fans shown in Fig. 5.19.

The ferrite 166 kW/20 kHz air-cooled transformer reaches an efficiency of 99.5% at rated power and a power density of 8.21 kW/liter.

### 5.3.3 Transformer Losses Breakdown

The summarized values for measured losses in each of the constructed transformers are shown in Fig. 5.20. In case of the nanocrystalline transformer assembly, the additional losses in the cooling system, which were not accounted for during the optimization process, reduce the expected efficiency of the transformer. In case of the ferrite transformer, an important share of the losses is attributed to the operating power in the cooling fans, which was accounted for during the optimization process.

In any case, both designed transformers reach very high efficiencies whereby their thermal behavior was tested either by simulations

in case of the nanocrystalline transformer concept or by a dedicated experimental test bench in case of the ferrite transformer.





# 6

## Flux Balancing

The converter bridges described in Chapter 2 and designed in Chapters 3 and 4 are built with arrangements of semiconductor switches. In these bridges, phenomena such as unmatched turn-on/turn-off times, semiconductor forward voltage drops, gate driving signal delays, insufficient PWM resolution or pulsating load, among others, can cause differences in the positive and negative volts-seconds applied to the transformer [107]. This results in a DC voltage component at the transformer terminals, which causes an undesired DC magnetic flux density component in the transformer core. If not properly accounted for, this DC bias can cause malfunctioning of the MF transformer since the transformer core will be operated in unsymmetrical magnetization condition, increasing the transformer losses or in worst case saturating the transformer core.

In order to avoid operation of the transformer with biased magnetic flux density, several methods have been proposed, all of which will be analyzed and classified in this chapter. Additionally, a novel concept for the measurement and active compensation of the DC flux bias in the transformer core is presented and extensively analyzed.

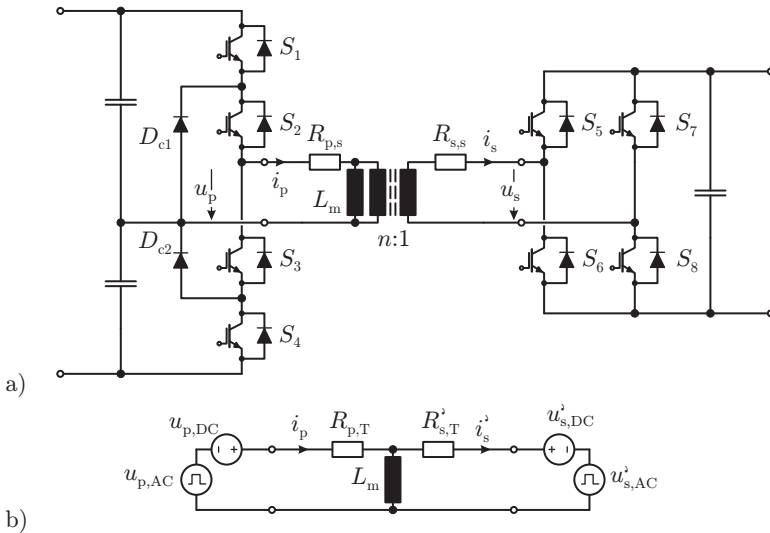
### 6.1 DC Magnetization Basics

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In order to show the relation between a DC voltage at the transformer terminals and the generated magnetic flux density DC component, consider the circuit presented in Fig. 6.1-a), where the TCM-DAB topology is shown. The primary and secondary side bridges<sup>1</sup> apply voltages  $u_p$

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<sup>1</sup>Primary and secondary correspond to the MV and LV side respectively. However, the terms primary and secondary are utilized throughout this chapter in order



**Figure 6.1:** a) DC-DC converter comprising a primary side NPC half-bridge and a secondary side full-bridge; b) Equivalent model of the converter with independent DC and AC voltage sources and reflected secondary side.

and  $u_s$  to the transformer respectively. The DC and the AC components of these voltages can be separated into independent voltage sources, building the circuit depicted in Fig. 6.1-b), where the secondary side has been reflected to the primary side. Here, the resistances  $R_{p,T}$  and  $R'_{s,T}$  represent the winding resistances  $R_{p,s}$  and  $R'_{s,s}$  plus the semiconductors' equivalent on-state resistances of the primary and secondary side switches.

In steady state, the DC part of the magnetizing current  $I_{m,DC}$  of the transformer is given by

$$I_{m,DC} = I_{p,DC} - I'_{s,DC} = \frac{U_{p,DC}}{R_{p,T}} + \frac{U'_{s,DC}}{R'_{s,T}}. \quad (6.1)$$

The DC magnetic flux density is then determined by the characteristics of the winding and core through

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to generalize the analysis.

$$B_{\text{DC}} = \frac{I_{\text{m,DC}} \cdot N_{\text{p}}}{l_{\text{m}}} \cdot \mu_0 \bar{\mu}_{\text{r}} = \left( \frac{U_{\text{p,DC}}}{R_{\text{p,T}}} + \frac{U'_{\text{s,DC}}}{R'_{\text{s,T}}} \right) \cdot \frac{N_{\text{p}}}{l_{\text{m}}} \cdot \mu_0 \bar{\mu}_{\text{r}}, \quad (6.2)$$

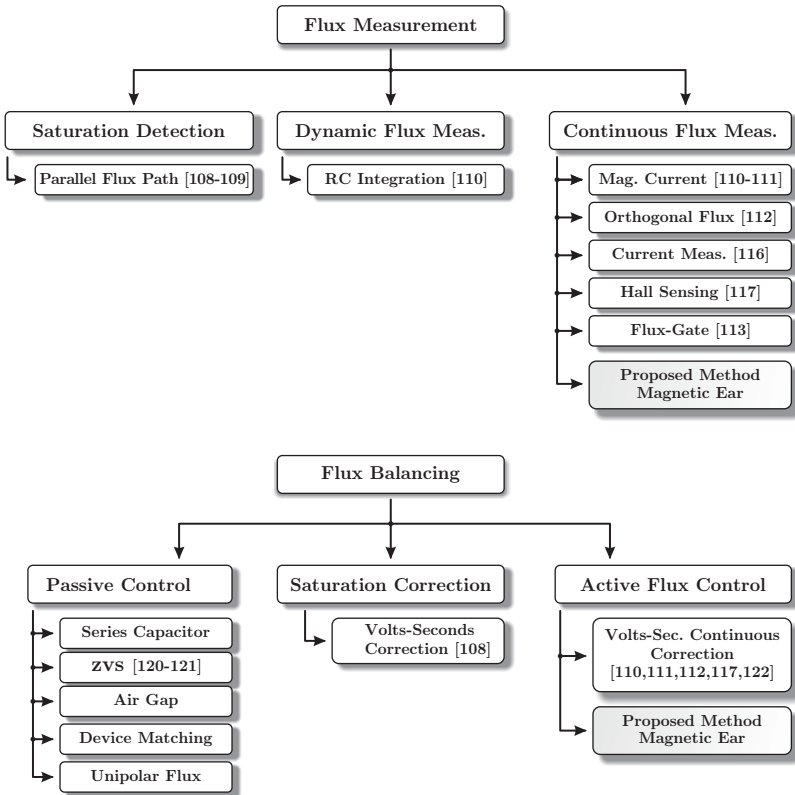
where  $l_{\text{m}}$  is the length of the magnetic path,  $N_{\text{p}}$  is the number of turns in the primary side,  $\mu_0$  is the permeability of air and  $\bar{\mu}_{\text{r}}$  is the core's relative permeability on the linear region of the B-H curve.

From (6.2) it can be seen that the DC magnetic flux density is limited by the equivalent series resistances,  $R_{\text{p,T}}$  and  $R'_{\text{s,T}}$ , of the circuit, which are typically kept as low as possible in order to decrease the converter's conduction losses. This means that a small DC component in the voltage applied to the transformer generates a large DC flux density component.

For example, taking the ferrite transformer presented in Chapter 5 (cf. Fig. 5.19) and the LV side bridge shown in Fig. 4.22, the primary side equivalent resistance  $R_{\text{p,T}}$  reaches 1.7 m $\Omega$ . This design considers a ferrite N87 core material which is characterized by a relative permeability  $\bar{\mu}_{\text{r}}$  around 1950. In this design, a 0.0125% of relative difference in the duration of the positive and negative semi-cycles of the primary voltage  $u_{\text{s}}$ , i.e. a switching time error of 2.5 ns, would suffice to create a DC flux density component of  $B_{\text{DC}} = 50$  mT (assuming no air gap in the magnetic path).

With this DC flux density component, the core can be easily driven outside the linear region of the B-H curve, generating a non-linear magnetizing current with high peak values. This results in increased conduction and switching losses, causing a reduction in efficiency and higher semiconductor and transformer operating temperatures, compromising the converter's reliability. Moreover, a DC biased flux density waveform results in higher core losses [100], further compromising the converter's efficiency. For these reasons, the operation of the transformer under balanced condition, i.e. with zero DC flux density component, must be ensured. It is also worth to note that if a balanced operation of the flux density in the core is ensured, the transformer can be designed with low flux density over-dimensioning, meaning that its magnetic core cross-section, and therefore its volume, can be reduced, increasing the converter's power density.

In the next section, previously proposed measures to avoid a flux density biased operation and/or to ensure operation of the transformer under safe flux density values will be covered, leading to the flux destiny

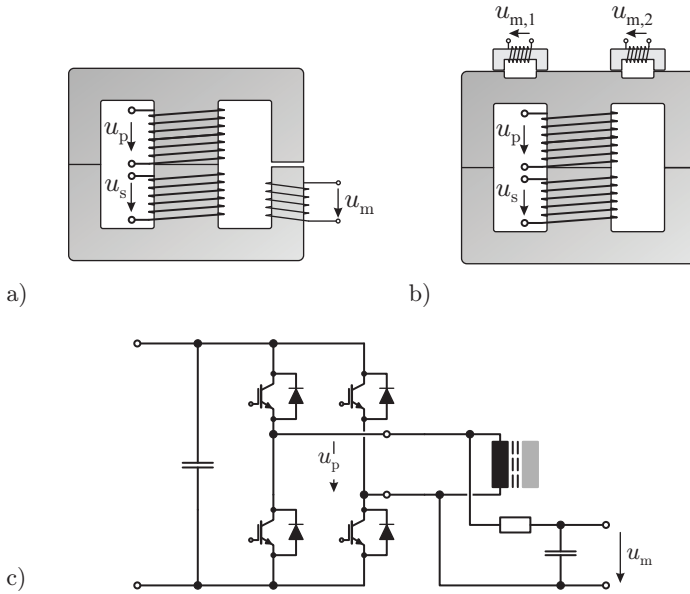


**Figure 6.2:** Classification of previously proposed flux balancing concepts. The two main areas are Flux Measurement and Flux Balancing. The proposed measurement concept, the "Magnetic Ear", is highlighted within this classification.

transducer proposed in this chapter.

## 6.2 Classification of Flux Measurement/Control Methods

In order to ensure balanced flux operation, the main problems that must be addressed are: measurement of the core's internal flux status



**Figure 6.3:** Previously proposed concepts for magnetic saturation prevention: a) Parallel magnetic path in an E-core with a gapped leg [108]; b) Parallel magnetic path with external cores and reduced cross-section [109] of the main core; c) Integration of the voltage applied to the transformer with an RC network [110].

and balancing or closed-loop control of the flux. Within these two topics, other sub-categorizations are possible, as displayed in Fig. 6.2 and discussed in the following sections.

### 6.2.1 Flux Measurement / Saturation Detection

The methods for recognition of the core's flux state can be classified into: Saturation Detection, Dynamic Flux Measurement and Continuous Flux Behavior Measurement. The measurement method proposed in this chapter belongs to this last class.

### Saturation Detection

In [108], an E-core was used with an air-gap in one of the external legs (Fig. 6.3-a)). During normal operation, the flux flows only in the un-gapped leg but as soon as this leg saturates, a part of the magnetic flux is forced through the gapped leg and therefore a voltage is induced in an additional winding, indicating the saturation of the main flux path. Alternatively, in [109] a slot is placed in one of the core legs, as shown in Fig. 6.3-b) in order to reduce the cross-sectional area in this place. An additional magnetic path with a winding is provided in parallel to the slotted part of the core. As the slotted section has a smaller cross-section, it saturates at lower flux densities with respect to the rest of the core and therefore the magnetic flux is forced into the parallel magnetic path. This induces a voltage in a winding indicating the impending core saturation.

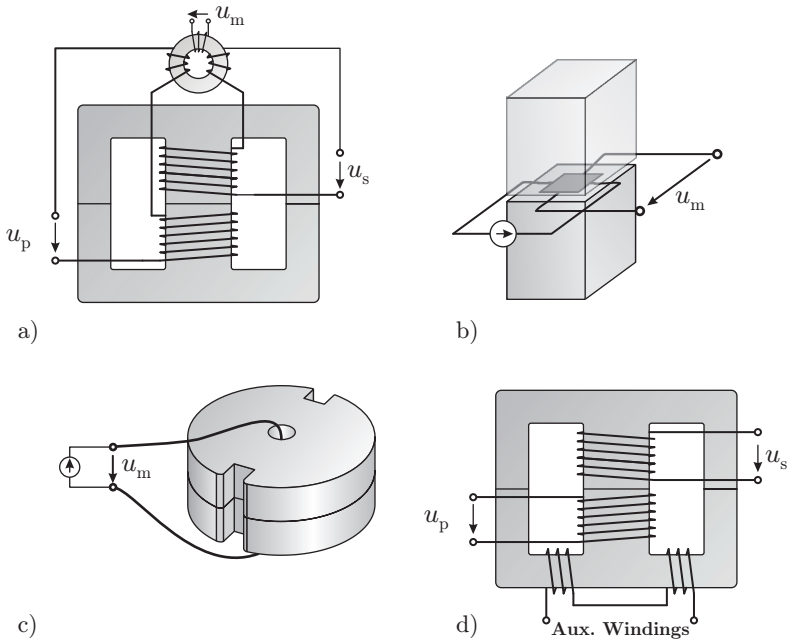
With both these methods, only the saturation of the core is detected, which may be enough in some applications. In applications which require high efficiency, however, this is not sufficient since the flux density in the core can still be biased without being saturated and therefore the core losses are increased. Moreover, in order to implement both these methods, modifications of the magnetic components are required, increasing its costs and complexity.

### Dynamic Flux Measurement

This method was proposed in [110] in order to detect flux unbalance due to variations in the converter's loading conditions. The principle is to perform an integration of the applied voltage through an RC network or an active integrator (cf. Fig. 6.3-c)). This integrated signal is proportional to the core's magnetic flux. It should be noted that if an active integration is utilized in order to increase the gain of the sensor, the known issues from offsets in active integration could potentially reduce the accuracy of the sensor.

### Continuous Flux Behavior Measurement

The sensing of the flux behavior with large bandwidth and independent of the operating conditions has been covered by several publications, where the following main categories can be identified:



**Figure 6.4:** Continuous measurement of the core's internal flux density: a) Construction of the magnetizing current with an external transformer [111]; b) Magnetic flux measurement with a Hall sensor in the magnetic path; c) Measurement based on orthogonal magnetic fluxes [112]; d) Flux-gate principle applied to flux density monitoring [113].

**Magnetizing Current Measurement** The magnetizing current  $i_m$  indicates the status of flux density in the core. The measurement of this current through subtraction of the scaled primary and secondary side currents was proposed in [110].

In [111] and later in [114], a measurement of the magnetizing current was performed by building an additional transformer with the same turns ratio as the main transformer but with one of the windings in the inverted orientation (cf. Fig. 6.4-a). As the primary and secondary side currents flow through this additional transformer or through a Hall current sensor, most of the magnetic flux caused by the individual currents is cancelled out and the remaining flux, which is proportional to the

magnetizing current, is measured with an additional winding and/or a Hall element (DC current sensor).

The disadvantage of this method is the requirement of isolation on the additional transformer, which needs to be at least the same as the one of the main core. Also, practical issues may arise in higher power transformers where the wiring of primary and secondary sides has an increased complexity, as can be seen for the MF transformer designs presented in Chapter 5.

***Orthogonal Magnetic Flux*** In [112] the internal flux of the core was measured by using an additional coil fed by a DC current which generates a magnetic flux orthogonal to the main flux (cf. Fig. 6.4-c)). The orthogonality of the magnetic fluxes ensures that no voltage is induced in the additional coil by the main flux. As the main magnetic flux density is changed, the B-H characteristic of the material is also changing. This material property change is translated into a variation of the flux in the orthogonal coil, inducing a voltage in its terminals. This principle was also proposed for microfabricated inductors [115] in order to intentionally shape the B-H loop of the magnetic material. In this concept, modified or specially shaped cores are required in order to insert the orthogonal winding, increasing its cost and complexity. Moreover, if the B-H loop has a large linear region, a voltage would be induced in the orthogonal coil only when the core is saturated.

***Converter Current Measurement and Processing*** The direct measurement of the primary and/or the secondary side currents has also been used to balance the flux in the core. As an example, a DC magnetization of the core generates primary/secondary currents with even numbered Fourier components. The amplitude of these components can be measured and used as feedback signal in order to balance the transformer flux, as was performed in [116].

In converters with modulations which do not operate always at 50% duty cycle, the magnetizing current is present during the freewheeling periods. The magnetizing current thus can be measured during these intervals obtaining information about the status of the core's flux density.

***Flux Observer*** In order to overcome the limitation of only dynamic flux measurement, the method described in Section 6.2.1 can be com-



plemented with a measurement of the transformer current [110]. This way, an observer that reconstructs the flux density would be feasible.

**Hall Sensing** The most direct way to measure the flux in the transformer core is to insert a thin Hall sensor in the magnetic flux path [117] (cf. Fig. 6.4-b). However, this requires the insertion of an air gap in the magnetic core, reducing the magnetizing inductance and increasing the reactive power which needs to be provided to the transformer. Moreover, the fabrication of the Hall sensor presents considerable challenges, as known from current probe manufacturing.

**Flux-Gate** The flux-gate principle is a well-known concept for current measurement [118]. This measurement principle can be adapted in order to build a flux density transducer, as presented in [113] and shown in Fig. 6.4-d). In this concept, an E-type core is utilized whereby the primary and secondary windings are placed around the core's middle leg while an additional winding is placed on each of the "I" parts of the core, as depicted in Fig. 6.4-d). With this arrangement, a DC-bias in the flux density would result in a change of the inductance measured between the terminals of the auxiliary winding, thus enabling monitoring of the flux density in the core.

The main disadvantage of this concept is the requirement of full isolation between the auxiliary windings and the primary and secondary windings. Additionally, the auxiliary windings must be placed in the core window, therefore reducing the respective filling factor.

## 6.2.2 Flux Balancing / Feedback Control

The internal core flux can be passively or actively balanced. Depending on whether the measuring principle detects core saturation or performs a complete flux measurement, the active flux balancing principles can be subdivided into saturation correction or continuous flux control.

### Passive Balancing

Passive balancing refers to any balancing principle which does not actively modify the switching signals of the semiconductor devices in order to keep the transformer flux within safe margins. The following passive flux balancing principles can be pointed out:

***Series Capacitor*** One of the most utilized flux balancing principles, due to its simplicity, is the inclusion of a capacitor in series to the transformer winding. The main disadvantages of this approach are (i) increased converter volume, (ii) increased converter losses and (iii) slow dynamic response. This idea was further developed in [119] where a resistor was placed in parallel to the capacitor in order to improve the circuit's LF behavior.

***Soft-Switching (ZVS)*** Ensuring ZVS of all converter semiconductor devices partially compensates for mismatches in the volts-seconds applied to the transformer, as presented in [120, 121]. Here, the modification of the current shape due to the biased operation results in an inherent modification of the voltage waveform during the switching intervals, therefore positively affecting the volts-seconds applied to the transformer which partially compensates for the biased operation.

***Air-gap in the Magnetic Path*** When an air-gap is introduced in the core, the total magnetic path permeability is effectively decreased. This in turn increases the tolerable DC magnetization but doesn't eliminate the DC flux component as achieved with a series capacitor, thus this is not strictly a flux balancing method. Moreover, the inclusion of an air-gap in the core decreases the value of the magnetizing inductance  $L_m$ , increasing the switched and conducted currents.

In addition to the previously presented passive flux balancing principles, the prevention of core saturation can be included into the converter design process. In [107] the different converter electrical parameters that influence the core saturation were clearly pointed out and used to give design considerations which help to prevent saturation.

### **Active Saturation Correction**

The flux measuring concepts presented in Section 6.2.1 can be used to implement a feedback control loop which only operates under impending core saturation, as was done in [108].

### **Active Feedback Control of the Flux**

If a signal proportional to the internal core flux density is available, the DC magnetization of the core can be actively controlled by modifying

the volts-seconds applied to the transformer. The main feedback flux control principles that have been proposed are detailed in [110–112, 117, 122], whereby the sensing principle analyzed in this thesis together with its respective balancing feedback loop are presented in the next section.

## 6.3 The Magnetic Ear

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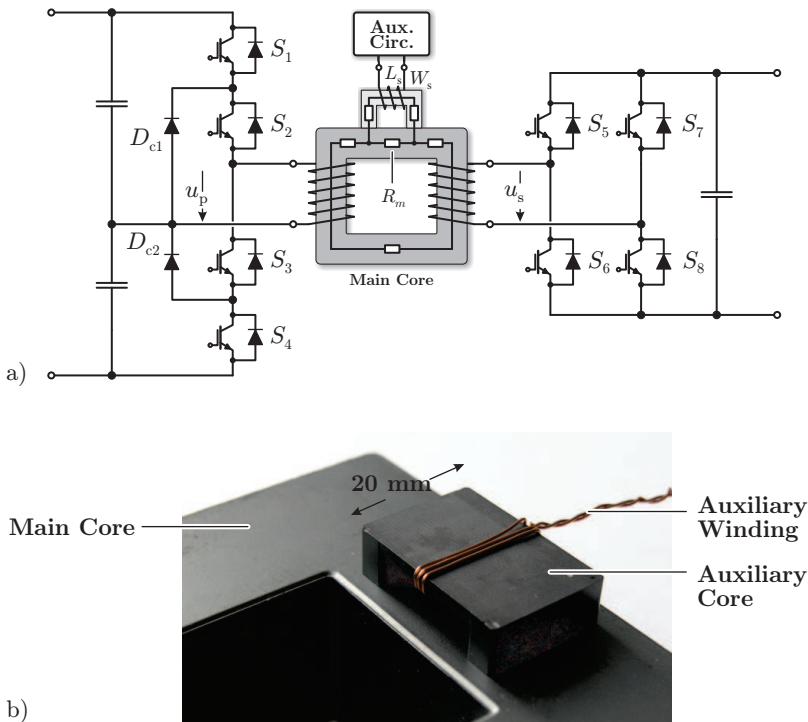
The main requirements for a flux density transducer for the high-power DC-DC converter designed in this thesis can be summarized as follows:

- ▶ **Continuous monitoring:** Since the MF transformer is a critical component of high-power DC-DC converters, it is desirable to continuously monitor the magnetization state of the transformer core.
- ▶ **Isolation:** The measurement concept needs to be specified for the same isolation level as the main transformer.
- ▶ **Non-invasive:** Due to the high complexity and cost of MF transformer technologies, it is highly desirable to realize the design of this component independent from its magnetic flux density measurement concept, i.e. a flux measurement principle which does not interfere with the MF transformer design is required.

Accordingly, a novel magnetic flux density transducer, the Magnetic Ear, which complies with these requirements is proposed and extensively studied in the following.

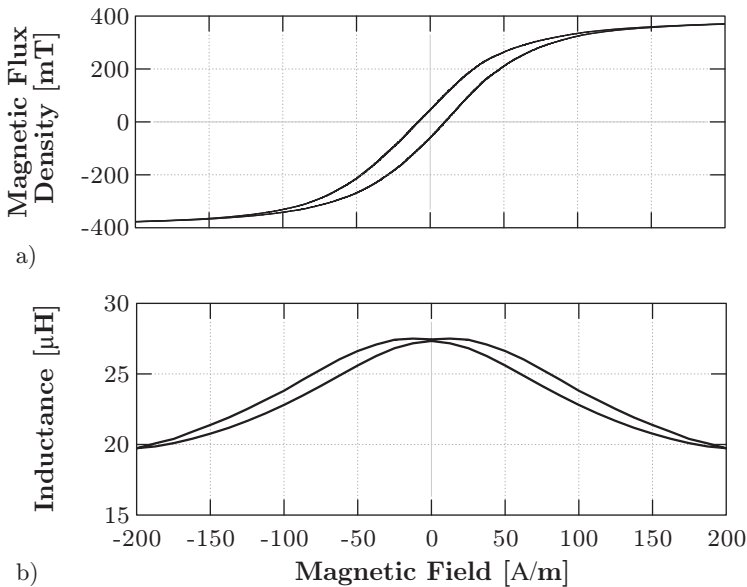
The Magnetic Ear's main concept consists of a shared magnetic path between the main core (the actual transformer core) and an auxiliary core represented by the reluctance  $R_m$  in Fig. 6.5-a). This shared reluctance  $R_m$  changes its magnetic properties, namely its relative permeability  $\mu_{r,m}$  as the main core is driven through its B-H loop. This variation results in a change in the inductance  $L_s$  measured between the terminals of the auxiliary core's winding  $W_s$ . This variation in inductance is sensed by an auxiliary drive circuit which extracts the inductance value of the auxiliary core, delivering a signal directly related to the instantaneous magnetization state of the core. The main and auxiliary cores used to test this concept are presented in Fig. 6.5-b).

The B-H loop of the ferrite transformer is presented in Fig. 6.6-a) while the measurement of the inductance for the auxiliary core arrange-



**Figure 6.5:** The Magnetic Ear main concept: a) Equivalent circuit representation with main core and auxiliary core sharing part of the magnetic path; b) Real implementation of the main core (EPCOS UU93/76/30 N87) and auxiliary core (EPCOS EQ30/8 N87 with removed middle leg) and  $N_{\text{aux}} = 3$  auxiliary winding turns.

ment shown in Fig. 6.5-b) is presented in Fig. 6.6-b) whereby the auxiliary core is built with an EPCOS EQ30/8 N87 core. As can be seen, the inductance of the auxiliary core is considerably sensitive to the instantaneous magnetization state of the main core, thus the instantaneous value of the auxiliary core's inductance can be used as measure of the magnetization state of the main core. It should be noted that the behavior of the auxiliary core's inductance is depending on the shape of the main core's B-H loop, whereby higher sensitivities are reached if the permeability of the main core continuously changes along the B-H loop.

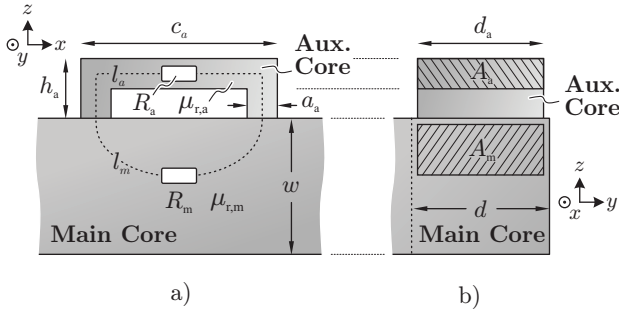


**Figure 6.6:** a) B-H loop of the transformer core shown in Fig 5.19; b) Measured inductance between the auxiliary core's terminals as the main core is driven through its B-H loop.

In case the core material is highly linear until saturation is reached, as given e.g. for gapped cores, this sensitivity is deteriorated and only a change in the inductance can be perceived once the core is driven into saturation. The details and trade-offs in the transducer's design, which is ultimately used to control the flux in the main core, will be discussed in the following.

## 6.4 Design, Drive Circuits and Sampling Methods

As mentioned earlier, the Magnetic Ear transducer consists of an auxiliary core with an auxiliary winding and the respective drive circuit used to measure the inductance between the auxiliary winding terminals and to convert it to an analog signal. Moreover, in order to implement the feedback loop which performs the flux balancing in the main trans-



**Figure 6.7:** Magnetic flux density transducer, the Magnetic Ear, geometric definitions.

former core, the sampling strategy of the aforementioned signal needs to be studied. As a start, the selection of the appropriate auxiliary core geometry (dimensions) and core material is addressed.

### 6.4.1 Auxiliary Core Design

The selection of the auxiliary core's shape and magnetic properties, namely its relative permeability  $\mu_{r,a}$ , will directly affect the sensitivity of the auxiliary inductance  $L_{aux}$  to changes of the main core's permeability  $\mu_{r,m}$ , i.e. changes of the magnetization state of the main core.

In order to analyze the impact of the auxiliary core's geometry and its magnetic properties on the measurement sensitivity, consider the arrangement presented in Fig. 6.7-a), where a C-core is used as auxiliary core. In order to achieve a high sensitivity to changes of the main core's permeability  $\mu_{r,m}$ , the total reluctance of the auxiliary core's magnetic path must be mainly defined by the shared reluctance  $R_m$  and not by the auxiliary core's reluctance  $R_a$ , i.e.  $R_m \gg R_a$ . These reluctances are defined by

$$R_a = \frac{l_a}{\mu_0 \mu_{r,a} A_a}, \quad (6.3)$$

$$R_m = \frac{l_m}{\mu_0 \mu_{r,m} A_m}, \quad (6.4)$$

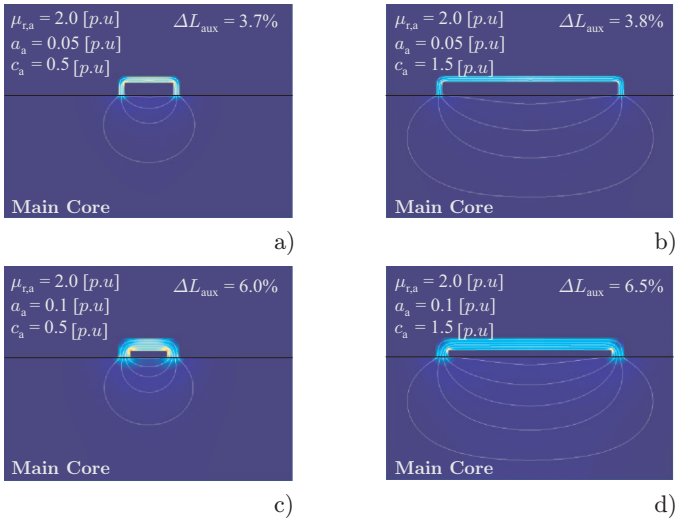
where  $l_a$ ,  $\mu_{r,a}$  and  $A_a$  are the magnetic path length, relative permeability and cross-section of the auxiliary core;  $l_m$ ,  $\mu_{r,m}$  and  $A_m$  are the

corresponding values of the shared magnetic path. It should be noted that  $A_m$  represents the mean core cross-section of the shared magnetic path since this area is not constant along  $l_m$ . Moreover,  $A_m$  is tightly linked with the dimension  $c_a$  of the auxiliary core, as will be shown later in this section.

Considering the definitions from Figs. 6.7-a) and b), the following observations can be made:

- ▶ The height  $h_a$  of the auxiliary core must be as small as possible in order to reduce the length of the auxiliary core's magnetic path  $l_a$  and therefore reduce the reluctance  $R_a$ .
- ▶ The width  $a_a$  of the core cross-section must be large in order to increase the auxiliary core's cross-section  $A_a$  and therefore reduce the reluctance  $R_a$ . For the same reason, the depth of the auxiliary core  $d_a$  must be as close as possible to the depth  $d$  of the main core.
- ▶ The permeability  $\mu_{r,a}$  of the auxiliary core must be high in order to reduce the reluctance  $R_a$ .
- ▶ The air-gap between the auxiliary core and the main core must be kept as low as possible since this air-gap introduces a constant reluctance that deteriorates the sensitivity of the transducer.
- ▶ The number of turns  $N_{aux}$  of the auxiliary core only affects the absolute value of inductance of the auxiliary core but does not affect the sensitivity to changes in the main core's permeability. Therefore, a low number of turns is suggested in order to reduce the induced voltage in the auxiliary core's winding due to the flux in the main core, as will be shown in the next section.

The dimension  $c_a$  of the auxiliary core has a large impact on the transducer's sensitivity. For example, a small  $c_a$  would result in a short magnetic path  $l_m$  and therefore the auxiliary core's inductance would be mainly defined by the auxiliary core's reluctance  $R_a$ . On the other hand, a large  $c_a$  results in a large cross-section  $A_m$  of the shared magnetic path and therefore in a small shared reluctance  $R_m$ , thus deteriorating the sensitivity of the transducer. For this reason, the influence of this dimension on the transducer sensitivity was studied by means of FEM simulations. In order to generalize the analysis, a per-unit system was used whereby the width  $w$  of the main core was taken as base dimension



**Figure 6.8:** Simulation examples for different auxiliary core geometries. The sensitivities i.e. the changes  $\Delta L_{aux}$  in auxiliary inductance value resulting for various values of  $c_a$  and  $a_a$  (cf. Fig. 6.7) are presented.

while the relative permeability (in non-saturated state)  $\mu_{r,m}$  of the main core was chosen as base permeability value.

As mentioned earlier, the goal is to find the geometry of the auxiliary core which results in the highest sensitivity of the auxiliary core's inductance  $L_{aux}$  to changes in the shared magnetic path's reluctance  $R_m$ . Therefore, the simulation consists of measuring the difference in the auxiliary system's inductance  $\Delta L_{aux}$  when the permeability  $\mu_{r,m}$  of the main core drops by 50% for different values of  $c_a$ . Additionally, the effect of the auxiliary core's permeability  $\mu_{r,a}$  as well as the dimension  $a_a$  in this inductance variation is analyzed since these two parameters were found to have the greatest influence on the transducer's sensitivity.

Fig. 6.8 shows the magnetic flux density for four exemplary simulations, whereby also the respective simulation parameters and resulting inductance variations  $\Delta L_{aux}$  are shown. In Fig. 6.8-a), a comparatively small value of  $c_a$  was employed, resulting in a short shared magnetic path length  $l_m$ . On the other hand Fig. 6.8-b) shows the resulting flux density distribution for a larger value of  $c_a$ . When compared to Fig. 6.8-



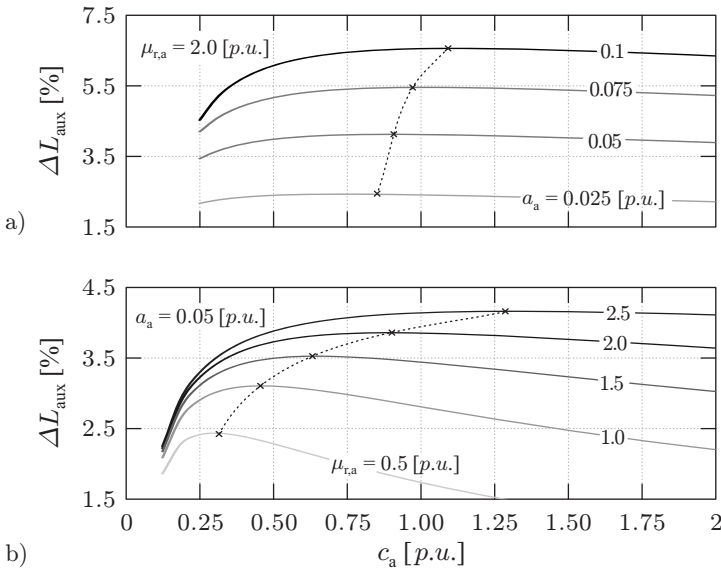
a), the flux lines in this figure show that a larger cross-section  $A_m$  is achieved with this value of  $c_a$ , thus no considerable gain in sensitivity is achieved (change in  $\Delta L_{\text{aux}}$  from 3.7% to 3.8%) in spite of the larger auxiliary core length  $c_a$ . Similar effects can be seen when comparing Figs. 6.8-c) and d), where a larger auxiliary core width  $a_a$  was used.

In Figs. 6.8-c) and d), the results for the same variation in  $c_a$  but with a larger value of  $a_a$  are shown. The increased value of  $a_a$  results in a larger auxiliary inductance variation when compared to Figs. 6.8-a) and b) due to the larger auxiliary core cross-section  $A_a$ , i.e. lower auxiliary core reluctance  $R_a$  while the shared magnetic path's cross-section  $A_m$  is not significantly increased, as can be seen from the flux lines in the respective figures.

The results of the performed parametric sweeps are summarized in Fig. 6.9. In Fig. 6.9-a), the effect of different auxiliary core widths  $a_a$  for a given auxiliary core permeability ( $\mu_{r,a} = 2.0$  p.u.) is presented. As expected, the variation  $\Delta L_{\text{aux}}$  in auxiliary inductance increases with increasing  $a_a$ , as the auxiliary core cross-section is also increased. Moreover, for each value of  $a_a$ , the value of  $c_a$  that maximizes the variation in auxiliary inductance can be found, as shown by the dashed line in Fig. 6.9-a). However, this optimum is not highly dependent on the core length  $c_a$ , i.e. this dimension and the core width  $a_a$  can be independently selected. As a result, independent of the core length  $c_a$ , the core width  $a_a$  must always be made as large a possible.

The sensitivity of the transducer to variations of the permeability  $\mu_{r,a}$  of the auxiliary core is studied in Fig. 6.9-b) for different values of auxiliary core width  $c_a$ . As mentioned earlier, a higher permeability of the auxiliary core affects positively the sensitivity of the transducer, whereby the value of  $c_a$  which maximizes the sensitivity can be found for each value of auxiliary core's relative permeability, as shown by the dashed line in Fig. 6.9-b). In this case however, the optimum value of core length  $c_a$  is considerably dependent on the value of relative permeability of the auxiliary core  $\mu_{r,a}$ . For example, if the main core and the auxiliary core possess the same permeability, i.e  $\mu_{r,a} = 1.0$  p.u., the peak of sensitivity is encountered when the length of the auxiliary core  $c_a$  is 0.45 times the width  $w$  of the main core whereas if the auxiliary core's permeability is 2.5 times that of the main core, the maximum sensitivity is found with an auxiliary core whose length  $c_a$  is 1.3 times the width  $w$  of the main core.

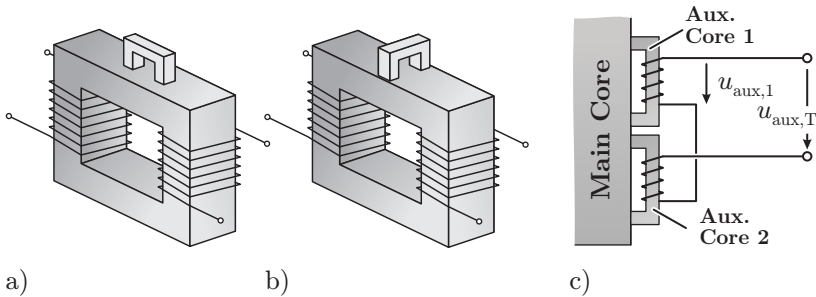
The previous analysis shows that, in order to achieve the highest



**Figure 6.9:** Sensitivity of the auxiliary system's inductance variation to different dimensions and permeabilities as determined through FEM simulations; a) Constant auxiliary core permeabilities  $\mu_{r,a} = 2.0$  p.u., variable width  $a_a$  and length  $c_a$ ; b) Constant auxiliary core width  $a_a = 0.05$  p.u., variable auxiliary core permeability  $\mu_{r,a}$  and length  $c_a$ . The width  $w$  of the main core was taken as base dimension while the relative permeability (in non-saturated state)  $\mu_{r,m}$  of the main core was chosen as base permeability value.

sensitivity of the transducer, first the relative permeability  $\mu_{r,a}$  of the auxiliary core must be selected as high as possible. Once this property is selected, the length  $c_a$  of the auxiliary core that maximizes the sensitivity for a given main core width  $w$  can be determined with help of Fig. 6.9-b).

With the rules for the selection of the auxiliary core dimensions defined, the next step in the implementation of the transducer is the proper placement of the auxiliary core, which ultimately defines the coupling of the main core's flux with the auxiliary core's winding. This topic is addressed in the following.

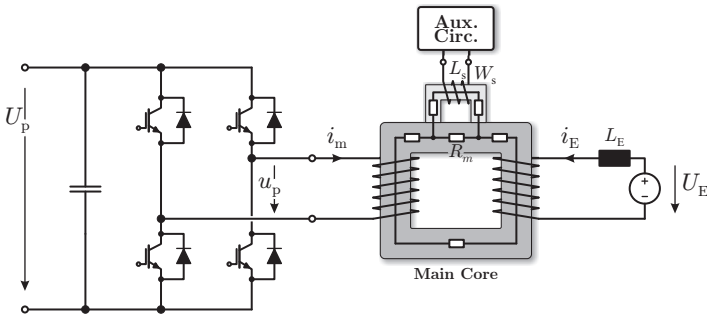


**Figure 6.10:** Arrangement of auxiliary cores utilized to reduce the effect of the main core’s flux on the auxiliary core inductance measurement. The auxiliary core can be placed so that its flux is a) parallel or b) orthogonal to the main flux. In order to further compensate for the induced voltage, the arrangement with two cores as shown in c) is proposed. The auxiliary core is not shown to scale.

## 6.4.2 Auxiliary Core Placement

The auxiliary core offers a parallel magnetic path for the flux in the main core and therefore a voltage is induced in the auxiliary core’s winding due to the main core’s flux. In a first step, the auxiliary core can be placed such that its magnetic flux is orthogonal to the main flux (cf. Fig. 6.10-b)) as opposed to a parallel orientation with respect to the main flux (cf. Fig. 6.10-a)) in order to reduce the coupling between the transformer’s main windings and auxiliary core’s winding. In order to further improve the decoupling from the main core’s flux, the arrangement presented in Fig. 6.10-c) is proposed. Here, two identical auxiliary cores with windings in opposed orientation are utilized. Nearly identical voltages are induced in the windings of these cores, and due to the opposed winding orientation, the induced voltages are virtually cancelling each other out.

In order to verify the effectiveness of this compensation scheme, consider the test circuit presented in Fig. 6.11, which is utilized to magnetize the ferrite transformer described in Chapter 5 (with secondary winding open) to nominal flux while the magnetizing current  $i_m$  is directly measured at the transformer’s primary winding. This test circuit is utilized in the following to experimentally verify the effectiveness of the proposed magnetic flux density transducer. The right-hand-side



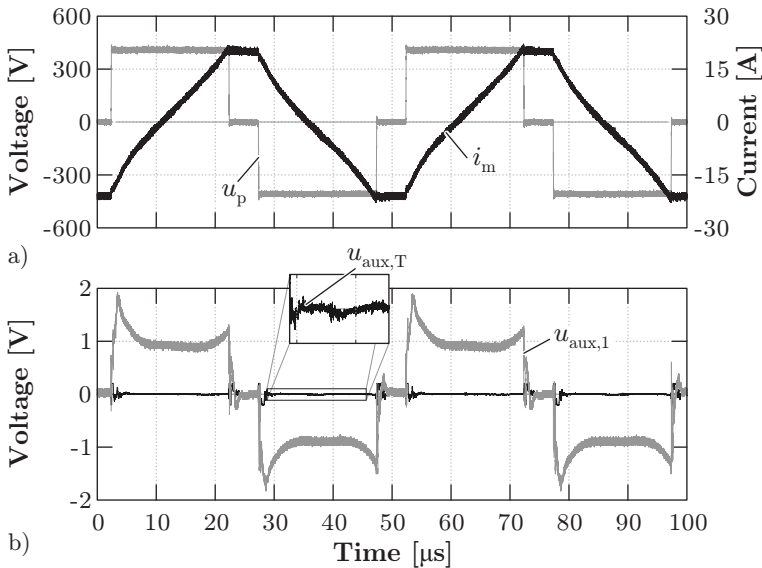
**Figure 6.11:** Test circuit consisting of a full-bridge driving the transformer’s main core, the magnetic flux density transducer and an external circuit utilized to force a DC flux component in the main core.

circuit is utilized later to force a DC flux component in the core.

Fig. 6.12 shows the results of the compensation arrangement testing. The full-bridge in Fig. 6.11, supplied with  $U_p = 400$  V, operated with 20 kHz switching frequency and 40 % duty cycle was used to magnetize the ferrite transformer described in Chapter 5. The resulting primary winding voltage  $u_p$  is shown in Fig. 6.12-a) together with the corresponding magnetizing current  $i_m$ . The auxiliary cores were arranged as presented in Fig. 6.10-c), whereby the voltage  $u_{aux,1}$  induced in the winding of the auxiliary core 1 and the compensated signal  $u_{aux,T}$  are depicted in Fig. 6.12-b). As can be seen, the voltage in a single auxiliary core winding is considerably higher and would result in a distorted measurement of the auxiliary inductance. When compensated, the signal  $u_{aux,T}$  features negligible induced voltage, thus this arrangement can be reliably used to extract the auxiliary inductance. This last task is performed by the driving circuit of the auxiliary core, as described in the next section.

### 6.4.3 Drive Circuit

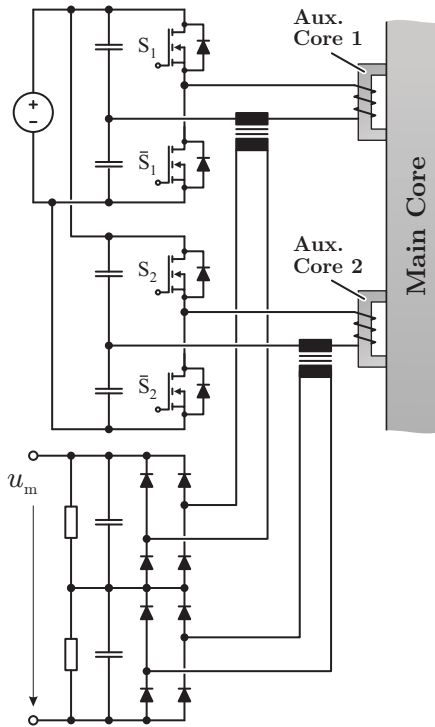
In order to extract the auxiliary inductance value, a constant amplitude high frequency excitation voltage is used to drive the auxiliary core, whereby the peak value of the current through the inductor is inversely proportional to its inductance. This current is later rectified and filtered, generating an LF signal directly related to the auxiliary



**Figure 6.12:** Testing of the compensation arrangement shown in Fig. 6.10-c): a) Applied voltage and resulting magnetizing current of the ferrite transformer described in Chapter 5; b) Induced voltage with (cf. Fig. 6.10-c)) and without (cf. Fig. 6.10-a)) compensation arrangement.

inductance and therefore to the magnetization state of the main core.

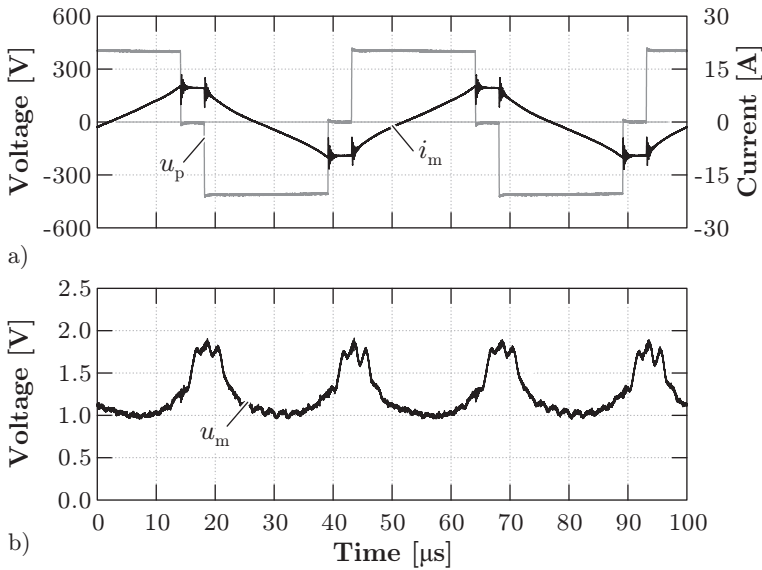
With the aforementioned driving circuit concept, however, the filtering stage at the output of the driving circuit defines the bandwidth of the transducer, thus, in order to improve this bandwidth limitation, the driving circuit of Fig. 6.13 is proposed. This circuit consists of two interleaved half-bridges phase-shifted by  $90^\circ$  driving each one of the auxiliary cores (each of these cores is then replaced by another pair of cores to compensate for the induced voltage, as shown in Fig. 6.10-c)) with a switching frequency several times higher than the main core's excitation frequency. Each bridge forces a current through their corresponding auxiliary core. Respective current transformers are used to sense this current which is then rectified by diode bridges. The output diode rectifiers are connected in series, causing the phase shifted currents to compensate the ripple in the output signal  $u_m$ , and therefore reducing the amount of required output filter capacitance and/or



**Figure 6.13:** Drive circuit utilized to extract the auxiliary inductance value.

increasing the bandwidth of the transducer.

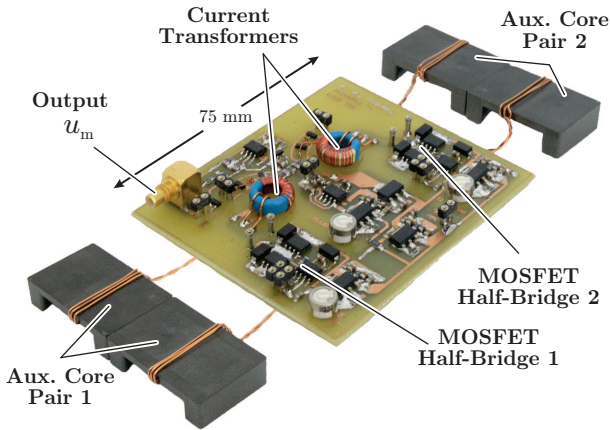
The final transducer comprising two pairs of auxiliary cores based on EPCOS EQ30/8 N87 cores and the described drive circuit was built and is shown in Fig. 6.15. This arrangement of cores (one pair for each auxiliary core in Fig. 6.13-a)) driven by the circuit presented in Fig. 6.13-a) was tested with the setup shown in Fig. 6.11. The resulting output signal  $u_m$  of the transducer is presented in Fig. 6.14-b). As shown in this figure, the transducer outputs a high signal value when the magnetizing current  $i_m$  reaches a high value, i.e. when the flux in the main core is entering the saturation region (cf. Fig. 6.14-a)). On the other hand, the output signal  $u_m$  stays low during the zero crossing of the magnetizing current, i.e. when the magnetic flux in the main core



**Figure 6.14:** Performance of the magnetic flux density transducer for unbiased operation: a) Excitation voltage  $u_p$  applied by the full-bridge shown in Fig. 6.11 and resulting magnetizing current  $i_m$ ; b) Output signal of the magnetic flux density transducer  $u_m$ .

is zero. The slight phase-shift between the peak magnetizing current  $i_m$  and the transducer's output signal  $u_m$  is due to the output filter capacitor of the drive circuit. However, since this signal is sampled only at the end of the freewheeling period, this phase-shift does not deteriorate the behavior of the closed loop controller, as described in the last section of this chapter.

The aforementioned behavior of the magnetic flux density transducer, comprising the drive circuit from Fig. 6.13-a), demonstrates the usability of this measurement concept, as the output signal of the transducer is directly related to the magnetization state of the main core. It is now the task of the digital controller to sample the transducer output signal  $u_m$  in order to detect and finally actively correct a biased magnetization state of the main core.



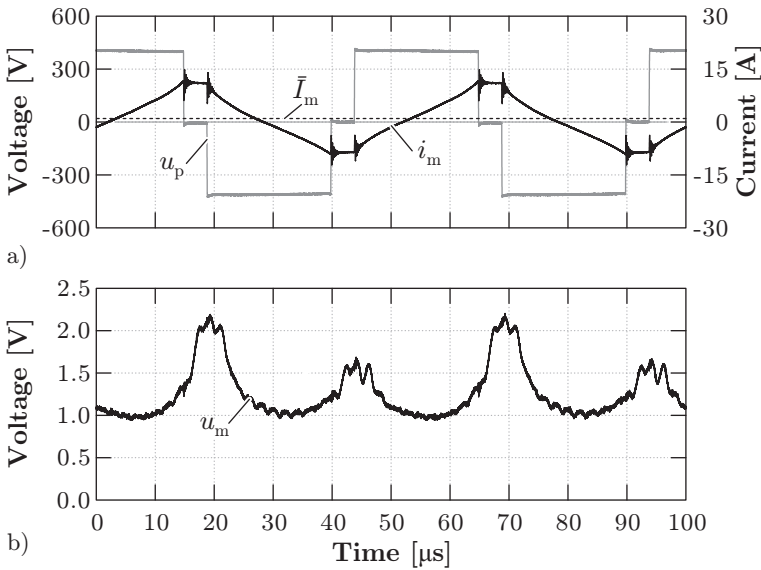
**Figure 6.15:** Hardware realization of the Magnetic Ear flux density transducer.

#### 6.4.4 Sampling Methods

The output signal shown in Fig. 6.14-b) continuously changes as the magnetization state of the main core is varying. This signal can be sampled at a high sampling rate, e.g. ten times higher than the frequency of the main core's excitation. A lookup table implemented in the digital control platform is utilized in order to translate the signal  $u_m$  into the instantaneous value of the magnetic flux density in the main core.

For the purpose of operating the main core with unbiased flux density, however, sampling the Magnetic Ear's output signal during the freewheeling states of the full-bridge (coinciding with the moment when the flux density is the highest in the main core) would suffice to obtain the DC magnetization state of the main core. This behavior can be seen from Fig. 6.16, where a DC component  $\bar{I}_m$  in the magnetizing current, i.e. in the main core's flux density was induced by adjusting the duty cycles of the test bridge (cf. Fig. 6.16-a)). Fig. 6.16-b) shows the resulting output signal  $u_m$  of the flux density transducer whereby a clear difference in its peak values can be noticed during two consecutive freewheeling intervals. Due to the biased flux density operation, the output signal  $u_m$  features its peak value at the end of the positive





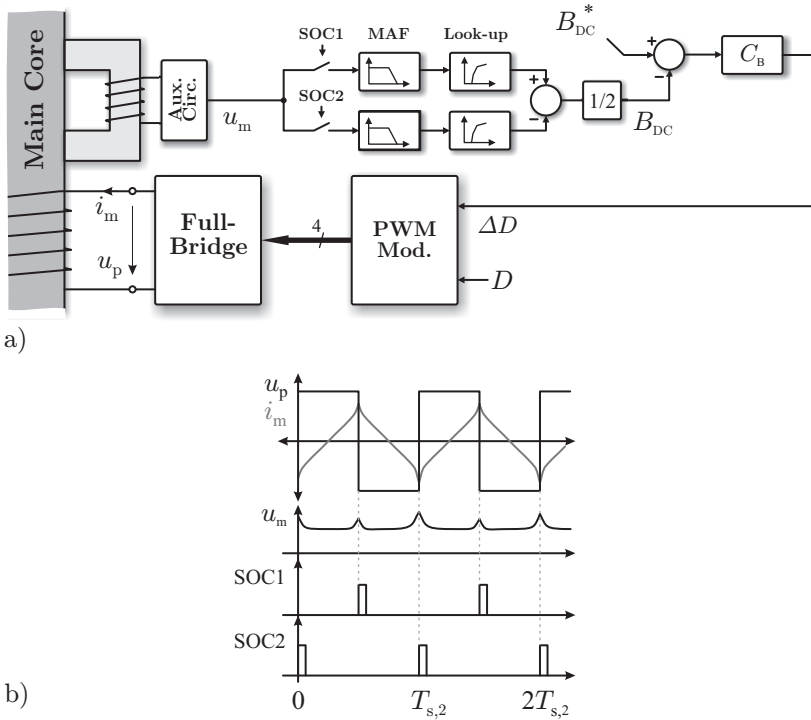
**Figure 6.16:** Performance of the magnetic flux density transducer for biased flux operation: a) Excitation voltage  $u_p$  applied by the full-bridge shown in Fig. 6.11 and resulting magnetizing current  $i_m$  with DC component  $\bar{I}_m$ ; b) Output signal of the magnetic flux density transducer  $u_m$ .

semi-cycle since it's at this instant when the main core's permeability is at its minimum, i.e. the auxiliary core's inductance is at its minimum.

The difference between the peak values of the output signal  $u_m$  at the end of the positive and negative semi-cycles is directly related to the biased magnetization state of the main core. This means that keeping this difference at its minimum is equivalent to minimizing the DC component of main core's magnetic flux density. This strategy is used to actively control the DC component of the magnetic flux density in the core, as will be experimentally shown in the next section.

## 6.5 Closed Loop Operation

The output  $u_m$  of the Magnetic Ear must be fed into the DSP controller of the full-bridge converter in order to actively compensate the DC



**Figure 6.17:** a) Feedback/balancing scheme: the output of the Magnetic Ear,  $u_m$ , is sampled by the ADC of the DSP board. By sampling on each switching event of the full-bridge (part b)), a construction of the DC flux density in the core is obtained and used to balance the flux in the main core.

bias of the flux density. In order to obtain the value of  $B_{DC}$  in the main core, the scheme shown in Fig. 6.17-a) was used. As can be seen from Fig. 6.17-b), different Start of Conversion (SOC) signals (the signals that trigger a conversion of the ADC converter of the DSP), i.e. SOC1 and SOC2 are generated at the positive and negative edges of the full-bridge output voltage  $u_p$ . The sampled values at each of these instants are independently stored and filtered by Moving Average Filters (MAF). In order to obtain the final flux density value, a look-up table is built based on the measurements of the Magnetic Ear output and the magnetic flux density calculated from the voltage applied to the

core. It should be noted that the gain from the Magnetic Ear output to the flux density is highly non-linear since, when the core is close to saturation, a small increase of the flux density generates a large change in the output signal of the transducer whereas, when the core is in the linear region, the change in output signal with respect to changes in the flux density is considerably smaller.

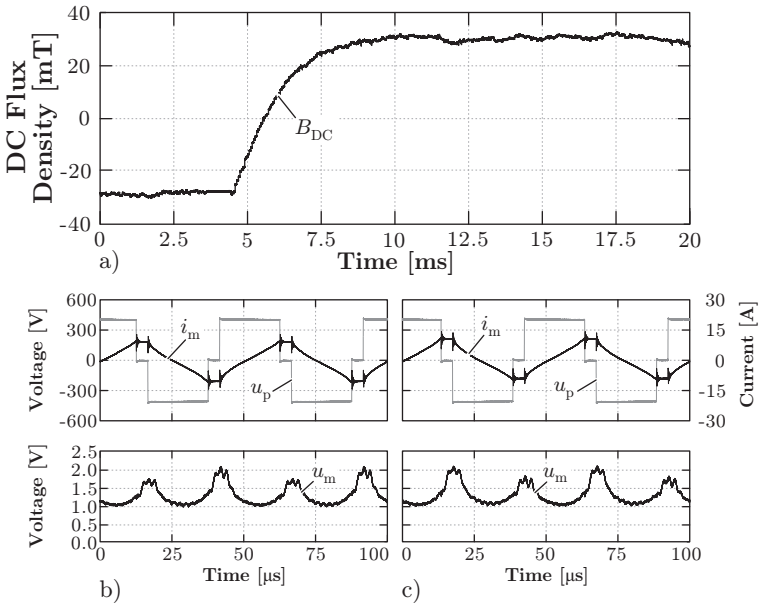
The outputs of the look-up tables are the absolute values of flux density in the main core at the switching instants. Therefore, the subtraction of these two signals gives twice the value of the DC flux density component  $B_{DC}$  inside the core. For example, in steady state operation, if no DC bias is present in the core, the output of the Magnetic Ear would be identical at the positive and negative edges of the applied voltage  $u_p$ . As a consequence, the output of the look-up tables, i.e. the flux density at the switching instants, would be identical and thus the measured DC flux density component would be zero.

In order to control the DC flux density in the core, a standard PI controller,  $C_B$  is used (cf. Fig. 6.17-a)). The output of this controller is the additional duty cycle  $\Delta D$  required to increase or decrease the DC voltage applied to the primary winding. In the PWM modulator, this signal is combined with the duty cycle  $D$  calculated to transfer the desired amount of power, or to achieve ZCS as described in Chapter 2. This duty cycle was left to 40 % in this case.

Several experiments for different testing conditions were realized in order to study the dynamic performance of this feedback loop.

### 6.5.1 Flux Density Reference Step

The first test, shown in Fig. 6.18-a), consists of a step response from  $-30\text{ mT}$  to  $30\text{ mT}$  in the DC flux density component reference  $B_{DC}^*$ . As can be seen, the feedback loop is successfully able to regulate within  $5\text{ ms}$  the DC component  $B_{DC}$  of the magnetic flux density. Considering the slow dynamics of the potential sources of a DC component in the voltage applied to the transformer (e.g. differences in switching times, forward voltage drops and gate driving signal delays), this response time is considered appropriate. Fast changes of the loading condition can also cause imbalances in the DC flux density component, as described in [119]. However, with modern digital control platforms, this problem can be solved by introducing a middle step in the duty cycle actualization, as described in [123]. Additionally in Fig. 6.18-b) and c), the voltage

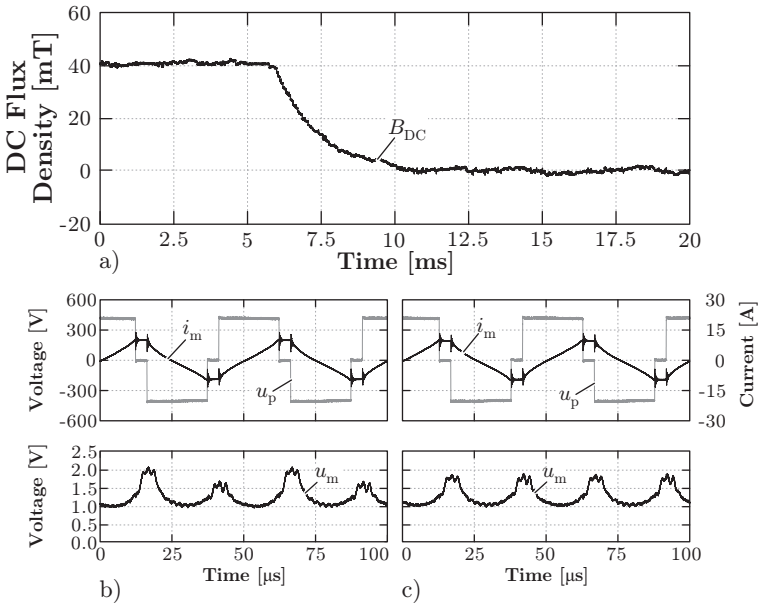


**Figure 6.18:** Step response of the closed-loop flux bias control scheme comprising the proposed transducer (cf. a)). Voltage  $u_p$  and current  $i_m$  (measured at the primary winding with secondary winding open) of the transformer and Magnetic Ear output  $u_m$  b) before and c) after the DC flux density step.

and current through the transformer together with the transducer's output signal are presented before and after the application of the step in  $B_{DC}^*$ . Here, the change in the output signal  $u_m$  can be clearly seen as the exhibits higher values at the positive voltage slopes before the step, meaning negative DC bias of the flux density. On the other hand, after the step in DC flux density, the higher values of the output signal are seen at the negative voltage slopes, which shows that the DC flux density component has changed to a negative value.

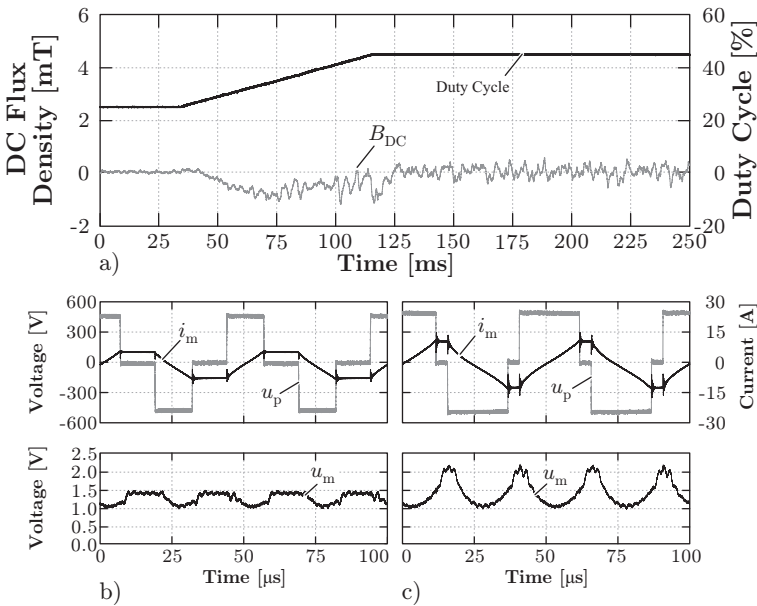
### 6.5.2 Disturbance Compensation

The second performed test consists of forcing an external DC flux density component with the external DC source and inductor shown in Fig. 6.11. By adjusting the current  $I_E$ , the DC flux density component



**Figure 6.19:** Response of the feedback loop to an external disturbance utilizing the proposed transducer. Voltage  $u_p$  and current  $i_m$  (measured at the primary winding with secondary winding open) of the transformer and the Magnetic Ear output  $u_m$  b) before and c) after the activation of the compensation loop.

$B_{DC,E}$  in the main core can be adjusted. This DC component is measured with the Magnetic Ear flux density transducer and used in the feedback loop for proper compensation with the driving full-bridge. The results of this test is shown in Fig. 6.19-a). Here, the feedback loop is left open until  $t=6$  ms, whereby before this time a forced DC component  $B_{DC,E}=40$  mT can be noticed. As the DC flux density component control loop is activated at  $t=6$  ms, this DC flux density component  $B_{DC}$  is regulated to zero after 5 ms, achieving finally an unbiased flux density operation. The output of the transducer before and after the activation of the feedback loop is shown in Figs. 6.19-b) and c) respectively. As can be seen, the transducer output features an unsymmetrical behavior before the compensation loop is activated, which implies a biased

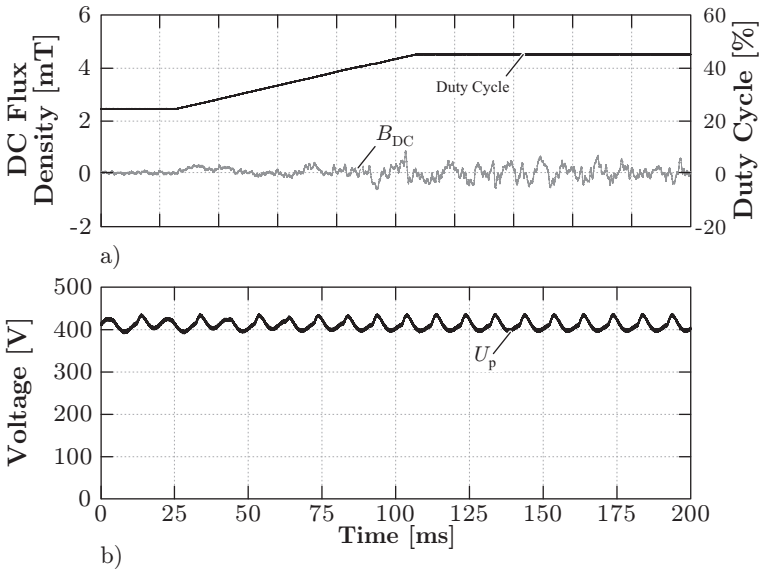


**Figure 6.20:** Feedback loop response to a change in duty cycle, representing a variation in transferred power. In a) the change in duty cycle and the respective response of the DC flux density component  $B_{DC}$  are shown. In b) and c), the transformer voltage  $u_p$  and current  $i_m$  (measured at the primary winding with secondary winding open) together with the transducer's output  $u_m$  is shown at low duty cycle and high duty cycle values respectively.

operation of the flux density. Once the compensation loop is activated, the DC flux density component is controlled to zero, which can be seen from the symmetrical behavior of the transducer's output signal.

### 6.5.3 Duty Cycle Ramp

An additional test consisting of ramping the duty cycle while controlling the DC flux density component to zero was performed. The duty cycle variation and the respective DC flux density component value  $B_{DC}$  are presented in Fig. 6.20-a). The duty cycle ramp starts at 25% and reaches 45%. The DC flux density component stays well regulated dur-



**Figure 6.21:** Response of the feedback loop to variation in the duty cycle and a 100 Hz harmonic in the DC-link voltage. In a) the duty cycle value and the controlled flux density  $B_{DC}$  are presented while b) shows the DC-link voltage with the mentioned 100 Hz voltage component.

ing the duty cycle ramp, with variations below  $\pm 1$  mT. Moreover, the primary voltage and magnetizing current of the transformer for 25 % and 45 % duty cycle are presented in Figs. 6.20-b) and c) respectively, where the change in the voltage's duty cycle can be clearly seen. Additionally, the output signal of the Magnetic Ear is affected for lower duty cycles as expected, reaching low values due to the lower reached magnetization state of the core.

#### 6.5.4 100 Hz Ripple in DC-link Voltage

Very often DC-DC converters are coupled with single-phase power factor correction rectifiers, which inherently generate a double frequency component in the DC-link's voltage. In order to test the performance of the compensation loop under these conditions, a 100 Hz voltage component was inserted in the driving bridge's DC-link voltage, as shown in

Fig. 6.21-b). The response of the feedback loop presented in Fig. 6.21-a) shows that the DC flux density component  $B_{DC}$  is kept regulated under this variation of the DC-link voltage and during the ramping of the converter's duty cycle.

These tests show the effectiveness of the proposed magnetic flux density transducer and its respective drive circuit and feedback scheme, ensuring an unbiased DC flux density operation of the transformer.



# 7

## Final Assembly and Back-to-Back System

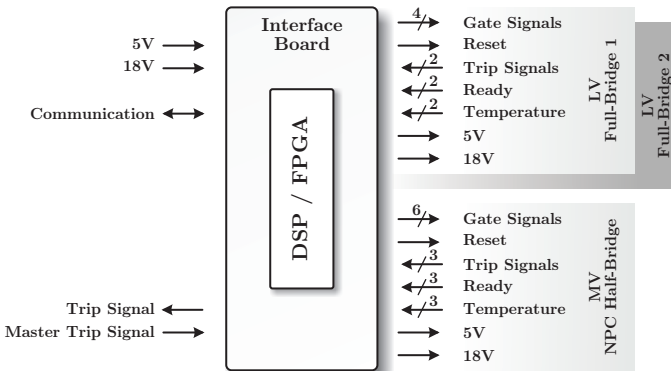
The previous chapters covered in detail the analysis, design and construction of the three main components of the high-power DC-DC converter: the MV side power electronics, the LV side power electronics and finally the MF transformer design together with its magnetic flux density balancing concept. The final step in the converter's construction consists of the complete assembly of the aforementioned converter parts, as will be addressed in the following. In addition, the required control platforms which provide the semiconductors' gate signals as well as supervision of the system's operation will be shown.

With the complete converters operational, the setup utilized to conduct the experimental tests is presented along with the respective experimental results.

### 7.1 Final Converters' Construction

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In order to complete the construction of the HC-DCM-SRC and TCM-DAB converters, the platform utilized to control the system was designed. Both control units are based on a DSP/FPGA platform integrating various functionalities such as 12 PWM channels, 32 general purpose input/output signals, 16 ADC channels and trip zone circuitry, among others. The respective block diagrams and assembled control units will be shown in the following section.

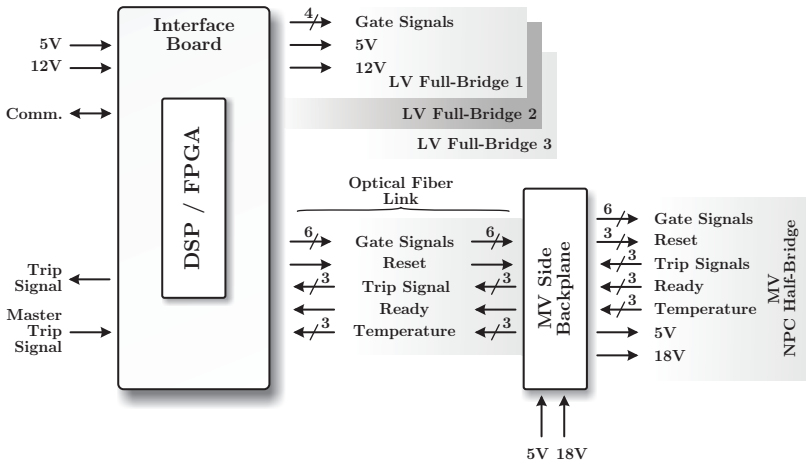


**Figure 7.1:** Block diagram of the HC-DCM-SRC’s control board. The control platform comprises three main blocks dedicated to each of the bridges of the converter. In addition, input and output trip signals together with communication and power supply inputs are provided.

### 7.1.1 Control Platforms

The control platform comprises the TMS320F28335 floating point DSP from TI and the LFXP2-5E-T144/TN144 FPGA from Lattice. This control unit is built on a PCB which additionally contains all voltage regulators and circuitry for all analog inputs. An interface board is required in order to link the control board with the respective gate signals, feedback signals and analog inputs.

A block diagram of the interface board for the HC-DCM-SRC is presented in Fig. 7.1. On the right-hand-side, the main blocks comprising the input/output signals for the three controlled bridges are shown, which are directly linked to the IGBT modules’ gate driver units (cf. Section 3.4.5). On the LV side bridges, four gate signals for each bridge are required. Additionally, all feedback signals such a trip and ready flags together with the analog temperature measurements are read by the DSP/FPGA unit. The power supply lines are routed through the interface board into the respective gate driver boards. The third block in Fig. 7.1 corresponds to the control and feedback signals to/from the NPC half-bridge on the MV side of the converter. In this case, one extra IGBT module needs to be controlled with respect to the LV side full-bridges, and therefore two additional gate signals are utilized together



**Figure 7.2:** Block diagram of the TCM-DAB converter’s control board. The main blocks are the outputs for the control of the three LV side bridges and the optical input/outputs utilized to control the MV side NPC half-bridge.

with the extra trip, ready and temperature signals.

From the left-hand-side, the power supply inputs, 5 V and 18 V are provided. A serial communication port links the control platform to the PC, allowing a real-time monitoring and modification of all DSP variables. The gate driver units are equipped with trip signals alerting of malfunction in the converter bridges. This trip signal must be propagated through the converter in order to promptly clear the fault, ensuring a safe turn-off process of the system. In addition, since the converter will be used as part of a larger system, a trip output and a master trip input signals are provided in order to alert the complete system about a fault as well as shutting down in case an external trip has been detected.

For the TCM-DAB converter, the interface board comprises three blocks for the gate signals and supply lines of the three LV side full-bridges’ gate units. Since the MOSFET gate drivers on the LV side of this converter do not possess feedback features, no input signals are required in the interface board. The input/output signals for the MV side NPC half-bridge are the same as the ones described for the HC-DCM-SRC. These signals, however, are transmitted through optical

fibers in order to achieve a high isolation between the control board and the MV side bridge. These optical signals are transformed into voltage signals in the MV side backplane, which directly interfaces the gate driver units of the MV side bridge. In addition, an independent power supply is utilized to power this backplane. Similar as with the HC-DCM-SRC, supply inputs are provided together with the required serial communication port and trip signals.

The software programmed in this platform allows to independently adjust the three TCM-DAB control signals: the phase-shift  $\phi$ ; the MV side duty cycle  $D_{MV}$  and the LV side duty cycle  $D_{LV}$ . Other functionality such as burst or continuous operation are also supported in order to safely test the converter. In case of the HC-DCM-SRC, only duty cycle control is provided. According to the described operation of the this bridge (cf. Section 2.3) one side of the converter is left uncontrolled.

The control platforms for the designed converters are integrated into the complete systems, therefore enabling the assembly of both converters as will be now presented.

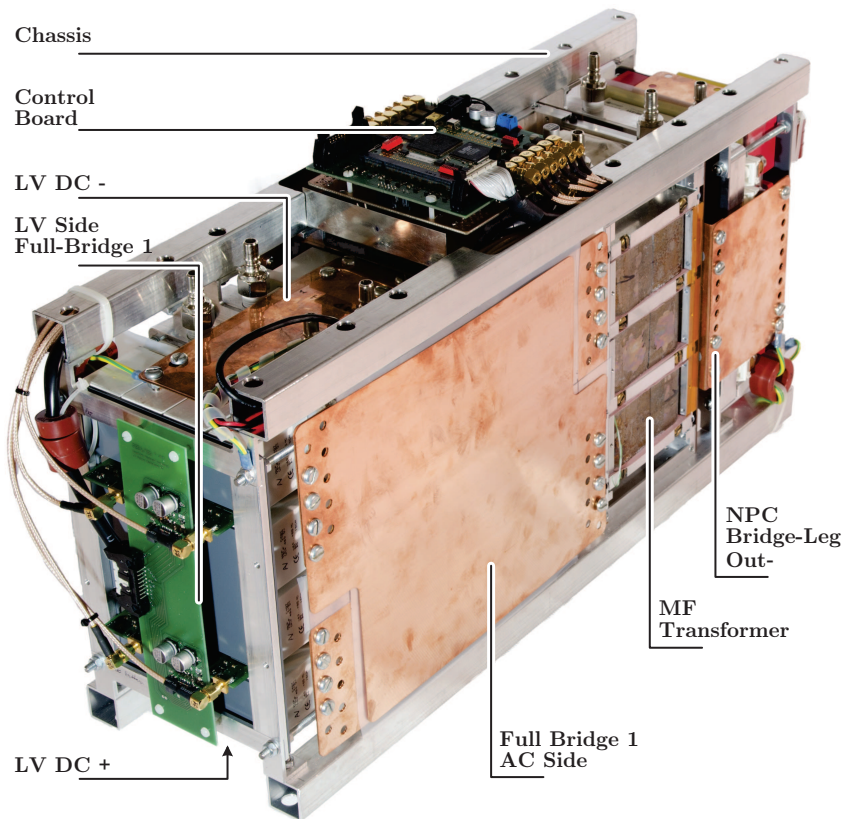
## 7.1.2 Converters' Mechanical Arrangement

The HC-DCM-SRC comprising: the LV side bridges, the MV side bridge, the MF transformer and the control platform is shown in Figs. 7.3 and 7.4.

The converter is arranged with the two LV bridges in the front, followed by the MF transformer and the MV bridge in the rear. Since all bridges and the MF transformer were designed with equal height and depth, they can all be fitted within an aluminum frame serving also as chassis in order to achieve a high mechanical stability. The AC power connections from the MV and LV bridges to the transformer are done with respective 0.5 mm copper plates, which are placed at the sides of the converter. The DC-link connections are placed on the top and bottom for both MV and LV side bridges. Additionally, all water-cooling connections are accessible from the top, leading to an easy connection of the hoses carrying the cooling fluid.

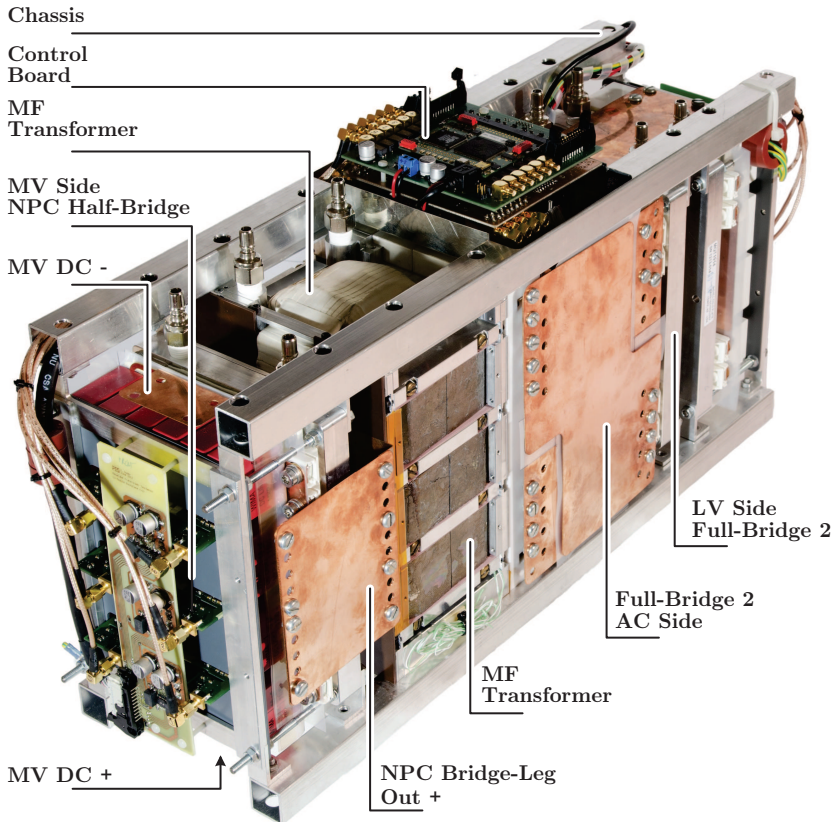
All gate and feedback signals are routed through the hollow aluminum bars in order to shield them from external disturbances. These signals are routed to the previously presented control board, which is placed on the top of the assembly.

The final construction of the TCM-DAB converter is presented in



**Figure 7.3:** Final assembly of the HC-DCM-SRC high-power DC-DC converter (front view).

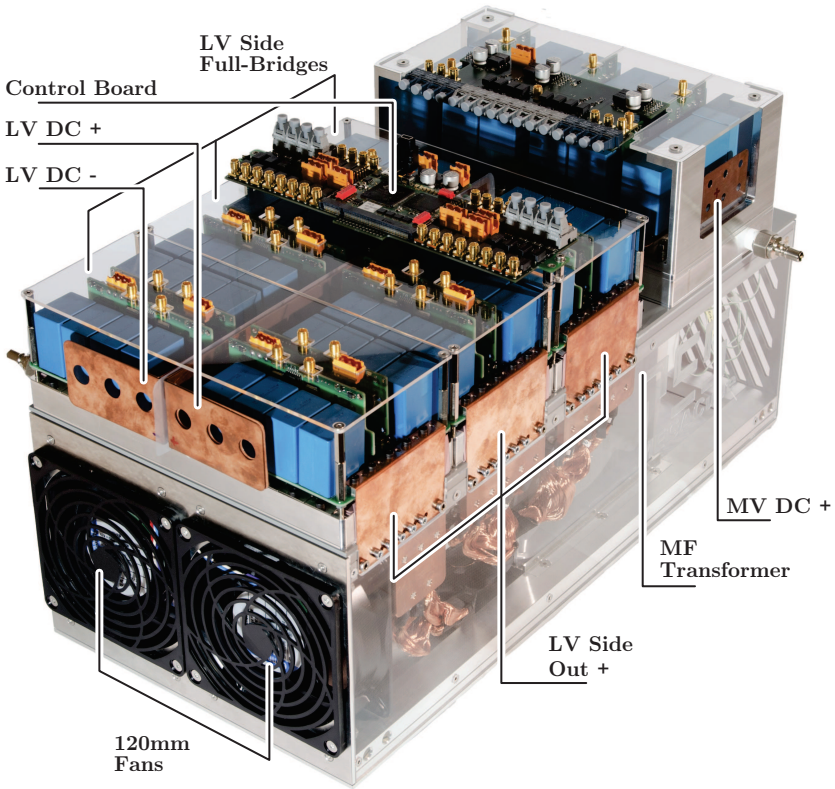
Figs. 7.5 and 7.6. On the bottom of the construction, the ferrite transformer is placed, whereby its top cover serves as mounting plate for the water-cooled heat sinks of the power electronic bridges. The three LV side full-bridges are paced next to each other and their connection to the MF transformer is done through independent copper plates, as shown in Fig. 7.5. The DC-link connection of the these bridges is done from the front with two copper busbars which then connect to all LV side bridges. Behind the LV side bridges, the MV side NPC half-bridge is placed. The MV side backplane is placed on the top contacting the



**Figure 7.4:** Final assembly of the HC-DCM-SRC high-power DC-DC converter (back view).

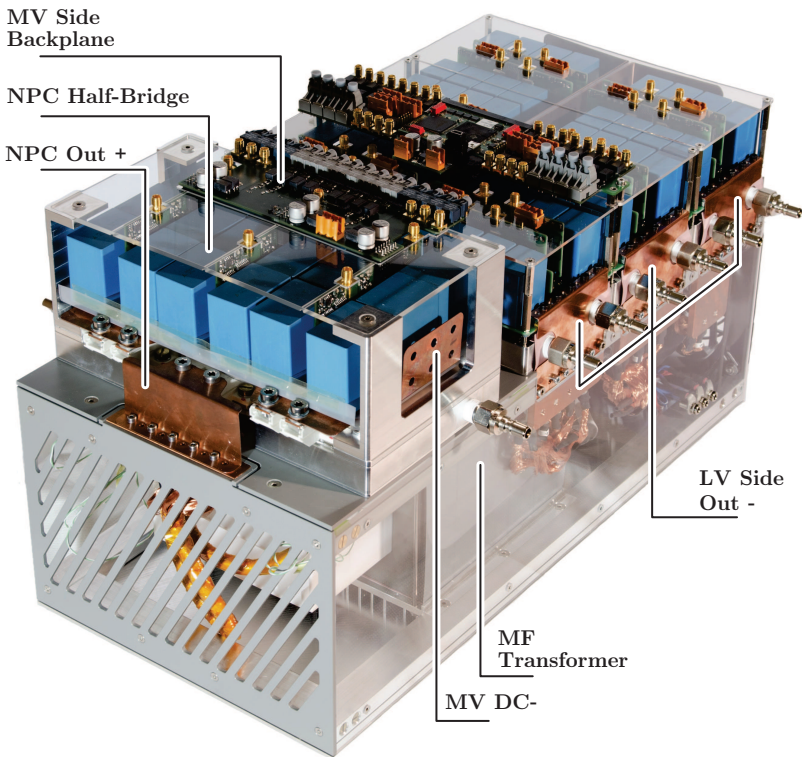
respective gate drivers. The MV side DC-link connections are placed on each side of the bridge, while the AC connections are done from the front and back side of the bridge. Finally, an aluminum frame provides the mechanical stability of the converter.

With the final construction of the converters described, the power density of the units can be calculated and displayed together with the calculated efficiencies of each system, as presented in Fig. 7.7. Considering power density, the HC-DCM-SRC system achieves the highest value, as expected due to the different cooling concepts, and core ma-



**Figure 7.5:** Final assembly of the TCM-DAB converter high-power DC-DC converter (front view).

materials utilized in both converter transformers. When analyzing the different contributions for volume, the biggest difference between the two systems is found in the MF transformer, given that the volume of the TCM-DAB converter's ferrite transformer comprises the air-cooling channel (cf. Fig. 5.19) necessary for the operation of the transformer. It should be noted that in case of the HC-DCM-SRC, the share of empty space within the converter parts exceeds that of the TCM-DAB converter mainly due to the large amount of customized components designed for this last system and the requirement of easy access to the bridges' input and output signals in the case of the HC-DCM-SRC.

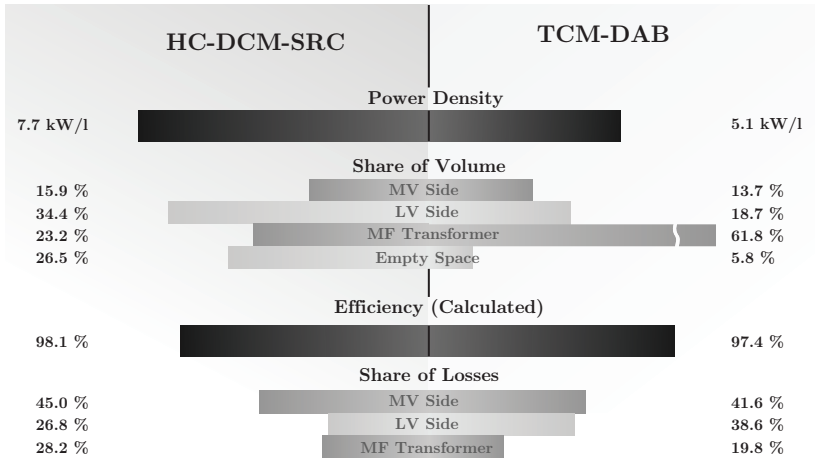


**Figure 7.6:** Final assembly of the TCM-DAB high-power DC-DC converter (back view).

On the other hand, the calculated efficiencies show a better performance for the HC-DCM-SRC due to its guaranteed QZCS operation on the LV and the MV sides for all operating conditions. This fact is seen in the loss share, where in the case of the TCM-DAB, the switching losses on the LV side represent a large contribution to the overall losses, despite the utilization of MOSFETs in these bridges.

With the two converters constructed, the means to test these systems while transferring high amounts of power in a standard laboratory environment will be presented in the next section.



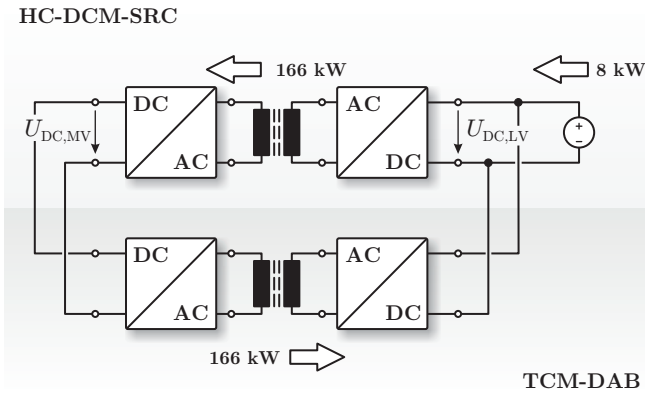


**Figure 7.7:** Summary of power densities and efficiencies at rated power of both designed converters and the respective volume and loss shares.

## 7.2 Back-to-Back Setup

Both converter systems, the HC-DCM-SRC and the TCM-DAB, possess bidirectional power transfer capability. Additionally, they possess equal terminal specifications such as power level and input/output voltages. This feature is utilized for conveniently performing the required experimental testing.

The concept of the test setup is shown in Fig. 7.8. This arrangement, known as back-to-back connection, is based on a direct connection of the MV side and LV sides DC-links of the two converters. One converter, e.g. the HC-DCM-SRC transfers power from the LV to the MV side, therefore charging the MV side DC-link. On the other hand, the TCM-DAB is adjusted to transfer power from the MV to the LV side, i.e. charging back the common LV DC-link. Furthermore, an external power supply is utilized to provide the losses of the system, which in this case at nominal conditions are about 8 kW. With this setup, the main part of the power circulates via the two converters, while only a small portion must be externally provided by the power supply, enabling the experimental testing in a standard laboratory environment, as was also demonstrated in [59].

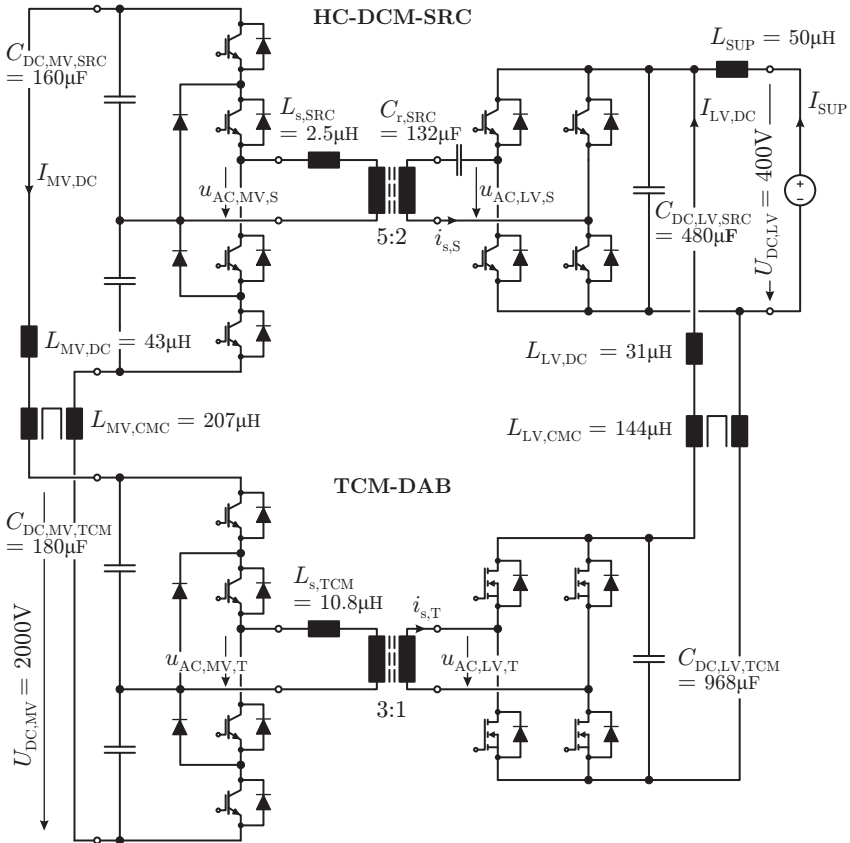


**Figure 7.8:** Concept of the back-to-back assembly. The HC-DCM-SRC is utilized to fix the LV and MV side voltages (without control of power flow) while the TCM-DAB controls the amount of power transferred between the MV and LV side DC-link.

A more detailed representation of the back-to-back arrangement is presented in Fig. 7.9. Here, additional inductors  $L_{LV,DC}$  and  $L_{LV,CMC}$  for the differential- and common-mode filtering between the HC-DCM-SRC and the TCM-DAB converters are placed on the LV side. In a similar way, the  $L_{MV,DC}$  and  $L_{MV,CMC}$  are utilized for differential- and common-mode filtering in the MV side. The DC side currents  $I_{LV,DC}$ ,  $I_{MV,DC}$  and  $I_{SUP}$  between the LV side DC-links, the MV side DC-links and the external power supply, are measured with current shunts in order to determine the total amount of circulating power between the converters.

It should be noted that the utilization of the HC-DCM-SRC and the TCM-DAB results specially convenient for this back-to-back setup as the HC-DCM-SRC is utilized to fix the voltage on the MV side, therefore from the TCM-DAB's point of view, two controlled voltage sources are connected to its DC-links, thus being able to directly control the amount of transferred power by adjusting the control signals while the HC-DCM-SRC naturally adapts to the transferred power level, keeping good regulation of the MV side DC-link.

With this arrangement, the simultaneous high-power testing of both systems can be performed, as will be shown in the next and final section



**Figure 7.9:** Details of the back-to-back assembly. Differential- and common-mode inductors are placed in order to decouple the two systems.

of this chapter.

## 7.3 Final Experimental Results

The testing sequence of the back-to-back system was implemented as follows: First the duty cycle of the HC-DCM-SRC is set to constant 48%. The duty cycles and phase shift of the TCM-DAB are calculated

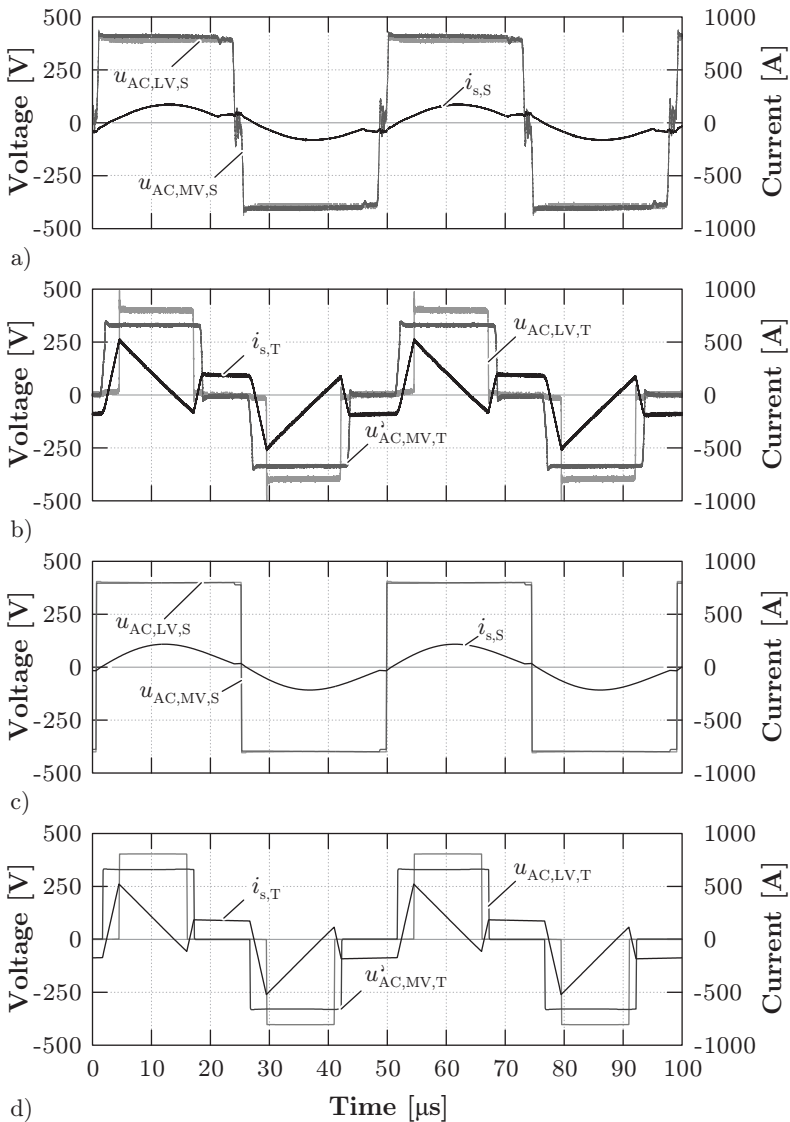
as described in Section 2.3.2 in order to transfer the desired amount of power and to switch  $I_{MV,SW} = 60 \text{ A}$  and  $I_{LV,SW} = 180 \text{ A}$  with the MV and LV side semiconductors respectively. The calculated values for phase-shift  $\phi$ , the MV side duty cycle  $D_{MV}$  and the LV side duty cycle  $D_{LV}$  are set in the TCM-DAB DSP with the system unpowered. Once the gate signals are activated, the external power supply fixing the voltage  $U_{DC,LV}$  is ramped-up to the full voltage of  $400 \text{ V}$ . This way, a soft start of the system is achieved while all critical quantities can be safely monitored.

With the aforementioned test concept of the two converters, high power testing of the system was performed. In Fig. 7.10, the AC-link quantities for both converters for a total of  $50 \text{ kW}$  of transferred power are presented. In Fig. 7.10-a), the resonant pulse combined with the magnetizing current can be seen in the AC-link current  $i_{s,S}$ . It should be noted that given the comparatively low amount of transferred power, the magnetizing current, utilized to reduce switching losses in the IGBT switches, represents a large part of the total current. Additionally, the small difference of voltages the reflected MV side voltage  $u'_{AC,MV,S}$  and the LV side voltage  $u_{AC,LV,S}$  is visible, which corresponds to the voltage difference required to transfer the specified  $50 \text{ kW}$  of power.

The complete back-to-back system shown in Fig. 7.9 was simulated using Gecko simulation software [60] with the operation conditions shown in Table 7.1. When compared with the simulation results shown in Fig. 7.10-c), a good agreement of the experimental waveforms can be seen for the HC-DCM-SRC system, proving the validity of the analysis performed in the previous chapters.

Fig. 7.10-b) shows the AC-link experimental quantities for the TCM-DAB system for  $50 \text{ kW}$  of transferred power while Table 7.1 presents the TCM-DAB duty cycles and phase shift for this operating point. The current  $i_{s,T}$  exhibits the expected triangular current shape, with the values of switched currents on the MV and LV side,  $I_{MV,SW}$  and  $I_{LV,SW}$  adjusted to achieve soft-switching transitions in all semiconductor devices. A peak current of about  $500 \text{ A}$  is switched off by the MOSFETs of the LV side full-bridges. Furthermore, the simulated waveforms shown in Fig. 7.10-d) confirm the validity of the previously performed analysis for this converter.

For this power level ( $50 \text{ kW}$ ), the total input power from the external  $400 \text{ V}$  supply is  $4.3 \text{ kW}$ , corresponding to a total back-to-back system efficiency of  $91.4 \%$  (cf. Table 7.1). It should be noted that



**Figure 7.10:** Continuous test of the back-to-back assembly with a total of 50 kW of transferred power: a) HC-DCM-SRC AC-link experimental waveforms; b) TCM-DAB AC-link experimental waveforms; c) HC-DCM-SRC AC-link simulated waveforms; d) TCM-DAB AC-link simulated waveforms.

**Table 7.1:** TCM-DAB duty cycles and phase shift for different transferred powers. In addition, the total input power from the external power supply, corresponding to the total generated back-to-back system losses, are also presented.

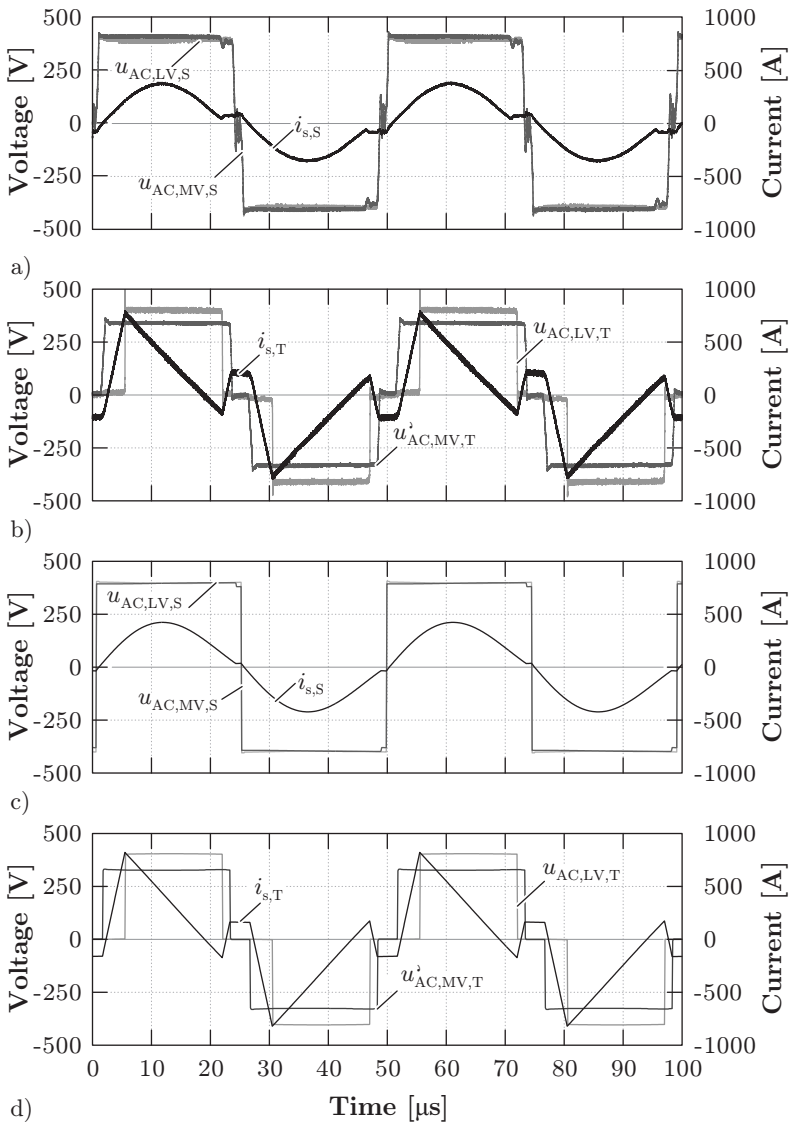
Parameter	Transferred Power	
	50 kW	80 kW
TCM-DAB MV side duty cycle	33.6 %	41.8 %
TCM-DAB LV side duty cycle	25.4 %	32.0 %
TCM-DAB phase-shift	21.9 °	26.9 °
Total back-to-back system power losses	4.3 kW	5.6 kW
Total back-to-back system efficiency	91.4 %	93.0 %

this efficiency corresponds to the total back-to-back system efficiency and not to the individual (HC-DCM-SRC and TCM-DAB) converters' efficiency. Nevertheless an improvement is achieved when operating at higher transferred power, as will be visible when the power level is increased in the next test.

The next measurement was done at 80 kW of circulating power, with the results shown in Fig. 7.11-a) for the HC-DCM-SRC. As can be seen, the HC-DCM-SRC features a higher current amplitude with respect to the operation at 50 kW, which reflects the higher amount of power transfer. It should be noted that, in comparison to the waveform in Fig. 7.10-a), the applied AC voltages remain virtually unchanged in spite of the higher transferred power, proving the capability of the HC-DCM-SRC to operate with a (nearly) constant input to output voltage transfer ratio. This feature is confirmed by the simulated waveforms shown in Fig. 7.11-d), where a good agreement of the simulated and experimental results can be seen.

The resulting waveforms of the TCM-DAB for this test are presented in Fig. 7.11-b) while Table 7.1 shows the TCM-DAB duty cycles and phase shift for this operating point. The triangular current shape is adjusted in order to achieve soft-switching transitions of all devices, as previously discussed. Furthermore, Fig. 7.11-d) shows the simulation results for this test, where a good matching of the simulated and experimental waveforms can be seen.

The total power delivered by the external 400 V power supply is 5.6 kW, corresponding to a total back-to-back system efficiency of 93 % (cf. Table 7.1). This efficiency represents an important improvement



**Figure 7.11:** Continuous test of the back-to-back assembly with a total of 80 kW of transferred power: a) HC-DCM-SRC AC-link experimental waveforms; b) TCM-DAB AC-link experimental waveforms; c) HC-DCM-SRC AC-link simulated waveforms; d) TCM-DAB AC-link simulated waveforms.

with respect to the value achieved at 50 kW of transferred power, showing the tendency of the system to higher efficiencies when operated at higher power levels.

Overall, the back-to-back testing of the converters shows a good agreement of experimentally measured voltage and currents with respect to the waveforms presented in Chapter 2 and the respective simulated results. For the HC-DCM-SRC, the sinusoidal pulse superimposed with the transformers magnetizing current can be seen and the natural adjustment of this pulse's amplitude, and therefore of the transferred power, is visible when the power transfer is increased by the TCM-DAB converter while the MV side voltage is kept nearly unchanged. This behavior proves the capability of the HC-DCM-SRC to operate with fixed voltage transfer ratio, while achieving QZCS in all semiconductor devices. On the other hand, the capability of the TCM-DAB to adjust the power transfer by modifying its control parameters, namely the MV side and LV side duty cycle and the phase-shift, was experimentally proven. Moreover, the capability of this converter to operate in QZCS mode on the MV side was tested by generating triangular current shape described in Section 2.3.2, whereby an accurate adjustment of the amount of residual switched current was achieved.



# 8

## Summary / Conclusions

Standard LF transformers present fundamental performance limitations due to their operating frequency and their passive nature. In order to overcome these limitations, the isolation transformer can be integrated with power electronics-based conversion stages. With this arrangement, an SST concept is realized, enabling a reduction in size/weight of the power transformer and an increased functionality of the complete AC-AC conversion system.

These new features are especially useful in traction applications, where, due to the limited space available for accommodating the LF transformer, a great benefit concerning weight and efficiency is achieved, improving the performance of the traction system. In Smart Grid applications however, the reduction in size is not a mandatory requirement, as these transformers are typically utilized in systems without stringent space restrictions. In this case, the additional functionality provided by the front-end power electronic circuits is the major motivation for the utilization of SST technology in this area.

An SST comprises all power conversion types found in power electronics engineering: AC/DC (rectifier), isolated DC/DC and DC/AC (inverter). Moreover, in order to fully replace a classical LF transformer, the SST is required to provide bidirectional power flow. These features result in diverse solutions, which can be classified in terms of the modularity level they achieve. The first aspect to be decided is the suitable number of power conversion stages, which can range from single-stage to three-stage conversion systems. The second dimension of modularization is given by the means to connect to three-phase systems, either in the LF or MF sides of the converter. Finally, a modularization concerning the series/parallel connection of modules in order to

deal with the MV level and the high currents on the LV side has to be considered. These three modularization axes lead to a fine mesh of available converter options, whereby higher modularity in all axes is recommended due to the ability to independently design each converter stage, enabling the synthesis of highly optimized components. Moreover, higher modularity can lead to higher reliability due to the capability of redundant cell-type constructions, whereby the system is able to operate with one or more faulty cells.

The previous discussion leads to the selection of a three-stage converter approach. Within this system, the high-power DC-DC conversion stage is identified as the main challenge within the converter construction, as it is responsible for the isolation of the primary and secondary sides, it is operated at MF/MV level and, in order to be a replacement for LF transformers, must comply with high efficiency requirements. Three main aspects can be highlighted within the design process of the converter: topology/modulation; MV side power electronics and magnetic components' design.

## **Topology/Modulation**

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Soft-switching schemes are mandatory within high-power DC-DC converters in order to meet the required efficiency goals while operating at MF and MV. In this context, two converter topologies result attractive given their capability of operating under soft-switching, namely ZCS, conditions: the HC-DCM-SRC and the TCM-DAB converter. While both these converters are able to operate the MV side semiconductors under ZCS conditions (also the LV side in case of the HC-DCM-SRC), the two systems differ greatly in their operating behavior. On the one hand, a very robust and reliable operation is achieved with the HC-DCM-SRC given its fixed voltage transfer ratio (and isolation), where a tight link between the DC voltages of both MV and LV sides is achieved. Moreover, this converter naturally achieves ZCS in all semiconductor devices for any operating condition. On the other hand, the TCM-DAB is able to achieve ZCS on the MV side and provides controllability of the power flow by actively adjusting the LV and MV side bridges' duty cycles and the phase-shift. This feature, however, comes with the price of lower efficiency due to the requirement of switching high currents on the LV side.

During the experimental verification done through the back-to-back

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connection of these two converters, their performance was tested, confirming a reliable operation of the HC-DCM-SRC. The high switched currents of the TCM-DAB caused considerable disturbances in the gate and feedback signals, rendering the practical implementation of this converter more challenging in comparison to the HC-DCM-SRC. For these reasons, a construction of a high-power DC-DC converter considering the HC-DCM-SRC structure is recommended in all cases, whereby the TCM-DAB would be better suited for applications which require power flow control of the high-power DC-DC stage.

## MV Side Power Electronics

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The implementation of the previously discussed modulation schemes enables the operation of the semiconductor devices under soft-switching conditions at least at the MV side. In devices with bipolar power stages, such as IGBT switches, the operation under ZCS does not imply zero switching losses. This phenomenon is due to the charge stored in the n-drift region of this type of semiconductor switches during their conduction phases. A simple model of the charge behavior, which requires two semiconductor parameters, was proposed in order to model the semiconductor losses under ZCS conditions. Given the growing amount of applications utilizing this type of modulation scheme, it is recommended that semiconductor manufacturers include these and possibly other meaningful parameters in their datasheets in order to facilitate an estimation of the switches' switching losses under ZCS conditions.

In addition, the strategies available to reduce the switching losses under ZCS conditions were presented and experimentally analyzed. The first strategy consists of switching a residual amount of current (QZCS), virtually eliminating the turn-on losses of the complementary switches found for standard ZCS. This switching condition can be achieved by adjusting the control variables in case of the TCM-DAB or by decreasing the value of the magnetizing inductance in case of the HC-DCM-SRC. The utilization of this strategy can reduce the switching losses to about one half when compared to pure ZCS and is therefore strongly recommended in order to achieve a highly efficient design of the converter. The second strategy is related to the shaping of the current during the conduction phase of the semiconductor. A time interval with low current can be provided for the semiconductor to achieve high recombination of its internal charge carriers, thus reducing the amount of losses

encountered during switching.

The utilization of SiC-based devices could open new frontiers in the construction of SSTs due to their (i) fast switching speeds leading to higher switching frequencies and hence to smaller reactive components; (ii) higher reachable junction temperatures, leading to smaller cooling solutions and (iii) high voltage blocking capability. However, several issues such as low parasitic power circuit layouts, passive components able to deal with high temperatures and high voltage packaging, among others need to be addressed. With a reliable package construction which overcomes the aforementioned limitations, SiC semiconductors would allow a major step in the implementation of SSTs, where the most attractive feature is the possibility to operate in the MF range while dealing with the MV level in a single semiconductor device, resulting in simple converter structures in comparison to the multi-cell arrangements described in this thesis.

## MF Transformer

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Two optimized transformer concepts differing in their core material and cooling strategies were constructed aiming for different power density/efficiency goals. The first one is based on nanocrystalline core material and water-cooling for heat extraction. The second prototype is based on ferrite cores and a forced air-cooling system.

Extensive experimental verification on these transformers exhibited several issues in their construction which were not accounted for during the design process. The first of them is the unsymmetrical current distribution within the litz wire strands. Due to the large dimensions and the operation at MF, parasitic effects not seen at lower frequencies and/or smaller sizes become visible, deteriorating the performance of the transformer. It is therefore recommended that litz wire manufacturers provide additional flexibility in the construction of their products, such as selection of length of lay and number of strands' sub-groups or bundles.

When measuring the core losses in the nanocrystalline transformer design, large differences in the losses generated in each core-pair were found. These differences were counteracted by the insertion of an air-gap in the transformer's magnetic path. This measure was however insufficient for levelling the losses in each of the cores, therefore further studies are required in this area in order to reveal the origin these losses.

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With increased frequency, the volumetric heat generation in the MF transformer is increased for a constant efficiency, resulting in high values of heat fluxes which demand high performance cooling systems. The nanocrystalline transformer's cooling system is based on water-cooled heat sinks. The losses induced in this cooling system, constructed purely of aluminum, were measured, where relatively large values were identified and attributed to induced eddy currents in these aluminum pieces not visible during the performed FEM simulations. For this reason, deeper analysis of the magnetic field distribution and the consequently generated losses in the transformer's cooling structure are required in order to effectively and efficiently implement MF transformers in future applications.

A further major research topic not covered in this thesis is the effectiveness of the utilized isolation strategies concerning long term operation and different operating conditions. This topic must be addressed in order to make the SST technology an attractive replacement for standard LF transformers.



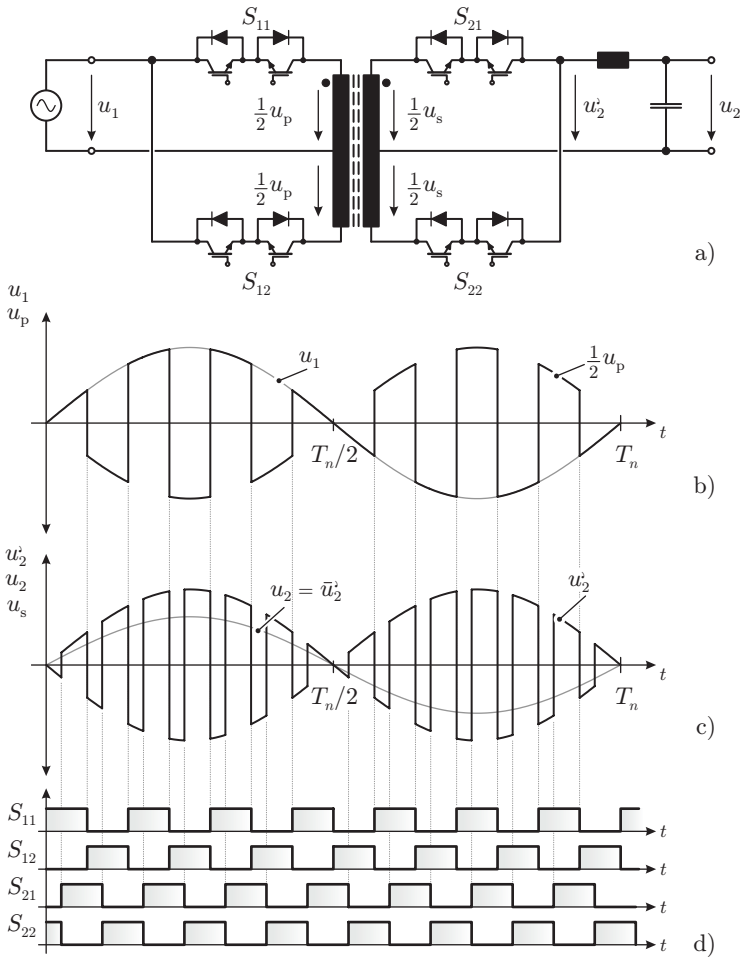
# A

## History of SSTs in Traction

The first form of a AC-AC power electronic circuit with galvanic isolation and power flow control, presented in Fig. A.1-a), was proposed in the early seventies by W. McMurray [124] and it may be considered as the first conceived isolated SST. This circuit consists of two four-quadrant switches on the primary side connected to a single-phase grid while feeding the primary of a center-tapped higher frequency transformer winding. On the secondary side, a similar structure comprising the required filter inductor and output capacitor is included. The switches  $S_{11}$  and  $S_{12}$  operate in complementary mode with 50 % duty cycle, same as with the secondary switches  $S_{21}$  and  $S_{22}$ . By adjusting the phase-shift between these two pairs of switches, the output voltage can be regulated while achieving sinusoidal input current [124]. It should be noted that the operation of this converter resembles in great manner that of the modern DAB DC-DC converter, reported originally in the nineties [67] and analyzed in Chapter 2.

In Fig. A.1-b) the grid voltage  $u_1$  as well as the voltage  $u_p$  applied to the transformer primary winding is presented. As can be seen, the input sinusoidal voltage  $u_1$  is transformed into a higher frequency AC voltage signal  $1/2 \cdot u_p$  with sinusoidal varying peak value. The control signals of the semiconductor devices are shown in Fig. A.1-d) where a phase-shift between the devices on the primary and secondary side can be seen. This phase-shift results in the secondary side voltage waveform presented in Fig. A.1-c) where the chopped voltage  $u_2$  is then filtered by an LC circuit, originating a sinusoidal output voltage  $u_2$  whose amplitude is controlled through the phase-shift of the switches' control signals.

A variation of the concept shown in Fig. A.1-a), which comprises



**Figure A.1:** First reported isolated SST concept [124] based on four-quadrant switches able to control output voltage and/or input current amplitude while providing galvanic isolation. In a), the circuit diagram (here shown with IGBT switches) is presented. The input and output voltages together with the respective transformer voltages are presented in b) and c). In d) the switches' control signals are presented.



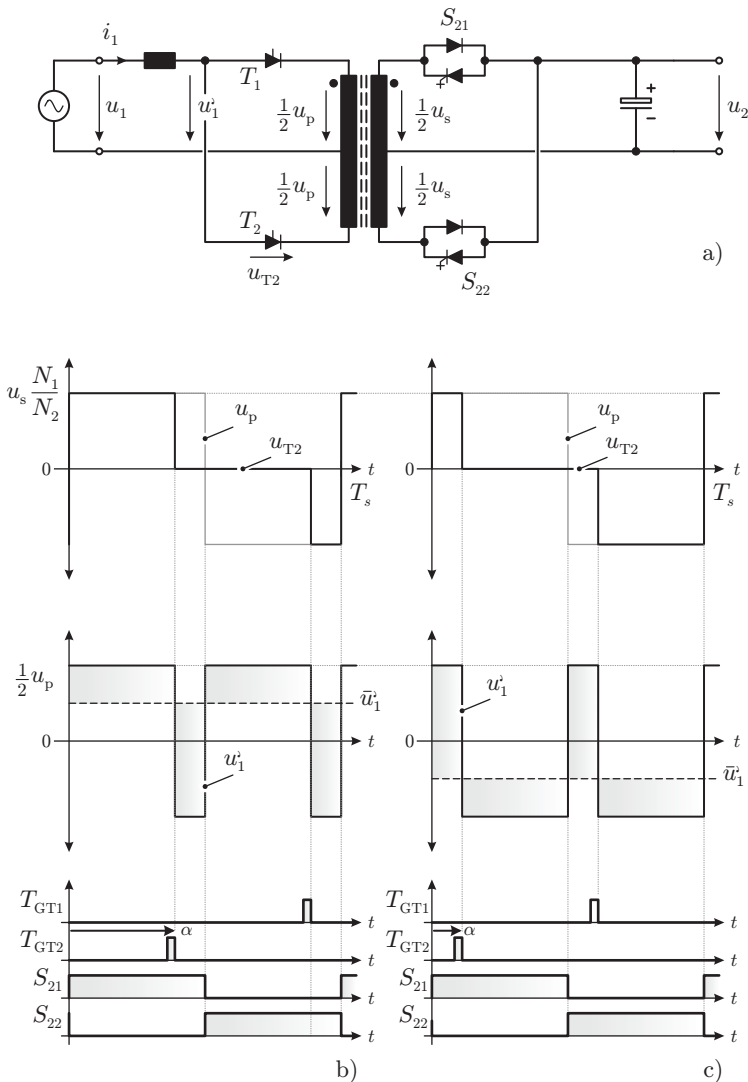
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a DC output voltage, is presented in Fig. A.2-a). This converter, proposed by Mennicken in 1978 [125] is the first step towards a solution for traction applications, where a DC output voltage is required in order to feed the driving inverters of the locomotive's electrical machines. In order to deal with the MV level at the input side, this concept utilizes thyristor devices on the primary side and gate turn-off thyristors with respective antiparallel diodes on the secondary side.

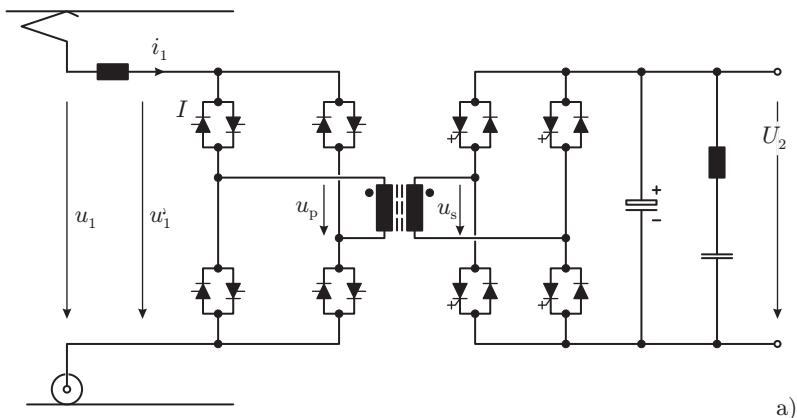
The operating principle is explained with Fig. A.2-b). At the beginning of a switching cycle, the secondary side switch  $S_{21}$  is turned on, thus applying a positive voltage at the secondary side of the transformer, which is translated, through the respective turns ratio  $N_1/N_2$ , into a positive voltage  $1/2 \cdot u_p$  at the primary side of the transformer; thyristor  $T_1$  is conducting and carrying the primary inductor current. After a certain angle  $\alpha$ , thyristor  $T_2$  is turned on, causing thyristor  $T_1$  to turn off and consequently the voltage  $u_1$  reverses its polarity. At the half of the switching period, switch  $S_{21}$  is turned off and  $S_{22}$  is turned on, causing the voltage  $u_1$  to reverse its polarity since thyristor  $T_2$  stays on. After reaching the angle  $\alpha$ , now measured from the middle of the switching period, thyristor  $T_1$  is turned on; due to the polarity of  $u_p$  this results in a current commutation and/or turn-off of  $T_2$  and an inversion of the polarity of  $u_1$ .

As can be seen from Fig. A.2-b), by controlling the angle  $\alpha$ , the voltage  $u_1$  applied to the grid can be controlled, whereby a sinusoidal variation of this angle along the mains period would result in a voltage waveform which is in average sinusoidal and is synchronized with the mains voltage  $u_1$ . By modifying the phase-shift between the fundamental of the voltage  $u_1$  and the input voltage  $u_1$ , the power transferred to the output side can be controlled, thus regulating the output DC voltage  $u_2$ .

A modification of the converter presented in Fig. A.2-a) which is specifically targeted for traction applications is shown in Fig. A.3-a) and was also proposed by Mennicken [125]. This converter utilizes four pairs of thyristors in antiparallel configuration at the input (MV side). These 4 thyristor pairs build a full-bridge arrangement able to operate in four quadrants, making it especially suitable for traction applications. This thyristor-based full-bridge converts the input voltage into a higher frequency voltage waveform applied to the MF transformer. On the secondary side, a gate turn-off thyristor-based full-bridge with the respective antiparallel diodes is utilized. This full-bridge converts the



**Figure A.2:** SST concept reported in [125] for isolated rectifier with thyristor-based front-side and turn-off devices on the load (DC) side. The circuit diagram is presented in a) while the relevant voltages and switching devices' control signals are shown in b) and c) for a control angle  $\alpha = \pi/3$  and  $\alpha = 2\pi/3$  respectively.

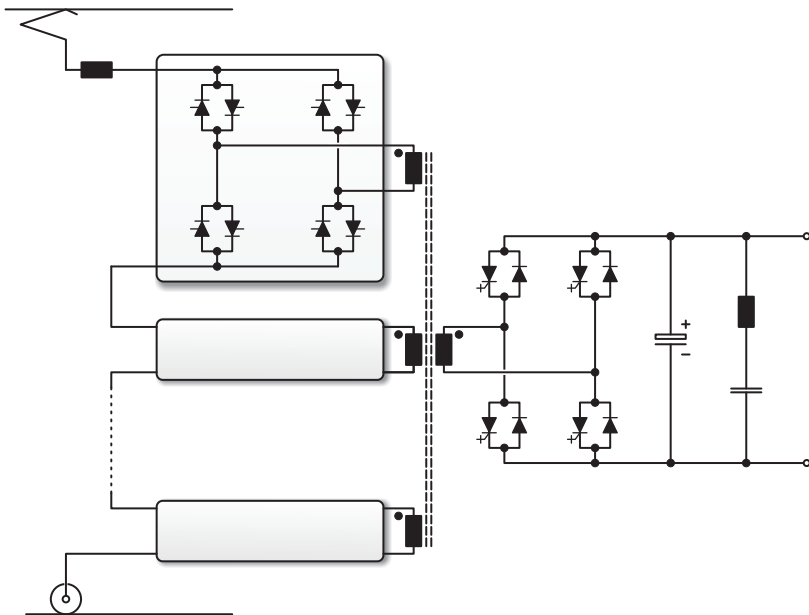


**Figure A.3:** Modification of the concept presented in Fig. A.2-a) comprising a full-bridge structure at the input and output sides [125].

AC voltage from the transformer secondary into a DC voltage supplying the inverter's DC-link. Furthermore, an LC filter network is connected to the output DC-link in order to filter the power fluctuation with twice mains frequency originating from the single-phase supply.

The solution shown in Fig. A.3 utilizes a single bridge to block the MV side voltage, which would require semiconductor devices with blocking capabilities in the tens of kilovolts range [4]. In order to deal with these high voltages while utilizing lower-rated semiconductor devices, a modular solution for the traction converter was proposed by Östlund in 1993 [126]. This concept with modular input stage is shown in Fig. A.4. Here, the input thyristor-based full-bridge is divided into cells which are stacked in series in order to deal with the total input voltage. With this structure, the transformer primary winding is split into several parts, each of them connected to one thyristor-based full-bridge as can be seen from Fig A.4. The LV side rectifier remains unchanged with respect to the concept in Fig. A.3.

Kjaer and Norrga analyzed an IGBT-based solution following the concept from Fig. A.4 [127, 128]. This concept is shown in Fig. A.5 where each thyristor pair of the primary side converter presented in Fig. A.3 is replaced by a pair of IGBT switches in anti-series connection. In addition, the secondary side full-bridge is also based on IGBT

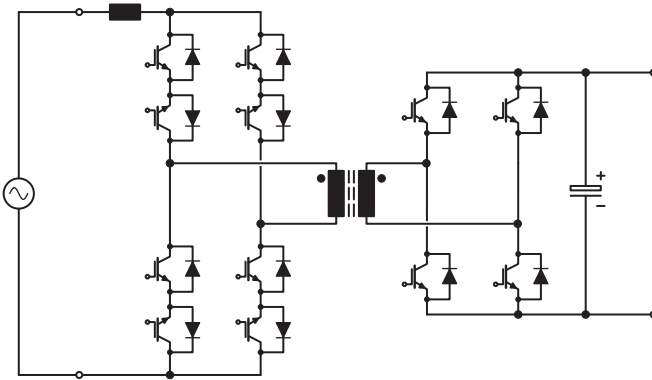


**Figure A.4:** Cascaded AC side version of the concept presented in Fig. A.3 proposed in [126] in order to deal with MV levels encountered in traction systems.

switches. With this converter, the commutation time of the semiconductors is considerably reduced with respect to the thyristor-based approach, resulting in increased switching frequencies and therefore in a highly compact input inductor and transformer design.

The concept shown in Fig. A.5 does not present a solution for the direct connection to an MV catenary line feeding a locomotive due to the relatively low blocking capabilities of available IGBT devices with maximum voltage rating of 6.5 kV. For this reason, Norrga proposed in [128] a structure with a series connection of four-quadrant IGBT switches as presented in Fig. A.6. With this arrangement, the MV side converter can be directly connected to an MV level railway feeding line while being operated in the MF range and therefore reaching a highly compact design.

This series connection of semiconductors, however, requires special measures in order to ensure a symmetric dynamic and static voltage dis-

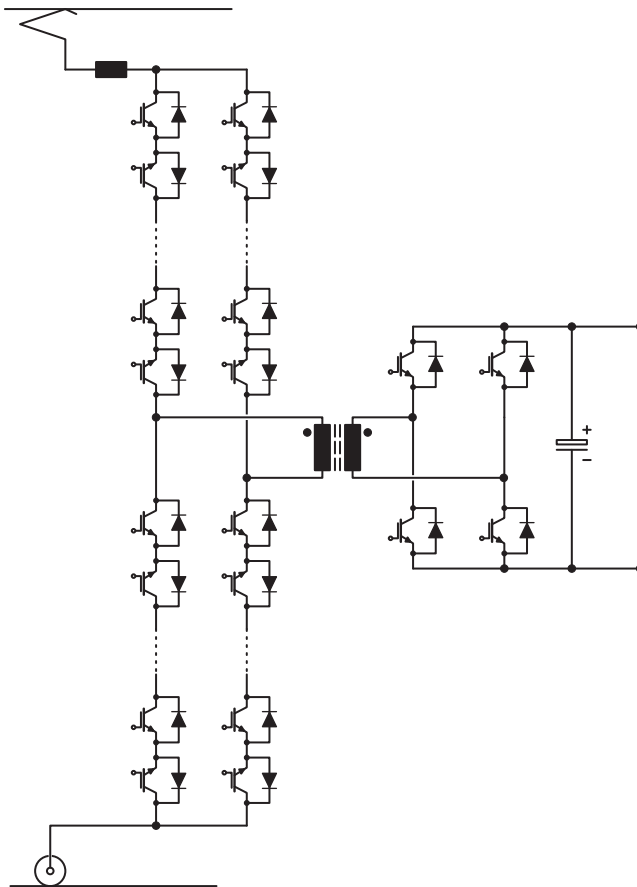


**Figure A.5:** IGBT-based variation of the concept presented in Fig. A.3-a) with possibility of higher operating frequencies [127].

tribution among the series-connected semiconductor devices. For this reason, other topology options were further studied in order to provide the required voltage blocking capability while ensuring the operation of the IGBT switches within their specified voltage range.

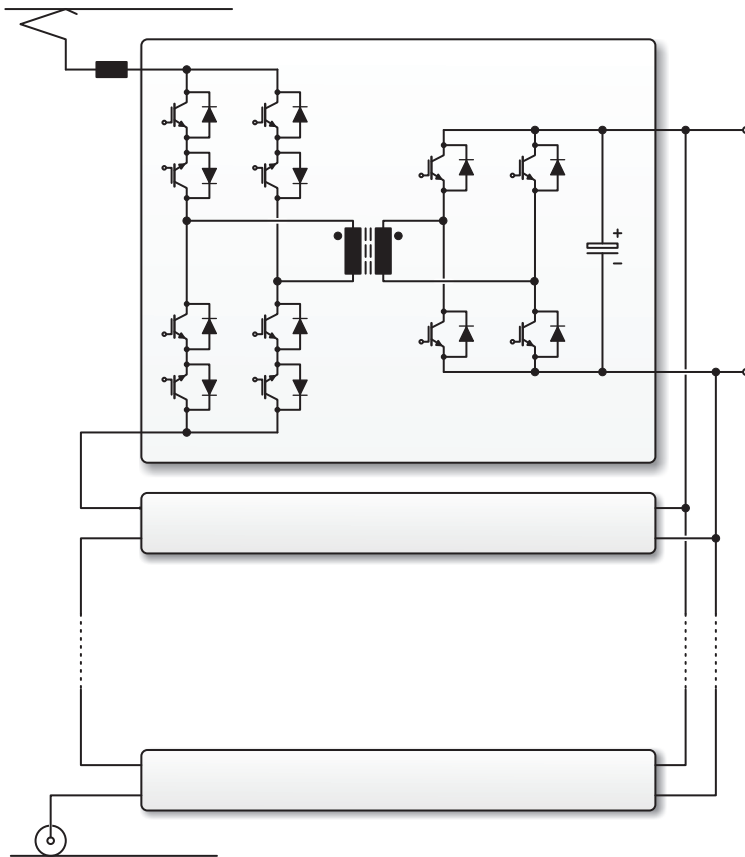
A modular version of the converter presented in Fig. A.6 was realized by Hugo in 2007 [7] targeting a 1.2 MVA power rating and 400 Hz switching frequency. This topology is shown in Fig. A.7. Here, a highly modularized converter was built, comprising independent transformers and output full-bridges. This concept utilizes identical modules connected in series on the MV side and in parallel in the LV side. As can be seen, with this concept, also independent transformers for lower power levels are utilized.

So far, the presented converters feature a matrix-type direct conversion from the MV side LF voltage to a MF voltage waveform supplying the transformer, which forces the utilization of four-quadrant semiconductor devices. The next step in modularization of the converter structure is to split the input stage into a rectifier providing a regulated DC-link which supplies an inverter operating at MF and feeding the transformer (cf. Chapter 1). This approach represents the modern modular traction solution and has been considered e.g. in 2007 by Steiner [13] and by Weigel and Hoffman [14, 44, 97]. This fully-modular structure is shown in Fig. A.8, where the resonant DC-DC



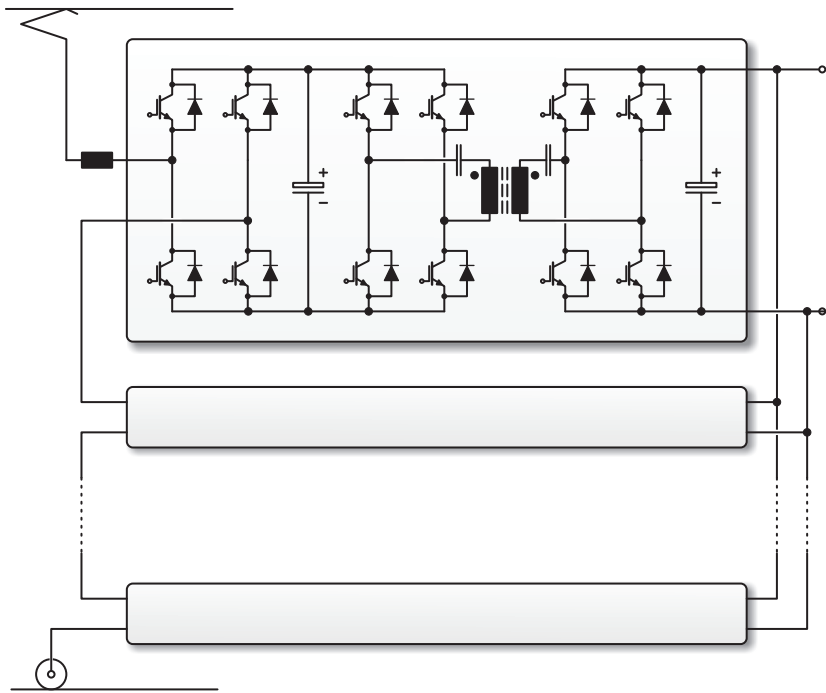
**Figure A.6:** Variation of the concept presented in Fig. A.5 with input series connection of four-quadrant IGBT switches for achieving higher voltage blocking capability [128].

converter stage discussed in Section 2.3.1 is also utilized. The benefit of this modular approach, which utilizes the ISOP concept, is the possibility to independently design each of the converter stages, thus enabling highly efficient and highly compact solutions. Further variations of this concept with other DC-DC converter structures have been reported [17, 59].



**Figure A.7:** Modular version of the concept presented in Fig. A.5 with ISOP connection for high input voltage blocking capability and high output currents [7].

An alternative to the concept presented in Fig. A.8 is shown in Fig. A.9 where the MV side of the DC-DC converter is replaced by a half-bridge structure with a mid-point DC-link. Here, two switches, with twice the current rating, are required for the MV side of the DC-DC converter. The solutions presented by Taufiq in 2007 [129] and by Engel in 2003 [45] comprise a multi-winding transformer and a single LV side converter, thus losing the modularity feature offered by the

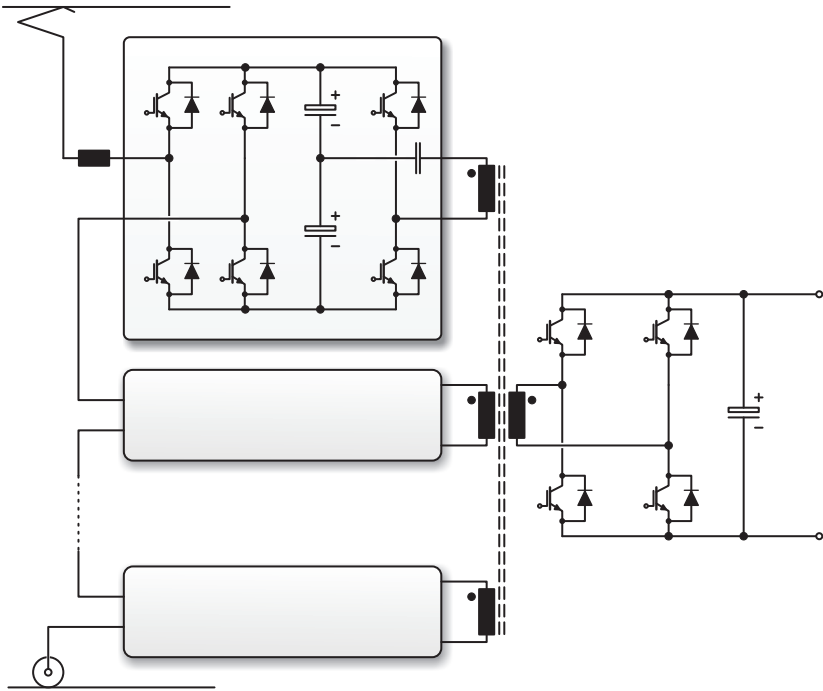


**Figure A.8:** DC-link-based variation of the concept presented in Fig. A.7 where the input AC side converter of each module is split into a rectifying stage and an inverter stage operated at MF [13, 44].

structure shown in Fig. A.8.

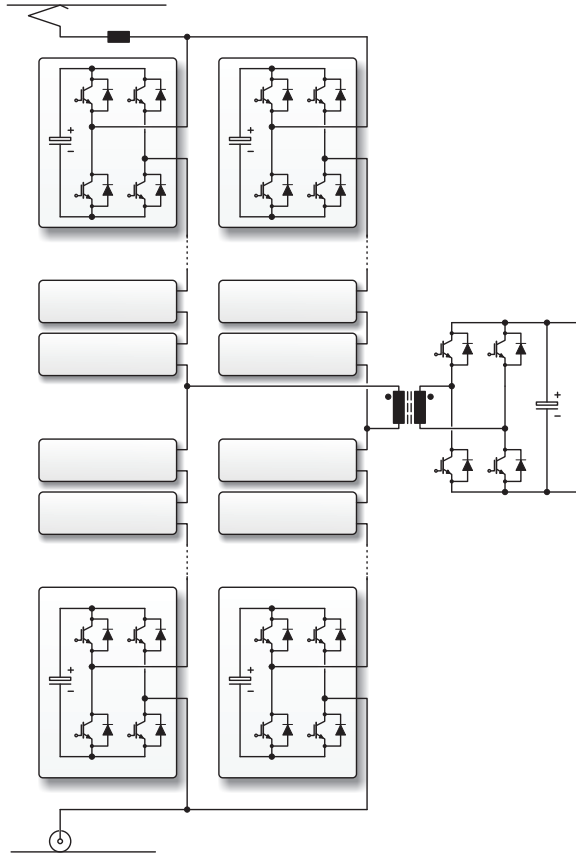
An alternative solution to the ones presented above which preserves the modularity feature and is well suited for connection to the MV grid is represented by the modular-multilevel converter shown in Fig. A.10 as proposed by Marquardt and Glinka in 2003 [130–132]. The cascaded feature of this converter allows to reach high effective frequencies at the input MV side, thus enabling a reduction in the independent cells' switching frequency, increasing the system's efficiency. Moreover, this converter structure offers a large modularity and scalability in its construction but with the price of a large amount of semiconductor devices, which potentially compromises its reliability.





**Figure A.9:** Modular concept with resonant DC-DC converter (as discussed in Chapter 2) utilized in [45, 129].

It should be noted that all the non-resonant topologies presented here operate their DC-DC stages in phase-shift modulation, the same strategy as utilized by McMurray in the seventies [124] whereas the resonant structures utilize the modulation scheme originally studied by the same author [66].



**Figure A.10:** Alternative traction solution with direct AC-AC conversion comprising a modular-multilevel approach [130].

# B

## LF-Isolated and Fractional-Power SST Structures

Besides the MF isolated SST structures presented in Chapter 1, other simplified arrangements based on LF transformers for isolation and step-down have been presented. In the following, a summary of the previously proposed concepts, which can be subdivided into fully-rated and fractional-power concepts, will be shown.

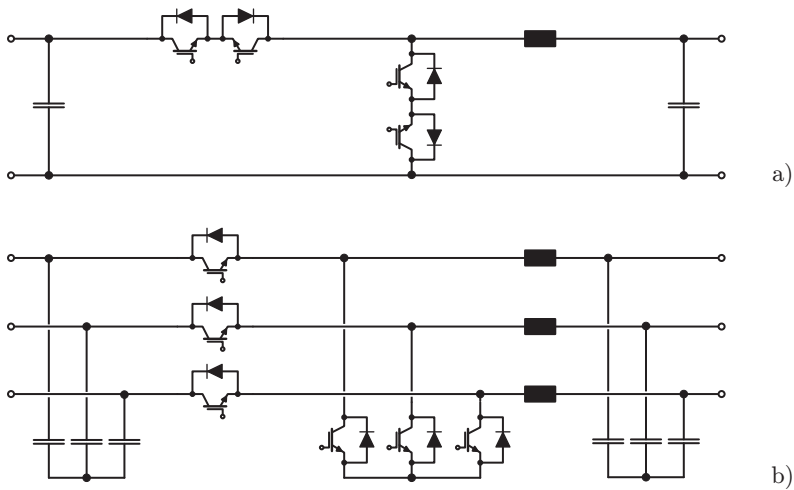
### **B.1 Fully-Rated LF-Isolated Concepts**

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In [5], the term SST was for the first time adopted. Here, a simple single-phase AC chopper utilizing four-quadrant semiconductor switches, as shown in Fig. B.1-a) was proposed. This converter represents the AC version of a standard buck converter, which is a well-known topology for DC-DC conversion. In this case, however, two four-quadrant semiconductors replace the diode and the switch utilized in the standard DC-DC buck converter.

The three-phase counterpart for the single-phase AC chopper topology presented in Fig. B.1-a) was analyzed in [18] and is shown in Fig. B.1-b). In this case, the capacitors and the inductor from Fig. B.1-a) are replaced by three-phase components. In addition, as explained in [18], no four-quadrant switches are required due to the three-phase feature of the system.

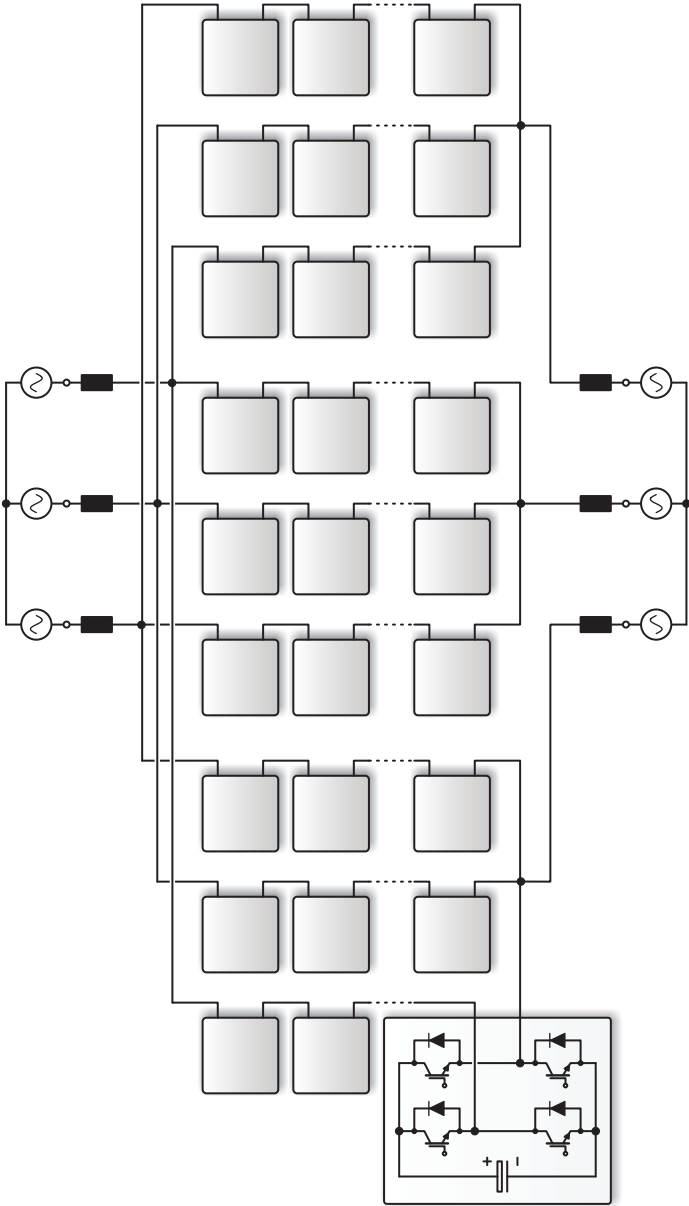
An alternative topology featuring a matrix-type conversion structure for direct three-phase conversion was proposed in [133] and is presented in Fig. B.2. Here, a modular-multilevel structure with indepen-



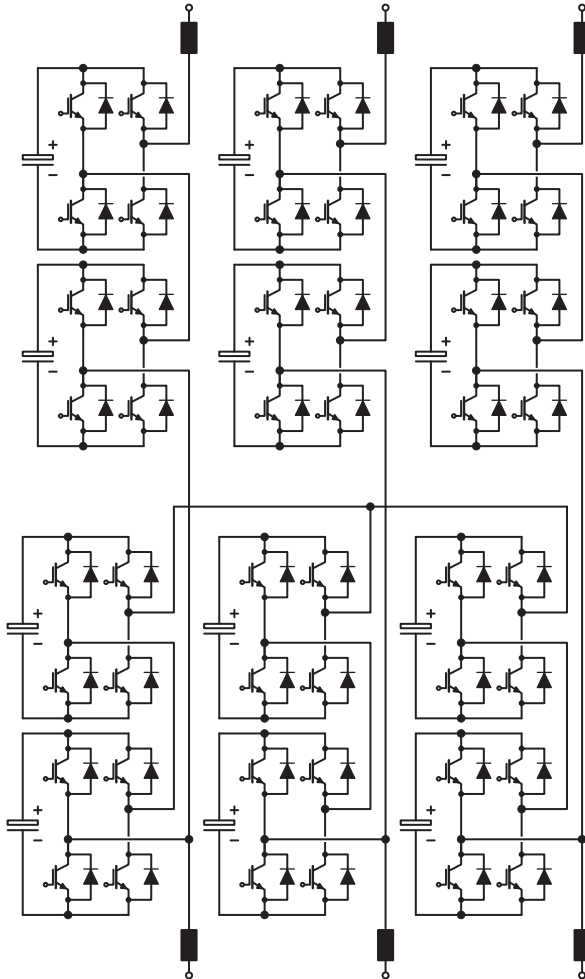
**Figure B.1:** Basic LF-isolated (transformer not shown) AC chopper concepts with AC voltage regulation capability and low sensitivity to grid and load side disturbances. The single-phase version [5] is shown in a) while the three-phase variant [18] is presented in b).

dent and equally-rated converter cells was proposed. As seen in Fig. B.2, three arms for each phase of the input three-phase system are required in order to interface the two three-phase networks, resulting in a large number of modules depending on the specific voltage level. Nevertheless, this converter possess the advantages of modular-multilevel-based converters, which is its modularity and scalability, making it suitable for applications with high grid voltages. It should be noted that this structure is often referred to as cascaded H-bridge converter whereby modular-multilevel represents the most general denomination.

A variation of the three-phase AC-chopper presented in Fig. B.1-b) suitable for higher mains voltages is presented in Fig. B.3. This structure replaces the semiconductor devices by converter modules based on full-bridges, thus enabling a modular/scalable structure.



**Figure B.2:** LF-isolated (transformer not shown) matrix-type modular-multilevel converter for direct AC-AC connection of two networks [133].



**Figure B.3:** LF-isolated (transformer not shown) modular-multilevel concept following the AC chopper structure shown in Fig. B.1-b) suitable for higher grid voltages.

## B.2 Fractional-Power LF-Isolated Concepts

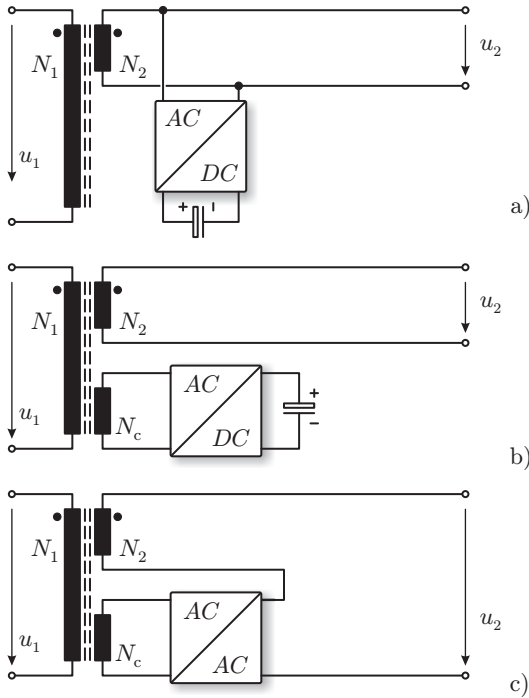
Other SST structures utilizing LF transformers and power electronic converters rated for a fraction of the total output power have been proposed in literature and were summarized in [134]. These structures are presented in Figs. B.4 and B.5. In Fig. B.4-a), an AC-DC converter is added in parallel to the secondary of the LF transformer, providing capability for active filtering and power factor correction. In Fig. B.4-b), the LF transformer has been modified, providing a tertiary winding connected to an AC-DC converter. The advantage with respect to the version in Fig. B.4-a) is the availability of an isolated DC port, which eases the connection to DC loads/sources.

A variation of the structure in Fig. B.4-b) with the possibility of output voltage regulation but losing the availability of a DC port is presented in Fig. B.4-c). Here, a direct AC-AC converter is utilized to process a fraction of the power supplied by the transformer. A circuit implementation of this concept was analyzed in [135] and is shown in Fig. B.6. The AC-AC fractional-power conversion stage consists of the single-phase AC chopper presented in Fig. B.1-a). It should be noted however that this fractional-power SST structure can be coupled with any single-phase AC-AC topology.

The alternative to the fractional-power conversion structure with an AC-AC converter shown in Fig. B.4-c) is represented by the two-stage converter with an intermediate DC-link, providing an isolated DC-port as shown in Fig. B.5-a), easing the integration of renewable energy sources.

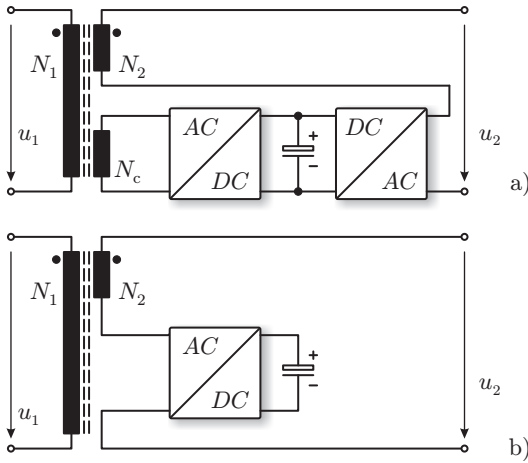
The fractional-power structure presented in Fig. B.5-b) is able to perform power-factor correction and active filtering. In this case, the power electronic converter is connected in series to the transformer secondary winding, providing voltage control capability and limited reactive power compensation capability.

In addition, in [22], a single-phase SST with output voltage regulation was proposed. This structure is presented in Fig. B.7 and consists of a full-bridge AC input stage comprising four-quadrant switches feeding a transformer. The secondary voltage of this transformer is added in series to the input voltage  $u_1$ , thus providing regulation of the output voltage  $u_2$ . The four-quadrant full-bridge operates synchronously with the input voltage, whereby the duty cycle and the phase-shift of this full-bridge is utilized for regulating the output voltage  $u_2$ .

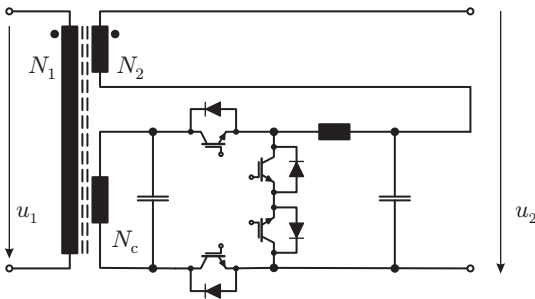


**Figure B.4:** Possibilities for fractional-power SSTs with different combinations of LF transformer and power electronic bridges [134] offering different functionalities: a) Power factor correction and active filtering; b) Power factor correction, active filtering and available isolated LV DC port; c) Output AC voltage regulation. Further structures in Fig B.5.

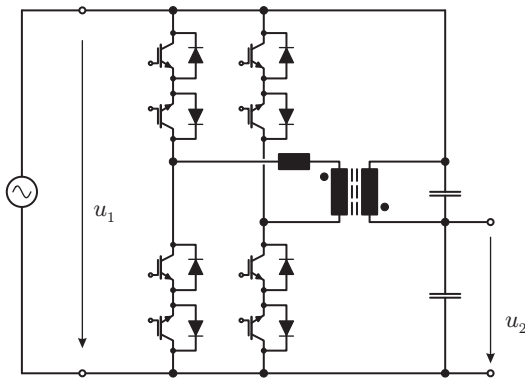




**Figure B.5:** Topologies of fractional-power SSTs with the following functionalities: a) Power factor correction, active-filtering, output AC voltage regulation and available LV DC port; b) Output voltage regulation and limited reactive power compensation. Further structures in Fig B.4.



**Figure B.6:** Fractional-power SST of the type presented in Fig. B.4-c) where the power electronic bridge is of the direct AC-AC type (cf. Fig. B.1).



**Figure B.7:** LF-isolated (transformer not shown) single-phase AC-AC converter with output voltage regulation capability proposed in [22].

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