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Multi-Input Module-Integrated PV Inverter Applying GaN Devices

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Abstract

The trend in small scale roof-top PV-systems is towards module integrated electronics, such as AC-modules, featuring MPP tracking on PV-module level and increasing energy-yield under partial shading conditions. Unlike common AC-modules, this work investigates multi-input AC-modules with MPP-tracking on sub-module level, which eliminates mismatch losses among the substrings of a PV-module.
Based on a review of AC-module topologies with single MPP-tracking, topologies for a multi-input AC-module with substring MPP-tracking are derived. As AC-modules must feature low part-count number due to cost and reliability specifications, the feasible multi-input topologies are severely restricted. A topology comparison identifies two viable candidates for a multi-input AC-module: first a LC-resonant cyclo-converter with a power-balancer multi-port and second a two-stage topology with three paralleled flyback DC-DC converters and a PWM fullbridge DC-AC inverter. The latter is investigated in this work, as it features the advantage of low capacitive energy storage for single-phase power-decoupling.
To perform a model-based optimization of PV-inverters, magnetic models are required, which accurately model the losses over the wide load range of the European efficiency from 100% down to 5% of the nominal output power. To achieve the desired modeling accuracy advanced magnetic models are applied. A new method is proposed to model losses in foil windings exposed to an airgap field, which is not restricted to certain winding geometries. The method is shown to achieve modelling errors below 15%. The transformer parasitics are found to substantially influence DC-DC flyback operation at low output power. Flyback operation under these non-ideal conditions is analyzed, analytical formulas for the involved losses are derived and improved methods to model transformer parasitics are derived.
GaN devices are applied, to allow an AC-module design with decent efficiency. High voltage devices with 600V blocking voltage are still a novelty and not available yet with the voltage and current rating of 600V/2A, typically required for AC-modules. Experimental results

on a 400V/10A halfbridge prototype show, that the switching speed is limited by parasitics of the not yet optimal packaging. Nevertheless excellent switching performance is confirmed with 30μJ total halfbridge switching losses at 400V/4A hard switched operation. This clearly outperforms state of the art silicon devices.
The performance of the proposed AC-module topology is investigated by calculating the volume versus-efficiency pareto-front with model-based optimization. A complete converter optimization routine is implemented, including system-level and component-level parameters. To verify the performed analysis, prototypes of the two AC-module stages are built. The deviation between the modeled and the measured converter losses are below 15%. The complete prototype system achieves an efficiency of η_{EU}=93.45%. This is 0.7% below the actual pareto-optimum, which can only be achieved by applying custom-made core-shapes. To increase the efficiency of the proposed multi-input AC-module above 94.5% an excessive volume of the passive components is required. The major efficiency limitations origin from the transformer-core of the flyback DC-DC stage.
Currently the benchmark efficiency of commercially available AC-modules is 95.5%. Given an estimated yield increase of 1-2% by substring MPP-tracking, the proposed multi-input AC-module only brings a marginal advantage at increased cost and system-complexity, compared to single-input AC-modules. In order to be competitive and exploit the advantage of substring MPP-tracking, the effciency of multi-input AC-modules must improve well above the level achieved with the investigated two-stage topology. Applying the alternative LC-resonant cycloconverter topology with a power-balancer multi-port would be one option to realize a multi-input AC-module with higher efficiency.

Kurzfassung

Im Bereich kleiner PV-Anlagen für Aufdach-Montage geht der Trend in Richtung modul-integrierte Elektronik wie z.B. AC-Module. Modul-integrierte Elektronik bietet den Vorteil von separatem MPP-Tracking für jedes PV-Modul und erhöht den Energieertrag bei Teilverschattung der PV-Anlage. Im Gegensatz zu herkömmlichen AC-Modulen werden in dieser Arbeit 'Multi-Input AC-Module' mit MPP-Tracking auf Substring-Ebene untersucht. Dies verhindert Verluste bei Teilverschattung des PV-Moduls und erhöht den Energieertrag.
Gestützt auf einen Topologievergleich herkömmlicher AC-Module werden verschiedene Topologie-Varianten zur Realsierung eines 'Multi-Input AC-Moduls' vorgestellt und untersucht. Aufgrund hoher Kosten- und Zuverlässigkeitsanforderungen müssen AC-Module mit einer möglichst kleinen Anzahl von Komponenten gebaut werden. Dies schränkt die möglichen Topologien stark ein. Ein systematischer Topologievergleich zeigt zwei valable Topologien zur Realisierung eines 'Multi-Input AC-Moduls' auf: erstens ein LC-resonanter Cyclo-Umrichter kombiniert mit einem 'Multi-Port Power-Balancer' und zweitens eine zweistufige Topologie mit drei parallelgeschalteten Flyback DC-DC Umrichtern und einer DC-AC Vollbrücke. In diser Arbeit wird die zweistufige Topologie untersucht, da sie zur einphasen Leistungsentkopplung eine viel kleinere Energiezwischenspeicherung benötigt.
Für die korrekte Modellierung von Verlusten in PV-Umrichtern werden Modelle benötigt, welche die Verluste über den gesamten, weiten Lastbereich von PV-Umrichtern korrekt modellieren können. Deshalb werden in dieser Arbeit verbesserte Methoden zur Modellierung magnetischer Komponten hergeleitet. Eine neue Methode zur Berechnung von Verlusten in Folienwicklungen mit Luftspaltstreufeld wird vorgestellt, welche auf beliebige Wickelanordnungen anwendbar ist. Die Genauigkeit der Methode wird anhand von Messungen an Prototyp-Transformatoren bestätigt. Der Fehler der modellierten Verluste ist kleiner als 15%.
Der Betrieb des DC-DC Flyback Umrichters wird bei tiefen Leistungen stark von den parasitären Elementen des Flyback-Transformators beeinträchtigt. Das Betriebsverhalten des Flyback Umrichters unter

diesen nicht-idealen Bedingungen wird im Detail analysiert. Analytische Formeln zur Berechnung der durch die parasitären Elemente verursachten Verluste werden hergeleitet. Zudem werden Methoden zur Modellierung der parasitären Elemente eines Transformators behandelt.
Um eine hohe Umrichtereffizienz zu erreichen, werden neuartige GaN Halbleiter eingestzt. GaN Schalter mit 600V Sperrspannung sind neu auf dem Markt und noch nicht in der für AC-Module benötigten 600V/2A Ausführung erhältlich. Ein 400V/10A Halbbrücken-Prototyp zeigt auf, dass die Schaltgeschwindigkeit im realen Betrieb durch parasitäre Induktivitäten des nicht optimalen Halbleiter-Packages limitiert ist. Trotzdem bestätigen Schaltverlustmessungen die hervoragenden Schalteigenschaften der GaN Schalter mit gerade mal 30μJ Halbbrückenschaltverluste bei 400V/4A hart geschaltetem Betrieb.
Mittels modelbasierter Optimierung wird die Effizienz versus Bauvolumen Pareto-Front der untersuchten 'Multi-Inpt AC-Modul' Topologie berechnet. Ein Prototypen-Aufbau bestätigt die Gültigkeit der Optimierung mit Abweichungen kleiner 15% zwischen den modellierten und gemessenen Umrichterverlusten. Der Prototyp erreicht eine Effizienz von η_{EU}=93.45%. Diese liegt 0.7% unter der pareto-optimalen Effizienz, welche nur durch Verwendung von massgefertigten magnetischen Kernen erreicht werden kann. Mit der untersuchten Topologie kann realistischerweise eine Effizienz von η_{EU}=94.5% erreicht werden. Eine weitere Effizienzsteigerung würde eine unverhältnismässige Vergrösserung des Bauvolumens erfordern. Die Effizienz des Gesamtsystems ist hauptsächlich durch den Transformator des DC-DC Flyback Umrichters limitiert, welcher die grössten Verluste beisteuert.
Herkömmliche, kommerziell erhältliche AC-Module weisen eine Efffizienz von 95.5% auf. Durch MPP-Tracking auf Substring-Ebene lässt sich der Energieertrag um 1-2% steigern. Das untersuchte 'Multi-Input AC-Modul' bringt daher nur einen marginal höheren Nettoertrag als herkömmliche AC-Module bei zugleich erhöhter System-Komplexität und höheren Herstellungskosten. Um den Vorteil des erhöhten Energieertrages ausnutzen zu können, muss die Effizienz von 'Multi-Input AC-Modulen' deutlich gesteigert werden. Die Verwendung der LC-resonanz Cyclo-Umrichter Topologie kombiniert mit einem 'Multi-Port Power-Balancer' wäre eine mögliche Alternative um dies zu erreichen.

Glosary

2D	...	Two Dimensional
2DEG	...	Two-Dimensional Electron Gas
3D	...	Three Dimensional
AC	...	Alternating Current
ADC	...	Analog to Digital Converter
BCM	...	Boundary Conduction Mode
BOS	...	Balance of System
CCM	...	Continuous Conduction Mode
DAB	...	Dual Active Bridge
DC	...	Direct Current
DCM	...	Discontinuous Conduction Mode
DUT	...	Device Under Test
DSP	...	Digital Signal Processor
ESL	...	Equivalent Series Inductance
ESR	...	Equivalent Series Resistanc
FEM	...	Finite Element Method
FET	...	Field Effect Transistor
FPGA	...	Field Programmable Gate Array
GA	...	Genetic Algorithm
GaN	...	Gallium Nitride
GSE	...	Generalized Steinmetz Equation
HEMT	...	High Electron Mobility Transistor
HF	...	High Frequency
HV	...	Low Voltage
IC	...	Integrated Circuit
IGBT	...	Insulated Gate Bipolar Transistor
iGSE	...	improved Generalized Steinmetz Equation
MF	...	Medium Frequency
MOSFET	...	Metal Oxide Field Effect Transistor
MPP	...	Maximum Power Point
MPPT	...	Maximum Power Point Tracking

MV	...	Medium Voltage
NDA	...	Non-Disclosure Agreement
NPT	...	Non Punch Through
LF	...	Low Frequency
LP	...	Low Profile
LV	...	Low Voltage
PCB	...	Printed Circuit Board
PV	...	Photovoltaic
PWM	...	Pulse Width Modulation
RMS	...	Root Mean Square
SRC	...	Series Resonant Converter
SiC	...	Silicon Carbide
TCM	...	Triangular Current Mode
THD	...	Total Harmonic Distortion
WBG	...	Wide Band-Gap
ZCS	...	Zero-Current Switching
ZVS	...	Zero-Voltage Switching

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1 Introduction

In spite of falling prices of fossil energy sources, renewable energy sources continue to grow. With the steady increase of installed capacity over the last ten years renewable energy is becoming significant in terms of produced energy. For instance in Germany renewable energy reached 38% of the total electric power consumption in 2015 [2]. For the first time over four decades global carbon emission stabilized in 2014, despite a global grow of the energy demand of 1.5% [1]. Even though renewable energy is gaining impact, the grow-rates are substantially

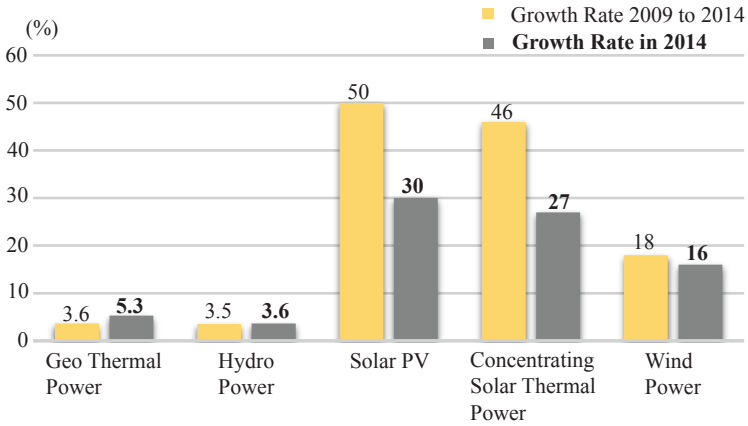


Figure 1.1: Average Annual Global Growth Rates of Renewable Energy Capacity, End 2009-2014, data published by REN21 [1]

below the projected scenarios to mitigate climate change [2],[3]. Not all renewable energy sources grow the same, as illustrated in fig. 1.1. The increase in capacity is mainly based on photovoltaics (PV), wind and hydro power. PV still is the leader in annual global growth rate, with an increase of 30% and a total global installed capacity of 177 Gigawatts in 2014, [1]. While PV is growing with record growth rates in Asia, growth slowed down in Europe due to changes in policy support and reduced financial incentives. These more market-based mechanism rely on a continuing price decay of PV-systems to increase the installed capacity. Thanks to the technology learning curve and economy of scale, average PV-module prices fall year-over-year by 10-15% and PV-generated electricity becomes competitive to conventional energy sources in more and more countries [1]. With the dropped prices for PV-modules, the balance of system (BOS) costs account for an increasing share of the total system costs [4]. Included in the BOS costs, the applied power electronic converters (PV-converter) contribute twofold to the costs. Firstly the actual converter price adds directly to the costs. Secondly the PV-converter determines the structure of the PV-system, which influences the system-installation costs. For a further progress of the well advanced PV-converter technology price-reduction and performance increase of the PV-converter itself is not the only criteria. Converter concepts, which allow to reduce the whole BOS costs will gain more importance.

1.1 Photovoltaics

Based on the photovoltaic effect in semiconductor pn-junctions, PV-cells generate electric energy upon exposure to light [5]. PV-cells can be made from several semiconductor materials, whereas mono-crystalline and poly-crystalline silicon are the most used materials.

Electrically, PV-cells behave as a source with the characteristic I-V curve shown in figure 1.2 a). When shorted, the PV-cell delivers its maximal current I_{sc}. The maximal voltage V_{oc} is achieved in open-circuit mode. At (V_{MPP},I_{MPP}) the power delivered by the PV-cell reaches its maximum, called the maximal power point (MPP). Typical crystalline silicon PV-cells exhibit a surface of 1dm^2 and an open-circuit voltage V_{oc} of ca. 0.6V [5]. To enhance the operating voltage of the interfacing device, PV-cells are connected in series and packaged to a PV-module. A module typically consists of 72 PV-cells exhibiting an

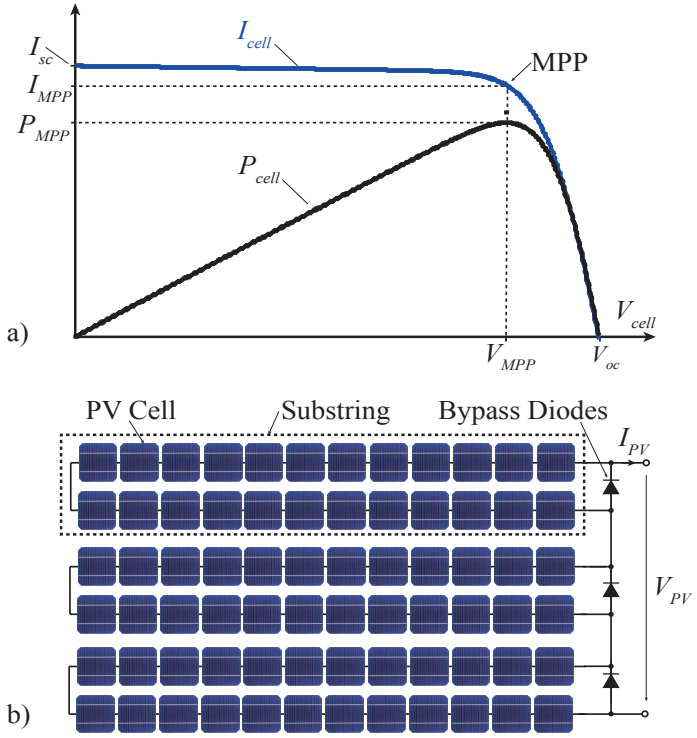


Figure 1.2: a) Characteristic I-V curve of a practical PV-cell at a given irradiation and temperature, b) PV-module schematic structure

MPP voltage in the range between 30V to 40V, as shown in fig. 1.2 b). In case of a current mismatch among the series connected cells, e.g. due to partial shading, losses are caused in the cells with a lower generated current. The surplus current, exceeding the current generated by the PV-cell, leads to resistive losses in the cell [6] and causes a negative PV-cell voltage. To protect these cells from overheating and breakdown due to negative over-voltage, the maximally possible current mismatch is kept low by limiting the number of series-connected PV-cells. Therefore the PV-cells in a PV-module are typically grouped in three substrings each equipped with a bypass-diode. The PV-modules are operated with

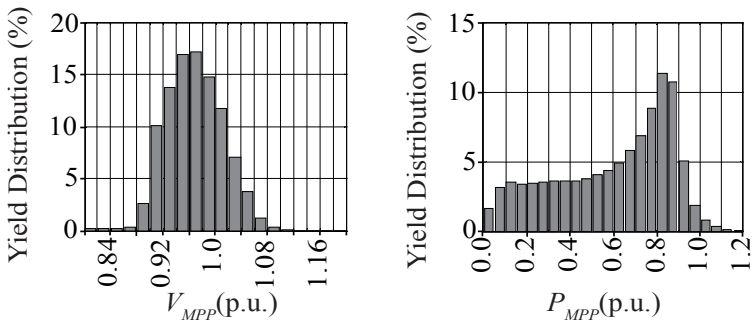


Figure 1.3: Distribution of the annual yield as a function of MPP voltage and MPP power, measurements from Burgdorf Switzerland published by B. Bletterie et al. [7]

power electronic converters (PV-converter), which extract the maximal power from the PV-module by regulating the module voltage to V_{MPP}.

The I-V curve (see fig. 1.2 a), and hence also the MPP, is not a constant characteristic of the PV-cell, but depends on the irradiation and the temperature of the PV-cell [5]. The exact operation characteristic of a PV-cell is determined by the PV-cell parameters, the geographic location and the mechanical installation of the cell. Figure 1.3 shows the variations of the MPP in relation to the annual yield for a PV-module installed in Burgdorf, Switzerland investigated by B. Bletterie et al. [7]. To track the variations of V_{MPP} by up to 40%, the PV-converter must feature a wide input-voltage range and a control algorithm to detect the MPP, so called MPP tracker (MPPT) [8],[9]. The maximal power P_{MPP} varies in an even bigger range, while a remarkable share of the annual yield is delivered at low P_{MPP}. PV-converters must therefore operate under a wide load-range and exhibit decent efficiency over the whole load-range. To account for this wide load-range, the efficiency of PV-converters is characterized by the European efficiency η_{EU}. It weights the efficiencies from 5% to 100% of the nominal load power according to a standardized European irradiation scenario [7]. Similarly η_{CEC} is a PV-converter efficiency for US south-west insolation, defined by the California Energy Commission.

PV-converters, as any switched mode power converters, exhibit a certain voltage-ripple on their input and output. The MPP of a PV-module is sensitive to such a ripple $\Delta_{V_{PV}}$. As shown in fig. 1.4, the

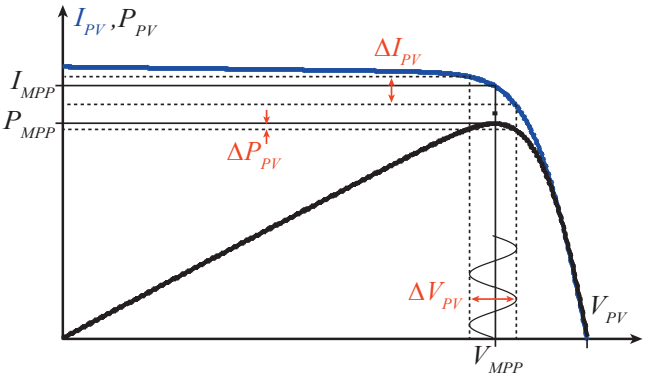


Figure 1.4: MPP tracking of a PV-module: sensitivity of harvested power p_{PV} on the voltage ripple $\Delta_{V_{PV}}$

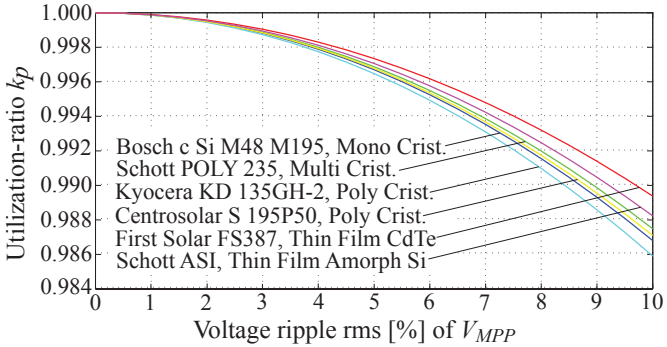


Figure 1.5: Degradation of harvested power in dependence of voltage-ripple rms $\Delta_{V_{PV},rms}$

operating point is shifted away from the MPP and a fluctuating power $p_{PV}(t)$ results. The average power extracted from the PV-module $\overline{P}_{PV}$ is lower than P_{MPP}. The yield is reduced by $\Delta_{P_{yield}}$=P_{MPP}-$\overline{P}_{PV}$, which can also be expressed as the utilization ratio $k_p = \overline{P}_{PV}/P_{MPP}$. The yield reduction depends on the voltage ripple as well as PV-module specific parameters and can be estimated with the analytical formula proposed in [10]. Figure 1.5 shows the utilization ratio as a function of $\Delta_{V_{PV}}$ calculated for several types of modules. In order not to sub-

stantially degrade the energy yield, PV-converters must feature low input-voltage ripples in the range of 4%.
Besides the described basic operational requirements resulting from the interaction of the PV-converter and the PV-module, PV-converters must fulfill regulations regarding safety and power-quality, as e.g. the norms EN 62109-1/2 and IEC 61727.

A practical grid-connected PV-system consists of several PV-modules and one or more PV-converters. Such a system can be realized in several ways. The following system concepts can be distinguished [11].
The centralized converter approach consists of one single DC-AC inverter interfacing a large number of PV-modules, see fig. 1.6 a). The modules are grouped in series connected strings to reach a sufficient voltage-level for three-phase grid-connection. The power is scaled-up by paralleling several strings, each protected by a string-diode. The string-converter concept shown in fig. 1.6 b) applies a separate DC-AC inverter for each string. This brings along the following advantages. MPP-tracking is performed on string-level. The string diodes, causing system losses, can be removed. A more flexible system design is possible, allowing for easy scale up and the application of different types of PV-modules. A similar approach is the multi-string concept shown in fig. 1.6 c). It applies separate DC-DC converters for each string and one centralized DC-AC inverter. It features the advantage of a more flexible string-input voltage range, a lower voltage-rating of the DC-AC inverter stage and easy enlargement of the system not affecting the grid-interface. Though it comes along with higher conduction losses due to the two converter stages. The discussed system concepts only track the MPP on string- or on system-level, causing reduced energy yield, if some PV-modules within a string are shaded [12]. There are three concepts overcoming this drawback by MPP tracking on module-level. Firstly the DC-module concept shown fig. 1.6 d), which applies a DC-DC converter integrated in each PV-module (DC-module) in combination with one DC-AC inverter. Most DC-modules are made for series connection in a string [13]. Secondly the AC-string concept shown in fig. 1.6 e), which is also known as 'Ultraverter-System' introduced by KACO new energy. This concept applies buck-type DC-AC converters integrated in each PV-module. The DC-AC converters are series connected to a string to achieve the grid-voltage level. An AC-combiner box for grid-connection provides the required safety functionalities and monitors the DC-AC converters. Thirdly PV-module integrated AC-

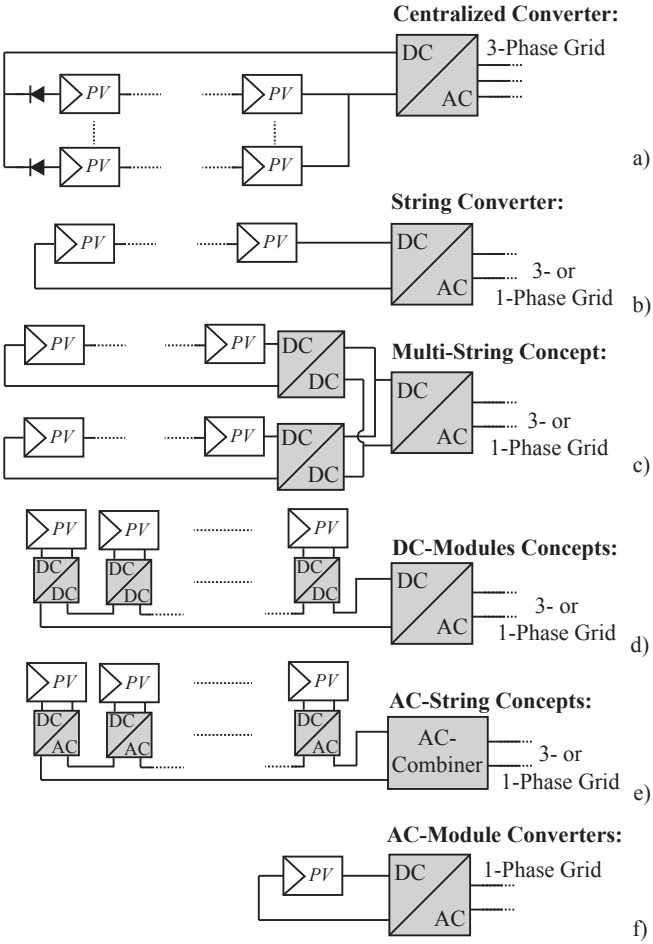


Figure 1.6: Categorization of PV-system concepts according to [11]: a) Centralized converter, b) String converter, c) Multi-string converter, d) DC-module concept, e) AC-String concept (proposed by KACO new energy) f) AC-module converter

converters (AC-modules), which provide a separate grid-connection for each PV-module, as shown in fig. 1.6 f). As for the string-converters the DC-module concept and the AC-string concept are constrained to

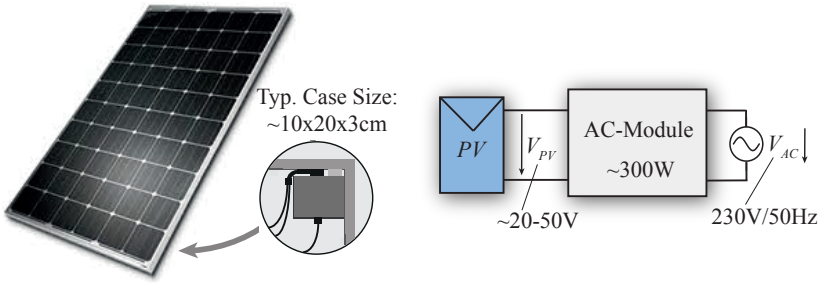


Figure 1.7: AC-Module: Mounting and Schematic

a certain string voltage-level. Further, the DC-module concept relies on DC-cabling of the PV-modules. In contrary the AC-module concept is fully modular with each AC-module independently providing plug & play functionality.
Whereas large scale commercial PV-systems are still designed using centralized or string converters, for smaller scale roof-top systems a trend towards module-integrated electronics can be observed. For these systems not only increased yield due to module-level MPP tracking, but also additional advantages such as reduced installation cost and safety issues become equally important [13], [14].

1.2 AC-Modules

Module integrated AC converters connect each PV-module separately to the single-phase grid, providing an autonomous DC-AC converter for each PV-module illustrated in fig. 1.7. The converters, designed with an appropriate low-profile housing, are mounted directly on the back-side of each PV-module.

First research on AC-module converters dates back to the late eighties [15], which led to several commercial products. Even though widely applied during the nineties, AC-modules disappeared from the market due to their high cost and issues with high failure rates [14]. However starting around 2007 AC-modules were reintroduced into the market, with technological advancements allowing to overcome the major issues of the first-generation of AC-module converters. Since then several companies emerged on the market. In parallel this triggered a still ongoing research effort to continuously improve the AC-module technology.

Compared to string-converters, AC-modules feature various benefits [14]:

- *Modularity:* The PV-system simply consists of paralleled AC-modules. It can be easily scaled up without any constraint on a certain type of PV-module.
- *Module-Level MPP-Tracking:* The MPP of each PV-module is tracked independently, eliminating mismatch losses on string-level and increasing the energy-yield
- *Installation-Effort:* The PV-system requires only a simple system-design and can be installed with standard AC-cabling. This reduces installation costs.
- *Safety of Installation:* The DC-bus needed for the installation of string-converters can cause harm to humans, for example when trying to extinct a possible fire. AC-module PV-systems, based on AC-cabling, do not have these safety issues.
- *Total System Reliability:* The risk of a total system failure, is reduced much. Thanks to the modularity and parallel operation of the AC-modules, the system does not have a single point of failure, as a string-inverter system.
- *Monitoring and Failure Detection:* The system performance can be monitored down to PV-module level, facilitating failure detection,

Unfortunately, these benefits do not come for free. AC-module converters also exhibit some inherent drawbacks compared to string- and multi-string converters and must compete against these system concepts. When designing PV-systems, the optimal system-concept follows from a variety of criteria finally reflecting the total cost of ownership. Even though these criteria depend much on the specific PV-system, it is evident, that for a PV-converter cost, efficiency and lifetime are the key factors to succeed. For the design of a competitive AC-module, the following challenges persist:

- The AC-module forms a functional unit with the PV-module, requiring a similar lifetime of 20 years. At the same time the AC-module is exposed to the same harsh environmental conditions as the PV-module with ambient temperatures from -20°C

to +50°C and daily temperature cycles. To meet these extreme requirements AC-modules must be designed with low part-count number and an optimized thermal design [14].

- Unlike the string-converters, the AC-module must step-up the voltage of one single PV-module to the grid-level. Depending on the operating point, the voltage step-up ratio is higher than 1:15. The high step-up ratio comes at the expense of increased converter losses and is a substantial drawback compared to high efficient transformerless string-converters.

- The power transferred to a single-phase grid is not continuous, but is pulsating with twice the line-frequency. The AC-module must temporarily buffer the energy to decouple the DC-power delivered by the PV-module from the grid-side. Electrolytic capacitors, which are usually applied, exhibit accelerated aging-effects under the given harsh environmental conditions (see appendix C.1). A careful thermal design and derating of the capacitors is required to achieve the targeted lifetime.

- Due to the higher number of converters, AC-module PV-systems have a much bigger overhead of control- and auxiliary electronics, such as micro-controllers and gate-drives. This cost-drawback can only be overcome by minimizing the part-count of the converters and by mass production of AC-modules, such that the economy of scale applies.

- Possible failure of communication interface. Despite its modularity, a PV-system consisting of AC-modules needs a communication interface to each AC-module to allow for emergency shutdown and monitoring. The communication interface is safety relevant and must feature high reliability.

For these reason the design of a competitive AC-module is still very challenging. A multitude of approaches are proposed in literature all of them aiming for the optimal trade-off of the mentioned issues [11],[16],[17]. Currently, the commercial AC-modules achieve weighted efficiencies up to η_{EU}=95.5% and peak efficiencies slightly above 96%. The record efficiency for a commercial AC-module is achieved for the North American grid and is claimed to be η_{CEC}=97% (Enphase S280). The AC-modules come with a life-time warranty of 15 to 25 years.

Though the long life-time is yet to be proven by field-data in the coming years.

While lifetime seems to have achieved a satisfactory level, AC-module technology must further catch up to the competing string converters regarding costs and efficiency. Another approach to make AC-modules more competitive is to strengthen their advantages concerning energy yield. Even with module-level MPP tracking mismatch losses still persist on submodule-level under partial shading of the PV-module. Taking the MPP tracking from module to submodule level can recover parts of these losses. To fully eliminate mismatch losses MPP-tracking would have to be performed on PV-cell level, which requires modifications of the PV-module structure and manufacturing process. Alternatively, standard PV-modules easily allow for MPP-tracking on substring-level (see fig. 1.2 b). The bypass diodes contained in a junction-box on the back-side of the module, can simply be replaced by an AC-module with three substring-level inputs.
Multi-input AC-modules with MPP-tracking on substring-level are, for the time being, the most effective way to further reduce mismatch losses of standard PV-modules. The potential gain in annual energy yield for substring MPP-tracking is reported to be 1% for moderate and 2% for heavy shading conditions [18]. The instantaneous energy yield increase can be as high as 20% [19].

1.2.1 AC-Module with Substring-Level MPP Tracking

To further push forward the AC-module technology, this work investigates the concept of substring-level MPP tracking for AC-modules. The resulting multi-input AC-module is schematically shown in fig. 1.8.

The multi-input AC-module is specified for 230V/50Hz grid connection and a substring voltage range of 8V to 21V for standard mono- and multi-crystalline silicon PV-modules. Besides the general power quality standards in table 1.2 the AC-module shall be able to deliver reactive power, allowing to scale up the PV-system to high power levels. Even if not required by the standards, galvanic isolation is defined as mandatory. The housing of the AC-module must feature a low profile with a maximal height of 30mm. The complete system specification is listed in table 1.1. Generally the multi-input AC-module must fulfill the same

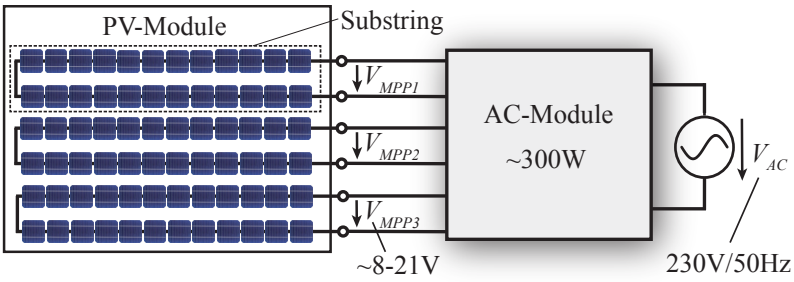


Figure 1.8: Multi-input AC-module with substring MPP-tracking

Table 1.1: Multi-input AC-module system specifications.

PV Interface	Power:	P_{Nom}=300W, $P_{Op,min}$=9W
	MPP-Tracking:	3xMPPT on substring level
	MPPT Range:	$V_{PV,MPP}$=3x8.5-21V
	Open Circuit Voltage/substring:	V_{oc}=21V
	Short Circuit Current/substring:	I_{sc}=10A
	Input Voltage Ripple:	$k_{PV,Europ} \geq$0.998
Grid Interface	Line Voltage:	V_{line}=207-253Vrms, THD_{max}=8%
	Line Frequency:	f_{line}=45-65Hz
	Line Current:	THD_{max}=4%, norms see table 1.2
	DC-Current Injection:	$I_{DC,max}$=0.01I_{rms}=11.3mA
	Reactive Power Support:	Up to power factor 0.9
General	Operable Temperature:	-40°C to +85°C
	Lifetime:	25 years
	Galvanic Isolation:	Required
	Volume and Dimension:	PCB-size max: 160x100mm PCB-height max: 30mm Component-height max: 25mm
Safety	Grounding:	equipment ground
	Anti Islanding:	VDE 0126-1-1, IEC 62116
	Line deviations:	see norms table 1.2

norms as the normal AC-modules, listed in table 1.2.

Table 1.2: List of standards relevant for the AC-Module Inverters [5].

Category	Standard	Description
General	DIN EN 50522	Ambient temperature range
Power Quality	EN 50160	Public distribution voltage quality
	EN 61000-3-2	Current Harmonic limits (I_{line} $\leq$16A)
	EN 61000-6-3:2007 EN 61000-6-2:2005	EMC (high frequency distortion) residential and industrial respectively
	VDE-AR-N 4105	Generators connected to LV grid
	IEC 61727	Characterization of PV-utility interface
Safety	EN 62109-1/2	Safety of converters in PV-systems
	IEC 62116	Anti islanding prevention measures
	VDE 0126-1-1	Line supervision, PV-specific

1.3 Objective and Contributions

The objective of this thesis is to investigate the concept of multi-input AC-modules with substring-level MPP-tracking. Different concepts to realize such a converter are derived and the most promising approach is identified. Compared to AC-modules with module-level MPP-tracking, multi-input AC-modules exhibit the drawback of higher system complexity and a lower input-voltage range, possibly leading to a lower system efficiency. Nevertheless multi-input AC-modules must compete with their single-input counter parts, regarding cost and efficiency. As a prerequisite to be competitive, multi-input AC-modules must feature a sufficiently high efficiency, such that the net energy yield is higher than for single-input AC-modules. Therefore, a main goal is to investigate the achievable system-efficiency of multi-input AC-modules in dependence of the converter volume. The performance limits are investigated by model-based optimizations of the converter system. To enable an increased system efficiency, novel, high efficient GaN devices are applied.

In the following the main contributions of this thesis are summarized. Parts of this work, including text, tables and figures have been previously published in international journals and conference proceedings. The according publication list can be found at the end of the thesis.

- *Multi-Input AC-Module Concepts and Topologies*: In literature

there are numerous publications dealing with AC-module topologies, all of them considering single-input AC-modules. This thesis systematically derives and categorizes the different system-concepts for multi-input AC-modules. Among the proposed AC-module topologies, a comprehensive topology comparison is performed to identify the most favorable topologies. For the selected multi-input topology, a complete model-based optimization is performed and a prototype is built, to demonstrate and analyze its performance.

- *Advanced Magnetic Models*: Model-based optimization of low-power PV-converters requires magnetic models, that accurately predict the losses not only at nominal power, but also at low output-power where parasitic effects are shown to become relevant. To model the leakage inductance of transformers an improved method is developed, which more accurately considers the frequency-dependence of the leakage inductance. In addition for the loss calculation of foil windings exposed to an airgap fringing field, a new method is proposed. Unlike the existing methods, it is applicable to arbitrary winding arrangements. Based on a semi-numerical field calculation, it features low computational effort suitable for model-based optimization of magnetic components.

- *GaN-Devices for Low Power Grid-Tied PV-Application*: GaN devices with 600V blocking voltage are still a novelty. In this thesis 600V rated devices are applied for interfacing the grid for a low-power PV-application. A feasible layout and gate-drive design for high-speed switching is developed and tested with a 400V/10A halfbridge demonstrator. The performance of the GaN devices is investigated by switching loss-measurements. It becomes evident that these devices clearly outperform the state of the art silicon-devices. A high efficiency fullbridge DC-AC inverter is designed by model-based optimization. The built prototype achieves a peak efficiency of 98.9% at 300W output-power and 400Vdc to 230V/50Hz AC-voltage.

- *High Efficiency High Step-Up Flyback DC-DC Converter*: Even though the flyback-converter is commonly applied for PV applications, most designs neglect the influence of the parasitic elements. In this work, the parasitic elements of the transformer are found to have a considerable influence on the converter operation and

losses at low output-power. An in-depth analysis of this non-ideal flyback-converter operation is given and formulas are derived to calculate the losses caused by the parasitic elements. A detailed converter loss model considering the parasitic elements is implemented and a model-based optimization for a high step-up DC-DC flyback converter is performed. Based on the optimization results, the efficiency versus volume limits are analyzed and discussed. The built prototype confirms the accuracy of the applied models and routines.

1.4 Outline

This thesis deals with the design and development of multi-input AC-modules with substring-level MPP-tracking.
The following **Chapter 2** derives topologies for multi-input AC-modules. First a detailed review of single-input AC-modules is performed. A comparison of the various topologies helps to identify the most promising system-concepts. Based on this insight, approaches for multi-input AC-modules are derived and different multi-input AC-module topologies are proposed. Among them the most promising topology is selected, based on a topology comparison.
Improved magnetic models required to accurately model the losses of PV-converters over the whole load-range, are given in **Chapter 3** . A new method is proposed, which accurately models losses in foil windings exposed to an airgap fringing field. Methods to model parasitic elements in magnetic components are discussed.
GaN devices exhibit unprecedented switching performance and allow to improved performance of AC-module converters currently built with MOSFETs. The status of these new devices is discussed in **Chapter 4**. The performance of 650V GaN devices is characterized by experimental results on a 400V/10A halfbridge demonstrator.
To perform a complete optimization of the AC-module, detailed loss models are derived in **Chapter 5**. Based on the calculated volume versus efficiency, η-ρ, pareto-front, the performance of the proposed AC-module is analyzed.
The model-based performance study is verified by a prototype system, described in **Chapter 6**. The design and the practical setup of the multi-input AC-module prototype is discussed and experimental results are given.

In **Chapter 7**, the last chapter of this thesis, the major findings are summarized, a final conclusion is drawn and an outlook on possible future work is given.

2

AC-Module Topologies - from Single to Multiple Inputs

Through the past decade various manufacturers of AC-modules entered the market. Besides that, noticeable research is going on at different research institutes and companies. This section discusses the various system concepts and topologies applied for AC-module converters. To begin with a categorization scheme for AC-module topologies is defined. The multitude of single-input topologies proposed in literature are reviewed and a comparison is performed to identify the most promising system concepts. Based on the insight derived from the single-input topologies, multi-input AC-module topologies are derived and compared. Finally the proposed multi-input topology is explained in detail.

2.1 Categorization of Power Decoupling for Single-Phase Grid Connection

It is an inherent characteristic of single phase grid connection, that the power flow from/to the grid is pulsating with twice the line frequency. A PV-module in contrary is a DC-source delivering a constant power (given constant radiation and temperature). Further the voltage at the PV-module output V_{PV} should be kept at a constant value to guarantee maximum power point tracking (MPPT). To match the constant input power to the pulsating output power, the AC-module must provide power decoupling by means of temporary energy storage. Figure 2.1 shows the categorization of the different ways of power decoupling in an AC-module. It is distinguished between the locations, where the

decoupling can be placed: at the PV-input side, integrated into one of the power processing stages of the AC-module and at the intermediate DC-link between two power processing stages. The decoupling methods are split into passive and active decoupling and will be explained in the following subsections.

Passive Decoupling

Passive decoupling is achieved by applying a sufficiently large capacitor either at the PV-input side or at an intermediate DC-link. Passive decoupling at the PV-input side (V_{PV}=30-60V) typically requires a large capacitance value in the range of 2-10mF (P_{Nom} up to 250W), because only a very small ripple is acceptable in order not to compromise MPPT. Such large capacitance values must be realized with electrolytic capacitors. Film-capacitors would lead to an excessive volume. If the topology has any, it is favorable to realize the passive decoupling at the intermediate DC-link for the following reasons:

- A ripple of up to 25% is acceptable in the intermediate DC-link if a special control of the DC-AC inverter is applied. This greatly reduces the stored energy. A capacitance value in the a range of 50μF-100μF is sufficient, which could also be realized with film capacitors [20].
- The higher voltage reduces the ripple current through the capacitor, compared to PV-side decoupling. This results in lower ESR-losses and thus lower self heating of the capacitor [21].

Active Decoupling

Active decoupling is achieved by incorporating a decoupling stage. The decoupling stage has a capacitor as energy storage element, whose power-flow is actively controlled. The energy storage could also be realized with an inductor, however these solution was not found in any topology proposed in literature and will not be considered here. Three basic types of power decoupling can be distinguished:

Serial active decoupling: Power decoupling is realized by a stage, which is in series with the other converter stages of the AC-module. The whole power from the PV-module flows through the decoupling stage, before it is transferred to the AC-side.

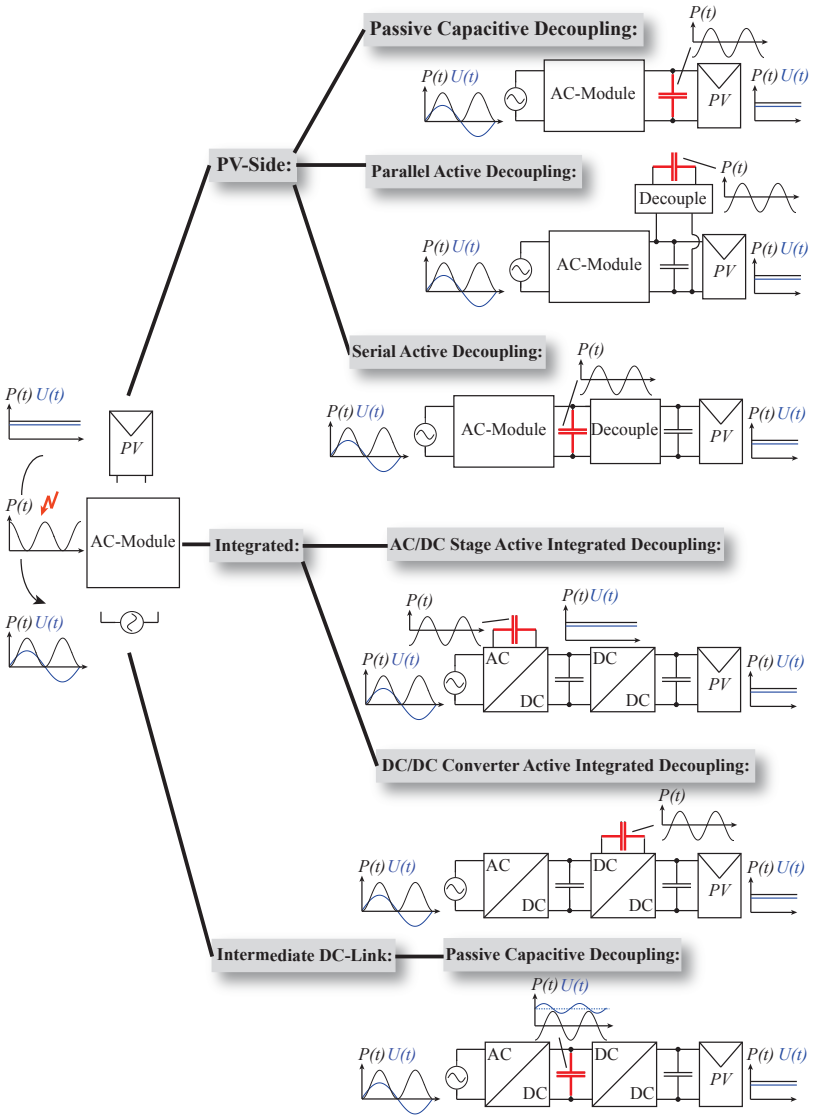


Figure 2.1: Categorization of power decoupling methods for single phase AC-modules.

Parallel active decoupling: The decoupling stage is in parallel to the other converter stages. Only the excess power is buffered in the decoupling capacitor. The main share of the power is transferred directly from PV-input to AC-side.

Active integrated decoupling: The decoupling stage is integrated in one of the conversion stages of the AC-module by means of a three-port inverter. In the same way as for parallel decoupling, only the excess power is buffered in the decoupling capacitor and the main share of the power is transferred directly from PV-input to AC-side. However, unlike for parallel decoupling, the energy stored in the power-decoupling capacitor is directly fed into the next power processing stage of the AC-module. Thus one processing stage can be avoided, when the energy buffered in the decoupling capacitor is transferred to the AC-side.

Compared to passive decoupling, the active decoupling inevitably leads to increased losses, due to the various types of losses in the decoupling stage. These additional losses can be reduced by two countermeasures. First, the amount of energy buffered in the decoupling capacitor has to be minimized. Therefore parallel and integrated active decoupling are clearly preferable from the efficiency point of view. Second, the number of processing stages from decoupling capacitor to AC-side need to be minimized, to allow efficient transfer of the buffered energy to the AC-side. This makes integrated decoupling the most promising active decoupling approach concerning efficiency.

2.2 Categorization of Module Integrated Converter Topologies

The various AC-module topologies can be categorized into distinct types. The categorization is based on how the DC-input at the PV-side is linked to the AC-output. Reviews on module integrated PV converters [21],[16] identified the following three distinct types of inverters: the high frequency-link (HF) inverter, the pseudo DC-link inverter and the DC-link inverter.

HF-link inverter: As shown in fig. 2.2(a), the direct current from the PV-input is transformed into a high frequency (HF) modulated current by a DC-AC stage, operating at high frequency. The

following AC-AC stage directly converts this HF current into a low frequency sinusoidal grid-current. Power-decoupling must be realized either at the PV-input side by passive or active decoupling or at the DC-AC stage by active integrated decoupling (see 2.1 for details). In any case, all stages must be able to handle a peak power of twice the nominal power.

Pseudo DC-link inverter: The pseudo DC-link inverter is shown in fig. 2.2(b). The current from the PV-input is transformed by a DC-DC stage operating at high frequency. The DC-DC stage is modulated to output a rectified sinusoidal current to the intermediate pseudo DC-link. The voltage of the pseudo DC-link is pulsating with double line frequency and has the shape of a rectified sinus. The following DC-AC stage switches at line frequency and unfolds the rectified current and voltage. The power decoupling is realized either at the PV-input by passive or active decoupling or at the DC-DC stage by active integrated decoupling (see 2.1). The stages must be able to handle a peak power of twice the nominal power.

DC-link inverter: The DC-link inverter, shown in fig. 2.2(c), has an intermediate DC-link. The DC-DC stage is controlled to charge the DC-link with a constant current from the PV-input side. The DC-AC stage converts the DC-current into a line frequency AC-current. The intermediate DC-link is controlled to a constant average value, whereas a double line frequency ripple of typically 25% is still tolerable. Both stages operate at high frequency. Power decoupling can be placed at the PV-input side (passive or active decoupling), the intermediate DC-link (passive decoupling) or at DC-AC stage (integrated active decoupling), see 2.1 for details. For power decoupling at the PV-input side all stages must be designed to handle a peak power of twice the nominal power. With power decoupling at the intermediate DC-link or the DC-AC stage, only the DC-AC stage must handle a peak power of twice the nominal power and the DC-DC can be designed for nominal power.

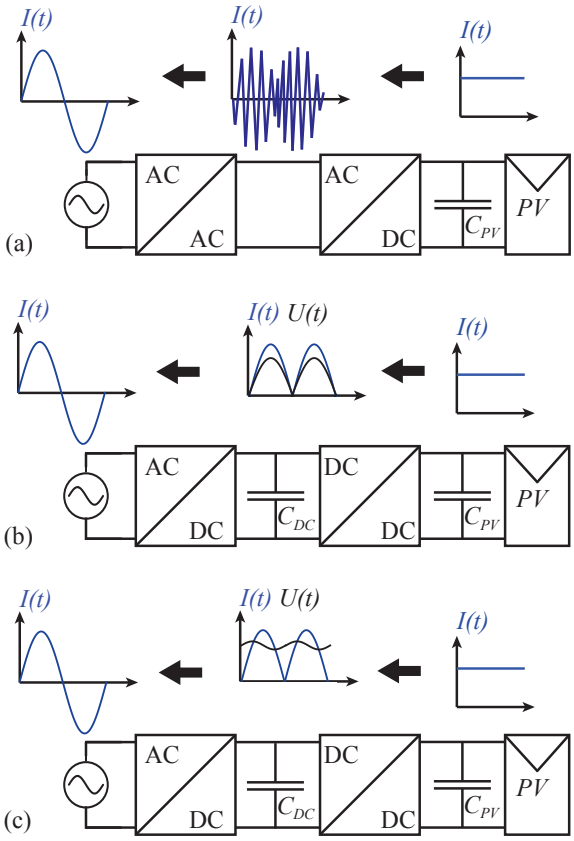


Figure 2.2: AC-module topology categorization: (a) HF-link inverter [21]; (b) Pseudo DC-link inverter [16]; (c) DC-link inverter.

2.3 Single-Input Topologies Review and Comparison

Among the multitude of AC-module topologies proposed in literature, a selection of topologies is presented and shortly discussed in this work. The selection focuses on the topologies with the highest reported efficiencies and the most promising system concepts.

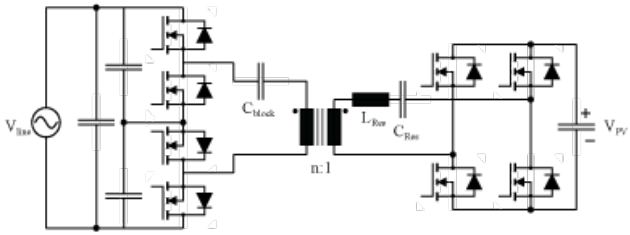


Figure 2.3: 175W series resonant LC inverter with HF-transformer and cyclo-inverter on AC-side [22].

2.3.1 High Frequency Link Topologies

Series Resonant LC combined with Cyclo Inverter

The topology proposed in [22] and shown in figure 2.3 consists of a series resonant LC-inverter on the DC-side combined with a cyclo inverter on the AC-side. The full bridge series-resonant inverter is operated under variable switching frequency and phase-shift control. Each bridge leg is operated under ZVS, which provides low switching losses when applying MOSFET's. The cyclo converter is configured as halfwave cyclo converter, by short-circuiting one of the split AC capacitor at each halfwave. The halfwave cycloconverter is operated under ZVS and exhibits two conducting transistors in the current path. By the halfwave configuration the amount of transistors is reduced, however a blocking capacitor C_{block} is needed on the AC-side to prevent transformer saturation. There are four distinct modes to control the power of the inverter: phase-shift control of the two full-bridge legs, cycloconverter phase modulation (phase-shift of secondary side, rel. to primary side), switching frequency (impedance of the resonant network) and burst mode control (only oparate during certain intervals at low load). These power control modes are combined (depending on load), to optimize the inverters efficiency. The LC-resonance frequency is designed to 40kHz, which is a tradeoff between efficiency (the lower the better) and resonance-component size (the smaller the better). The inverter operates at switching frequencies between 40kHz and 350kHz. Ringing, due to circuit-parasitic and the high switching frequency showed to be an issue and was estimated cause 10% increased switching losses on the laboratory test setup [22]. The high switching frequencies allow for a

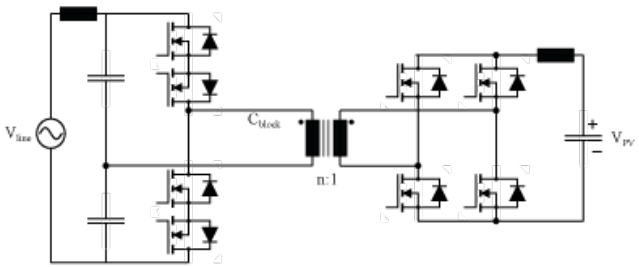


Figure 2.4: Dual active bridge with HF-transformer and cyclo-inverter on AC-side [24].

compact transformer and inductor design, though total inverter volume is not given in [22].
The authors of [23] proposed a series resonant LC-inverter with a bidirectional fullbirdge on the AC-side (instead of the halfbridge shown in fig. 2.3). The inverter is controlled in phase-shift mode and operates at a constant switching frequency $f_s = 100kHz$. The LC resonance frequency is $111kHz$. Simulation results confirm the control-strategy, but a laboratory prototype was not built and no details are given regarding system design and efficiency.

By the nature of the inverters structure, the power-decoupling must be achieved by a large capacitor on the PV-input side of typically several $mF's$ (the autors did not perform a proper DC-input capacitor-design).

The authors of [22] built a laboratory prototype, which reached an efficiency of η_{CEC}=95.9% ($V_{in} = 35V, V_{out} = 240Vrms/60Hz$, $P_{Nom} = 175W$).

Dual Active Bridge combined with Cyclo Inverter

The topology in figure 2.4 was proposed by the authors of [24]. The inverter combines a dual active bridge on the DC-input connected to a HF-transformer and a bidirectional halfbridge cycloconverter on the AC-side. The inverter is proposed for a battery charger with an input voltage of 280V-430V, but it could be adapted for connection to a PV-module, by changing the transformer turns-ratio. The inverter applies two power-control modes, frequency-control and phase-shift control. These two modes are combined to achieve ZVS over a wide op-

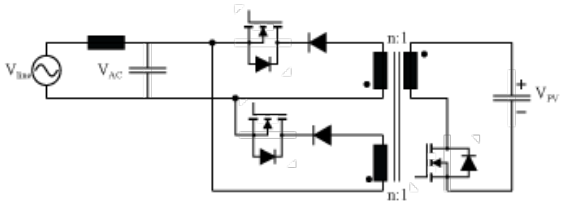


Figure 2.5: Single Transistor Flyback Inverter [25],[26].

erating range. The inverter operates at variable switching frequencies between 20kHz and 100kHz. The half bridge cycloconverter minimizes the amount of switches. Compared to the series LC-resonant inverter (fig. 2.3) this topology has the advantage, that one can get rid of the resonant-circuit elements. The power-decoupling must be realized by a large capacitor on the PV-input side of typically several $mF's$.

Proper operation of the control-strategy is demonstrated by simulation results. System design, laboratory prototype and efficiency measurements are not performed in [24].

Single Transistor Flyback Inverter

Figure 2.5 shows the inverter designed in [25]. It consists of a single transistor flyback converter with two center tapped transformer secondary windings. The center tap is connected to the AC-ground. The two outputs are connected to a common grid filter by a MOSFET-switch and a diode in series. The flyback switch is operated at high switching frequencies, whereas the secondary side switches are operated at the double line frequency under zero voltage and current condition. The flyback converter is operated in two distinct operating modes: discontinuous conduction mode (DCM) and BCM, on the boundary between DCM and continuous conduction mode (CCM). CCM is not an option, because the flyback converter must be controlled as current-source in order to maintain controllability [25]. In DCM the flyback converter is operated at a constant switching frequency. In BCM the switching fre-

quency is variable and depends on the line voltage and the load. At low load the switching frequency in BCM becomes very large, increasing the switching losses. By a clever combination of DCM, at low load, and BCM, at high load, a very compact transformer design can be realized. The maximal switching frequency for BCM is designed to be 40kHz, which denotes the border for changing from BCM to DCM.

The primary side flyback switch must withstand the sum of the input voltage and the output AC-voltage, which is reflected to the primary side of the transformer (when the primary switch is turned off). Additionally there will be an over-voltage spike caused by the leakage current of the transformer and the magnetizing current.

Again, the power decoupling must be realized by a large capacitor of several $mF's$ at the PV-input side.

The laboratory prototype built in [25] achieves an efficiency of 96% ($V_{in} = 50V$, $V_{out} = 230V/50Hz$, $P_{Nom} = 200W$).

Three-Port Flyback converter with Unfolding Bridge and Integrated Ripple-Port

The topology proposed in [27] and shown in fig. 2.6 is a modification of the single transistor flyback inverter in fig. 2.5. The DC-input side of the flyback inverter has an additional winding and two additional diodes. The ripple port is actually realized as second DC-input in parallel to the PV-input. At excess PV-power, energy is transferred to the ripple port via the diodes D_1 and D_2. At lacking PV-power, energy is directly transferred from the ripple-port to the AC-side by switch S_2, diode D_1 and the two primary windings in parallel. Therefore only the excess power is transferred to the ripple-port and fed directly from the ripple-port to the AC-side. Hence active integrated decoupling is achieved, which substantially reduces the losses, caused by the active decoupling. However the switches of the unfolding bridge at the secondary side are operated at high switching frequency equal to the primary side switches. The flyback operates at a switching frequency of 100kHz in DCM, which provides zero-current-switching (ZCS) turn-on and zero-voltage-switching (ZVS) turn-off. The ripple-port acts as a snubber-circuit, to eliminate voltage overshoot due to the leakage inductance. The voltage of the ripple port must be higher than the sum of the PV-input voltage and the AC-voltage reflected to the primary side. In [27] $V_{Rippleport}$ was designed to 150V with a ripple of 40V,

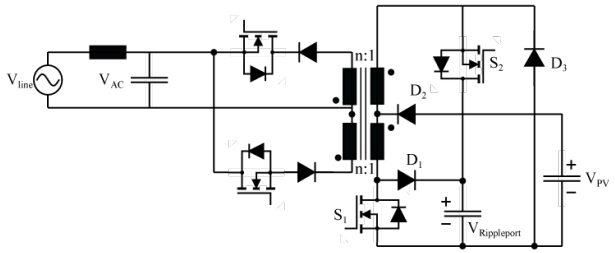


Figure 2.6: 110W Three-port flyback converter with unfolding bridge and integrated ripple-port [27].

for which a 50μF capacitance was necessary. The voltage stress of the flyback switch equals $V_{Rippleport}$, which is somewhat higher, than for a normal flyback inverter. The switch of the ripple-port must withstand twice the AC-voltage reflected to the primary side.

In [27] a laboratory prototype of the inverter is reported to have an efficiency of 91.2% ($V_{in} = 60V$, $V_{out} = 110V/60Hz$,$P_{Out} = 50W$).

An alternative variant of a three-port flyback inverter is proposed in [17] and shown in fig. 2.7. The ripple-port is realized with a reduced number of components and one primary winding. It features as well integrated active power decoupling and leakage current absorbtion by the ripple-port but at lower part-count.

The laboratory prototype built in [17] features a peak efficiency of 90.6% ($V_{in} = 60V$, $V_{out} = 110V/60Hz$,$P_{Out} = 40W$) and a Californian efficiency of 89% ($V_{in} = 60V$, $V_{out} = 110V/60Hz$,$P_{Nom} = 100W$).

Three Port Inverter with Push-Pull DC-port and Unfolding Bridge

The topology shown in fig. 2.8 applies a push-pull converter on the PV-side while the AC-side is realized by a bidirectional thyristor unfolding bridge [29]. This combination has the advantage of low amount of semiconductors in the conduction-path, hence reducing the conduction losses (same amount as single transistor flyback). Power-decoupling

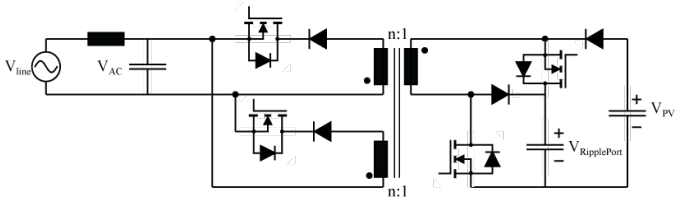


Figure 2.7: Three-port Flyback converter with integrated ripple-port using minimized number of components [28],[17].

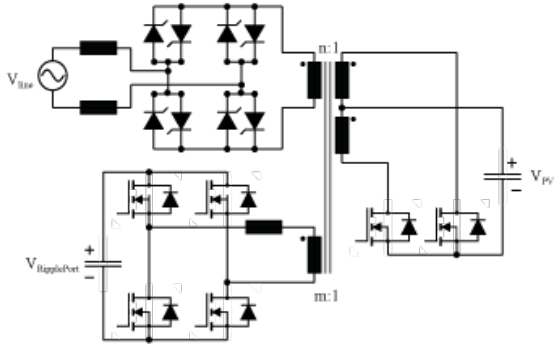


Figure 2.8: Three-port inverter with push-pull DC-port and unfolding bridge [29].

is realized by a ripple-port on a third transformer winding, consisting of a full bridge, a boost inductor and a capacitor. The ripple port injects/extracts current so that a constant power is drawn from the PV-side. The winding-ratio of the ripple port is designed in such a way, that small capacitances of tens of $\mu F's$ can be applied for both, the ripple port and the PV-side capacitance. The push-pull inverter operates at high switching frequencies and outputs a bipolar voltage pulse of 50% duty ratio to the AC-link transformer. The thyristor bridge switches at the same switching frequency as the push-pull switches. It operates as cyclo converter, described in [30], which controls the line current through the AC-inductors. The line current is continuous (CCM) with a switching frequent ripple. For a switching frequent ripple in the range of Δi_{line} ~20%I_{Nom} an AC-inductor of typically severall mH is needed. The full bridge of the ripple-port is operated as dual

active bridge and outputs a bipolar voltage pulse with 50% duty ratio at the same frequency as the AC-link voltage. The current through the ripple-port inductor is controlled by the phase-shift between the AC-link and the ripple-port voltage pulse.

The ripple-port voltage is controlled to follow the reference $v_{c,ref} = |\hat{V}_c \cos(\omega t + \Theta)|$. This effectively decouples the second harmonic power fluctuation, when $\hat{V}_c$ is adjusted according to the actual output-power. Details are discussed in [29]. This way of power decoupling has the advantage of minimal decoupling capacitance, because the ripple-port capacitor is discharged down to 0V and hence the whole stored energy is used for decoupling.

The transformer ratio from PV- to AC-side must be chosen, such that the AC-link voltage-pulse is higher than $\hat{V}_{line}$ under any operating conditions: $n_{trafo} U_{PV,min} > \hat{V}_{line}$. This unfortunately results in a rather high transformer ratio. The ratio between PV- and ripple-port-side is not restricted by fixed limits. However, together with the rippleport inductor, the transformer ratio determines the ripple-current on the PV-side and the maximal transferable power to/from the ripple-port. There exists a design trade-off between low PV-side ripple-current and transferable power, resulting in an optimal combination of transformer ratio and ripple-port inductor for a given maximal ripple-port power.

The transistor of the push-pull converter are exposed to a voltage stress of twice the value of U_{PV}, when one switch is on. The switches in the ripple-port full bridge must withstand the ripple-port voltage $U_{RipplePort}$. The switches at the PV-side port are exposed to an additional over voltage spike at turn-off due to the transformer leakage inductances. The thyristors of the AC-side cyclo converter must withstand the PV-side voltage reflected to the transformer AC-side $n_{trafo} U_{PV,max}$, which can be as high as 2-3x$\hat{V}_{line}$ (given an accordingly large input voltage range).

Nevertheless this topology is reported to be used by the AC-module manufacturer Solarbridge [13]. The P250HV-240 series micro inverter features efficiency values of η_{peak}=95.7% and η_{CEC}=95% (P_{nom}=240W, V_{in}=25V-50V, V_{out}=240Vrms/60Hz).

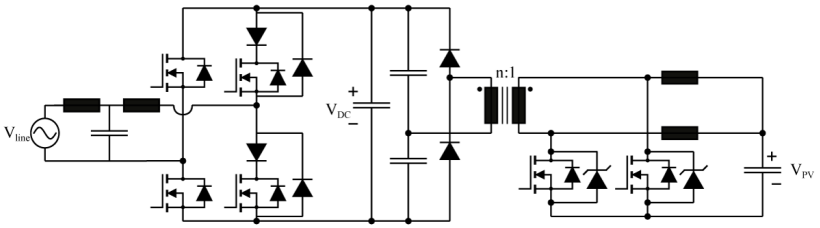


Figure 2.9: 250W micro inverter: interleaved boost, PWM full bridge inverter [31].

2.3.2 DC Link Topologies

Interleaved Boost, PWM Full Bridge Inverter

An isolated interleaved boost converter feeds into an intermediate DC-link, from which the power is transferred to the AC-side by a PWM full bridge inverter (see fig. 2.9). The interleaved boost inverter switches at 35kHz. The input and output current ripple is greatly reduced by the interleaving. The transformer turn-ratio N must be chosen, so that the DC-link voltage reflected to the primary side is higher than V_{PV} and so that the minimal duty-ratio is above 50% for any operating condition. This second constraint guarantees a freewheeling path for the boost inductor currents and is an inherent characteristic of this isolated boost converter. It unfortunately limits the transformer-ratio to rather low values for an actual design with high voltage input variations. For the prototype built by the authors of [31] the transformer-ratio is designed to be N=2 with an input voltage variation of 20V-40V. The voltage stress of the boost transistors equals the DC-link voltage reflected to the primary side. At turn-off an additional over voltage spike is caused by the transformers leakage inductances. Instead of adding passive or active snubbers, the authors minimized the leakage inductance during transformer design and added a safety margin of 20% to the voltage rating of the switches, resulting in a total blocking voltage of 100V for the boost switches. The DC-AC PWM inverter has one leg switching at line frequency and one leg switching at high frequency. This modulation scheme is commonly named single phase chopping. The high frequency leg performs the PWM and is equipped with external antiparallel SiC diodes, to reduce the switching losses. An advantage of

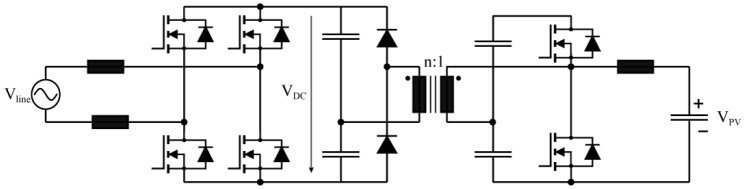


Figure 2.10: 210W micro inverter: Isolated Boost Halfbridge, PWM Full Bridge Inverter [32].

the PWM DC-AC inverter is its capability to deliver reactive power. Power-decoupling is achieved by passive capacitive decoupling at the intermediate DC-link. An electrolytic capacitor of $C_{DC} = 88\mu F$ value is used in [31]. The electrolytic capacitor is not thought to be critical for the lifetime of the inverter, however no detailed lifetime analysis is performed.

A laboratory prototype was built in [31]. The inverter achieves the following efficiencies: $\eta_{peak} = 94.5\%$ and $\eta_{EU} = 93.5\%$ ($P_{Nom} = 250W$, $V_{in} = 36V$,$V_{out} = 230V/50HZ$).

Isolated Boost Halfbridge, PWM Full Bridge Inverter

The authors of [32] proposed an isolated boost half bridge DC-DC inverter for a 210W micro inverter, as shown in fig. 2.10. The focus of their investigations was on the DC-DC converter. Due to resonant transition intervals, the boost half bridge switches under ZVS conditions over a wide operating range. Only at low power, ZVS is not possible anymore. Voltage spikes at turn-off due to the transformer leakage inductance are eliminated by the additional capacitances across the switches. The boost inductance is designed to $200\mu H$ and the boost switches are operated at 21.6kHz. The topology features a low amount of active switches, but has a higher number of passive components. Unfortunately the designed capacitance values at the transformer input and output are not given. The voltage stress of the boost switches is equal to the sum of the reflected voltage of the output half bridge capacitor and the input half bridge capacitor. Though the authors of [32] did not provide waveforms and analysis on how the parallel con-

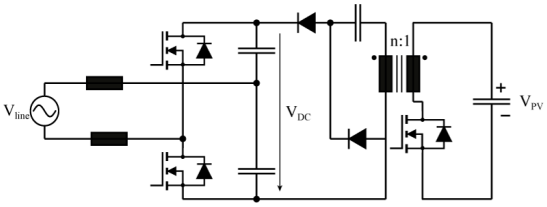


Figure 2.11: 180W micro inverter: Resonant switching flyback and PWM halfbridge [33].

nected capacitors on the input and output half bridge are balanced and controlled. The power-decoupling is achieved by the large intermediate DC-link capacitance. Details on the designed capacitance value are not provided.

It is claimed in [32], that the laboratory prototype reaches a peak efficiency of the DC-DC converter stage of 98.2% ($V_{in} = 43V$,$V_{out,DC} = 380V$,$P_{Nom} = 210W$).

Resonant Switching Flyback and PWM Halfbridge

The topology shown in fig. 2.11 and proposed in [33] consists of a resonant switching flyback converter, an intermediate DC-link and a PWM halfbridge. The flyback inverter has an additional serial capacitance and a diode on the secondary-side to operate in a quasi resonant mode. A resonance circuit is formed on the secondary side by the additional capacitance and the transformer leakage inductance, which provides zero currrent turn-off of the secondary diodes. Therefore the turn-off losses of the secondary side diode, due to the leakage inductance, are eliminated. The size of the additional resonance capacitance is $20\mu F$. The switching frequency is 50kHz. The authors report, that the resonant switched flyback improves the efficiency by 0.8%, compared to the normal flyback converter [33]. Over voltage spikes at turn-off of the primary flyback-switch still persist and the authors do not address this problem. The voltage stress of the primary flyback switch is the sum of the PV-input voltage and the DC-link voltage reflected to the primary side. The DC-AC PWM half bridge has the advantage of lower amount of active switches, but requires a higher DC-link voltage, which increases the voltage stress of the switches. The authors compared the

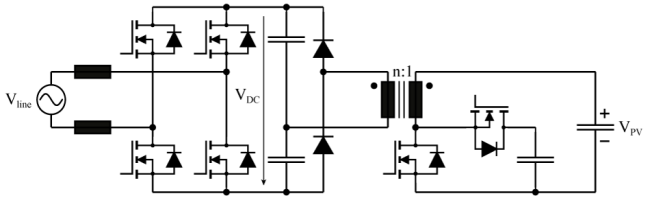


Figure 2.12: 1kW micro inverter: Active clamp flyback and PWM full bridge [34].

PWM half bridge inverter with a PWM full bridge inverter by means of a laboratory test setup. The half bridge inverter showed to have 0.3% higher efficiency. ($P_{Nom} = 180W$). Power-decoupling is performed by the intermediate DC-link. The total DC-link capacitance is $440\mu F$ at 380V DC-link voltage.

A laboratory prototype of the whole AC-module showed, that the inverter achieves a maximal efficiency of 93% ($V_{in} = 24$V, $V_{Out} = 120$V/ 60Hz, $P_{Nom} = 180$W) [33].

Active Clamp Flyback and PWM Halfbridge Converter

The inverter proposed in [34] and shown in fig. 2.12 is based on a modified active clamp flyback DC-DC converter and a PWM full bridge inverter. The modified flyback DC-DC converter has an active clamp circuit on the primary side consisting of an additional switch and clamp capacitor. The secondary side consists of a dual series resonant circuit. The DC-DC converter is actually not operated as flyback, but as forward converter. The voltage of the active clamp capacitor is higher than V_{PV}. The current transferred through the transformer increases, when the flyback-switch is turned on. To decrease the current, the active clamp switch is turned on. The DC-DC converter is operated in continuous conduction mode (CCM). The resonance circuit on the secondary side formed by the parallel capacitances and the additional inductance provides zero current turn off of the diodes. This eliminates the reverse recovery losses and losses caused by the secondary transformer leakage inductance. On the primary side the switches are turned-off and -on under ZVS condition. At commutation, a resonant circuit is formed by the transformer leakage inductance and parasitic ca-

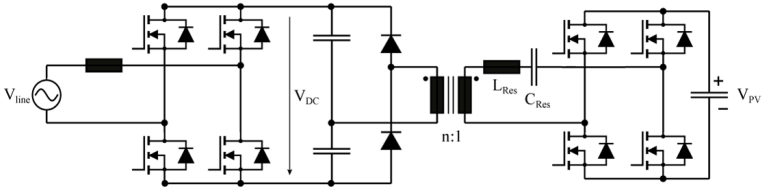


Figure 2.13: Series LC-resonant DC/DC and PWM full bridge converter [35].

pacitances of the switches, which discharges the parasitic capacitances. The voltage-stress of the primary side switches is equal to the clamp capacitor voltage. Voltage spikes at turn-off, cause by the leakage inductance, are not an issue, due to the forward-converter operation mode. The DC-DC converter operates at 50kHz and the DC-AC inverter at 20kHz.

Power-decoupling is achieved by the intermediate DC-link capacitor, whose capacitance value was designed to $560\mu F$.

Experimental results from a laboratory prototype show, that the inverter has a maximum efficiency of 94% ($V_{in} = 60$V, $V_{out} = 220$V/60Hz, $P_{Out} = 600$W)[34].

Series LC Resonant and PWM Full Bridge Converter

The two stage micro-inverter shown in fig. 2.13 applies a convectional LC-series resonant DC-DC converter to boost the voltage to the intermediate DC-link. A PWM full bridge acts as interface between the DC-link and the AC-grid. The resonant converter is realized with a minimized amount of semiconductor devices as discussed in [35]. The PV-side consists of a full bridge and the DC-link side is realized with a half bridge diode rectifier feeding a split DC-link. At high load, power transfer is controlled by the duty-ratio of the voltage pulses operating with constant switching frequency. At lower loads, the power control mode is changed to frequency-control, to maintain ZVS of all switches. The voltage stress of the full bridge on the PV-side equals V_{PV}. The half bridge diodes must with-stand the DC-link voltage.

A laboratory prototype and measurements do not exist for the com-

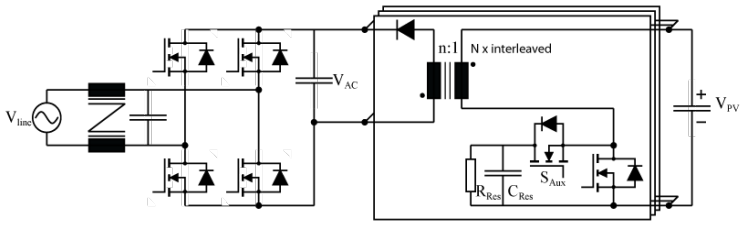


Figure 2.14: 260W micro inverter: Interleaved resonant switched flyback converter with an unfolding bridge [36],[37], [38].

plete micro-inverter, because only the LC-series resonant DC-DC stage was discussed and implemented in [35]. The efficiency of the DC-DC stage is demonstrated to be η_{Euro}=96.0% (P_{nom}=140W, V_{in}=35V, $V_{out,DC}$=700V)

2.3.3 Pseudo DC Link Topologies

Interleaved Resonant Flyback Converter with Unfolding Bridge

The topology shown in fig. 2.14 is an interleaved resonant flyback converter with an unfolding bridge. The flyback converter, which switches at high frequency, is controlled to deliver a rectified sinusoidal current, which is filtered by the AC-capacitance and unfolded by the full bridge, switching at line frequency. Each basic flyback module operates in boundary conduction mode (BCM). By activation of the resonance snubber circuit (S_{Aux}: ON), the main flyback switch, can be turned on and off under ZVS, due to a resonant transition that charges/discharges the capacitance in parallel to the switch. The resonant circuit is formed by the transformer leakage inductance and C_{Res}. At turn-off, the energy in the leakage inductance is stored into C_{Res} and fed back to C_{PV} when the switch is turned on again. In this way over voltage peaks due to the leakage inductance can be eliminated. The voltage stress of the flyback switch equals the sum of V_{PV} and V_{AC}, reflected to the primary side.

The interleaved flyback inverters can operate in 3 different modes, which are chosen, so that the conversion efficiency is optimized. First there is the normal flyback-mode, which is used for low V_{AC} and P_{Out}.

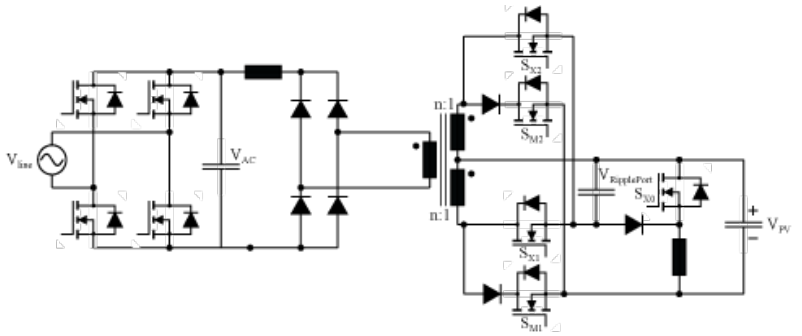


Figure 2.15: 500W micro inverter: Push pull converter with unfolding bridge and decoupling circuit. [39].

For high output voltages V_{AC}, the quasi-resonant mode is applied to reduce the switching losses. At high power P_{Out}, several flyback modules are interleaved to decrease the conduction losses. This operation strategy enhances the efficiency over wide operating range.

The power-decoupling is achieved by a large capacitance on the PV-input side. Typically a capacitance of several mF's is necessary, however the exact value is not specified in [36].

This topology is applied by the AC-module manufacturer Enphase. The M215-60-2LL-S22/S23 series micro inverter features efficiency values of η_{peak}=96.3% and η_{CEC}=96.0% (P_{nom}=215W, V_{in}=22V-36V, V_{out}=240Vrms/60Hz). This is the record for commercially available micro inverters, as of September 2012.

Push Pull Converter with Unfolding Bridge and Decoupling Circuit

A push-pull converter with an unfolding bridge and a parallel active decoupling on the PV-side is proposed by [39] and shown in fig. 2.15. A parallel active ripple port is installed on the PV-input side. The capacitor of the ripple-port is charged from the PV-input capacitor by means of a booster (switch S_{X0}) to a voltage level higher than V_{PV}. The push-pull converter has actually two independent parallel inputs, one from the PV-input side (switches S_{M1} and S_{M2}) and one from the ripple-port capacitor (switches S_{X1} and S_{X2}). The push-pull converter

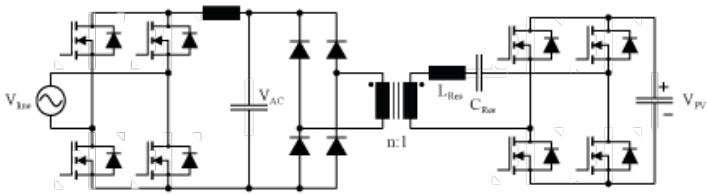


Figure 2.16: 100W micro inverter: Series resonant LC converter with unfolding bridge. [13].

is operated as a forward converter in discontinuous conduction mode. It is modulated at 20kHz switching frequency to output a sinusoidal current envelope. On the transformer secondary side a diode bridge rectifies the current and the LC-filter removes the current ripple. Finally an unfolding bridge, switching at double line frequency, sets the right current polarity. The voltage stress of the push-pull switches of the ripple port equals twice the value of $V_{RipplePort}$. The push-pull switches of the PV-input must withstand the sum of V_{PV} and $V_{RipplePort}$. Further the transformer leakage inductance leads to an additional over voltage spike, when turning off the push-pull switches. The boost-switch must withstand the voltage $V_{RipplePort}$.

The ripple-port is controlled in such a way, that a constant current flows from the PV-input side. In this way small capacitances can be used for the PV-input side, $C_{PV} = 22\mu F$, and the ripple port, $C_{RipplePort} = 50\mu F$.

The laboratory prototype, built by the authors of [39], exhibits a peak efficiency of 94% ($V_{PV} = 35V$, $V_{out} = 100V/50Hz$,$P_{Out} = 300W$). When deactivating the active ripple port, the measured efficiency increases to 95% under the same conditions. Hence the losses due to the active ripple port cause a 1% efficiency decrease.

Series LC Resonance Converter with Unfolding Bridge

Fig. 2.16 shows the commercial available inverter from OKE services [13]. The inverter consists of a series resonant LC converter that is modulated to output a current waveform with sinusoidal envelope. On the transformer secondary side, the diode bridge rectifies the current

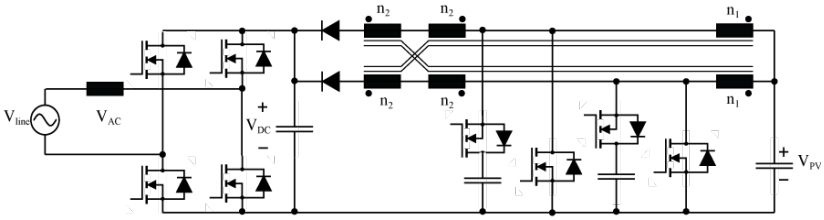


Figure 2.17: 2kW Dual Coupled inductor boost PWM converter [41].

and the LC-filter removes the current ripple. The unfolding bridge, switching at double line frequency, unfolds to current waveform to the right polarity. The resonant converter exhibits low switching losses due to soft switching. The voltage stress of the primary side switches equals V_{PV}. There are no over voltage spikes, caused by the leakage inductance, because of the resonant operation. Power-decoupling must be achieved by a large capacitance at the DC-input side (typical value of several mF's).

The OKE4 inverter reaches an efficiency of $\eta_{Europ} = 91.6\%$.

2.3.4 Topologies without Galvanic Isolation

AC-module topologies without galvanic isolation could actually also be classified into the categories HF-link, DC-link and pseudo DC-link. However the literature review revealed only a few publications, dealing with transformer-less AC-module topologies. The work in [40] gives a comprehensive overview of transformerless AC-module topologies. It is concluded that for the European 230V/50Hz grid transformerless topologies suffer from low efficiency, do to the high voltage step-up ratio. The only transformerless AC-module proposed in literature featuring a sufficient efficiency is the following topology.

Coupled Inductor Boost PWM Converter

The topology in fig. 2.17 and proposed in [41] consists of a high step-up interleaved boost converter, an intermediate DC-link and a PWM full bridge inverter. The boost converter is made with coupled inductors, to

achieve high step-up ratio and has an active clamp circuit, which realizes ZVS of the main and the auxiliary switches (leakage energy is recovered). Moreover diode reverse recovery losses are reduced, as the di/dt is controlled by the inherent leakage inductance of the coupled inductors. The DC-link voltage is designed to 380V, whereas the input voltage is 38-50V. The boost converter switches at 50kHz and the full bridge at 20kHz. The voltage stress of the boost switches is $V_{S,boost} = V_{in}/(1-D)$ (D: boost converter duty ratio). The Diodes must withstand twice the DC-link voltage (detailed analysis of the voltage stress is not provided by the authors). The designed prototype inverter applies 250V rated boost switches and 1.2kV diodes. Power decoupling is achieved at the intermediated DC-link.

The 2kW prototype is reported to achieve a European efficiency of 92.7% (P_{Nom}=2kW,V_{In}=48V,V_{DC}=380V).

2.3.5 Comparison of the Topologies and System Concepts

The preceding review of the single input topologies revealed a multitude of different system concepts and topologies for the realization of an AC-module. A systematic topology comparison serves to analyze the advantages and disadvantages of the various system concepts and helps to identify the most promising AC-module topologies. The comparison is based on a common specification derived from the requirements in chapter 1.2.1. Though the comparison focuses on the component ratings of the power processing stage. Hence general aspects, safety issues and several requirements for the grid interface are not taken into account. Further, in contrast to the specification in chapter 1.2.1, the compared AC-modules are specified to a have single MPP-tracking port only. Table 2.1 lists the system specification for the performed design. A switching frequency of 20kHz is assumed for DC-AC inverters, which is often regarded as the minimal feasible switching frequency for grid-tied inverters. The DC-DC converters are assumed to operate at a switching frequency of 40kHz. Even though the switching frequencies are selected without an optimization, their exact values do not greatly alter the relative results of the topology comparison, because all compared topologies rely on the same switching frequencies.

From the over twenty AC-module topologies reviewed in sec.2.3,

Table 2.1: Summary of specifications and assumptions for the performed system design.

Specifications:	Power:	P_{Nom}=300W
	MPP-Tracking:	1xMPPT on module level
	PV Input Range:	$V_{PV,in}$=25.5-63V
	Input Voltage Ripple:	$k_{PV,Europ} \geq$0.998
	Line Voltage:	V_{line}: 230Vrms/50Hz
	Line Current Ripple:	$\hat{I}_{f,switch} \leq 0.05 \cdot \hat{I}_{1,p_{nom}}$
Assumptions:	Switching frequency:	DC-AC inverter $f_{s,AC}$=20kHz DC-DC converter $f_{s,DC}$=40kHz Variable $f_{s,avg} = f_{s,DC}$ resp. $f_{s,AC}$
	DC-DC Conv. current:	For CCM $i\Delta_{p,p} \leq 0.2 \cdot I_{DC,rms}$
	Stand-By Reactive Power:	$Q_{noload,max}$=8VA
	Flyback Transformer Ratio:	low primary switch voltage-stress [25] $V_{prim,min} \cdot \frac{N_{sec}}{N_{prim}} \simeq 0.3 \cdot V_{sec,max}$
	Power Decoupling:	$\Delta_{Vdc,pp} = 0.25 V_{dc,avg}$ [42]

eleven topologies are preselected based on the performance reported in the respective publication. Topologies with a reported efficiency below 90% or a large amount of semiconductors are not considered. The compared topologies are listed in table 2.2

Applied Topology Comparison Method

An often applied, rough measure to compare different topologies simply counts the number of active switches and the number of switches and diodes in the conduction path. Additionally the number of passive components can also be taken into account. This approach is easy to apply and does not require the design of any of the compared topologies. A more detailed comparison, which is often desirable to perform a meaningful comparison, involves a system design of the compared topologies based on a common system specification. The detail in which this system design is performed finally depends on the required accuracy of the comparison.

The current and voltage peak values of the components can normally still be calculated with low effort by considering the worst case operating-point, e.g. maximal line voltage for DC-AC inverters. Though in order to determine the rating of the semiconductors and approximate con-

duction losses of a component, the rms-current is needed. For the calculation of the rms-currents the exact modulation and control of each converter stage needs to be known, which requires calculations of each switching period over a line period for DC-AC inverters. If in addition losses in magnetic components and switching losses shall be considered, first exact switching times and turn-on/-off currents and voltages must be calculated over at least a quarter line period, which involves an extension of the calculation. The second, more challenging task is then to select valuable design parameters for the magnetic components (core-size and material, windings, type of wire etc,) and the semiconductors (type of semiconductor and chip-area). Only with these design parameters the losses can finally be calculated. The challenge about selecting the design parameters is, that they are very application specific and must actually be optimized separately for each topology. Selecting the parameters based on assumptions, strongly influences the comparison and hence the result of the comparison becomes somehow arbitrary.

In literature different examples of topology comparisons can be found. In [21] for example a comparison of eight different topology candidates for an AC-module are compared. For each of the compared topologies, such as flyback, push-pull, full-bridge and resonance converter, a system design is performed to determine the component stresses and the size of the passive components (transformer, inductors, capacitors). This allows to calculate the ratings of the switches and estimate the cost and the efficiency (for a given semiconductor technology using the ratings of the switches). In addition to the system specifications a set of assumptions are made to facilitate system design (including also above mentioned design parameters for magnetics and semiconductors). Some of the assumptions seem somehow arbitrary, as they would be subject to optimization in a practical system design.
Another approach is pursued for the comparison of 3 phase current-source inverters in [43], as well as for the comparison of single-phase transformerless PV-inverters in [44]. For the comparison method normalized bench marking factors are defined as indicators for semiconductor and inductor losses. This bench marking factors, originally proposed in [45] (section 3.2), are based on electrical ratings (voltage and current peak/rms values). Detailed parameters for semiconductors and magnetics are not required. In this way arbitrary assumptions required for a system design can be avoided and a comparison of various topologies

can be performed based on an electrical design only. However, the validity of the bench marking factors must be kept in mind, when analysing the results of the comparison.
The following approaches aim for a true optimized system design without any assumptions. The comparison of three phase power factor correction (PFC) topologies in [46] is based on efficiency and the power density of each topology. Assumptions are only made regarding switching frequency. The chip area based comparison of three different three phase DC-AC inverter topologies in [47] is based on a complete system optimization for each topology, getting rid of any assumptions. Needless to say that both of these approaches require detailed system models and are time-consuming to perform. Therefore they do not allow for a larger number of compared topologies.

Due to the multitude of single-input topologies and system concepts proposed in literature, the comparison performed in this work must be feasible for a set of up to twenty topologies. The comparison is therefore performed using six different bench marking factors. The bench marking factors are based on electrical design only, in the same manner as for the comparisons in [43],[44] discussed above. The semiconductor bench marking factors also rely on the method in [45] (section 3.2).

Total Installed Semiconductor Power $\mathbf{VA_{Tot}}$: The total installed semiconductor power is an indicator for semiconductor costs. It is calculated by summing up the product of the rms-current $I_{i,rms}$ and the blocking voltage $\hat{V}_{block}$ over all applied semiconductors N:

$$VA_{Tot} = \sum_{i=1}^{N} \hat{V}_{block} \cdot I_{i,rms}. \tag{2.1}$$

Conduction Loss Factor $\mathbf{\Xi_{Cond}}$: The semiconductor conduction losses are approximated by the normalized conduction loss factor Ξ_{Cond} defined in [45] (section 3.2, formula 3.2.6):

$$\Xi_{Cond} = \sum_{i=1}^{N} \left(\frac{I_{rms,i}}{I_{line,nom}}\right)^2 \cdot \left(\frac{\hat{V}_i}{V_{line,nom}}\right)^{\beta}. \tag{2.2}$$

N is the number of applied semiconductors. $I_{rms,i}$ and $\hat{V}_i$ denote the rms-current and the blocking voltage of each semiconductor. These values are normalized to the AC-side nominal voltage

$V_{line,nom}$ and current $I_{line,nom}$. The semiconductor technology specific factor β accounts for the fact, that conduction losses increase with increased voltage rating.

Switching Loss Factor $\Pi_{\mathbf{Switch}}$: The semiconductor switching losses are also approximated by the normalized switching loss factor Π_{Switch} defined in [45] (section 3.2, formula 3.2.10 and 3.2.14). First the currents and voltages at commutation ($I_{on}(t_k)$, $V_{on}(t_k)$, $I_{off}(t_k)$ and $V_{off}(t_k)$) are used to calculate turn-on and turn-off energies for a specific semiconductor, which are again normalized to nominal AC-side voltage $V_{line,nom}$ and current $I_{line,nom}$. For DC-AC conversion the switching energies of a given switching instant t_k vary over a line period and are therefore summed up for every switching period over a line period:

$$\Pi_{on} = \sum_{t_k=0}^{T_{line}} \frac{I_{on,i}(t_k)}{I_{line,nom}} \cdot \frac{V_{i,on}(t_k)}{V_{line,nom}} \tag{2.3}$$

$$\Pi_{off} = \sum_{t_k=0}^{T_{line}} \frac{I_{off,i}(t_k)}{I_{line,nom}} \cdot \frac{V_{i,off}(t_k)}{V_{line,nom}}. \tag{2.4}$$

Second the turn-off and turn-on energies are scaled by a factor, which takes into account the dependence of the switching losses on the devices voltage rating. The factor α is a semiconductor technology specific constant. The scaled switching energies are summed up over all applied semiconductors N to get the bench marking factor:

$$\Pi_{Switch} = \sum_{i=1}^{N} (\Pi_{i,on} + \Pi_{i,off}) \cdot (\frac{\hat{V}_i(t_k)}{V_{line,nom}})^{\alpha}. \tag{2.5}$$

Transformer Area-Product $\mathbf{A_{CW,Trafo}}$: To get an idea of the size of the applied transformers, the transformer area product is used as bench marking factor. The winding area is calculated assuming a current density of S_{rms} =5A/mm^2, where M is the number of windings, n_i the turns-number of each winding and $I_{rms,i}$ the rms-current of the corresponding winding:

$$A_W = \frac{1}{S_{rms}} \sum_{i=1}^{M} n_i \cdot I_{rms,i}. \tag{2.6}$$

The maximal flux density is proportional to the winding voltage integral $\int U_{wind}(t)dt$. The core area can be calculated with the maximal value of this integral, by assuming a saturation flux density of B_s =250mT (typical value for ferrite). In DC-AC and DC-DC conversion, voltage pulses at switching frequency are applied at the winding terminals, whose amplitudes $\hat{U}_{pr}$ are approximately constant over a switching period. The length of the voltage pulses are given by the on-time t_{on} of the semiconductors applied at the winding terminals. The on time $t_{on,max}$ and voltage $\hat{U}_{pr,max}$ leading to the highest integral value over the specified operating range, are needed to calculate the core area:

$$A_C = \frac{\hat{U}_{pr,max} \cdot t_{on,max}}{B_s}. \tag{2.7}$$

The transformer area product is finally given by:

$$A_{CW,Trafo} = A_C \cdot A_W. \tag{2.8}$$

Total Stored Inductive Energy $\mathbf{E_{Ind,Tot}}$: The total stored inductive energy reveals the size of the applied inductors. For each inductor the maximal stored energy is calculated by the maximal current flowing through the inductor. The energies of all applied indcutors N, are then summed up:

$$E_{Ind,Tot} = \sum_{i=1}^{N} \frac{1}{2} \cdot L_i \cdot \hat{I}_{Li}^2. \tag{2.9}$$

Magnetic energy stored in the magnetizing inductance of flyback-transformers is also counted as stored inductive energy.

Total Stored Capacitive Energy $\mathbf{E_{Cap,Tot}}$: This bench marking factor indicates the size of the installed capacitors. The maximal stored energy of each capacitor in the topology is calculated by taking into account the maximal voltage (at any specified operating condition), to which a capacitor is charged. These energies are then summed up over all applied capacitors N:

$$E_{Cap,Tot} = \sum_{i=1}^{N} \frac{1}{2} \cdot C_i \cdot \hat{V}_{Ci}^2. \tag{2.10}$$

Assumptions and Simplifications

The following assumptions are made for the design and comparison of the AC-module topologies:

Inductor Design for DCM: In the case of discontinuous conduction mode (DCM) operation, DCM shall be guaranteed for any operating condition. The inductance value is calculated, such that the converter reaches BCM (boundary conduction mode) at the critical operating point (being nominal power and minimal input/output voltage).

Inductor Design for CCM: When the converter operates in continuous conduction mode (CCM), the allowed output current ripple is specified as percentage of the current at nominal power, I_{Nom}. For DC-AC inverters the limit is $\hat{I}_{f,switch} \leq 0.05 \cdot \hat{I}_{1,p_{nom}}$ and for DC-DC converters it is $i\Delta_{p,p} \leq 0.2 \cdot I_{DC,rms}$.

LC Line filter: In case of a DC-AC inverter operating in DCM, an LC filter is added, to attenuate the line current ripple at switching frequency to the limits specified in 2.1. When the inverter is operating in stand-by (P_{out}=0W), the reactive power generated by the LC filter shall not surpass the limit $Q_{NoLoad,max}$=8VA.

Selection of Semiconductor Types: All diodes are assumed to be SiC Shottky diodes, for the sake of simplicity. Switches are assumed to be MOSFET, if they are either operated under ZVS or under hard switching but with blocking voltages below 200V. Switches operated under hard switching and higher blocking voltages are selected to be IGBTs

Model of MOSFETs for Rating Factors: The MOSFETs are assumed to be of type Super Junction (SJ) MOSFETs, if their blocking voltage is above 250V, and of type GD MOSFET, for blocking voltages below 250V ([48],section 7 and 6).
The dependence of conduction losses on the voltage rating, see eqn. 2.2, are determined out of the analytical equations for the on-resistance in [48] (formula 1.20, 6.26 and 7.14): $\beta_{GD} = 1$ and $\beta_{SJ} = 4/3$.
The switching loss parameter α, see eqn. 2.5, is determined according to the following considerations: For the calculation of the scaling factor two MOSFETs with the same current capability

but with different voltage ratings are considered. The MOSFET switching losses are approximately given by:

$$P_{switch} = 0.5 \cdot U_{d,off} \cdot I_{d,off} \cdot t_{rv} + 0.5 \cdot (U_{d,off} + U_{pk}) \cdot I_{d,off} \cdot t_{fi}, \tag{2.11}$$

where t_{rv} is the voltage rise time, t_{fi} is the current fall time and U_{pk} the over-voltage spike at turn-off. In equation 2.11 only t_{rv} and t_{fi} are dependent on the rated blocking voltage of the switch. Further for the same current capability the chip area must increase for higher blocking voltage. The necessary increase in chip area can be approximated by calculating the thermal resistance and assuming unchanged junction and ambient temperature for the switch with higher blocking voltage. The rise and fall times are assumed to increase proportional to the chip-area. From this considerations results after solving some algebraic equations the dependency: $\alpha = \beta/2$

Model of IGBTs for Rating Factors: In [43] the switching loss parameter α is derived out of data from Infineons IGBT portfolio and is found to be $\alpha = 1.4$. The conduction loss parameter β is determined from the latest generation of IGBTs from IR, fig.4 in [49]: $\beta = 0.5$.

Model of Diodes for Rating Factors: The characteristics for SiC diodes are taken from a publication from the manufacturer Cree [50]. The conduction loss factor is read out from fig.1: β= 0.8. Switching losses of SiC Schottky diodes are assumed to be negligibly small. The switching loss parameter α is therefore irrelevant.

Results Rough Comparison

For each of the considered topologies in table 2.1 a system design is performed based on the common system specification in table 2.1. The waveforms are calculated based on a simple converter model implemented for each topology. This allows to calculate the six bench marking factors, described above.

Table 2.3 lists the calculated factors for all eleven topologies. The smaller the benchmarking factor, the better the performance of the topology. Hence, the best values for each benchmarking factor are the minima, which are highlighted in bold. The worst values, being the maxima, are marked in italic. For a more intuitive evaluation of the

Table 2.2: Overview of the compared topologies.

Topologies			Comment	*ID*
HF-Link:	LC-Resonant & Cyclo:	Fig. 2.3	Recommended	*I*
	Rippleport Push-pull:	Fig. 2.8	Solarbridge	*II*
Pseudo DC-link:	Flyback in BCM:	Fig. 2.5		*III*
	Resonant Flyback:	Fig. 2.14	Enphase	*IV*
	Rippleport Flyback:	Fig. 2.7		*V*
	Rippleport Push-pull:	Fig. 2.15		*VI*
DC-link:	Resonant Flyback:	Fig. 2.11		*VII*
	Clamped Flyback:	Fig. 2.12		*VIII*
	Isolated Boost:	Fig. 2.9		*IX*
	Coupled Inductor Boost:	Fig. 2.17		*X*
	LC Resonant Boost:	Fig. 2.13		*XI*

Table 2.3: Topology comparison calculated bench marking factors: The best values of each category are the minima, which are marked in bold. The worst values are the maxima, marked in italic.

ID:	VA_{Tot}	Ξ_{Cond}	Π_{Switch}	$A_{CW,trafo}$	$E_{Ind,Tot}$	$E_{Cap,Tot}$
I	5.68E+3	2.05E+2	4.19E+3	1.70E-8	2.01E-2	*1.25E+1*
II	1.00E+4	2.18E+2	*1.05E+5*	6.60E-8	4.56E-2	**9.39E-1**
III	7.26E+3	2.66E+2	4.35E+3	2.05E-8	2.24E-1	1.24E+1
IV	5.43E+3	**8.17E+1**	**3.89E+3**	2.32E-8	**1.374E-2**	1.24E+1
V	*1.63E+4*	*5.75E+2*	2.02E+4	3.48E-8	1.259E-1	2.41
VI	9.47E+3	1.75E+2	4.85E+3	5.06E-8	7.97E-2	1.33
VII	1.07E+4	2.54E+2	3.18E+4	*6.97E-8*	1.33E-1	4.15
VIII	7.24E+3	2.29E+2	7.42E+3	3.29E-8	2.34E-1	2.53
IX	6.47E+3	1.04E+2	1.13E+4	2.26E-8	6.80E-2	2.28
X	9.41E+3	3.39E+2	1.39E+4	5.54E-8	*2.52E-1*	2.81
XI	**5.03E+3**	1.15E+2	7.70E+3	**1.35E-8**	5.88E-2	2.84

comparison, the results are further illustrated on a six-axis spider plot. As an example, fig. 2.18 shows the calculated bench marking factors, for a single transistor flyback. Note that the axis are inverted. The component values, currents and voltages needed for calculating the bench marking factors are indicated in fig. 2.18. For better comparison the bench marking factors of all topologies are normalized to the maxima among the compared topologies (marked in italic in table 2.3). The normalized characteristic of the single transistor flyback inverter is given

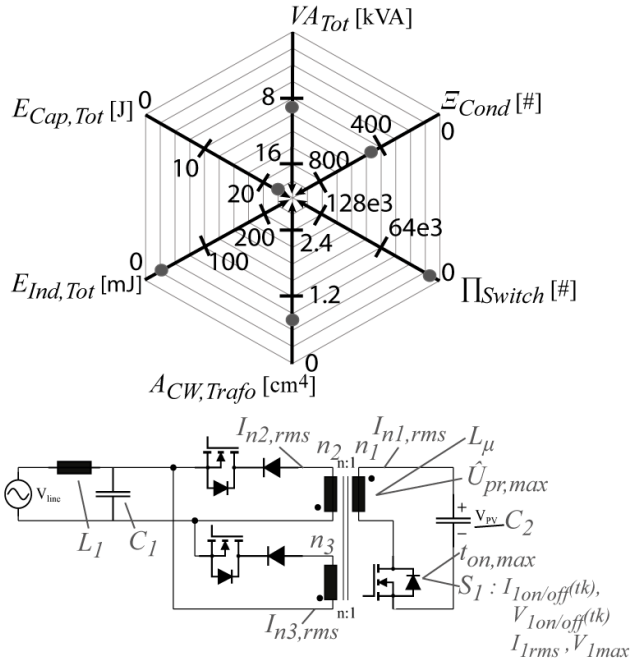


Figure 2.18: Example topology characteristic of the single transistor flyback: spider-plot of the six bench marking factors with inverse axis.

in figure 2.19.
Figure 2.20 shows the spider plot of the various compared topologies. Three topologies are omitted in the plot for the sake of clarity.

The pseudo DC-link resonant flyback topology (*ID: IV*) is found to feature high efficiency of the semiconductors. In addition, it also exhibits relatively small values for the total semiconductor rating, transformer-size and inductance energy. In comparison to the BCM flyback topology (*ID: III*), it can be seen that the paralleling of the flyback stages brings significant advantages regarding the stored inductive energy and the conduction losses. It results a well balanced topology characteristic with high semiconductor performance and reasonable implementation

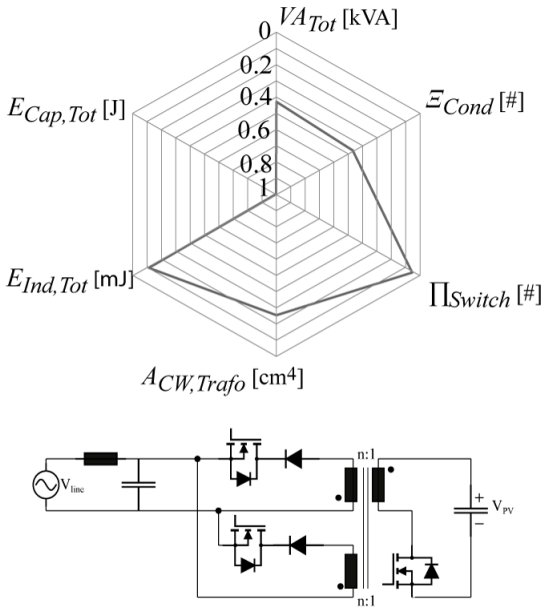


Figure 2.19: Example topology characteristic of the single transistor flyback. Each bench marking factor is normalized to the highest value among the compared topologies (single transistor flyback has highest $E_{Cap,Tot}$).

effort for the passive components. This also agrees with the fact, that this topology is reported to have outstanding efficiency and is applied in a commercial AC-module inverter (see section 2.3.3). An alternative topology, which achieves a comparable performance, is the HF-link LC-resonant & cyclo topology (*ID: I*). The resonance converter operating principle brings along an even smaller transformer factor than the resonant flyback topology and also allows for zero voltage switching. Unlike the resonant flyback topology, this topology does not suffer from additional, not considered losses caused by the transformer leakage inductance. This would probably compensate the somewhat higher conduction loss factor in a real system. The HF-link LC-resonant & cyclo topology is in addition capable of delivering reactive power. The draw back of these two topologies are their high capacitive energy value,

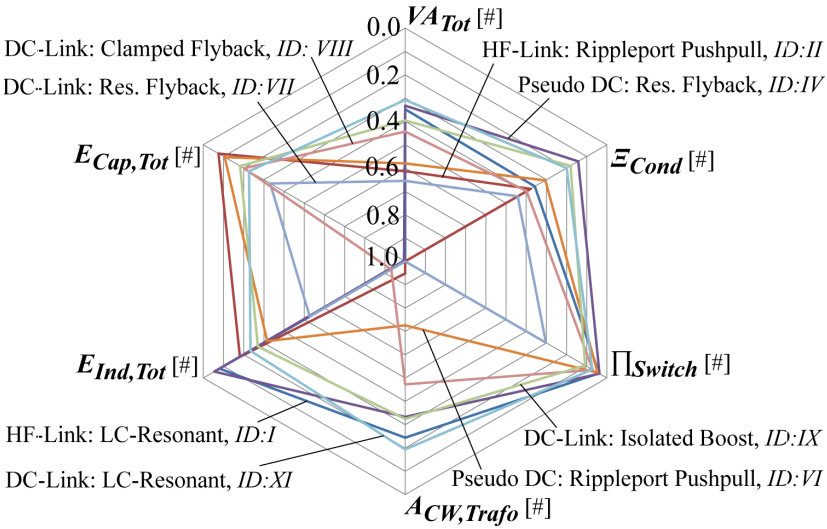


Figure 2.20: AC-module topology comparison: the six bench marking factors of the compared topologies plotted on an normed six-axis spider plot.

which is due to the passive capacitive power decoupling realized with large electrolyte capacitors on the PV-side.
Some of the compared topologies apply active power decoupling to overcome this drawback. Though it can be clearly seen, that power decoupling is achieved at the expense of reduced performance. The HF-link rippleport push-pull topology (*ID: II*) realizes very low stored capacitive energy by active integrated power decoupling. But the topology suffers from a very high switching loss factor, a high transformer size and relatively high installed semiconductor power. Also the pseudo DC-link flyback topology with ripple port (*ID: V*) exhibits a very high installed semiconductor power and conduction loss factor. The pseudo DC-link push-pull topology with rippleport (*ID: VI*) features a more balanced characteristic, but still exhibits a relatively high installed semiconductor power, transformer size and inductor size. Nevertheless among the compared topologies, it is the most attractive topology featuring active power decoupling.
Alternatively to the topologies with a rippleport, the DC-link topologies provide power decoupling at the intermediate DC-link. The two DC-

link topologies with a resonant flyback (*ID: VII*) and with a clamped flyback (*ID:VIII*), actually operated as kind of resonance converters with fixed switching frequency, suffer from high resonance currents. This leads to an increased conduction losses factor, transformer factor and inductance energy factor. The DC-link topology with an LC resonant boost converter (*ID: XI*) shows the most balanced characteristic with low bench marking factors in the same range as the pseudo DC-link resonant flyback topology (*ID: IV*) and the HF-link LC-resonant & cyclo topology (*ID: I*). All considered DC-link topologies apply a fullbridge PWM inverter between the DC-link and the grid. This fullbridge converter operates in hard switched mode, whereas most of the other compared topologies operate with ZVS. For the calculation of the switching loss factor it can not be distinguished between soft switching and hard switching. This is an inherent drawback of the definition of the switching loss factor, using only electrical parameters. The DC-link topologies are therefore subject to additional not considered switching losses, which would reduce the system performance relatively to the other compared topologies.

The topology comparison reveals the following conclusions. The first and most important decision, when designing an AC-module converter, is wether electrolytic capacitors are an acceptable component to be used or not.
If so, passive capacitive power decoupling can be applied at the PV-input side and a single stage topology can be chosen. Among these, the pseudo DC-link resonant flyback converter (*ID: IV*) with 3 paralleled flyback stages features minimal semiconductor part-count and a proven high performance. The comparison further identifies the HF-link LC-resonant & cyclo topology (*ID: I*) as a second very interesting candidate for an AC-module. It features comparable performance as the flyback topology and is in addition capable of delivering reactive power.
If it is decided, that electrolytic capacitors are not an option, then passive capacitive power decoupling can not be applied, due to the reduced energy-density and the high cost of alternative capacitor technologies. This decision will inherently lead to a system with reduced system performance, due to increased switching and conduction losses. There are two approaches to provide the necessary power decoupling. First with a ripple-port and second with a two stage topology and an intermediate DC-link. The two stage DC-link approach applying an LC resonant

boost converter and a PWM fullbridge shows to be the most promising candidate. Though the PWM fullbridge operates under hard switched operation, actually causing higher switching losses than anticipated by the applied switching loss factor. The challenge when designing an AC-module converter with a DC-link topology is therefore to implement an efficient fullbridge converter with ultra low switching losses. Though new high efficient wide band gap semiconductor devices would be a promising choice to master this challenge.

2.4 Multi-Input Converters - Topologies and Comparison

Unlike the single-input converters, the multi-input AC module converters track the MPP on each PV-substring as illustrated in fig. 2.21. In this way the power can be extracted more effectively from the PV-module, whereas single-input converters fail to extract the maximum power from the PV-module for certain unbalanced operating conditions of the three substrings (see chapter 1).
The substring MPPT concepts proposed in literature as well as the commercially available products are to the knowledge of the author solely based on DC to DC module integrated converters [19], [51], [52], [13]. In the following section of this work MPPT on substring level is extended to AC-module converters. The various approaches to realize such a converter are analyzed and compared.

2.4.1 Categorization of Realisation Possibilities

The AC-module converter topologies with three MPP tracking inputs on substring-level (3xMPPT) are categorized by the realization of the galvanic isolation. The galvanic isolation can be either realized by three two-port transformers, one multi-port transformer or one two-port transformer with a non-isolated multi-port stage on the PV-input side. This allows to distinguish the three types of topologies shown in figure 2.22. The galvanic isolation is in any case realized with a high-frequency transformer. A line-transformer is not considered as an option for obvious reasons. Within each of these three categories, the

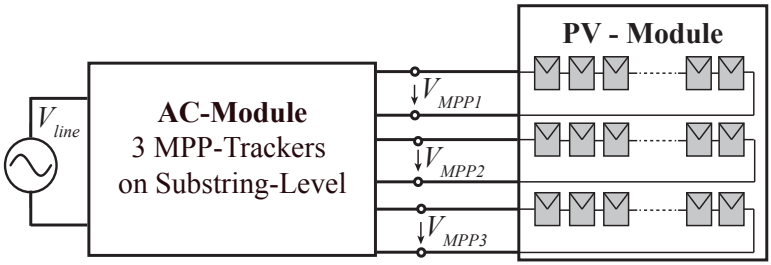


Figure 2.21: Multi-input AC module converter with three inputs for substring level MPP tracking.

topologies can be distinguished in the same manner as for the normal, one-port AC-modules (see section 2.2):

3x 2-Port Transformer: This type of multi-input converter can be realized in two ways. Firstly by simply applying three single-port AC-module topologies and connecting them either in parallel or in series. Secondly a DC-link topology with three paralleled or serial DC-DC converters and one DC-AC inverter. For the DC-link topology power decoupling is best realized with passive capacitive decoupling at the DC-link.

1x Multi-Port Transformer: The multi port transformer can be combined with all system concepts: DC-link, pseudo DC-link and HF-link. The realization with a DC-link is a part-count reduced version of the topology applying three paralleled DC-DC converters. Both, the pseudo DC-link and the HF-link inverters, can be realized with passive capacitive decoupling at PV-side or active decoupling at an additional ripple port.
The multi-port transformer topologies achieve reduced semiconductor part-count, but come along with very high design and control complexity. The investigation of appropriate modulation and control schemes would require substantial effort.

1x 2-Port Transformer and Multi-Port Stage: A non-isolated multiport stage is applied, which features MPP-tracking at each of its three inputs and one single DC output. The multiport stage is combined with any single-input AC module converter. Two

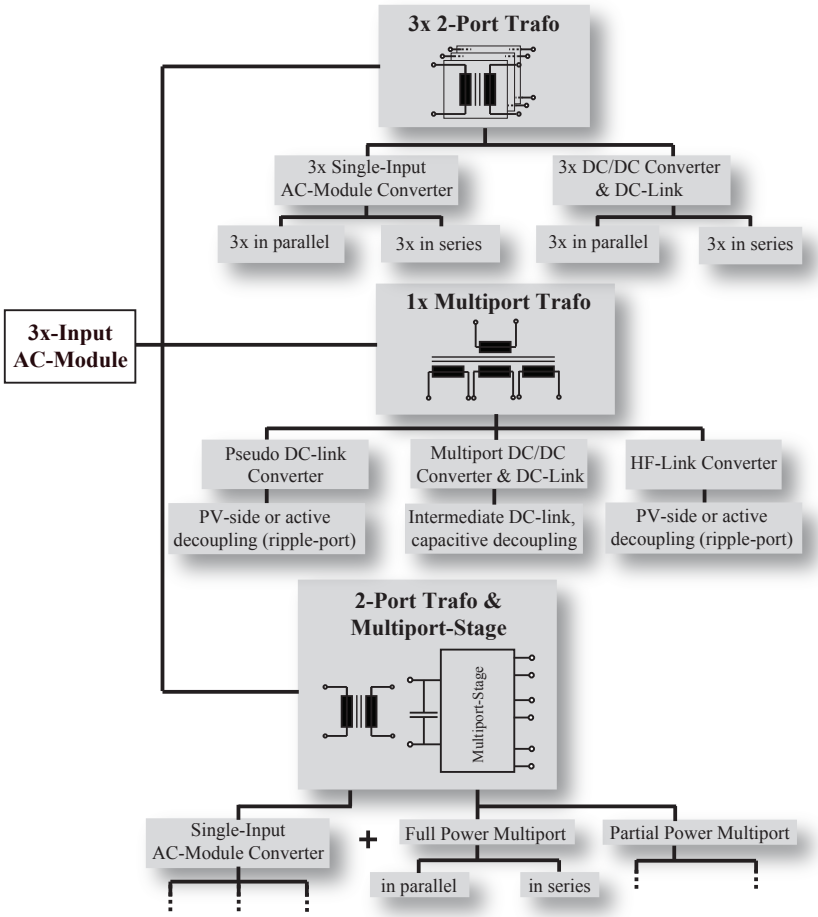


Figure 2.22: Overview of the realisation possibilities for an AC-module with 3 MPP-trackers on substring-level.

different system concepts can be distinguished based on the functionality of the DC-DC multiport stage.
First the DC-DC multiport can be designed as pure power-balancer with an output voltage equal to the sum of all substring voltages. In case of unshaded conditions the power-balancer is not active and does not cause additional losses. Further the voltage step-up

ratio of the single-input AC-module converter is the same as for single MPP tracking on PV-module level.
Second the DC-DC multiport can be implemented as buck-boost converter, which is controlled to a set output voltage. In this case the DC-DC multiport can feature the additional functionality of power-decoupling at its output capacitor.
An overview of PV multi port DC-DC converters and power-balancers is given in [53] and [19],[51].

2.4.2 Feasible Topology Candidates

Compared to a single-input AC-module converter with MPP tracking on PV-module level, a multi-input AC-module with MPP-tracking on substring-level comes along with the following drawbacks:

- *Increased part count:* Three separate inputs demand for more active and passive components, such as semiconductors, gate-drivers, auxiliary supplies and magnetic components. This causes not only increased costs, but also leads to reduced reliability and reduced low-load efficiency due to increased quiescent supply currents.

- *Higher voltage step-up ratio:* The voltage range of the substring MPPT inputs is one third of the PV module voltage range, requiering a three times higher voltage step-up ratio. This has a negative impact on the achievable converter efficiency and leads to a higher influence of converter parasitics, such as semiconductor output capacitances and transformer parasitics.

When selecting a topology for a multi-input AC-module it must therefore be taken care, that the advantage of substring MPPT is not overcompensated by the above mentioned system drawbacks. For the topology selection this has the consequence, that only topologies with a reasonable amount of semiconductors are considered. An upper limit of 16 switches is set, which corresponds to twice the amount of most of the single-input AC-module topologies.
In the following, promising multi-input topologies are derived, taking into account the results of the comparison for single-input topologies in section 2.3.5.

3x 2-Port Transformer: The application of three separate single-input converters requires a high amount of semiconductors. Therefore only a pseudo DC-link inverter with one common unfolder is an option. Among these, the pseudo DC-link resonant flyback topology exhibits the best performance (see sec.2.3.5). Another feasible system is a DC-link topology with a PWM fullbrdige and three paralleled or serial DC-DC converters. The comparison in sec.2.3.5 identified the LC-resonant converters to be a good choice for the DC-DC converters. Though a fullbridge on each of the three inputs is thought to cause a too high semiconductor and auxiliary circuit parts-count. In order to reduce the amount of switches a DC-DC flyback topology is chosen for the three DC-DC converters.

1x Multi-Port Transformer: There is only one topology, which does not require an excessive amount of switches. A DC-link topology with a PWM fullbridge and a four-port flyback transformer.

1x 2-Port Transformer and Multi-Port Stage: In a system with a buck-boost DC-DC multi-port stage and a HF-link or pseudo DC-link AC-module converter, the DC-DC multi-port stage causes a substantial amount of the overall system losses [54],[55]. A power-balancer multi-port stage does not cause substantial losses in balanced conditions. Therefore a power-balancer multi-port stage seems to be the best choice. It is most favorable combined with a HF-link LC-resonant AC-module topology, which features a good overall system performance and in addition reactive power capability (see sec.2.3.5).

The following subsections describe the topology candidates more in detail.

Pseudo DC-link with parallel Flyback DC-AC (*Top.-ID: A*)

Three paralleled flyback DC-AC converters are operated to output a rectified sine-waveform current. A common unfolding bridge folds the current waveforms to the correct line voltage polarity. Except the lower input voltage, the paralleled stages are operated exactly as the single-input AC-module converter described in section 2.3.2 and shown in fig. 2.14.

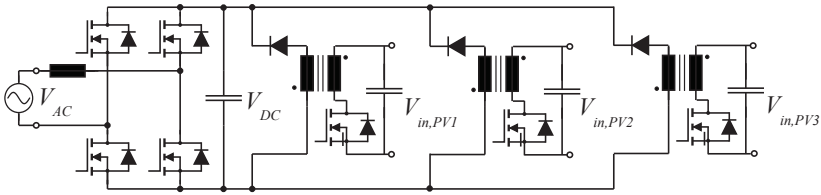


Figure 2.23: 3x2Port Transformer Topology: three paralleled Flyback DC-DC converters and a PWM full bridge inverter (*Top.-ID: B*).

Parallel Flyback DC-DC & PWM Fullbridge (*Top.-ID: B*)

Figure 2.23 shows the paralleled flyback DC-DC & PWM fullbridge topology. Three paralleled Flyback DC-DC converters, operating in boundary conduction mode (BCM), deliver the DC-power from the PV substrings into the DC-link. The DC-link serves as energy-buffer for power decoupling. A PWM full bridge inverter with an LCL line-filter feeds the PV-power into the grid.

Serial Flyback DC-DC & PWM Fullbridge (*Top.-ID: C*)

The topology is shown in figure 2.24. Three Flyback DC-DC converters in DCM, are put in series to feed into a DC-link, as shown in fig. 2.24. The operating conditions (power, voltage step-up ratio) under different shading conditions are given in section D.1. Again the DC-link serves as energy-buffer for power decoupling and a PWM full bridge inverter with an LCL line-filter feeds the PV-power into the grid.

Multiport sequential Flyback DC-DC & PWM Fullbridge (*Top.-ID: D*)

A Flyback multiport converter is used for delivering the power from the PV substrings to the DC-link. The flyback transformer has three PV-side input ports and one output port on the DC-link side. The flyback converter operates in DCM and the three input ports are operated sequentially one after another. Hence the effective switching frequency seen on the DC-link output side is three-times higher than the flyback-switching frequency. The DC-link serves as energy-buffer for power

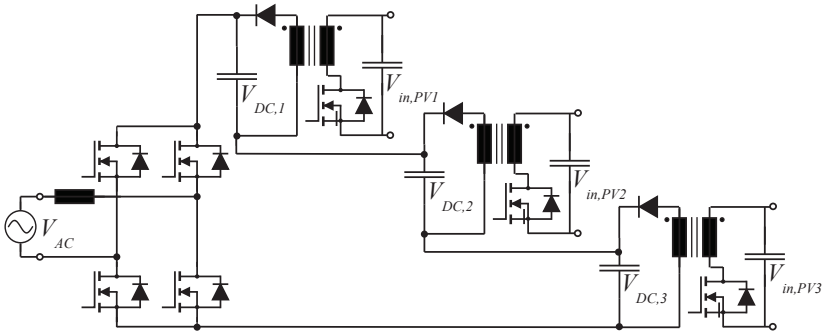


Figure 2.24: 3x2Port Transformer Topology: three serial Flyback DC-DC converters and a PWM full bridge inverter (*Top.-ID: C*).

decoupling and a PWM full bridge inverter with an LCL line-filter feeds the PV-power into the grid.

Power-Balancer Multiport & HF-link LC Resonant Converter (*Top.-ID: E*)

A power-balancer circuit as proposed in [52] is combined with the single-input HF-link LC-resonant converter described in section 2.3.1 and shown in fig.2.3.

2.4.3 Rough Comparison Topology Candidates

To evaluate the performance of the proposed multi-input AC-module converter topologies, again a systematic topology comparison is performed. The same topology comparison approach as for the single-input topologies is applied. It is based on six benchmarking factors and a system design of each topology for the common system specification in table 2.4. In accordance to the single-input topology comparison in sec. 2.3.5, a switching frequency of 20kHz is assumed for DC-AC inverters and the DC-DC converters are assumed to operate at a switching frequency of 40kHz. Even though the switching frequencies are selected without an optimization, their exact values do not greatly alter the relative results of the topology comparison, because all compared topologies rely on the same switching frequencies. The comparison method and

Table 2.4: Specifications and assumptions for the performed system design for 3xMPPT topologies, based on the multi-input AC-module converter specification in table 1.1.

Specifications:	Power:	P_{Nom}=300W
	MPP-Tracking:	3xMPPT on substring level
	PV Input Range:	3x - $V_{PV,in}$=8.5-21V
	Input Voltage Ripple:	$k_{PV,Europ} \geq$0.998
	Line Voltage:	V_{line}: 230Vrms/50Hz
	Line Current Ripple:	$\hat{I}_{f,switch} \leq 0.05 \cdot \hat{I}_{1,p_{nom}}$
Assumptions:	Switching frequency:	DC-AC inverter $f_{s,AC}$=20kHz DC-DC converter $f_{s,DC}$=40kHz Variable $f_{s,avg} = f_{s,DC}$ resp. $f_{s,AC}$
	DC-DC Conv. current:	For CCM $i\Delta_{p,p} \leq 0.2 \cdot I_{DC,rms}$
	Stand-By Reactive Power:	$Q_{noload,max}$=8VA (0.03 P_{nom})
	Flyback Transformer Ratio:	low primary switch voltage-stress [25] $V_{prim,min} \cdot \frac{N_{sec}}{N_{prim}} \simeq 0.3 \cdot V_{sec,max}$
	Power Decoupling:	$\Delta_{V\,dc,pp} = 0.25 V_{dc,avg}$ [42]

Table 2.5: Multi-input AC-module topology comparison: Calculated benchmarking factors. The best values of each category are the minima, which are marked in bold.

ID:	VA_{Tot}	Ξ_{Cond}	Π_{Switch}	$A_{CW,trafo}$	$E_{Ind,Tot}$	$E_{Cap,Tot}$
A	4.89E+3	2.23E+2	**2.25E+3**	2.32E-8	**1.37E-2**	1.25E+1
B	**4.88E+3**	**1.49E+2**	9.49E+3	1.68E-8	6.41E-2	**2.29**
C	5.03E+3	1.58E+2	6.66E+3	**1.67E-8**	6.41E-2	2.35
D	7.40E+3	4.44E+2	1.53E+4	2.26E-8	6.41E-2	2.35
E	5.68E+3	2.05E+2	4.19E+3	1.70E-8	2.01E-2	1.25E+1

the assumptions made for the system design are described in detail in sec. 2.3.5.

The calculated benchmarking factors for the five multi-input topologies are listed in table 2.5. In the same way as in sec. 2.3.5 the benchmarking factors are plotted on a spider plot with inverted axes, shown in fig.2.25. The benchmarking factors are normalized to the maximal values among all topologies compared in this work, the multi-input topologies as well as the single-input topologies in table 2.3. The serial flyback DC-DC topology (*ID. C*) exhibits similar benchmarking

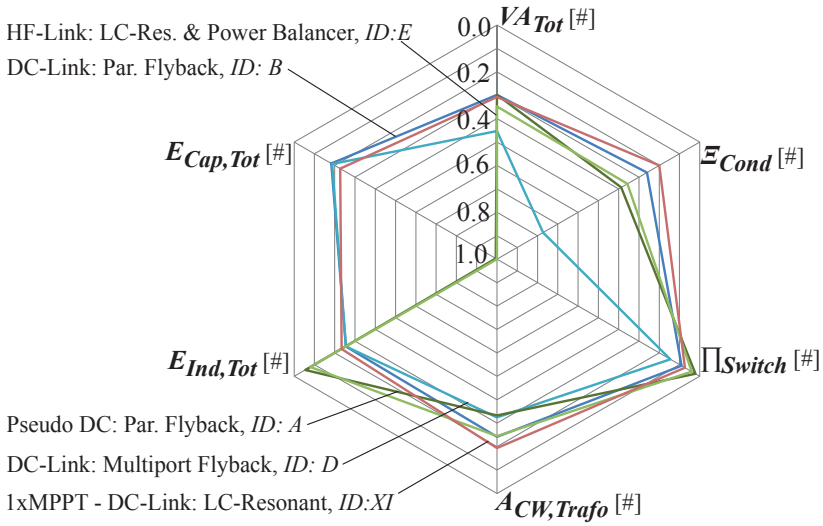


Figure 2.25: Comparison of topology candidates with 3xMPPT from section 2.4.2.

factors as the parallel flyback DC-DC topology (*ID. B*) and is therefore omitted in fig. 2.25. In addition to the multi-input topologies also a single-input topology, the DC-link LC resonant boost topology (*ID: XI*), is shown in the figure.

The multiport sequential flyback DC-DC topology (*ID: D*) exhibits the worst performance. Due to the sequential operation of the three inputs, the converter exhibits higher peak currents than the paralleled or serial flybacks. This increases the semiconductor rating, the conduction losses, the switching losses and the transformer size.
The pseudo DC-link topology with paralleled DC-AC flyback converters (*ID: A*) and the power-balancer multiport with a HF-link LC resonant converter (*ID: E*) feature a small stored inductive energy, a small transformer size and a good semiconductor performance. Power-decoupling is realized with PV-side passive capacitive power-decoupling (sec. 2.1), requiring the application of electrolytic capacitors. Both topologies operate under ZVS conditions. However the flyback topology is subject to additional not considered switching losses, caused by the transformer leakage inductance. The LC-resonant topology is in addition capable

of delivering reactive power. Further the voltage step-up ratio of the LC-resonant converter is the same as for the single-input topologies, thanks to the power-balancer multiport. This makes the LC-resonant topology the preferable choice among these two topologies.
The DC-link topology with paralleled flyback DC-DC converters (*ID: B*) features power decoupling at the DC-link, which enables a much smaller capacitive energy storage. Also the other benchmakring factors are relatively small, confirming an overall good performance of the DC-link topology with flyback DC-DC converters. Figure 2.25 contains as a benchmark the most favorable single-input DC-link topology, being the DC-link LC-resonant topology (*ID: XI*). The multi-input flyback topology exhibits comparable values of the benchmarking factors as the single-input topology. However the multi-input topology will suffer from reduced performance due to the three times increased voltage step-up ratio and switching losses caused by the leakage-inductance. The serial connection of the DC-DC converters (*ID: C*) exhibits slightly better benchmarking factors than the parallel connected DC-DC converters (see table 2.5). Especially the switching loss factor is reduced by a factor one and a half. Though as derived in appendix D.1, the series connection requires a very wide voltage step-up range. For a practical flyback converter design, ZVS could not be achieved for low step-up ratios. This greatly increases switching losses at low output power. In contrary the parallel connected flyback DC-DC converters can achieve ZVS over the whole load range and therefore achieves lower switching losses at low output power. Further a parallel connection features an easier control and design of the converters. For these reasons parallel connection of the flyback DC-DC converters (*ID: B*) is the preferred topology.

In summary the comparison reveals two distinct approaches to realize the multi-input converter. Which one is favorable depends again on the fundamental question, if power decoupling may be realized with electrolyte capacitors (see sec. 2.3.5).
If electrolyte capacitors may be used, then the power-balancer multiport topology with a HF-link LC-resonant converter (*ID: E*) is the best choice. Power decoupling can be realized by passive capacitive decoupling at the output of the multiport stage.
If electrolyte capacitors are not allowed, then a DC-link topology is applied with power-decoupling at the DC-link. The topology with paral-

leled flyback DC-DC converters and a PWM fullbridge (*ID: B*) appears to be the preferred DC-link topology. As discussed in sec. 2.3.5 for the single-input topologies, the main challenge for the implementation of an AC-module converter with a DC-link topology is to achieve an efficient fullbridge converter stage featuring very low switching losses.

2.4.4 Advanced Flyback DC-DC Stages for DC-link Multi-Input Converters

The comparison performed in section 2.4.3 showed, that the DC-link topology with three paralleled DC-DC flyback converters and a PWM fullbridge converter is an interesting candidate for a multi-input AC-module converter. In the following section different options to improve the performance of the DC-DC flyback stage are investigated and compared based on a more detailed converter loss model.

Active Clamp Resonant Flyback Converter

The flyback converter has two main issues. Firstly the energy stored in the leakage inductance can not be transferred to the output-side and causes additional losses at the turn-off of the input-side switch. Secondly the whole energy transferred to the output is temporarily stored in the flyback transformer, which requires a sufficient cross-sectional core area in order to avoid saturation of the magnetic flux. The LC resonant DC-DC converter does not have these drawbacks and therefore theoretically would allow for lower switching losses and a more compact transformer. The comparison of the single-input topologies (sec. 2.3.5) confirmed the good performance of the LC-resonant DC-DC converter. However three paralleled resonance converters, requiring each a fullbridge on the input-side, are considered to cause a too high semiconductor and auxiliary-circuits parts-count. An alternative with lower part-count is the active clamp resonant flyback converter shown in figure 2.12 and described in sec. 2.3.2, [34]. It requires only two active switches and two diodes and achieves resonant operation in a similar way as the LC-resonance converter. It is therefore considered as a viable alternative to the DC-DC flyback converter.

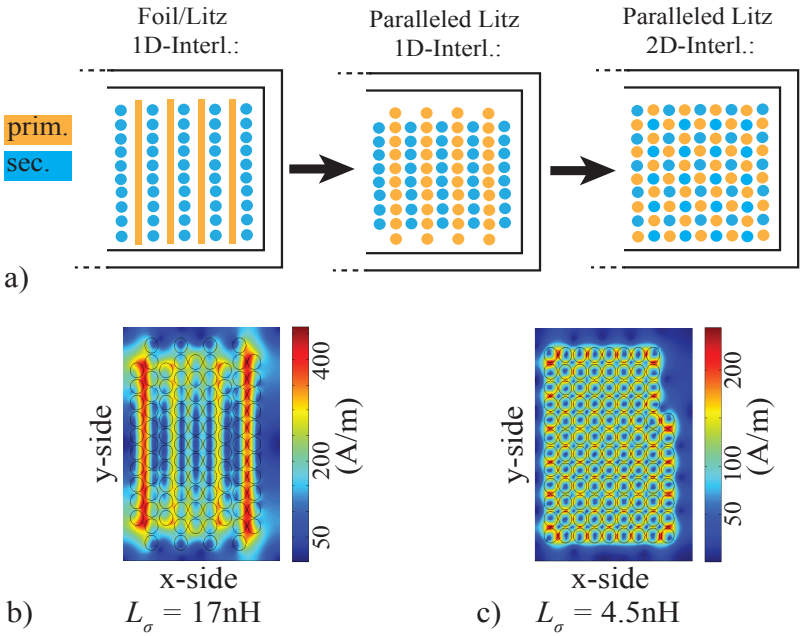


Figure 2.26: a) from 1D- to paralleled wires 2D-interleaving, b) 1D full interleaving magnetic leakage field in winding window, c) advanced 2D interleaving magnetic leakage field in winding window

2D Transformer Winding Interleaving

Another way to tackle the issue with the leakage inductance is an advanced transformer setup with improved arrangement of the windings. The transformer for a high step-up flyback converter with the given specification typically exhibits a primary turns number in the range of N_1=2..6 and a transformer ratio of n=10..15. To keep the leakage inductance low, a foil winding is normally applied for the primary winding and litz-wire is used for the secondary winding. Figure 2.26a) schematically shows the arrangement of the primary and secondary windings in the winding window for N_1=4 and n=12.5. The left hand side of fig. 2.26a) shows the maximally possible interleaving with foil and litz wire windings. The windings are wound around the vertical axis. As

the primary and secondary are fully interleaved on the horizontal axis, this interleaving structure is denoted as full 1D interleaving. If the primary foil winding is replaced by paralleled round-conductors or litz wires, the windings can be interleaved on the horizontal, as well as the vertical axis. This arrangement is shown on the right hand side of fig. 2.26a) and is denoted as 2D interleaving. The 2D interleaving greatly reduces the magnetic leakage field in the winding window, as shown in fig. 2.26b) and c). This reduces the leakage inductance by nearly a factor four, compared to full 1D interleaving. The challenge is the mechanical realisation and manufacturing of such 2D interleaving. Further, a higher degree of interleaving increases the interwinding capacitances. Consequently the smaller leakage inductance comes at the expense of increased winding capacitances.
The practical realisation of a 2D interleaved flyback transformer is derived in section A.3. Measurements on the built transformer prototype showed, that the imperfections of the wiring and non-ideal placement of the windings contribute to an additional inductance of 24nH. The built transformer prototype achieves a total leakage inductance of 30nH, instead of the ideal 6nH. Whether such a transformer winding is still advantageous compared to conventional 1D interleaving, needs to be evaluated based on a converter-level loss optimization.

Fine comparison

The above discussed approaches to improve the flyback DC-DC stage are compared to the conventional flyback converter with 1D interleaving. The comparison is based on a complete converter optimization for each approach. The applied converter optimization routine as well as the loss models are described in detail in the separate section 5.1. To reduce the calculation time of the comparison, the optimization routine is simplified in the following way:

- *Ideal Converter Waveforms:* The operating waveforms of the flyback transformer are assumed to be ideal, hence the influence of the transformer parasitic elements and the semiconductor output capacitances on the operating waveforms are neglected
- *Fixed Transformer Cores:* The transformer core is fixed to the following three standard core shapes from the manufacturer Epcos: RM10LP , RM12LP and RM14LP. SiFerrite N49 from Epcos is chosen as core material.

Table 2.6: Fine comparison DC-DC converter specification.

Output Power:	P_{nom}=100W
Input Voltage:	V_{in}=12V
DC-link Voltage:	V_{DC}=400V
Ambient Temperature:	T_{amb}=30°C
Max. Transformer Temperature:	$T_{trafo,max}$=100°C

- *Constant DC-link Voltage:* The DC-link on the output of the flyback converter is assumed to be constant. A possible ripple of the DC-link voltage due to power decoupling is neglected.
- *Worst Case Temperature:* A simplified thermal model is applied. For the calculation of the semiconductor and the magnetic losses the worst case temperature, hence the specified maximal temperature $T_{trafo,max}$, is assumed.

The common converter specification, serving as input to the optimization routine, is listed in table 2.6. The optimization results are illustrated in figure 2.27, where the European efficiency is plotted for the three core sizes. Five different DC-DC converter configurations are investigated. The normal flyback converter with foil and a freely optimized 1D interleaving structure, serves as benchmark for the comparison. It is named 'Flyback - Foil 1D multiple interl.' in fig. 2.27.
If the interleaving is not freely optimized, but constrained to a single interleaving with an 'sps' structure, the efficiency decreases for the smaller core sizes. With increasing core size it approaches the efficiency achieved with multiple interleaving.
The active clamp resonant flyback converter with freely optimized 1D interleaving exhibits lower efficiency than the normal flyback with multiple interleaving. Though the converter performs better with increasing core size. With an RM14 core it nearly reaches the same efficiency as the benchmark flyback converter. Additional optimization runs at an increased core-volume showed, that the active clamp resonant flyback slightly outperforms the benchmark flyback converter. However the increase in efficiency is within the modelling inaccuracy and does therefore not justify the increased semiconductor and auxiliary-circuits partcount. A detailed analysis of the optimization results further revealed, that the active clamp resonant flyback converter features outstanding efficiency for a single operating point, but can not achieve decent effi-

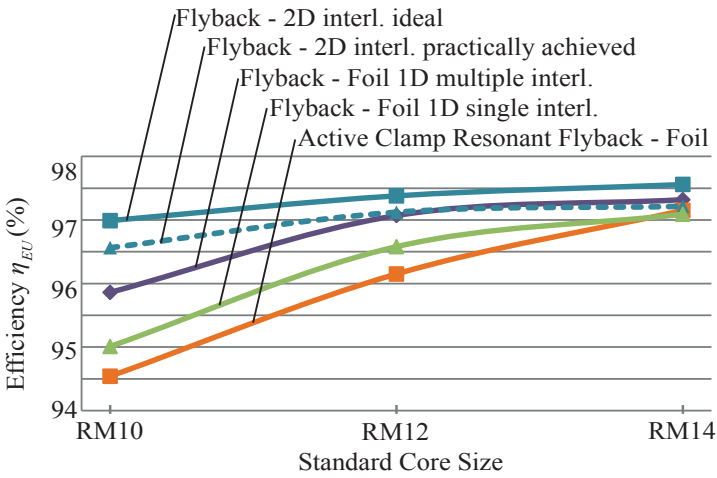


Figure 2.27: Fine comparison of advanced flyback DC-DC stages.

ciency at varying operating points.
The flyback converter with a 2D interleaved transformer winding, would ideally allow for an increased efficiency, compared to the benchmark flyback converter with 1D interleaving. Though the built 2D interleaved prototype transformer achieves a leakage inductance, which is 24nH higher, than predicted under ideal conditions. If the practically achieved leakage inductance is taken into account, the converter efficiency decreases. At the smallest core size the 2D interleaving still features higher efficiency than 1D interleaving. Though with an RM12 and RM14 core the 2D and 1D interleaving allow for approximately the same efficiency.

It can be concluded, that the proposed approaches to improve the efficiency of the DC-DC flyback converter do not achieve a substantial increase in efficiency. The standard flyback converter with foil windings on the primary-side and 1D multiple interleaving appears to feature the best performance at minimal part-count and reasonable transformer manufacturing complexity.

2.5 Selected Two Stage Multi Input Converter Topology

The analysis and comparison of the multi-input converter topologies in the preceding section revealed two attractive topologies. First the power-balancer multiport topology with a HF-link LC-resonant converter and the DC-link topology with paralleled Flyback DC-DC converters and a PWM fullbridge DC-AC stage (sec. 2.4.2, *ID: E* and *ID: B*).
The multiport topology actually corresponds to a combination of a conventional single-input AC-module converter and a power-balancer DC-DC converter. Hence a conventional single-input AC-module would have to be designed, with the goal of outperforming the state of the art AC-module converters. The advantage of this approach is, that it does not have any system inherent drawbacks compared to a single-input AC-module and can achieve a comparable performance level.
On the other hand, the DC-link topology additionally features power decoupling at the DC-link, which allows to greatly reduce the capacitor size. This is advantageous concerning converter reliability and cost. Though compared to single-input AC-modules, this topology has the inherent drawback of a three times higher step-up ratio of the DC-DC stage. Further the DC-AC PWM fullbridge operates hard switched. Applying conventional semiconductors, such as MOSFETs and IGBTs, it is therefore hard to compete with soft-switched AC-module topologies. Newly available GaN-based power semiconductors feature much improved hard switching performance, compared to MOSFETs or IGBTs. Compared to soft switching, the drawback of hard switching becomes less significant. With the application of GaN devices, the performance of a hard switched DC-link could possibly compete with soft switched AC-modules. If so, this would result in a very attractive AC-module topology.

Even though for this work the use of electrolyte capacitors is considered as a viable option, the DC-link topology with three paralleled flyback converters (fig. 2.23) is finally chosen for the following reasons:

- The DC-link topology features a much reduced power-decoupling capacitor, overcoming a main drawback of the conventional HF-link and pseudo DC-link AC-module topologies.

- The newly available GaN devices promise unprecedented hard switching performance. It is therefore very interesting to investigate, to which level the efficiency of the hard switched fullbridge and consequently the efficiency of the whole multi-input AC-module converter can be pushed.

2.5.1 Two Stage Converter Control and Operating Principle

The input side DC-power from the three PV-substrings is delivered to the DC-link by three paralleled high step-up Flyback-converters. The bottom of fig. 2.28 shows the current, voltage and power waveforms of one substring input at a nominal output power of 100W. From the DC-link a PWM fullbridge converter delivers AC-power to the grid. The grid-side output waveforms are shown on the top of fig. 2.28. The DC-link decouples the 100Hz pulsating line-power from the DC-power delivered by the PV substrings. Depending on the instantaneous line-power, the excess or lacking energy is temporarily buffered in or taken from the DC-link. Consequently the voltage V_{DC} exihibits a sinusoidal 100Hz ripple $\Delta_{V_{DC}}$ overlaid to the average DC-link voltage $\overline{V}_{DC}$, as shown in fig. 2.28. The ripple $\Delta_{V_{DC}}$ depends on the output power and the size of the DC-link capacitor. With an appropriate controller, $\Delta_{V_{DC}}$ can be as high as 50V, allowing for a reduced capacitor size [20]. This kind of power decoupling at the intermediate DC-link is described in detail in [56], including the design of the DC-link capacitor and the implementation of the appropriate controller.

Fig. 2.29a) shows the block diagram of the implemented DC-AC stage controller. It is based on the standard control structure commonly applied for single-phase grid-tied converters: a phase locked loop (PLL) for grid synchronization, a PI control-loop for V_{DC} and an underlaying PI control-loop for I_{line} in combination with a current feed-forward. For fast response to load changes, the DC-link controller bandwidth must be well above the line frequency. Consequently, the DC-link ripple needs to be estimated and used to form a time-dependent reference voltage $V_{DC,ref}(t)$. The ripple estimator is implemented according to [56]. It estimates $\Delta_{V_{DC}}$ based on the grid voltage V_g, the grid phase φ_g, the reference line current, the DC-link average reference voltage $\bar{V}_{DC,ref}$ and the DC-link capacitance. The implemented control scheme successfully decouples the DC from the AC power with a maximal ripple of

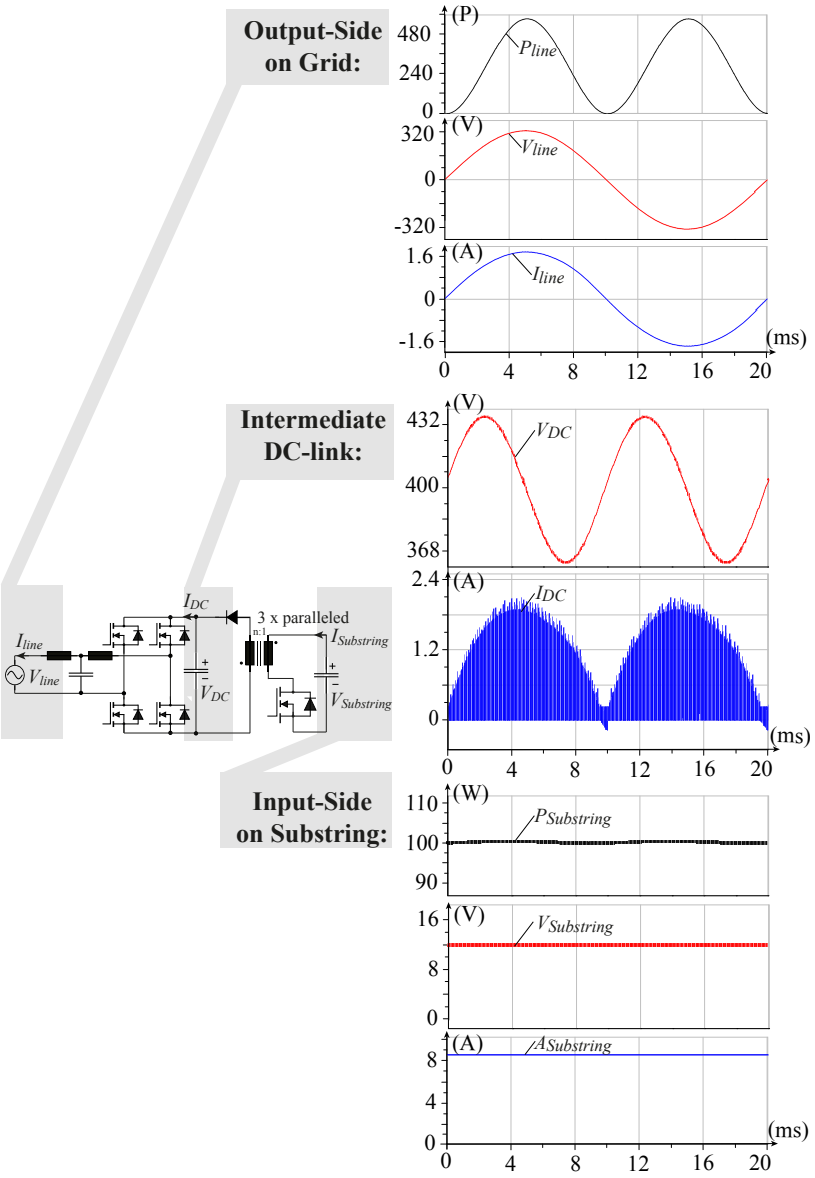


Figure 2.28: Two stage multi-input converter topology: simulated operating waveforms at 300W output power and C_{DC}=30uF

$\Delta_{V_{DC}}$=45V at 300W output power and a DC-link capacitance of $30\mu F$.

The PWM fullbridge is operated in so called single-phase chopping mode. Unlike for unipolar or bipolar modulation [57], in single-phase chopping mode one halfbridge is operated at high switching frequency to control the current through the inductor L_{inv} and the other halfbridge is switched at line-frequency. This allows to design a simpler gate drive and apply lower cost semiconductors for the low frequency halfbridge.
The three paralleled flyback converters of the DC-DC stage are operated in boundary conduction mode (BCM) or discontinuous conduction mode (DCM). In these operating modes the flyback converter behaves as an on-time controlled current-source [25]. Therefore each PV substring voltage can be controlled by means of a simple PI voltage control-loop, as shown in fig. 2.29b). In BCM the end of a switching period must be detected, which is achieved by a voltage-comparator circuit generating the signal b_{zvs}. With a typical flyback switching frequency in the range of 20-100kHz, the voltage controller bandwidth can be chosen above 1kHz. Thanks to the high controller bandwidth, the 100Hz ripple in the DC-link voltage is easily compensated by the controller and is not transmitted to the PV-substring voltage.

When connected to a PV-panel, the paralleled DC-DC converters must perform MPPT on the three substring inputs. This can be realized with a current and voltage measurement at the input of each substring. The MPPT algorithm calculates the instantaneous power from the measured current and voltage and sets the voltage reference $V_{substring,ref}$. To reduce the number of voltage and current sensors, unified MPPT control can be applied as proposed in [58]. This advanced MPPT control only requires one current sensor and one voltage sensor at the common output to the DC-link. A time sequential MPPT algorithm is applied to track the three individual MPPs. Due to the current-source behaviour of the flyback converter, the substring voltage must not be controlled directly. Instead the MPPT algorithm can directly set the converter on-time t_{on}, such that no input-side sensor is required.

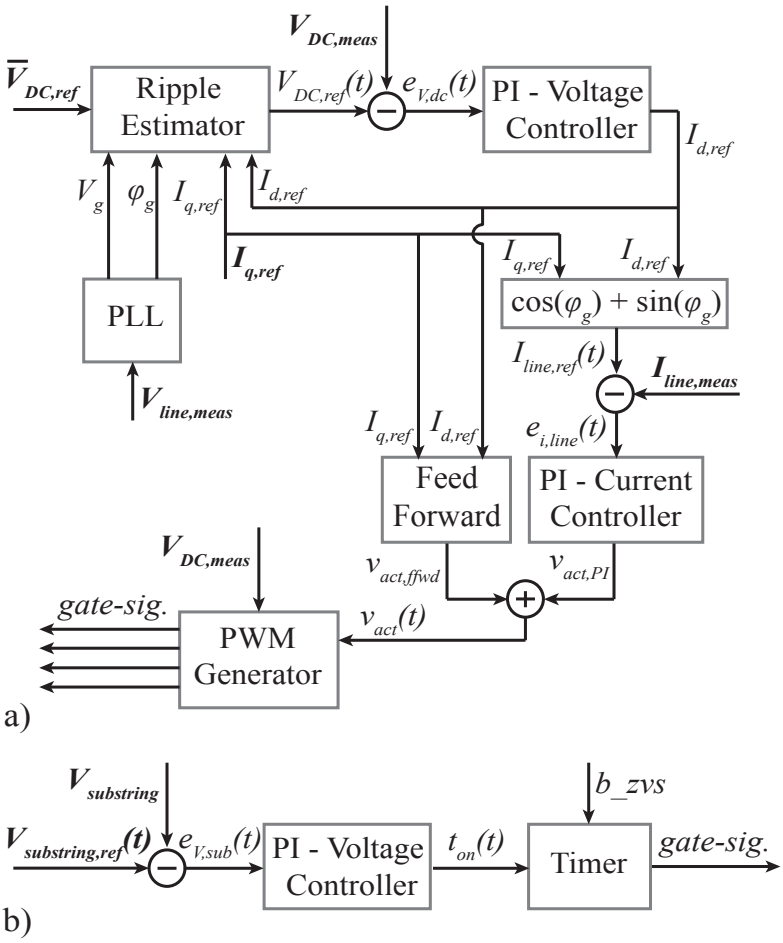


Figure 2.29: Two stage converter system with intermediate DC-link power-decoupling: a) DC-AC stage controller, b) DC-DC stage controller

3

Advanced Modelling of Magnetic Components

PV-converters operate over a wide power and input voltage range. In order to perform a feasible and decent design of such a converter, losses must be predicted with high accuracy over the whole load range. In general, the optimal design of a magnetic component is characterized by an optimal ratio between core losses and winding losses. For an application with wide power range, this optimal ratio can only be achieved at one certain power level. At the other power levels the magnetic component is operated in a non-optimal way. Under this non-optimal operating conditions other loss components might be dominant, such as excessive winding losses or losses caused by parasitic elements. Therefore the applied magnetic models demand a more detailed modelling of the physical effects, than models applied for a single operating point.
Where possible, state of the art magnetic models are applied. Though in the case of the losses in foil windings and the parasitic elements of a flyback transformer, the state of the art models did not meet the accuracy and/or calculation speed requirement. In this two cases advanced models are developed. The state of the art models and the new developed advanced magnetic models are discussed and described in the following subsections.

3.1 Applied State of the Art Magnetic Models

3.1.1 Core Losses

The losses in a magnetic core are well known to depend on the waveform of the magnetic flux-density in the core $B(t)$ [59]. From the flux density waveform, the losses for a given core segment can be calculated using the Steinmetz parameters, given in the datasheet of the according core-material. If $B(t)$ is purely sinusoidal the losses are calculated using the Steinmetz equation [60]. In modern switched mode power electronic circuits, $B(t)$ is typically non-sinusoidal, but piecewise linear. For these type of flux waveforms, the core losses are calculated with the improved general Steinmetz equation (iGSE) [61]. The iGSE allows for a more accurate loss-calculation with non-sinusoidal waveforms.
Relaxation effects, as described in [62], are not taken into account. To model the losses caused by relaxation effects, the author of [62] proposed the i^{2}GSE, which relies on measured core parameters in addition to the Steinmetz parameters. Though this method is considered to be out of scope for this work.
Another effect, greatly influencing core-losses, is the presence of an airgap in laminated cores [63]. This effect increases core-losses at high frequencies due to Eddy currents in the vicinity of the airgap. The increased high frequency core-losses in gapped laminated cores are taken into account as derived in appendix B.

3.1.2 Winding Losses

Conduction losses in the windings of magnetic components are influenced by the effect of Eddy currents, which lead to an increased conductor resistance at higher frequencies, due to current displacement, see [59] chapter 5.

For the calculation of the Eddy-current losses, the low frequency approximation defined in [59] chapter 5.2.1 is applied. This approximation neglects the magnetic field caused by the Eddy-currents, hence the magnetic field is assumed to fully penetrate through the conductor. This assumption holds true if the largest conductor-dimension $l_{cond,max}$ is

lower than:

$$l_{cond,max} \leq 1.6 \cdot \delta, \tag{3.1}$$

where δ is the so called penetration- or skin-depth defined by:

$$\delta \leq \sqrt{\frac{2 \cdot \rho_c}{\mu \cdot \omega}} \tag{3.2}$$

with

ω**:** angular frequency of the applied magnetic field

μ**:** permeability of the material

ρ_c**:** electrical resistivity of the conducting material

The losses caused by Eddy-currents can be split into two parts, skin-effect and proximity-effect losses. These two loss-components are shown to be orthogonal to each other and can be treated separately, [64],[59] chapter 5.2.3. The skin-effect describes the effect, that a sinusoidal current flowing through a single conductor is displaced towards the edges of the conductor at high frequencies. The proximity-effect takes into account the current displacement in a conductor caused by an external magnetic field, that penetrates through the conductor. The proximity-losses in a magnetic component can therefore only be determined, if the magnetic field in the winding window is given.

Winding-Window H-Field Approximation

To determine the exact field in the winding window is a complex task and is usually performed with a FEM simulation tool. Besides FEM simulation, there exist various analytical methods for approximating the external field in the winding window. These methods offer much lower computational effort than FEM simulations and can easily take into account arbitrary H-field waveforms by Fourier decomposition. The methods can be categorized into 1-D and 2-D methods, see [59] for an overview. 1-D methods feature low computational effort and take into account the field component in parallel to the winding layer. Magnetic components with a gapped core (e.g. inductors and flyback transformers) have a fringing field, which introduces a non-negligible radial field component. 2-D methods take into account radial fringing fields and

lead to higher accuracy of the proximity losses, at the expense of higher computational effort [65].

In this work the so called mirroring method, [59], [65], is applied for the approximation of the H-field. The mirroring method is based on a low frequency, 2-D field approximation. This low frequency-type approximation neglects the H-field caused by the induced eddy currents, assuming that the external H-field fully penetrates through a conductor. This holds true, if (3.1) is fulfilled [65]. For a given conductor diameter, the frequency up to which, the low frequency approximation holds, follows from (3.1) and (3.2):

$$f_{max} = \frac{2.56 \cdot \rho_c}{\mu \cdot \Pi \cdot l_{cond,max}^2}. \tag{3.3}$$

The mirroring method is implemented according to the work presented in [65]. Figure 3.1a) schematically shows windings arranged in the rectangular winding window of a magnetic core. This arrangement causes a field vector $\hat{H}_e$ across conductor q_{x_i,y_k} due to the current $\hat{i}_{x_u,y_l}$ of conductor q_{x_u,y_l}. When the low frequency approximation in 3.1 is fulfilled, the following further assumptions hold true. The current distribution in conductor q_{x_u,y_l} is approximately uniform and can be represented as point-current located at the center position (x_u, y_l)[65]. Moreover the field vector $\vec{H}_e$ is assumed to be constant across the surface of conductor q_{x_i,y_k} and the field value at its center is assigned to conductor q_{x_i,y_k}. To simplify the numerical field calculation, the winding window is mapped into the complex plane. The positions of conductor q_{x_i,y_k} and q_{x_u,y_l} are expressed as complex numbers and the field vector $\hat{H}_e$ is determined by

$$\begin{aligned}\hat{H}_e &= -j\frac{\hat{i}_{x_u,y_l}}{2\pi\sqrt{(x_u-x_i)^2+(y_l-y_k)^2}} \cdot \frac{(x_u-x_i)+j\,(y_l-y_k)}{\sqrt{(x_u-x_i)^2+(y_l-y_k)^2}} \\ &= \frac{\hat{i}_{x_u,y_l}\,((y_l-y_k)-j\,(x_u-x_i))}{2\pi\left((x_u-x_i)^2+(y_l-y_k)^2\right)}.\end{aligned} \tag{3.4}$$

To calculate the total external field across conductor q_{x_i,y_k}, the contribution from all conductors must be summed up. The magnitude of

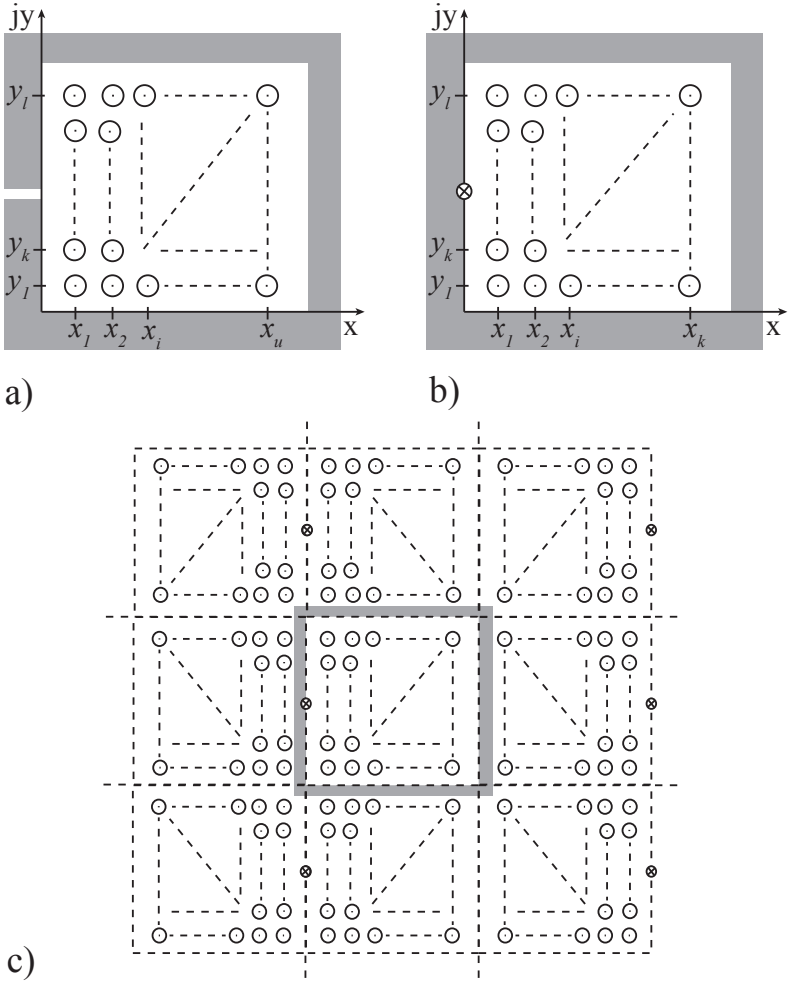


Figure 3.1: a) Schematic of 2-D winding arrangement b) Modelling of air gap as fictitious conductor with equivalent current density c) Mirroring: replacing magnetic walls by mirrored conductors.

the total external field $\hat{H}_e$ across conductor q_{x_i,y_k} is thus given by

$$\hat{H}_e = \left| \sum_{u=1}^{m} \sum_{l=1}^{n} \varepsilon(u,l) \frac{\hat{i}_{x_u,y_l} \left((y_l - y_k) - j \left(x_u - x_i \right) \right)}{2\pi \left(\left(x_u - x_i \right)^2 + \left(y_l - y_k \right)^2 \right)} \right| \tag{3.5}$$

where $\varepsilon(u,l) = 0$ for $u = i$, $l = k$ and $\varepsilon(u,l) = 1$ for $u \neq i$, $l \neq k$.

The impact of a magnetic conducting material is modeled with the *method of mirroring*, which is based on the fact, that the magnetic H-field is always perpendicular to a magnetic wall with infinite permeability [59]. The wall is replaced by injected currents resulting in the same field, as if the magnetic wall would be present. The new currents are the mirrored version of the original currents, as illustrated in 3.1c). In case of windings that are fully enclosed in a winding window, the opposite wall is mirrored as well, thus a new wall is created. With each mirroring step the walls are pushed further away.

Airgap Modelling with Mirroring Method

The Mirroring method allows for modelling of the airgap as a current density. The airgap is removed from the core and replaced by a fictitious conductor [65], as shown in fig. 3.1b). An equivalent airgap current density is flowing through the fictitious conductor, which is introduced in such a way, that the resulting H-field is equivalent to the fringing field of the airgap. The equivalent airgap current $\hat{I}_{airgap}$ can be calculated out of the magneto motive force of the windings $\hat{Mmf}_{wdgs}$ as follows.

First, the airgap reluctance R_g and the core reluctance $R_{c,sum}$ must be calculated. The airgap reluctance is calculated with the 3-D approach presented in [66], formula (8)-(12). The reluctances of the core sections of an E-core are calculate with [66], formula (15). For other core-shapes these formulas must be adapted accordingly. By setting up the reluctance model of the transformer ($\hat{Mmf}_{wdgs}$ as source), the magneto motive force of the airgap $\hat{Mmf}_g$ is given by:

$$\hat{Mmf}_g(k) = (-1) \cdot \hat{Mmf}_{wdgs}(k) \cdot \frac{R_g}{R_g + R_{c,sum}}, k = 0, .., M-1. \tag{3.6}$$

Note the factor (-1), which follows from geometrical considerations.

Next, it is assumed that $\hat{Mmf}_g$ is caused by a single conductor $\hat{Mmf}_g(tk) = N_g \cdot \hat{i}_g(tk)$ with $N_g = 1$. The equivalent airgap current is then given by:

$$\hat{I}_{airgap}(k) = (-1) \cdot \hat{Mmf}_{wdgs}(k) \cdot \frac{R_g}{R_g + R_{c,sum}}, k = 0, .., M-1. \quad (3.7)$$

Losses in Round Wires

Eddy-current losses in round wires can be calculated using the formulas in [64], appendix A. Skin losses are calculated by Fourrier decomposition of the winding current. The proximity losses for a given conductor are derived from the Fourrier decomposition of the external field in the winding window at the position of the conductor.

Losses in Litz Wires

The losses in Litz wire are calculated according to [67]. The proximity losses in the Litz wire are separated into two parts: the external proximity losses, caused by the external field, and the internal proximity losses caused by the field of the other strands in the Litz wire. This separation is based on the assumption, that the external field is constant over the conductor area cross-section.

Losses in Foil

For the cases of foil windings not exposed to an airgap fringing field (e.g. in transformers), the losses are calculated with the method proposed in [68], assuming a magnetic field parallel to the foil windings. If the foil winding is exposed to an airgap fringing field, the method developed in section 3.2 is applied.

3.1.3 Thermal Model for Inductors and Transformers

The temperature of the magnetic components is modelled in thermal steady state with an equivalent thermal circuit based on thermal resistances. Figure 3.2 shows the equivalent thermal circuit applied for transformers as well as inductors. The thermal resistances $R_{th,L1}$ to

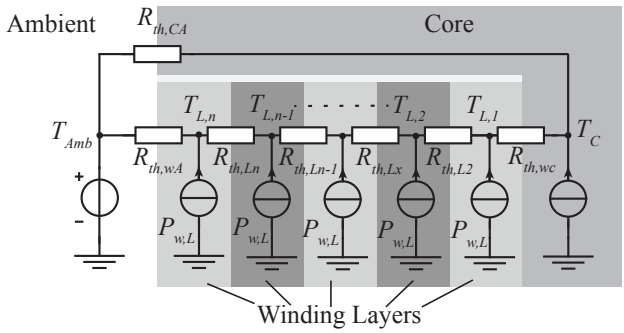


Figure 3.2: Thermal equivalent circuit for transformer or inductor

$R_{th,Ln}$ within the winding are calculated for each pair of adjacent layers. The heat is assumed to be transferred through the layers by conduction. The thermal resistance $R_{th,Ln}$ can be calculated by the basic formulas presented e.g. in [57] section 29-2. In case of round conductors or Litz wires the improved analytical model presented in [69] is applied to calculate $R_{th,Ln}$. The winding losses are assumed to spread uniformly among the layers.
The heat is transferred to the ambient by free convection cooling through the surface of the core and the windings to the ambient air. The thermal resistance $R_{th,CA}$ from core to ambient and $R_{th,WA}$ from winding to ambient are modelled based on the formulas and results in [59],[70].

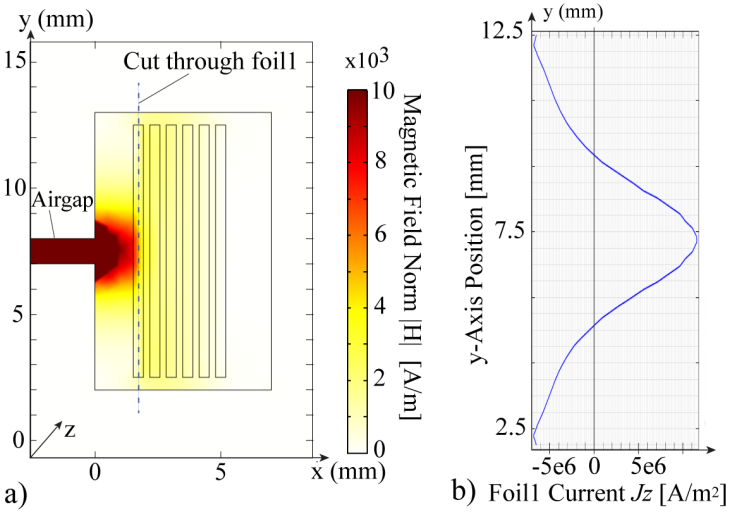
3.2 Eddy Current Losses in Foil Windings exposed to an Airgap Fringing Field

Foil windings exposed to a 2-D magnetic fringing field are subject to current displacement in two directions, along the thickness *thck* as well as the width *wdth* of the foil, see the example of a foil-inductor in fig.3.3a) and b). Calculation methods neglecting the influence of this current displacement suffer from poor modeling accuracy [71],[72], as shown for the foil-inductor in fig.3.3c). To accurately predict the losses in the foil windings, the current displacement must be taken into account, which requires a 2-D field calculation in the winding window. A finite element

simulation (FEM) is the most commonly applied approach to perform this 2-D field calculation. Though FEM suffers from long calculation times and difficult parametrization [71]. The work in [73], which applied a genetic algorithm to optimize a transformer with foil windings, reported calculation times of 20 hours even for a simplified FEM model considering only one harmonic component. However, for most applications it is inevitable to consider more than one harmonic component for accurate loss prediction. Therefore, FEM is not considered to be an ideal option for automatized model-based optimization. Various alternative methods are proposed in literature to consider the effect of 2-D fringing fields. They can be categorized into two distinct approaches.

The first approach is to derive analytical formulas, which take into account the losses caused by the fringing field and allow for very high calculation speed. The derived formulas rely on an analytical solution of the Maxwell equations in the winding-window. However, to obtain analytically solvable differential-equations, approximations and restrictions to simple geometries are required. The solid-conductor-method proposed in [71], [72] and the method proposed by [74], [59] are the most known methods of this kind. The solid-conductor-method approximates the layers of a foil-winding as one unified solid conductor. The model is shown to be accurate for low frequencies, but at high frequencies the accuracy decreases, because the solid conductor exhibits different eddy currents, than a foil winding would actually have. The method described in [74], [59] approximates the eddy current as line-current-density located at the surface of the foil closest to the gap. This foil is assumed to absorb the whole fringing field. The air-gap is also modelled as line-current-density (by Fourier-decomposition in space). For either of these two methods, the air-gaps must be located at the inner core-leg and the area between the air-gap and the foil-winding must be filled with air or a spacer only (no additional round-conductor winding).

The second approach is often referred to as semi-empirical or semi-numerical. A closed-form formula for the losses is derived from a set of prior FEM simulations. This approach tries to combine the advantages of the FEM-approach - high accuracy and no geometrical restrictions - and the advantages of the analytical-approach - high calculation speed. The squared-field-derivative method, proposed in [75] for round-wires is an example of such a method. The work in [76] derives a modified Dowells-formula [68] for losses in the foil-winding of a high-



c)

Foil Winding Losses (W/m)

	10kHz	30kHz	50kHz
FEM-Simulation:	78mW/m	315mW/m	830mW/m
1D Dowel Method:	65mW/m	242mW/m	560mW/m
DC-Loss ($I^2_{rms}R_{dc}$):		25mW/m	

Figure 3.3: FEM Simulation of foil windings in a winding window of a gapped magnetic core (I_{foil}=5A/30kHz): a) Magnetic field b) Non-homogeneous current density along foil 1 (see cut-line in fig.3.3a).The homogeneous current density would be 2.5e6A/m^2) c) Losses in the foil winding at 5Arms sinusoidal winding current at different frequencies in comparison to a simple 1D calculation method [68] and the DC-losses.

frequency transformer. The formula contains additional parameters, used to curve-fit the losses from 2-D FEM simulations and enables fast calculation of winding losses. Though, it is restricted to a certain geometry, analyzed prior by FEM simulations.
To be able to effectively perform model-based optimization of magnetic components with foil windings, a method is needed, which features much lower calculation times than a FEM-simulation and on the same time is not subject to restrictions on air-gap and winding arrangement

as the existing analytical and semi-numerical approaches. To fulfil this need, a novel, semi-numerical method is developed, which can be applied to arbitrary winding and air-gap geometries. Regarding calculation times, the new method is in between the FEM- and the existing semi-empirical approaches. The developed method can be combined with the mirroring method and is a true 2-D field approximation for foil windings. The method is described in section 3.2.1 and its validation is given in section 3.2.4.

3.2.1 Foil- to Square-Conductor Method

In the following the principle of the calculation method is explained with the example of an inductor with foil windings. Figure 3.3a) shows a 2-D finite element simulation of an inductor with a sinusoidal winding current of $I_{z,foil}$=5A@30kHz. $|H|$ is the amplitude of the 2-D magnetic field introduced by the air-gap. The x-component of the H-field, which is perpendicular to the foils, causes an eddy current flowing in the y-z plane. The existence of the eddy currents results in an inhomogeneous current distribution J_z, which is shown in fig. 3.3b) for the foil closest to the air-gap. For accurate loss modelling, the investigated method must determine the non-homogeneous J_z of every foil of the winding. The routine to perform this task, consists of two major parts. The first part is the calculation of the non-homogeneous current density $J_{z,foil}$ in a single foil by the following steps shown in fig. 3.4:

1. *Transformation to round-conductors:* The foil is transformed into area-equivalent round-conductors.

2. *Calculation of current $J_{z,round}$ in round-conductors:* The well known formulas for round conductors are used to calculate the eddy current in each separate round conductor. The external magnetic field H_e is derived using the mirroring method, as will be explained in detail later in this section.

3. *Calculation of foil current $J_{z,foil}$:* The current density in the foil is derived from the current density of the round conductors, by postulating continuity of $J_{z,foil}$ at the boundary of adjacent round conductors.

4. *Discretize and average to square-conductors:* The foil is cut into area-equivalent square-conductors. To each square-conductor a

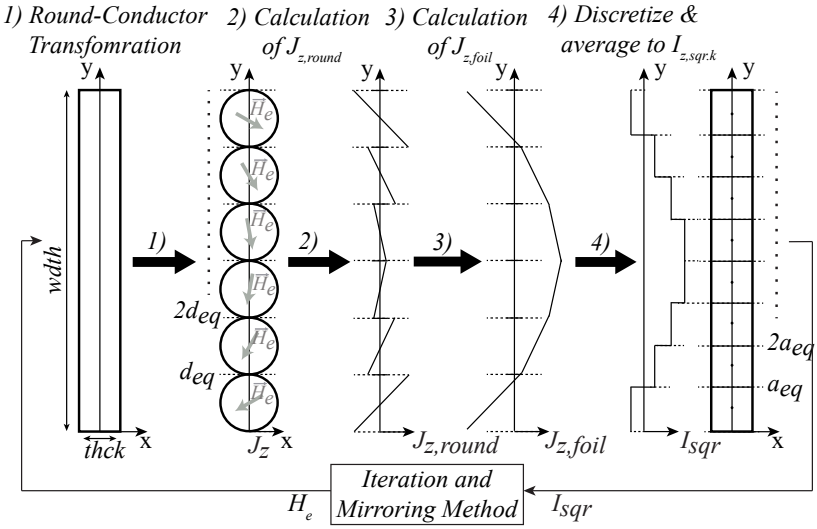


Figure 3.4: Overview calculation procedure for non-homogeneous current distribution in a foil, exposed to a 2-D transverse magnetic field: *1)* Round-Conductor Transformation, *2)* Calculation of round-conductor current density, *3)* Calculation of foil current density, *4)* Transformation to square-conductors and calculation of square-conductor currents.

current $I_{z,sqr,k}$ is attributed according to $J_{z,foil}$, whereas the current density is approximated to be constant over the cross-section of each square-conductor. Unlike in step 1), a transformation to square-conductors is applied, as they represent the actual foil-winding more accurately. In this way, the current displacement in the foil is taken into account by the square-conductor currents and the mirroring method can be applied to calculate the H-field and the losses in the same way as for round- and Litz-wires [59], [65].

The second part of the routine considers the entire foil-winding and involves a numerical iteration to determine $J_{z,foil}$ in each foil of the winding, starting from the uniform distribution. The method is applicable to arbitrary air-gaps and winding arrangements. As the mirroring

method is based on a low-frequency approximation ([59] chapter 5.2.1), the model is applicable as long as the foil thickness *thck* fulfills the following condition:

$$thck \leq 1.6 \cdot \delta, \tag{3.8}$$

where δ is the so called penetration- or skin-depth. The same condition can be alternatively expressed as a frequency limit at a given winding geometry:

$$f_{max} = \frac{2.56 \cdot \rho_c}{\mu \cdot \pi \cdot thck^2}, \tag{3.9}$$

where ρ_c is the electrical resistivity of the conductor material and μ the permeability of the material.
The following two sections describe both parts of the routine in detail.

Non-Homogeneous Current Density in a 2-D Transverse Field

The inhomogeneous foil current density $J_{z,foil}$ caused by the 2-D transverse field H_e is calculated with the procedure shown in fig. 3.4, which consists of four steps:

- *Transformation to round-conductors:* The foil-winding is transformed into a series of aligned equivalent round-conductors, using the equivalent DC-resistance transformation ([59], chapter 5.4.1 and [77]) and postulating equivalent width *wdth* of the transformed winding, see fig. 3.4, *1)*. The constraints on surface and width can be expressed by $wdth \cdot thck = n_{cond} \cdot \pi \cdot (d_{eq}/2)^2$ and $n_{cond} \cdot d_{eq} = wdth$ from which follows:

$$d_{eq} = \frac{4 * thck}{\pi}. \tag{3.10}$$

- *Calculation of Current $J_{z,round}$ in round-conductors:* With the foil decomposed into aligned round conductors, the eddy current caused by the external magnetic field $\overrightarrow{H}_e$ in a round conductor can be calculated using the formula derived in [78] formula (7-45):

$$\bar{J}_z(r,\varphi) = 4\mu_2 H_e j^{\frac{3}{2}} k \frac{J_1(j^{\frac{3}{2}} kr)}{F(j^{\frac{3}{2}} kr_{eq})} sin(\varphi - \varphi_{He}). \tag{3.11}$$

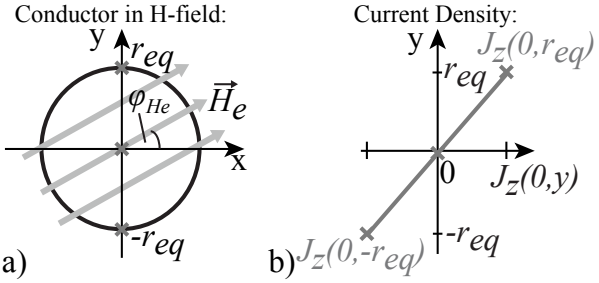


Figure 3.5: a) Round-conductor in a transverse H-field b) Linearized eddy current density J_z in the round conductor evaluated on the y-axis: $(0,-r_{eq})$, (0,0) and $(0,r_{eq})$.

where

$$F(j^{\frac{3}{2}}kr_{eq}) = (\mu_1+\mu_2)J_0(j^{\frac{3}{2}}kr_{eq})+(\mu 1-\mu 2)J_2(j^{\frac{3}{2}}kr_{eq}) \qquad (3.12)$$

$$k = \sqrt{(2\pi f)\rho 1\mu 1} \qquad (3.13)$$

and

μ_1 magnetic permeability of the conductor material

ρ_1 conductivity of the conductor material

μ_2 magnetic permeability of material around the conductor

$\overrightarrow{H}_e$ sinusoidal transverse magnetic field vector with amplitude H_e and φ_{He}

f frequency of H_e.

Figure 3.5a) illustrates a single round-conductor exposed to a transverse H-field. The current density is derived on the y-axis by evaluating the current density at the three points ($J_z(r_{eq}, \frac{\pi}{2} - \varphi_{He})$, $J_z(r_{eq}, -\frac{\pi}{2} - \varphi_{He})$, $J_z(0,0)$) and linear interpolation, as shown in fig. 3.5b). By assuming, that the aligned round-conductors are isolated from each other, the eddy current J_z along the y-axis is calculated separately for each round-conductor in the transformed foil winding, resulting in the current density shown in fig. 3.4, *2)*.

- *Calculation of foil current $J_{z,foil}$:* The current density in the foil $\bar{J}_{z,foil}(y)$ ($y = [0, wdth]$) is derived from the eddy currents of the separated round-conductors. Unlike before, the aligned round conductors are now assumed to be electrically connected. Under this condition, the current density must be continuous at the boundary between two conductors. This can be expressed as the following condition, which must hold true for all conductors

$$\bar{J}_{z,k}(d_{eq}, \frac{\pi}{2}) = \bar{J}_{z,k+1}(d_{eq}, -\frac{\pi}{2}); k = [1..n_{cond} - 1]. \tag{3.14}$$

As a consequence of (3.14), the derivative of the current density $\frac{dJ_{z,foil}(y)}{dy}$ is fully determined by the current density in the round conductors

$$\frac{dJ_{z,foil}(y)}{dy} = \frac{dJ_{z,k}(0, y_k)}{dy}; y_k = mod(y, d_{eq}), k = int(1 + \frac{y}{d_{eq}}), \tag{3.15}$$

where the function $int()$ rounds down to the next integer. Note that $J_{z,k}$ is given in cartesian coordinates, for the sake of simplicity. A second condition for $J_{z,foil}(y)$ follows from the total current, flowing through the foil winding

$$\int \bar{J}_{z,foil}(y) dA = \bar{I}_{foil}. \tag{3.16}$$

The foil current density $\bar{J}_{z,foil}(y)$ can be calculated considering (3.15) and (3.16), which is shown schematically in fig. 3.4, *3)*.

- *Discretize and average to square-conductors:* The foil is transformed into n_{sqr} square-conductors with the size $a_{eq} = thck$ as shown in fig. 3.4f). The dimension of the square-conductors is such, that they fulfill the low frequency approximation in (3.8). Hence for the mirroring method [79], the square-conductors can be treated in the same manner as windings of round conductors. It is assumed, that the current density in the foil is approximately linear across the crossection of the square conductors. With this assumption the current in each square conductor can be derived from the current distribution $\bar{J}_{z,foil}(y)$ by

$$\bar{I}_{z,sqr,k} = a_{eq}^2 \bar{J}_{z,foil} \left(\frac{a_{eq}}{2} + a_{eq}(k - 1) \right) . k = [1..n_{sqr}]. \tag{3.17}$$

3.2.2 Numerical Iteration for entire Foil Winding

In section 3.2.1 a single foil exposed to a sinusoidal transverse field is modelled as n_{sqr} aligned square-conductors with a non-homogeneous current distribution $\bar{I}_{z,sqr,k}, k = [1..n_{sqr}]$. When a magnetic component with an entire foil winding is modelled, the correct determination of the square-conductor currents $\bar{I}_{z,sqr}$ becomes a non-trivial task. This is due to the fact, that a certain calculated $\bar{I}_{z,sqr}$ actually affects its root cause, being the external field $\overrightarrow{H}_e$. Therefore a numerical iteration is applied to determine $\bar{I}_{z,sqr}$.
The numerical iteration will again be explained on the example of the inductor with a foil winding, shown in fig. 3.3. Each foil is cut into n_{sqr} square conductors. Thus the whole foil winding is represented as $n_{sqr,tot} = n_{sqr} \cdot N_{foil}$ square conductors, where N_{foil} is the turns number of the foil winding. For the winding loss calculation, an arbitrary winding current waveform $i_{foil}(t)$ is decomposed into its complex spectrum by means of the Fourier transform. For each harmonic $\bar{I}_{foil}$ at frequency f_h, the iteration must be performed separately. The complex array $\bar{I}_{sqr}$ of size (1 x $n_{sqr,tot}$) contains the current amplitudes of all square conductors. The starting point of the iteration is the uniform current-distribution:

$$\bar{I}_{sqr,0} = \left[\frac{\bar{I}_{foil}}{n_{sqr}} \dots \frac{\bar{I}_{foil}}{n_{sqr}} \right]. \tag{3.18}$$

Figure 3.6 shows the overview of the numeric iteration. At the kth iteration, the latest current-distribution $\bar{I}_{sqr,k}$ is used as input to the mirroring method, to calculate the external H-field at the position of each square conductor $\bar{H}_{e,x}$ and $\bar{H}_{e,y}$. With the foil-to-square-conductor method described in section 3.2.1, the current distribution $\bar{I}_{sqr,calc}$, that is caused by this external field, is calculated. The expression

$$\bar{I}_{sqr,k} = \bar{I}_{sqr,calc}. \tag{3.19}$$

is a sufficient condition for the correct current distribution. It describes the situation, where the physical root cause and its effect are in balance. Due to the miscellaneous approximations involved in this method, condition (3.19) can not be exactly fulfilled. The goal of the iteration is therefore to minimize the error

$$\bar{e}_{sqr} = \mid \bar{I}_{sqr,calc} - \bar{I}_{sqr,k} \mid . \tag{3.20}$$

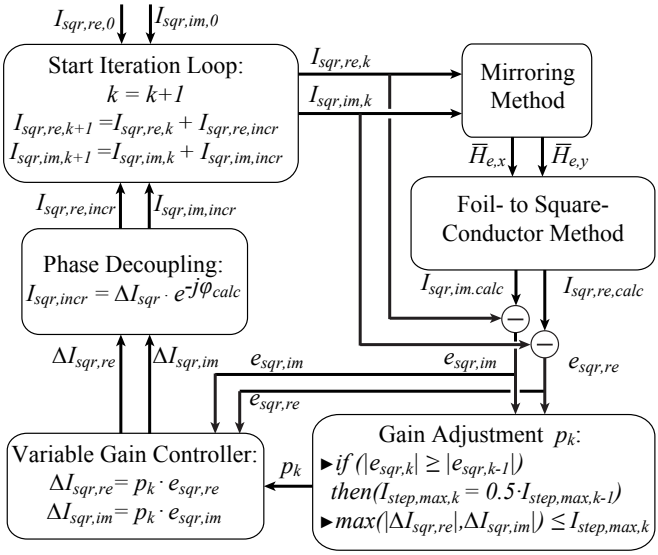


Figure 3.6: Overview numerical iteration for calculation of the non-homogeneous current distribution in foil windings.

This minimization could as well be treated as a purely mathematical problem and state of the art algorithms could be used to determine $\bar{I}_{sqr}$. Though the investigation of such algorithms and the comparison of their performance to the applied iteration-method is out of scope for this work. The applied iterative calculation method for $\bar{I}_{sqr}$ is based on a control-loop analogy. Further it is taken advantage of the fact, that the calculated current distribution $\bar{I}_{sqr,calc}$ exhibits, apart from a proportional scaling factor, approximately the same waveform as the correct current distribution $\bar{I}_{sqr,end}$. This makes it possible to adjust $\bar{I}_{sqr,k}$ by adding an increment $\bar{I}_{sqr,incr}$ derived from $\bar{e}_{sqr}$ at each iteration. Figure 3.7 illustrates this on the example of the inductor, shown in fig. 3.3. The norm of the current distributions in foil 1, $|\bar{I}_{sqr,k}|$ and $|\bar{I}_{sqr,calc}|$ are shown at the very beginning of the iteration and after 5 and 10 iteration steps. The current distribution, $|\bar{I}_{sqr,FEM}|$, derived from a 2-D FEM simulation, is shown as comparison. From the first iteration step on, $|\bar{I}_{sqr,calc}|$ and $|\bar{I}_{sqr,FEM}|$ exhibit similar waveforms and $|\bar{I}_{sqr,k}|$ approaches $|\bar{I}_{sqr,FEM}|$ with advancing iteration.

The detailed function to determine $\bar{I}_{incr}$ from $\bar{e}_{sqr}$ is split into three

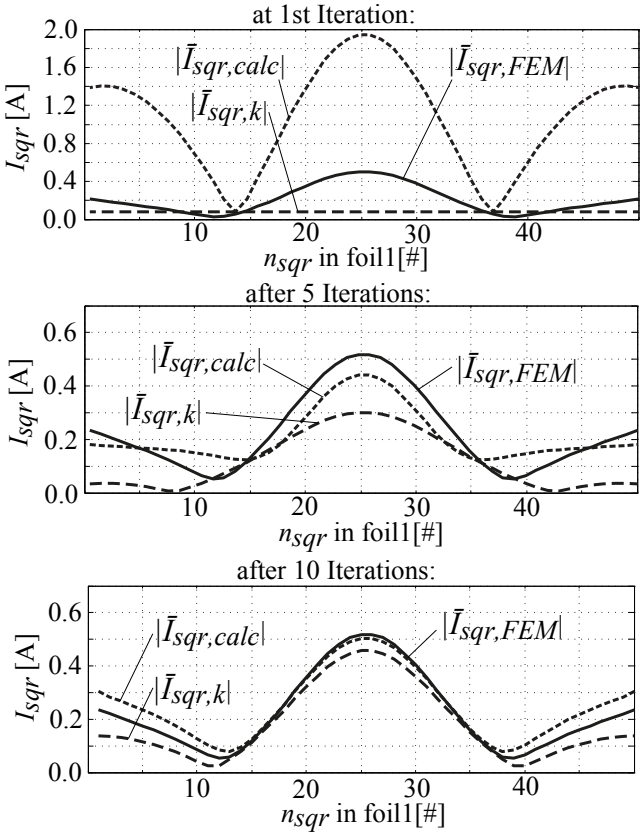


Figure 3.7: Numeric iteration for the current in foil 1 of the inductor with foil-winding (shown in fig. 3.3): $\bar{I}_{sqr,k}$ and $\bar{I}_{sqr,calc}$ at different iteration-steps in comparison to the current distribution $\bar{I}_{sqr,FEM}$ derived from the 2-D FEM simulation of the inductor.

parts, shown in fig. 3.6, which are described in the following:

- *Variable Gain Controller*: To iteratively reduce the error $\bar{e}_{sqr}$, the current distribution is incremented by

$$\bar{\Delta} I_{sqr} = p_k \cdot \bar{e}_{sqr}. \tag{3.21}$$

- *Gain Adjustment*: The proportional gain p_k is adjusted in each

iteration step, in order to limit the maximal current increment per iteration step to $I_{step,max,k}$, hence

$$p_k = \frac{I_{step,max,k}}{max(\bar{e}_{sqr})}. \tag{3.22}$$

The limit $I_{step,max,k}$ is initialized to the uniform current distribution

$$I_{step,max,0} = \frac{\bar{I}_{foil}}{n_{sqr}}. \tag{3.23}$$

During iteration $I_{step,max,k}$ is stepwise reduced to ensure, that $\bar{e}_{sqr}$ converges. If the averaged error over the whole winding $\bar{e}_{sqr,avg,k} = \sum \bar{e}_{sqr,k}/n_{sqr,tot}$ did not diminish compared to the error at the last iteration $\bar{e}_{sqr,avg,k-1}$, than $I_{step,max}$ is adjusted:

$$\begin{aligned} &(e_{sqr,avg,k} > e_{sqr,avg,k-1}) \Rightarrow \\ &I_{step,max,k+1} = \frac{I_{step,max,k}}{2}. \end{aligned} \tag{3.24}$$

- *Phase Decoupling*: The feedback-loop introduces a phase-shift, see equation 3.11 of the foil-to-square-conductor method. To ensure, that the current increment $\bar{\Delta}I_{sqr}$ will actually compensate for the error $\bar{e}_{sqr}$, the phase-shift of the current increment must be compensated by:

$$\bar{I}_{incr} = \bar{\Delta}I_{sqr} \cdot e^{-j\varphi_{calc}}. \tag{3.25}$$

where φ_{calc} is the phase-shift of the foil-to-square-conductor method given by:

$$\varphi_{calc} = \angle\bar{I}_{sqr,calc} - \angle\bar{I}_{sqr,k}. \tag{3.26}$$

The iteration loop is executed and the current distribution is adjusted by

$$\bar{I}_{sqr,k+1} = \bar{I}_{sqr,k} + \bar{I}_{incr} \tag{3.27}$$

until $\bar{e}_{sqr}$ converges to a negligible small value, having an insignificant influence on the calculated winding losses. Alternatively the winding

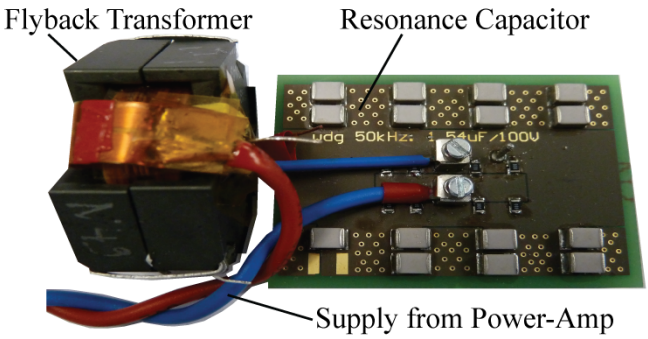


Figure 3.8: Experimental setup for winding loss measurement of the flyback transformer.

losses in the whole foil winding can be directly taken as convergence criteria.

$$P_{foil,tot,k} = \sum_{k=1}^{n_{sqr,tot}} P_{sqr,k}, \tag{3.28}$$

$$\Delta_{P,k} = 100 \frac{|P_{foil,tot,k} - P_{foil,tot,k-1}|}{|P_{foil,tot,k}|} \tag{3.29}$$

where $P_{sqr,k}$ are the eddy current losses in the kth square-conductor calculated as described in [59]. The iteration is stopped, if $\Delta_{P,k}$ stays below a certain threshold over 5 iterations:

$$max(\Delta_{P,k-5}, \ldots, \Delta_{P,k}) \leq 0.1\% \Rightarrow \text{Stop} \tag{3.30}$$

3.2.3 Applied Method for Measuring Winding Losses and Core Losses

For experimental verification of the proposed foil-loss model, the following measurement method proposed in [80] is applied. It allows to derive the losses in the foil-winding at a sinusoidal winding-current. Figure 3.8 shows the measurement setup consisting of the flyback transformer and a resonance capacitor. The schematic of the entire measurement setup is shown in fig. 3.9 and the applied measurement equipment is listed in

table 3.1. The primary winding is put in series with a capacitor C_{res} to form a resonant circuit together with the transformers magnetizing inductance. A sinusoidal voltage source, realised with a signal generator and a power amplifier, drives the test current I_{test} through the primary winding. The secondary Litz-winding is left open circuit. The transformer has an additional sensing-winding (0.1mm^2 Cu round-wire) having the same turns-ratio as the primary winding, which is used for voltage measurements only. Hence no net current is flowing through the sensing-winding. The losses in the sensing winding are negligibly small, due to the low turns-number and the small conductor diameter.

The schematic in fig. 3.9 shows the T-equivalent circuit of the transformer, the parasitic cable inductance L_{Cable} and the resonance capacitor series resistance R_{CESR}. The equivalent components of the sensing winding are not relevant, because the winding does not carry any current. L_σ and L_{mag} are the magnetizing- and stray-inductance referred to the primary winding. The resistors R_{Core} and R_{wdg} model the losses in the core and the primary winding. The aim of the setup is to deter-

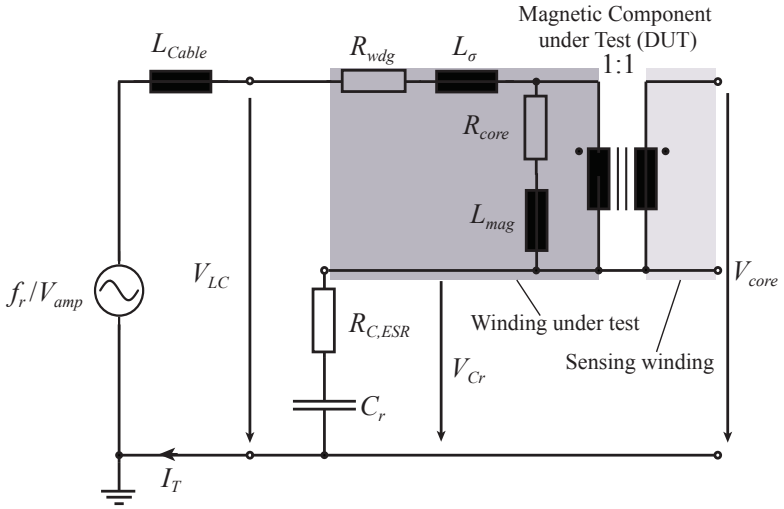


Figure 3.9: Overview measurement method for core- and winding-loss measurement of a magnetic component, according to [80].

Table 3.1: Winding loss measurement setup: used equipment

Waveform Generator	Agilent 33522A
Power Amplifier	AE Techtron 7224
Oscilloscope	LeCroy WaveSurfer 24MXSB
Voltage Probes	LeCroy PP008
Current Probe	LeCroy AP015

mine the resistive losses in R_{wdg}. This can be achieved by two distinct measurements.

- *The Resonant Method* as proposed in [81] and described in [80] section 1.2.4, allows to determine the total resistive losses of the resonant-circuit by operating the voltage-source at

$$f_r = \frac{1}{2\pi\sqrt{(L_{mag} + L_\sigma)C_r}}. \tag{3.31}$$

  At this operating point the voltage over L_σ, L_{mag} and C_r cancel out and the voltage measured at the input of the resonant circuit V_{LC} only contains the resistive parts

$$V_{LC} = V_{R,wdg} + V_{R,core} + V_{R,C,ESR}. \tag{3.32}$$

  Consequently, the losses in the resonance circuit can be split into three parts

$$P_{LC} = P_{R,wdg} + P_{R,core} + P_{R,C,ESR}. \tag{3.33}$$

  The losses caused by the resonance current $P_{LC,fr}$ can be calculated from the measured voltage V_{LC} and current I_T by

$$P_{LC,fr} = \frac{1}{2}\hat{I}_{T,fr}\hat{V}_{LC,fr}\cos(\varphi_{I,T,fr} - \varphi_{V,LC,fr}), \tag{3.34}$$

  where $\hat{I}_{T,fr}$, $\varphi_{I,T,fr}$ and $\hat{V}_{LC,fr}$, $\varphi_{V,LC,fr}$ are the amplitude and phase at the resonance frequency derived from the fourier transform.

- *The Capacitive Cancellation Core Loss Method* proposed in [80] section 2.1.2, can be applied to measure the core losses separately. Unlike the resonant method, where the winding losses are included

in the measured losses. The voltage V_{core} is measured between the upper port of the sensing winding to ground, as shown in fig. 3.9. Note that the lower port of the sensing winding is connected to the resonance capacitor and hence V_{core} can be expressed as

$$V_{core} = V_{R,core} + V_{L,mag} + V_{R,C,ESR} + V_{C,r}. \tag{3.35}$$

The frequency of the voltage-source is chosen, such that $V_{L,mag} = -V_{C,r}$, which is the case at

$$f_r = \frac{1}{2\pi\sqrt{L_{mag}C_r}}. \tag{3.36}$$

The measured voltage only contains the resistive parts $V_{core} = V_{R,core}+V_{R,C,ESR}$ and the resistive losses caused by the resonance current can be calculated by:

$$P_{core,fr} = \frac{1}{2}\hat{I}_{T,fr}\hat{V}_{core,fr}\cos(\Delta\varphi_{fr}), \tag{3.37}$$

with

$$\Delta\varphi_{fr} = \varphi_{I,T,fr} - \varphi_{V,core,fr}. \tag{3.38}$$

The losses consists of the following two parts

$$P_{core,fr} = P_{R,core,fr} + P_{R,C,ESR,fr}. \tag{3.39}$$

To obtain the magnetic losses $P_{R,wdg,fm}$ at a certain frequency f_m the losses $P_{LC,fm}$ and $P_{core,fm}$ are measured as explained above. For the measured transformer the stray inductance L_σ is much smaller than L_{mag} and hence the same resonant capacitance C_r can be used for both measurements. The magnetic losses can be obtained from the measurements with (3.34) and (3.39) by:

$$P_{R,wdg,fm} \simeq P_{LC,fm} - P_{core,fm}. \tag{3.40}$$

The losses in $R_{C,ESR}$ cancel out, though $R_{C,ESR}$ should not be much higher than R_{wdg} to obtain a good resolution of the measurement.

The accuracy of the performed loss measurements caused by the deviations in the current Δi, voltage- Δu and phase-angle measurements $\Delta\varphi$ can be deducted from (3.34),(3.37) using the second-order

Taylor-series of the cosine $\left(\cos(x) = 1 - \frac{x^2}{2}\right)$ and neglecting deviation-coefficients of third order:

$$\Delta p_{meas} = \Delta v I + V \Delta i + \Delta v \Delta i - \frac{P}{2} \Delta \varphi^2. \tag{3.41}$$

The phase-deviation follows from the time-delay between the voltage- and current-probe by

$$\Delta \varphi = 2\pi \cdot 16ns \cdot f_{meas}, \tag{3.42}$$

whereas the time-delay is derived from a reference-measurement using a shunt-resistor. Voltage and current deviation are found to be

$$\Delta v \simeq 80\mu V, \Delta i \simeq 1mA. \tag{3.43}$$

This is above their theoretical resolution-limit of 63μV and $313\mu A$, due to the low signal-to-noise ratio at high scale-factors of the oscilloscope. An additional measurement error introduced by the parasitic inter-winding capacitance, described in [80] (2.11), is found to be negligible small, due to the relatively low measuring frequencies. The deviation in the measured winding losses follows from (3.40)

$$\Delta p_{wdg} \simeq \Delta p_{LC} + \Delta p_{core}, \tag{3.44}$$

where Δp_{core} and Δp_{LC} are calculated with (3.41).

3.2.4 Validation of the Proposed Method

The proposed foil-loss method is validated on the example of a flyback-transformer for a PV-inverter. The whole calculation routine, including the foil-to-square-conductor method, is implemented as software program. The losses in the conductors are calculated according to [67], for Litz-wires, and [59], for square-conductors. The air-gap fringing field is modelled according to [79]. The Fourier decomposition of the flyback winding-currents is performed according to [77].

It is important to keep in mind, that the mirroring method restricts the validity of the calculated losses. For accurate calculation of the magnetic field in the winding window (3.8) must be fulfilled. This constraint results in a frequency limit f_{max}, that can be calculated for the considered flyback-transformer using (3.9). Above this frequency limit the mirroring method overestimates the magnetic field in the winding

Table 3.2: Parameters 2-D flyback transformer with foils and Litz-wire.

Core	$a = 15\text{mm}, c = 7\text{mm}, d = 11\text{mm}$
Winding	Cu foil and Litz wires N_1=5, $thck_{w1}$=0.2mm, $wdth_{w1}$=10mm $N_2 = 50, d_{s,w2} = 0.1\text{mm}, N_s = 7$
Air-gap	$l_{airgap} = 1\text{mm}$

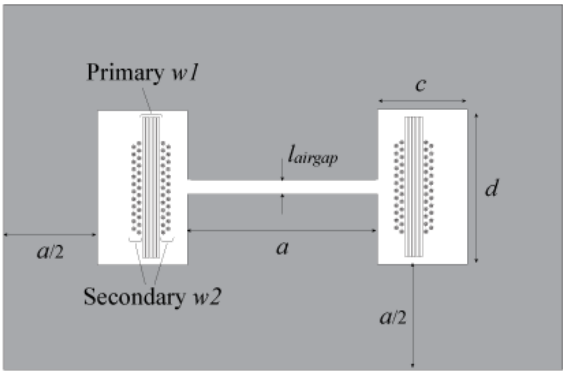


Figure 3.10: 2-D Flyback transformer with foils and Litz wires: E-core with air-gap and 'sps' interleaved windings with foils on the primary and Litz wire for the secondary.

window and hence the calculated winding losses are subject to a modeling error. Note that a transformer or inductor design, optimized for low winding losses, generally fulfills (3.8). Hence (3.8),(3.9) do not restrict the applicability of the proposed method for a practical design.

The validation is performed twofold, first with a FEM simulation and second with measured losses of a flyback-transformer. Further the calculation complexity of the model is discussed and the calculation speed is investigated.

Validation with FEM Simulation

The model for foil-winding losses is compared to the conduction losses derived from a 2-D FEM simulation. The specification of the modelled

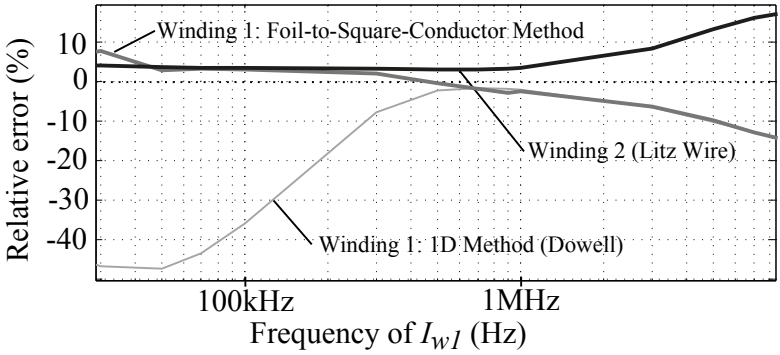


Figure 3.11: Flyback-Transformer as specified in tab. 3.2, with sinusoidal excitation of the foil-winding ($I_{w1} = 5$A) and open circuit on the secondary: 2D FEM simulation results compared to losses derived from the foil-to-square-conductor method and the 1D calculation method [68].

transformer is given in table 3.2 and the 2-D winding arrangement is illustrated in fig. 3.10. The range of validity for the low frequency approximation of the mirroring method given by (3.9), is $f_{max,w1}$=270kHz for the foil winding and $f_{max,w2}$=1MHz for the Litz-wire winding.
A first validation of the loss calculation is performed for the case of a sinusoidal current of 5A and various frequencies from 10kHz to 10MHz flowing through the foil winding. Whereas winding two is an open circuit. The deviation of the new loss model to the 2D FEM simulation is shown in fig. 3.11 (in percentage, normed to the FEM simulation values). The losses calculated with the new loss model exhibit good accordance to the 2D FEM simulation. The difference is below 7%, as long as the low frequency approximation is valid, and up to 15% in the whole considered frequency range. Figure 3.11 further shows the foil losses derived from the simple 1D calculation method [68]. In the frequency range up to 400kHz, where a typical flyback converter would operate, this method exhibits deviations up to 40% compared to the FEM simulation. For the investigated transformer geometry, the influence of the airgap becomes negligible in the MHz-range with the two methods predicting approximately the same losses.

The second validation is done by considering actual winding current waveforms of a DC-DC flyback converter operating in boundary con-

Table 3.3: Comparison Foil-to-Square-Conductor Method to 2D FEM Simulation for Flyback Transformer Winding Losses.

Calculation Method	2D FEM Simulation	Foil-to-Square-Cond. Method	
Computer	Laptop, Intel-Core i7-M620@2.67GHz		
Calculation time	320s	19s	113s
Number of Harmonics	20	20	100
Number of Iterations	-	43	42
Winding Losses P_{w1}	1.32W	1.28W	1.33W
Winding Losses P_{w2}	0.576W	0.575W	0.67W

duction mode (BCM) at a switching frequency of 100kHz (8A peak, 0.75 duty cycle). To limit the FEM calculation time, only harmonics from 100kHz to 2MHz are considered. Figure 3.12 shows the convergence of the error in the non-homogeneous current density $\bar{e}_{sqr,avg,k}$ and the total foil winding losses $P_{foil,tot,k}$ during the iteration (see section 3.2.2). The error $\bar{e}_{sqr,avg,k}$ converges step-by-step and decreases below 3% after 40 iterations. Simultaneously the calculated losses converge to the final value. After 43 iterations the convergence criteria for the calculated losses (3.30) is fulfilled. The final value is 1.28W, which corresponds to a difference of 3.5% compared to the 2D FEM simulation, see table 3.3. To demonstrate the increase in calculation time, a second calculation-run of the foil-to-square-conductor method is performed and also listed in table 3.3, taking into account a larger number of harmonics from 100kHz-10MHz. The winding losses in the foil increase marginally by 4% due to the higher order harmonic currents.

Validation with Measured Flyback Transformer

The model for foil-winding losses is verified by measurements on a flyback transformer. The transformer is built with a gapped RM low-profile core and foil windings on the primary and Litz wire on the secondary. The flyback transformer loss model is parameterized to model the measured flyback transformer. The frequency limit, up to which the low-frequency 2-D field approximation used for winding loss calculation

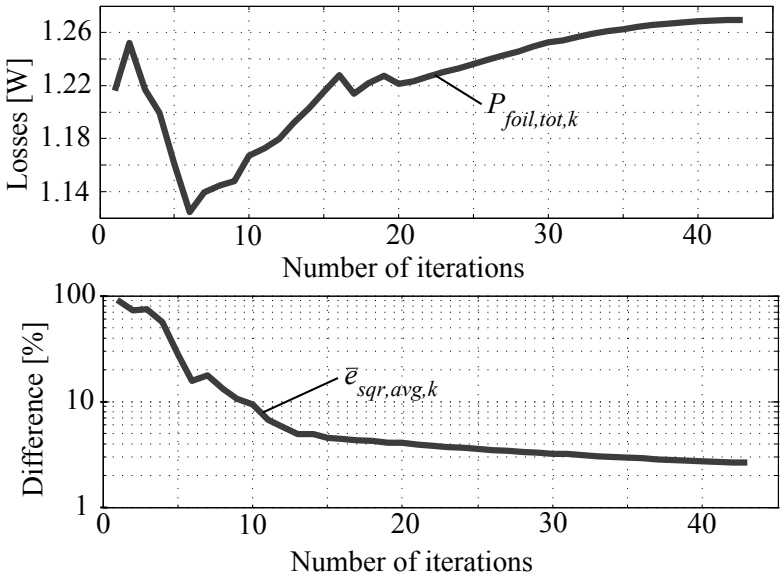


Figure 3.12: Loss-calculation for flyback-transformer as specified in tab. 3.2: Iteration convergence of the winding losses in the foil winding $P_{foil,totk,k}$ (see (3.28)) and the error in the current distribution $\bar{e}_{sqr,avg,k}$ (averaged over all harmonics and normed to $I_{foil,rms}$, the foil rms-current, see (3.20)).

applies, is determined by (3.9) and equals

$$f_{max,low,freq} = 172kHz \tag{3.45}$$

for the investigated flyback transformer geometry. Above this frequency the modelled winding losses are subject to an increasing modelling error. In table 3.4 the measured winding losses are compared to the losses calculated with the model at three different measuring points: 50kHz, 100kHz and 200kHz. Further the accuracy of the measured losses is determined with (3.44). The model exhibits a good accordance to the measured losses. The winding losses predicted by the model show a deviation below 15% for the measuring points at 50kHz and 100kHz. The measuring frequency of 200kHz is above $f_{max,low,freq}$ and accordingly the deviation increases to a value of 21%.

Table 3.4: Flyback Transformer Winding Loss Model Validation by comparison to measured losses.

Frequency:	Loss Measurements:		Loss Model:	Deviation:
f_{meas}	P_{wdg}	Δp_{wdg}	P_{wdg}	Δ_{model}
50kHz	0.0136W	$< \pm 3.9\%$	0.0132W	**-2.6%**
100kHz	0.0046W	$< \pm 6.2\%$	0.0052W	**14.9%**
200kHz	0.0022W	$< \pm 7.5\%$	0.0026W	**21.3%**

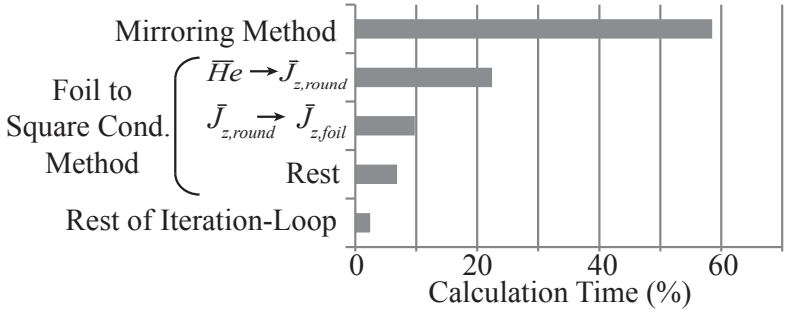


Figure 3.13: Flyback Transformer Model (specification as in table 3.2 at DC-DC BCM operation with harmonics from 100kHz to 2MHz): calculation complexity analysis.

Calculation Time and Complexity

Reducing the calculation time was a major motivation to develop the foil-to-square-conductor method. The achieved evaluation time for the whole loss-model of a flyback-transformer in DC-DC BCM operation (see 3.2.4 and table 3.2 for specifications), is 19s and 113s for a considered number of higher order harmonics of $n_h = 20$ and $n_h = 100$ on a laptop computer equipped with an Intel-Core-i7-620M@2.67GHz. In comparison, the speed optimized FEM model, using the software FEMM 4.2, exhibits a calculation time of 320s for $n_h = 20$, see table 3.3 for details. Figure 3.13 shows the relative calculation time of the most dominant tasks of the loss-model. The calculation complexity of the foil-to-square-conductor method and the mirroring method scales linearly with n_h and the number of conductors, being $n_{sqr,tot}$ for the foil-to-square and $n_{sqr,tot} + n_{wdg,2}$ for the mirroring method ($n_{wdg,2}$

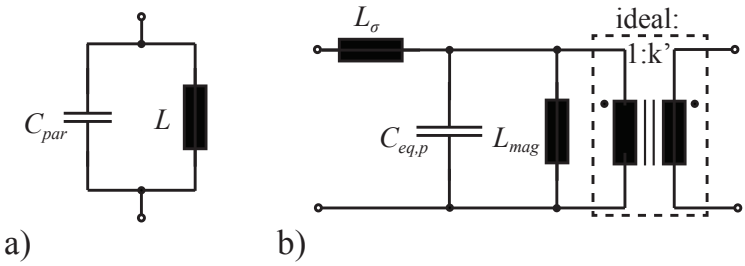


Figure 3.14: Equivalent circuit considering parasitic elements: a) inductor, b) flyback transformer

is the secondary turns number). Note, that all dominant tasks are in the iteration loop (see fig. 3.6). Thus the iteration itself is the most time-consuming part of the loss-model, whose calculation time depends linearly on the number of iterations $n_{num,it}$. Evaluations with different parameters showed, that the developed numerical iteration needs an average of $n_{num,it} \simeq 45$ to converge. To further reduce calculation time, an improved iteration-method would be most effective. While $n_{sqr,tot}$ and $n_{wdg,2}$ follow from the specifications, the number of harmonics n_h can be chosen as low as possible, depending on the considered current waveform. A further speed improvement can be achieved in the mirroring method by reducing the number of mirroring below the currently implemented 11x11 mirrored basic winding windows.

3.3 Parasitic Capacitance and Inductance of Magnetic Components

It is well known, that practical setups of magnetic components exhibit unwanted effects caused by magnetic stray fields and electric fields, e.g. in between layers of the windings [68],[59]. The effect of these electromagnetic fields can be modelled as lumped parasitic elements. Figure 3.14a) shows the equivalent circuit of an inductor with the parasitic capacitance C_{par} in parallel to the main inductance L. The equivalent circuit of a flyback transformer is shown in fig. 3.14b). The detailed derivation of the circuit is given in appendix A.1. The circuit also exhibits a parasitic capacitance $C_{eq,p}$ in parallel to the primary side

magnetizing inductance L_{mag}. The leakage inductance L_σ models the stray-field between the primary and the secondary winding of the transformer.
In a switched mode power electronic circuit, the parasitic elements influence the operating waveforms and cause additional losses. Wether the respective parasitic element has a relevant influence on the total converter losses depends very much on the operating point and the operating mode of the circuit. In general at low output power the parasitic capacitances cause non negligible losses, whereas at high output power the influence of leakage inductances must be considered. An accurate converter loss model for a wide power range requires accurate modelling of both types of parasitic elements, parasitic capacitances and leakage inductances. A design of the magnetic component, by means of a model-based optimization algorithm, further requires the models to feature fast calculation time and applicability to arbitrary geometries. The following sections describe the applied modelling methods. For the modelling of the leakage inductance a new method is proposed, which more accurately considers the frequency dependence of the parasitic inductance.

3.3.1 Equivalent Parasitic Capacitance

In literature, various approaches can be found for predicting parasitic capacitances of transformers and inductors. Whereas some approaches, e.g. [82], apply time consuming finite element simulations, most approaches are based on analytical formulas. A comprehensive review of these analytical approaches is given in [83]. Among them, the method in [84] is most suited for low power flyback-transformers. It allows to predict the capacitances of multi-layer transformers with interleaved windings, based on a parallel plate approach. Another approach for capacitance prediction, is the charge simulation method [85],[86]. This method is, unlike the analytical approaches, not restricted to certain windings and core geometries. Furthermore, the core-to-winding capacitances, which are commonly neglected in the analytical approaches, can easily be taken into account.
In this work, the charge simulation method is the approach of choice, since its calculation time showed to be fast enough for model based optimization. For applications where calculation time is more critical, the approach [84] would be an alternative.

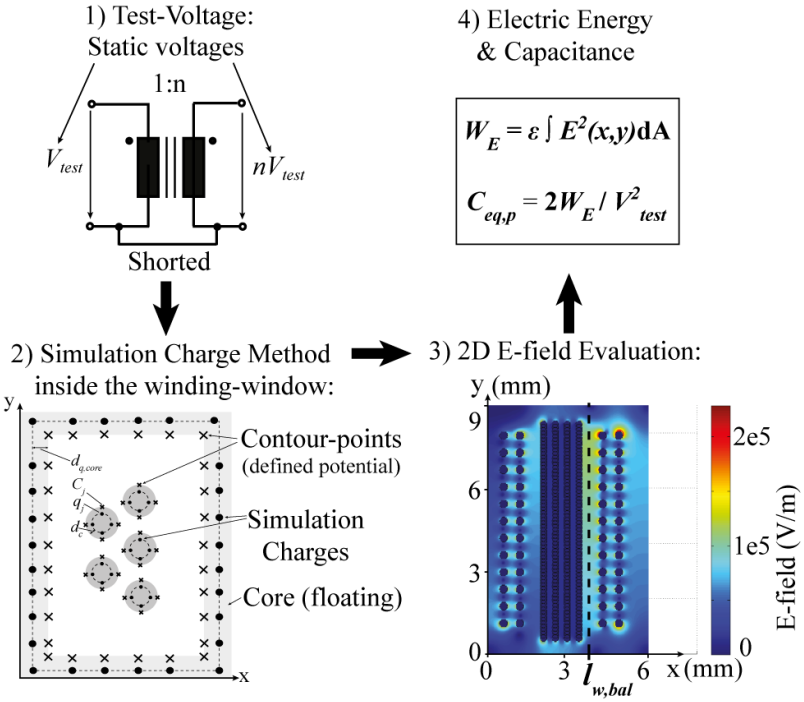


Figure 3.15: Procedure for parasitic capacitance calculation

The procedure for calculating $C_{eq,p}$ with the charge simulation method is schematically shown in fig. 3.15. First an electrostatic test-voltage V_{test} is applied to the transformer terminals. Assuming a linear decrease of the potential along the turns of a winding, the potential of each conductor $\Phi_1..\Phi_{n_w}$ in the winding window is determined. Second the 2-D charge simulation method is used to calculate the 2-D E-field in the winding window. Each conductor is represented by four simulation charges $q_j - q_{j+3}$ arranged circularly inside the conductor. For each of these simulation charges a corresponding contour-point $C_j - C_{j+3}$ is defined on the surface of the conductor, having the reference potential Φ_j of the considered conductor. If the conductor is not a round-conductor but a Litz-wire, it is approximated as round-conductor with the same outer-diameter as the actual Litz-wire. Foil-windings can be treated

in the same manner as round-conductors, just with more simulation charges and contour-points placed along the long side of the foil. The walls of the winding window are replaced by a parameterizable number n_{core} of simulation charges, placed at a distance $d_{q,core}$ from the winding window surface, as shown in fig.3.15. Again, for each simulation charge a contour-point is defined on the surface of the winding-window. The contour-points have the reference potential Φ_{core}. This potential can either be specified directly or assumed as unknown, for the common case of a floating core. It results a linear equation system for a total number of $n_{tot} = n_w + n_{core}$ unknown simulation charges and the unknown core potential Φ_{core} ([85] section II, [86] section 2.2), which can be expressed in matrix-form:

$$\begin{bmatrix} p_{1,1} & . & . & p_{1,n_{tot}} & 0 \\ . & . & . & . & 0 \\ . & . & . & . & 0 \\ p_{n_w,1} & . & . & p_{n_w,n_{tot}} & 0 \\ p_{n_w+1,1} & . & . & p_{n_w+1,n_{tot}} & -1 \\ . & . & . & . & -1 \\ . & . & . & . & -1 \\ p_{n_{tot},1} & . & . & p_{n_{tot},n_{tot}} & -1 \\ k_1 & . & . & k_{n_{tot}} & 0 \end{bmatrix} \cdot \begin{bmatrix} q_1 \\ . \\ . \\ q_{n_w} \\ q_{n_w+1} \\ . \\ . \\ q_{n_{tot}} \\ \Phi_{core} \end{bmatrix} = \begin{bmatrix} \Phi_1 \\ . \\ . \\ \Phi_{n_w} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} . \tag{3.46}$$

The rows $1..n_w$ of this matrix-equation define the potential of all conductor contour-points. Rows $n_w{+}1..n_{tot}$ set the potential of all contour-points on the core-surface to be equal to Φ_{core}. The geometrical coefficients $p_{i,j}$ are given by ([85], expression 23):

$$p_{i,j} = \frac{1}{2\pi\epsilon} \cdot \ln\left(\frac{1}{\sqrt{(x_i - x_j)^2 + (y_i - y_j)^2}}\right) \tag{3.47}$$

where ϵ is the electrical permittivity, (x_i, y_i) the position of the contour-point C_i and (x_j, y_j) the position of the simulation-charge q_j. The last row of (3.46) accounts for the fact, that the core is floating. Therefore, the sum of all core simulation charges must be zero, setting $k_1..k_{n_w}{=}0$ and $k_{n_w+1}..k_{n_{tot}}{=}1$. In the third step in fig. 3.15, the 2D electrical field within the winding window is calculated. Due to the 2-D nature of the applied charge-simulation method, the resulting electrical field $\vec{E}'$ is per unit length and can be calculated at an arbitrary position (x, y)

inside the winding window with:

$$E'_x = \sum_{j=1}^{n_{tot}} \frac{q_j}{2\pi\epsilon} \cdot \frac{x - x_j}{\sqrt{(x-x_j)^2 + (y-y_j)^2}}, \tag{3.48}$$

$$E'_y = \sum_{j=1}^{n_{tot}} \frac{q_j}{2\pi\epsilon} \cdot \frac{y - y_j}{\sqrt{(x-x_j)^2 + (y-y_j)^2}}. \tag{3.49}$$

In case of an RM-core with a cylindrical center-leg of diameter a, the actual E-field $\vec{E}$ is given by

$$\vec{E} = \vec{E'} \cdot 2\pi \left(\frac{a}{2} + l_{w,bal} \right) \tag{3.50}$$

assuming rotation symmetry. In case of a non-linear energy-distribution, the mean turns length can not be used to calculate $\vec{E}$. An energy weighted mean turns length $l_{w,bal}$ must be used instead (see fig.3.15, step 3), which can be numerically determined by:

$$\int_0^{l_{w,bal}} \int_0^{Y} {E'}^2 dy dx = \int {E'}^2 \mathrm{dA}/2 \tag{3.51}$$

The last, straight forward step in fig. 3.15 involves the calculation of the equivalent capacitance from the total electric energy in the winding window.

3.3.2 Leakage inductance

Finite element simulations are commonly applied to determine the leakage inductance, based on 2D H-field calculation. However, FEM suffers from long computation times and difficult parametrization [87]. Alternatively, there exist methods based on 1D H-field-calculation, which allow for an analytical calculation of the leakage inductance. Among them, the method in [68] is the most accurate, considering also the frequency dependence of the leakage inductance caused by eddy currents. However, this method showed to be inaccurate (deviation above 30%) for the investigated flyback transformers of typical core size similar to RM12, low number of layers and low filling factor.
Therefore, a new approach has been developed. It combines the analytical methods with a numerical calculation of the H-field. This results in a method applicable to arbitrary geometries and is more accurate for

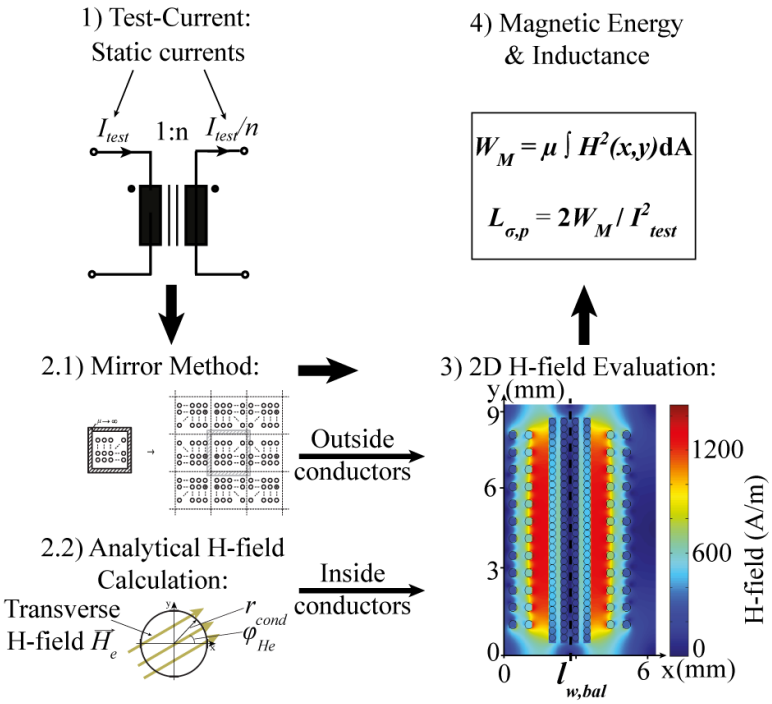


Figure 3.16: Procedure for leakage inductance calculation

the above mentioned winding arrangements.

The new semi-numerical method is based on a 2D H-field calculation applying the mirroring method [59],[65] and consists of four steps, schematically shown in fig.3.16. First, the test-currents I_{test} and I_{test}/n are applied to the primary and the secondary winding. Second, the field outside of the conductors is calculated numerically using the mirroring method [65]. Note that the calculated 2-D H-field $\vec{H}'$ is per unit length. Winding types others than round-conductor are treated as follows. Litz-wire windings are taken into account by treating each strand as separate round-conductor. Foil-windings are transformed into aligned paralleled round-conductors with the equivalent copper-area and the same height as the original foil-winding.
The H-field inside the conductors is attenuated at higher frequencies

due to Eddy currents, which makes the leakage inductance frequency dependent. The mirroring method, being a low frequency-approximation method [59], can not consider this effect. To accurately model the H-field attenuation, the H-field inside the conductors is calculated analytically by using the formulas given in [78] for a cylinder exposed to an external transverse H-field:

$$H_r(r,\varphi) = \frac{4\mu_2|\vec{H}_e|}{j^{\frac{3}{2}}k}\frac{1}{F_{r_0}}\frac{J_1(j^{\frac{3}{2}}kr)}{r}cos(\varphi), \tag{3.52}$$

$$H_\varphi(r,\varphi) = -\frac{1}{2}j^{\frac{3}{2}}k\frac{4\mu_2|\vec{H}_e|}{j^{\frac{3}{2}}k}\frac{1}{F_{r_0}}[J_{-1}(j^{2/3}kr) - J_1(j^{2/3}kr)]\sin(\varphi), \tag{3.53}$$

where

$F_{r_0} = (\mu_1+\mu_2)J_0(j^{\frac{3}{2}}kr_{cond})+(\mu_1-\mu_2)J_2(j^{\frac{3}{2}}kr_{cond}); \quad k = \sqrt{(2\pi f)\rho_1\mu_1}$

μ_1 magnetic permeability of the conductor material

ρ_1 conductivity of the conductor material

μ_2 magnetic permeability of material around the conductor

$\vec{H}_e$ sinusoidal transverse magnetic field vector with amplitude H_e and φ_{He}

f frequency of H_e.

The external transverse field $\vec{H}_e$ is derived at the center of the considered conductor using the mirroring method, see step 2.1 and 2.2 in fig.3.16. The third step in fig.3.16 involves the calculation of the magnetic-field $\vec{H}'$ inside the winding window over a given x-y grid. Note that the H-field is obtained per unit-length, because of the 2-D field calculation. In the same way as for the E-field, the magnetic field per unit length is transformed using the energy weighted mean turns length:

$$\vec{H} = \vec{H}' \cdot 2\pi\left(\frac{a}{2} + l_{w,bal}\right) \tag{3.54}$$

assuming rotation symmetry. Where $l_{w,bal}$ is the energy weighted mean turns length (see fig.3.16, step 3) numerically determined by:

$$\int_0^{l_{w,bal}} \int_0^{Y} H'^2 dydx = \int H'^2 \mathrm{dA}/2 \tag{3.55}$$

Finally, the inductance $L_{\sigma,p}$ is obtained from the total magnetic energy in the winding window.

3.3.3 Model Validation

The models for the parasitic elements described in the first part of this section are verified on a set of three flyback transformer prototypes. The transformer prototypes consist of an RM12 core, foil windings on the primary and round wire on the secondary. The turns-ratio is $n_2 : n_1 = 55 : 5$. The three transformers differ in the interleaving of the primary and the secondary winding. The interleaving varies from single to full interleaving, as shown in fig.3.17a)-c). The leakage inductance can be derived with an impedance-analyzer by measuring the impedance on the secondary side, while shorting the primary-side (see fig. A.3c). The constraint that $L_m >> L_\sigma$ is fulfilled for all three transformers. The leakage inductance reduces greatly when interleaving is changed from single interleaving to multiple interleaving, see fig. 3.17a) and b). Increasing the degree of interleaving from multiple to full interleaving results in only a small reduction of the leakage inductance, because the influence of the inter-layer distance becomes dominant. The new developed model for the leakage inductance shows good accordance with the measurements. Up to 2MHz, the deviations are below 15% and reach maximally 22% at higher frequencies. The model slightly underestimates L_σ, because of not considered effects, such as the wiring to the transformer ports and imperfect geometric winding arrangement. The parasitic capacitance referred to the primary side is measured in open-circuit mode by measuring the impedance on the primary side above the resonance frequency given by $\omega_{res} = 1/\sqrt{L_{mag} C_{eq,p}}$. The modelled capacitances exhibit good accordance with the measurements. The deviations stay below 18%.

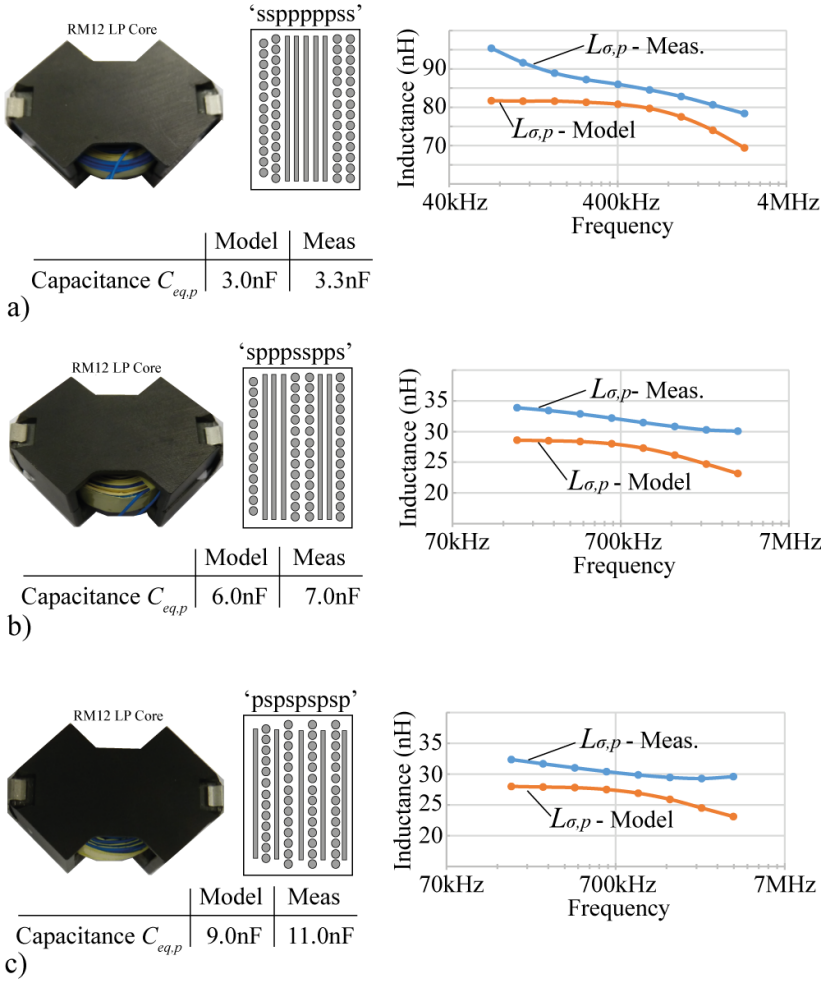


Figure 3.17: Flyback transformer prototypes: a) Single interleaving b) Multiple interleaving c) Full interleaving

4

GaN Devices for Low Power PV Applications

High efficiency is one of the main requirements for a PV converter. Especially for low-power converters, with voltage and current ratings in the range of 600V/10A for grid interfacing and 100V/40A for the PV input-side, low semiconductor losses are a key factor to achieve high converter efficiency. GaN devices, a recently available new generation of power semiconductors, feature unprecedented switching performance. This makes them the ideal device for low power high efficiency PV converters, which up to now rely on Si-MOSFETs.

Introduced back in 1976 ever since the Si-MOSFET has been the dominating device for low power applications. Replacing the bipolar transistors, MOSFETs, as unipolar devices, were more rugged than the bipolar devices and featured various benefits, such as higher switching speed, higher current gain and an isolated gate [88]. This superior performance enabled a swift adoption of switched mode power supplies, which are the back-bone for the many electronic devices we use nowadays. After over thirty years of continuous performance improvements and the overcoming of the silicon limit by the invention of the super-junction MOSFETs, the rate of performance improvement of silicon based MOSFETs slowed down in the past years.

In parallel new types of power transistors, gallium nitride on silicon transistors (GaN FET), emerged throughout the past ten years. These devices are high electron mobility transistors (HEMT), hence are based on a different semiconductor structure as well as a different semiconductor material than Si-MOSFETs. GaN FETs feature an unprecedented performance. Compared to Si-MOSFET the switching figure of merit

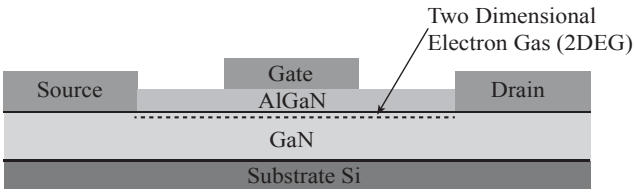


Figure 4.1: GaN High Electron Mobility Transistor typical structure with gate, drain and source contact [88],[89].

($R_{DS,on} \cdot Q_{GD}$) is shown to improve by a factor of two to three for devices up to 100V blocking voltage and by a factor of six for 200V devices [88]. For devices rated at 650V a substantial decrease of the on state resistance $R_{DS,on}$ by a factor two and more is reported [89].

The superior performance of GaN FETs originates from the characteristic of gallium nitride as a wide band-gap (WBG) material. Gallium nitride, such as silicon carbide (SiC), possesses a higher critical electric field strength than silicon. This allows for devices with a lower $R_{DS,on}$ at a given blocking voltage. GaN further exhibits the remarkable characteristic that it forms a 2D electron gas (2DEG) with high electron mobility in the intimacy of a thin AlGaN layer [88]. This effect is utilised to realise a high electron mobility transistor, exhibiting a lateral structure as schematically shown in figure 4.1. Depending on the realisation of the gate-contact there result two distinct operation modes: depletion mode (d-mode) and enhancement mode (e-mode). The gate-contact of depletion mode devices is formed as a Schottky contact. By applying a negative voltage to this contact the electrons underneath become depleted and the 2DEG in between the gate and the source is interrupted [88]. Hence d-mode devices have normally-on behaviour and must be actively turned off by driving the gate negative. In contrary e-mode devices feature normally-off behaviour. The gate-contact for enhancement mode devices is realized in such a way, that a depletion region is formed underneath the gate-region and the 2DEG is interrupted [88]. The transistor is enhanced applying a positive gate-voltage, which closes the interrupted channel between drain and source and turns the device on. Both types of devices, e-mode and d-mode, are naturally capable of reverse conduction and do not have an intrinsic body diode thanks to the pure lateral device structure [88],[90]. In reverse conduction the GaN devices perform similar to a SiC Schottky

diode, featuring no reverse recovery charge [89] and enabling high speed switching.
For the application in power electronic converters normally-on behaviour bears the inherent risk of DC-link short-circuit at start-up and in case of a gate-drive failure. Whereas the early GaN devices were d-mode transistors, most of the latest devices are therefore designed as e-mode transistors. Further there exist the so called cascode-devices, which combine a d-mode GaN transistor and a low-voltage normally-off MOSFET to realize normally-off behaviour.

The outstanding figure of merit of GaN devices and the advantageous device characteristics enable the design of power electronic converters with higher efficiency and/or higher switching frequencies allowing for a smaller size of the passive components [91],[55],[92],[93],[94]. Due to the excellent switching performance of GaN devices with voltage slopes of 100V/ns and above [90],[95], not the transistor itself, but the parasitic elements of the package and the circuit become the major limiting factor for system performance [96],[97],[98]. Even small parasitic inductances in the commutation loop can cause substantial overshoot at these high voltage slopes, imposing a limit to the maximal feasible switching speed. This issue becomes even more critical due to the fact, that the current GaN devices are not avalanche rated. Also for the gate-driver, the parasitic loop-inductance must be kept to a minimum to avoid parasitic turn-on issues. Due to the low threshold voltage of typically 1.5V, GaN devices are prone to parasitic turn-on at high dV/dt switching, as explained more in detail in section 4.1.2 dealing with the design of gate-drivers for GaN devices. Furthermore common parasitic inductances, shared by both the gate-drive and the commutation-loop, slow down the turn-on and turn-off of the transistor, increasing the switching losses [99].

4.1 Available GaN Devices and Packaging Technologies

Conventional semiconductor packages, such as the D2PAK exhibit parasitic package inductances up to 5nH. A GaN transistor operated in such a package can not be operated at its full switching speed. To guarantee stable operation, the voltage slope must be limited for the

reasons stated above. Though slower switching speed results in higher switching losses. To allow high speed switching of GaN devices and to fully exploit the outstanding switching performance improved semiconductor packages with reduced package parasitics are required [100]. Package parasitics are mainly determined by the following two package properties, first the mere distance between the package-pad and the actual contact on the semiconductor-die, second the way the connection between pad and die-contact is realized. The conventional way of wire-bonding spans rather high loop areas, causing parasitic inductances. Various approaches to improve packaging are proposed in literature and nearly each manufacturer of GaN devices developed its own solution. An overview on the improved packaging technologies is given in the following:

Improved Standard Packages: The most obvious approach is to improve existing packages for minimized parasitics. This can be achieved by an optimized placement of the semiconductor-die inside the package and by improved wire-bonding or contacting with copper clips. An improved DPAK package, named thinPAK$^{\text{TM}}$, is developed in [91]. The source inductance is reduced to 1.8nH by reducing the length of the external legs and the use of many paralleled bond wires. The work in [101] improves a high-voltage cascode GaN HEMT packaged in a PQFN package by stacking the Si-MOSFET and the GaN FET die and bonding with copper clips.

Near Chip-Scale Packaging: A more substantial improvement in package parasitics can be achieved by packages tailored to the size of the semiconductor-die, such as the DirectFET$^{\text{TM}}$ packages for low voltage MOSFETs, featuring parasitic package inductances below 0.5nH [88]. The GaNPX packaging technology, applied for 650V GaN devices, is based on embedding of the semiconductor die in a thin PCB-style package and bonding with micro-vias and copper planes. The GaNPX packages exhibit package inductances of 0.4nH to 0.8nH.

Passivated Die Form Packaging: The most radical way to shrink the size of the package is the passivated die form approach. The semiconductor die is actually not packaged, but passivated and contacted directly by solder bars. Getting rid of any interfacing bonding, extremely low parasitic packaging inductances are

achieved. The LGA packages applied for low voltage GaN FETs by Efficienct Power Conversion (EPC) and International Rectifier (IR) achieve parasitic package inductances of 0.2nH [88].

Power-Module Packaging with PCB Integration: The switching cell of power electronic converters actually consists of a pair of transistors in halfbridge configuration and a DC-link capacitor. Even if discrete packages with minimal parasitic inductances are applied, the layout of the switching cell on the PCB adds some further parasitic inductances. The power module approach therefore packages two transistors in halfbridge configuration and aims to minimize the parasitic inductances of the entire switching cell. The power-module package, as proposed by [96],[100] consists of a PCB with two embedded semiconductor dies. For the DC-link capacitors and the gate-drivers standard SMD components are used, which are soldered on the top-side of the PCB-package. The PCB embedding of the semiconductors, brings several advantages [97]. The dies can be placed much closer to each other, which allows for an improved design trade-off between parasitic loop inductance and parasitic capacitance. The module can be designed to be conform with EMI requirements, which are difficult to fulfill at high switching speeds [96]. The gate-drive loop inductance can be minimized, by putting the gate-driver closer to the transistor. A first stage DC-link capacitor could be directly integrated into the PCB close to the semiconductors, to protect the transistors from overvoltage. The power-module PCB-package developed in [100] achieved a total switching cell parasitic inductance of 0.6nH.

4.1.1 Low Voltage High Current Application

The first GaN devices introduced to the market in 2009 were low voltage devices [88]. Since then a broad variety of devices arose, covering blocking voltages from 15V to 200V and rated currents from 1A to 90A. There exist several manufacturers, but some of them up to now only deliver devices to key customers under a non-disclosure agreement (NDA). Among them efficient power conversion (EPC) is the most prominent manufacturer offering the broadest product portfolio and the most advanced devices. Its GaN FETs are commercially available, without any NDA or restrictions. Further EPC developed a decent collection on online available application notes and reference designs, well establishing

the application of low voltage GaN FETs in power electronic converters.
Reference designs operated at 50V blocking voltage are reported to achieve switching speeds with rise and fall times of 2.5ns and 4ns and a peak dV/dt of 30V/ns [92]. Consequently the parasitic turn-on issue is less pronounced, than for high voltage GaN FETs switched with 100V/ns. The gate can be driven with a unipolar gate voltage and a bootstrap for the supply of high-side switches in a haflbridge. A detailed gate-drive design-guide is given in [88]. Given the fast rise and fall times and high currents, a very high current slope results. To avoid over voltage spikes, an extremely low commutation loop inductance is required.
To achieve this goal, EPC and also IR deliver their GaN FETs in LGA passivated die form packages, featuring ultra low package parasitics. Reference PCB designs achieve total halfbridge loop inductances below 1nH [92],[98]. To further improve performance EPC is aiming one step further. Monolithic halfbridge power chips are currently in development. Unlike the power-module packaging approach with PCB integration discussed before, the halfbridge is integrated on semiconductor die level, resulting in a power module IC with a halfbridge loop inductance of a mere 0.2nH [102].

4.1.2 High Voltage Low Current Application

GaN FETs rated at 600V or 650V needed some more years to emerge than their low voltage counterparts. Several players, such as Panasonic, GaNSystems, Transphorm etc. but also academia, spent a lot of effort to develop GaN FETs with a higher level of blocking voltages. Still these devices are often only available under NDA. Last year GaNSystems was the first manufacturer to make their devices commercially available without restrictions. Others are surely to follow soon.
Though the application of these devices in power electronic circuits is still a novelty and yet to be successfully established. Limited information on reference designs and application examples are available from manufacturers and in literature. Nevertheless in the last years these devices attracted a lot of attention at universities and in industry. For instance 'The Little Box Challenge', an international competition to build a much smaller power inverter (www.littleboxchallenge.com), further boosted the application of high voltage GaN FETs. Such that an

increasing number of publications is about to be available, giving application examples, optimizing designs and slowly establishing the use of high voltage GaN FETs.
GaN devices operating at 400V DC-link voltage can easily achieve peak voltage slopes of 100V/ns [90],[95]. For low power applications with currents up to 10A, voltage overshoot due to the parasitic commutation loop inductance is not such an issue. For instance for a current fall-time of 1ns and a commutation loop inductance of 5nH an overvoltage spike of 50V results, being well in the safe range. However the risk of parasitic turn-on is high, due to switching with very high dV/dt (see sec. 4.2).
Most of the available high voltage GaN FETs are packaged in improved standard packages, such as the devices from Panasonic (DFN package), On Semiconductors (TO-220) or Transphorm (TO-220, PQFN88). With its near chip-scale GaN*PX* packaging technology the GaN FETs from GaNSystems exhibit a more advanced packaging. They achieve best in class package parasitics e.g. $L_{ds,tot}$ ∼0.8nH (power-path) and $L_{gs,tot}$ ∼3nH (gate-path) for a 650V/7A device.
The given package parasitics allow for a halfbridge PCB design with a total halfbridge loop inductance of ∼4.5nH and a gate-loop inductance of ∼3.5nH (assuming PCB parasitics of roughly 3nH for the power loop and 0.5nH for the gate loop). This is way above the values achieved for the low-voltage GaN FETs and for the PCB integrated power-module packaging discussed before. Especially the high gate-loop inductance, which is critical for stable operation at high dV/dt switching, is a substantial drawback for high speed switching.

4.2 400V/10A GaN Halfbridge Demonstrator

A GaN halfbrdige demonstrator board is designed and built, applying the 650V/34A enhancement mode GaN transistors GS66508P from the manufacturer GaN-Systems. At the time when the halfbridge demonstrator was designed, only limited information on reference designs and application notes were available in literature and from the manufacturers. The main purpose of the demonstrator is therefore to derive and verify a viable gate-drive design and PCB layout, enabling stable hard switched operation of the GaN halfbridge. Further, the low side switch

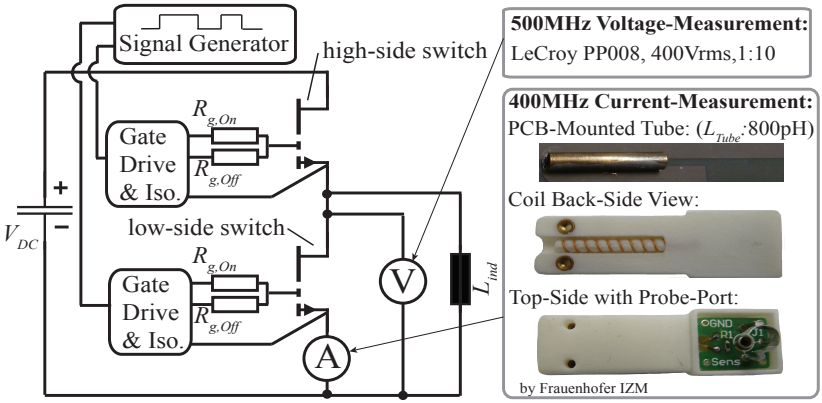


Figure 4.2: GaN halfbridge demonstrator schematic circuit

of the halfbridge is equipped with a high bandwidth current sensor, as shown in fig. 4.2. This allows to perform switching losses measurements, which can later on be used for model based optimization of a GaN converter system.

4.2.1 Gate-Driver Concepts and Design

Compared to the standard silicon semiconductors, GaN devices have similar gate-driving requirements as Si-MOSFETs. The well established gate-driving concepts for MOSFETs, e.g. explained in [103], can therefore be taken as starting point to develop a GaN device gate driver for a specific converter topology. Nevertheless there are also important GaN specific gate drive requirements:

- *Tight gate voltage margin:* GaN transistors exhibit a low margin between the required turn-on gate voltage $V_{gs,on}$ and the absolute maximum gate voltage $V_{gs,max}$ in the range of typically 1...4V [88]. For example the GaN device GS66508P used for the halfbridge demonstrator is operated with $V_{gs,on}$=7V and exhibits a $V_{gs,max}$=±10V.

- *Low gate drive impedance in off-state:* GaN transistors are prone to parasitic turn-on in haflbridge configuration due to their low threshold voltage in combination with the low gate-source capac-

itance and extremely fast switching times [88],[97]. Figure 4.3 schematically shows a GaN transistor with its gate-driver. The equivalent circuit of the GaN transistor includes the non-linear capacitances C_{ds}, C_{gd} and C_{gs}. In halfbridge-operation the blocking voltage V_{ds} increases with a very high dV/dt at the turn-on of the complementary switch. This causes a charging current flowing not only through the drain-source capacitance, but also through the drain-gate capacitance $I_{charge,gd}$. Without any gate-driver connected, $I_{charge,gd}$ flows through C_{gs} and charges the gate, whereas C_{gd} and C_{gs} act as a capacitive voltage divider. Above a certain blocking voltage level the gate voltage reaches the threshold voltage $V_{gs,th}$ and a so called parasitic turn-on happens. The transistor turns on and a high shoot through current flows through the halfbridge, with both transistors being turned on simultaneously. In order the keep the transistor in off-state, the gate driver must sink the charging current $I_{charge,gd}$, such that C_{gs} is not charged to $V_{gs,th}$ and ideally stays constant. Depending on the voltage slope, $I_{charge,gd}$ can reach a peak of several amperes and builds up within nanoseconds. To sink such a current, the gate loop, including gate driver and PCB-traces, must feature a very low total gate resistance $R_{g,Off,tot}$ and gate loop inductance $L_{gs,loop}$. The acceptable maximal gate impedance for a given voltage slope can be calculated with the formulas derived in [103],[97].

- *High dV/dt common mode noise immunity:* In a halfbridge the gate drive of the high-side switch is referenced to the output-potential of the halfbridge, which swings between 0V and V_{DC} at every switching cycle with the same voltage slope as the V_{ds} of the transistors (see fig. 4.2). Depending on the exact realisation of the gate driver, the high-side gate driver is isolated from the ground either with a semiconductor isolation barrier (e.g. bootstrap supply) or by galvanic isolation (e.g. isolated gate-supply, digital isolator). Both exhibit a certain parasitic isolation capacitance. The high dV/dt causes a common mode current, charging the isolation capacitances. This common mode current causes noise on the signal ground, which can disturb the gate signals and lead to a false turn-on of a switch [104]. Such false turn-on must be prevented by an appropriate design of the gate driver.

- *Gate to source leakage current:* Most GaN transistors have a neg-

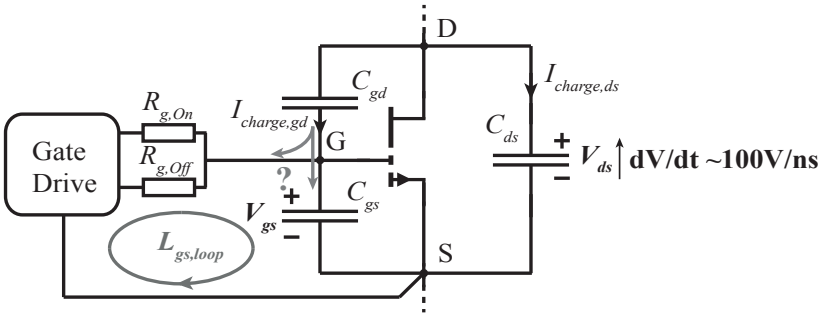


Figure 4.3: GaN transistor parasitic turn-on issue due to Miller-effect at very high $\frac{dV_{ds}}{dt}$.

ligible small gate to source current, as Si-MOSFETs. Though some special types of high voltage GaN transistors exhibit a relatively high gate to source leakage current I_{GS} of up to 50mA [93]. The GaN transistor applied for the halfbridge demonstrator, as well as all other GaN transistors applied in this work, feature a negligible small gate to source current. Gate drivers for GaN transistors with non-negligible gate to source current are discussed in [93],[105],[106], but are not further considered in this work.

These GaN specific gate-drive requirements have the following implications on the gate-drive design.

Gate Supply Voltage Regulation

The tight gate voltage margin requires a precise regulation of the gate supply voltage. The generally applied gate voltage supplies, such as bootstrap circuits or isolated push pull converters [103] are not actively regulated. Due to parasitic effects, such as diode forward voltage or transformer leakage inductance, the output voltage can vary under certain load conditions. To ensure that the gate-voltage does not surpass $V_{gs,max}$ under these conditions, the gate supply output voltage must be actively regulated. There exist dedicated GaN FET drivers, such as the LM5113 from Texas Instruments, which feature an integrated supply voltage clamping. This gate driver is compatible with the eGaN FETs from the manufacturer EPC and limits the gate supply voltage to a maximum of 5.2V.

The GaN transistors GS66508P, applied for the halfbridge demonstrator, are operated with a gate-voltage of $V_{gs,on}$=8V. An adjustable LDO is therefore used to regulate the gate supply voltage to 8V.

Low gate-loop impedance

The total gate drive impedance consists of three parts, the impedance of the gate driver itself, the impedance of the PCB tracks and the discrete gate-resistor. Low gate-loop impedance can be achieved applying an appropriate gate-driver and optimizing the PCB layout.
Gate-drivers especially developed for GaN transistors (e.g. LM5113 and LM5114 from Texas Instruments) tackle this issue featuring split outputs, one for the on-state gate-voltage and one for the off-state gate-voltage with a very low output impedance. Gate drivers with a single output require the use of diodes to separately set the gate-resistor in on- and off-state, which increases the loop impedance.
To reduce the resistance and loop-inductance introduced by the PCB tracks two design constraints are crucial. First the distance between the gate-driver and the gate of the transistor should be kept to a minimum. Second the PCB track from gate-driver to the gate and the return path should be designed as planes rather than small PCB tracks and should be arranged on top of each other on adjacent layers of the PCB. The most beneficial PCB layout depends also very much on the footprint of the GaN transistor. Some devices feature a footprint especially designed for low inductance PCB-layouts [88]. The work in [107] deals with an optimized PCB layout applying also the GaN transistors GS66508P and reports a gate-loop inductance of 0.2nH.
For the halfbridge demonstrator the split output gate-drive LM5114 is applied, which features 7.6A sink-current and 230mΩ sink-resistance. Further the LM5114 is available in a tiny 6-Pin WSON package, which allows for an optimized PCB layout.

Negative Gate-Voltage Offset

GaN transistors with lower voltage rating up to 200V are commonly operated with a gate turn-off voltage of 0V and a boot-strap circuit for the high side switch [88]. With reported voltage rise and fall times of two to four nanoseconds voltage slew rates in the range of dV/dt$\sim$30V/ns are achieved [92]. 600V rated transistors operated with 400V blocking voltage achieve voltage slew rates of typically 100V/ns [90], but even slew

Table 4.1: Isolated gate voltage supply: isolation transformer specification

Transformer Core:	Epcos R10, B64290L0038X087
Transformer Winding:	enameled copper wire d_{CU}=0.25mm
Turns Number:	$N_{prim,I}$:$N_{prim,II}$:$N_{sec,I}$:$N_{sec,II}$=30:30:60:12
Magnetizing Inductance:	$L_{mag,prim}$ = 1mH
Isolation Capacitance:	$C_{iso,primtosec} \approx$ 6pF

rates above 200V/ns are reported [95]. To increase the parasitic turn-on margin and ensure reliable operation most reported designs apply a bipolar gate-voltage with a negative turn-off voltage [93],[95],[104]. The gate voltage is provided by an isolated DC-DC supply.
The halfbridge demonstrator also applies a bipolar gate-voltage of +8V/-2.5V. An isolated push-pull DC-DC converter with a 2.5V and a 9V output delivers the required voltage levels. An LDO is connected to the 9V output, to regulate the turn-on level to 8V. The isolation capacitance of the DC-DC converter adds to the output capacitance of the transistor and causes additional switching losses in hard switched operation. Commercial available integrated isolated DC-DC converters exhibit rather high isolation capacitance of 10-20pF. The designed push-pull DC-DC converter consists of a transformer driver chip MAX258ATA+ and a costum made isolation transformer featuring low isolation capacitance. The isolation transformer design is given in table 4.1.

Low Common Mode Noise Design

To prevent a false turn-on due to noise in the gate-signals, the common mode noise level must be kept below the digital signal threshold. This is achieved by keeping the capacitive coupling to a minimum and apply common mode filter chokes on the signal and power-supply path.
The gate driver design for the halfbridge demonstrator exhibits two galvanically isolated connections between the high-side gate-driver and the reference ground: the digital isolator to transmit the gate-signal and the isolated gate voltage supply. Both are designed for minimal isolation capacitance. The applied digital isolator Si8610BC-B-IS is optimized for high common mode transient immunity and has a input to output isolation capacitance of 2pF. The isolated gate voltage supply applies the custom made isolation transformer (see table 4.1) with an isolation

capacitance of 6pF. The gate signal as well as the DC-DC supply lines are further filtered with common mode chokes (ACM2520-801-3P-T002, ACM2012-201-2P-T002).
Capacitive coupling can also be caused by overlapping of adjacent PCB planes. Therefore the PCB must be layouted such that all copper planes, which are referenced to the output potential of the halfbridge, have a sufficient clearance to copper planes referenced to ground. This clearance constraint applies especially to copper planes on different PCB layers, unlike the clearance required for electrical isolation.

4.2.2 PCB Layout

The halfbridge demonstrator is built on a four layer PCB with 35μm copper thickness. The GaN transistors shall be place on the same side of the PCB, such that a common heat sink could be used for an actual converter design. Voltage and current probing shall be possible from the top-side.
Figure 4.4 a) and b) shows the top- and bottom-side of the designed PCB. The GaN transistors are placed on the back-side and positioned with a minimal distance in between. The DC-link consists of five paralleled MLCC capacitors to reduce the series inductance introduced by the capacitors. The halfbrdige current return path is realized with a copper plane on the mid-layer right underneath. The mid-layer plane is connected with a bank of paralleled vias, to reduce the introduced impedance.
The gate-drivers are also placed on the bottom-side of the PCB as close as possible to the transistors. The gate-supply capacitors are actually also part of the gate-drive loop. To keep the gate-drive loop inductance low this capacitors are placed on the top-side of the PCB right above the gate-drivers. A clearance of minimally two millimeter is maintained between the planes referenced to ground and the planes referenced to the output potential of the halfbridge. This clearance is clearly visible in fig. 4.4 b). The area of the copper planes referenced to the output potential of the halfbridge is kept at a minimum to minimize capacitive coupling to ground. Further the signal and power ground are separated and only connected at one single point, to avoid ground loops.

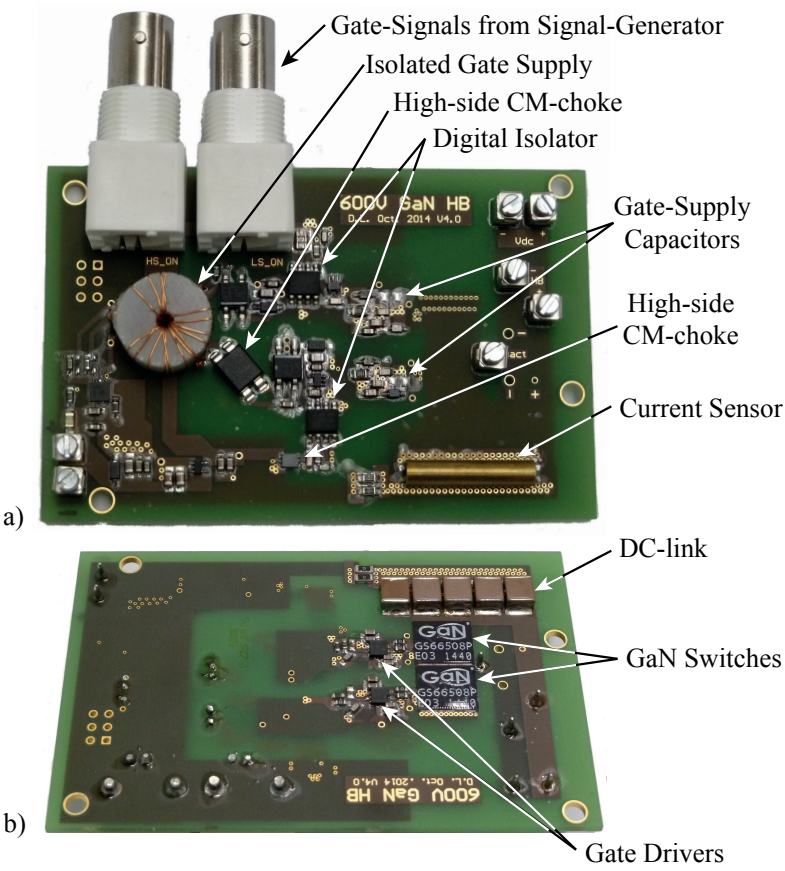


Figure 4.4: Pictures of GaN halfbridge demonstrator a) Top-side, b) Bottom-side

Table 4.2: GaN halfbridge demonstrator: Inductor specification

Inductor Core:	Microlite MP4010MDGC
Winding:	enameled copper wire d_{CU}=1mm, N=47
Inductance:	L_{ind} = 500μH (measured)
Parasitic Capacitance:	$C_{par} \approx$ 3.7pF (measured)

4.2.3 Experimental Results

The experiments on the GaN halfbridge are performed with a $500\mu H$ inductor designed for low parasitic capacitance, as specified in table 4.2. The current and voltage switching waveforms of the low-side switch, see fig. 4.2, are measured with a standard LeCroy PP008 500MHz voltage probe and a high bandwidth current sensor (by Frauenhofer IZM). The current sensor is based on a rogowski coil. It exhibits a bandwidth of 400MHz and only adds 0.35nH additional inductance to the circuit [100]. The output-voltage of the current sensor is sensed with a PP008 voltage probe. The waveforms are traced with the Waverunner 620Zi oscilloscope featuring a sampling rate of 10Gs/s and a bandwidth of 2GHz.

In halfbridge configuration four distinct types of switching operation can be distinguished: turn-on and turn-off with a forward current flowing through the transistor and turn-on and turn-off with a reverse current through the transistor. Note, that the switching with reverse current is not actively initiated, but caused by the turn-on/-off of the complementary switch in the halfbridge conducting a forward current. Figure 4.5 shows the measured switching waveforms for V_{DC}=400V and I_{ind}=6A. With the applied gate-resistors of $R_{g,on}$=10Ω and $R_{g,off}$=2Ω voltage fall- and rise times of ∼10ns are achieved. The voltage overshoot, see the forward-off and reverse-on switching waveforms, is very low. The subsequent oscillation, exhibiting a frequency of ca. 325MHz, is well damped and decays within a few tens of nanoseconds. From the oscillation frequency and the transistor output capacitance (C_{oss}=65pF at V_{ds}=400V) the total commutation loop inductance can be estimated as

$$L_{par,com} \approx \frac{1}{(2\pi \cdot 325MHz)^2 \cdot 65pF} = 3.7nH. \tag{4.1}$$

The transistor GS66508P exhibits low package gate and source inductances of each 0.2nH (see datasheet). Hence in halfbridge configuration the packages account for totally 0.8nH, consequently it is the PCB and the current sensor, which account for the main share of $L_{par,com}$. The current sensor itself exhibits an inductance of 0.8nH (see fig. 4.2). Additionally the integration of the current sensor increases the geometrical dimensions of the PCB tracks forming the commutation loop, which increases the inductance caused by the PCB.

The critical switching operation for parasitic turn-on is the reverse-

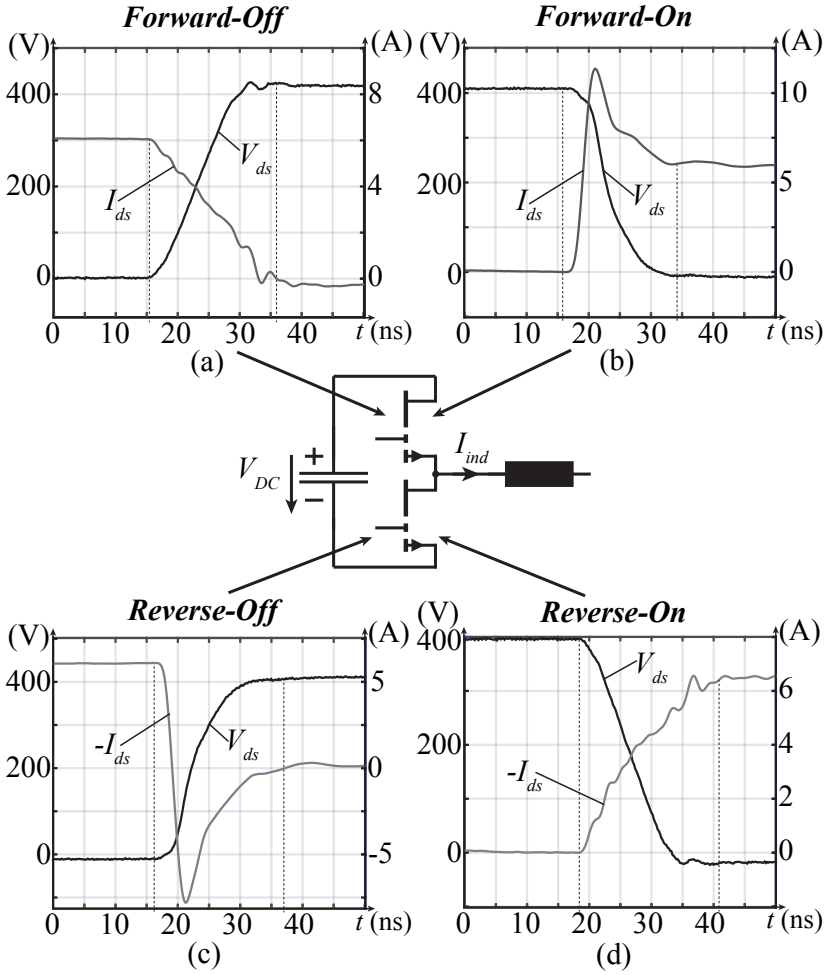


Figure 4.5: GaN halfbridge measured waveforms for 400V/6A hard switched operation (gate-drive: +8V/-2.5V, $R_{g,on}$=10Ω/$R_{g,off}$=2Ω): a) forward current turn-off, b) forward current turn-on, c) reverse current turn-off, d) reverse current turn-on

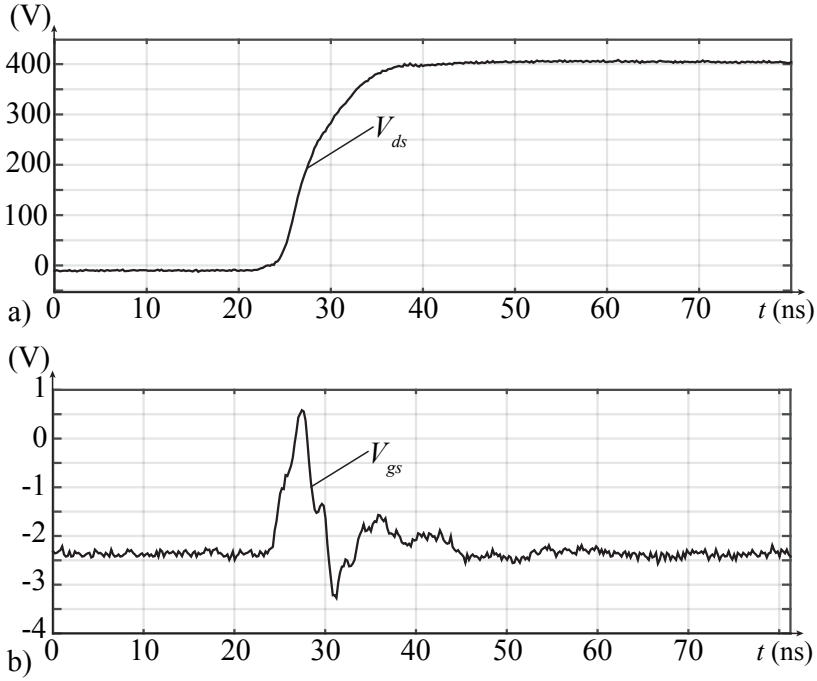


Figure 4.6: GaN halfbridge waveforms at turn-on of complementary switch in halfbridge (400V/8A operation,gate-drive: +8V/-2.5V, $R_{g,on}$=10Ω/$R_{g,off}$=2Ω): a) drain-source voltage, b) gate-source voltage

off switching. Figure 4.6 shows the drain-source voltage V_{ds} and the gate-source voltage V_{gs} at reverse-off switching. The high dV_{ds}/dt induces an oscillation in V_{gs} with a peak of 3V and a frequency of ∼167MHz. Without the negative turn-off voltage V_{gs} would rise well above the threshold of $V_{gs,th}$=1.3V. The gate-loop inductance can again be estimated from the oscillation frequency and the transistor input capacitance (C_{iss}=270pF) as

$$L_{gate,loop} \approx \frac{1}{(2\pi \cdot 167MHz)^2 \cdot 270pF} = 3.4nH, \qquad (4.2)$$

which is mainly caused by the package gate-inductance of 1.8nH and the Kelvin-source-inductance of 1.3nH (see datasheet of the transistor

Table 4.3: Gate-resistor tuning: comparison of switching speed for forward-off switching (I_{ind}=8A, gate-drive: +8V/-2.5V)

Gate-Resistors: $R_{g,on}$=10Ω,$R_{g,off}$=2Ω		
DC-link voltage:	Peak voltage slope	fall-time 90%-10%
V_{DC}=350V	max. dV/dt ≈67V/ns	T_f ≈7.3ns
V_{DC}=400V	max. dV/dt ≈73V/ns	T_f ≈8.6ns
V_{DC}=450V	max. dV/dt ≈80V/ns	T_f ≈9.7ns
Gate-Resistors: $R_{g,on}$=5Ω,$R_{g,off}$=1Ω		
DC-link voltage:	Peak voltage slope	fall-time 90%-10%
V_{DC}=350V	max. dV/dt ≈94V/ns	T_f ≈5.1ns
V_{DC}=400V	max. dV/dt ≈103V/ns	T_f ≈5.8ns
V_{DC}=450V	max. dV/dt ≈113V/ns	T_f ≈6.3ns

GS66508P).
The switching waveforms show, that the V_{ds} voltage-overshoot is not an issue for the considered switching currents up to 10A. It is rather the spike in V_{gs} at reverse-off switching, which puts a limit to the achievable dV/dt in order to avoid destruction of the halfbridge by parasitic turn-on. Though the switching speed is not yet at the limit with the applied gate-resistors of $R_{g,on}$=10Ω and $R_{g,off}$=2Ω. For the tuning of the gate resistors an acceptable maximal spike of $V_{gs,pk,max}$=1.5V at 10A switching current is defined, to guarantee stable and reliable operation. Resistance values of $R_{g,on}$=5Ω and $R_{g,off}$=1Ω are found to feature the fastest feasible switching speed for stable operation up to V_{dc}=450V and I_{ind}=10A. The maximal switching speed is achieved at forward-on, resp. reverse-off, switching. The forward-off switching is considerable slower and is found to mainly depend on the load current I_{ind} and not on $R_{g,off}$. Table 4.3 shows the peak voltage slopes and the voltage fall-times for both gate-resistor settings and different DC-link voltages. The optimized gate-resistor values of $R_{g,on}$=5Ω and $R_{g,off}$=1Ω feature a 35% increased switching speed with a maximal voltage slope of 110V/ns and voltage fall times in the range of 6ns.

Switching Loss Measurements

The switching performance of the halfbridge demonstrator are characterized by double-pulse tests for load currents in the range of I_{ind}=1..8A

and DC-link voltages in the range of V_{DC}=300..450V. For each combination of I_{ind} and V_{DC} the current and voltage waveforms are recorded for all four switching operations, as shown in fig. 4.5. The switching-loss energy is derived by simply integrating the measured voltage and current waveforms during the switching operation. The borders of the integration intervals are marked as dotted vertical lines in the plots in fig. 4.5. The accuracy of the calculated switching loss is determined by the deviation of the voltage measurement Δ_v, the current measurement Δ_i and the time-shift between the two measurements Δ_t as follows

$$\begin{aligned} p(t) = (i_{ds}(t) + \Delta_i)\,(v_{ds}(t + \Delta_t) + \Delta_v) = (i_{ds}(t) + \Delta_i) \\ \left(v_{ds}(t) + \frac{dv_{ds}(t)}{dt}\Delta_t + \Delta_v\right) = v_{ds}(t) \cdot i_{ds}(t) + \Delta p(t) \end{aligned} \tag{4.3}$$

with

$$\begin{aligned} \Delta p(t) = v_{ds}(t) \cdot \Delta_i + \frac{dv_{ds}(t)}{dt}\Delta_t \cdot i_{ds}(t) + \frac{dv_{ds}(t)}{dt}\Delta_t \cdot \Delta_i \\ +\Delta_v \cdot i_{ds}(t) + \Delta_v \cdot \Delta_i. \end{aligned} \tag{4.4}$$

The deviation of the calculated switching energy $\Delta_{E,meas}$ follows by integrating (4.4) over the switching-loss integration interval. The voltage and current measurement deviation are given by the noise-floor of the measured signals and are Δ_v=1.5V and Δ_i=20mA for the performed measurements. The voltage and the output of the Rogowski-coil are both sensed with the same type of voltage probes, having the same time-delay. To check if a relevant phase-shift is introduced by the Rogowski-coil, matching of current and voltage oscillations are checked at forward-off switching. Current and voltage measurement exhibited a correct phase-shift close to 90° at ca. 325MHz oscillation frequency. To account for the uncertainty in the determined phase-shift, a time-delay of Δ_t=±0.3ns (corresponding to ca. ±45° phase-shift) is considered for the accuracy calculation. The measurement deviation $\Delta_{E,meas}$ is in the range of 10% to 20% depending on the measuring point, as listed in table 4.5.
The plausibility of the measured switching losses is further cross-checked with switching losses derived from a PSPICE simulation of the half-bridge. The complete PSPICE model of the GaN transistors is provided by the manufacturer and available online (on: 'www.gansystems.com'). The comparison of the measured and simulated switching losses is given

Table 4.4: Plausibility check of measured GaN halfbridge switching losses with simulated losses derived from a Pspice model at 400V DC-link voltage:

Drain Current I_{ds}:	1.3A	2.2A	4.3A	6A	8.3A
Measurement $E_{Tot,HB}$:	20.7μJ	23.6μJ	27.0μJ	30.8μJ	34.1μJ
Pspice-Model $E_{Tot,HB}$:	20.8μJ	23.1μJ	28.2μJ	32.6μJ	38.0μJ

in table 4.4. The PSPICE model exhibits a good accordance to the measured switching losses.

The measured switching losses are given in figure 4.7 and 4.8 for both gate-resistor sets: $R_{g,on}$=10Ω/$R_{g,off}$=2Ω and $R_{g,on}$=5Ω/$R_{g,off}$=1Ω. The GaN halfbridge exhibits remarkably low switching losses. Total halfbridge switching losses $E_{Tot,HB}$ as low as 20.40μJ are achieved. At reverse-off switching the energy stored in the transistors output capacitance is recovered, which is confirmed by the negative values of the measured switching losses $E_{rvrs,on}$. Despite its 35% increased switching speed the gate-resistor setting with $R_{g,on}$=5Ω/$R_{g,off}$=1Ω only achieves a marginal reduction of $E_{Tot,HB}$, compared to $R_{g,on}$=10Ω/$R_{g,off}$=2Ω. Hence there exist a certain minimum, at which switching losses can not be further reduced by increasing the switching speed.
This effect can be analyzed more in detail by inspecting the switching energies for the two cases. The higher switching speed leads indeed to a reduction of the forward turn-on switching losses $E_{fwd,on}$ by roughly 20%. Though this reduction is largely compensated by increased reverse-off switching losses $E_{rvrs,off}$. The $E_{rvrs,off}$ losses behave actually similar to the reverse recovery losses of a diode in halfbridge configuration, which increase with higher di/dt [108]. However the GaN transistor does not have an intrinsic body diode and exhibits no reverse recovery charge. The possibility of a measurement artefact is excluded, as also the PSPICE simulation confirms an increase of $E_{rvrs,off}$ with higher switching speeds. Another cause for the increase of $E_{rvrs,off}$ with switching-speed could be the package and circuit parasitics, which are known to increase switching losses [98]. Though from the limited information, that the manufacturer provides on the semiconductor structure of the GaN transistor, it is difficult to explain the exact mechanism of this effect.

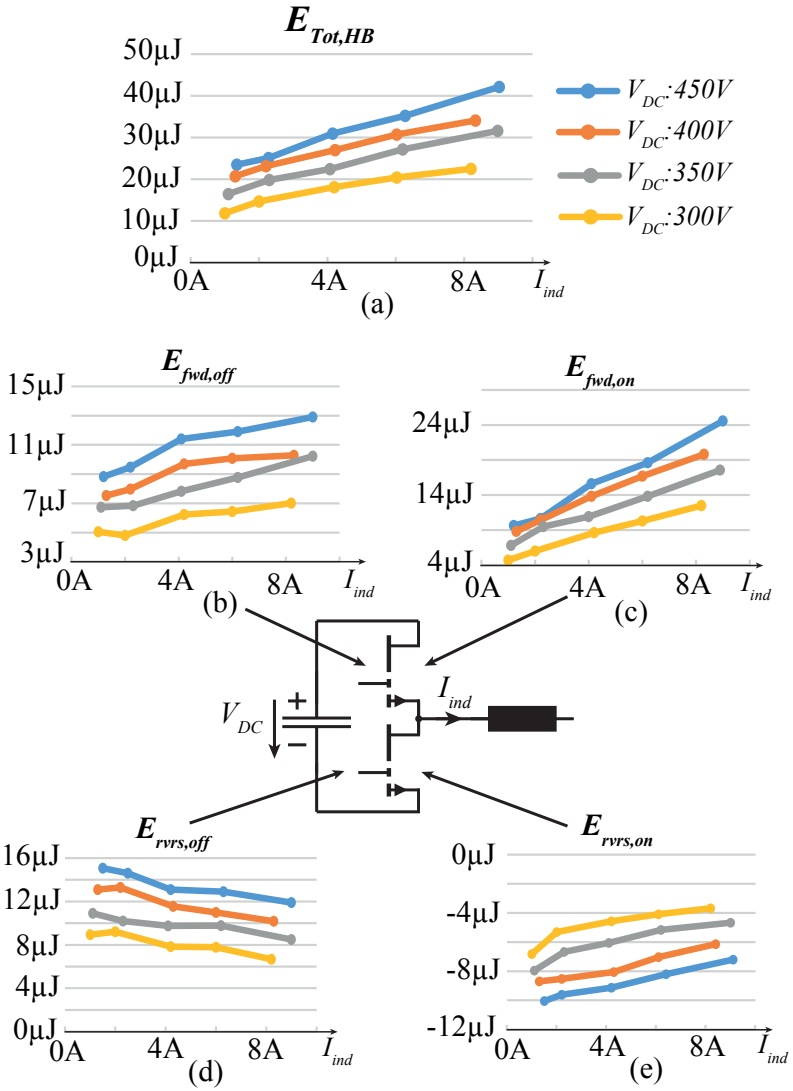


Figure 4.7: GaN halfbridge measured switching losses with Gate-resistors $R_{g,on}$=10Ω,$R_{g,off}$=2Ω: a) total halfbridge switching loss, b) forwad current turn-off losses, c) forward current turn-on losses, d) reverse current turn-off losses, e) reverse current turn-on losses.

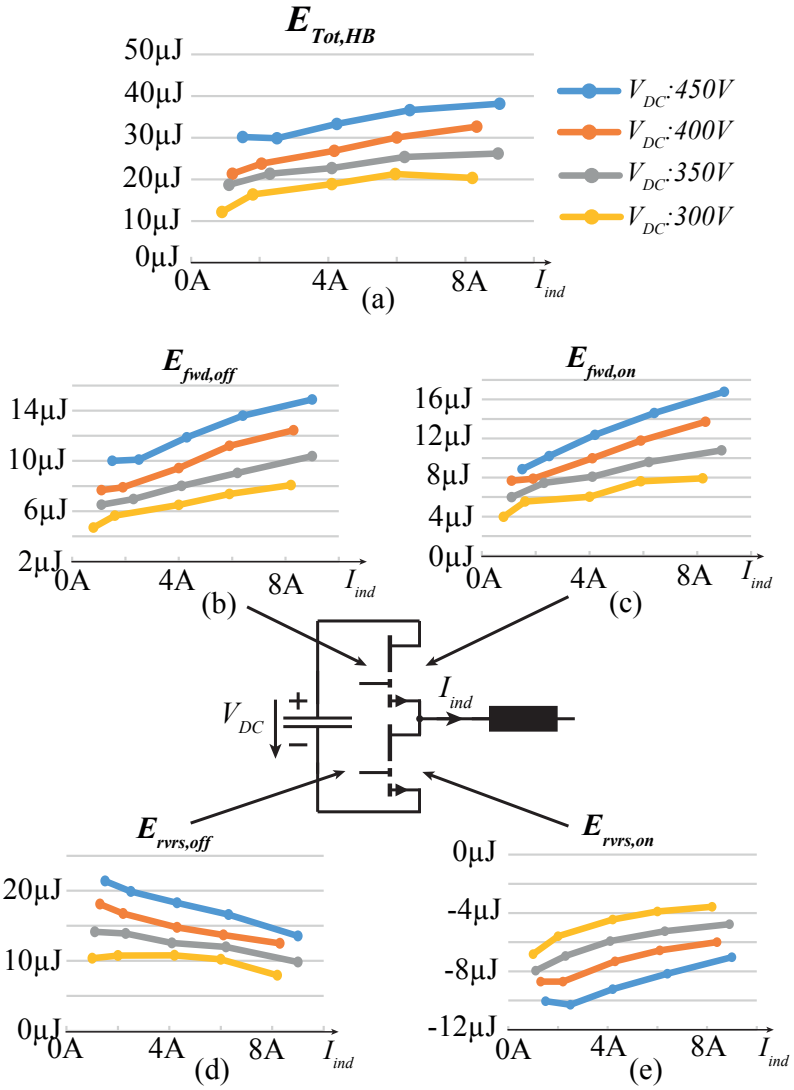


Figure 4.8: GaN halfbridge measured switching losses with Gate-resistors tuned for maximal switching speed $R_{g,on}$=5Ω,$R_{g,off}$=1Ω: a) total halfbridge switching loss, b) forwad current turn-off losses, c) forward current turn-on losses, d) reverse current turn-off losses, e) reverse current turn-on losses.

Table 4.5: Accuracy $\Delta_{E,meas}$ of measured GaN halfbridge switching losses (maximal deviation for both gate-resistor measurement series and all DC-link voltages from 300-450V)

Drain Current I_{ds}:	1.3A	2.2A	4.3A	6A	8.3A
$E_{fwd,off}$:	±9.8%	±9.7%	±9.6%	±9.6%	±10.6%
$E_{fwd,on}$:	±4.7%	±6.0%	±9.9%	±12.1%	±16.3%
$E_{rvrs,off}$:	±9.9%	±6.3%	±6.3%	±7.1%	±8.6%
$E_{rvrs,on}$:	±17.5%	±16.7%	±17.3%	±16.9%	±17.1%

4.3 Summary

Due to their outstanding performance GaN devices allow for the design of PV converters with higher efficiency and/or reduced size of passive components. Low voltage GaN devices up to 200V are already well established with many reference designs and design guidelines available from the manufacturers and in literature. Regarding device packaging, being a major obstacle to reveal the full potential of GaN devices, innovative packaging technologies are applied, featuring ultra low package parasitics. To tackle the problem of commutation loop inductances caused by the PCB layout, Power module IC's integrating a halfbridge on a single chip are about to be developed, reducing the parasitic inductance to merely 0.2nH. The trend will possibly go further with the gate-drivers embedded on the same chip, which would greatly reduce the gate-loop inductance and would enable even higher switching speeds.
High voltage GaN devices with 600V blocking voltage are still a novelty and not fully mature yet. Nevertheless they already outperform the state of the art silicon devices. The experimental results from the 400V/10A halfbridge demonstrator confirmed their excellent performance, exhibiting total halfbridge switching losses of just 30μJ. In comparison, the high speed 5 IGBT series from Infineon are the best in class silicon devices suited for hard switching. The appropriate device for low-power PV-applications, the IKP08N65NH5 with an 8A current rating, exhibits total halfbridge switching losses of 140μJ. The latest silicon MOSFETs, which are though not suited for hard switching due to excessive diode reverse recovery losses, exhibit in fact similar raise- and fall-times as the investigated GaN halfbridge (IPD60R180C7). But the total gate-charge is much increased for the same value of $R_{ds,on}$: 1.5nC for the GS66502B GaN devices compared to 24nC for the IPD60R180C7

MOSFET.
The packaging of the GaN devices appears to be the bottleneck, limiting the performance of the devices. The halfbridge demonstrator achieves a total commutation-loop inductance of $L_{par,com}$=3.7nH and a gate-loop inductance of $L_{gate,loop}$=3.4nH. Whereas the achieved commutation loop inductance might still be an acceptable value for low power applications, the high gate-loop inductance actually limits the maximal achievable switching speed. The best in class packaging technology applies near chip-scale packaging based on PCB-embedding. The packaging technology itself is very promising, though the design of the packages is not optimal yet. Firstly the packages must be optimized for lower gate-loop parasitics. Secondly the devices should be packaged as power modules, hence optimized packaging of two devices in halfbridge configuration. This not only allows to greatly reduce the commutation-loop inductance but also to optimize the EMI behaviour of the halfbridge. Only the combination of these two criteria allows to exploit the full switching speed of GaN devices for practical grid-tied applications.

5

Model Based Design of a Two Stage Multi-Input Converter

The following chapter deals with the modelling and design of the two stage multi-input converter topology, selected in section 2.5 as the most promising candidate for implementing the multi input module integrated converter specified in section 1.2.1. The converter, shown schematically in fig. 5.1, can be classified as a two-stage DC-link topology with passive power-decoupling at the intermediate DC-link, according to the topology-characterization in section 2.1 and 2.2. The converter consists of three paralleled DC-DC Flyback converter stages at the input-side and a DC-AC fullbridge converter for grid-connection on the output-side.

The design of this converter system is a non-trivial task. The multitude of its design variables leads to a vast amount of possible designs,

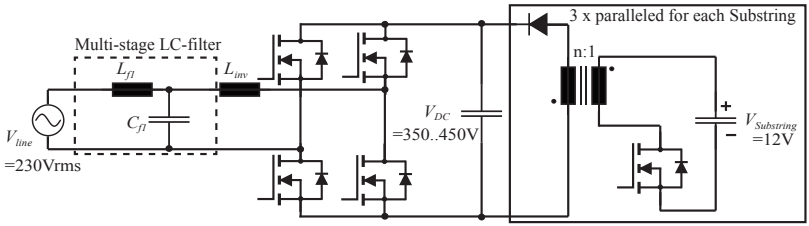


Figure 5.1: Two stage multi-input converter topology with three paralleled 12V DC inputs to 230V AC output and intermediate DC-link power decoupling

which need to be evaluated and compared to find the optimal design. Model based optimization is applied to perform this task: an optimization algorithm iteratively evaluates designs based on a model of the converter and searches for the optimal design variables. Hence an optimization routine consists of two distinct parts, the converter model and the optimization algorithm. The crucial issue, when setting up a model based optimization routine, is to keep calculation time of the optimization routine to an acceptable level. The two key factors, which keep the optimization time low, are discussed below:

- *Fast calculation time of the performance factors:* The converter model, calculating the converter performance factors from a given set of design variables, must be fast to execute. The first and obvious countermeasure, speed optimized coding of the model, is normally not enough to achieve the required calculation speed of the converter model. Such that simplification and approximation methods are applied to reduce the calculation time of the performance factors e.g. [73],[79],[109].

- *An efficient optimization algorithm:* The number of iterations, respectively evaluations of the converter model, executed by the algorithm to converge to the optimal design shall be kept at a minimum. The brute force approach for optimization problems is to sweep through the entire combinatorial range of the design variables. Any optimization algorithms aims to reduce this worst case amount of evaluations by only evaluating the promising designs and skipping the others. The strategies on which the promising designs are identified are manifold. Gradient based algorithms are the most promising approach from a mathematical point of view. Though they can not cope well with discrete design variables [110] typically present in power electronic design problems, and are therefore seldom applied for the design of power electronics [79],[111]. Heuristic algorithms aim to identify beforehand the sets of design variables, which are likely to achieve higher performance, based on the performance of the already evaluated designs. The most prominent of these algorithms are the genetic algorithms (GA), which apply evolutionary techniques to optimize the performance. They can cope well with discrete design variables and are often applied for power electronic design problems, e.g.

[73],[112],[113],[114]. However GAs suffer from non-deterministic results and may fail to converge to a global optimum especially given a larger number of design variables. In contrary to heuristic algorithms, direct search methods apply advanced techniques to identify the promising sets of design variables. These advanced techniques are based on basic system knowledge, e.g. fundamental physic laws of magnetic components or scaling laws of cooling systems etc. Direct search methods are successfully applied for complex optimizations on system level, with many design variables [115],[116].
Which type of algorithm is going to solve a given optimization problem in the most effective way, depends very much on the specific optimization problem.

The two stage multi-input converter is designed with the European efficiency η_{EU} as performance factor [7]. Furthermore the volume of the converter is defined as a constraint, which allows for the derivation of the converters efficiency versus power-density, η-ρ, pareto front applying a single-objective optimization algorithm. To determine η_{EU}, the converter model must calculate the converter efficiency at the following six operating points: $P_{out} = [100\%, 50\%, 30\%, 20\%, 10\%, 5\%] \cdot P_{nom}$. Figure 5.2 schematically shows the operating waveforms for the six operating points. The wide load span of a factor 1:20 has a big influence on the required accuracy of the converter loss model. At low power different loss components are dominant, than at nominal power. When optimizing for nominal load only, these losses can normally be neglected. Though a wide load span optimization requires a model, which accurately models the loss components over the whole load range. This especially involves an accurate, time-consuming modeling of parasitic elements, such as semiconductor non-linear output capacitances and parasitic capacitances and leakage inductance of magnetic components (see section 3).
The entire two stage system, including the magnetic components, requires a set of 20-30 design variables to completely parameterize a design. Keeping in mind the required high modeling accuracy, this optimization problem is too complex to solve within a reasonable time with the available calculation power. The approach chosen in this work, is therefore to split the two stage system. The DC-DC stage and the DC-AC stage are optimized individually for $\eta_{EU,DCDC}$ and $\eta_{EU,DCAC}$. The operating waveforms used for the loss models of each stage are those of

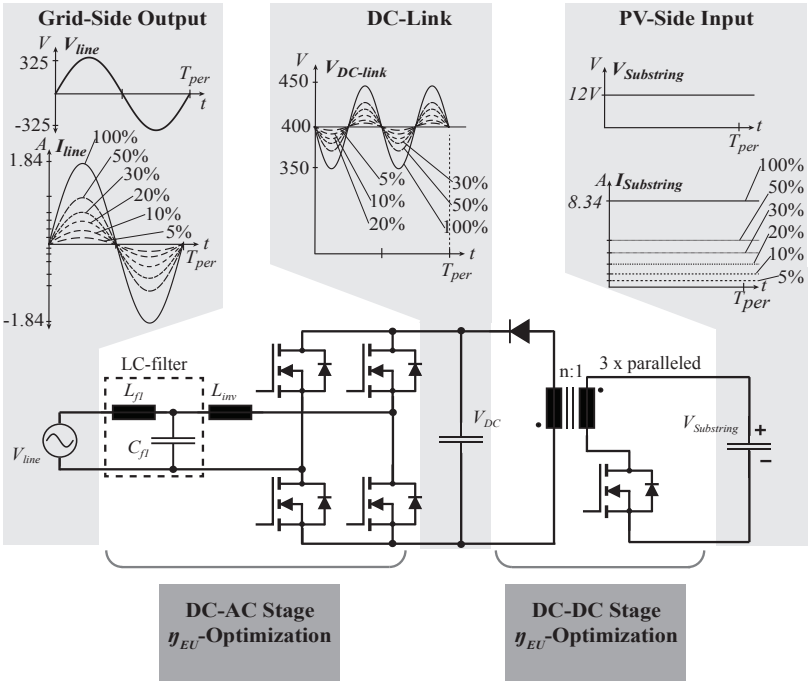


Figure 5.2: Overview of the optimization procedure for European efficiency.

the two stage system with power decoupling, as illustrated in fig. 5.2 The optimization routines implemented for each stage, DC-AC and DC-DC, are described in detail in the following sections. A complete system optimization is subsequently performed which allows to analyse and discuss the performance of the proposed two stage multi input converter in the efficiency versus converter-volume, η-ρ, space.

5.1 DC-DC Flyback Optimization Routine

The first step in any design process is the specification of the system. The DC-DC converter system-specification contains the following parameters, specifying the input and output, the ambient condition and

the volume constraints:

P_{nom}:	Nominal converter output power
V_{substr}:	Input-side PV substring voltage
$\bar{V}_{DC}$:	Output-side average DC-link voltage
C_{DC}:	DC-link power decoupling capacitor
Vol_{trafo}:	Flyback transformer boxed volume
h_{trafo}:	Flyback transformer maximal allowed height
T_{amb}:	Ambient temperature
$T_{trafo,max}$:	Maximal allowed transformer hot-spot temperature at specified T_{amb}

The system specification is the starting point of the optimization routine, illustrated in fig. 5.3. Together with the design variables, the system specification forms the input to the converter model. The design variables define a specific converter design, based on a set of 9 design variables. They can be sectioned into three subgroups.

- *The operating mode* at a specific output power is given by L_{mag}, the transformers magnetizing inductance, and $f_{sw,min}$ and $f_{sw,max}$, the minimal and maximal switching frequency of the converter.
- *The core geometry* is given by the width a and the thickness b of the center core leg. The rest of the core geometry parameters are derived from the specified core volume and the winding arrangement.
- *The winding geometry and placement* is determined by d_s, N_s and $thck_{foil}$ specifying the secondary winding litz wire strand diameter and strands number and the primary winding foil thickness. The interleaving of the primary and secondary winding is specified by a string '*Interleaving*'.

The design variables are iteratively varied by the optimization algorithm, which evaluates and optimizes the performance. The algorithm returns as result the maximal achieved performance and the set of optimal design variables. For this optimization problem with a relatively low number of design variables, a genetic algorithm (GA) from the Matlab toolbox proved to be effective and exhibited good repeatability.
The converter model calculates the converter performance, being the efficiency η_{EU}, for the given design variables and system specification.

As shown in fig. 5.3, the model is sectioned into two main routines, the transformer routine and the flyback converter routine. The latter calculates the operating waveforms for all considered output power levels. The operating waveforms are handed over to the transformer routine and subfunctions calculating semiconductor losses and auxiliary losses. The transformer routine calls a detailed underlaying multi physics model of the flyback transformer including transformer parasitics, a thermal model and the losses. The underlaying magnetic models are derived and described in section 3. The transformer parasitics, L_σ and C_{par}, are handed over to the flyback converter routine, which considers these non-ideal elements for the calculation of the operating waveforms and the losses.
The following subsections give detailed information on the operation of the flyback converter under non-ideal conditions and the semiconductor and auxiliary loss models.

5.1.1 Non-Ideal Flyback Converter Operation

The parasitic elements of the flyback transformer influence the operation of the converter and cause additional losses, depending on the operation mode. In the following subsections, the operation of the non-ideal flyback converter is analyzed for the different operation modes and analytical formulas are derived to calculate the adapted waveforms and the losses caused by the parasitic elements.

Boundary Conduction Mode (BCM)

Figure 5.4 shows simulated current and voltage waveforms of a DC-DC flyback converter operating in BCM. Its switching period is split into four intervals. The first interval, $[t_0, t_1]$, and the third interval $[t_2, t_3]$ correspond to the operation-intervals of an ideal flyback converter. The additional two intervals are due to the charging and discharging of the parasitic transformer capacitance. Figure 5.4, at the bottom, shows the current paths for the four intervals in the circuit diagram. The main current path, driven by the magnetizing current I_{LM}, is denoted with a solid line. At the transition between some of the intervals, damped high frequency resonances dissipate energy stored in the parasitic elements. These high frequency resonance currents are denoted with dotted lines in the circuit diagram. The four intervals are described in the following:

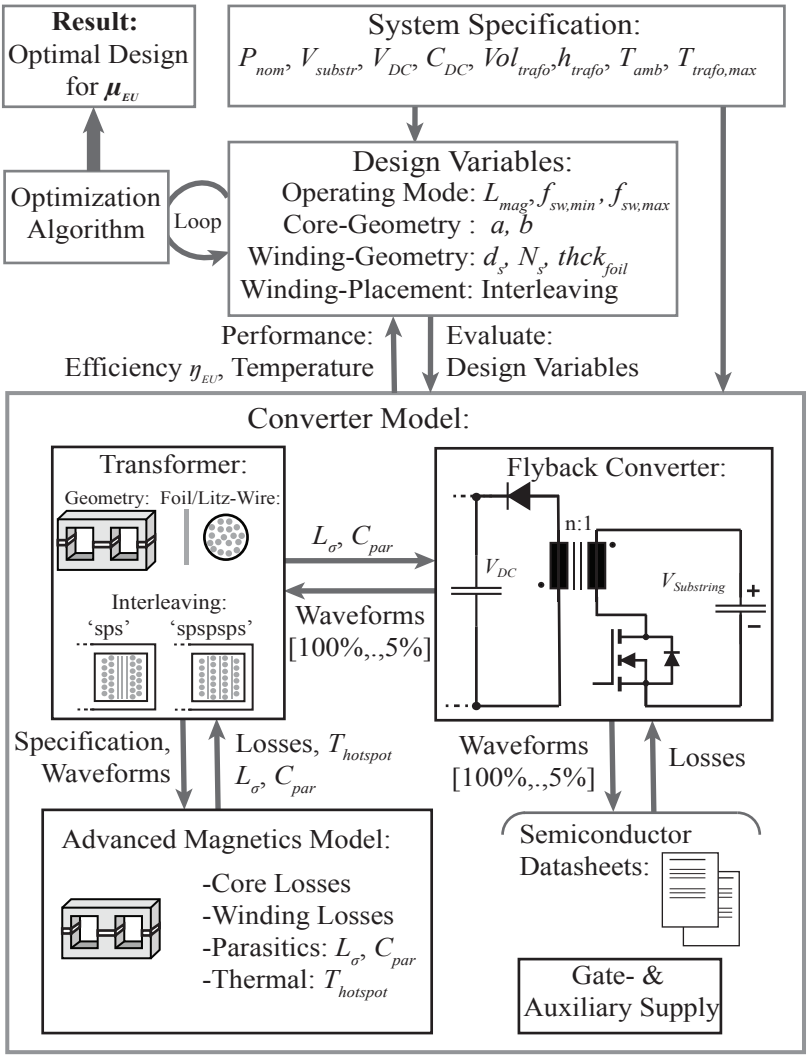


Figure 5.3: DC-DC flyback converter optimization routine.

1) In interval $[t_0, t_1]$ the current builds up in L_σ and L_m.

2) When switch S_1 is turned off at t_1, the capacitor $C_{eq,p}$ is discharged

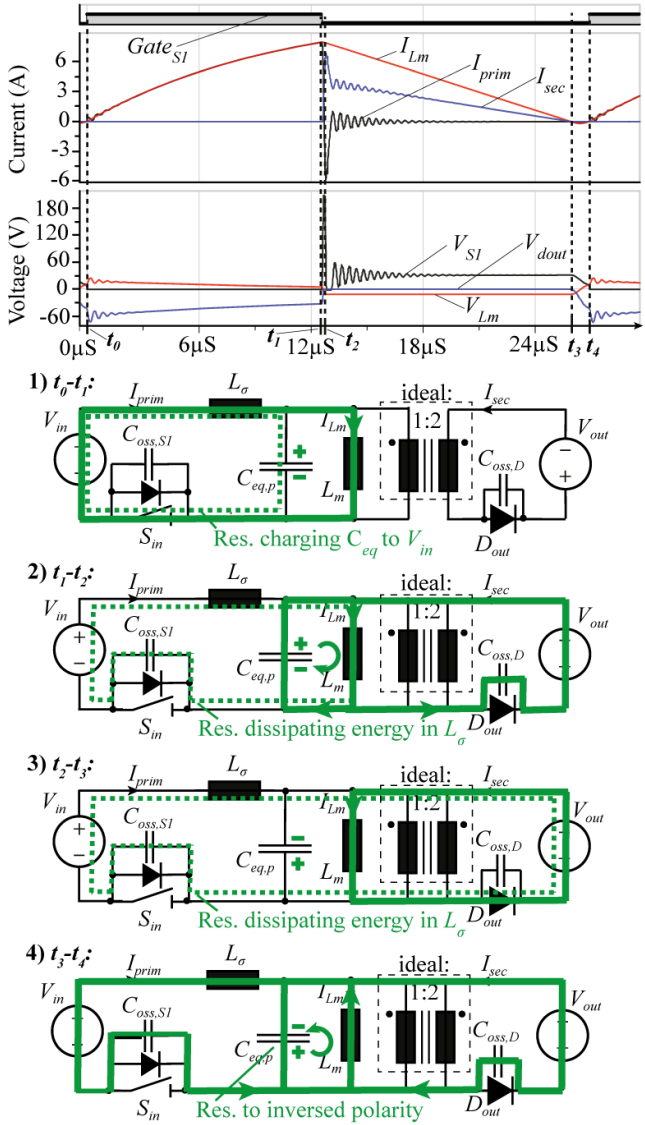


Figure 5.4: Flyback Operation in BCM with valley switching: $V_{in} = 20V$, $V_{out} = 80V$, $n = 2$, $L_{mag} = 20\mu H$, $P = 40W$

by I_{Lm} and reaches the negative value V_{out} at t_2. Simultaneously the energy stored in L_σ is dissipated in a damped resonance starting at t_1 through the elements L_σ, $C_{oss,S1}$ and $R_{wdg,tot,p}$. This resonance further causes an over voltage at switch S_1, which will in most cases require a dissipative clamp circuit to protect the switch. In most practical cases the resonance is sufficiently damped, such that the energy in L_σ is dissipated within one switching period. Under this assumption the losses caused by the leakage inductance can be expressed as:

$$P_{L,lkg} = \frac{1}{2} L_\sigma I_{LM}(t_1)^2 f_{switch}, \tag{5.1}$$

where $I_{LM}(t_1)$ is the current through L_m at the turn-off of S_1 and f_{switch} the instantaneous switching frequency.

3) During the interval $[t_2, t_3]$ the current is flowing through the output side and I_{LM} decreases, reaching zero at t_3.

4) In the following interval $[t_3, t_4]$, a resonant circuit is formed by L_m, $C_{eq,p}$,$C_{oss,S1}$ and $C_{oss,D}$. The voltage of $C_{eq,p}$ being initially $-V_{out}/n$, changes its polarity. At this instant two distinct cases need to be distinguished: valley switching and zero voltage switching.

If $\mid V_{in} \mid > \mid V_{out}/n \mid$, the resonance can not charge $C_{eq,p}$ to V_{in} and switch S_1 is turned on at its minimal blocking voltage $V_{S1,valley} = |V_{in}| - |V_{out}/n|$. Figure 5.5a) shows zoomed in waveforms of this valley switching case. Once the switch is turned on, $C_{eq,p}$ is charged to V_{in} by the damped resonance circuit formed by L_σ, $C_{eq,p}$ and S_1. The surplus-energy dissipated in this charging process, is the energy stored in L_σ during the first half-cycle of the resonance. Based on a standard LCR resonant-circuit these losses can be derived as:

$$P_{C,eq,ValSw} = \frac{1}{2} C_{eq,p} (\mid V_{in} \mid - \mid V_{out}/N \mid)^2 f_{switch}, \tag{5.2}$$

The other case is for $\mid V_{in} \mid \leq \mid V_{out}/N \mid$, where the resonance charges $C_{eq,p}$ to V_{in}, see figure 5.5b). In this case, V_{S1} reaches 0V at t_4 and the antiparallel diode of S_1 begins to conduct. While the diode is conducting, S_1 can be turned on under ZVS conditions. During the charging of $C_{eq,p}$, the input side current I_{prim} consists of two overlaid resonance

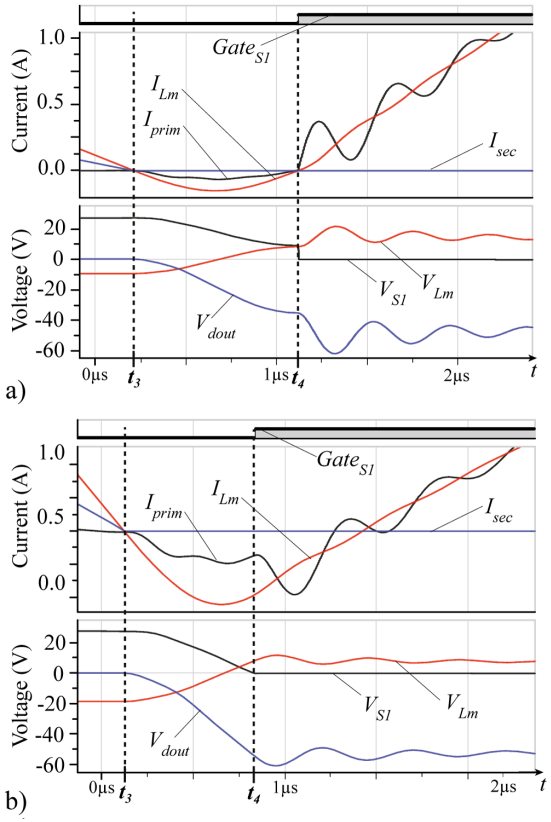


Figure 5.5: Flyback Operation in BCM a) Valley switching, b) Zero voltage switching

currents: the main charging current $I_{prim,chg}$ at the frequency

$$\omega_{chg} = 1/\sqrt{L_m(C_{eq,p} + C_{oss,S1} + n^2 C_{oss,D})} \tag{5.3}$$

for $L_{\sigma \ll L_{mag}}$ and the damped resonance current $I_{prim,res}$ at

$$\omega_{res} = 1/\sqrt{L_\sigma \cdot 1/(1/C_{eq,p} + 1/C_{oss,S1})}. \tag{5.4}$$

Note that the switch output capacitance $C_{oss,S1}$ is actually nonlinearly dependent on the blocking voltage, which would require numerical methods to solve the involved second order differential equations

for V_{S1}. For the following analysis the capacitance is assumed to be constant, with $C_{oss,S1}$ equal to the energy equivalent capacitance at the maximal blocking voltage. The charging current amplitude results from the standard LCR resonant-circuit as

$$\hat{I}_{prim,chg} = C_{oss,S1}\omega_{chg}\frac{\mid V_{out} \mid}{n}, \tag{5.5}$$

and its value at the instant t_4, the end of the resonance, is

$$I_{prim,chg}(t_4) = \hat{I}_{prim,chg}\sin\left[\arccos\left(\frac{V_{in}}{-V_{out}/n}\right)\right]. \tag{5.6}$$

The high frequency resonance is caused by the fact, that the voltage across L_σ at the beginning of the charging interval is $V_{L,\sigma}(t_3)$=0V. Though that V_{S1} can keep track with the charging of $C_{eq,p}$, the initial voltage would need to be

$$V_{L,\sigma,Nores}(t_3) = L_\sigma\frac{dI_{prim,chg}(t_3)}{dt} = -L_\sigma C_{ossS1}\omega_{chg}^2\frac{\mid V_{out} \mid}{n}. \tag{5.7}$$

Consequently a resonance settles this difference, exciting the high frequency current $I_{prim,res}$. This resonance is actually also present for valley switching, however its amplitude is much lower for the given example. Generally, the amplitude of this resonance is negligible small, such that its losses are not considered.

Once switch S_1 turned on at t_4, the magnetizing current starts to increase. As result of the foregoing charging interval, I_{Lm} and I_{prim} do not initially match. A damped resonance through the elements L_σ, S_1 and $C_{eq,p}$ settles this difference. The losses related to this resonance are given by

$$P_{on,ZVS} = \frac{1}{2}L_\sigma[I_{prim,chg}(t_4) - I_{Lm}(t_4)]^2 f_{switch}, \tag{5.8}$$

$$I_{Lm}(t_4) \simeq (C_{eq,p} + C_{oss,S1})\omega_{chg}\frac{\mid V_{out} \mid}{N}\sin\left(\arccos\left(\frac{V_{in}}{-V_{out}/N}\right)\right) \tag{5.9}$$

Besides of directly causing converter losses, the parasitic capacitance also influences the modulation. The resonance interval $[t_3, t_4]$ lowers the switching frequency. Furthermore, because the primary current

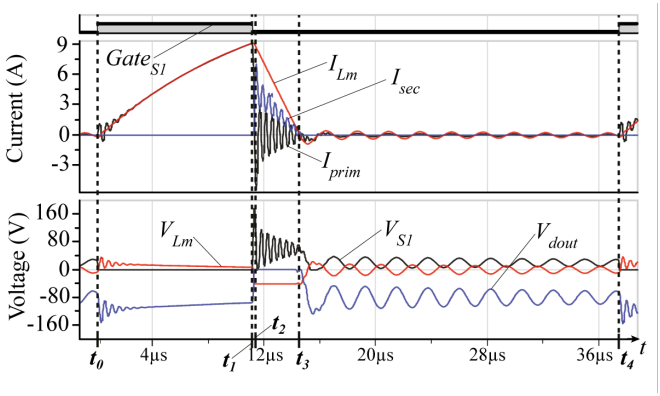


Figure 5.6: Flyback Operation in DCM: $V_{in} = 20V$, $V_{out} = 80V$, $n = 2$, $L_{mag} = 20\mu H$, $P = 20W$

is negative in the interval $[t_3, t_4]$, and for ZVS case also during $[t_0, t_1]$, there is energy fed back to the input. This lowers the transferred energy and will require an increased peak-current to maintain the same power transfer as in ideal operation. Whether these two effects have a relevant influence on the converter losses, depends on the actual transformer design and the operating point.

Discontinuous Conduction Mode (DCM)

The discontinuous conduction mode is very similar to the BCM. Simulation waveforms are shown in fig. 5.6. The current paths are the same as for BCM, see fig. 5.4. The first three intervals $[t_0, t_1]$, $[t_1, t_2]$, $[t_2, t_3]$ are identical to BCM and so is the calculation of the losses caused by the leakage inductance (5.1). In the following resonance interval $[t_3, t_4]$ the switch is not turned on after the first resonance cycle, but $C_{eq,p}$ keeps oscillating with

$$\omega_{res} = 1/\sqrt{L_m(C_{eq,p} + C_{oss,S1} + n^2 C_{oss,D})}. \tag{5.10}$$

Under the assumption of a critically damped RLC series resonance, the initial resonance amplitude $\hat{V}_{eq,p}(t_3) = V_{out}/n$ decays with time by

$$\hat{V}_{eq,p}(t) = V_{out}/n e^{\alpha(t-t_3)} \tag{5.11}$$

where α is given by $\alpha = R_{wdg,1}/(2L_m)$ and $R_{wdg,1}$ is the primary side winding resistance at the resonance frequency. If the resonance did not fully decay within the interval $[t_3, t_4]$, valley switching can be applied at the turn-on of S_1 in the same way as for BCM. The losses involved to charge $C_{eq,p}$ to V_{in} are given by

$$P_{C,eq,DCM} = \frac{1}{2} C_{eq,p} (\mid V_{in} \mid - \hat{V}_{eq,p}(t_4) \mid)^2 f_{switch}. \tag{5.12}$$

Continuous Conduction Mode (CCM)

The continuous conduction mode consists of three intervals, see fig.5.7. The turn off of S_1 at t_1 and the following interval $[t_1, t_2]$ is equivalent to BCM and hence the losses caused by the leakage inductance can be calculated by (5.1). After a fixed time S_1 is turned on at t_3 and a high frequency damped resonance with

$$\omega_{res} = 1/\sqrt{L_\sigma \cdot 1/(1/C_{eq,p} + 1/C_{oss,S1})} \tag{5.13}$$

charges $C_{eq,p}$ from $-V_{out}/N$ to V_{in} and builds up the current in L_σ to I_{Lm}. The losses involved in this resonance can be derived by combining (5.2) and (5.8)

$$P_{on,CCM} = \frac{1}{2} C_{eq,p} (V_{in} + V_{out}/N)^2 f_{switch} + \frac{1}{2} L_\sigma (I_{Lm}(t_3)^2 f_{switch}. \tag{5.14}$$

5.1.2 Semiconductor and Auxiliary Loss Models

The semiconductor losses are calculated solely based on information given in the data sheets. The considered switches are eGaN FETs from the manufacturer EPC. The conduction losses of the GaN FETs are calculated as

$$P_{cond,GaN} = R_{ds,on}(T_j) \cdot I^2_{ds,rms} \tag{5.15}$$

from the rms-current flowing through the device $I_{ds,rms}$ and the on-state resistance $R_{ds,on}$ at the respective junction temperature T_j. It is assumed, that the junction temperature T_j increases relative to the

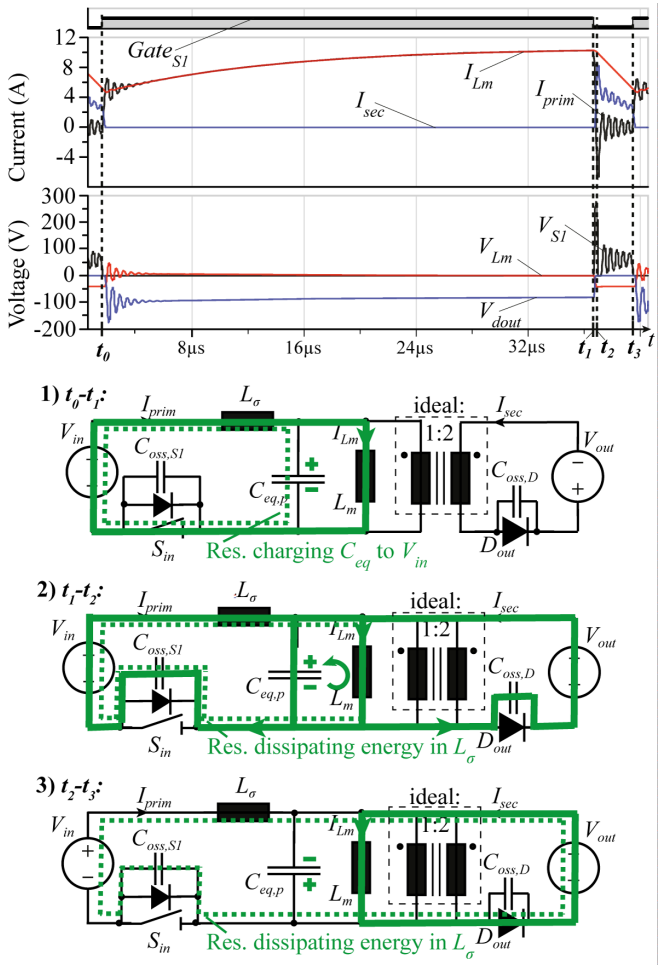


Figure 5.7: Flyback Operation in CCM: $V_{in} = 20V$, $V_{out} = 80V$, $n = 2$, $L_{mag} = 20\mu H$, $P = 150W$

specified T_{amb} by Δ_T=40°C at nominal output power and decays proportional to $I^2_{ds,rms}$ at lower power. The switching losses are calculated with the simple triangular voltage current overlapping model

$$E_{sw,Off,GaN} = V_{ds,off} I_{ds,off} t_{rise} \tag{5.16}$$

$$E_{sw,On,GaN} = V_{ds,on} I_{ds,on} t_{fall} \tag{5.17}$$

where $V_{ds,off}$, $V_{ds,on}$, $I_{ds,off}$, $I_{ds,on}$ are the blocking voltages and drain-source currents at the turn-on, resp. turn-off instant. Derived from [92] t_{rise} and t_{fall} are the drain-source voltage rise and fall time at turn-off and turn-on.
For the output diode a SiC Shottky diode is applied. The SiC diode is assumed not to cause any turn-off losses, as it exhibits no reverse recovery current. The conduction losses for a given conduction interval are calculated by

$$E_{cond,D,SiC} = \int_{t_{on}}^{t_{off}} V_f(I_f, T_j) \cdot I_f(t) dt \tag{5.18}$$

where t_{on},t_{off} are the start and the end time of the conduction interval, $I_f(t)$ is the diode forward current and $V_f(I_f, T_j)$ the diode forward voltage. Again it is assumed, that the junction temperature T_j increases relative to the specified T_{amb} by Δ_T=40°C at nominal output power and decays proportional to $I^2_{f,rms}$ at lower power.

Auxiliary losses are considered, including gate-drive and gate supply losses and supply of the digital isolator for the gate signal and other analog circuits. The gate losses follow as

$$P_{gate} = 2 \cdot Q_{gs} \cdot V_{gs} \cdot f_{sw} \tag{5.19}$$

from the gate charge Q_{gs}, the gate-voltage V_{gs} and the switching frequency f_{sw}. The non-isolated supply is assumed to have an efficiency of 90%. The supply power for the digital isolator and measurement circuits is estimated from the quiescent currents given in the data sheets to P_{analog}= 15mW. The total auxiliary losses follow as

$$P_{aux} = P_{gate} + 0.1 \cdot P_{gate} + P_{analog}. \tag{5.20}$$

5.2 DC-AC Fullbridge Converter Optimization Routine

The optimization routine implemented for the DC-AC fullbridge is illustrated in fig. 5.8. The routine starts with the general specification of the system, given by the following set of parameters:

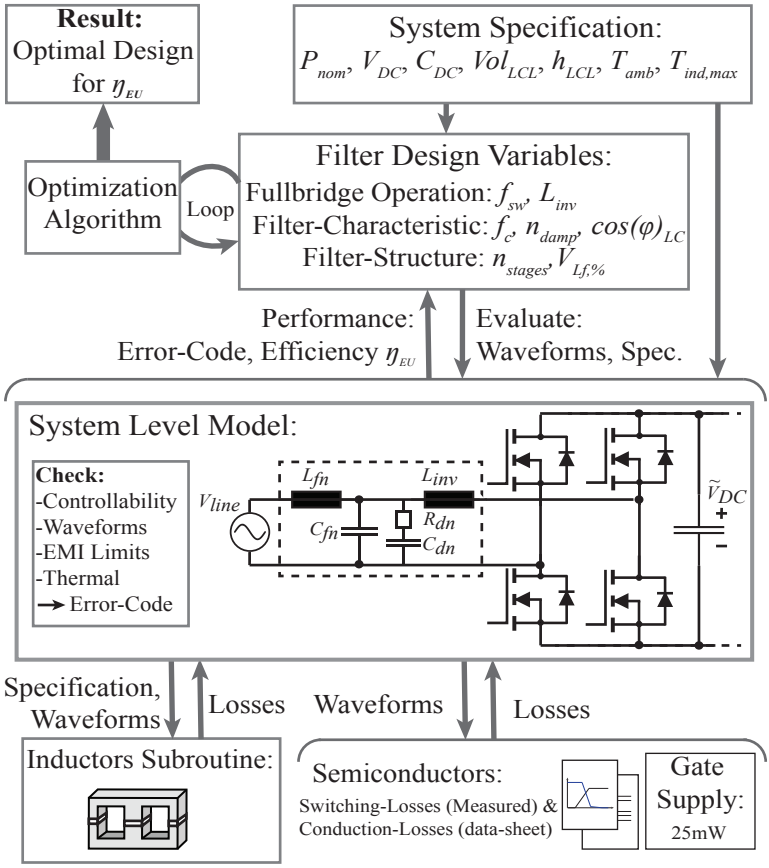


Figure 5.8: DC-AC fullbridge converter optimization including multi-stage LC output differential mode filter.

P_{nom}:	Nominal converter output power
$\bar{V}_{DC}$:	Output-side average DC-link voltage
C_{DC}:	DC-link power decoupling capacitor
Vol_{LCL}:	Boxed volume of the inductor and the output LC filter-stage
h_{LCL}:	Maximal allowed height of the inductors
T_{amb}:	Ambient temperature
$T_{ind,max}$:	Maximal allowed inductor hot-spot temperature at specified T_{amb}

The specific filter design is given by a set of 7 variables, sectioned into 3 groups

- *The fullbridge operation* is determined by the switching frequency f_{sw} and the inductor value L_{inv}.
- *The output filter characteristic* is defined by the filter cut-off frequency f_c, the filter damping coefficient n_{damp} and LC-filter reactive power consumption $cos(\phi)_{LC}$.
- *The output filter structure* is given by n_{stages}, the number of LC-filter stages, and $V_{Lf\%}$, the volume of the filter inductors relative to Vol_{LCL}, the total volume of the inductor and the entire LC filter stage.

The filter design variables and the system specification form the input to the converter model. The converter model is structured into an upper system level part and underlaying component level parts. On the system level the components of the LC-filter are calculated from the given filter characteristic. The filter is damped with a parallel RC-element, as it exhibits a comparable volume as the topologies with a damped filter inductor [115], but features the advantage of lower optimization effort. With all components determined, the operating waveforms are calculated and the feasibility of the filter design is checked, such as the Middlebrook's stability criterion [117] for controllability and EMI limits including additional medium frequency limits as defined in [115]. If the filter design fulfills these requirements, the waveforms and specifications are handed over to the component level routines. Otherwise the execution of the converter model is stopped with an according error-code. As shown in fig. 5.8, the model contains two component level routines, one for the semiconductors and auxiliary and one for the

inductors L_{inv} and L_{fn}. The inductor subroutine contains a complete model based optimization routine with its own subset of inductor design variables, providing an optimally designed inductor for the given specification and waveforms.
The separation of the optimization into a system level and a component-level serves the purpose of reducing complexity and applying the optimal algorithm for each problem. On the one hand the system level design exhibits a high number of combinatorial designs. However the evaluation of a design on system level is fast to evaluate. On the other hand the inductor optimization on component level is more time-consuming to execute, whereas this subproblem has a low number of design variables. A direct search algorithm proposed in [115] is applied for the system-level optimization of the filter design. This algorithm takes into account basic principles of filter-design and stability-analysis, to identify filter design, which are likely to achieve a high performance. In this way the time consuming component level optimization must only be executed for a reduced number of filter designs.
The component level routines are explained more in detail in the following subsections.

5.2.1 Semiconductor and Auxiliary Subroutine

The semiconductor and auxiliary subroutine calculates the auxiliary and semiconductor losses for the given operating waveforms. The semiconductors applied for the DC-AC fullbridge converter are 650V E-HEMT GaN transistors from the manufacturer 'GaN-Systems', applying the reference halfbridge design from section 4. The conduction losses of the GaN E-HEMT are calculated from $I_{ds,rms}$, the rms-current flowing through the device, and $R_{ds,on}(T_j)$, the on resistance of the switch at the respective junction temperature T_j, by

$$P_{cond,GaN} = R_{ds,on}(T_j) \cdot I_{ds,rms}^2. \tag{5.21}$$

It is assumed, that the junction temperature T_j increases relatively to the specified T_{amb} by Δ_T=40°C at nominal output power and decays proportional to $I_{ds,rms}^2$ at lower power. The switching losses $E_{off}(I_{ds}, V_{ds})$, $E_{off}(I_{ds}, V_{ds})$ at given switching voltages V_{ds} and currents I_{ds} are based on the measured switching losses of the reference halfbridge design in section 4. The temperature dependence of the switching losses is assumed to be negligible.

From the gate charge Q_{gs}, the gate-voltage V_{gs} and the switching frequency f_{sw}, the gate losses follow as

$$P_{gate} = 2 \cdot Q_{gs} \cdot V_{gs} \cdot f_{sw}. \tag{5.22}$$

The supply losses include the isolated gate supplies and the supplies of the digital isolators. The supply losses are derived from the GaN-halfbridge design in section 4 as $P_{aux,supply}$=280mW. The total auxiliary losses are

$$P_{aux,tot} = P_{gate} + P_{aux,analog}. \tag{5.23}$$

5.2.2 Inductor Optimization Subroutine

The inductor optimization subroutine performs a complete model based design for the given inductor specification. The specification is handed over from the system-level model and consists of the following parameters:

L_{ind}:	Inductance value
Vol_{ind}:	Boxed volume of the inductor
h_{ind}:	Maximal allowed height of the inductor
T_{amb}:	Ambient temperature
$T_{ind,max}$:	Maximal allowed inductor hot-spot temperature at specified T_{amb}

An overview of the optimization routine is shown in fig. 5.9. In addition to the inductor specification a set of 7 design variables defines the complete inductor design:

a:	Core center leg width
b:	Core center leg thickness
k_{core}:	Core material spec. index
N:	Inductor turns-number
d_s:	Winding litz-wire strand diamater
N_s:	Winding litz-wire strand number
n_{layers}	Winding number of layers

The magnetic model calculates the percental losses at all output power levels for the European efficiency: [100%, 50%, 30%, 20%, 10%, 5%]$\cdot P_{nom}$. The percental loss factor $P_{EU,\%}$ weighted according to the European efficiency [7] is returned as performance factor. By considering weighted

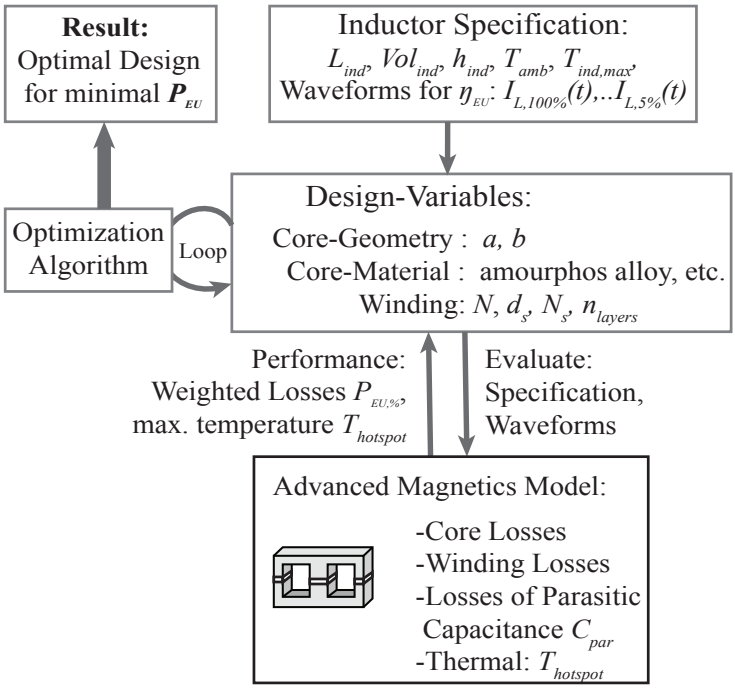


Figure 5.9: Inductor optimizatin procedure for minimizing weighted losses, incorporated as subroutine in the DC-AC fullbridge converter optimization.

losses on the component level, it is aimed to achieve an overall design with optimal weighted efficiency. The loss model not only considers core and winding losses, but also additional losses in hard switched operation caused by the parasitic capacitance of the inductor. A thermal model calculates the winding and core temperature for the nominal output power. The loss and thermal models are based on the advanced magnetic models derived in section 3. The maximal temperature $T_{ind,max}$ is defined as a constraint for the optimization algorithm, in order to guarantee thermal feasability of the optimized inductor. A genetic algorithm (GA) from the Matlab toolbox proved to be well suited for this optimization problem.

Table 5.1: DC-DC stage optimization: specification of system parameters.

P_{nom}:	100W
V_{substr}:	12V
$\bar{V}_{DC}$:	400V
C_{DC}:	28μF
Vol_{trafo}:	30-400cm3
h_{trafo}:	25mm, 37.5mm, 50mm
T_{amb}:	50°C
$T_{trafo,max}$:	90°C

5.3 Model-Based Converter Optimization

First, the DC-DC and the DC-AC stage are optimized individually. The optimization results are then merged to obtain and analyze the total system performance.

5.3.1 DC-DC Flyback Converter

The optimization routine described in section 5.1 is in the following applied to perform a model based optimization of the DC-DC stage. The specification is deducted from the general multi-input AC-module specification in table 1.1. The complete system parameters are given in table 5.1.

The optimization is performed for a fixed nominal substring-voltage of 12V. The DC-link capacitor is selected, such that a power-decoupling ripple of $\Delta_{V_{DC}}$=50V results (see section 2.5.1). To obtain the η-ρ pareto front different optimization runs are carried out for a varying transformer volume from 30cm^3 to 400cm^3. The height of the transformer is constrained to a low profile of 25mm. The influence of the transformer height on the system efficiency is investigated by additional optimization runs for a transformer height of 37.5mm and 50mm. The transformer hot-spot temperature $T_{trafo,max}$ is constrained to raise maximally 40°C above the ambient temperature. This limit is chosen, because the converter shall not exceed a targeted maximal temperature of 125°C at the worst case ambient temperature of 85°C.

Component and Material Selection

For the model based optimization of the DC-DC converter the following components and materials are considered:

- *Semiconductors:* Fourth generation eGaN FETs from the manufacturer EPC are applied for the primary side switch S_1. The 100V/4mΩ device EPC2032 is considered for the design. Among EPC's product portfolio it is the most suited device. A lower blocking voltage would result in a lower margin for over voltage spikes and derate life-time and reliability. A higher voltage rated device would either have higher conduction or switching losses. On the output side of the flyback converter a SiC Shottky diode is applied due to its excellent reverse-recovery behaviour. Among the required 1.2kV blocking voltage devices, the lowest available current rating is in the range of $\sim$2A. The 1.2kV/2A rated diode C4D0212E from Cree is found to feature the lowest V_F among the commercially available SiC diodes with 2A current rating.

- *Magnetic Materials:* The current of a flyback-transformer in BCM exhibits a large ripple at high frequencies. This requires a core-material with low high-frequency losses, such as ferrite-, powder- and nano crystalline cores. To allow the manufacturing of a transformer winding with low leakage inductance a cut-core is required, hence C- or E-type cores. Further an actual optimized design will rely on a custom made core-shape, hence easy manufacturing of relatively small custom made core-shapes must be possible. These requirements identifies ferrite as the most suitable core-material. For the given flyback transformer optimization the Si-ferrites N87, N97 and N49 from Epcos are considered.

- *Cooling System:* The converter is solely cooled by free convection. The transformer is cooled through its surface only, not using any additional heat-sinks or cooling pipes. The GaN transistor and the SiC diode are cooled from the top-side with small standard-size black anodized heat-sinks.

Volume versus Efficiency Optimization

The optimization-results are given in figure 5.10, illustrating the η-ρ pareto-front of the DC-DC converter with the efficiency η_{EU} plotted

versus the boxed volume of the flyback transformer.
Among the considered ferrite materials, SiFerrite N49 appeares to be the best core-material for all designs, owing to its lower high frequency losses. With the actual transformer height constraint of 25mm the efficiency reaches a plateau at an efficiency of 96.8% and a volume of 60-100cm^3. The efficiency decreases with decreasing transformer volume. At a volume of 40cm^3 and an efficiency of η_{EU}=96.5%, the thermal limit $T_{ind,max}$ is reached. The transformer hot-spot temperature appears to be in the layers of the interleaved transformer windings. A further volume-reduction would require additional cooling of the transformer. Despite the fact, that in general the losses of magnetic components decrease with higher component volume, the DC-DC stage efficiency drops at volumes above 100cm^3. Due to the limited transformer height the increase of the volume comes at the expense of a higher mean turns-length of the transformer winding. This increases the transformer parasitic elements, being the leakage inductance and the interwinding capacitance, and the converter losses caused by these elements. At the point where the increased parasitic losses outweigh the reduction in magnetic losses, total converter efficiency drops despite an increased transformer volume. When the height constraint is increased, the efficiency raises well above 96.8% as can be seen in fig. 5.10 for a transformer height of 37.5mm and 50mm. At a transformer volume of 200cm^3 the DC-DC stage efficiency reaches η_{EU} ∼97.5% for either transformer heights. A further volume increase only marginally increases the efficiency for the 50mm height constraint. With 37.5mm height constraint the efficiency slowly drops at volumes above 200cm^3 due to the same effect discussed above.
The optimization reveals a strong influence of the low-profile constraint on the achievable performance. Moreover a DC-DC stage efficiency above η_{EU}=96.5% only comes at the expense of a highly increased volume. To achieve an efficiency of 97%, the volume must increase by a factor two and the low-profile constraint must be loosened.

5.3.2 DC-AC Fullbridge Converter

Applying the optimization routine from sec. 5.2, a model-based optimization of the DC-AC stage is carried out. The system parameters specified in table 5.2, serve as input for the optimization routine and are derived from the general multi-input AC-module specification (see table

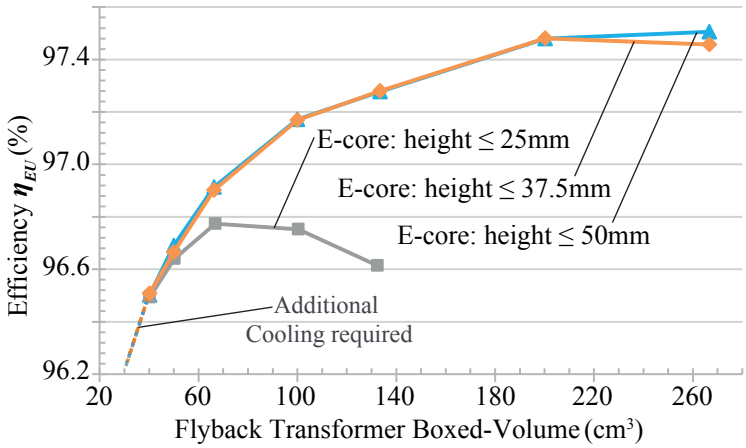


Figure 5.10: DC-DC Stage efficiency optimization results: η_{EU} versus transformer volume, η-ρ pareto-front

Table 5.2: DC-AC stage optimization: specification of system parameters.

P_{nom}:	300W
$\bar{V}_{DC}$:	400V
C_{DC}:	28μF
Vol_{LCL}:	60-200cm3
h_{LCL}:	25mm (35mm, 50mm)
T_{amb}:	50°C
$T_{ind,max}$:	90°C

1.1). The DC-link capacitor is designed for a maximal power-decoupling ripple of $\Delta_{V_{DC}}$=50V (see section 2.5.1). The specified maximal boxed volume of the differential mode filter and the inductor Vol_{LCL} is gradually varied from 60cm^3 to 200cm^3 to obtain the η-ρ pareto front. The maximal height of the filter and inductor are limited to 25mm. Though, if for a given core-material no feasible inductor design results, the core-height constraint is gradually loosened up to 50mm in order to allow for a feasible inductor design. For the same reason as for the DC-DC optimization, the maximal inductor hot-spot temperature is constrained to increase not more than 40°C above the assumed ambient temperature of 50°C.

Component and Material Selection

In the following the components and materials are described, which are considered for the model based optimization of the DC-AC fullbridge converter:

- *Semiconductors:* 650V E-HEMT GaN transistors are applied for the fullbridge converter offering unprecedented switching performance. The considered 650V/30A device GS66508P from the manufacturer GaN Systems is surely overrated for the 300W nominal output power of the converter. Though GaN transistors in the 600V category are still a technological novelty and devices are only available in a limited amount as engineering samples. The GS66508P was the first device available from the GS665-familiy of transistors with the 650V/7A GS66502 to be released later. Therefore its performance has been characterized by means of a GaN halfbridge reference design, see section 4, and consequently the GS66508P is considered for the given design.

- *Magnetic Materials:* The inductor of the DC-AC fullbridge inverter is exposed to a sinusoidal load current at line frequency and an overlaid current-ripple at switching frequency. The current flowing through the filter inductor is approximately sinusoidal at line frequency, with the switching ripple being greatly reduced. To enable a compact design of the filter and inductor a core-material featuring high magnetic permeability and a high saturation flux-density would be optimally suited. For the inductor the material must further feature low high frequency losses. Among the magnetic materials powder cores, amorphous alloy cores and nanocrystalline cores are a viable option. Iron-cores are not considered due to their high losses. For the model-based optimization of the inductor the following core-materials are taken into account: amorphous alloy gapped C-cores (Metglas 2605SA1, Hitachi Metals), toroid powder cores with distributed airgap (Microlite DGC cores, Hitachi Metals) and nanocrystalline gapped C-cores (Vitroperm 500F cut cores, Vacuum Schmelze). For the filter-inductors toroid powder cores from the following materials are considered: Microlite DGC cores (Hitachi Metals), HighFlux and MPP powder cores (Magnetics).

- *Cooling System:* All components are cooled by free convection.

The magnetic components are cooled through their surface only, not using any additional heat-sinks or cooling pipes. The GaN transistors are cooled from the back-side with small standard-size black anodized heat-sinks [118].

Volume versus Efficiency Optimization

An according set of optimization runs is performed, to derived the efficiency versus volume, η-ρ, pareto front. Figure 6.10 plots the achieved efficiency η_{EU} versus the boxed volume Vol_{LCL} for the three different considered inductor core-materials. Further the switching frequency is given for all points forming the pareto front. The three inductor designs are listed in table 5.3. For all designs the filter inductors are toroidal powder cores, whereas the optimization reveals Microlite as the optimal core-material for the filter inductors.
Firstly, the Vitroperm design applies a gapped C-core of the nanocrystalline Vitroperm 500F material. The low profile C-core fulfills the 25mm height constraint.
Secondly, the Microlite design consists of a inductor with a Microlite DGC toroidal core. At the original height constraint of h_{LCL}=25mm, no feasible inductor designs are possible, due to the winding temperature exceeding the maximal temperature constraint. The optimized Microlite inductors exhibit a turns-number and core-area in the same range as the Vitroperm inductor designs. Though, for the toroid-geometry the radius of the inner hole also enters into the total inductor height. Hence the height constraint limits the winding window size to smaller values, requiring smaller conductor-diameter and increasing winding losses. The aim of the model-based optimization is to evaluate and compare the performance of the different core-materials and not the core-shapes. Therefore this geometry-related drawback is accounted for with an increased height-constraint of 35mm, allowing for conductor-diameters in the same range as for the Vitroperm design.
Thirdly, the Metglas design uses a gapped C-core of the amorphous material Metglas 2605SA1. At switching-frequency the 2605SA1-material exhibits substantially higher core-losses than the Microlite and Vitroperm 500F materials. A loss-optimized design compensates the higher core-losses with a higher inductor turns number, typically three times higher than for the Vitroperm and the Microlite designs. Moreover a low-profile core-design increases both the magnetic path-length and the mean winding turns-length. Even higher core-losses and winding

Table 5.3: DC-AC stage optimization: the three inductor designs.

Design Name:	Ind. L_{inv}:	Filter Ind. L_{fn}:	Max. heigth
Vitroperm	Vitroperm 500F gapped C-core	Microlite Powder DGC Toroid	h_{LCL} = 25mm
Microlite	Microlite Powder DGC Toroid	Microlite Powder DGC Toroid	h_{LCL} = 35mm
Metglas	Metglas 2605SA1 gapped C-core	Microlite Powder DGC Toroid	h_{LCL} = 50mm

losses result, causing temperature hot-spots above the specified maximum. Increasing the allowed inductor height reduces the magnetic path-length and the mean turns-length. Even though an increased component height increases the thermal resistance from winding to ambient, the reduction in losses showed to overcompensate the increase in thermal resistance for the considered designs. The temperature-limitations are therefore mitigated by increasing the height constraint to 50mm, which enables feasible inductor designs to a volume of Vol_{LCL}=120cm^3.

The optimization clearly shows, that the performance of the DC-AC stage correlates with the performance of the applied core-material. In the frequency and flux-density range, relevant for the switching-ripple, the Microlite and the Metglas 2605SA1 material exhibit approximately three and eight times higher core-losses than the Vitroperm 500F material (see Appendix B). The superior characteristic of the nanocrystalline Vitroperm material results in both a higher efficiency and a more compact volume. Depending on the volume, a DC-AC stage efficiency between 98% and 98.5% can be achieved. The optimal switching frequency is 40kHz for a compact volume of 60cm^3 and decreases to 20kHz with increasing volume.

The Microlite design ranks second in efficiency. It allows for an efficiency of 97.8%. The optimal switching frequency is 40kHz. As the optimization algorithm varies f_{sw} in discrete 2.5kHz steps and the sensitivity of the efficiency to the switching frequency is relatively small, the optimal switching frequency is the same for all considered volumes. The Metglas design exhibits the lowest efficiency of 97.2%. Again the optimal switching frequency is 40kHz for all considered volumes, for the same reason mentioned before.

The Vitroperm design also enables the most compact design. The

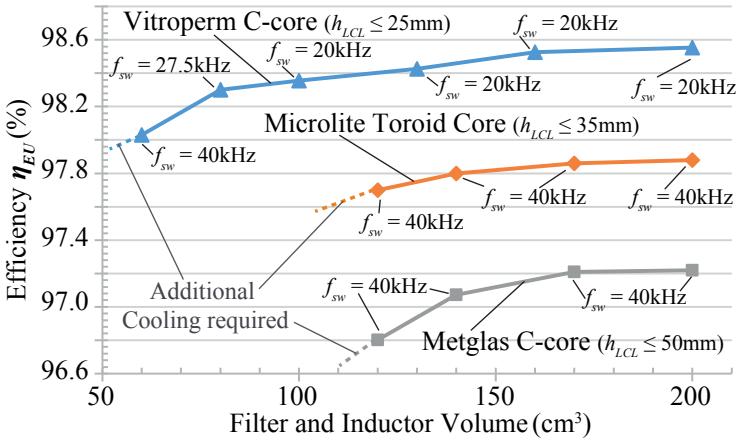


Figure 5.11: DC-AC Stage efficiency optimization results: η_{EU} versus Vol_{LCL}, the total boxed volume of the inductor and the differential mode filter

volume-limit, below which additional cooling with heat-pipes or fans becomes necessary, is at 60cm^3. For the other designs the volume-limit is already reached at 120cm^3.

5.3.3 Optimized Multi-Input AC-Module Performance

The performance of the complete two-stage multi-input AC-module, consisting of one DC-AC stage and three paralleled DC-DC stages, is derived from the optimization results of the DC-DC and the DC-AC stage. For each of the optimized DC-DC and DC-AC designs in figure 5.10 and 6.10 the total losses are calculated at all output power levels for the European efficiency. The European efficiency is calculated out of the sum of the DC-AC and DC-DC stage losses. The loss-models of the DC-AC and DC-DC stage contain auxiliary losses caused by gate-drivers, gate-supply and analog measurement circuits, see eq. (5.23) and (5.20). Though a microcontroller, required for the actual operation of the converters, is not yet included in the loss models. The power-consumption of a single microcontroller, operating all four stages, is therefore considered on the system level. Among other low-power micro controllers, the DSP from the TI piccolo series TMS320F2807x is one viable option,

Table 5.4: Multi-input AC-module optimization designs.

Design Name:	DC-AC Stage	DC-DC Stages
Vitroperm DC-AC, h_{DCDC}=37.5mm	L_{inv}: Vitroperm 500F C-core L_{fn}: Microlite DGC Toroid	Si-Ferrite N49 core h_{trafo} = 37.5mm
Vitroperm DC-AC, h_{DCDC}=25mm	L_{inv}: Vitroperm 500F C-core L_{fn}: Microlite DGC Toroid	Si-Ferrite N49 core h_{trafo} = 25mm
Microlite DC-AC, h_{DCDC}=37.5mm	L_{inv}: Microlite DGC Toroid L_{fn}: Microlite DGC Toroid	Si-Ferrite N49 core h_{trafo} = 37.5mm
Microlite DC-AC, h_{DCDC}=25mm	L_{inv}: Microlite DGC Toroid L_{fn}: Microlite DGC Toroid	Si-Ferrite N49 core h_{trafo} = 25mm

featuring an optimized low power consumption of 490mW. Moreover to fulfill the safety regulations a relay is required to disconnect the system from the grid. Such a relay typically adds another 250mW of losses. Taking into-account the micro-controller and the line-relay the total power-consumption of $P_{syst,aux}$=750mW is added to the losses. Summing up the volume of the DC-AC and the three DC-DC stages, the total magnetic components and filter volume is derived. From the combination of the DC-DC and DC-AC designs, four two-stage designs can be distinguished, based on the applied core-materials and component heights. The four designs are listed in table 5.4 and the corresponding η-ρ pareto fronts are shown in figure 6.10.

The application of a nanocrystalline Vitroperm core as inductor enables a European efficiency in the range of η_{EU}=94...94.5% at a relatively compact magnetics and filter volume of 200cm^3 to 300cm^3. The low-profile constraint of h_{mag}=25mm does only bring a slight efficiency drawback up to 0.1% in this volume-range. To increase the efficiency above 94.5% requires an ever increasing volume and a loosened height constraint of 37.5mm for the DC-DC stage. The efficiency benchmark of 95% can only be reached at the expense of an excessive magnetics and filter volume of 600cm^3.
With Microlite toroidal powder cores applied for the inductor, efficiency is ca. 0.7% lower over all volumes. An efficiency of η_{EU}=93.5% can be achieved at a volume of 250cm^3. To increase the efficiency to 94%, the height constraint must be loosened to 37.5mm and the volume must be increased to 400cm^3. An excessive magnetics and filter volume as high as 800cm^3 is required, to achieve an efficiency of 94.5%.

The power consumption of the controler $P_{control}$ greatly reduces sys-

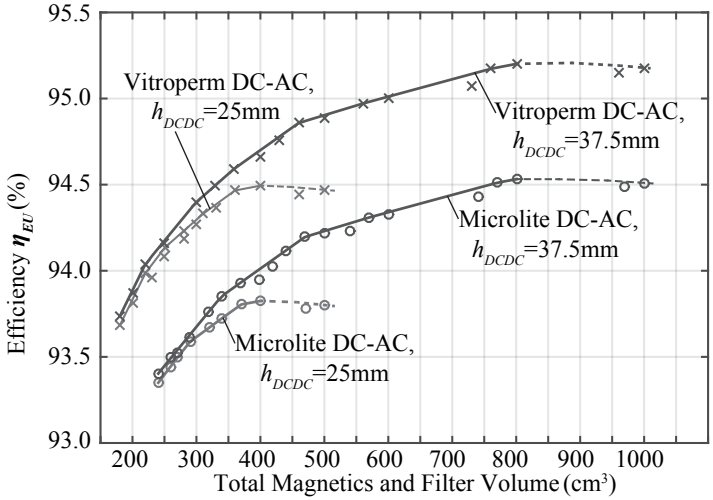


Figure 5.12: Multi-input AC-module optimization η-ρ pareto-front: η_{EU} versus the total volume of the magnetics and filter components.

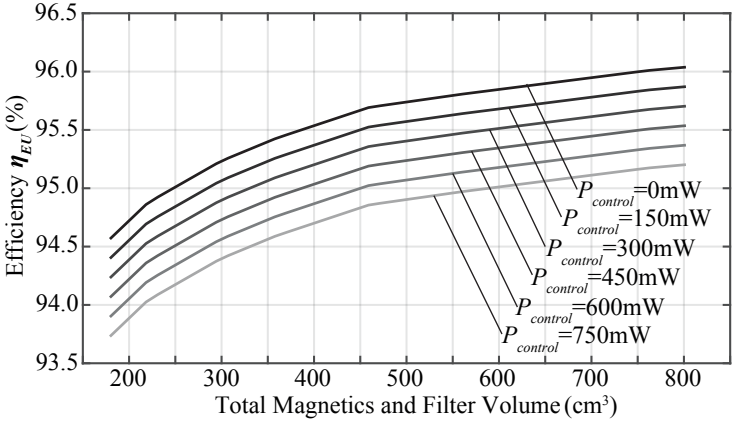


Figure 5.13: Multi-input AC-module η-ρ pareto-front for Vitroperm DC-AC, h_{DCDC}=37.5mm design: influence of controller power-consumption $P_{control}$ on system efficiency

tem efficiency at the low output power. Consequently, the European efficiency of the AC-module is very sensitive to $P_{control}$. Figure 5.13 shows the η-ρ pareto-front of the Vitroperm DC-AC, h_{DCDC}=37.5mm design for different $P_{control}$ power-levels. A control-power of 100mW directly translates into a 0.1% reduced European efficiency. It is therefore crucial to implement the two-stage system control with power-optimized microcontrollers.

6 Prototype Systems

To experimentally evaluate the multi-input AC-module, prototypes of the DC-DC stage and the DC-AC stage are built. For each stage an optimized design is performed and an according prototype is built. The prototypes are characterized by efficiency measurements. This allows to validate the applied converter models and analyze the total two-stage system performance.

6.1 DC-DC Flyback GaN/SiC Converter Prototype

6.1.1 Flyback Converter Design

The design of the DC-DC flyback prototype is performed with the model based optimization described in section 5.1. Though the following components are selected in advance and fixed for the optimisation: a PM5039 N87 core for the transformer, a 180μm copper-foil for the primary winding, a 7x0.1mm Litz wire for the secondary winding, an EPC2032 GaN switch on the converter input-side and a SiC Schottky diode on the output-side.
Figure 6.1 shows the efficiency and volume of the prototype design in comparison to the η-ρ pareto front. The efficiency of the prototype design lays 0.4% below the actual pareto front. In comparison to the pareto optimal core, the standard-core PM5039 has a lower core-area and a higher winding-window and is made of ferrite N87, instead of the optimal N49 ferrite.

The schematic in fig. 6.2a) shows the components used to build the

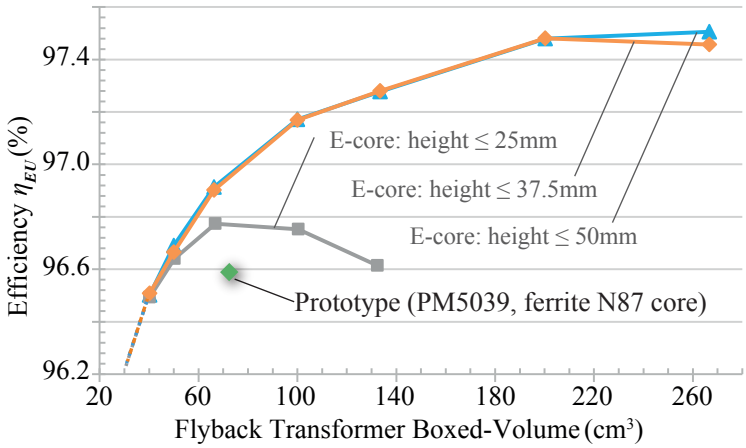


Figure 6.1: Efficiency of the designed prototype and the DC-DC stage η-ρ pareto-front (derived in section 5.3.1).

flyback converter. Besides the basic flyback converter components, a passive clamp-circuit is used to damp the voltage overshoot at turn off, caused by the transformer leakage inductance. The detailed converter component list is given in table 6.1. The transformer primary and secondary windings are arranged in an interleaved manner, as shown in fig. 6.2b). At the given volume of the transformer-core a conventional single interleaving structure showed to be optimal. The more advanced full interleaving, discussed in sec. 2.4.4, would only be beneficial for a smaller transformer volume. Table 6.1 further contains the equivalent circuit elements of the designed transformer, on the one hand measured with an impedance analyzer on the built transformer and on the other hand calculated with the models developed in section 3.
Note, that for S_1 a 3.2mΩ/80V EPC2029 switch is finally applied. The optimally suited 4mΩ/100V EPC2032 switch, used for the design of the converter, is still a preproduction unit and turned out to be out of stock. It would have had 6 months delivery time. Therefore the EPC2029 switch with identical footprint, but lower voltage rating is chosen as viable alternative. Due to its lower blocking voltage it exhibits a lower margin for overvoltage spikes at turn-off, which might limit maximal operating power.
The converter operates in boundary conduction mode (BCM) at high

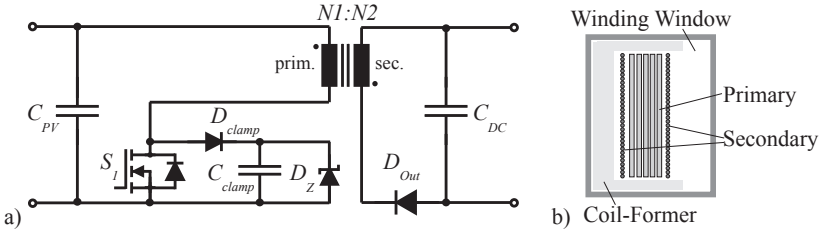


Figure 6.2: a) DC-DC flyback prototype power circuit, b) Flyback transformer winding arrangement

output power and changes to discontinuous conduction mode (DCM) at low output power. The optimized switching frequency ranges from 20kHz to 160kHz, depending on the operating point. Table 6.2 contains the operating-points for 12V input to 400V output at the output powers relevant for the European efficiency. Even though the applied GaN switches would allow for much higher switching frequency, the optimal switching frequency range is given by a trade-off between the efficiency at nominal load and at low load. At low output power the switching losses and the losses of the parasitic transformer capacitance are dominant. Both would increase with higher switching frequency.

6.1.2 Flyback Prototype Control-Implementation and Measurement Circuits

The laboratory tests on the prototype are performed with a fixed input and output voltage externally supplied by laboratory DC-supplies. The flyback converter is operated in current control mode. As the converter is designed to exclusively operate in BCM and DCM, the converter behaves like an on-time controlled current-source, see [25] and sec. 2.5.1. Therefore, the current can be directly set by the on-time of the switch, without the need for a feedback-loop. An FPGA control-board is used to generate the actual gate-signal. The structure of the VHDL-components implemented on the FPGA is shown in fig. 6.3a). The reference on-time is set as parameter. The gate-signal is generated by a timer-block. A new switching-cycle is either started after a fixed time, in case of DCM operation, or the rising flank of the ZVS-detection bit b_{ZVS}, in the case of BCM operation. The state of the converter is

Table 6.1: DC-DC flyback prototype design component list

Input-side	Capacitor C_{PV}	235uF, MLCC X5R, 5x47uF parallel
	Diode D_{clamp}	100V,1A, Schottky, CDBM1100-G
	Capacitor C_{clamp}	3uF, MLCC X7S, 3x1uF parallel
	Zener-Diode D_Z	60V,5W,SMBJ5371B-TP
	Designed: Switch S_1	4mΩ,30A,**100V**, GaNFET, EPC2032
	Applied: Switch S_1	3.2mΩ,31A,**80V**, GaNFET, EPC2029
Output-Side	Capacitor C_{DC}	1.88uF, MLCC X7T, 4x0.47uF parallel
	Diode D_{Out}	1.2kV,2A, SiC Schottky, Cree C4D02120E
Transformer	Turns-Number	N_1=5,N_2=80
	Transformer Core	EPCOS PM5039, Si Ferrite N87
	Primary Winding	Foil, 22mmx0.18mm
	Secondary Winding	Litz-wire, 7x0.1mm, Furakawa TEX ELZ
	Mag. Inductance	Model: $L_{m,prim}$= 10uH Meas: $L_{m,prim}$= 11.2uH
	Leakage Inductance	Model: $L_{\sigma,prim}$= 56.7nH, at 100kHz Meas: $L_{\sigma,prim}$= 63nH, at 100kHz
	Parasitic Capacitance	Model: $C_{eq,prim}$= 24.4nF Meas: $C_{eq,prim}$= 20nF

Table 6.2: DC-DC flyback prototype design operating points for V_{PV}=12V to V_{DC}=400V operation

Output Power	100W	50W	30W	20W	10W	5W
Operating Mode	BCM	BCM	BCM	BCM	DCM	DCM
Switching Frequency	30kHz	51kHz	75kHz	97kHz	20kHz	20kHz

surveyed by a state-machine block, which disables converter operation at a parameterized DC-link over voltage level.

Figure 6.3b) shows the schematic of the flyback converter including the measurement- and control-circuits. The ZVS-detection bit is generated by monitoring the blocking-voltage of the output-diode V_{Dout}. An RC-divider with a ratio of 800:3 scales down V_{Dout} to the analog-signal level. When V_{Dout} raises at the end of a switching-cycle, a comparator sets b_{ZVS} as soon as V_{Dout} exceeds an adjustable threshold V_{th}. The fast rising time of V_{Dout} requires a high bandwidth of the RC-divicer of 10MHz. On the same time the capacitance of the RC-divider must be kept low, 1pF for the given design. Because this capacitance adds

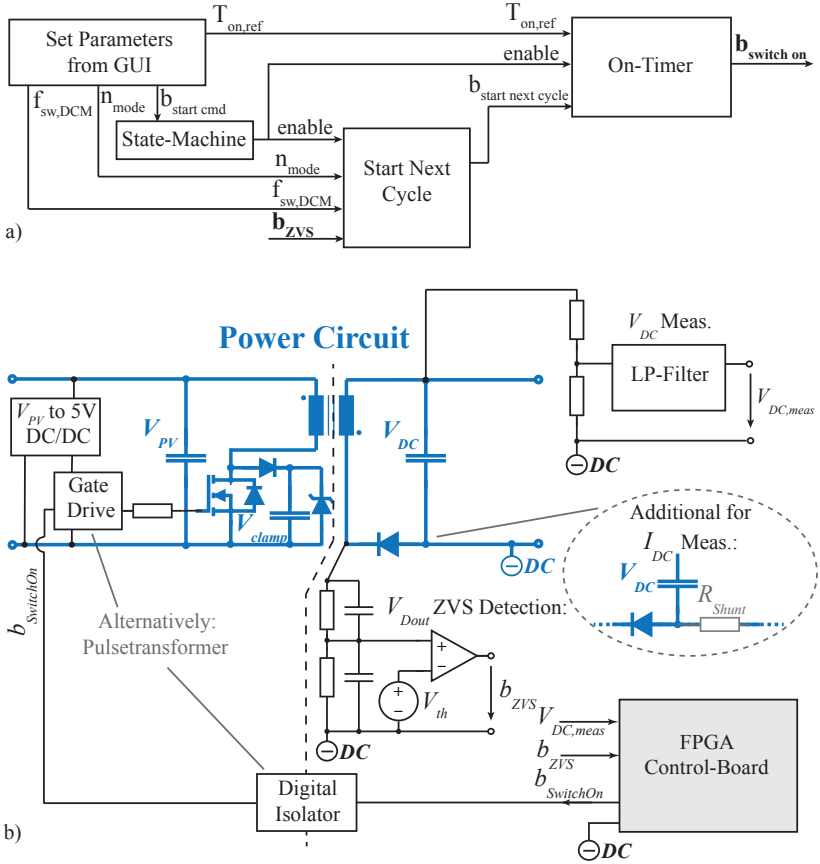


Figure 6.3: DC-DC flyback prototype: a) Overview of FPGA-based control b) Schematics of measurement- and control-circuits

up to the total capacitance on the primary-side of the transformer with the square of the transformer turns-ratio. And a large primary-side capacitance highly influences operating waveforms at low output power, degrading efficiency. The DC-link voltage measurement, needed for overvoltage protection, is realized with an RC-divider and a Sallen-Key low pass filter.
Both voltage measurements, DC-link and output-diode, as well as the

FPGA control-board are referenced to the negative rail of the DC-link. In this way the complete two stage multi-input converter, see sec. 2.5.1, could be controlled by one centralized controller. For MPPT of the three paralleled inputs, the measurement of the DC-link current I_{DC} would be needed, see sec. 2.5.1. This could be realized by an additional current-shunt sensor, as schematically shown in fig. 6.3b).
The gate-drive circuit is supplied from the PV-input side with an integrated buck-converter. The only signal, which needs to be transferred across the isolation barrier from the output- to the input-side, is the gate signal.

6.1.3 Flyback Converter Layout and Mechanical Setup

Figure 6.4a) shows a picture of the DC-DC flyback prototype, with the FPGA control board connected to the actual power-PCB containing the flyback converter. This general FPGA prototyping board, also used for other prototyping projects, is of course oversized for a low power PV application. It would actually be replaced by suitable low-power controller directly put on the power PCB. The power PCB is a four-layer PCB with 70μm copper thickness and is populated only on the top-side. A detailed view of the power PCB is shown in fig. 6.4b). The PV-input side carries relatively high currents up to 12.5A rms and 30A peak. Therefore the layout must be optimized to reduce conduction losses and loop inductance. Several measures are taken, to achieve this goal. A copper layer thickness of 70μm is used, in combination with a compact layout, reducing the length of the current paths. The transformer foil winding is directly soldered to dedicated pads on the PCB, without any connector in between. The return path of the current is on the layer adjacent to the top-layer, minimizing the PCB loop inductance. The input capacitor is realized by five paralleled ceramic capacitors, resulting in very low values of ESL=0.13nH and ESR=0.4mΩ.
The clamp circuit shall protect the switch S_1 from overvoltage spikes with frequencies well above 10MHz. The effectiveness of the clamp circuit is degraded even by very small loop inductances. The loop inductance is minimized by using components with small case-sizes and placing the clamp circuit next to the switch.
At the output-side of the converter, the issue is the high blocking voltage of the components and the relatively high dV/dt. Primarily the layout must fulfill the clearance constraints to withstand a maximum of 800V

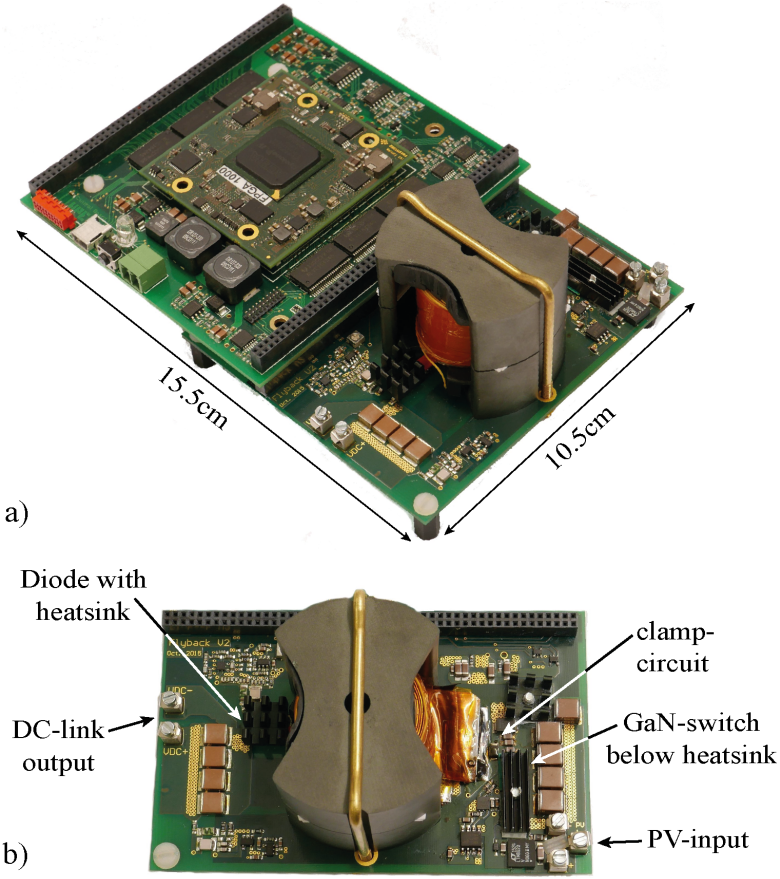


Figure 6.4: DC-DC prototype pictures a) with FPGA control-board b) detailed view of power-circuit

at the transformer secondary winding. Secondarily the cathode-side of D_{out} shall not form parasitic capacitances to other PCB-layers. Because the cathode changes its potential from 0V to a blocking voltage of up to 800V at every switching cycle, causing dielectric losses. To minimize parasitic PCB capacitances the overlapping of planes on different layers is avoided.
Whereas the transformer is designed to be cooled by free convection, the

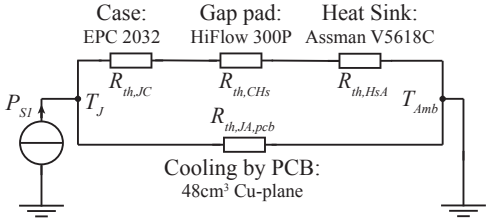


Figure 6.5: DC-DC prototype switch S_1 thermal equivalent circuit

semiconductors need additional heat-sinks to be mounted. The switch S_1 is on the one hand cooled from the top, by a heat-sink and natural convection. On the other hand heat is also transferred through the pads and the copper-planes on the PCB [119]. The thermal equivalent circuit for switch S_1 is shown in fig. 6.5. A total thermal resistance to ambient of $R_{th,JA,tot} = 30$ °C/W is achieved, which leads to maximal junction temperature of T_j=110 °C at full load and 80 °C ambient temperature. The output diode D_{out} can be operated without additional cooling, reaching a temperature of T_j=120 °C at full load and 80 °C ambient temperature. Further the zener-diode D_Z of the clamping circuit, see fig. 6.2a), is subject to substantial losses. Due to its package size it can only be cooled through its pads and copper planes on the PCB. To reduce the thermal resistance from the copper planes to ambient, a 10x10mm heatsink, Assmann V2017B, is mounted on the cooper plane close to D_Z.

6.1.4 Flyback Converter Experimental Results

Figure 6.6 shows operating waveforms of the DC-DC flyback converter at an input voltage of V_{PV}=15V and an output voltage of V_{DC}=400V. The voltage V_{ds} over the primary switch S_1 and the current through the primary transformer winding I_{prim} are shown for three different operating points. The voltage waveform is measured with a standard 400V oscilloscope probe and the current waveform is measured with a CWT 3R mini rogowski coil from PEM.
In fig.6.6a) the converter operates in BCM at nominal load. When the switch turns off, an overvoltage spike is caused on V_{ds} by the transformer leakage inductance L_σ. The spike reaches a maximum of 65V

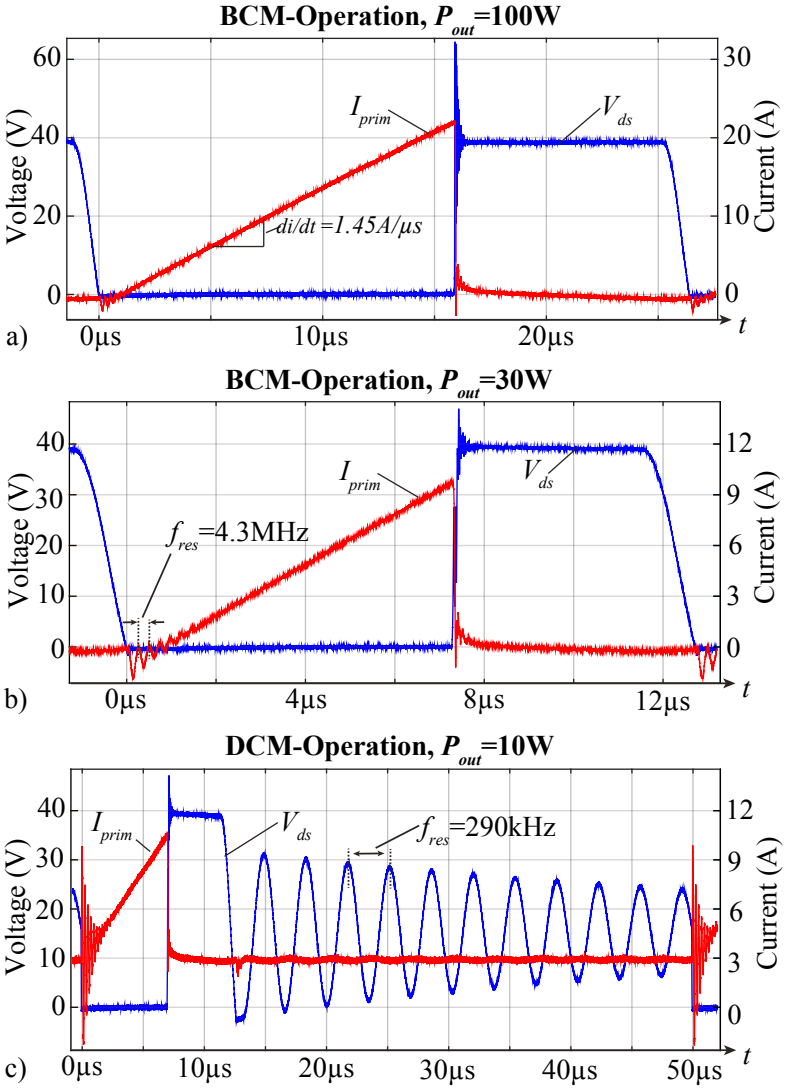


Figure 6.6: DC-DC prototype Operating Waveforms at V_{PV}=15V and V_{DC}=400V: a) BCM at P_{out}=100W, b) BCM at P_{out}=30W, c) DCM at P_{out}=10W

and the subsequent oscillation with a frequency of $f_{res,HF}$ ≃35MHz is damped within several hundreds of nanoseconds. Even though the voltage of the clamp-circuit is set by the Zener diode to 60V, see fig. 6.2, the voltage spike across S_1 can not be fully clamped to this voltage level. The rise-time of the voltage spike, being ca. 10ns, is obviously faster than the current rise-time of the clamping circuit, determined by the reaction time of the clamping diode and the clamping-circuit loop inductance. Despite its limited performance, the clamping circuit still effectively limits the overvoltage spike. For experiments under the same operating conditions but without the clamping circuit (D_{clamp} removed), the voltage spike reached 65V allready at a turn-off current of 14A, hence an output power of ca. 60W. In order not to destroy the switch (3.2mΩ/80V EPC2029), a maximal tolerable voltage spike of 65V is defined for the experiments. The prototype can therefore not be operated at nominal load for input voltages below 15V. The 4mΩ/100V switch EPC2032 would need to be applied for full output power over the whole input voltage range.
Figure 6.6b) shows the operating waveforms at 30W output power, where the converter still operates in BCM. The overvoltage spike is much less pronounced, due to the lower turn-off current. At low output power the converter changes to DCM. Figure 6.6c) shows the waveforms at 10W output power. The resonance of V_{ds} decays relatively slow during the discontinuous interval. This would allow to apply valley switching even in DCM, also called valley-hopping. Though this feature is not implemented in the applied control software.
By the analysis presented in sec. 5.1 the circuit parasitics can be readout from the operating waveforms and compared to the modelled values. From the $\frac{di}{dt}$ in fig. 6.6a) the magnetizing inductance can be determined to $L_{m,meas}$=10.4μH. This matches well with the designed value of $L_{m,prim}$=11.2μH. The resonance frequency of V_{ds} in fig. 6.6c) and $L_{m,meas}$ can be used to calculate the total primary side capacitance $C_{eq,tot,meas}$=29nF. This capacitance includes the transformer capacitance $C_{eq,prim}$ and the output-capacitances of V_{Dout} and S_1. The model predicts a capacitance of $C_{eq,tot,model}$=32nF, confirming a good matching to the measurements. From the high frequency resonance in fig. 6.6b) and $C_{eq,prim}$, the primary-side leakage inductance follows as $L_{\sigma,meas}$=44.9nH. The modelled leakage inductance is $L_{\sigma,prim}$=40nH at 4MHz, achieving a modelling deviation of 13% even at this high frequency.

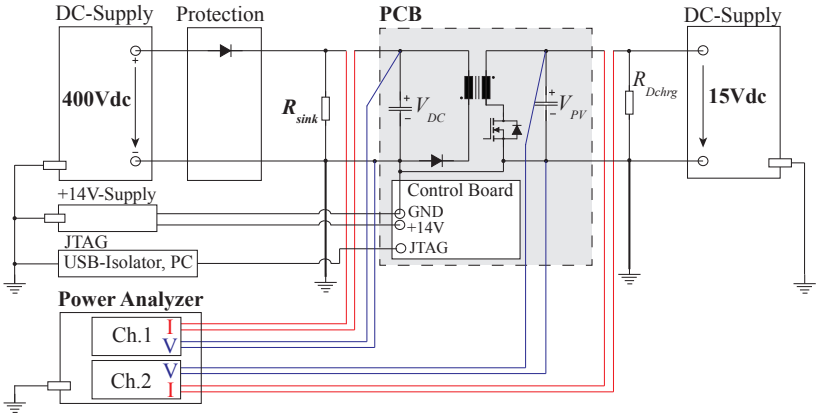


Figure 6.7: DC-DC prototype efficiency measurements laboratory setup

The performance of the DC-DC converter is characterised by means of the high precision power analyzer, ZES LMG 670. Figure 6.7 schematically shows the laboratory setup and the applied devices for measuring the efficiency of the converter. Measurements are performed for an input voltage range of V_{PV}=15V-20V and an output voltage range of V_{DC}=350V-450V. Different output power levels are measured according to the European efficiency: 5%, 10%, 20%, 30%, 50%, 100% P_{nom}. Figure 6.8 shows the efficiency versus output power measured at V_{PV}=15V and V_{DC}=400V. The converter reaches a European efficiency of η_{EU}=96.45% and maximal efficiency of 96.9% at 50W output power. The efficiency includes all converter losses, measurement circuit losses and gate-driver and gate-supply losses. The only loss component not included is the power consumption of the FPGA control-board. The power consumption of a suitable low power controller, would have to be added to the losses, to get the effective efficiency. Figure 6.8 further shows the modelled efficiency, which predicts a European efficiency of η_{EU}=96.59%. The matching between the measured and the modelled efficiencies is best at medium power levels and increases at low and high output power. Table 6.3 quantifies the modelling error Δ_P of the modelled converter losses relative to the measured converter losses. The modelling error is given for a broad set of input and output voltages.

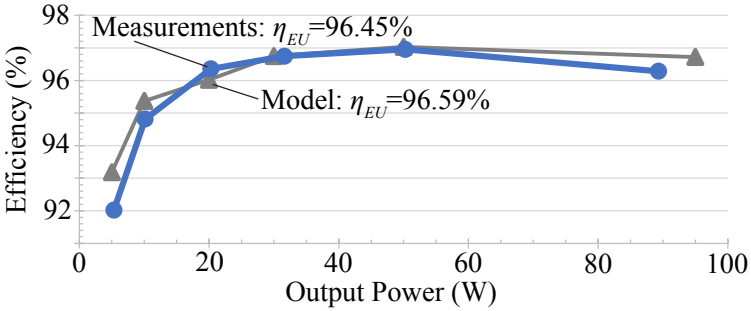


Figure 6.8: DC-DC prototype measured efficiency versus model (V_{PV}=15V and V_{DC}=400V, at 30°C converter temperature)

Table 6.3: DC-DC flyback prototype: Difference of the modelled to the measured converter losses, Δ_P (at 30°C converter temperature)

Operating Point: V_{PV}=15V-20V, V_{DC}=400V							
Input Voltage	P_{Out}:	100W	50W	30W	20W	10W	5W
V_{PV}=15V	Δ_P(%):	11.7%	2.5%	0.1%	-9.2%	10.7%	14.5%
V_{PV}=17V	Δ_P(%):	11.3%	0.7%	-0.7%	1.5%	-8.8%	-9.7%
V_{PV}=20V	Δ_P(%):	11.5%	0.9%	-5.4%	0.4%	-3.9%	1.8%
Measurement Accuracy	Δ_{meas} (%):	0.013	0.011	0.012	0.012	0.011	0.011
Operating Point: P_{Out}=50W, V_{DC}=350-450V							
Input Voltage	V_{DC}:	350V	375V	400V	425V	450V	
V_{PV}=15V	Δ_P (%):	-3.4%	-3.1%	-2.3%	-4.1%	-3.5%	
V_{PV}=17V	Δ_P (%):	-0.3%	-2.1%	-1.3%	-1.5%	-3.7%	
V_{PV}=20V	Δ_P (%):	0.2%	-0.6%	-0.5%	-2.2%	-1.4%	
Measurement Accuracy	Δ_{meas} (%):	0.011	0.011	0.011	0.011	0.011	

The measurement uncertainty of the power analyzer Δ_{meas} is further given at each measuring point. The deviation of the modelled losses is within +/-15%, which confirms a good overall accordance of the applied converter models.

The above discussed measurements are performed with the converter

components being at ambient temperature. The converter is operated for several tens of seconds, just enough to get a valid efficiency measurement. An additional long time test run at 100W output power is performed to reach thermal steady state. The temperature is surveyed and measured with an Optris OPTPI400O38T900 thermo camera. The temperature measurement is subject to a measurement uncertainty of ∼+/-4°C, due to the accuracy of the camera itself and uncertainty of the emissivity of the measured materials. Figure 6.9 shows a thermo camera picture of the converter in thermal steady-state after 75min operation. The switch S_1, the transformer windings and the output diode appear as hot-spots, heating up above 50°C. Table 6.4 compares the measured temperature of the transformer and the heat-sink of switch S_1 to the values predicted by the thermal model. The transformer winding and core temperature are predicted well. Though the heat-sink temperature of switch S_1 is highly underestimated by nearly 20°C. The reason for this deviation is either caused by an increased total thermal resistance $R_{th,J-A}$ or increased losses in the switch. The scenario of increased losses seems more probable. When looking at fig. 6.8 one can see, that the model underestimates some resistive losses at high output loads. If parts of these additional resistive losses are dissipated in the vicinity of S_1, e.g. PCB resistances, it would increase the heat-sink temperature. Further the operation waveforms showed, that the clamping circuit does not absorb the whole overvoltage spike, as assumed in the loss model. Instead a part of this energy is dissipated in a high frequency resonance, causing additional conduction losses in the switch.
Finally the efficiency is measured in thermal steady-state and compared to the modelled losses, assuming 50°C converter-temperature. The measured efficiency is $\eta_{meas,100W}$=96.16% and model efficiency is $\eta_{meas,100W}$=96.76%. The difference of Δ_P = -15.6% is slightly increased compared to the values in table 6.3, but stays still in the same range.

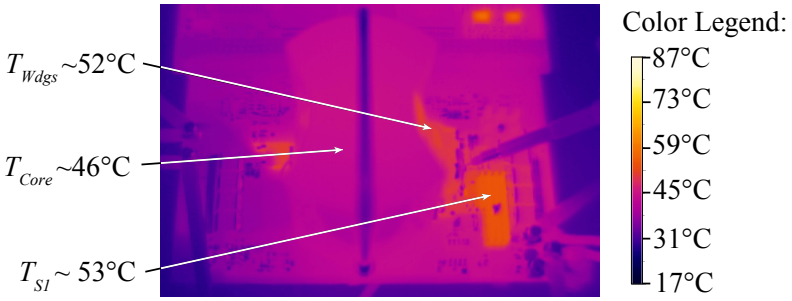


Figure 6.9: DC-DC prototype thermal test run: thermo camera picture in thermal steady-state after 75min operation (P_{out}=90W, V_{PV}=15V, V_{DC}=400V, T_{amb}=30°C)

Table 6.4: DCDC flyback operation at V_{PV}=15V to V_{DC}=400V and 100W output power: modelled temperature versus temperature measured in thermal steady-state with an Optris OPTPI400O38T900 thermo camera (accuracy +/- 4°C)

Device:	Transformer Winding	Transformer Core	Heatsink Switch S_1
Measurement:	T_{Wdgs} ~52°C	T_{Core} ~46°C	T_{S1} ~53°C
Model:	T_{Wdgs} ~49°C	T_{Core} ~45°C	T_{S1} ~34°C

6.2 DC-AC GaN Fullbridge Converter Prototype

6.2.1 Fullbridge Converter Design

The fullbridge converter is designed by model based optimization, see sec.5.2. From the three core-materials considered in the optimzation in sec. 5.3.2, the nanocristalline Vitroperm 500F from Vacuum Schmelze features the best performance regarding volume and losses. Though the smallest standard Vitroperm 500F core size is a factor two to three too big, for the considered inductor L_{inv}. Instead of that the Microlite distributed gap cores from Metglas, rating second-best in sec. 5.3.2, are commercially available in appropriate core-sizes. Therefore the inductor L_{inv} and the filter-inductor of the prototype are designed with these

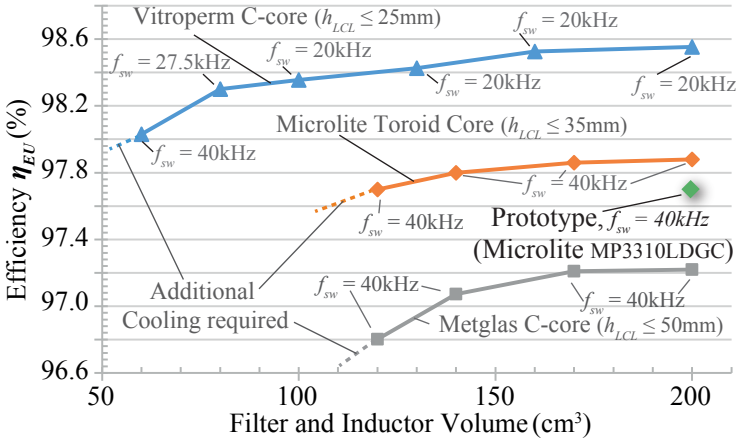


Figure 6.10: Efficiency of the designed prototype and the DC-AC stage η-ρ pareto-front (derived in section 5.3.2).

cores. The fullbridge converter design is deducted from an optimization run with freely varied toroid cores and a maximal total volume of the filter and inductor of $130cm^3$. The actual inductor design is obtained by stacking commercially available standard cores to reach the same core-area as for the optimized inductors. Due to the non-optimal core-geometry of the standard cores, the total volume of the stacked prototpye design adds up to V_{LCL}=$200cm^3$.
Figure 6.10 shows the prototype design in the volume versus efficiency plane in comparison to the DC-AC stage η-ρ pareto front. The efficiency of the prototype design is 0.2% below the pareto optimum, due to the non-optimal stacked standard-cores increasing the mean turns-length and the use of an enameled copper wire instead of litz-wires.

A schematic of the power circuit in fig. 6.12 shows the components used to build converter. Table 6.5 gives detailed information for every component. The fullbridge operates in single-phase chopping mode (see sec. 2.5.1): one halfbridge switches with line frequency, denoted with LF in fig.6.12, and the other halfbridge switches with high frequency for current control, denoted as HF. Both halfbridges are built based on the reference design developed in sec. 4. Though the HF halfbridge applies switches with a low current rating to reduce switching losses, whereas for the LF halfbridge switches with higher current rating are

Table 6.5: DC-AC fullbrdige converter prototype design component list

DC-side	Capacitor C_{PV}	4.7uF, MLCC X7T, 10x0.47uF parallel
	HF Switches $S_{1,1}$,$S_{1,2}$	220mΩ,7A,650V, GaN transistor, GS66502B
	LF Switches $S_{2,1}$,$S_{2,2}$	41mΩ,34A,650V, GaN transistor, GS66508P
AC-Side	Modulation Scheme	Single-Phase Chopping f_{sw} = 40kHz
	Inductor L_{inv}	5.3mH, 5x stacked core MP3310LDGC N=68, roundwire d_{cu}=1mm Model:C_{par}=65pF, Meas.: C_{par}=62pF
	Filter Inductor L_f	350μH, core MP2310PDGC N=40, roundwire d_{cu}=1mm
	Filter Capacitor C_F	1.2μF, 275VAC, Würth 890324027012CS
	Damping Capacitor C_d	0.8μF, 275VAC, Würth 890324026024
	Damping Resistor R_d	21Ω, 3x paralleled 66Ω,0.25W chip resistor
Alternative Inductor		
AC-Side	Inductor L_{inv}	5.3mH, VAC T60102-L2083-W156 Vitroperm 500F, N=64, roundwire d_{cu}=1mm Model: C_{par}=26pF, Meas.: C_{par}=24pF

used, to reduce conduction losses. The separation of the fullbridge into a LF and a HF halfbridge, would allow the use of lower cost MOSFET's for the LF halfbridge, without any trade-off in efficiency.
In addition to the inductor L_{inv} with Microlite distributed gap cores, a second, alternative inductor with the same inductance value is built applying the nanocristalline Vitroperm 500F core material. The smallest available standard core is the T60102-L2083-W156, resulting in a way oversized boxed inductor volume of ∼300cm^3. Therefore only one fourth of the winding window is used for the winding, see fig. 6.13c). In this manner a smaller custom made core with a reasonable boxed volume of ∼120cm^3 can be emulated. The detailed specification of the alternative inductor is also given in table 6.5.

6.2.2 Fullbridge Converter Prototype Control Implementation and Measurement Circuits

The laboratory prototype is operated with a DC-source connected on the DC-link and a single-phase AC-source connected on the AC-side. In this configuration the converter does not perform any power-decoupling

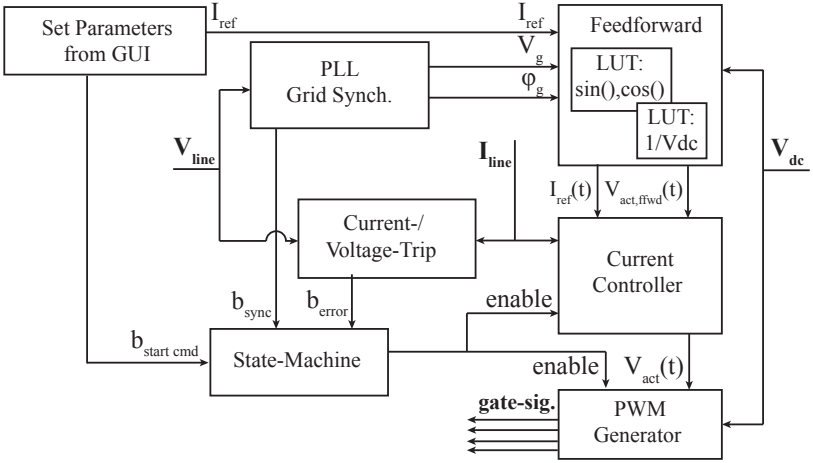


Figure 6.11: DC-AC converter prototype: overview of FPGA-based control

as described in sec. 2.5.1, but operates with a constant DC-link voltage, set by the DC-source. With the input and output voltages given by the sources, the converter operates in current-control mode. The structure of the appropriate control implemented on the FPGA-board is schematically shown in figure 6.11. The reference line current is set as a parameter. A phase locked loop (PLL) detects the grid amplitude and phase from the measured line voltage. The feedforward block calculates the sinusoidal reference current and actuator-voltage feedforward, using look-up tables for the real-time calculation of sinus, cosinus and the inverted DC-link voltage. The current control block calculates the control error between the measured and the reference current and adjusts the actuator voltage $V_{act}(t)$ accordingly. The PWM block finally sets the gate-signals of the fullbridge, to generate the desired actuator voltage on the fullbridge output. A state machine monitors the converter state and disables operation in case of over-current or over-voltage errors.

The converter control requires three quantities to be measured: the DC-link voltage V_{DC}, the line voltage V_{line} and the line current I_{line}. Figure 6.12 schematically illustrates the measurement circuits. The DC-link voltage measurement is realized with an RC-divider and a Sallen-Key low pass filter. The line-voltage measurement consists of

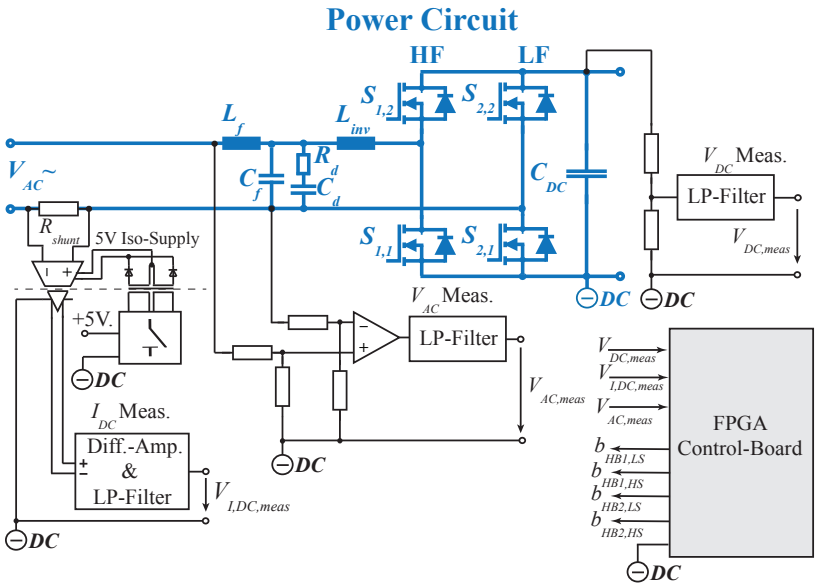


Figure 6.12: DC-AC converter prototype: Schematics of measurement- and control-circuits

two RC-dividers, a differential operation amplifier and a Sallen-Key low pass filter. The current is measured with an isolated current shunt monitor, designed according to [120]. A low power push-pull DC-DC converter delivers the isolated 5V supply voltage to the input-side of the shunt monitor. The shunt monitor outputs a differential signal, which is consecutively processed with a differential amplifier and a low pass filter.

The measurement circuits and the FPGA control-board are referenced to the negative DC-link rail. Hence, the complete two stage system including the DC-DC stage, see sec. 2.5.1 and sec. 6.1.2, could be operated with one single controller.

6.2.3 Fullbridge Converter Layout and Mechanical Setup

Figure 6.13a) shows the fullbridge converter prototype. The FPGA control-board is connected to the power-PCB, which contains the power-

circuit. For an actual design the FPGA control-board would be replaced by a low power micro-controller, see sec. 6.1.3. The power-PCB consists of 4 layers with 70μm copper thickness. The auxiliary circuits, such as measurements and gate-supplies, are located on the top-side of the PCB. The bottom-side contains the power-circuits, as shown in fig. 6.13b). It consists of two GaN-halfbridges, designed and layouted according to the reference-design developed in sec. 4.
The inductor L_{inv} and the filter inductor are designed for free convection cooling and do not need additional cooling. The power semiconductors need to be cooled by heatsinks, in order not to overheat at nominal output power. The applied GaN switches are back-side cooled devices [118]. The drain-pad of the package serves as thermal pad. Thermal vias transfer the heat from the thermal pad to the other-side of the PCB. With the given layout, the resulting thermal resistance from the junction to the other side of the PCB is $R_{th,J,PCBpad}$=20°C/W [118]. The heat is transferred from the PCB-pads to the air by heat-sinks, Aavid Thermalloy 508500B00000G. They are mounted on the PCB-pads with an electrically isolating gap pad, HiFlow 300P, in between. This setup features a thermal resistance from PCB-pad to ambient of $R_{th,PCBpad,A}$=50°C/W. Hence a total thermal resistance from junction to ambient of $R_{th,J,A,tot}$=70°C/W is achieved. The HF halfbridge, is subject to higher semiconductor losses, than the LF halfbridge. Therefor two heat-sinks are mounted on the HF halfbridge, whereas one heat-sink is sufficient for the LF halfbridge. At nominal output power and 80°C ambient temperature the junction temperature reaches a maximum of $T_{j,HF}$=120°C, for the HF halfbridge, and $T_{j,LF}$=90°C, for the LF halfbridge.

6.2.4 Fullbridge Converter Experimental Results

Figure 6.14, illustrates the laboratory setup used for the tests of the DC-AC prototype. The AC-side grid, which must act as a sink, is realized with an AC-source, a resistor and an isolation transformer. The resistor R_{sink} sinks the load current, which is either supplied by the fullbridge converter during operation, or by the AC-supply in idle mode. The isolation transformer is inserted for safety reasons, such that the AC-supply and the sink resistor can be grounded. The power analyzer features a sufficient voltage isolation rating between each channel and measures the current and voltage at the input and output of the full-

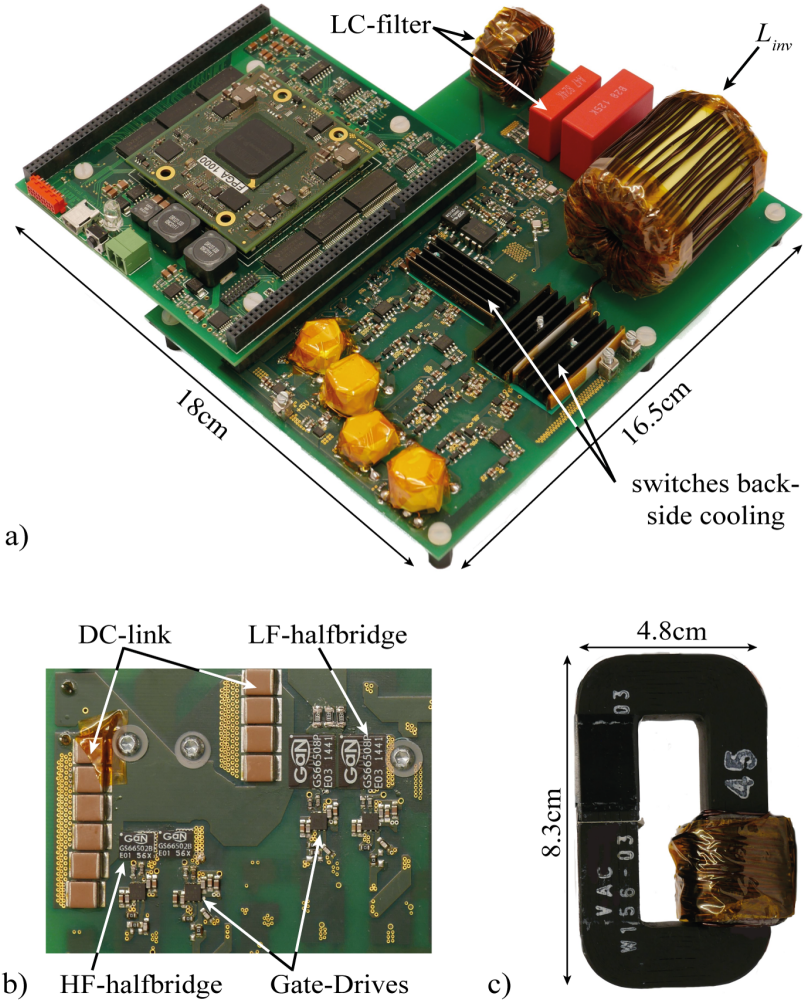


Figure 6.13: DC-AC prototype pictures: a) with FPGA control-board b) back-side detailed view of power-circuit c) alternative inductor L_{inv} with Vitroperm 500F core (see specification in table 6.5)

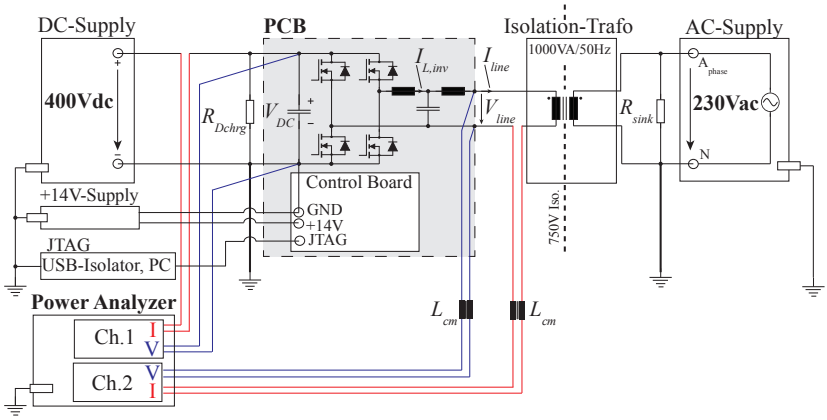


Figure 6.14: DC-AC prototype efficiency measurements laboratory setup

bridge converter.

Figure 6.15 shows operating waveforms of the DC-AC fullbridge converter operating at 400V DC-link voltage and 230V/50Hz line voltage. The line voltage is measured with a LeCroy ADP305 differential voltage probe. The currents $I_{L,inv}$ and I_{line} are measured with a LeCroy AP015 and a CP030 current probe. In fig. 6.15a) the measured line current is shown over a full lines period at the output power levels relevant for European efficiency. The respective measured line voltage is given in fig. 6.15b), showing that the converter is operated at unity power factor. The reactive power of the filter capacitors C_f and C_d is successfully compensated by the converter control. Figure 6.15c) shows $I_{L,inv}$ and I_{line} at P_{out}=300W. The inductor current exhibits high current spikes due to the parasitic capacitance of the inductor. The fast voltage rise- and fall-time of the GaN-switches of ∼10ns (see sec. 4) make the inductor voltage change by $dV/dt = 400V/10ns$, leading to capacitive charging current spikes of ∼2.5A during the switching transition. Depending on the semiconductor rise-/fall-times and the DC-link voltage, the capacitive charging current spikes are essentially constant over a lines period. The variation of the spikes in $I_{L,inv}$ in fig. 6.15c) are an artefact caused by undersampling of $I_{L,inv}$. A correct sampling of the charging frequent spike requires sampling with 5Gs/s, which does

not allow to record an entire lines period of 20ms, due to limited memory of the oscilloscope.
The designed differential mode filter effectively filters the inductor current $I_{L,inv}$. The remaining total harmonic distortion of the line current is $THD_{I_{line}}$=3.1%.
Despite the low THD, the line current waveforms exhibit two defects, firstly a high frequency distortion at the zero-crossing of the line voltage, secondly some low order harmonic distortion.
The distortion at the zero-crossing of V_{line} has two causes. The fullbridge is interlocked at the zero-crossing for 1μs, which excites an oscillation of the LC filter stage. This oscillation can be minimized by reducing the interlocking time, which is currently limited by the implementation of the PWM generator, see fig. 6.11. A further cause of the current distortion at zero-crossing is the LF halfbridge, which switches at the zero-crossing and causes a high frequency current charging/discharging the parasitic capacitance of the isolation transformer.
The low order harmonic distortion is in the frequency range of 350Hz, which actually should be compensated by the current controller. Though the bandwidth of the current controller showed to become unstable for bandwidths higher than 1.2kHz. The isolation transformer is found to exhibit a leakage inductance of 1.2mH. Seen from the output-side of the DC-AC fullbridge the leakage inductance acts as an equivalent line-inductance of 1.2mH. This value is way above the line inductance of a typical grid-connection of up to 50μH [121] and limits the achievable bandwidth of the current controller. For an actual grid-operation the current controller bandwidth could be set higher and the low frequency distortion could be compensated.

The performance of the DC-AC converter is measured with the high precision power analyzer, ZES LMG 670, as shown in fig. 6.14. The measurements are performed at V_{DC}=400V and V_{ac}=230V/50Hz for the output power levels required for the European efficiency: 5%, 10%, 20%, 30%, 50% and 100% of P_{nom}. The performance of the prototype is investigated for two distinct configurations, once with the Microlite toroid inductor and once with the alternative Vitroperm 500F inductor, see sec. 6.2.1 and table 6.5. Figure 6.16 shows the efficiency versus the output power for the two configurations. With the Microlite toroid inductor a weighted efficiency of η_{EU}=97.72% and a maximal efficiency

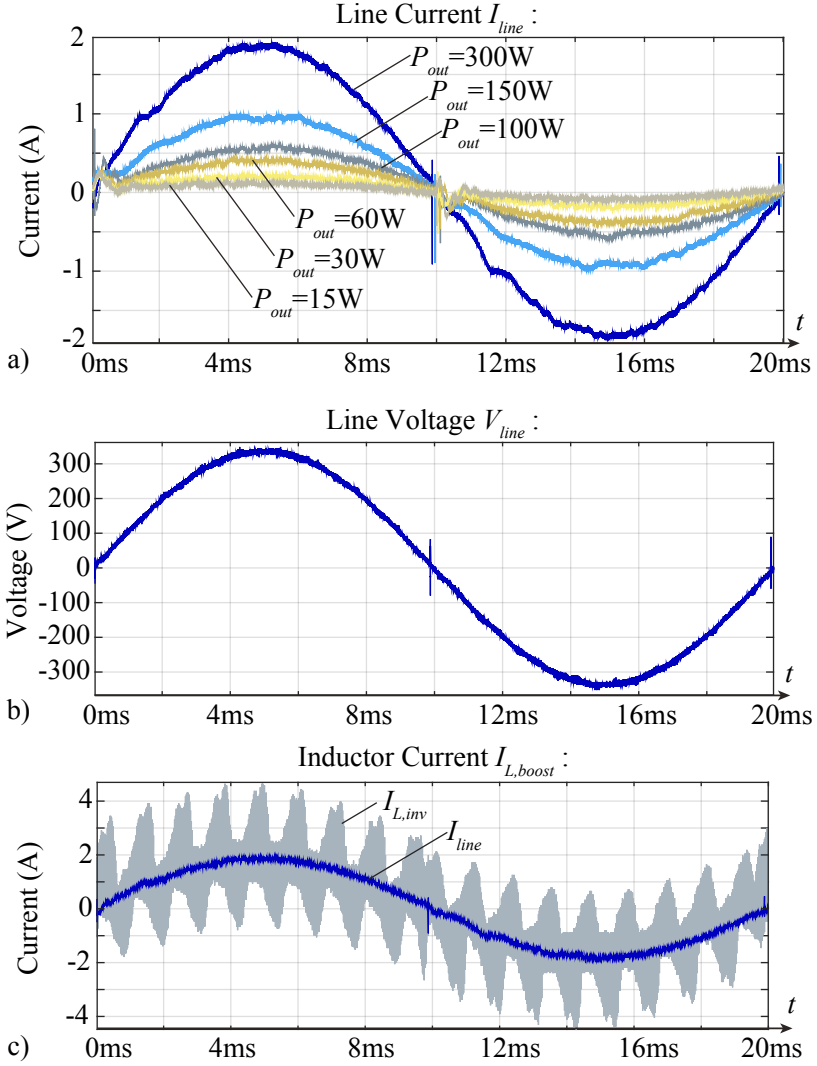


Figure 6.15: DC-AC prototype operating waveforms (V_{dc} =400 to V_{ac}=230V/50Hz): a) line current at different output power, b) line voltage, c) inductor current $i_{L,inv}$ and line-current at 300W output power

Table 6.6: DC-AC fullbridge prototype: Difference of the modelled to the measured converter losses, Δ_P (V_{DC}=400V, V_{AC}=230V, converter temperature T_{op}=30°C)

Regular Inductor with Microlite distributed gap toroids:							
Output Power	P_{Out}:	100W	50W	30W	20W	10W	5W
Difference	Δ_P(%):	-1.8%	5.6%	8.2%	-8.5%	-7.1%	-3.1%
Measurement Accuracy	Δ_{meas} (%):	0.019	0.014	0.016	0.016	0.013	0.019
Alternative Inductor with a Vitroperm 500F C-core:							
Output Power	P_{Out}:	100W	50W	30W	20W	10W	5W
Difference	Δ_P (%):	-0.7%	0.8%	14.7%	2.1%	3.9%	4.2%
Measurement Accuracy	Δ_{meas} (%):	0.019	0.014	0.016	0.016	0.013	0.019

of 98.7% is achieved. The configuration with the Vitroperm 500F inductor reaches a comparable weighted efficiency of η_{EU}=97.76% and a slightly higher maximal efficiency of 98.9%. Figure 6.16 further shows the modelled efficiency in comparison to the measured efficiency. The model shows generally a good accordance to the measurements with a slightly higher deviation at medium output power. The difference of the modelled losses to the measured losses Δ_P is given in table 6.6 together with the measurement accuracy at the respective measuring point. The deviation of the modelled losses is within +/-15%, confirming a good modeling accuracy over the whole load range.
The efficiency measurement includes all converter losses, the losses of the measurement circuits, the gate-drive losses and the gate-supply and auxiliary-supply losses. The only not considered loss component is the power consumption of the FPGA control-board. The power consumption of an appropriate low-power controller would have to be added, to get the practical converter efficiency.

The above presented efficiency measurements are performed with the converter components at ambient temperature. The converter is operated for several tens of seconds, just enough to perform the efficiency measurement. An additional long-time test run is performed at 300W output-power to achieve thermal steady state. The temperature is measured with an Optris OPTPI400O38T900 thermo camera.

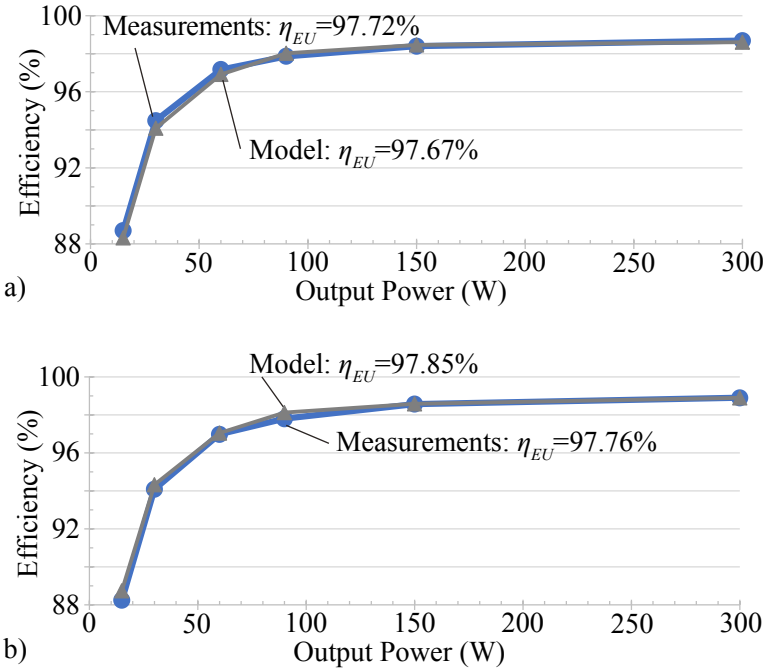


Figure 6.16: DC-AC prototype measured efficiency versus model (400Vdc to 230Vac operation): a) with the regular inductor L_{inv} built with Microlite distributed gap toroids, b) with the alternative inductor L_{inv} built with a Vitroperm 500F C-core

The uncertainty of the temperature measurement is ∼+/-4°C, due to the accuracy of the camera itself and uncertainty of the emissivity of the measured materials. Figure 6.17 shows a thermo-camera picture taken in thermal steady state after 60min of operation at full load. The hottest spots are the two heat-sinks of the HF-halfbridge and the windings of the inductor L_{inv} with a moderate temperature increase of 20°C compared to T_{amb}. Table 6.7 compares the measured temperatures of the heat-sinks and the inductor to the temperatures predicted by the thermal model. For the Vitroperm 500F inductor the winding temperature T_{wdgs} is predicted well. In case of the Microlite toroid inductor, the thermal model overestimates the temperature by 6°C.

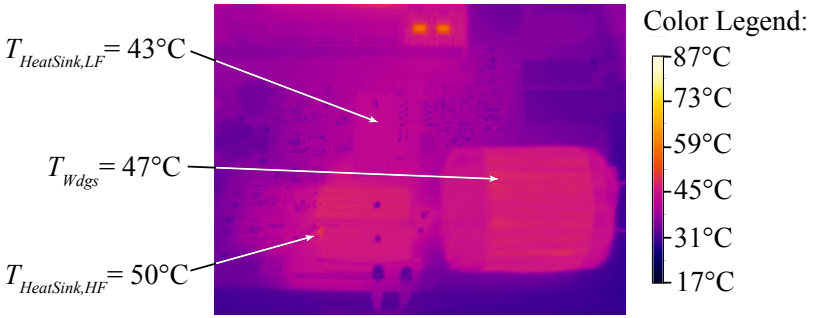


Figure 6.17: DC-AC prototype thermal test run (with the Microlite toroid inductor): thermo camera picture in thermal steady-state after 60min operation (P_{out}=300W, V_{DC}=400V, V_{AC}=230V, T_{amb}=30°C)

The modelled temperature of the LF heat-sink matches well with the measurements, whereas the HF heat-sink temperature is predicted 6°C too high. Considering the accuracy of the thermo camera, the thermal model matches well the measurements. The reason for the somewhat overestimated temperatures could be additional cooling through the PCB planes, which is not considered in the thermal model.
The efficiency is further measured in thermal steady state and compared to the modelled value, see table 6.7. The difference of the modelled to the measured losses is Δ_P=6.5% and Δ_P=7.8%, being in the same range as for the measurements at ambient temperature.

6.3 Complete Two-Stage System Performance

In the following the performance of the complete two-stage system is analyzed based on the results from the DC-DC and the DC-AC prototype. The efficiency of the two stage system is derived from the measured efficiencies in fig. 6.16 and 6.8 in the way described in section 5.3.3. Also the same additional power-consumption $P_{syst,aux}$ is taken into account for the micro-controller and the line-relay of the two stage system. The derived prototype two-stage system efficiency and volume is plotted in figure 6.18 in comparison to the multi-input AC-module η-ρ pareto front. Note that with 15V PV-side input voltage and a constant DC-link voltage the efficiency is measured at a slightly

Table 6.7: DC-AC fullbridge thermal steady state operation at V_{DC}=400V to V_{ac}=230V/50Hz, P_{out}=300W and T_{amb}=30°C: modelled temperature versus temperature measured with an Optris OPTPI400O38T900 thermo camera (accuracy +/-4°C)

Regular Inductor with Microlite distributed gap toroids:				
	LF Halfbridge	HF Halfbridge	Inductor	Efficiency
Measurement:	$T_{HS,LF}$ ~43°C	$T_{HS,HF}$ ~50°C	T_{wdgs} ~48°C	η=98.66%
Model:	$T_{HS,LF}$ ~42°C	$T_{HS,HF}$ ~56°C	T_{wdgs} ~54°C	η=98.56%
Alternative Inductor with a Vitroperm 500F C-core:				
	LF Halfbridge	HF Halfbridge	Inductor	Efficiency
Measurement:	-	-	T_{wdgs} ~47°C	η=98.91%
Model:	-	-	T_{wdgs} ~45°C	η=98.84%

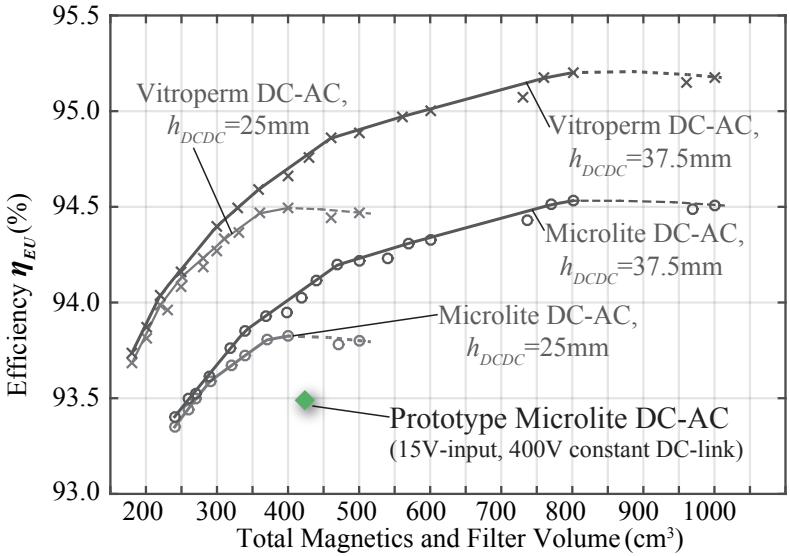


Figure 6.18: Merged two-stage prototype efficiency in comparison to the multi-input AC-module η-ρ pareto front.

different operating point than assumed for the calculation of the η-ρ pareto front. Though the models showed that the influence on the efficiency is negligibly small. The prototype efficiency is 0.6% below the

pareto optimum. This difference is directly caused by the DC-DC and DC-AC stage being 0.4% and 0.2% below their corresponding optimum.

Figure 6.19 a) shows the relative loss distribution of the DC-DC stage for the output power levels used for European efficiency calculation. The losses caused by the transformer are split into two shares, the core and winding losses and the losses $P_{parasitics}$ indirectly caused by the parasitic elements of the transformer. Considering both shares, the transformer is the major loss contributor at any load power. System efficiency appears to be limited by the transformer core. The use of a custom-made core-shape would allow to achieve the pareto-limit in figure 5.10. A further efficiency improvement would require a core-material with improved characteristics. A material with a higher saturation flux density, but the same low high frequency losses as ferrite, would enable a transformer design with a reduced turns-number being beneficial for both winding-losses and parasitics.

The loss-distribution of the DC-AC stage is shown in 6.19 b). The share of the magnetic losses is less pronounced than for the DC-DC stage design. Nevertheless at 100% output power the inductors winding and low frequency core losses dominate the losses. With decreasing output power the loss-components related to the switching-frequency become dominant. Firstly there are the switching losses in the semiconductors. Secondly the switching frequency current ripple causes a substantial amount of core-losses in the inductor L_{inv}. The total losses reach a plateau at 30% output power and do not decrease further at lower output power. This can be seen from the loss-distribution, which stays basically the same for 30% down to 5% output power. Further the magnetic and semiconductor losses are well balanced at low output power. This is due to the trade-off between switching and core-losses. A higher switching frequency decreases the core-losses due to a reduced magnetic-field amplitude, but increases switching losses. The model-based optimization finds the switching frequency featuring the optimal ratio between these two loss-components, which is 40kHz for the given design. This switching frequency might seem rather low for GaN-switches, but it directly follows from the efficiency optimization for wide output power-levels.
Another pair of loss-components, which is though not well balanced are the semiconductor switching and conduction losses. The switching

losses are dominant at all output power levels. Even at 100% output power the conduction losses stay very low, being not much higher than the auxiliary losses. This confirms the fact, that the applied 650V/7A rated semiconductors are overrated for the 300W fullbridge application with a nominal current of 1.4Arms.
Even though the 650V GaN switches proved an excellent switching behaviour with extremely low switching losses, the application of switches with lower current-rating, hence lower semiconductor die size, would beside reduced costs bring potentially increased efficiency. A reduced semiconductor die exhibits a lower gate-source and drain-source capacitance, which reduces gate-drive and switching losses. If optimally packaged (see section 4.1), a smaller die allows for reduced package parasitics, improving the switching speed and hence reducing switching losses. Alternatively, a core-material with lower high frequency losses would allow to reduce the loss-plateau at low output power and effectively improve the system efficiency. The nanocrystalline Vitroperm 500F material is one viable option. A further improvement could be achieved by the use of custom-made core-shapes. The limited availability of standard-core sizes reduces the efficiency 0.2% and 1% below the pareto optimum for Microlite toroids and Vitroperm C-cores.

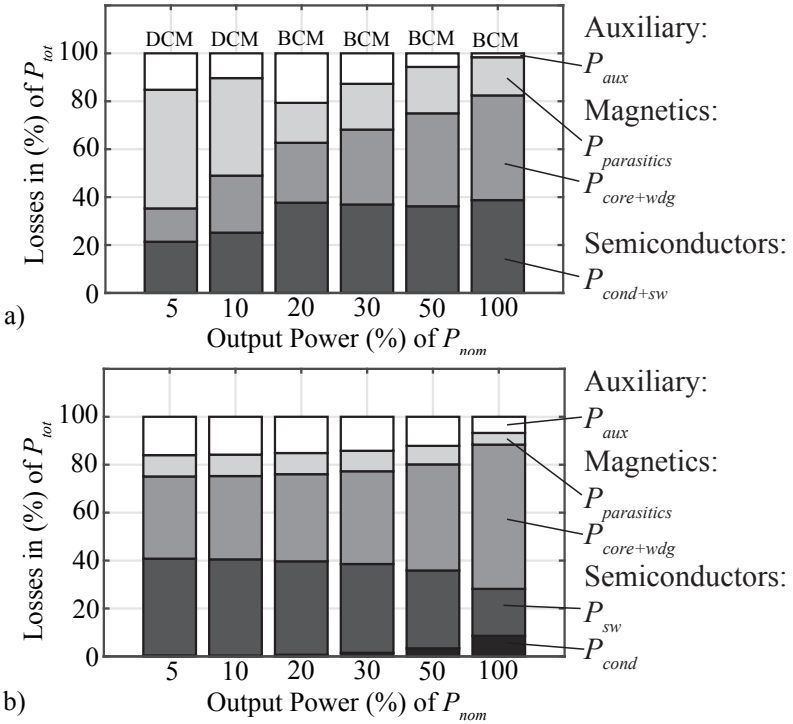


Figure 6.19: Loss components in percentage of total losses at different output-power (predicted by model): a) DC-DC stage prototype, b) DC-AC stage prototype with Microlite inductor

7 Summary & Conclusion

7.1 Summary

For small scale roof-top PV-systems the trend is towards module-integrated electronics featuring separate MPP-tracking for each PV-module and increasing energy-yield under partial shading conditions. Among the module-integrated electronics, the AC-module features the advantage of modularity, low installation cost and simple straight forward design of the PV-system. Whereas common AC-modules track the MPP on PV-module level, this work investigates AC-modules with MPP-tracking on substring-level. Mismatch losses among the three substrings of the PV-module are eliminated and a higher energy-yield results under partial shading of the PV-module.

Based on a review of AC-module topologies with single MPP-tracking, topologies for a multi-input AC-module with substring MPP-tracking are derived. To achieve targeted cost and reliability, AC-modules must be designed with a low part-count number. This severely restricts the feasible topology candidates, because a multi-input AC-module inherently exhibits more components than its single-input counterpart. The derived multi-input topologies are compared to the single-input topologies, based on six-benchmarking factors, taking into account the size of the passive components and the semiconductor losses and rating. The following results can be concluded. The most important conceptual decision is whether or not an electrolyte capacitor may be used for power decoupling. If so, the most promising multi-input topology is a power-balancer multiport stage in series with a LC resonant cyclo-converter.

If not, a two-stage topology consisting of a DC-AC PWM fullbridge and three paralleled DC-DC flyback stages features the best performance. Among these two topology options for a multi-input AC-module, the two-stage topology is investigated in this work. It features the advantage of a smaller power decoupling capacitor and allows to investigate the application of GaN devices for hard switched low power PV-applications.

The performance of the selected multi-input AC-module topology is analyzed by model-based optimization. The wide-operating range of PV-converters, accounted for by the European efficiency, requires detailed loss models accurately predicting losses over the whole load range. To achieve the desired modelling accuracy advanced magnetic models are applied. To accurately model the losses in a foil winding exposed to an airgap-field, a new method is proposed, which is not restricted to certain winding geometries. Measurements on prototype transformers confirm the validity of the developed method. The deviation between the measured and the modelled foil losses stays below 15%. The leakage inductance and parasitic capacitance are modelled by improved methods, applicable to arbitrary winding geometries. The accuracy of the applied models is verified by experiments. The modelling error is below 20%. Furthermore the transformer parasitics are found to substantially influence the operation of the DC-DC flyback converter at low output power. A detailed analysis of the flyback operation under these non-ideal conditions is performed and formulas are derived, which allow to calculate the losses caused by the parasitic elements.
To reduce the complexity of the system-optimization, the optimization of the DC-AC stage and the DC-DC stage are performed separately. The implemented optimization routines optimize the system efficiency for a given volume-constraint. The routines include the optimization of system-level parameters, such as switching frequency and output-filter parameters, as well as component-level parameters, such as inductor core-size, winding turns-number and wire diameter.

To enable an AC-module design with decent efficiency the converter is built with GaN devices, featuring unprecedented switching performance. For the primary switch of the flyback DC-DC stage 100V rated GaN devices are applied and 650V rated devices are used for the DC-AC fullbridge stage. Low voltage GaN devices up to 200V blocking volt-

age are already well established and are available in the appropriate current- and voltage ranges needed for the design of AC-modules. The high voltage GaN devices with 650V blocking voltage are still a novelty and not yet available with the voltage and current-rating of 600V/2A, typically required for an AC-module. Overrated 650V/7A devices are applied for the prototype of the DC-AC stage, causing higher gate-drive and switching-losses than an optimally rated device. Moreover the packaging, the key to reveal the full performance of GaN, is not fully mature yet. Experimental results on a 400V/10A halfbridge demonstrator setup reveal, that the achievable switching speed is limited by the package parasitics. Nevertheless switching-loss measurements confirm the outstanding performance of the GaN devices with total halfbridge switching losses of merely 30μJ at 400V and 4A. With expected improvements in packaging soon to come, the switching performance will further improve.

A performance study of the multi-input AC-module is carried out, calculating the volume versus efficiency, η-ρ, pareto-front by model-based optimization. To verify the performed analysis, prototypes of the DC-AC and the DC-DC stage are built. The models agree well with the experimental results, exhibiting deviations below 15% between modeled and measured losses. The efficiency of the complete prototype is estimated from the measurement results of the DC-AC and DC-DC stage prototypes and appears to be η_{EU}=93.45%. This is 0.7% below the pareto-optimum for the given volume and core-material. The availability of appropriate standard core-sizes is very limited, such that custom-made core-shapes would be required to achieve the pareto-optimal efficiency. The core of the DC-DC stage flyback transformer is best made of Si-ferrite N49. For the inductor of the DC-AC stage, cut-cores made of the pricey nano-crystalline Vitroperm 500F clearly outperform Microlite toroid powder cores, allowing for an increase of the European efficiency by 0.6%. With custom-made core-shapes and nano-crystalline inductor core-material a system efficiency of η_{EU}=94.5% can be achieved with a total boxed volume of the magnetic components and the output-filter of 325cm^3. This efficiency is substantially lower than the benchmark efficiency of commercially available single-input AC-modules of 95.5%. To improve the efficiency to η_{EU}=94.8% the volume must be increased to 450cm^3. An efficiency of η_{EU}=95% can only be achieved by nearly doubling the volume to 600cm^3. The system efficiency is

mainly limited by the DC-DC stage, whose efficiency can only be increased above 96.5% at the expense of an excessive transformer volume. Moreover the system-efficiency is extremely sensitive to auxiliary losses, such as the power-consumption of the control-electronics. A 100mW of auxiliary losses is found to result in 0.1% reduced European efficiency.

7.2 Conlusion

The concept of MPP-tracking on substring-level must finally compete against single-input AC-modules. Considering the BOS costs the only advantage of multi-input AC-modules is the increased energy yield under partial shading. For a commercial product, cost considerations limit the allowable magnetics and filter volume. With a typical volume of an AC-module converter housing in the range of 400cm^3, the investigated two-stage multi-input AC-module maximally achieves an efficiency of η_{EU}=94.5%. This is 1% lower than the benchmark efficiency of commercial AC-modules being η_{EU}=95.5%. Even with the application of the latest GaN device technology and low loss nanocrystalline core-materials, the efficiency-level of single-input AC-modules can not be achieved. The main loss-contribution originates from the transformer of the DC-DC stage, which limits the DC-DC stage efficiency to 96.5%. Depending on the partial shading conditions the substring MPP-tracking increases the yield by 1% to 2% for moderate and heavy shading scenarios [18]. In these cases the increased yield outweighs the reduced efficiency of the multi-input AC-module, resulting in a higher energy yield of the multi-input AC-module under heavy shading conditions. Considering the costs, a multi-input AC-module is more expensive than a single-input AC-module, due to the inherent higher part-count number. Moreover pricey, high performing semiconductor devices and core-materials must be applied in order to achieve a decent efficiency. This makes it difficult to compete against single-input AC-modules, given the fact that an increased yield can only be expected under heavy shading conditions. Furthermore GaN devices will for sure also be applied for single-input AC-modules, such that the benchmark efficiency will increase from currently 95.5% to possibly 96.5%, making competition even harder.
In order to be competitive, the efficiency and volume of multi-input AC-modules must improve well beyond the level achieved with the investigated two-stage AC-module topology.

The following improvements of the investigated two-stage multi-input AC-module topology could possibly increase the system efficiency:

- For the DC-AC fullbridge GaN devices with a rating of 600V/2A would be optimally suited. Moreover an improved power-module packaging in halbridge configuration would allow for improved switching performance
- The isolated gate-drive supply and the current and voltage mesurement circuits of the DC-AC fullbridge exhibit a standby power-consumption of 280mW. A redesign for minimized quiescent power could improve the European efficiency by 0.1% per 100mW power-reduction.
- The achievable efficiency of the DC-DC stage is dominated by the transformer core-material. A nano-crystalline material, with a higher saturation flux density, but same low core losses, would allow for an increased efficiency of the DC-DC stage. Unfortunately nano-crystalline materials are not available in appropriate small-scale standard core-sizes and feasible custom-made core-shapes would have to be designed.

Alternatively another topology could be chosen to realize the multi-input AC-module. The topology comparison identified a second promising multi-input AC-module topology. This topology, shown in figure 7.1 is conceptually similar to the high efficient single-stage AC-module topologies with single MPP-tracking. It consist of a power-balancer multi-port, which performs MPP-tracking on substring-level, and an LC resonant cyclo-converter, which is actually a single-input AC-module converter. The multi-port stage balances the three serial-connected ports and is only active, if the three inputs are unbalanced. In this way, the same efficiency as for single-input AC-modules can be achieved in balanced conditions. The single-phase power-decoupling is provided by electrolyte capacitors at the output of the multi-port. The challenge of this approach is the design of a power balancer stage with a low-loss standby-mode in balanced conditions and a low part-count.

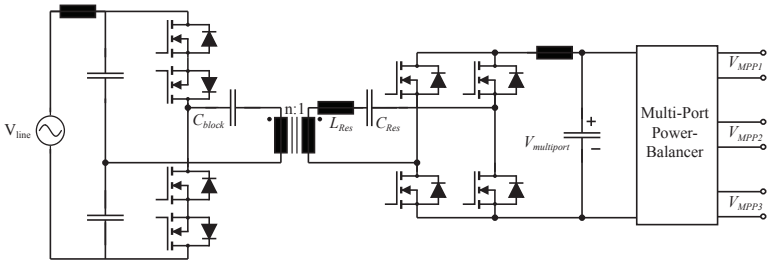


Figure 7.1: Alternative multi-input AC module converter topology with a power-balancer multiport [52] and an LC-resonant cyclo-converter [22],[23],[24].

List of Publications

Different parts of this thesis, including text, tables and figures have already been published in international scientific journals and conference proceedings. The publications generated in course of this PhD thesis are listed below, including also findings of other research projects carried out in parallel.

Journal Papers

- D. Leuenberger, and J. Biela, "Semi-Numerical Method for Calculation of Loss in Foil Windings Exposed to an Air-Gap Field", in *IEEJ* Journal of Industry Applications, vol.4, no.4, pp.301–309, 2015,
- M. Jaritz, S. Bluma, D. Leuenberger, J. Biela, "Experimental Validation of a Series Parallel Resonant Converter Model for a Solid State 115-kV Long Pulse Modulator", in *IEEE* Trans. on Plasma Science, vol.43, no.10, Oct. 2015

Conference Papers

- D. Leuenberger, and J. Biela, "Accurate and Computationally Efficient Modeling of Flyback Transformer Parasitics and their Influence on Converter Losses", Proc. of the 17th European Conference on Power Electronics and Applications (*EPE*'15, *ECCE* Europe), Geneva, Switzerland, September, 8-10, 2015.
- D. Leuenberger, and J. Biela, "Semi-numerical method for loss-calculation in foil-windings exposed to an air-gap field", Proc. of the International Power Electronics Conference 2014 (*IPEC*-Hiroshima 2014 - *ECCE-ASIA*), Hiroshima, Japan, May 18-21, 2014.
- D. Leuenberger, and J. Biela, "Comparison of a Soft Switched TCM T-Type Inverter to Hard Switched Inverters for a 3 Phase

PV Grid Interface", Proc. of the 15th International Power Electronics and Motion Control Conference (*EPE-PEMC*), Novi Sad, Serbia, Sept. 4.-6., 2012.

- D. Leuenberger, and J. Biela, "Triangular Current Mode Operation of a Three Phase Interleaved T-Type Inverter for Photovoltaic Systems", Proc. of the Power Conversion Intelligent Motion Europe (PCIM), Nuremberg, Germany, Mai 8.-10., 2012.

A

Flyback Transformer Design and Modelling

A.1 General Flyback Transformer Equivalent Circuit

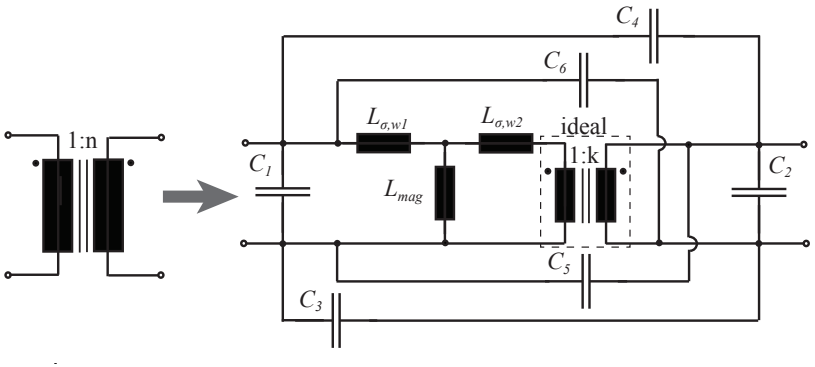


Figure A.1: General input-equivalent transformer circuit

The parasitic elements of any two port transformer can be split into an electrostatic and a magnetic part. The electrostatic behaviour of the transformer can be described by the equivalent circuit proposed in [122] and [123], consisting of six equivalent capacitances, the 6C-model. The magnetic part consists of the transformer magnetizing inductance L_{mag} and the leakage inductances between the primary and the sec-

ondary winding, referred to as the T-equivalent circuit [59]. The complete general equivalent circuit is shown in fig.A.1. Taking into account the specific operating conditions of the flyback converter, this general transformer equivalent circuit can be simplified for flyback-operation:

- **Equivalent Parasitic Capacitance:**
  In flyback converter operation, the transformer is subject to a bipolar voltage pulse V_{pulse} on the primary winding. Furthermore in most applications there is a constant isolation voltage V_{iso} between the negative rail of the primary and the secondary, see fig.A.2a).

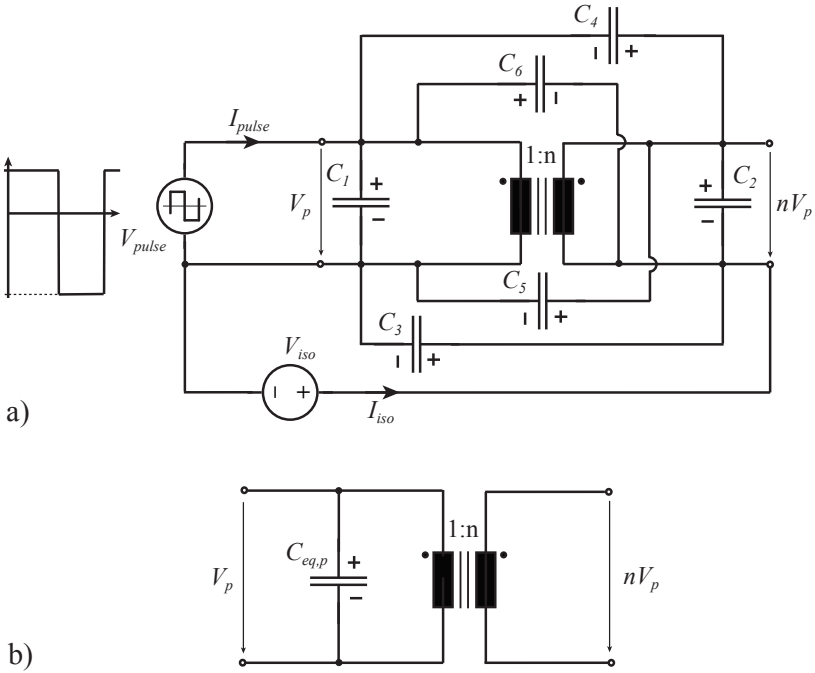


Figure A.2: a) Electrostatic model of flyback converter operation, b) general input-equivalent circuit

Under this operating condition, the total electrostatic energy stored

in the transformer can be expressed from the 6C-model by

$$W_{trafo} = \frac{1}{2}V_p^2[C_1 + C_2n^2 + C_4(N-1)^2 + C_5n^2 + C_6] + \frac{1}{2}V_{iso}^2[C_3 + C_4 + C_5 + C_6] + \frac{1}{2}V_pV_{iso}[C_4(n-1) + C_5n - C_6]. \quad \text{(A.1)}$$

The first part of this equation contains the energy, that the source V_{pulse} must deliver to charge the primary input to V_p, if $V_{iso} = const.$ Its structure allows for derivation of the energy equivalent capacitor

$$C_{eq,p} = C_1 + C_2n^2 + C_4(n-1)^2 + C_5n^2 + C_6 \quad \text{(A.2)}$$

The second part in (A.1) contains the energy delivered by the source V_{iso}, to charge C_3, C_4, C_5, C_6 to V_{iso}, under the condition that $V_p = 0V$. The last part of (A.1) is the additional energy delivered by V_{iso}, when $V_p \neq 0V$. It is caused by the charging currents of C_4,C_5 and C_6 flowing through V_{iso}. The equivalent capacitance $C_{eq,p}$ fully describes the dynamic behaviour as well as the capacitive energy seen from the flyback transformer primary and secondary input. There is a high frequency current I_{iso} flowing through the source V_{iso}, though this current does not cause losses in the voltage-source V_{pulse}. The losses caused by I_{iso} can only be determined on a system-level context. For the flyback converter analysis, the terms in (A.1) containing V_{iso} are therefore not relevant and the electrostatic model can be simplified to a one capacitor model as shown in fig. A.2b).

- **L-Type Magnetic Model:**
  The flyback converter operates the transformer as a coupled inductor. Figure A.3a) shows the equivalent magnetic circuit under these operating conditions. At turn-off of switch S_{in}, the current commutates from the input to the output-side. However due to $L_{\sigma,1}$ and $L_{\sigma,2}$ the current can not commutate immediately. A resonance takes places through the loop Com_{loop} marked in fig. A.3a), which leads to an overshoot of the blocking voltage at switch S_{in}. Changing the model to the simpler L-equivalent circuit, (fig. A.3b), does not influence this resonance, as the inductance L_σ is still within the same loop. The difference in

the two models is the current through L_{mag}. The T-equivalent reproduces a distortion in $i_{L,mag}$ caused by the resonance. The L-equivalent can not account for the magnetizing current distortion. For low leakage inductance, $L_\sigma \ll L_{mag}$, this distortion has a negligible influence on converter operation and transformer losses. As a flyback-transformer must fulfill this requirement for performance reasons anyway, the L-equivalent can usually be applied to model the magnetic behavior.

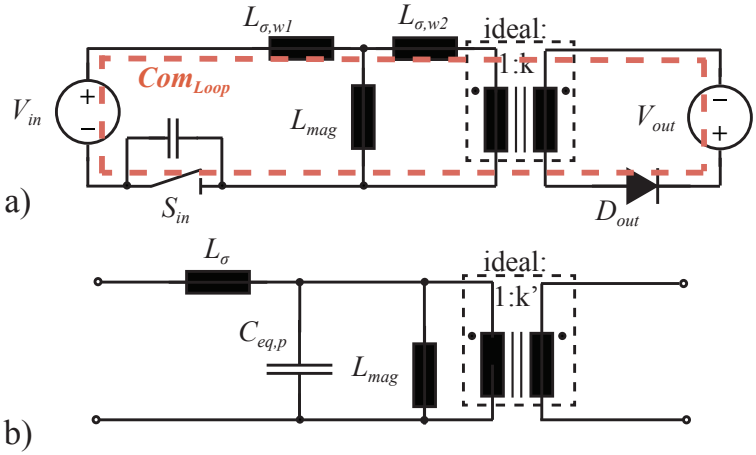


Figure A.3: a) Schematic of T-equivalent magnetic circuit in flyback operation b) General equivalent transformer circuit for flyback converter operation, with $k' \simeq n$ for $L_\sigma \ll L_{mag}$.

Finally, the general flyback transformer equivalent circuit is derived from the simplified electrostatic and magnetic model. The equivalent circuit referred to the primary side is shown in fig.A.3b). The equivalent capacitance $C_{eq,p}$ is in parallel to L_{mag}, to correctly reproduce the resonance taking place between L_σ and $C_{eq,p}$.

A.2 Calculation of the Magnetic Field in the Winding Window

The H-field in the winding window is determined by the current waveforms of the windings, which need to be given over at least one funda-

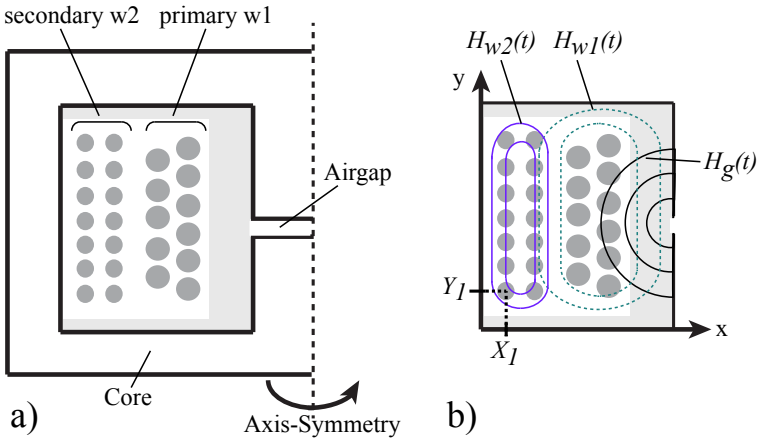


Figure A.4: Two winding flyback transformer calculation of 2-D H-field in winding window: a) winding arrangement, b) schematic graphic of the different H-field components in the winding window.

mental period T_p with a sampling frequency of T_s: $i_{w1}(tk)$ and $i_{w2}(tk)$ with $tk = kT_s$. To be able to calculate the proximity losses (see section 3.1.2), the discrete Fourier series of the H-field in the winding window must be calculated at the position of all conductors.

Figure A.4a) shows the example of a winding arrangement in a two-port flyback transformer. In fig. A.4b) a cartesian coordinate system is defined in the winding window. The H-field at the position of an arbitrary conductor (x_1,y_1) is then given by a vector field, which can be decomposed into an x- and y-component:

$$\overrightarrow{h}_e(x_1, y_1, t_k) = h_{e,x}(x_1, y_1, t_k) \cdot \overrightarrow{e}_x + h_{e,y}(x_1, y_1, t) \cdot \overrightarrow{e}_y, \qquad \text{(A.3)}$$

where $\overrightarrow{e}_x$ and $\overrightarrow{e}_x$ are the unit-vectors in x- and y-direction. Due to the orthogonality of the x- and the y-component, the discrete Fourier series (DFT) of $h_{e,x}$ and $h_{e,y}$ can be calculated separately (definition of

DFT see [124],formula 3.41):

$$\overline{H}_{e,x}(x_1, y_1, k) = \sum_{n=0}^{M-1} h_{e,x}(x_1, y_1, nT_s) \cdot e^{-j2\pi nk/M}, k = 0, .., M-1 \tag{A.4}$$

$$\overline{H}_{e,y}(x_1, y_1, k) = \sum_{n=0}^{M-1} h_{e,y}(x_1, y_1, nTs) \cdot e^{-j2\pi nk/M}, k = 0, .., M-1 \tag{A.5}$$

For proximity loss calculation, the normed field-amplitude $|\overline{H}(x_1, y_1, k)|$ at the frequency f_k is needed, which can be derived by applying the vector-norm:

$$|\overline{H}(x_1, y_1, k)| = |\begin{pmatrix} \overline{H}_{e,x}(x_1, y_1, k) \\ \overline{H}_{e,y}(x_1, y_1, k) \end{pmatrix}| \tag{A.6}$$

$$= \sqrt{|\overline{H}_{e,x}(x_1, y_1, k)|^2 + |\overline{H}_{e,y}(x_1, y_1, k)|^2} \tag{A.7}$$

$$f_k = \frac{k}{M \cdot T_p}. \tag{A.8}$$

By inspecting the equation for the proximity losses in 3.1.2 one can see, that this basically denotes, that the proximity losses in a conductor caused by $h_{e,x}$ and $h_{e,y}$ can be calculated independently $P_{prox,e} = P_{prox,e,x} + P_{prox,e,y}$. This is consistent with the fact, that losses in a round-wire can be calculated independently, if the current densities are orthogonal to each other [59],section 5.2.3 and 5.6.

As schematically shown in fig. A.4b), the H-field in the winding window consists of the super-position of three field components: the H-field caused by winding one h_{w1}, winding two h_{w2} and the airgap fringing-field h_g. Consequently $h_{e,x}$ and $h_{e,y}$ can be derived accordingly:

$$h_{e,x}(x_1, y_1, t_k) = h_{w1,x}(x_1, y_1, t_k) + h_{w2,x}(x_1, y_1, t_k) \tag{A.9}$$

$$+h_{g,x}(x_1, y_1, t_k), \tag{A.10}$$

$$h_{e,y}(x_1, y_1, t_k) = h_{w1,y}(x_1, y_1, t_k) + h_{w2,y}(x_1, y_1, t_k) \tag{A.11}$$
$$+h_{g,y}(x_1, y_1, t_k). \tag{A.12}$$

From the linearity of the Fourier expansion (see [124],section 3.5), it follows that the Fourier series of $h_{e,x}$ and $h_{e,y}$ can be calculated by:

$$\overline{H}_{e,x}(x_1, y_1, k) = \overline{H}_{w1,x}(x_1, y_1, k) + \overline{H}_{w2,x}(x_1, y_1, k) \tag{A.13}$$
$$+\overline{H}_{g,x}(x_1, y_1, k), k = 0, .., M-1, \tag{A.14}$$

$$\overline{H}_{e,y}(x_1, y_1, k) = \overline{H}_{w1,y}(x_1, y_1, k) + \overline{H}_{w2,y}(x_1, y_1, k) \tag{A.15}$$
$$+\overline{H}_{g,y}(x_1, y_1, k), k = 0, .., M-1. \tag{A.16}$$

The Fourier series of the winding- and airgap-fields in eq.(A.14) and (A.16) are calculated using the mirroring method explained in section 3.1.2.

The calculation of the winding-fields and the airgap fringing field are explained step by step in the following:

- $\overline{\mathbf{H}}_{\mathbf{w1,x}}(\mathbf{x_i}, \mathbf{y_i}, \mathbf{k})$ and $\overline{\mathbf{H}}_{\mathbf{w1,y}}(\mathbf{x_i}, \mathbf{y_i}, \mathbf{k})$:
  First, the winding current DFT is derived:

$$\overline{I}_{w1}(k) = \sum_{n=0}^{M-1} i_{w1}(nT_s) \cdot e^{-j2\pi nk/M}, k = 0, .., M-1. \tag{A.17}$$

  Then the equivalent field distance from winding one to the position (x_i, y_i) is calculated, which is defined in the following way, based on [65] eqn.(15):

$$\overline{efd}_{w1}(x_i, y_i) = \sum_{u=1}^{N_{w1}} \epsilon(x_i, y_i, x_k, y_k) \frac{((y_k - y_i) - j(x_k - x_i))}{2\pi((x_k - x_i)^2 + (y_k - y_i)^2)}. \tag{A.18}$$

N_{w1} is the number of conductors carrying the current $i_{w1}(tk)$, including the mirrored conductors. The function $\epsilon(x_i, y_i, x_k, y_k) = 0$, if $(x_i = x_k \cap y_i = y_k)$ and $\epsilon(x_i, y_i, x_k, y_k) = 1$, if $(x_i \neq x_k \cup y_i \neq y_k)$. Finally with the equivalent field distance and the winding current DFT follows:

$$\overline{H}_{w1,x}(x_i, y_i, k) = \overline{I}_{w1}(k) \cdot \mathfrak{RE}(\overline{efd}_{w1}(x_i, y_i)), k = 0, .., M-1, \tag{A.19}$$

$$\overline{H}_{w1,y}(x_i, y_i, k) = \overline{I}_{w1}(k) \cdot \mathfrak{IM}(\overline{efd}_{w1}(x_i, y_i)), k = 0, .., M-1. \tag{A.20}$$

- $\overline{\mathbf{H}}_{\mathbf{w2,x}}(\mathbf{x_i}, \mathbf{y_i}, \mathbf{k})$ and $\overline{\mathbf{H}}_{\mathbf{w2,y}}(\mathbf{x_i}, \mathbf{y_i}, \mathbf{k})$: The calculation is equivalent to winding one, with $\epsilon(x_i, y_i, x_k, y_k)$ defined in the same way:

$$\overline{I}_{w2}(k) = \sum_{n=0}^{M-1} i_{w2}(nT_s) \cdot e^{-j2\pi nk/M}, k = 0, .., M-1. \tag{A.21}$$

$$\overline{efd}_{w2}(x_i, y_i) = \sum_{u=1}^{N_{w2}} \epsilon(x_i, y_i, x_k, y_k) \frac{((y_k - y_i) - j(x_k - x_i))}{2\pi((x_k - x_i)^2 + (y_k - y_i)^2)}. \tag{A.22}$$

$$\overline{H}_{w2,x}(x_i, y_i, k) = \overline{I}_{w2}(k) \cdot \mathfrak{RE}(\overline{efd}_{w2}(x_i, y_i)), k = 0, .., M-1, \tag{A.23}$$

$$\overline{H}_{w2,y}(x_i, y_i, k) = \overline{I}_{w2}(k) \cdot \mathfrak{IM}(\overline{efd}_{w2}(x_i, y_i)), k = 0, .., M-1. \tag{A.24}$$

- $\overline{\mathbf{H}}_{\mathbf{airgap,x}}(\mathbf{x_1}, \mathbf{y_1}, \mathbf{k})$ and $\overline{\mathbf{H}}_{\mathbf{airgap,y}}(\mathbf{x_1}, \mathbf{y_1}, \mathbf{k})$: The airgap is modelled by a current density as described in section 3.1.2.
  First the magneto motive force of the windings Mmf_{wdgs} is calculated:

$$Mmf_{wdgs}(tk) = N_1 \cdot i_{w1}(tk) + N_2 \cdot i_{w2}(tk) \tag{A.25}$$

and with the linearity of the DFT (see [124],section 3.5) follows the Fourier series of $\overline{Mmf}_{wdgs}(tk)$:

$$\overline{Mmf}_{wdgs}(k) = N_1 \cdot \overline{I}_{w1}(k) + N_2 \cdot \overline{I}_{w2}(k), k = 0, .., M-1. \tag{A.26}$$

N_1 and N_2 are the turns-number of winding one and two. Next, the airgap current density is calculated according to formula 3.6 and 3.7. The magneto motive force of the airgap Mmf_g is given by:

$$\overline{Mmf}_g(k) = (-1) \cdot \overline{Mmf}_{wdgs}(k) \cdot \frac{R_g}{R_g + R_{c,sum}}, k = 0, .., M-1. \tag{A.27}$$

The DFT of the airgap current follows again by the linearity of the DFT [124]:

$$\overline{I}_{airgap}(k) = (-1) \cdot \overline{Mmf}_{wdgs}(k) \cdot \frac{R_g}{R_g + R_{c,sum}}, k = 0, .., M-1. \tag{A.28}$$

The calculation of the H-field caused by the airgap is then equivalent to winding one and two:

$$\overline{efd}_g(x_i, y_i) = \sum_{u=1}^{N_{g,mirr}} \epsilon(x_i, y_i, x_k, y_k) \frac{((y_k - y_i) - j(x_k - x_i))}{2\pi((x_k - x_i)^2 + (y_k - y_i)^2)}. \tag{A.29}$$

Note that $N_{g,mirr}$ includes the mirrored airgap conductors, and is therefore bigger than one.

$$\overline{H}_{g,x}(x_i, y_i, k) = \overline{I}_g(k) \cdot \mathfrak{RE}(\overline{efd}_g(x_i, y_i)), k = 0, .., M-1, \tag{A.30}$$

$$\overline{H}_{g,y}(x_i, y_i, k) = \overline{I}_g(k) \cdot \mathfrak{IM}(\overline{efd}_g(x_i, y_i)), k = 0, .., M-1. \tag{A.31}$$

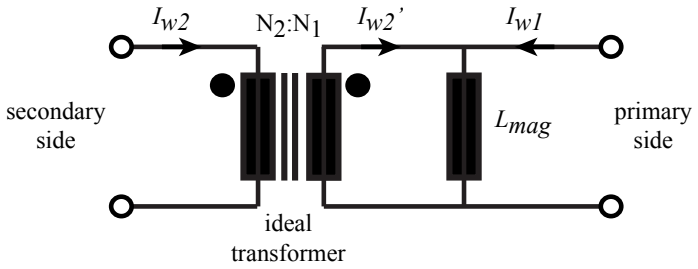


Figure A.5: Simplified flyback transformer model for B-field calculation.

A.2.1 B-field for Core Loss Calculation

The waveform of the core flux density $B(t)$ needs to be known, in order to calculate the core losses, see 3.1.1. $B(t)$ is determined by the current waveforms of the windings, which need to be given over at least one fundamental period T_p with a sampling frequency of T_s: $i_{w1}(tk)$ and $i_{w2}(tk)$ with $tk = kT_s$.
The flux-density is assumed to be uniformly distributed along the core-length, hence core-segments are not treated separately. The simplified transformer model shown in fig. A.5 is used, where the stray-inductances are neglected. The current through the magnetizing inductance L_{mag} referred to the primary-side of the transformer is given by:

$$i_{Lmag}(tk) = i_{w1}(tk) + N_2/N1 \cdot i_{w2}(tk). \tag{A.32}$$

N_1 and N_2 are the turns-number of winding one and two. The B-field in the core is calculated by approximating the transformer as an inductance with value L_{mag} and current $i_{Lmag}(tk)$. The B-field is then given by:

$$B(tk) = i_{Lmag}(tk) \cdot \frac{L_{mag}}{A_{core} \cdot N_1}, \tag{A.33}$$

where A_{core} is the cross section area of the transformer core.

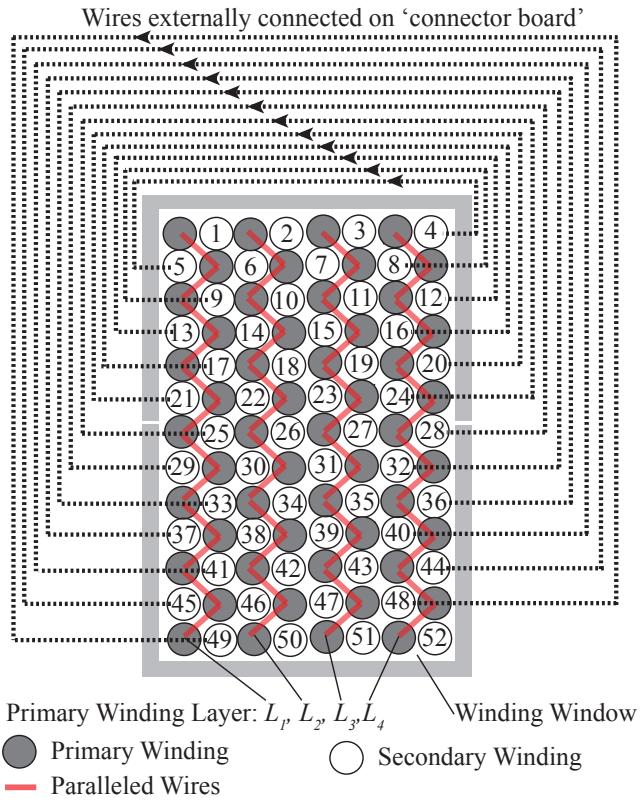


Figure A.6: 2D interleaving schematic layer arrangement approach using an external connector board

A.3 Advanced 2D Winding Interleaving

One of the main issues, limiting the efficiency of a flyback converter is the leakage inductance, caused by limited magnetic coupling between the primary and the secondary winding. As derived in section 2.4.4 and shown in fig. 2.26, the leakage inductance of a high step-up flyback converter could be reduced by a 2D interleaving structure. The difficult part is to derive an appropriate mechanical design and a feasible method to manufacture such an interleaving structure.

A feasible approach to manufacture an 2D-interleaved transformer

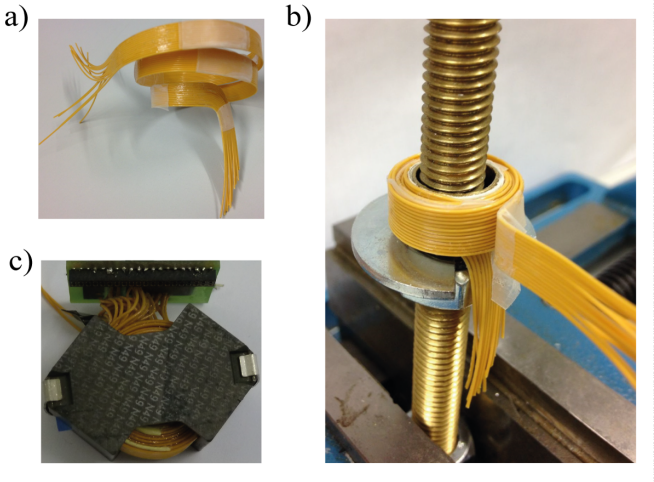


Figure A.7: 2D interleaving manufacturing steps: a) one layer of paralleled wires fixed with glue, b) wound coil with double layer of paralleled wires, c) mounted coil with external connector realized with a PCB

winding is developed in [125]. The layer-arrangement is schematically shown in fig. A.6. The primary winding consists of n_{ratio} paralleled wires with n_{prim} turns, where n_{prim} is the primary turns number and n_{ratio} the primary to secondary turns ratio. The secondary winding is realized by connecting n_{ratio} wires in series, whereas each of these wires having n_{prim} turns. The series connection of the wires is realized externally with a dedicated PCB connector board.

This approach allows to manufacture the coil as two layers, consisting of n_{ratio} wires and wound n_{prim} times. Figure A.7a)-c) shows pictures of the manufacturing steps. First, two layers of paralleled wires are manufactured. Glue is used to fix the wires. Second, the coil is built, with two layers wound n_{prim} times. Third, the wires are soldered to the PCB connector board, to realize the interconnection according to fig. A.6.
The most difficult part for this 2D interleaving approach is the connection of the wires to the external PCB connector board. The PCB connector board could not be mounted close to the transformer, due to

Table A.1: 2D Interleaved Flyback Transformer Prototype: Parasitic capacitance and leakage inductance.

Matlab-Model:	$C_{eq,prim}$= 12.7nF	L_σ= 6nH
Measured:	$C_{eq,prim}$= 12.6nF	L_σ= 30nH

the stiffness of the wires, as shown in fig. A.7c). This distance between the core and the PCB of course causes magnetic stray-fields, increasing the leakage inductance. Table A.1 compares the modelled versus the measured parasitic elements, see sec. A.1 and 3.3.3 for details on the transformer equivalent circuit and the measurement method. Whereas the measured parasitic capacitance corresponds well to the value predicted by the model, the measured leakage inductance L_σ is a factor five higher than predicted by the model. The wiring to the PCB connector board and maybe also some imperfect placement of the wires within the coil leads to a large increase in the magnetic stray-field. Such that the ideally predicted leakage inductance can not be achieved with the practical setup. The additional leakage inductance caused by the imperfections of the practical setup is 24nH for the given prototype transformer.

B

Core Losses in Gapped Laminated Cores

Laminated cores exposed to a magnetic field perpendicular to the laminated sheets are subject to Eddy currents [126],[127],[128]. When using laminated cores for inductors, the airgap causes a magnetic fringing field. The fringing field, exhibiting also field-components perpendicular to the laminated sheets, causes eddy-currents in the vicinity of the airgap. These eddy currents influence the inductance characteristic [129] and locally increase the core-losses [130]. The work in [63], which investigates laminated cores from Hitachi Metals, reports an increase of the high-frequency core-losses by 200%-300% compared to ungapped cores. Special shaping of the core in the vicinity of the airgap can substantially reduce these additional core losses [63],[130]. Though the shaping is difficult to manufacture and not applicable to standardized available cores. For a general switched-mode power converter application, the Eddy currents are negligible for low-frequency, e.g. the line-frequency, but become relevant for the flux-components with switching frequency. For accurate core-loss calculation, the increase of these high-frequency losses must be considered.

In this work laminated cores from two manufacturers are taken into account for the model-based system optimization and the prototype systems.
First, the AMCC-series C-cores made of the amorphous metal Metglas 2605SA1. The high frequency losses for these cores are modelled baaed on [63], reporting an increase of the high frequency losses by a factor two to three. At switching frequency, the core-loss components calcu-

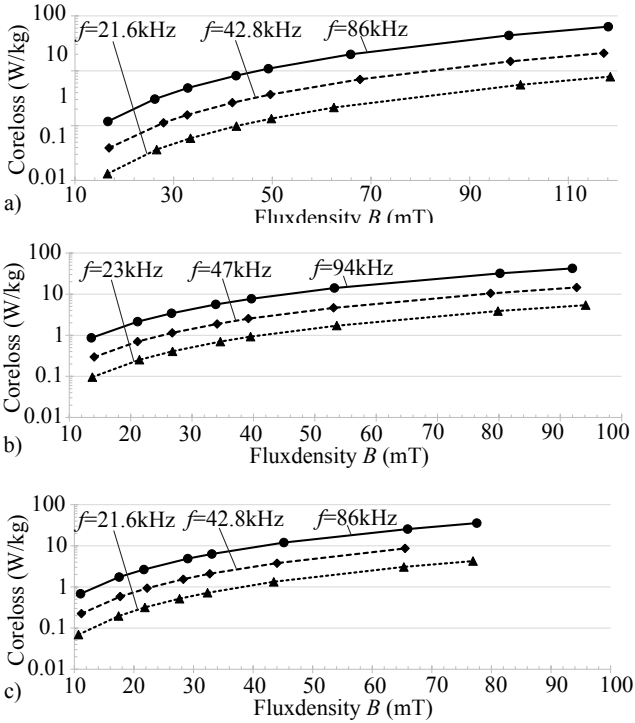


Figure B.1: Measured core-losses of VAC W156 core for different airgap-lengths (at room-temperature ∼25°C): a) 2·120μm, b) 2·240μm, c) 2·480μm

lated with the iGSE (see section 3.1.1) are multiplied by a factor three, to account for the increased losses.

Second the nanocrystalline cut cores from Vacuumschmelze (VAC) made of VITROPERM 500F. These cores are predominantly applied for power transformers. Nevertheless the VITROPERM 500F material exhibits decent core-loss characteristics, making it interesting for the design of high efficiency inductors. From the manufacturer and also in literature no information is available on the loss-characteristics of gapped VITROPERM 500F cores. The core-losses are therefore measured on a T60102-L2083-W156 C-core with two airgaps (one on each leg) for the typical frequency and flux-density range of a switching ripple. The ap-

plied measurement method is described in detail in section 3.2.3. The core-losses are measured at three frequency points ∼20kHz, ∼45kHz, ∼90kHz and for flux-densities between 10mT and 100mT. Further the measurements are carried out for varying airgap lengths: 120μm,240μm and 480μm. The complete measurement series are shown in fig. B.1. The high frequency losses increase with bigger airgap. Compared to the losses predicted with the iGSE [61] for an ungapped core, the measured high frequency losses increase by 200% to 450% depending on the frequency and the airgap length. The accuracy of the performed core-loss measurement is ±1.8%, based on the derivation in sec. 3.2.3. For the system design and model-based optimization the losses in gapped VITROPERM 500F C-cores are modelled based on interpolation of the measured losses.

C

Lifetime of Capacitors used in AC-Modules

C.1 Aluminium Electrolytic Capacitors

Aluminium electrolytic capacitors differ from other types of capacitors, regarding their operation principle, which is based on electrochemical processes in the liquid electrolyte [131]. This particular operation principle offers the well known advantages of these type of capacitors:

- high power density (i.e. capacitance per unit volume)
- high ripple current capability paired with a high reliability
- good price/performance ratio

An inherent characteristic of electrolytic capacitors is their fast aging at high operating temperature. It reduces the useful lifetime at higher operating temperature and is actually the main drawback of this capacitor technology.

C.1.1 Basic Construction

The aluminium electrolytic capacitor consists of two wound up aluminium foils, an anode and a cathode foil. The surface area of the anode foil is enlarged by electrochemical edging [131]. The dielectric layer consists of an aluminium oxide layer (Al_2O_3) built up directly on the anode, by the so called forming process. The cathode is realized by a liquid electrolyte, which ensures proper contact between the dielectric

layer and the cathode, and an aluminium foil, that passes the current to the electrolyte. Details on the production processes are given in [131].

C.1.2 Aging of Electrolytic Capacitors

The primary cause for aging, resp. wear-out of electrolytic capacitors is the vaporization of the liquid electrolyte and its loss through the seal [132]. With decreasing amount of electrolyte the capacitor parameter drift. The equivalent series resistance (ESR) increases, whereas the capacitance value decreases. The end of useful lifetime is reached, when the parameter drift reaches a certain limit.
The loss of electrolyte is caused by the following mechanism: The volume decreases, when the electrolyte is under high pressure, hence the volume decrease (dV_{el}/dt) is a function of the electrolyte vapor pressure. The vapor pressure itself depends on the temperature of the electrolyte and can be modelled as an exponential function of the temperature [132]. The electrolyte temperature rise, for a given ambient temperature and operating current waveform, is determined by the thermal resistance (electrolyte to ambient) and the ohmic losses (ESR). The thermal resistance depends on the internal geometry and the dimensions of the capacitor and is essentially constant over the whole lifetime. The ESR, as mentioned before, is not constant. First it increases over the lifetime when electrolyte volume diminishes. Second a temperature increase in the electrolyte also increases the ESR. This accelerates the aging.

C.1.3 Lifetime Models for Electrolytic Capacitors

Lifetime of electrolytic capacitors is normally derived by accelerated testing. The measured lifetimes are extrapolated to estimate lifetime using the following commonly used equation [132], [133] :

$$L_x = L_0 \cdot 2^{\frac{T0-Ta}{10K}} \cdot K_R \cdot K_V \tag{C.1}$$

With

L_x resulting lifetime

L_0 lifetime at nominal ripple and upper category temperature (datasheet)

T_0 upper category temperature

T_a ambient temperature during application

K_R ripple factor (self-heating)

K_V voltage factor (operating temperature)

This lifetime model predicts a doubling of lifetime for every 10K decrease in operating temperature. Even though (C.1) is widely used for the design of power electronic components, the authors of [132] showed, that the equation leads to overestimation of the lifetime of up to 130%, when the temperature difference between the upper category temperature T_0 and the operating temperature T_a is high ($\Delta T = 50K$). The equation (C.2) is the Arrhenius equation. It relates energy levels through temperature to chemical reaction rates [132].

$$L_x = U \cdot e^{E/T} \tag{C.2}$$

With

L_x resulting lifetime

U constant (hrs)

E activation energy / Boltzmann's Constant (1/K)

When the Arrhenius equation is related to the upper category temperature as in eqn. (C.3), a more accurate prediction of lifetime is achieved [132]. The

$$L_x = L_0 \cdot e^{E\frac{T_0 - T_a}{T_0 \cdot T_a}} \tag{C.3}$$

With

L_x resulting lifetime

L_0 lifetime at nominal ripple and upper category temperature (datasheet)

T_0 upper category temperature

T_a ambient temperature during application

E activation energy / Boltzmann's Constant (1/K)

The parameter E takes into account the effect of many physical constants and geometric parameters and is specific for individual series of capacitors [132].

Table C.1: Calculation of estimated electrolytic capacitor lifetime for the Negev desert temperature profile shown in fig. C.1.

L_0 (hrs)	T_0 (°C)	Aging per year L_{year,T_0} (hrs)	Useful lifetime L_x (years)
4000	85°C	288	14
10000	85°C	288	34
4000	105°C	72	55
10000	105°C	72	138

C.1.4 Lifetime Estimation of Electrolytic Capacitors in AC-Modules

To estimate the lifetime of the electrolytic capacitor in an AC-module, the typical capacitor temperature is needed over a time span of one year (averaged values over several years favorable). From the temperature measurements, the temperature frequency distribution can be calculated. Equation (C.1) is used to determine L_{year,T_0}, the effective aging at rated temperature T_0 over one year. Subsequently the expected lifetime L_x at rated ripple current and voltage is calculated by:

$$L_x = L_0 / L_{year,T_0}. \tag{C.4}$$

As explained in C.1.2, high operating temperature accelerates the wear-out effects of electrolytic capacitors. The worst-case scenario for electrolytic capacitor lifetime is therefore operation under very high temperature. In [14] the temperature distribution of an AC-module capacitor was calculated out of PV-cell temperature measurements in the Negev desert in Israel. The temperature distribution assumes that the capacitor temperature equals the inverters heat sink temperature. The heat sink temperature is approximated by: $T_{heatsink} - T_{ambient} = 1.25 \cdot (T_{cell} - T_{ambient})$, which was shown to be realistic for inverters with a proper thermal design. The capacitor temperature distribution for the Negev desert calculated in [14], is shown in fig. C.1 and will be used to calculate capacitor lifetime under worst case condition.

Table C.1 shows the calculated lifetime estimation, L_x, and the effective aging at rated temeperature per year, L_{year,T_0}, for four different capacitor specifications. According to the estimated lifetimes a capacitor with a useful lifetime of 10000hrs@85°C or 4000hrs@105°C is sufficient to exceed a lifetime of 25 years, which is normally required for AC-modules.

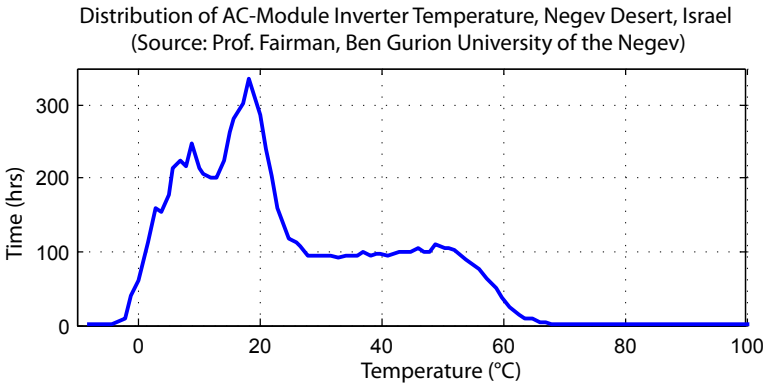


Figure C.1: Frequency distribution over one year of the AC-module inverter heat-sink temperature, measured at the Negev desert, Israel [14].

However these lifetime estimations have to be interpreted with care. As mentioned in [132] and discussed in C.1.3, the accuracy of equation (C.1) drops, when the difference between the upper category temperature T_0 and the operating temperature T_a is high (130% overestimation at Δt=50K). As can be seen from fig. C.1 the highest share of operating hours is in the temperature range of 0-40°C. Especially for the lifetime estimations with T_0=105°C, but also with T_0=105°C, a substantial amount of the operating hours have a difference bigger than 50°C to T_0. Thus, according to [132] the calculated lifetime estimation are propably overestimated by at least a factor two. The only way to get higher accuracy would be to perform systematical lifetime measurements, fit them to equation (C.2) and finally use (C.3) for lifetime estimation.

In [21] a similar capacitor lifetime estimation was performed also based on equation (C.1). These calculations use a simplified temperature profile, but additionally take into account the ripple current flowing through the capacitor. With the ESR and the thermal resistance the temperature rise caused by the ripple current is calculated. Two different placement of the electrolytic capacitor are investigated: in parallel to the PV-module ($V_dc = 40 - 60V$) and at an intermediate DC-link ($V_{dc} = 300-500V$). The calculations revealed, that the capacitor placed

at the intermediate DC-link has a 46% longer expected lifetime, than the capacitor placed in parallel to the PV-module. The reason for the different lifetime is the higher operation temperature of the capacitor at the PV-module due to higher currents and hence higher ohmic losses.

C.1.5 Electrolytic Capacitors in AC-Modules: No-Go or No Problem?

In the foregoing sections it was shown, that electrolytic capacitor lifetime is sensitive to operation under high temperature. The important question that arises is, whether a lifetime of 25 years can be achieved with electrolytic capacitors or not. If not they should be avoided in AC-modules.

From the lifetime estimation in C.1.4 it seems feasible to achieve a lifetime of 25 years. However a careful thermal design, systematical lifetime measurements on the applied capacitor and voltage- and current-overrating are necessary to get an accurate lifetime estimation and a sufficient margin to compensate for overestimation.

In literature electrolytic capacitors were often declared as the lifetime limiting component in AC-modules [11],[134],[135]. Various topologies were investigated and proposed, which made it possible to avoid electrolytic capacitors [134],[135],[29],[136],[20]. However recently the trend changed and newer publications propose topologies, were large capacitive storage is necessary, which is realized with electrolytic capacitors [22],[23],[25].

When analyzing the topologies of commercially available AC-modules, it turns out, that the manufacturers don't agree neither [13]. There are AC-modules with [29] and without electrolytic capacitors [37] , depending on the manufacturer. One manufacturer applying electrolyte capacitors, provides an expertise, which shall confirm 30-years lifetime of the capacitors in their design (with $T_{max} = 65°\mathrm{C}$) [137], [138].

C.2 Multilayer Ceramic Capacitors (MLCC)

Multilayer ceramic capacitors are manufactured as chips, for surface mounting on the PCB (SMD). MLCC feature a high capacitance density ($\mu F/\mathrm{m}^3$) and are available at capacitance values up to $100\mu F$ and a rated voltage up to 1.2kV.

C.2.1 Basic Construction and Features

The capacitance is formed by two electrode foils, which have a gap in between, filled with ceramic dielectric. The ceramic dielectric features a high relative dielectric constant, which allows for higher capacitance densities than other capacitor technologies (electrolyte and film). The MLCC chip consists of multiple layers of serial connected electrode foils, to increase to effective surface area of the electrode foils, which increases the resulting capacitance. The applied ceramic dielectrics can be roughly divided into two subgroups, the low relative dielectric constant types using materials as calcium zirconate or similar (Class I), and the high relative dielectric constant types using barium titanate or similar materials (Class II) [139]. The high relative dielectric constant type material is used to achieve capacitors with a high capacitance density. But these materials have the disadvantage of varying capacitance with temperature and applied AC-voltage. The low relative dielectric constant type materials feature a capacitance independent on temperature and AC-voltage, but lead to a lower capacitance density.

C.2.2 Aging of MLCC's

The capacitance value of MLCC's decrease with time, which is also referred to as aging. The decrease in capacitance is caused by alignment of electrical dipoles in the dielectric [140]. The alignment reduces the dielectric's capability of holding electrical charge and thus reduces the capacitance. The aging can be reversed by heating the dielectric above its Curie temperature. This process is also denoted as de-aging [140].

C.2.3 Lifetime and Reliability of MLCC's

MLCC's feature low failure rates of 0.001% per 1000hours, when manufactured according to military-standards [141].
Beside the reversible aging effect, manufacturers do not report significant wear-out mechanisms of MLCC's [141], [142]. However [143] notes, that insulation resistance of the dielectric degrades over time due to migration of vacancies. This has not been an issue so far, but can become a life-time limiting factor for miniaturized capacitors with a dielectric width in the range of 2-3μm or lower. Therefore [143] suggests an extra reliability assessment for capacitors with a high capacitance density (e.g. C $> 10\mu$F with X5R dielectric in an 0805 case size).

A further lifetime issue for MLCC's is mechanical destruction of the MLCC chip, due to cracking. Cracking is caused by mechanical stress applied on the solder joints, due to thermal cycling of the PCB and the MLCC chip [139] and bending of the PCB board in general. The mechanical stress on the MLCC chip can be reduced by either adjusting the amount of aplied tin-solder or mounting the MLCC's by the use of metal caps.

D

Multi-Input AC-Module Converters

D.1 Serial versus Parallel connected DC-DC Converters

The DC-DC converters for substring MPP-tracking can either be put in series or in parallel to feed energy into a common DC-link, as shown in fig. D.1. To compare these two approaches, the operating conditions are derived in the following for a given irradiance scenario.

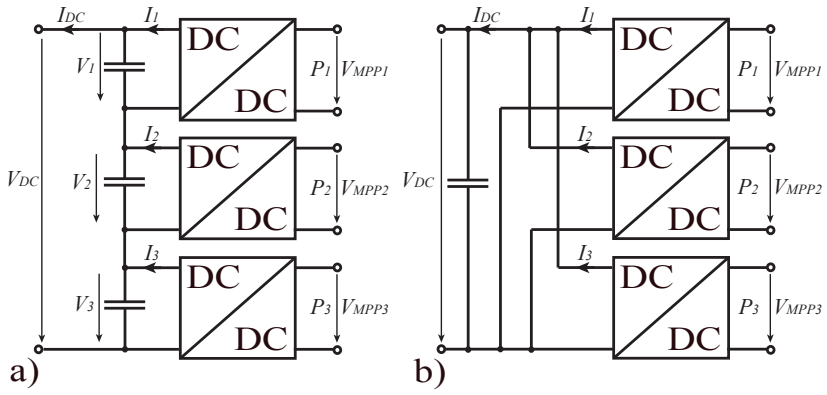


Figure D.1: 3xMPPT with intermediate DC-link: a) serial connection of DC-DC converters, b) parallel connection of DC-DC converters.

Operating Conditions:

- Indirect irradiance is assumed to be one forth of the global irradiance [53], hence $P_{pv,indirect} = 0.2 \cdot P_{pv,global}$.
- Intermediate DC-link voltage: $V_{DC} = 400V$.
- PV-string input voltage: $V_{MPPi} = 8.5V..21V$, i=1..3.
- The nominal power of the whole PV-module is $P_{nom} = 300W$
- $P_{str,max}$ is the power of one substring, without shadow. Hence under standard test conditions $P_{str,max} = P_{nom}/3$
- Temperature is assumed to be equal for the three substrings.

Serial Connection (fig. D.1a)):

- Szenario 1: String1 is shadowed,$P_1 = 0.2P_{str,max}$, and String2&3 are under direct irradition $P_2 = P_3 = P_{str,max}$. The total power is then $P_{tot} = 2.2P_{str,max}$ and substring powers are $\mathbf{P_1 = 1/11P_{tot}}$, $\mathbf{P_2 = P_3 = 5/11P_{tot}}$.
- Szenario 2: String1&2 are shadowed,$P_1 = P_2 = 0.2P_{str,max}$, and String3 is under direct irradition $P_3 = P_{str,max}$. The total power is then $P_{tot} = 1.4P_{str,max}$ and substring powers are $\mathbf{P_1 = P_3 = 1/7P_{tot}}$, $\mathbf{P_3 = 5/7P_{tot}}$.
- Szenario 3: All strings are either shadowed or under direct irradiation. In this case the power is either $P_{tot} = 0.6P_{str,max}$ or $P_{tot} = 3P_{str,max}$ and $\mathbf{P_1 = P_2 = P_3 = P_{tot}/3}$.
- Converter output current: $\mathbf{I_i = I_{DC}}$, i=1..3 and $I_{i,max} = P_{nom}/V_{DC} = 0.75A$
- Converter output voltage-range: With $P_{tot} = V_{DC}I_{DC}$ it follows for $V_i = Pi/I_{DC} = Pi/P_{tot} \cdot V_{DC}$. As P_i varies for the different shading Szenarios the range is $V_i = [0.091..0.71]V_{DC}$.
- Converter step-up ratio: The step-up ratio is $V_i/V_{MPP,i}$. Considering both ranges, of V_i as well as of $V_{MPP,i}$ the **step-up ratio** is [**1.73**..**33.5**]

Parallel Connection (fig. D.1b)):

- Converter output current: $\mathbf{I_i = I_{DC}/3}$, i=1..3 and $I_{i,max} = 1/3 \cdot P_{nom}/V_{DC} = 0.25A$
- Converter output-voltage and step-up ratio: The output voltage is constant and equals V_{DC}. The step-up ratio is $V_i/V_{MPP,i}$. Considering the range of $V_{MPP,i}$ the **step-up ratio** is [**19**..**47.5**]

For the given scenario, the serial connection features a lower total voltage step-up ratio than for the parallel connection of DC-DC converters. Though the serial connection requires a much larger relative step-up range, which could make a proper converter design more challenging.

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