Master Thesis

DC current breaking solutions in HVDC applications

Author(s):
Lenz, Viktor

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DC CURRENT BREAKING SOLUTIONS IN HVDC APPLICATIONS

MASTER THESIS

Viktor Lenz
vlenz@ee.ethz.ch

Supervisors: Tim Schultz and Arman Hassanpoor (ABB AB, Sweden)
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Abstract

A growing energy demand and the increasing integration of renewable generation require a major renovation of today's electricity grids. The most anticipated technology to upgrade the transmission grids are meshed high voltage direct current (HVDC) networks, which are capable of transmitting high power over long distances at low losses. Even though the required converter station technology as well as the lines are available and employed in point-to-point connection, “one of the key enabling technologies” [Fra11] is not market ready yet: The development of HVDC circuit breakers is an unavoidable necessity for reliable multi-terminal HVDC networks. Still, while up to now many concepts have been proposed, only a few prototypes have been tested for relevant voltage levels.

To identify the potential of existing approaches, this work attempts to identify the most practical HVDC circuit breaker concepts based on an extensive literature and patent review. The circuit breakers interruption characteristics are derived analytically and verified by computer simulations. The results of this analysis and a simulated test circuit serve as a basis to subsequently investigate the stress on the circuit breaker's components. Additionally, a sensitivity analysis of the interruption characteristics for different circuit breaker ratings and components is conducted to identify potential for technological improvement. In a simulated 4-terminal HVDC network, the circuit breakers are tested in three different fault cases to identify their applicability for future networks. This includes an analysis of fault currents, voltages in adjacent busses and currents in adjacent lines.

All of the investigated circuit breakers are able to deal with the different fault cases. However, due to the different topologies, the individual breakers offer diverse sets of features and limitations, which are described in depth in the corresponding chapters.
Acknowledgements

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Furthermore, I would like to acknowledge the fast, elaborate and helpful responses by M. Kowal, RWTH Aachen, and Y. Wang, Universität der Bundeswehr, to my questions regarding their publications and the circuit breakers discussed within.

Last but not least, I want to thank my parents and my girlfriend for their support throughout my studies and especially this final thesis work. Without the precious support of all the above mentioned people, it would not have been possible to conduct this project.
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1. Introduction

1.1. Motivation

Already more than 15 years ago, the need for HVDC circuit breakers for the operation of multi-terminal direct current networks was identified and specific requirements and protection schemes were discussed in detail [GKL+97]. These discussions were based on MTDC networks with current-source converter (CSC), which use thyristor valves switching in the frequency of the connected alternating current (AC) grid. Whilst the low switching frequency allows low loss operation, the main drawback of the CSC is their low controllability, especially the lack of reactive power control. This issue is addressed by the voltage-source converter (VSC) that uses switch-off semiconductors to be able to control active and reactive power independently. Due to considerable improvements in the technology of these devices, namely Insulated-Gate Bipolar Transistors (IGBTs), VSCs can nowadays be used to transmit high power at low losses. Because of these advantages, the voltage-source converter technology, especially in the improved form of the Modular Multi-Level Converter, have by now superseded the current-source converters, which dominated HVDC transmission for almost 50 years. Thanks to the simple power flow reversal and the power control, the voltage-source converter technology is more suitable for MTDC networks, and together with the technological improvement of cables for higher voltage ratings and the growing number of installed and planned HVDC links, commercial MTDC links are expected to be realized in the near future [MCB+15].

The VSC technology has one significant disadvantages towards the CSC by using IGBT valves: Due to the the anti-parallel diodes the converter station is not able to block the AC grid from feeding into the HVDC grid in case of a fault on the direct current (DC) side. The resulting high rates of rise of current require a very fast interruption of the fault, which is extremely challenging for HVDC applications.

On the basis of these findings HVDC circuit breakers were described as the “key technology” [Fra11] or the “show-stopper” [HJ11] for the realization of MTDC networks, whose introduction by now is desired by academia, industry and politics [Mey07, MCB+15, Eur13]. As a consequence, research groups have developed and proposed many HVDC circuit breaker concepts or worked on the improvement of the required components, such as fast mechanical switches. The proposed concepts utilize either mechanical or semiconductor switches or a combination of both, called hybrid, to break the fault current. Hybrid circuit breakers are regarded as the most promising concepts in the nearer future because they combine the advantages of fast operating times with low conduction losses. Nevertheless, only three circuit breaker concepts
suitable for VSC operation and all of hybrid design have been tested for high voltages [HJ11,GDPV14,WWZ+15].

To identify the potential of these and other promising circuit breaker concepts, this thesis aims at conducting a case study of the performance of promising circuit breaker concepts for application in future HVDC networks, focused on a comparison of their interruption characteristics and development potential.

1.2. State of the Art

Prior to this work, other studies have focused on comparing different breaker technologies and their results have influenced the selection of investigated circuit breakers as well as the studied characteristics.

[MKD05] conducted a comparison of four different circuit breaker concepts, three of hybrid and one of semiconductor design, with respect to scalability, costs, the maximum interruptible current and the resulting required grid inductance. For simulation, an idealized HVDC network, consisting of a DC source, an inductor and a resistor, was used. A circuit breaker solely based on semiconductors was identified as the best possible solution. However, the fact that industry has not followed this direction until now suggests that the occurring conduction losses or other disadvantages have not been weighted sufficiently.

[MLCS14] performed a purely analytical comparison of three different general concepts, namely mechanical, semiconductor and hybrid switch design. The concepts were discussed regarding their interruption time and power losses, as well as with respect to the published voltage and current ratings. As a conclusion, recommendations for technical improvement of the different technologies are provided.

[SD15] provided an extensive review of published DC circuit breaker solutions for all voltage levels and discussed their respective topology and operation principle. However, the publication neither discusses the performance of the individual solutions nor does it compare them.

[BF16] presented a comparison of four different circuit breakers with significant differences in operation speed, two mechanical, one hybrid and one semiconductor-switch based solution. The circuit breakers were simulated in a 4-terminal HVDC grid and the influence of the operation time on the network as well as of the grid parameters on the circuit breaker performance was investigated. The publication concludes that even relatively slow circuit breakers can operate in an MTDC when the grid parameters are adjusted accordingly.

A very recent publication, [YB15], compares three hybrid circuit breaker concepts proposed by industry, which are in the scope of this work as well but dimensioned differently, namely [HJ09], [DGC11] and [GV11]. The circuit breakers are simulated in an MTDC network and the stress on the circuit breakers are investigated. Aside from the latter publication, the comparisons merely focus on the fundamental comparison of different switch concepts rather than on practical circuit breaker designs. In addition, the assumptions for dimensioning or even the model parameters
itself are seldom published and in each publication the circuit breakers are only simulated for one single fault case. Parameter or fault variations are still missing in most publications.

1.3. Report Structure

To provide a theoretical overview of the latest circuit breaker concepts, a comprehensive insight into the most promising solutions and a clear, reproducible analysis of the circuit breaker characteristics, this thesis is organized as follows:

Chapter 2 presents the theoretical background of HVDC transmission. A general comparison outlines the strengths of HVDC before the components of an HVDC link are presented. Subsequently, the differences between point-to-point transmission and MTDC networks are discussed and the requirements for HVDC circuit breakers are derived.

Chapter 3 summarizes the key differences between the individual circuit breaker concepts and proposes a classification based on these differences. Out of the resulting classes, the most promising solutions are selected for further investigation based on well-defined criteria.

Chapter 4 presents the methods of the circuit breaker investigation. Definitions and modeling rules are set and the environment, in which the circuit breakers are simulated, is presented.

In Chapter 5, the interruption characteristics of the six selected circuit breaker solutions are described analytically and the results are verified by simulation. Subsequently the stress on the circuit breakers’ components is investigated and a sensitivity analysis of the interruption characteristics for different ratings and components is performed.

Chapter 6 presents the performance results of the circuit breakers in three different fault cases in a simulated exemplary MTDC network as well as the effects of the different circuit breakers on the network.

Chapter 7 compares the findings of the circuit breaker analysis and the MTDC grid study to provide an overall picture of the capabilities of the circuit breakers in comparison to each other as well as to outline the differences between fault interruption in the simple test circuit and the MTDC grid.

In Chapter 8 the key findings of this work are concluded and recommendations for further research are given.
2. HVDC Transmission Basics

Whilst high voltage AC networks were the technology of choice for power transmissions for more than one century, a rise of HVDC transmission from niche application towards a substantial element of electricity grid within the next decades has already started [MCB15]. In this chapter, the main differences between high voltage AC and DC transmission are outlined and the technology necessary for the promised development of HVDC system is presented.

2.1. Direct Current and Alternating Current Power Transmission

Using DC instead of AC for power transmission is not a new idea but has already been commercialized by Thomas Edison in the 1880s. As his systems operated at low voltage levels with high transmission losses at longer distances, and because the technology to transform DC voltage to higher levels was not available, the DC technology lost the “war of currents” against the AC system by Nikola Tesla, which was able to transmit power over longer distances at low losses thanks to the relatively easy AC voltage transformation [WGLC13]. Ever since, the AC technology has been the dominating technology for power transmission, but nevertheless, HVDC transmission has some key advantages over AC, which are summarized in Table 2.1.

Whilst most of the electric power is generated in form of AC, as it relies on rotating machines, such as steam and gas turbines, a few other technologies directly provide DC power, such as the latest wind power plants or solar panels, but the latter ones only on a low voltage level. The transformation of AC to higher voltage levels is cheaper in both, installation and running costs, as magnetic coupling can be used in-

<table>
<thead>
<tr>
<th></th>
<th>AC</th>
<th>DC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Generation</td>
<td>rotating machines, most power plants</td>
<td>solar (LV), wind</td>
</tr>
<tr>
<td>Transformation</td>
<td>Magnetic coupling</td>
<td>Power electronics</td>
</tr>
<tr>
<td>Power Transmission</td>
<td>$U_{rms}$</td>
<td>$U$</td>
</tr>
<tr>
<td>Transmission losses</td>
<td>Skin effect</td>
<td>linear</td>
</tr>
<tr>
<td>Length Restriction</td>
<td>Reactive power losses, Ferranti Effect</td>
<td>-</td>
</tr>
<tr>
<td>Conversion</td>
<td>AC-DC converter (Power electronics)</td>
<td></td>
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</tbody>
</table>

Table 2.1.: Comparison of HVDC and HVAC technology
stead of power electronics based DC-DC converters. Once the power is transformed to a high voltage level, the transmission capacity for DC systems in a given corridor, in terms of voltage rating, conductor distance and insulation requirements, exceeds the one of AC systems, because in the latter case the peak voltage defines insulation requirements whereas the root mean square value determines the transmitted power. In addition, significantly higher loses occur in AC than in DC lines, respectively a larger conductor is required for AC transmission because of the occurring skin effect, causing a non-uniform current distribution in the conductor. Furthermore, in AC systems the length dependent demand for reactive power limits the transmission of active power for long lines. This effect is even more severe for cables, due to their higher capacity per unit length, which results in a maximum economical link length of less than 100 km [Mig13]. Even though reactive power compensation is possible, it comes with the installation of costly devices in the grid and is unsuitable for sub-sea cables. To overcome the reactive power losses in AC cable systems, concepts of low frequency AC transmission have been proposed, especially for offshore connection, but not realized yet [RMO15].

Summarizing the advantages and disadvantages of AC and DC transmission, it becomes clear that HVDC is the preferable technology for the transmission itself, but it is only economical when the transmission savings exceed the costs for the converter stations compared to AC transformers, as illustrated in Figure 2.1.

The first rectifier valves on mercury-vapor basis were already developed at the beginning of the 20th century, but only after the development of mercury-arc valves, the first commercial HVDC system was put in operation 1954 to transmit 20 MW between the Swedish mainland and the island of Gotland with a length of 96 km. Following this milestone of HVDC technology, many other links were commissioned around the world, with ongoing improvement in the valve technology, such as the first thyristor based converter stations at the Eel River in Canada, commissioned 1972 [LN07]. With the fast development of the semiconductor technology during the last decades, the terminal costs of HVDC have been reduced considerably, making thyristor and IGBT-converter based HVDC transmission an economical alternative to AC trans-
Table 2.2: Fields of HVDC application and exemplary projects [RCS00]

<table>
<thead>
<tr>
<th>Field of application</th>
<th>Examplary projects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interconnecting non-synchronous grids</td>
<td>Brazil-Argentina Interconnection, Chateauguay (US-CA)</td>
</tr>
<tr>
<td></td>
<td>Chateauguay (US-CA)</td>
</tr>
<tr>
<td>Subsea</td>
<td>East-West Interconnector (UK-IE), CrossChannel (UK-FR)</td>
</tr>
<tr>
<td>Remote generation</td>
<td>BorWin 1-5, DolWin 1-4 (DE)</td>
</tr>
<tr>
<td></td>
<td>Destertec (Proposed)</td>
</tr>
<tr>
<td></td>
<td>Three-Gorges (CN), Itaipu (BR)</td>
</tr>
<tr>
<td>Bulk transmission</td>
<td>Rihand-Delhi (IN), Terranora (AU), Pacific Intertie (US), Ultranet (D, planned)</td>
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</table>

mission for an increasing field of applications [Jac11]. Some examples of the different fields of application of HVDC are listed in Table 2.2, ranging from the interconnection of non-synchronous grids and power markets to the connection of remote power generation or the bulk transmission to load centers.

Up to now, all commercial HVDC projects are two-terminal point-to-point connections, either employing converters based on thyristor, or IGBT technology. The following section describes the elements of an HVDC link and why circuit breakers are required for larger HVDC networks.

2.2. From Point-To-Point to Multi-Terminal HVDC Transmission

2.2.1. Point-To-Point HVDC Links

Nowadays HVDC links consist of two converter stations, each connected to an AC grid or power generator, one of them operating in rectifier mode transforming AC to DC power and the other operating as an inverter, transforming DC to AC, as well as HVDC cables or overhead lines, connecting the converter stations.

Converter Station

HVDC converter stations are either CSCs, based on thyristors, or VSCs, based on IGBTs. Aside from their design and control, the main differences of these two technologies are [SB08,Fra11,Buc14]:

- Active and reactive power can be controlled independently in a VSC system. For CSC, reactive power compensation equipment is needed.
To change the direction of the power flow, in VSC systems the direction of the current is changed, while in CSC, the voltage polarity is reversed by mechanically switching poles.

- The CSC technology achieves higher power ratings.
- Power losses due to switching are smaller in CSC.
- VSC systems can operate into weak AC grids and feature “black-start capability”.
- Other than VSC, CSC can limit DC short circuit currents.

Due to these differences, CSC-systems were primarily employed for high and very high power transmission over long distances, whereas VSC systems are employed in the the lower power range, e.g. offshore wind parks, due to their higher flexibility and control as well as their ability to function with significantly smaller filter units. Thanks to technological development in terms of reduced losses and costs, the VSC technology is expected to replace CSC in most fields of application [MCB+15,BWAF14].

Converter stations, respectively the complete HVDC link can either be realized in monopolar or in bipolar configuration. Bipolar configuration allows the transmission of higher powers, than a monopolar link by introducing a second pole of different polarity, but comes at the cost of doubling the number of components (converter stations, lines). Compared to two independent monopolar links, the bipolar design provides a higher level of redundancy and flexibility. Different combinations and realizations of these configurations are described and analyzed in more detail in [ABB+13b] and [Buc14].

Cables and Lines

<table>
<thead>
<tr>
<th>Table 2.3.: Ratings of HVDC cables and advantages, based on [Mig13]</th>
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<tbody>
<tr>
<td>MI-P/PPL</td>
</tr>
<tr>
<td>Installed ratings</td>
</tr>
<tr>
<td>Fabrication</td>
</tr>
<tr>
<td>Commissioning &amp;</td>
</tr>
<tr>
<td>Operation</td>
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For HVDC transmission, either overhead lines or cables (underground, sub-sea) can be used.

- For overhead lines, the maximum voltage ratings are expected to be at ±800 kV to ±1100 kV, only restricted by the insulation requirements. For Europe, a maximum voltage limit of ±500 kV is anticipated [MCB+15].

- For cable transmission, two different cable types are used in combination with HVDC transmission, mass impregnated cables with polypropylene laminated paper insulation (MI-P/PPL) and cross-linked polyethylene cables (XLPE), whose main differences...
are summarized in Table 2.3. Whilst MI-P/PPL is a proven technology with a long history and widely applied in CSC systems, XLPE cables are much easier and cheaper to manufacture and commission. Because of the elaborate but heavy insulation, MI-P/PPL cables are available for higher transmission voltages, but further development in the field of XLPE is expected, as the first VSC projects with 500 kV XLPE cables are already projected [Mig13, MCB+15]. As XLPE, other than MI-P/PPL, is not suitable for polarity reversal, it can only be used for VSC applications.

2.2.2. Faults in MTDC Networks

In HVDC networks, transient fault voltages and current surges can arise due to pole-to-ground, and in a bipolar network pole-to-pole faults. While overhead lines are often subject to temporary faults like lightning strokes, cables are affected by faults less often but usually more severe (e.g. mechanical damages by excavators or ship anchors). Furthermore, a fault can occur directly at the converter terminals, e.g. due to a technical failure in the appending switchyard, as well as in a remote place, hundreds of kilometers from the converter.

After the occurrence of a fault along the line, the voltage at the fault location decreases within microseconds to a voltage determined by the fault resistance, and voltage surges start traveling towards both terminals, discharging the line’s capacitance into the fault. In the following, these waves travel through the system and are (partly) reflected at places with a change of surge impedance, e.g. the current limiting reactor or the fault location. Due to reflection and superposition of traveling waves, the temporary voltage drop across the reactor can rise up to twice the nominal voltage for a specific fault distance, and induces a high rate of rise of current in the reactor, as described in more detail in [CBS13] and [SR14].

In case of a terminal fault, a voltage surge is only traveling towards the remote terminal, whereas the voltage at the faulted terminal immediately drops to the fault voltage level and the system voltage drop along the current limiting reactor defines the rate of rise of the fault current, which is nearly constant.

CSC have the capability of limiting the fault current to reduce the disturbance on the AC grid until circuit breakers on the AC side have interrupted the power supply. Similarly, in case of a fault on the DC side of conventional VSC systems, currently employed protection schemes can only trip the AC side circuit breakers cut of the power supply feeding the fault. Consequently, a fault in such a system causes a complete shut down of the DC system and an interruption of the power flow. Obviously, while this may be possible in smaller links or even small MTDC grids, this is not an option for high capacity links or larger MTDC grids.

Even though pole-to-ground faults are regarded as significantly more frequent than pole-to-pole faults [CP11], this thesis focuses on pole-to-pole faults as these are expected to be more severe [YFO10].
2.2.3. Multi-Terminal HVDC Transmission

Whilst all commercial HVDC links have been realized as two-terminal point-to-point connection, interconnecting several terminals with HVDC would be beneficial, as it for example promises a significantly cheaper and in terms of power flow control more advanced way of connecting large remote generation with multiple load centers. On a larger scale, e.g. in form of a European supergrid, an HVDC grid can increase trading capacity, balance power markets and share both intermittent renewable power and power reserves to provide higher security of supply [MCB+15]. It is expected that a large interconnected HVDC network will only develop over time, starting from the most needed and economically attractive interconnections and small MTDC networks [MCB+15]. A first three-terminal VSC 32 km pilot project, commissioned in China 2013, and a 1728 km three-terminal project, planned for commissioning in 2016, in India, indicate that the first generation of MTDC is of radial topology. But theoretically MTDC grids can be realized in radial, ring, lightly or heavily meshed, with different effects on power flow control and stability, as presented in [BWAF14]. [GKL+97] discusses theoretical design aspects of CSC-based MTDC networks, and the realization of hybrid MTDC networks, utilizing both VSC and CSC has been investigated [PCC06] as well. However, primarily because of their ability to control active and reactive power independently as well as to reverse the power flow without reversing the pole voltages, VSC are the preferred technology for future HVDC networks [Buc14, WJDS14, MCB+15].

2.2.4. VSC Topologies

Voltage-source converter are based on turn-off semiconductors, which allow controlled switching sequences to reduce low frequency harmonics compared to CSC topologies. Most of the VSC systems currently in operation are built as two-level converters, however, in recent years a trend towards multilevel converters is observed [WJDS14]. In the following paragraphs, the fundamentals of both technologies are presented [Buc14].

Two-level Converter

![Figure 2.2.: Two-level converter, adopted from Buc14](image)

The two level converter is the simplest converter technology to transform three phase AC voltage into a DC voltage. As illustrated in Figure 2.2, the three AC phases are
connected to both DC poles via a series connection of IGBTs. Between the DC poles, a capacitor is connected to smoothen the output voltage. The IGBT valves are switched based on a pulse width modulation scheme. The 2-level voltage switching leads to high harmonic distortion and extensive filter are required on both AC and DC side. As the valves consist of many IGBTs to provide full blocking capability, sophisticated drive units are required for simultaneous control, and due to the high switching frequency by the pulse-width modulation control, relatively high switching losses occur.

**Modular Multi-Level Converter**

![Image of Modular Multi-Level Converter](image)

**Figure 2.3.:** Modular Multi-Level Converter, adopted from [Buc14]

Multilevel converters intend to reduce the harmonic disturbances and high switching losses by providing multiple levels of output voltages. In principle, the different voltage levels are achieved by a series connection or cascade of capacitors are charged to a common fraction of the total voltage $U_{DC}$ and can be connected or bridged in discrete steps. Several multilevel topologies have been developed, which are discussed in more detail in [Buc14]. The most popular multilevel converter concept is the MMC, first proposed in [LM03]. Like the two-level converter, the MMC consists of six valve arms. In difference to the two-level converter, the valve arms of the MMC consist of $n$ submodules, each consisting of a charged capacitor and (in half-bridge configuration) two IGBTs, as illustrated in Figure 2.3. Therefore, each submodule is an independently controllable voltage source of either $U_{SM}$ or zero voltage and bypassing, depending on the switching state of its IGBT. With an adequate number of submodules, which the converter can control dynamically, a stepped sinusoidal voltage at the AC side is provided, which causes considerably less distortions compared to the pulse-width modulated two level converter.

Whilst the MMC successfully reduces the switching losses and harmonic distortions, a relatively high number of IGBTs and large capacitors are required.
Challenges for VSC MTDC

The main challenge for MTDC in general and for VSC MTDC in particular, is the handling of faults in the DC grid. As mentioned previously, for high power links and larger grids, a shut down of the DC system is unacceptable, since interrupting the power flow could result in stability problems in the connected AC grid as well.

To protect the AC grid from HVDC faults several converter concepts have been proposed, which are capable of blocking AC current contribution in case of a fault [WM13]. However, these converter stations come at the cost of a higher number of semiconductors, and on the other hand, a fault would still require the whole MTDC network to be de-energized.

As a consequence fast and reliable HVDC circuit breakers, which allow selective fault clearing similar to AC networks, are a necessity for MTDC networks. Furthermore, circuit breakers can also be employed in point-to-point links to provide a faster disconnection [DJSH14].

Depending on the fault location and resistance, very high rates of rise of fault current that exceed the circuit breakers interruption capabilities, can occur in an HVDC network. It is likely that these have to be limited to ensure the network’s protection, e.g. by reactors in series with circuit breakers. As an alternative or in combination, the aforementioned converter stations with fault current blocking or limiting capability can be used to reduce the requirements on the deployed circuit breakers [CG15].

2.3. HVDC Circuit Breaker

In principle the key requirements for HVDC circuit breakers are the same as for their AC counterpart [Fra11]:

- Interrupting the line current in any fault case by building up a counter voltage equal to or larger than the system voltage.
- Withstand the transient voltage response of the network subsequent to the interruption.

In addition, the HVDC circuit breakers must de-energize the system inductances, i.e. the current limiting reactor and the line inductance.

Research on HVDC circuit breakers has already been conducted for more than three decades and various applications, e.g. CSC point-to-point transmission [AC78] or nuclear fusion devices [TSK+80] and to some extent already in the anticipation of CSC MTDC networks [AYT+85,GKL+97]. Most of these concepts were based on a mechanical AC circuit breaker with a resonant LC circuit connected in parallel, to impose an alternating current onto the DC fault current and to enforce a current zero crossing as required for interruption, called passive resonance principle. The interruption with the employed AC circuit breakers takes several of tens of millisecond, which was found to be significantly to slow to interrupt the fast rising fault currents in VSC networks to maintain operation [TEK+15,SR14].
With improving of mechanical opening time, new actuation concepts and semiconductors for higher voltage ratings, and due to the increasing popularity of HVDC transmission, many new HVDC circuit breaker concepts have been proposed during the last decade. In principle, all of these concepts consist of two or three functional paths in parallel, as illustrated in Figure 2.4. After a short description of the functional path and the key switching devices, the following Chapter classifies many of the recently published concepts and describes the key operation principles.

**Nominal current path (NCP)** The nominal current path allows the current to pass through the circuit breaker with low conduction losses during normal operation. In the case of a fault, this conductive path has to be opened and must be able to withstand the transient interruption voltage (TIV) during the switching process. Due to the low ohmic losses in closed state and good dielectric performance in the open state, mechanical switches offer important advantages, but come at the cost of relatively long opening times. Today’s semiconductor switches have the disadvantage of higher on-state losses when conducting, but the ongoing research in the field of wide band-gap semiconductors will possibly reduce these losses in the future [Fra11, KMX+14].

**Current commutation path (CCP)** In contrast to the semiconductor solutions, most mechanical interrupters are not able to create a sufficient counter voltage in the nominal branch to interrupt the current. Hence, to bring the current to zero in the NCP and enable the mechanical switch to build up its voltage withstand capability, the current is commutated into the CCP. Different principles and components are used to achieve this, e.g. small semiconductor switches or arcs in the mechanical interrupters to create a voltage drop in the NCP as well as charged capacitors in the CCP, which force the current into the CCP. This path may be split into different sections that are activated by switching on semiconductor stacks or closing mechanical switches. In case of a semiconductor switch with full blocking capability on the NCP, a CCP is not required, a fault current is directly commutated into the energy absorbing path (EAP). The different commutation principles will be explained in more detail in the following Section 3.1.
Energy absorbing path (EAP)  When the circuit breaker acts to interrupt a fault current, severe transient over-voltages can occur. To limit the over-voltage across the circuit breaker and to dissipate the remaining energy from the system’s inductances, the decreasing current is redirected into the energy absorbing path. In most cases surge arresters with non-linear current-voltage characteristics are employed. In HVDC they usually consists of metal-oxide varistors that combine a very low leakage current at system voltage with a very low resistance above the clamping voltage. To reduce the risk of breakdown due to excessive heating and a thermal runaway, the operating time above the clamping voltage must be kept short.

2.3.1. Switches

In HVDC circuit breakers, either fast mechanical or semiconductor switches are employed. Both solutions include advantages and disadvantages.

Fast Mechanical Switches

In recent years, extensive research on fast mechanical switches has been conducted to overcome the use of slow AC circuit breakers for HVDC interruption concepts, e.g. [HF02, SFHK03]. The most promising approaches propose actuators based on the Thomson effect to achieve fast opening of the contacts in the range of milliseconds, either for no-load switches that only open at zero current [SOK+11, YHR+11, Bis15] or for vacuum interrupters with current interruption capability [NMY08, PHH15, WHD+15]. Prototypes of the so called Ultra-Fast Disconnector no-load switch achieved opening times of 2 ms at a nominal voltage rating of 320 kV [DJSH14] and for single 40.5 kV-VI 2.5 ms have been reported [WHD+15]. Aside from unanswered questions regarding the voltage grading and simultaneous opening of series connected vacuum interrupters as well as the wearing of the opening mechanisms in both technologies, the presented devices are prototypes and extensive test results are yet to be published.

Semiconductors

Commercially available high power semiconductor achieve blocking capabilities of 5 kV to 10 kV and above, but in the interest of reliability in HVDC applications, semiconductor are connected in series to provide at last 1.5 times the required blocking capability [HHJ14a]. As the current semiconductor technology causes voltage drops of at least 1 V to 2 V per device (cf. Table 4.2) at nominal current, a semiconductor array in the nominal current path of an HVDC link would cause conduction losses in the range of several hundred kilowatt. Wide band-gap power semiconductors are expected to achieve higher voltage ratings at lower losses [MGP+14], however these values until now are only predictions.
3. Classification of HVDC Circuit Breakers

In the scope of this project, an extensive literature and patent research of the latest CB technology was performed. As Table 3.1 shows, a scheme was developed that enables a classification of the HVDC circuit breakers based on two different criteria: (1) The method used to force the current in the nominal current path to zero and (2) the key switching device in the nominal current path, able to withstand the TIV. The first section of this chapter describes the classification criteria in more detail to provide a basic understanding for different circuit breaker concepts. In the second section, the most promising concepts and the reason for their selection are presented.

3.1. Classification

3.1.1. Interruption Method

Regarding the method which is used to reduce the current in the nominal current path to zero, three different methods are used by the latest HVDC circuit breakers [ABB+13b]:

1. Counter voltage
2. Divergent oscillation
3. Current injection

Counter Voltage

The counter voltage method covers all principles, which build up a voltage drop along the NCP to force the current in this path to zero. Concepts to build up this voltage include (1) the voltage of an arc drawn by opening a mechanical switch [MKD05, MR06], (2) semiconductor switches with turn-off capability [HJ09, KMX+14], (3) superconductors/PTC resistors [CBS13, LP06] or (4) a triggered LC-circuit [MKD05]. Depending on the magnitude of the counter voltage, the current either commutates into a path of lower resistance or it starts decreasing immediately, if the counter voltage is larger than the source voltage.

Building up a counter voltages which aim at current commutation (hundreds of volts up to tens of kilovolts) can be realized with all mentioned methods. But in all cases, a low-ohmic CCP must be connected in parallel to the NCP. In general the CCP is
Table 3.1.: Exemplary classification of analyzed circuit breaker solutions by DC interruption method and nominal path switch. The solutions selected for detailed analyses are set bold.

<table>
<thead>
<tr>
<th>Interruption method</th>
<th>NCP switch</th>
<th>Counter voltage</th>
<th>Current injection</th>
<th>Divergent oscillation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupter/Turn-off</td>
<td>[MKD05],</td>
<td>[RFRT07],</td>
<td>[AH01],</td>
<td>[Ska13]</td>
</tr>
<tr>
<td></td>
<td>[KMX+14],</td>
<td>[Mar11]</td>
<td>[AH01],</td>
<td></td>
</tr>
<tr>
<td></td>
<td>[ST14],</td>
<td>[EBH14],</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>[NX14],</td>
<td>[TEK+15],</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>[MR06],</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>[Cra12],</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>[WQLY13],</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>[BPSC11],</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>[LP06]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Disconnector/Turn-on</td>
<td>[HJ09],</td>
<td>[WWR+14]</td>
<td>[CA12],</td>
<td></td>
</tr>
<tr>
<td></td>
<td>[DGC11],</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>[DOB12],</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>[CBS13],</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>[MKD05]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

controlled by a switching device, in most cases a semiconductor which is turned on in the case of a fault. To limit the rate of rise of current in the semiconductor, a reactor can be connected in series.

In some concepts, a capacitor is connected in series with the semiconductor, so that the CCP operates like a snubber circuit. After interrupting the nominal current path, the capacitor’s voltage level increases until the current commutates into the EAP (e.g. clamping level of the arrester). An advantage of this concept is that it relies only on turn-on semiconductors instead of more expensive turn-off devices.

Building up counter voltages that are higher than the source voltage, to force the current to zero is also possible. However, while this can be achieved relatively easy by arcing voltages in low voltage grids, it becomes more difficult for higher voltages. Pure semiconductor switches are a possible realization for HVDC circuit breakers, but the required large stacks of turn-off semiconductors come at the cost of considerably higher conduction losses than mechanical or hybrid switching solutions [MLCS14]. In this case no additional commutation path but only a path to de-energize the system, e.g. through a varistor or a freewheeling diode [NX14], is required. This path can be connected in parallel [KMX+14] or as shunt to the ground [ST14].

Divergent Oscillation

The divergent oscillation method relies on the concept of a resonant LC circuit, formed between the commutation path and the nominal current path. In case of a fault, the resonant circuit can be excited by creating a commutation voltage in the main path. For a divergent oscillation, the superposition of fault current and oscillating current in the NCP eventually becomes zero, which makes it possible for a mechanical circuit
3.1 Classification

Figure 3.1.: Typical current and voltage waveform of a divergent oscillation [ABB⁺13b]

breaker or a turn-on semiconductor to interrupt the current as illustrated in Figure 3.1. To excite and stimulate this oscillation, several means can be used, such as (1) the arcing voltage of an opening mechanical switch, (2) a turn-off semiconductor or (3) the rising fault current itself if the inductor of the LC circuit is placed on the NCP. If an arc is used to excite the oscillation, a negative current-voltage characteristic is needed. However, the increase of the current amplitude is relatively slow and limited to a maximum value in the first case [AH01,Wal13]. By connecting turn-off semiconductors, which are switched on and off in the circuits eigenfrequency, in parallel [ALS94] or in series [Ska13], the amplitude growth is the accelerated and the performance can be improved.

Self-exiting resonant circuits require semiconductor switches on the NCP for immediate interruption. But because of the current zero crossings the less expensive turn-on semiconductors are sufficient [CA12,TKMK12].

Current Injection

Figure 3.2.: Typical current and voltage waveform of a current injection [ABB⁺13b]

The current injection method comprises principles which force the fault current in the NCP to zero by injecting a current of larger amplitude and opposite direction. In general, the required energy is stored in a capacitor, which is either charged by external
power units [EBH14] or by the power system [Mar11, TIK+12]. The most common implementation of this principle includes a capacitor that is placed in parallel to the NCP [AH01], in a shunt to the ground [GV11] or connected to the commutation path via inductive coupling [YTI+82]. The shape of the injected current pulse is defined by an inductor connected in series or in parallel. The moment of injection can be controlled by triggered sphere gaps [SZJ+15] or turn-on semiconductors [KCHM15]). In most cases, the current injection is realized by a pre-charged capacitor that gets discharged via an inductor and a (mechanical) switch into the nominal current path. Some configurations are limited to single pulse injections by unidirectional semiconductors [RFRT07, WWR+14] whereas others allow multiple zero crossings (resonant oscillation). Because of decreasing amplitude, the fault current is to be interrupted as fast as possible within the first current zero (CZ) in the NCP [HHJ+14b]. Due to the fixed amplitude of the injected current, small currents may constitute a challenge for a mechanical circuit breaker, since the superposition of small fault currents and high oscillation currents results in a high $\frac{dI}{dt}$ at current zero. The typical current and voltage curve of the current injection method are illustrated in Figure 3.2.

3.1.2. Nominal Current Path Switch

As outlined in the previous chapter, the type of switch in the nominal current path, which is able to withstand the transient overvoltage, determines the opening time (mechanical disconnector vs. interrupter) as well as nominal conduction losses and costs (turn-on vs. turn-off semiconductors) and is of high significance for the overall breaker performance. With respect to the nominal path switch, breakers are classified on whether they can (1) (interrupter/turn-off semiconductor) or (2) cannot operate under load (disconnector/turn-on semiconductor).

Interrupter/Turn-Off Semiconductor

Modern mechanical switching devices, which are capable of opening under load by drawing an arc, use either vacuum or gas as insulation medium. Due to their ability to create high arcing voltages, in the range of kilovolts [Wal13], gas interrupters are more suitable to build up a commutation voltage than VIs, with arcing voltages in the range of tens of volts [Sla08]. In contrast, VIs only need a relatively small contact separation distance, which is beneficial for high-speed operation. Additionally, VIs are able to cope with steeper current slopes before the zero crossing due to a faster de-ionization compared to gas circuit breakers. Consequently, the use of gas circuit breakers is preferred [MKD05, BPSC11, Cra12] for the counter voltage principle compared to VI [MR06]. The current injection method as well as the divergent oscillation utilize both kinds of mechanical interrupters (vacuum: [Mar11], [Ska13]; gas: [ALS94], [AH01]). Turn-off semiconductors with full voltage blocking capability on the other hand are only practical in combination with the counter voltage method [ST14, NX14, KMX+14].
### 3.2 Promising Concepts

Out of 32 interesting publications, the most promising solutions were chosen for further analysis and comparison, as highlighted in Table 3.1. Whilst one aim was to cover a broad range of different approaches, the main selection criterion was the expected performance of the different solutions, based on:

- Applicability for HVDC
- Interruption time (preferably below 10 ms [TEK+15])
- Losses during normal operation
- Published simulation data for HVDC operation
- Prototype test results
- Additional features of the CB

All but one circuit breaker topology are designed for the use in HVDC grids. However, even though this breaker is intended for the use in medium voltage grids, it appears to be scalable to high voltages. The requirement of a fast interruption time (< 10 ms) rules out all solutions that rely on the opening of gas-insulated circuit breakers as this technology has not yet achieved sufficiently fast opening times. The economical demand of low losses during normal operation cannot be met using state of the art semiconductors with full voltage blocking capability in the NCP, hence these are excluded as well. As a consequence of the latter, both classes *Counter voltage method with disconnector/turn-on semiconductor* and *Divergent oscillation method with turn-off semiconductor* are not further considered for investigation.

Based on the published information and some trial simulations, six promising circuit breaker concepts were selected out of the four remaining classes.

---

**Disconnector/Turn-On Semiconductor**

Gas or vacuum insulated disconnecting switches, which are only able to open under no-load conditions, are employed in the counter voltage method. They open as soon as a series connected unit (turn-off semiconductors [HJ09, DGC11, DOB12], PTC [CBS13], LC-circuit [MKD05]) successfully commutated the fault current into the CCP by building up a counter voltage.

Furthermore they can be combined with the current injection method in combination with a series connected unidirectional semiconductor, which prevents reversed current flow through the NCPs subsequent to the first pulse injection [WWR+14].

The application of turn-on semiconductors with full voltage blocking capability on the NCP is has only been proposed in combination with the divergent oscillation method, where they promise a fast interruption of the fault current at the first current zero crossing [CA12, TKMK12], but can theoretically be combined with the current injection method in a similar way.
1. LCS-MB: *Counter voltage method with disconnector*. Turn-off semiconductors in the NCP (Load Commutation Switch (LCS)) to build up the counter voltage and in the CCP (main breaking unit (MB)) to block the flow of the fault current.

2. LCS-C: *Counter voltage method with disconnector*. Turn-off semiconductors to build up the counter voltage in the NCP (LCS), turn-on semiconductors and capacitors in the CCP to build up the fault current limiting TIV.

3. Inj-C: *Current injection method with disconnector*. Multi-stage current injection from a single pre-charged capacitor (C) through different turn-on semiconductor paths.

4. Inj-PG: *Current injection method with interrupter*. Resonant circuit based pulse generating unit (PG) unit with turn-on semiconductors in shunt configuration for current injection into the NCP.

5. Inj-LC: *Current injection method with interrupter*. CCP consists of a resonant circuit with pre-charged capacitor and triggered spark gap (TSG) for current injection into the NCP.

6. Osc-ES: *Divergent oscillation method with interrupter*. Turn-off semiconductors (Excitation Switch (ES)) on the NCP to excite the oscillation, the CCP consists of a resonant LC circuit.

The following sections present each of these circuit breakers in more detail and explains its breaking operation based on a simplified, unidirectional layout. Table 3.2 summarizes the most important information that is publicly available.

### 3.2.1. Circuit Breaker 1: LCS-MB

The concept of the LCS-MB, a counter voltage method circuit breaker with mechanical disconnector in the NCPs, was patented 2009 [HJ09]. Following publications discussed the utilization of newly developed semiconductor devices [RSD14], design and protection of the LCS [HH11, HHJ14a] and its performance in multi-terminal grids [DJSH14, AAM15, CCBS15]. Further patents, proposing modifications with regard to operation [DW13] and components [WZX13, YZHM13], were published.

This concept was selected for further evaluation because of its fast mechanical opening time within 2 ms [HJ11], the published simulation data and most of all because of published test results. Successful operation of a 80 kV full scale prototype [HJ11], interrupting fault currents up to 16 kA within 2 ms [RSD14] has been reported. The LCS-MB is expected to have a short interruption time and the capability to interrupt a wide range of fault currents due to the interruption capability and speed of the semiconductors in the CCP. Additionally it allows pre-activation, which describes the initialization of the interruption process based on local fault detection before a trip signal is received. Thereby, the operation time delay between the trip signal and the current breaking can be reduced. If no trip signal is received for a defined amount of
### Table 3.2.: Overview of the circuit breaker solutions chosen for analysis

<table>
<thead>
<tr>
<th>Name</th>
<th>LCS-MB</th>
<th>LCS-C</th>
<th>Inj-C</th>
<th>Inj-PG</th>
<th>Inj-LC</th>
<th>Osc-ES</th>
</tr>
</thead>
<tbody>
<tr>
<td>First Publication</td>
<td>[HJ09]</td>
<td>[DGC11]</td>
<td>[WWR +14]</td>
<td>[GV11]</td>
<td>[TIK +12]</td>
<td>[Ska13]</td>
</tr>
<tr>
<td>Interruption Method</td>
<td>Counter voltage</td>
<td>Counter voltage</td>
<td>Current injection</td>
<td>Current injection</td>
<td>Current injection</td>
<td>Divergent oscillation</td>
</tr>
<tr>
<td>Switch</td>
<td>Disconnector</td>
<td>Disconnector</td>
<td>Disconnector</td>
<td>Interrupter</td>
<td>Interrupter</td>
<td>Interrupter</td>
</tr>
<tr>
<td>Simulated</td>
<td>Yes</td>
<td>Yes</td>
<td>Only MV</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Test Results</td>
<td>(80 \text{kV}, \ t_{CC} = 2 \text{ms}, \ i = 19 \text{kA})</td>
<td>(120 \text{kV}, \ t_{break} = 5 \text{ms}, \ i = 7 \text{kA})</td>
<td>(800 \text{V}, \ t_{CC} = 1 \text{ms}, \ i = 13 \text{kA})</td>
<td>(230 \text{V}, \ t_{break} = 10 \text{ms}, \ i = 10 \text{kA})</td>
<td>(i = 16 \text{kA})</td>
<td>No</td>
</tr>
<tr>
<td>Expected Advantages</td>
<td>Speed, (I_{max})</td>
<td>Speed, costs</td>
<td>Low losses</td>
<td>No losses, (I_{max})</td>
<td>Simple design and control</td>
<td>Simple design, (I_{max})</td>
</tr>
<tr>
<td>Expected Disadvantages</td>
<td>Control of semiconductors, costs</td>
<td>Resonance with grid, capacitor discharging</td>
<td>Capacitor size, complex design and control</td>
<td>speed, VI</td>
<td>(I_{max}, \ VI)</td>
<td>Stress on semiconductors</td>
</tr>
<tr>
<td>Expected Features</td>
<td>Pre-activation, current liming, O-C-O</td>
<td>Pre-activation</td>
<td>Pre-activation</td>
<td>Pre-activation</td>
<td>Pre-activation</td>
<td>Pre-activation</td>
</tr>
</tbody>
</table>
time, the interruption process is aborted, current is commutated back into the NCP and the breaker returns to normal operation. During this pre-activation phase, this circuit breaker furthermore has a current limiting functionality. These advantages come with the large array of turn-off semiconductors in the CCP, which is required to interrupt the full current and to block the TIV. Turn-off semiconductors are expected to be costly and to require precise simultaneous control for on-and off-switching [DGC11].

Layout and Operation

![Functional layout of LCS-MB (unidirectional)](image)

As illustrated in Figure 3.3, the LCS-MB has three parallel functional paths. The NCP is a series connection of a mechanical UFD and an LCS, rated for a voltage level sufficient to commutate the fault current into the CCP. The CCP consists of a turn-off semiconductor array called MB, which has full voltage blocking capability. In the EAP, MOVs are employed for the necessary energy dissipation.

In case of a fault breaking operation, the following steps are performed:

1. The LCS is turned off. When the current has fully commutated into the turned-on CCP, the UFD begins to open.

2. When the UFD has opened completely, the MB is turned off. The TIV builds up across the MB and the decreasing current is commutated into the EAP.

3. The remaining energy of the system is dissipated in the EAP and the fault current drops to the MOV leakage level, which can be switched off by a residual current switch subsequently.

A modular combination of the MB-semiconductors and the MOV is possible and bidirectional operation is achieved by expanding all semiconductor units with anti-parallel units in series [HJ11], which results in doubling the component costs except for the UFD.
3.2 Promising Concepts

According to [HJ11, HHJ14a, RSD∗14], the LCS-MB is projected for a nominal voltage of 320 kV and 2 kA nominal current. The maximum interruptible current ranges between 9 kV to 16 kV, given by the saturation current of the used semiconductors. The circuit breaker is designed to withstand a TIV of 480 kV, which corresponds to the clamping voltage level of the MOV in the EAP.

As turn-off semiconductors, 4.5 kV ABB StakPak IGBT or Bimode Insulated Gate Transistor (BIGT) modules [ABB13a] are employed in the LCS (3 × 3 modules per direction) and the MB (4 × 80 kV modules, each consisting of 40 IGBTs per direction). Adequate RCD snubber circuits protect the IGBTs against overvoltages. The mechanical opening time of the UFD to reach its full voltage withstand capability of 480 kV is 2 ms [DJSH14].

3.2.2. Circuit Breaker 2: LCS-C

The LCS-C applies the counter voltage method in combination with a mechanical disconnector in the NCPs. In difference to the LCS-MB’s turn-off semiconductor, turn-on semiconductors and capacitors are employed in the CCP. The concept was patented in 2011 [DGC11] and simulation as well as test results of components and a circuit breaker prototype have been published subsequently [CDN∗13, GP14, GDPV14].

The concept is analyzed in more detail, because its test results promise fast operation (2.4 ms from opening signal until TIV in a 120 kV prototype [GP14]). In contrast to earlier implementations of this principle [MKD05, Cra12], Dupraz et al. use multiple commutation paths in parallel, which are operated subsequently. The capacitors are not pre-charged and are rated for increasing voltage levels but with decreasing capacities. This design, which builds up the TIV in short time, is mainly rendered necessary by the \( \frac{di}{dt} \) and \( \frac{du}{dt} \) limits of the semiconductors [DGC11].

Advantages of the LCS-C concept are a high operation speed and relatively low costs, as it mainly employs turn-on semiconductors instead of the more expensive turn-off semiconductors. Similar to the LCS-MB, pre-activation is possible by directing the current flow through a varistor element in the first commutation branch.

Possible disadvantages include the time required to discharge the capacitors to reset the circuit breaker for operation as well as the risk of resonance between the CCPs and the grid inductances affecting the turn-off of the semiconductors.

Layout and Operation

Figure 3.4 shows the functional topology of the LCS-C circuit breaker. It consists of four parallel paths: The NCP, the Timing Branch and the Arming Branch, both CCPs, and the EAP. As for the LCS-MB, the NCP consists of a UFD and an LCS in series. In the Timing Branch a turn-on semiconductor unit TB is connected in series with two parallel sub-branches. Each of the two sub-branches consists of turn-on semiconductors (TB1 and TB2, respectively) and capacitors \( C_{TB1}, C_{TB2} \). The capacitor’s
voltage is limited by a metal-oxide varistor connected in parallel. The Arming Branch is a series connection of turn-off semiconductors AB and a capacitor $C_{AB}$, the EAP consists of MOVs.

The splitting of the Timing Branch allows the use of fewer semiconductor units and consequently reduces the branch resistances, which allows faster commutation compared to two fully independent branches equipped with semiconductors rated for the TIV. The voltage rating of the MOV in Timing Branch 1 is smaller than the rating of the MOV in the second timing.

In case of a fault, the breaker operates as follows to interrupt the current:

1. The LCS is turned off and TB and TB1 are turned on. The UFD begins to open as soon as the current commutated into Timing Branch 1.

2. After the UFD has opened, the current is commutated into Timing Branch 2 by turning TB2 on. TB1 switches off as soon as the current reverses since the voltage in $C_{TB1}$ is higher than on $C_{TB2}$.

3. When $C_{TB2}$ reaches a defined voltage level, AB is turned on to commutate the current into the Arming Branch.

4. The TIV is build up across $C_{AB}$ and the current commutates into the EAP.

5. The remaining energy of the system is dissipated in the EAP and the fault current drops to the MOV leakage level, which can be switched off by a residual current switch subsequently.
3.2 Promising Concepts

To ensure successful commutation between the branches and a fast operation, the capacitances must decrease from branch to branch with an increase of the voltage rating of the parallel connected MOVs.

To allow bipolar operation, the LCS and the turn-on semiconductors TB, TB1, TB2 and AB have to be extended with anti-parallel units in series, respectively, in parallel, which increases the investment costs by the semiconductor costs.

Published Information

The project’s publications [CDN+13, GP14] reported successful breaking operations of 5.2 kA to 7.7 kA within 5 ms to 8 ms using a 120 kV-prototype. In the LCS, IGBTs are used, whereas thyristors serve as the turn-on semiconductor units [GDPV14]. The UFD is air-insulated [CDN+13]. The patent [DGCI1] suggests a maximum voltage of 10% to 20% of the TIV on the Timing Branch 2 capacitor. Further information regarding the prospective rating or the dimensioning of components is not publicly available.

3.2.3. Breaker 3: Inj-C

The Inj-C circuit breaker concept applies the current injection method with a no-load mechanical disconnector. In [WWR+14] the concept is described and simulated for medium voltage and successful testing of a low voltage prototype is presented. The Inj-C concept is investigated in more detail because it uses a fast disconnector and solely turn-on semiconductors in combination with the current injection method, which promises fast and reliable operation and allows to be upscaled for use in HVDC grids.

As this concept in combines a mechanical disconnector with unidirectional semiconductors on the nominal current path, possible advantages are lower nominal conduction losses at similar operation times as the investigated counter voltage principles. Further more, the operation principle allows pre-activation.

On the other hand, the necessity to store the energy required for the current injection and the expected complexity of a bidirectional layout may be pitfalls of the technology.

Layout and Operation

As illustrated in Figure 3.5, the Inj-C consists of a NCP, two CCP which are bridged by a capacitor charged to a voltage $U_C$ and an EAP. The NCP consists of a UFD in series with unidirectional semiconductors. In the first parallel CCP, two turn-on semiconductor arrays T1 and T4 are connected in line. The second CCP connects the turn-on semiconductors T2 and T3 in a similar way, but with an individual inductor in series with each of the semiconductors. The capacitor bridges both CCP between the semiconductors. Initially, the capacitor is charged so that its positive pole is connected to the second CCP (T2, T3). In the EAP, an MOV stack is used for energy dissipation.
During the opening sequence, only three of the four possible CCP switch combination are in use:

1. T1 and T3 are turned on. The current is forced into the commutation branch by the negative voltage across the capacitor (T1-C-T3, first injection). D switches to blocking mode and the UFD begins to open.

2. T2 is turned on to prevent building up a large positive voltage across the capacitor and hence the NCP components. The current now solely flows through the second CCP (T2-T3).

3. When the UFD is opened, T4 is turned on (second injection). The current is commutated from T2-T3 to T2-C-T4. The capacitor voltage is reversed again and charged up to the TIV until the EAP takes over the current.

4. The remaining energy of the system is dissipated in the EAP and the fault current drops to the MOV leakage level, which can be switched off by a residual current switch subsequently.

To ensure that the semiconductors T1 to T4 are turned off in the correct sequence, the current injected by the charged capacitor has to be dimensioned properly for the prospective maximum fault current. The series connected inductors can be used for the tuning of the commutation process and are furthermore necessary to limit the rate of rise of current in the semiconductors.

For a bidirectional design, the unidirectional semiconductor D has to be replaced by two anti-parallel turn-on semiconductors, the number of turn-on semiconductors in the CCP has to be doubled since anti-parallel units are necessary.
3.2 Promising Concepts

Published Information

[WWR+14] describes the design and parameters of a simulation for a 10 kV unit, which achieved an interruption time of 2.5 ms, as well as of a tested 800 V prototype, which successfully interrupted a fault current of 13 kA within 1 ms, in detail. However, the capacitor was pre-charged to more than twice the testing voltage, which obviously is not suitable for HVDC applications. Hence, a re-dimensioning of the components was necessary.

3.2.4. Breaker 4: Inj-PG

The Inj-PG concept is a current injection - mechanical interrupter type breaker. Patented first in unidirectional configuration in 2011 [GV11], a subsequent patent [Mar11] and publications presented a bi-polar version and component test results [WM14] as well as it’s applicability in grids [WM13]. Following publications discussed its breaking performance [YB15] as well as the optimal design of its CCP [WM15] and its EAP [SL14].

This solution was selected for further investigation because its ground connection allows advantageous charging of the energy storing capacitor and because it is easy to extend to bidirectional operation.

Possible advantages of this circuit breaker are very low nominal conduction losses due to the absence of semiconductors in the NCP and the interruption of high fault currents. Due to its modular design, this circuit breaker topology can be adapted to a wide range of system voltages and fault currents.

Compared to no-load switch based solutions, this concept is expected to operate slower since the mechanical switch has to be optimized on current interruption behavior which comes at the cost of operation speed. Additionally, the interruption of relatively small fault currents may be problematic since the amplitude of the injected current is adapted to interrupt high currents. Hence the superposition of a small fault current and a large injected current lead to a high \( \frac{di}{dt} \) at current zero, which can be challenging for the mechanical circuit breaker. The latter problem may also occur in case of a fault close to the breakers terminal because of the chance of a weakly damped current injection via the ground connection and the fault. Further more, a successful application of series connected VIs in HVDC has not been presented yet.

Layout and Operation

As shown in Figure 3.6, the Inj-PG design has a fixed connection to ground and not all functional paths can simply be assigned to physical branches. The NCP consists of a mechanical interrupter unit (VI). The CCP consists of a pulse generator, connected between the first terminal of the interrupter and ground, a damping branch, which connects ground with the second interrupter terminal, and a unidirectional semiconductor in parallel to the interrupter, conducting in opposite direction to the nominal current (from terminal two to one). In series with the PG a unidirectional element


(conducting towards ground), and a resistor are connected. The PG itself consists of a capacitor, which initially is charged to the nominal voltage, with a turn-on semiconductor PG and an inductor connected in parallel. The DB consists of a resistive and a unidirectional element connected in series (conducting in the direction from ground to the nominal path). The EAP consists of the DB in combination with an MOV connected in parallel to the resistor and the PG.

In case of a fault, the following operation is performed by the circuit breaker:

1. The VI is opened, drawing an electric arc.

2. As soon as the VI is fully opened, PG is turned on, inducing a quick reversal of the capacitor voltage.

3. The voltage decrease and subsequent reversal leads to a current injection from the grounded terminal of the capacitor along the DB and the VI. The superposition of fault current and injected current results in a current zero crossing during which the VI can interrupt the arc.

4. While the injected current of the PG can continue to flow via the diode parallel to the VI, the TIV starts to build up since the PG capacitor is charged by the fault current.
5. Once the capacitor is charged up to the clamping voltage of the MOV, the current commutates to the varistor and the remaining energy is dissipated there.

The resistor in series with the capacitor is necessary to ensure the turn-off of the PG semiconductor after the pulse. In case of a bipolar configuration the DB should employ MOVs, in a monopolar configuration resistors can be used.

The extension to bidirectional operation requires a second VI with parallel diode as well as a second damping branch. To interrupt currents of the same magnitude as in unidirectional configuration, the pulse in the pulse generator has to be doubled or the resistance of the CCP has to be reduced accordingly.

**Published Information**

According to [WM14], the VI consists of series connected vacuum interrupters rated for 30 kV to 50 kV. The proposed pulse generator consists of a series connection of 30 kV PG modules with proportionally scaled components. Thyristors are used as the turn-on semiconductor devices, and the dimensions of all passive components are provided by [WM14]. Simulations of a 450 kV-version of this circuit breaker interrupting currents above 15 kA have been conducted. Additionally, tests proved that the PG thyristors can be operated at rates of rise of current of 3 kA µs⁻¹. Very recently, test results of a 230 V circuit breaker prototype have been presented [WM15].

### 3.2.5. Breaker 5: Inj-LC

The Inj-LC concept is one of the oldest [AC78, TSK+80] HVDC circuit breaker concepts and has been investigated in detail [YTI+82, AYT+85, AH01, EBH14]. Recent patents [TIK+12] and publications discuss its use for VSC-HVDC and its combination with fast mechanical interrupters [SJM+10, ZSJ+14, SZJ+15, TEK+15]. Many of the recent publications furthermore propose topologies, which pre-charge the capacitor to the grid voltage without having to use an external power source [TIK+12, SZJ+15, KCHM15].

The concept was selected for further evaluation because of the extensive test results and a recent publication stating its applicability for MTDC grids.

The advantages of the Inj-LC are its relatively simple design, avoiding the use of semiconductors, and the uncomplicated control. Furthermore, the concept allows pre-activation.

The fixed amplitude of the injected current and the relatively high frequency of the pulse [SZJ+15] can impede the extinguishing of the arc in the VIIs at smaller fault currents.

**Layout and Operation**

The Inj-LC circuit breaker consists of three parallel paths. In the NCP an interrupter unit VI is installed, which can interrupt under load. The CCP consists of a series connection of a capacitor, pre-charged to the nominal voltage, an inductor and a
switching device, which can be a TSG. In the EAP, MOV are employed. The Inj-LC interrupts a fault current in the following way:

1. The VI is signaled to open, drawing an arc between its contacts.

2. As soon as the VI contacts reached sufficient insulation distance, the TSG is triggered and a current pulse is injected into the NCP, creating a current zero crossing in the VI.

3. After arc extinction, the fault current is redirected into the CCP to build up the TIV on the capacitor.

4. Once the capacitor is charged up to the clamping voltage of the MOV, the current commutates to the EAP and the remaining energy is dissipated there.

Bidirectional operation of the Inj-LC circuit breaker is possible without additional components when using mechanical interrupters and switches. For a simple switch alignment, as proposed in [TIK +12], the capacitor is pre-charged to the system voltage in direction of the current when re-energizing the link after an interruption. Consequently, in case of a fault, the injected current is of similar direction as the fault current in the NCP during the first half wave. To avoid the resulting time delay after mechanical opening, the capacitor polarity has to be reversed before interruption, e.g. by using additional switches [KCHM15].

Published Information

Recent publications presented successful interruption of currents from 0.5 kA to 16 kA within 10 ms [TEK +15] as well as 10 kA within 10 ms at 80 kV [EBH14]. The dimensioning of the LC circuit is discussed and simulated in [SZJ +15], using a TSG in the CCP.
3.2.6. Breaker 6: Osc-ES

The Osc-ES concept applies the divergent oscillation method in combination with a mechanical switch capable to open under load. It was filed as a patent in 2010 [Ska13] and is a further development of an earlier concept [ALS94].

The concept was chosen for detailed analysis to investigate the potential of active divergent oscillation concepts, which may overcome the interruption speed limitations of passive versions of this principle.

Expected advantages of the design are the use of passive, reliable components in the CCP and the capability to interrupt a wide range of fault current amplitudes.

On the downside, the fast resonant switching might cause high stress on the turn-off semiconductors.

**Layout and Operation**

![Functional layout of Osc-ES (unidirectional)](image)

Figure 3.8: Functional layout of Osc-ES (unidirectional)

Figure 3.8 shows the functional layout of the Osc-ES circuit breaker concept. The circuit breaker consists of three parallel current paths. In the NCP, an interrupter array VI is connected in series with the Excitation Switch ES, consisting of turn-on semiconductors with an MOV in parallel. The CCP is a resonant LC circuit. In the EAP an MOV is connected in parallel to the NCP.

To successfully interrupt the fault current, the breaker performs the following steps:

1. The VI begins to open. The ES turns off, building up a voltage equivalent to the MOV’s clamping level. The resulting voltage drop across the CCP starts exciting the divergent oscillation.

2. When the current in the CCP crosses zero and changes its direction, opposing the fault current, the ES is turned on again.

3. By toggling the ES on and off in twice the LC circuit’s eigenfrequency at the current zero crossings, the amplitude of the oscillating current and voltage (each...
period by twice the ES voltage rating) increases linearly. If the oscillating current exceeds the fault current, the ES frequency can be adjusted to control the amplitude growth.

4. As soon as the VI is capable of preventing a re-ignition, the arc is extinguished after the next current zero crossing. The fault current is commutated into the capacitor, charging it up to the clamping voltage of the MOV.

5. The decreasing current is commutated into the EAP where the remaining energy of the system is dissipated in the MOV until the fault current drops to the specific leakage level. Subsequently, a residual current switch can isolate the link.

Published Information

The patent [Ska13] provides exemplary parameter values for a 320 kV circuit breakers.
4. Methods

In this chapter, the definitions and methods for the analysis of the six different circuit breaker concepts are presented. The first section explains the most important times during the breaking operation, which allows comparing the concepts’ speeds. The subsequent section describes how the individual circuit breakers are modeled. Section 4.3 presents the test circuits for the investigation of the circuit breaker’s interruption capabilities. In Section 4.4, the HVDC network, which is used to test the breakers’ applicability to an exemplary MTDC grid, is discussed.

4.1. Timing Definitions

In this section, the timing definitions, as proposed in a working paper by the Cigré Joint Working Group JWG A3/B4-34, are presented. The definitions were developed by the JWG A3/B4-34 to allow a comparison of the speed of circuit breaker operations independent of the circuit breaker’s topology or the components. For this reason, these definitions are adopted for this investigation.

In Figure 4.1, the timing definitions are shown in relation to typical circuit breaker current and voltage curves during a successful DC fault interruption. The interruption begins with the *fault inception*, the moment at which the fault causes the current through the circuit breaker to rise. If the circuit breaker features pre-activation, a *preliminary order* can be issued to start the interruption, however the irreversible part of the breaking operation is earliest initialized after the *trip order* is given by the protection control. The circuit breaker then completes its operation by building up a voltage exceeding the system voltage. At the instant this voltage intersects the system voltage, the *peak fault current* is reached. The voltage across the circuit breaker rises further, up to the *peak transient interruption voltage (TIV)*, forcing the fault current to decrease. In general the *peak TIV* is defined by the clamping voltage of the circuit breakers’ internal arrester which dissipates the remaining energy of the grid inductances. As soon as this energy is completely dissipated, the voltage across the circuit breaker drops to the system voltage. At this time, the *leakage current level is reached*. Only a small leakage current is flowing through the circuit breaker, which is primarily defined by the arrester design. A residual current switch can now chop the leakage current to provide a galvanic insulation of the faulted line.

Based on the explained time instances, various time durations, related to the circuit breaker operation, the protection scheme and to the system, have been defined. In the scope of this work, five of these timing definitions are recorded for each circuit breaker solution. These five definitions (1) capture the key steps and differences in operation
Figure 4.1.: Schematic circuit breaker voltage and current curves with corresponding timing definitions according to Cigré Working Paper JWG A3/B4-34
4.1 Timing Definitions

of the breakers and (2) allow the calculation of most other defined times:

**Breaker operation time** The *breaker operation time* is measured between the breaker receiving the *trip order* and the beginning of the TIV. The beginning of the TIV is defined as the moment of zero crossing of the TIV secant, which connects the points in time where the TIV reaches 20 % and 80 % of its maximum value. The *breaker operation time* represents the time the breaker needs for internal commutation processes up to the last stage and can be an indicator for the complexity of the breaker operation.

**Voltage rise time** The *voltage rise time* is defined by the time difference between the TIV secant crossing zero and reaching the maximum TIV value. The TIV secant is defined by the 20 % and 80 % points of the TIV. The *voltage rise time* is critical when mechanical interrupters or semiconductors are employed to withstand the TIV as their blocking capability and the risk of a breakdown depend on the rate of rise of voltage immediately after interruption.

**Relay time** The time interval between *fault inception* and the breaker receiving the *trip signal* is the *relay time*. In case of preliminary orders, e.g. circuit breaker pre-activation, the *relay time* is composed of the detection time and the selection time. In the simulations performed in this work, no preliminary orders are given and therefore the relay time equals the detection time. The fault inception describes the moment at which the fault arrives at the circuit breaker and is therefore independent of the fault location and line parameters. As the modelled protection schemes do not include further delays or selection processes, the *relay time* is not distinguished further but serves as an indicator for the speed of the detection and protection scheme in use.

**Fault neutralization time** The *fault neutralization time* describes the time from the *fault inception* until the *peak fault current*\(^1\) is reached. This time period is relevant from a system perspective. The healthy part of the system can start to recover after the *fault neutralization time*, as the voltage at the circuit breakers healthy terminal is back at the nominal level.

**Break time** The *break time* is measured from the *trip order* until the *leakage current level is reached*. In the scope of this work, the first time instance of the fault current falling below the nominal leakage current level defines the end of the *break time*, assuming a residual current switch can open at this moment. Consequently, the *break time* describes the time after which the fault stops affecting the operation of the system’s healthy part.

\(^1\)In the grid study, the fault neutralization time is measured until the *TIV peak*, which in general is close to the peak fault current. This is necessary because grid induced oscillations hinder a clear identification of the peak fault current.
4.2. Modelling of HVDC Circuit Breakers

To provide a fair comparison of the different concepts, all circuit breakers are modeled using the same component models and according to the same design and control rules. The components are based on the PSCAD standard library and extended either with datasheet parameters of commercially available products or published prototype results. In this section, the modeling rules and different components as well as their parameters are presented in the following order: (1) general breaker modeling, (2) mechanical switches, (3) semiconductor devices, (4) passive elements, (5) parasitic elements.

4.2.1. General Breaker Modelling

As this work investigates the applicability of circuit breaker concepts for MTDC networks, the following main rules apply for the developed models:

- The circuit breaker models are primarily optimized to achieve the fastest possible fault neutralization time in the defined nominal fault case, because this time is the most critical requirement for HVDC circuit breakers in an MTDC network [TEK+15].
- The circuit breakers are modeled for bidirectional operation. As many circuit breakers in an MTDC network will have to offer this capability, the investigated circuit breakers have to fulfill this requirement too.

The nominal fault case is defined in Section 4.3.

4.2.2. Mechanical Switches

Regarding mechanical switches, only two different models are implemented, one switch that can open under load and one switch that can only open during zero current: (1) The Ultra-Fast Disconnector (UFD) and (2) a series connection of 8 vacuum interrupters (VIs) with high speed opening mechanisms. Table 4.1 summarizes the implementation of the models, as described in the following two sections.

**UFD Model**

The UFD model is based on the gas insulated disconnector as described in [SOK+11, DJSH14]. It is rated for a nominal voltage of 320 kV DC and a nominal current of 2.6 kA. The time delay from trip signal to dielectric insulation (above 1.5 times the rated voltage) is lower than 2 ms [DJSH14].

The open- and close-state resistance of the UFD are idealized as the nominal resistance of mechanical switches is negligibly small. For simulation purposes, a finite resistance in the open-state has to be set \( R_{\text{open}} = 1 \Omega \). When the signal to open the UFD is given, an opening time delay of 2 ms starts after
4.2 Modelling of HVDC Circuit Breakers

<table>
<thead>
<tr>
<th>Table 4.1.: Mechanical switch models</th>
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<tbody>
<tr>
<td><strong>Ultra-fast disconnector (UFD)</strong></td>
</tr>
<tr>
<td>Rated voltage</td>
</tr>
<tr>
<td>Rated nominal current</td>
</tr>
<tr>
<td>( R_{\text{closed}} / R_{\text{open}} )</td>
</tr>
<tr>
<td>Opening time</td>
</tr>
<tr>
<td>Opening condition</td>
</tr>
<tr>
<td>Breaking condition</td>
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the current through the UFD decreased below 1 A to ensure that the disconnector is not operated under load conditions. After the time delay has passed, the simulated switch immediately changes its resistance from \( R_{\text{closed}} \) to \( R_{\text{open}} \), with the prerequisite that the current is below the limit of 1 A. Implementing a variable resistance in series with the breaker which increases proportional to the contact distance during opening was considered initially, but first simulations suggested that the above described model is sufficient.

**VI Model**

The implemented VI model is based on the datasheet of a commercially available 40.5 kV vacuum interrupter [Eat11]. It is assumed that the voltage is shared equally between the breakers, which are operated by an ultra-fast drive as proposed in [ZSJ+14]. A medium voltage VI has approximately a DC blocking capability of twice its rated AC voltage [Int08]. However, with respect to the high rate of rise of the TIV across the vacuum interrupter terminals, eight 40.5 kV VIs are connected in series in the VI model. The rated nominal current is 2 kA [Eat11] and the opening time is set to 2.5 ms, a value which has already been archived under laboratory conditions using a standard 40.5 kV VI [WHD+15].

The open- and close-state resistance of the VIs are assumed to be the same as for the UFD.

When the breaker is signaled to open, a series connected voltage source, representing the vacuum arcs between the VIs’ opening contacts, is activated. The voltage of the vacuum arc is assumed to be constant [Sla08] and is set to conservative 30 V per VI in direction of the current flow (in total 240 V) [WLR08]. When the opening time of 2.5 ms has passed and the current through the breaker falls below the chopping limit of 1 A [WLR08], the interrupter resistance switches immediately to \( R_{\text{open}} \).

**Interruption capability of vacuum interrupters** Even though the interruption capability of VIs has been analyzed in detail [Sla08, SAA+11, SFB+14], few information is available on their performance in DC applications [AC78], especially when connected in series and when using very fast opening mechanisms [SAA+11].
Experimental investigations have proven that a successful interruption is to a very high extent determined by the rate of rise of the current shortly before current zero crossing \( \frac{\mathrm{d}I}{\mathrm{d}t} \) and the subsequent rate of rise of the transient voltage \( \frac{\mathrm{d}U_{\text{TRV}}}{\mathrm{d}t} \) across the interrupter’s contacts [YTI+82, Pre82, PPS99, HHJ+14b] as well as by the arcing time [NYF+06] and the design of the VI, especially its contacts [PHH15].

For a VI’s interruption performance, [Gre94] suggests as a conservative rule of thumb of
\[
\frac{\mathrm{d}U_{\text{TRV}}}{\mathrm{d}t} \cdot \frac{\mathrm{d}I}{\mathrm{d}t} = \varepsilon.
\]
Depending on the VI’s design, \( \varepsilon \) can be found in the range of 14 kVA/\( \mu \)s\(^2\) to 140 kVA/\( \mu \)s\(^2\) [Sla08, p. 404-405].

In this thesis, a closer look is taken at the circuit breakers’ interruption capabilities, limited by the rate of rise of current and voltage in the vacuum interrupters in the nominal fault case, based on this aforementioned approximation.

### 4.2.3. Semiconductors

According to the requirements of the investigated concepts, three different types of semiconductors are implemented: (1) IGBT with anti-parallel diode as turn-off semiconductor, (2) thyristor as turn-on semiconductor and (3) diode as rectifying element. Each of the three semiconductor models is based on the datasheet of a commercially available product. For the selection of the respective datasheet, the information of different manufacturers were compared and the most advantageous device, fulfilling all requirements for the different breaker concepts, was chosen. Table 4.2 provides an overview of the parameters of these three models, which are used for realistic modeling of the semiconductor components using the standard PSCAD power electronic switch model. To allow a simple implementation of multiple units connected in series and/or parallel and do reduce the runtime computation effort, the power electronic switch model is modified accordingly.

In the scope of this thesis, the minimum necessary number of series connected devices that have to block a specific voltage \( \hat{U}_{\text{stack}} \) is set to
\[
n_{\text{ser}} = \frac{\hat{U}_{\text{stack}}}{1.5 \hat{U}_{\text{unit}}} \text{ to provide a 50% redundancy margin for all semiconductor devices [HIJ14a].}
\]

Even though on-line monitoring of the currents and voltages in the semiconductor devices is implemented, the identification of possible violations of the \( I, \frac{\mathrm{d}I}{\mathrm{d}t} \) and \( \frac{\mathrm{d}I}{\mathrm{d}t} \) limits of the devices has to be performed manually as the PSCAD model lacks this feature.2

**IGBT**

As IGBT, the ABB 4.5 kV Stakpak IGBT 5SNA 2000K450300 with integrated anti-parallel diode [ABB13a] was selected, because of its overall performance, low losses and its design which eases compact series mounting.

The data for both PSCAD pes-switch models, IGBT and anti-parallel diode, is taken

\footnote{According to the PSCAD On-Line Help System, the derivative “block is fraught with danger because of its tendency to amplify noise”. Over-proportional high peaks are observed at moments when the semiconductor switches between blocking and conducting state because of the simulation stepwidth, which have to be judged manually.}
4.2 Modelling of HVDC Circuit Breakers

Table 4.2.: Semiconductor models, values per semiconductor unit

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<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>$\hat{U}$</td>
<td>4.5 kV</td>
<td>9.6 kV</td>
<td>5 kV</td>
</tr>
<tr>
<td>$I_N$</td>
<td>2 kA</td>
<td>2.36 kA</td>
<td>9.1 kA</td>
</tr>
<tr>
<td>$I_{\text{surge}}$</td>
<td>32 kA</td>
<td>28 kA</td>
<td>110 kA</td>
</tr>
<tr>
<td>$dI/dt$</td>
<td>N/A / 4 kA $\mu$s$^{-1}$</td>
<td>3 kA $\mu$s$^{-1}$</td>
<td>N/A (100 A $\mu$s$^{-1}$)</td>
</tr>
<tr>
<td>$dU/dt$</td>
<td>N/A</td>
<td>2 kV $\mu$s$^{-1}$</td>
<td>N/A</td>
</tr>
<tr>
<td>$U_{\text{fwd}}$</td>
<td>1.7 V / 1.5 V</td>
<td>0.7 V</td>
<td>0.63 V</td>
</tr>
<tr>
<td>$r_{\text{on}}$</td>
<td>0.85 m$\Omega$ / 4 m$\Omega$</td>
<td>0.95 m$\Omega$</td>
<td>0.087 m$\Omega$</td>
</tr>
<tr>
<td>$R_{\text{off}}$</td>
<td>1 T$\Omega$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

from the product datasheet. The maximum forward blocking and reverse voltage is set to the Stakpak’s rating of 4.5 kV. The on-state resistance and the forward voltage drop when conducting are adopted from the characteristic chip-level curves at 2 kA and 125°C (IGBT: $U_{\text{fwd}} = 1.7$ V, $r_{\text{on}} = 0.85$ m$\Omega$; Diode: $U_{\text{fwd}} = 1.5$ V, $r_{\text{on}} = 0.4$ m$\Omega$). Even though the datasheet does not provide clear maximum $\frac{di}{dt}$ or $\frac{du}{dt}$, $\frac{di}{dt} < 4$ kA $\mu$s$^{-1}$ is given as a maximum value for the provided safe operating area of the diode.

To ease the detection of high $\frac{di}{dt}$ or $\frac{du}{dt}$ values in the IGBT significantly exceeding these 4 kA $\mu$s$^{-1}$, a second PSCAD model is developed. It provides on-line calculation and plotting of the respective values both in the IGBT stack and per semiconductor, under the assumption of ideal voltage and current sharing.

**Thyristor**

The Mitsubishi General Use Thyristor FT1500AU-240 is chosen as representative turn-on semiconductor device because of its high off-state voltage rating 9.6 kV and nominal current 2.36 kA$_{\text{rms}}$, the favorable forward characteristics ($U_{\text{fwd}} = 0.7$ V, $r_{\text{on}} = 0.95$ m$\Omega$) normalized to the blocking capability and for the detail of information published.

The $\frac{di}{dt}$ (100 A $\mu$s$^{-1}$) and $\frac{du}{dt}$ limitation (2 kV $\mu$s$^{-1}$) are typical for its class. However, as discussed in [WM13], higher rates of rise of current, up to 3 kA $\mu$s$^{-1}$, can be achieved with adequate snubber circuits. For this reason, the thyristor model allows an RC snubber circuit. The proposed equivalent snubber circuit for a stack of 75 units, capable of blocking $1.5 \cdot U_N = 480$ kV, is set to the PSCAD default values of 5 k$\Omega$/5 m$\mu$F for 75 units. By changing the number of series-connected units, the snubber is automatically scaled proportionally to provide voltage grading along different arrays.
Diode

Compared to its competitors, the Infineon Rectifier Diode D6001N [Inf14] provides a low threshold voltage and slope resistance $U_{fwd} = 0.63 \text{V}$, $r_{on} = 0.087 \text{m}\Omega$ at high reverse blocking voltage of $5 \text{kV}$. As in all investigated circuit breaker concepts in bidirectional design, the diodes only have to carry current for short times, the nominal current rating of (6 kA) is irrelevant, and the surge current limit of $I_{surge} = 110 \text{kA}$ provides sufficient margin.

As for the IGBT and the thyristor, the simple diode model allows series connection of multiple devices, assuming equal voltage sharing, and the extended model provides on-line monitoring of $\frac{dI}{dt}$ and $\frac{dU}{dt}$ as well. The nominal $\frac{dI}{dt}$ for the peak reverse recovery current is $-10 \text{A}\mu\text{s}^{-1}$, which will be used as a guideline.

4.2.4. Passive Elements

Passive circuit breaker components, resistors, capacitors and inductors, are assumed to be ideal and individual parasitic effects of these elements are neglected. Resistors are available at any size required, whereas the variation of inductor and capacitor ratings is varied in tens of microhenry and in microfarad as a conservative estimate due to the lack of information regarding the sizes of available high power HVDC products. In the circuit breaker models, where multiple identical components are combined into a single one (to reduce the computation effort) or where a topology is down- or upscaled from another voltage level, exceptions are made, to maintain the functionality of the concept.

Varistor

For the varistors employed in all the analyzed concepts, the standard PSCAD MOV model is used. Its $U-I$-characteristic, as shown in Figure 4.2, is based on the ASEA XAP-A.

The energy absorbing path MOV rating is set to achieve a clamping voltage$^3$ of $1.5 \cdot U_N = 480 \text{kV}$ as proposed in most of the investigated HVDC circuit breaker concepts [SR14].

This rating results in a relatively high leakage current of $5.2 \text{A}$ at $320 \text{kV}$. However, this does not impose a problem since it is a realistic value to be interrupted by a residual current switch and both measurement of the break time (Figure 4.1) as well as triggering of the residual current switches are adjusted accordingly so that no negative effects arise.

As the energy absorption is almost exclusively defined by the MOV rating and characteristic, the energy stored in the system and the peak fault current, it is the circuit breakers speed (fault neutralization time), but not its topology, that directly influences

$^3$In the investigated default fault case (Section 4.3) the clamping level approximately requires $I_{MOV} > 10 \text{kA}$
4.2 Modelling of HVDC Circuit Breakers

Figure 4.2.: U-I characteristic of the MOV model (ASEA XAP-A) employed on the EAP. The nominal voltage (320 kV) and the clamping voltage (480 kV) are indicated by the dashed lines.

The absorption process [SL14]. For an investigation with focus on the energy absorption process, a more sophisticated MOV model should be implemented to achieve the same clamping level and a lower residual leakage current at the same time, e.g. by increasing the rating of MOVs while connecting several units in parallel.

4.2.5. Parasitic Elements

The circuit breakers operate at voltages in the range of hundreds of kilovolts and consequently large or many series connected components and long connectors are required to fulfill the insulation requirements. By assuming a stray inductance of 50 µH per commutation branch, an attempt is made to account for the parasitic inductance of these components and induced commutation delays. This fix approximation is chosen based on discussion with experts and literature [Tho99, AH01, Cre13, AAM+15, CCBS15]. This work does not account for stray capacitance in parallel to mechanical switches and MOVs for two reasons: (1) Their effect is expected to be marginal for both mechanical switches and MOVs with a similar induced charging delay for all concepts as well as because (2) the few data available [SJM+10] is insufficient for an educated estimate.
4.2.6. Residual Current Switch

To facilitate the detection of the instant when the leakage current level is reached for the first time, a second circuit breaker model, equipped with a residual current switch in series, is available for each of the breakers. This model is only required for precise detection in the system study (Section 4.4), where subsequent oscillations due to the converter control and system design can occur.

The residual current switch is modeled using the standard PSCAD breaker model, with the chopping limit set to the leakage current level through the opened breaker at nominal voltage. It is signaled immediately after the breaker operation is completed and opens without additional delay as soon as its current falls below the chopping limit.

For a complete investigation, especially of the post-fault stabilization and the practical requirements for residual current switches, the MTDC network is simulated with the circuit breaker models without the residual current switch.

4.3. Simple HVDC Circuit for Breaker Analysis

![Diagram of the simple HVDC circuit for breaker analysis](image)

**Figure 4.3.:** Topology of the simple HVDC circuit for breaker analysis

To (1) verify the analytically derived breaker operation, (2) optimize the circuit breaker dimensioning and (3) investigate the circuit breaker’s operation range and parameter sensitivity for individual concepts, the different circuit breakers are simulated in a simple HVDC circuit. The circuit, illustrated in Figure 4.3, consists of a series connection of an ideal DC source $U_N$, a current limiting reactor $L$, the circuit breaker and a selectable resistor, which can be switched from nominal resistance $R_N = \frac{U_N}{I_N}$ to fault resistance $R_F$.

The nominal voltage and current as well as the current limiting reactor, as listed in Table 4.3, are selected to match the most common of the projected ratings of the selected circuit breakers. The voltage and current level furthermore correspond to the
maximum ratings of the latest generation of installed HVDC cables. As a consequence, all components in the circuit breakers’ NCPs are required to have at least a continuous current carrying capability of this rating and are selected accordingly. The fault resistance is set to a small value to provide an approximately linear rate of rise of the fault current \( \left( \frac{dI_F}{dt} \approx \frac{U_N}{L} \right) \) for all the circuit breakers independent of their speed. In a real grid the current converges towards a maximum value, but as this current slope is highly dependent on the grid parameters [BWAF14], a non-decreasing rate of rise of the fault current is essential to analyze the maximum current breaking capabilities of the circuit breakers.

**Table 4.3.:** Parameters of the simple HVDC circuit for breaker analysis

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( U_N )</td>
<td>320 kV</td>
</tr>
<tr>
<td>( I_N )</td>
<td>2 kA</td>
</tr>
<tr>
<td>L</td>
<td>100 mH</td>
</tr>
<tr>
<td>( R_N )</td>
<td>160 ( \Omega )</td>
</tr>
<tr>
<td>( R_F )</td>
<td>0.01 ( \Omega )</td>
</tr>
</tbody>
</table>

**Circuit Operation Sequence**

To simulate the fault interruption, the HVDC circuit is operated in the following sequence:

1. The current limiting reactor \( L \) and capacitors as well as inductors belonging to the respective circuit breaker are energized until the grid reaches a steady state.

2. After 40 ms, the load resistance is switched from the nominal to the fault resistance.

3. The circuit breaker is signaled to trip when the current through the circuit breaker exceeds \( 1.2 \times I_N = 2.4 \text{ kA} \) [HHJ14a].

4. The simulation continues for 60 ms and the fault interruption behavior of the circuit breaker is calculated.

The values mentioned above constitute the standard parameter set, any changes are indicated. Due to the constant rate of rise of current, the fault detection equals to a relay time of 0.125 ms, as defined in Section 4.1. This short time delay can only be realized with a local fault detection scheme [SR14], a non-local detection scheme would experience a propagation delay of several milliseconds, depending on the length and type of the line [BWAF14,LH15]. The HVDC circuit detection threshold functions are (1) to simulate a simplified but realistic fault case and (2) to ensure consistent triggering of the circuit breaker, irrespective of possible transient responses, which
depend on the grid and circuit breaker topology that may vary considerably, to the
fault inception by the individual circuit breakers, to allow precise time measurements.
In addition to the above described operation sequence, the HVDC circuit features
multiple runs in series with variation of e.g. the series reactor or the nominal current
to analyze the sensitivity of the circuit breakers for varying fault cases.

Measurements
In the simple HVDC circuit simulation, four different measurements are conducted
with a simulation stepwidth of 0.5 µs: (1) The voltages on both sides of the circuit
breaker. (2) The current flowing through the circuit breaker, (3) the times, as defined
in Section 4.1 and (4) the stresses on the circuit breakers’ paths and components in
terms of voltages and currents.
Furthermore, several other parameters for the circuit breaker analysis are evaluated
during the simulation, based on the measurements mentioned above, such as the volt-
age across the breaker $U_{CB} = U_{in} - U_{out}$ or the power loss in the breaker during normal
operation $P_L = I_N \cdot U_{CB}$.

Sensitivity Analysis
For all investigated circuit breaker models, several parameters are varied to identify
the circuit breakers’ sensitivity: (1) Based on the interruption results, the margins for
a higher trip signal current level or a higher linear rate of rise of the fault currents
are calculated, each with the other parameter kept constant (2) Three different trip
signal current levels are simulated, 1.2 kA, 2.9 kA and 3.6 kA, approximately −50 %,
+20 % and +50 % compared to the nominal fault case. (3) The circuit breaker is re-
dimensioned to successfully interrupt a fault current 1 kA larger than the maximum
interruptible current of its default dimensioning (4) The opening time of the mechanical
switch is reduced by 20 % and the circuit breaker is re-dimensioned for optimal
speed in the nominal fault case. (5) Other variables with significant influence on the
circuit breaker speed are identified and the circuit breakers sensitivity is at least
theoretically investigated for changes in this variable.

4.4. Multi-Terminal HVDC Grid
Subsequent to the circuit breaker performance analysis in the HVDC circuit described
in the previous Section 4.3, the circuit breaker concepts are simulated in an examplary
meshed multi-terminal HVDC grid to evaluate their performance for different
fault cases. These simulations may serve as a possible reference case to identify grid
dependent effects that are not included in the simpler fault model, presented in the
previous section. However, due to the variety of possible grid topologies, the presented
grid study is by no means considered exhaustive.
Several MTDC topologies, suitable for the investigation of circuit breakers, have al-
ready been published [Buc14,YB15,LAB+15]. Because of the quality of these previous
4.4 Multi-Terminal HVDC Grid

Figure 4.4.: The four-terminal HVDC grid, as proposed in [LAB+15], single line diagram

publications, this work omits the development of a new grid topology but adopts the MTDC design by [LAB+15]. The proposed grid is chosen over the other mentioned publications, because it combines some of their strengths, as listed in the following, and furthermore the PSCAD simulation model of the grid is published in full detail.

- The implemented converter model simulates state of the art technology (Modular Multi-Level Converter).
- The system is designed for bipolar operation, which allows the investigation of the more severe pole-to-pole fault and the testing of bipolar circuit breaker design and control.
- The MTDC grid is relatively small, which makes it suitable for parameter studies and allows the reproduction of results with an academic PSCAD license.

In the following sections, (1) the grid topology, (2) the converter station, (3) cable model as well as (4) the protection scheme, (5) the investigated fault cases and (6) the conducted measurements are described.

4.4.1. Topology of the MTDC Grid

Figure 4.4 illustrates the topology of the MTDC grid presented [LAB+15]. It consists of four Modular Multi-Level Converter stations, as summarized in Table 4.4, which are connected by five cables. The grid is operated in a bipolar configuration at a nominal voltage of ±320 kV. Two of the converter stations, converter 1 and converter 2, operate as rectifiers connected to offshore wind parks. Each of the two rectifiers feeds 700 MW active and 100 MVAr reactive power into the grid. These power set-points
Table 4.4.: Converter Stations in the MTDC

<table>
<thead>
<tr>
<th>Converter</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$U_N$</td>
<td>±320 kV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mode</td>
<td>Inverter</td>
<td>Inverter</td>
<td>Rectifier</td>
<td>Rectifier</td>
</tr>
<tr>
<td>Set-Points</td>
<td>$P$</td>
<td>$-700, \text{MW}$</td>
<td>$-700, \text{MW}$</td>
<td>$800, \text{MW}$</td>
</tr>
<tr>
<td></td>
<td>$Q$</td>
<td>$100, \text{MVAr}$</td>
<td>$100, \text{MVAr}$</td>
<td>$100, \text{MVAr}$</td>
</tr>
<tr>
<td></td>
<td>% of $S_r$</td>
<td>$79%$</td>
<td>$79%$</td>
<td>$90%$</td>
</tr>
<tr>
<td>Gains</td>
<td>$K_p / K_i (P)$</td>
<td>$0.0001 / 0.01$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$K_p / K_i (Q)$</td>
<td>$-0.0001 / -0.03$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Droop</td>
<td>0</td>
<td>0</td>
<td>20</td>
<td>20</td>
</tr>
</tbody>
</table>

The cables “12” (100 km), “13” (200 km), “34” (100 km) length and “24” (150 km) interconnect the four stations in a ring configuration, the additional cross-link “14” of 200 km connects converter 1 with converter 4. At both ends of each cable, a circuit breaker and a current limiting reactor of 100 mH are connected to allow selective fault clearing and to limit the rate of rise of fault currents.

4.4.2. Converter Station Model

On the AC side, the converter station is connected to the AC grid via a YD (voltages) transformer. On the DC side, small 2.5 µF capacitors are connected between each pole and ground and all four converters have a low ohmic midpoint grounding. The possible contributions of these two parameters to the fault current in a pole-to-ground fault are investigated in detail in [BWAF14], chapters 5 and 8, which is why they are not further investigated in this work.

To avoid modeling the large number semiconductor switches used in an MMC, a continuous converter model with an equivalent branch for each of the six converter arms is implemented [AAM+15]. The equivalent branches, built up by a voltage source, an inductor and a resistor in series, thereby represent the instantaneously inserted voltage of each converter arm. The available energy, stored on each of the arms capacitors, is estimated using the measured AC currents and the desired AC voltages.
4.4 Multi-Terminal HVDC Grid

Table 4.5.: Current control in MTDC converter stations

<table>
<thead>
<tr>
<th>Variable</th>
<th>Set-point</th>
<th>P gain</th>
<th>I gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{d+}$</td>
<td>f(U/P)</td>
<td>500</td>
<td>1000</td>
</tr>
<tr>
<td>$I_{q+}$</td>
<td>f(Q)</td>
<td>500</td>
<td>1000</td>
</tr>
<tr>
<td>$I_{d-}$</td>
<td>0</td>
<td>500</td>
<td>1000</td>
</tr>
<tr>
<td>$I_{q-}$</td>
<td>0</td>
<td>500</td>
<td>1000</td>
</tr>
</tbody>
</table>

Table 4.6.: MTDC cable parameters [LAB$^+15$]. The inner Semiconducting Layer is 1.7 mm, the outer 1.9 mm thick

<table>
<thead>
<tr>
<th></th>
<th>$r$ [mm]</th>
<th>$\rho$ [$\Omega$ m]</th>
<th>$\epsilon_{rel}$</th>
<th>$\mu_{rel}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conductor</td>
<td>19.5</td>
<td>1.7 $\cdot 10^{-8}$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Insulator 1</td>
<td>46.8</td>
<td>2.3</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Sheath</td>
<td>51.7</td>
<td>2.2 $\cdot 10^{-7}$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Insulator 2</td>
<td>54.7</td>
<td>2.3</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Armour</td>
<td>58.7</td>
<td>1.8 $\cdot 10^{-7}$</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>Insulator 3</td>
<td>63.7</td>
<td>2.3</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Inner Control

Based on the active power, reactive power and voltage (droop) set-points of the four converters, the positive sequence current reference values for the inner control are calculated. Furthermore, the inner converter control allows set-points for the negative sequence control and the adjustment of the PI-controllers for all these set-points. The PI-controllers as well as the negative sequence current set-point are set to identical values for all converter stations. Set-points and the control gains, are listed in Table 4.4 and Table 4.5, and are adopted from [LAB$^+15$] after the correction of one inconsistent set-point.

Figure 4.5 illustrates the high level control as implemented. Based on the outer and inner control, two different sets of phase voltages and currents are calculated. For the first set, which is solely based on the outer control parameters, all voltages, respectively, all currents, are equal. For the second set, the values for each phases are individually calculated by additionally using the negative sequence current control. For the first 0.1 s, during which the grid is energized, the first of the two sets is used. When the grid has reached a steady state, the sequence control selector switches to the second set and activates the more elaborate and sensitive control scheme.

The implemented converter model is also capable of simulating the blocked-mode operation. Anyhow, to allow some generalization of the results and to avoid converter control specific reactions of the grid, this option was disabled.
Figure 4.5.: Schematic illustration of the high level converter control

Figure 4.6.: Cross-section of the XLPE insulated cable link
4.4.3. Cable Model

In the used MTDC network, PSCAD’s frequency-dependent distributed parameter cable model is used, as proposed by [LAB+15]. This model provides the most detailed description of the cable parameters, accounts for its transient behavior and the mode propagation of traveling waves as well as their reflections at both converter terminals and faults [BWAF14].

The parameters, as listed in 4.6, are representative for 320 kV XLPE insulated HVDC cables [LAB+15]. The two cables per link are assumed to be laid 1 m under ground in wet soil and with a mid-point distance of 1 m. The ground return resistivity is modeled with $1 \Omega \cdot m$. The cross-section of the cables is shown in Figure 4.6.

The cable parameters result in a surge impedance of $33.73 \Omega$ and a propagation velocity of $183.5 \text{ km} \cdot \mu \text{s}^{-1}$ [LAB+15].

4.4.4. Protection Control and Circuit Breakers

The MTDC grid is protected against DC faults by circuit breakers installed at all cable ends. This configuration allows selective insulation of a fault and consequently maintaining operation of the healthy parts of the grid.

To detect a fault, a local detection scheme is implemented for each pair of circuit breakers at the end of a cable. The local detection measures the voltage and current at the converter side terminal of the circuit breaker between the current limiting reactor and the breaker. A trip signal is send to the circuit breakers at both poles simultaneously when two conditions are fulfilled at the same time: (1) The absolute value of the current through the circuit breaker must exceed $1.6 \text{ kA}$ and remain above $1.2 \text{ kA}$ or (2) the absolute voltage to ground at one of the two poles must drop below $32 \text{ kV}$ and remain below $100 \text{ kV}$ due to the incoming voltage wave and its reflection at the current limiting reactor. The threshold limits for current and voltage correspond to twice, respectively 10% of the steady state values.

For all three investigated fault cases, which are presented in the next section, none of the circuit breakers in the non-faulted lines have been activated after a successful opening of the circuit breakers adjacent to the fault. Based on this observation, all unaffected protection controls and circuit breakers are deleted to reduce the simulation effort and the fault detection for the remaining line is simplified to already trigger the circuit breaker when one of the two described criteria is fulfilled.

Furthermore, the complexity of the circuit breaker models is reduced by (1) omitting submodules but modeling the circuit breaker on one single layer, (2) by removing protective components (such as surge arresters in parallel to semiconductor stacks) or by replacing them with linear components and (3) by reducing the number of circuit breaker internal meters significantly. All these simplifications do not affect the circuit breakers’ operation or capabilities in the investigated cases, this was verified by simulation in both the HVDC circuit and in the MTDC grid.
4.4.5. Investigated Fault Cases

Because the voltage amplitude is twice as high, the fault currents in pole-to-pole faults are considerably higher than pole-to-ground faults in bipolar MTDC [LAB+15]. For this reason, this work focuses only on three different pole-to-pole fault scenarios and neglects pole-to-ground faults. A more detailed investigation of the impact of different fault types exceeds the scope of this thesis.

All three faults occur on link “13”, which has the highest pre-fault steady state current. Fault 1 occurs in the middle of the link, 100 km from each bus, fault 2 is 25 km away from bus 1 and fault 3 is a pole-to-pole fault, directly at the terminal of the circuit breakers at bus 1. The short circuit resistance of the fault is assumed to be 0.01 $\Omega$ in all simulated cases.

Even though [LAB+15] already identified fault 3, at the circuit breaker terminal, as the most severe of the three fault cases, all of them are investigated for two reasons: First, faults 1 and 2 promise stronger effects of the traveling waves which are reflected at the current limiting reactors [SR14, CCB+15]. Possible effects of the resulting oscillation on the rate of rise of current and hence the circuit breaker operation are to be investigated. Second, by comparing the performance of each circuit breaker and its impact on the grid in the three different fault types, the sensitivity of the fault protection and clearing to the fault location can be investigated.

4.4.6. Measurement

The critical values, which are metered in every fault case with all circuit breakers with a simulation stepwidth of 2$\mu$s, are:

- The pole-to-pole voltage at bus 1 and bus 3, as these voltages strongly affect the converter control.

- The currents in the faulted cables and the adjacent cables for both polarities, as these currents are metered by the protection scheme.

- The current in the circuit breakers’ functional paths, as an indicator of the stress on the circuit breakers components in comparison the HVDC circuit for analysis.

- The voltage across the breaker, necessary for the time measurement.

- The relay time, the fault neutralization time and the break time (Figure 4.1), as key indicators for the circuit breakers operation speed.

To minimize the computation effort, all other additional measurement such as the circuit breaker internal $\frac{dI}{dt}$ monitoring, the voltage at bus 2 and 4 or the in-fed power, are only metered selectively for special cases.
5. Analysis of HVDC Circuit Breakers

In this chapter, the results of the analysis of the six HVDC circuit breakers are presented. For each circuit breaker, first, the maximum interruptible current and the minimum internal current commutation time are described analytically as functions of the component dimensioning and limits. Second, the resulting dimensioning of the model and its implementation in PSCAD is described. Subsequently, the analytic results are verified by simulating the circuit breaker in the HVDC circuit, and the electrical stress on the switching components is investigated. Then, the circuit breaker’s capability to operate in different fault cases and the effect of faster mechanical switches are inspected, before the potential features of the circuit breaker are discussed. The circuit breaker-wise investigation is concluded with a discussion. After presenting all circuit breakers, the chapter’s last section gives a comparison of the different topologies.

5.1. LCS-MB

Figure 5.1.: Functional bidirectional layout of LCS-MB (greyed out components are activated only for breaking fault currents from right to left; neither showing snubber circuits in parallel to semiconductor stacks nor stray inductances)
5.1.1. Analytical Description

Maximum Interruptible Current

For the LCS-MB, the maximum interruptible current is limited by two constraints during the circuit breaker operation:

Commutation NCP–CCP A snubber circuit in parallel to the LCS is required to protect the semiconductors against the transient overvoltage, which occurs after their turn-off. By adequately dimensioning the snubber, a fast commutation can be achieved, but at the same time it can only operate up to a certain fault current. As the snubber circuit is described in [HHJ14a], this is not elaborated further. The defined snubber circuit commutation capability has to exceed the fault current in the instant when the circuit breaker receives the trip signal.

CCP The maximum current that can be interrupted by the MB-unit in the CCP is defined by the interruption capability of the IGBT stack. [HJ11] showed that this limit is defined by the saturation current limit of the IGBT rather than by the Safe Operation Area (SOA). The interruption capability has to exceed the fault current in the moment when the UFD is opened completely.

Internal Current Commutation Time

The internal current commutation time in the LCS-MB concept can be described by

$$\Delta t_{CC} = t_{peak} - t_{trip} = \Delta t_{NCP-CCP} + \Delta t_{UFDopening} + \Delta t_{CCP-EAP}$$  \hspace{1cm} (5.1)

The time $\Delta t_{NCP-CCP}$ required for the commutation of the current from the NCP into the CCP is primarily defined by the time necessary to energize the stray inductance $L_{stray}$. By assuming the fault current to be constant during the short commutation period, by approximating the voltage across the LCS by $V_{sn} \approx I(t_{trip}) \cdot R_{sn}$, and by neglecting the MB’s resistance,

$$\Delta t_{NCP-CCP} \approx \frac{I(t_{trip})}{dI_{CCP}(t_{trip})} = \frac{I(t_{trip})}{V_{sn}} \cdot \frac{L_{stray}}{R_{sn}} = \frac{L_{stray}}{R_{sn}}.$$  \hspace{1cm} (5.2)

The opening time of the UFD $\Delta t_{UFDopening}$ is defined by the mechanical switch. The commutation time $\Delta t_{CCP-EAP}$ from the CCP into the EAP is partly defined by the snubber circuits in parallel to the semiconductors in the MB. But as this delay is very short, in the range of microseconds [HHJ14a], $\Delta t_{CCP-EAP}$ can be omitted.

1 Valid for the $R$-$C$ ratio of the implemented snubber circuit.
5.1.2. Implemented Circuit Breaker Model

The implemented model of the circuit breaker is based on the information published in [HHJ14a], as the published dimensioning is rated for a voltage and fault similar to the ones investigated in the scope of this work. The topology of the model implemented in PSCAD for simulation is illustrated in Figure 5.1.

NCP On the NCP, a UFD is connected to a bidirectional LCS. It consists of two series connected $3 \times 3$ IGBT stacks, each of the two protected by an RCD snubber circuit ($1 \Omega, 16 \mu F$).

CCP The main breaking unit is modeled with four bidirectional modules, each consisting of two times 40 series connected IGBTs and an inductor of $\frac{L_{\text{stray}}}{4} = 12.5 \mu H$ in series.

EAP The EAP is realized by four MOV, each with a clamping voltage of $80 \text{kV}$ and connected in parallel to an MB-module, each with an inductor of $\frac{L_{\text{stray}}}{4} = 12.5 \mu H$ in series.

5.1.3. Simulation Results

Figure 5.2.: LCS-MB path currents and circuit breaker voltage, simple HVDC circuit ($t_{\text{fault}} = 0 \text{ ms}, U_N = 320 \text{kV}, I_N = 2 \text{kA}, L = 100 \text{mH}, R_F = 0.01 \Omega$)

Figure 5.2 shows the currents in the circuit breaker’s paths and the voltage across the circuit breaker with the fault occurring at 0 ms. During steady state operation, 22.6 kW losses in the breaker are measured, which result from the use of an LCS.
Operation Speed and Maximum Current

The circuit breaker is signaled 125.5 µs after the fault occurs, when the fault current reaches 2.4 kA. The breaker operation time for this fault case is 2.05 ms, and the voltage rise time is 0.13 µs. Because of the very short voltage rise time, the time difference between the fault current peak and the TIV peak is negligibly small. The overall break time, until the leakage current level is reached, is 8.45 ms.

The calculated internal current commutation time of 2.05 ms equals the sum of the breaker operation time and the voltage rise time of the simulation.

The snubber circuit protects the LCS in simulations up to a current of 9.6 kA at the moment of the LCS signaling. This value exceeds the published value of 8 kA [HHJ14a]. The maximum current in the MB is limited by the published testing limits of 16 kA [RSD+14], respectively the datasheet surge current limit of 32 kA, which has to be checked manually in the simulation for the moment when the MB is signaled.

Stress on Components

**NCP** The UFD has to carry a maximum current of 2.4 kA, which is 0.2 kA below its rated continuous current. The maximum voltage across the UFD equals the TIV of 477 kV.

The opening of the UFD is performed completely load-free, no current is flowing through the UFD between commutation and final triggering of the PSCAD circuit breaker model.

Assuming a homogeneous distribution, the maximum current in the individual IGBTs of the LCS is measured to be 0.8 kA, when blocking, the maximum voltage across a single IGBT devices is 1.19 kV. The maximum \( \frac{dI}{dt} \) and \( \frac{dU}{dt} \) observed in the IGBTs are 1.60 kA s⁻¹ and 1.66 kV s⁻¹ respectively.

**CCP** In the MB’s series connected IGBTs, a maximum current of 8.92 kA and a voltage peak of 2.98 kV is observed. The \( \frac{dI}{dt} \) and \( \frac{dU}{dt} \) peaks are very high, 17.85 kA s⁻¹ and 5.94 kV s⁻¹, which is due to neglecting the snubber circuit for the MB. However, test results showed [HJ11], that a very steep voltage rise can be mastered by the breaker and does not cause problems.

**EAP** In the EAP, the MOVs have to carry a current of up to 8.2 kA and the energy dissipation, until the leakage current level is reached, takes 6.4 ms.

5.1.4. Sensitivity Analysis

In this section’s first part, the fault current margin for successful interruption is identified and the re-dimensioning for higher currents as well as the circuit breakers most current-sensitive components are discussed. In the second part, the sensitivity of the internal current commutation time to a faster opening of the UFD is investigated.
Sensitivity to Fault Current

Sensitivity of default dimensioning  Figure 5.3 shows the interruption limits, identified in the previous section, as well as the default fault case with 2 kA nominal current and a \( \frac{dI}{dt} \) of 3.2 kA ms\(^{-1}\). The first limitation, of the LCS snubber circuit, is 5.6 kA above, the MB limit is 5 kA above the default fault current. For a successful interruption of a fault, the fault current curve must pass below the two discussed limitations: Assuming a \( \frac{dI}{dt} = 3.2 \text{ kA ms}^{-1} \), interruption is successful up to a current of 8 kA at the moment of LCS signaling. For a detection at 2.4 kA, the \( \frac{dI}{dt} \) can be up to 6.6 kA ms\(^{-1}\). Neither increasing the fault detection level up to 2.9 kA or 3.6 kA nor reducing it to 1.5 kA affect the internal current commutation time of the circuit breaker. For a smaller nominal current of 1.5 kA, the internal current commutation time prologues only by 3 \( \mu \text{s} \), necessary to build up the commutation voltage in the snubber. The internal current commutation time is almost completely independent of the fault current because of primarily using semiconductors, which interrupt all currents within their limitations in insignificantly short time.

Upgrading for higher fault currents  Upgrading the LCS-MB circuit breaker for a higher fault current interruption capability primarily requires increasing the current carrying capability of the IGBTs in the MB. This is either achieved by connecting a second row of IGBTs in series and designing a control for simultaneous turn-off or by developing switch-off semiconductor devices with a better performance.
Furthermore, to ensure the commutation of currents exceeding the identified NCP–CCP commutation limit, an adjustment of the snubber circuit for the LCS and a higher blocking capability of the LCS may be required. The latter can be achieved by additional units in series, which come at the cost of higher conduction losses during normal operation.

**Breaker Speed Sensitivity**

**Mechanical switch opening time**  By reducing the opening time of the UFD by 20\% to 1.6 ms, the internal current commutation time decreases by 20\%/0.4 ms, too.

**Other variables**  As the contribution of the other components, such as the stray inductance, is negligibly small compared to the opening time of the UFD and the latter’s effect on the circuit breaker speed, no further investigation is performed.

### 5.1.5. Features

The LCS-MB circuit breaker promises three features, whose limitations are discussed qualitatively:

**Pre-activation**  Based on local detection schemes, it is possible to pre-activate the circuit breaker. The current can be commutated and the mechanical switch opened. The trip signal has to reach the breaker before the energy dissipated in the CCP leads to a thermal destruction of its IGBTs. However, to successfully commutate the current back into the NCP, the mechanical circuit breaker has to be closed again. Hence, the MB has to withstand the fault current for at least the sum of the opening and closing time of the UFD plus a possible dead time in between.

**Current limiting**  Current limiting is achieved by selective turn-off of the MB modules after the current has been commutated into the CCP and the UFD has been opened. By building up a voltage inverse to the system voltage and dissipating excess energy in the parallel MOVs, the current increase can be reduced in discrete steps. As for the pre-activation, the current limiting functionality can only be used for a limited amount of time, which is defined by thermal limits of the MOVs and the IGBTs in the MB.

**Open–Close–Open**  The LCS-MB in principle is capable of performing an immediate performance of an Open–Close–Open sequence, to check whether the fault was cleared in the meantime or not. However, thermal limits for the whole process have to be respected for the sequence, especially if the current limiting feature has been used during the turn off.
5.1.6. Discussion

The LCS-MB circuit breaker concept operates at high speed, very close to the intrinsic limit of the opening time of the UFD. Because of the employed turn-off semiconductors, a wide range of fault currents up to 16 kA can be interrupted. The operation time is almost completely independent of the fault current.

The maximum interruptible current can only be increased, by increasing the interruption capability of the IGBTs in the MB. Lifting this *hard limit* comes at high costs, either by a parallel connection of a second row of 320 IGBTs and the necessary control [DW13] or with the development of improved power semiconductors. Thanks to the pre-activation feature, upgrading the LCS for currents exceeding the already provided margin of 8 kA [HHJ14a] during the first commutation most likely can be avoided.
5.2. LCS-C

![Functional bidirectional layout of LCS-C](image)

Figure 5.4.: Functional bidirectional layout of LCS-C (greyed out components are activated only for breaking fault currents from right to left; neither showing snubber circuits in parallel to semiconductor stacks nor stray inductances)

5.2.1. Analytical Description

**Maximum Interruptible Current**

The maximum fault current, that can be interrupted by the LCS-C circuit breaker is limited primarily by the three commutation steps between the CCP branches, more precisely by the dimensioning of the respective capacitances. Neither the current carrying capability of the semiconductors nor the cooling of the MOV is critical, because of the short operation times.

**Commutation NCP–TB1** The first commutations step is successful as long as the voltage across the LCS remains below its forward blocking voltage. This depends on the size of the inductance of the TB1 and the capacitor of the snubber circuit for the LCS and is calculated from

$$\frac{1}{C_{sn}} \int_{t_{trip}}^{t_{sn=0}} i_{sn}(t) \, dt \leq U_{LCS,\text{rating}}.$$  \hspace{1cm} (5.3)
The instant $t_{i_{sn}=0}$ when $i_{sn} = 0$ is obtained from solving the second-order differential equation

$$\frac{1}{C_{sn}} \int_0^t i_{sn} dt + R \cdot i_{sn} + L_{TB1} \frac{di_{sn}}{dt} = 0$$

with the initial conditions $i_{sn} = I(t_{trip})$, $V_C = 0$ kV and the fault current assumed to be constant during the short time of commutation. The capacitance in first Timing Branch $C_{TB1}$ is much larger than the snubber capacitance, dimensioned to reach the clamping level of the parallel MOV shortly before the UFD has opened, and can therefore be ignored in this equation, too.

**Commutation TB1–TB2** For the commutation into the second Timing Branch, the voltage $U_{C_{TB1}}$ across the the capacitance $C_{TB1}$ is assumed to be constant at the clamping voltage level $U_{MOV_{TB1}}$ of the parallel connected MOV, because $C_{TB1} \gg C_{TB2}$. The maximum fault current that the circuit breaker is able to commutate from TB1 into TB2, after the UFD has opened, is derived from the energy stored on the capacitor $C_{TB2}$ that is transferred to the inductor $L_{TB1–TB2}$:

$$i_{TB1–TB2} = U_{MOV_{TB1}} \cdot \sqrt{\frac{C_{TB2}}{L_{TB1–TB2}}}.$$

**Commutation TB2–AB** As for the commutation between the two Timing Branches, $U_{C_{TB2}} = U_{MOV_{TB2}}$ can be assumed, because $C_{TB2} \gg C_{AB}$. The fault current limit for the commutation from Timing Branch 2 into the Arming Branch, initialized after the voltage across the capacitor $C_{TB2}$ crosses the commutation threshold, is

$$i_{TB2–AB} = U_{MOV_{TB2}} \cdot \sqrt{\frac{C_{AB}}{L_{TB2–AB}}}.$$

**Internal Current Commutation Time**

The internal current commutation time, from the trip order until the TIV peak is

$$\Delta t_{CC} = \Delta t_{NCP–TB1} + \Delta t_{UFDopening} + \Delta t_{TB1–TB2} + \Delta t_{TB2,charged} + \Delta t_{TB2–AB} + \Delta t_{AB,charged}$$

The commutation delay $\Delta t_{NCP–TB1}$ can be approximated with the time required for the increasing current in the inductor reaching the fault current level $\Delta t_{NCP–TB1} = \frac{L_{TB1}}{I_{sn}}$, as for the LCS-MB, but for larger inductances $L_{TB1}$ on the Timing Branch 1, this approximation is very conservative.

The maximum times necessary for commutation between TB1 and TB2, respectively, TB2 and AB are calculated as the peak of the current counter-injected from the first
of the two branches to enforce the commutation.

\[
\Delta t_{TB1-TB2} = \frac{\pi}{2} \sqrt{L_{TB1-TB2} \cdot C_{TB2}} \tag{5.8}
\]

\[
\Delta t_{TB2-AB} = \frac{\pi}{2} \sqrt{L_{TB2-AB} \cdot C_{AB}} \tag{5.9}
\]

The time necessary for charging the capacitors in TB2 and AB up to the respective clamping voltage of the parallel MOV are obtained by solving

\[
U_{MOV_{TB1}} = \frac{1}{C_{TB2}} \int_{t_{TB2}}^{t_{TB2}+\Delta t_{TB2,charged}} i(\tau) d\tau \tag{5.10}
\]

\[
TIV = \frac{1}{C_{AB}} \int_{t_{AB}}^{t_{AB}+\Delta t_{AB,charged}} i(\tau) d\tau \tag{5.11}
\]

The charging time can be approximated by defining \( t_{TB2} \), respectively \( t_{AB} \), as the moment of completing the commutation into the respective branch, as the charging of the capacitor during the short commutation period is relatively small.

From these formulas, it is obvious that the prospective fault current slope has a considerable impact on the time it takes to operate this circuit breaker. Since commutation times are relatively small compared to the charging times, this effect largely influences the total operation time of the circuit breaker.

For small detection levels and low rates of rise, this can cause a considerably higher interruption time, for high detection levels and high rates of rise of current, the breaker operates faster, the natural limit being that the mechanical switch must be opened before the second timing branch and the arming branch are charged.

### 5.2.2. Implemented Circuit Breaker Model

As no precise information has been published on the dimensioning of the LCS-C circuit breaker, it was dimensioned from scratch in the scope of this work, to achieve a successful interruption of the default fault case at minimum time. The implemented bidirectional circuit breaker topology was adopted from [DGC11], as shown in Figure 5.4.

**NCP** For the LCS identical dimensions as for the LCS-MB concept were selected, to provide sufficient commutation voltage at low losses during normal operation. Two anti-parallel stacks of \( 3 \times 3 \) IGBTs with parallel \( 1 \Omega \), 16 \( \mu \)F RCD snubber circuits are connected in series with the mechanical switch, a UFD with the same characteristics as the one used in the LCS-MB.

**CCP** To minimize the energy dissipation in the MOV and the voltage opposing the LCS during commutation, a large capacitor of 800 \( \mu \)F and an additional inductor of 50 \( \mu \)H in series to the stray inductance of equal size were selected for the Timing Branch 1 of the CCP. With these dimensions, charging the capacitor to the clamping
voltage of the parallel MOV takes almost the complete UFD opening time. The MOV starts conducting at 11 kV to prevent charging the capacitor up to the breakdown voltage of the parallel LCS. According to the formulas presented in the previous section and the prospective fault current, a capacitor of 120 µF is connected, in series with the stray inductance, in Timing Branch 2 to ensure the commutation of the default fault current after the UFD opening. The clamping voltage of the parallel MOV is set to 50 kV, based on the recommendations in [DGC11].

To allow fast charging up to the TIV, while ensuring the current commutation out of the Timing Branches and the turn off of the respective semiconductors at current reversal, the Arming Branch capacitor, in series with the stray inductance, is set to 7 µF. To prevent undesired overcharging of the capacitor by energy stored in the stray inductance, line and current limiting reactors, a large, protective MOV, clamping at 640 kV, is connected in parallel.

Furthermore, bleeding resistors of 1 MΩ are connected in parallel to all the branch capacitors, as proposed in [DGC11]. All commutation branches are equipped with 75 thyristors in series, to withstand the TIV. In the Arming Branch, these 75 semiconductors are combined in the stack AB. For the Timing Branches, they are split up into the 60-units TB stack and the two 15-units stacks TB1 and TB2. This reduces both the voltage drop along the semiconductors during the commutation from the first into the second Timing Branch and the total number of required semiconductors. The 15 units in TB1 and TB2 are selected to provide a sufficient reliability margin above the maximum voltage drop across TB1, but for the default fault case 10 units operate successful, too. To ensure both transient and steady state voltage sharing between these capacitors, proportional snubber circuits and high-ohmic grading resistors are connected in parallel to the stacks [Sev06]. The voltage level of \(U_{C_{TB2}}\) at which AB is turned on, is set to 48 kV [DGC11].

**EAP** In the EAP, the default MOV, rated for 240 kV, which corresponds to a clamping voltage of 480 kV, is connected in series with the stray inductance.

### 5.2.3. Simulation Results

In Figure 5.5, the currents in the circuit breaker’s branches and the voltage across the circuit breaker are shown. The currents in the branches are differentiated by color. A decreasing time of current carrying is observed along the three branches. The desired early rise of voltage to the Timing Branches’ voltage levels as well as an undesired residual current in the NCP during the UFD opening, are observed.

The simulated nominal losses of the LCS-C concept are equal to those in the LCS-MB concept, 22.6 kW.
Operation Speed and Maximum Current

After a relay time of 125.5 ms the breaker is signaled, from then on it takes a total of 10.72 ms until the interruption is completed and the leakage current level is reached. The fault neutralization time for the simulated fault is either 3.06 ms (to fault current peak) or 3.10 ms (to TIV peak), depending on the definition used. The difference results from the, compared to the other concepts relatively large, capacitor in the Arming Branch.

The internal current commutation time, consisting of the breaker operation time and the voltage rise time, as defined in Chapter 4, is \( \Delta t_{CC,sim} = 2.73 \text{ ms} + 0.31 \text{ ms} = 3.04 \text{ ms} \). When comparing the analytically derived times with the measured times in the nominal fault case

\[
\Delta t_{CC,sim} = 0.06 \text{ ms} + 2 \text{ ms} + 0.17 \text{ ms} + 0.47 \text{ ms} + 0.03 \text{ ms} + 0.31 \text{ ms} = 3.04 \text{ ms} \\
\Delta t_{CC,ana} = 0.1 \text{ ms} + 2 \text{ ms} + 0.21 \text{ ms} + 0.54 \text{ ms} + 0.04 \text{ ms} + 0.3 \text{ ms} = 3.19 \text{ ms}
\]

(5.12)  
(5.13)

the approximation of the charging time of \( C_{TB1} \) is set off by 70 \( \mu \text{s} \), because the charging of the capacitor during the commutation is neglected. In the simulation, the commutation is completed before the LC pulse reaches its peak, and therefore the analytic commutation times are longer by 10 \( \mu \text{s} \) to 50 \( \mu \text{s} \).

The maximum current, which the LCS is able to commutate into the Timing Branch 1, is 7.5 kA and must not occur earlier than 73 \( \mu \text{s} \) after the trip signal, as the circuit breaker

Figure 5.5.: LCS-C path currents and circuit breaker voltage, simple HVDC circuit  
\( (t_{\text{fault}} = 0 \text{ ms}, U_N = 320 \text{ kV}, I_N = 2 \text{ kA}, L = 100 \text{ mH}, R_F = 0.01 \Omega) \)
requires a certain time to build up the required commutation voltage. For the commutation TB1–TB2, simulations returned a maximum current of 9.62 kA, 2.27 ms after the trip signal. This result is 280 A below the calculated value and is due to omitting the semiconductors’ resistance. The simulation shows that the fault current during commutation TB2–AB must be below 12.5 kA, 2.72 ms after the trip signal. Again this current is 200 A below the predicted maximum due to the semiconductors. Concluding, the simulation results match the analytically derived values. The relatively small deviations can be attributed to the simplifications used in the analytical calculations and indicate that the presented formulas are sufficient for the dimensioning of the used components.

**Stress on Components**

**NCP** For the UFD, a maximum current of 2.4 kA and a maximum voltage of 479 kV are measured, which is in the expected range. Due to the simplified UFD model (transition from $R_{\text{closed}}$ to $R_{\text{open}}$ only at the moment when UFD is fully open), a small current flow, with a peak value below 200 A, can be observed in the UFD during the opening process. However, due to the fact that the current remains considerably smaller for the first 0.25 ms and the voltage across the UFD remains close to zero, a successful switching operation of the UFD can be assumed. Hence, due to an almost immediate contact separation in reality no such current is expected to flow. In the LCS, a maximum current of 800 A per IGBT is measured. The maximum voltage goes up to 4.00 kV, which is 0.5 kV below the breakdown voltage. The rate of rise of current and voltage remain below 1.60 kA $\mu$s$^{-1}$ and 2.24 kV $\mu$s$^{-1}$.

**CCP** The thyristors in the CCP are exposed to currents from 8.88 kA to 11.06 kA as well as voltages from 2.07 kV to 6.87 kV, with TB2 and AB thyristors exposed to much smaller voltages than TB and TB1. The $\frac{di}{dt}$ in TB1 reaches a maximum of 107 A $\mu$s$^{-1}$ while in TB, TB2 and AB values from 666 A $\mu$s$^{-1}$ to 790 A $\mu$s$^{-1}$ are reached, which still is significantly below the limit of 3 kA $\mu$s$^{-1}$ [WM13]. Regarding the rate of rise of voltage, the highest values observed in TB1, TB2 and AB are 1.2 kV $\mu$s$^{-1}$ to 2.7 kV $\mu$s$^{-1}$. These occur in the moment when TB turns off and suddenly relieves the blocking burden of TB1 as well as when TB2 and later AB are turned on. In contrast, for the timing branch semiconductor units, the critical rate of rise of voltage, immediately after turn off, is only in the range of 5 V $\mu$s$^{-1}$ to 25 V $\mu$s$^{-1}$ and for the AB below 300 V $\mu$s$^{-1}$. The voltage across the capacitors $C_{TB2}$ and $C_{AB}$ in the CCP rises at a maximum level of 88 V $\mu$s$^{-1}$ and 1.60 kV $\mu$s$^{-1}$, respectively.

**EAP** The MOV in the EAP has to dissipate the remaining energy, which is done in 7.64 ms from a current of 11.02 kA to the leakage current level of 5.2 A.
5.2.4. Sensitivity Analysis

In this section, the fault current margin for successful interruption is identified and the re-dimensioning for higher currents as well as the circuit breakers most current-sensitive components are discussed. The sensitivity of the internal current commutation time to a faster opening of the UFD or to a lower TB2 voltage threshold is investigated.

Sensitivity to Fault Current

Sensitivity of default dimensioning  In Figure 5.6 the interruption limits, achieved from the simulation, are shown together with the linearly increasing default fault current. Only if any arbitrary fault current curve passes below all of the limits, the interruption is be successful. As Figure 5.6 illustrates, neither an increase of the rate of rise of current nor the detection limit can result in a successful interruption since basically no margin is left between the indicated fault current and the interruption limits of the presented dimensioning. In both cases the fault current will exceed the maximum for the commutation TB1–TB2.

When the trip order is issued delayed, at a 0.5 kA higher current of 2.9 kA, successful interruption can be achieved by reducing the additional inductance in the Timing Branch 1 from 50 µH to 30 µH. This modification increases maximum interruptible current slightly without negatively affecting the internal current commutation time, neither when the trip signal is given at 2.9 kA nor at 2.4 kA. Only the rate of rise of current through TB and TB1 increases.
When the trip signal is given at 3.6 kA, all branches have to be adjusted:

\[
\begin{align*}
L_{TB1} &= 80 \mu \text{H} (-20 \mu \text{H}) \\
C_{TB1} &= 1 \text{mF} (+200 \mu \text{F}) \\
C_{TB2} &= 150 \mu \text{F} (+30 \mu \text{F}) \\
C_{AB} &= 8 \mu \text{F} (+1 \mu \text{F})
\end{align*}
\]

The basic idea of the adjustment is to balance the charging time that decreases due to higher fault currents with increasing the size of the capacitors. Higher rates of rise of current also merit a faster commutation, hence the inductance of some branches needs to be reduced. As a consequence, the internal current commutation time, which also includes the charging time of the capacitors, increases only by about 1.6% compared to the 3.09 ms of the default case. Interrupting the default fault current with this adjusted circuit breaker takes 0.18 ms longer than with the default dimensions.

The interruption of a smaller fault current, detected at 1.2 kA is successful but the observed internal current commutation time is 3.18 ms, 0.14 ms longer than in the default fault case. This is mainly caused by a residual current in the NCP which prevents the UFD from immediate opening after 2 ms for 0.1 ms and to a small extent to the longer time for charging the capacitors 0.04 ms.

**Upgrading for higher fault currents**  As discussed in the previous paragraph, interrupting currents higher than the presented fault case at maximum possible speed can only be achieved by adjusting the CCP-branches. Primarily, the limit of the commutation TB1–TB2 has to be increased by adjusting \(C_{TB1}\) or the LCS rating, according the analytic formulas presented. Depending on the slope of the fault current, the other branches have to be adjusted as well, to ensure commutation and thyristor turn off. For the exemplary case of increasing the interruption capability by 1 kA above the default limits, the adjustments explained in the previous paragraph have to be realized.

**Breaker Speed Sensitivity**

**Mechanical switch opening time**  When the UFD opening time is reduced by 0.4 ms to 1.6 ms, the internal current commutation time can be improved. By reducing the capacitances to match the decreased prospective fault current following the UFD opening (\(C_{TB1} = 500 \mu \text{F}, C_{TB2} = 100 \mu \text{F}, C_{AB} = 5 \mu \text{F}\)), the internal current commutation time reduces by 0.43 ms. In addition to the 40 ms faster UFD, 0.03 ms are gained by the shortened voltage rise time, due to the smaller Arming Branch capacitance.

**Other variables**  Setting the TB2 voltage threshold, above which the commutation into the Arming Branch is initialized, to the lowest of the exemplary values published in [DGC11], is investigated. This modification requires, in addition to further adjustments, a doubling of the Arming Branch capacitance and consequently leads to an increase of the internal current commutation time of 0.14 ms.
5.2.5. Features

**Pre-activation** The LCS-C circuit breaker concept allows pre-activation by performing the interruption sequence until the UFD has opened autonomously. Subsequently, the heat dissipation at the semiconductors TB and TB1, as well as at the MOV in the first Timing Branch, determine how long the circuit breaker can wait for a trip signal. If no trip signal is received in time, the current is commutated back into the NCP by closing the UFD and turning the LCS back on. If this feature is desired, the thyristor stacks and especially the MOVs have to be designed accordingly.

**Current limiting** The LCS-C concept does not have any turn-off semiconductors in the CCP and hence is less flexible than the LCS-MB. Still, a basic current limiting function may be archived the LCS or the different branches of the CCP. However, to evaluate and qualify the current limiting potential of the LCS-C, further investigations are necessary that would exceed the scope of this thesis.

**Open–Close–Open** The LCS-C can be closed again after current interruption by closing the UFD. However, to perform another interruption, necessary for a full Open–Close–Open cycle, the capacitances have to be discharged first. By waiting for a discharge through the proposed large bleeding resistors, a fast re-opening may not be achieved. Fast discharging units, consisting of a TSG and small resistors, in parallel to the capacitors can be employed to quickly reduce the capacitor voltage to levels at which interruption is successful.

5.2.6. Discussion

The LCS-C circuit breaker concept requires approximately 1 ms after the UFD opening to complete its three-branch sequence. When the circuit breaker is intended to operate at maximum speed, the maximum interruptible fault current has to be well defined. Even though the circuit breaker imposes three different limit onto the fault current during its operation, only the second limit is expected to be relevant for the operation. Compared to prospective fault currents in grids [LAB+15], the first limit provides sufficient margin and the third limit is unlikely to be reached as the rate of rise of the fault current is expected to decrease much faster than in the presented fault case.

As both the analytical formulas and the simulation data show, the circuit breaker is very sensitive to adjustment of the dimensioning. Scaling the circuit breaker up for higher fault currents comes at the cost of a longer operation and voltage rise time for the nominal fault currents, since it will take longer to charge the scaled-up capacitors. In contrast, most of the employed semiconductors operate far below their limits and do not impose a hard limit onto the maximum interruptible current.

The sensitivity analysis showed that the derived dimensioning of the LCS-C is close to achieving maximum speed with the given topology and modeling rules. The residual current re-occurring in the NCP, due to the simplified model, may cause the UFD to open with significant delay in other fault cases. Hence, there may be fault
cases in which the performance of the switch is negatively influenced, which needs to be checked in every simulation. An update of the opening characteristics of the model for the mechanical switch should fix this issue.
5.3. Inj-C

![Functional bidirectional layout of Inj-C](image)

**Figure 5.7.** Functional bidirectional layout of Inj-C (greyed out components are activated only for breaking fault currents from right to left; neither showing snubber circuits in parallel to semiconductor stacks nor stray inductances)

5.3.1. Analytical Description

**Maximum Interruptible Current**

For the Inj-C concept, the maximum interruptible current is defined by two limits. First, a limit for the initial commutation into the CCP is imposed, and second, after the UFD opening another limiting condition has to be fulfilled before the TIV starts to rise. In both formulas presented below, the resistance of the semiconductors is neglected, therefore limits achieved in simulation are expected to be slightly smaller.

**Commutation NCP - CCP**  For the initial commutation of the current from the NCP to the CCP, the devices T1 and T3 are turned on, connecting the pre-charged capacitor in parallel to the NCP. The peak amplitude of the injected current pulse defines the maximum current that can be commutated and is derived by the energy conversion from electric energy (stored in the capacitor) to magnetic energy (in the inductor)

\[
i \left( t_{\text{trip}} + \frac{\pi}{2} \sqrt{\frac{L_{T1-C-T3} \cdot C}{2}} \right) = U_{\text{pre}} \sqrt{\frac{C}{L_{T1-C-T3}}} \tag{5.14}
\]
Commutation T2–T3 – T2–C–T4  After the successful opening of the UFD, the current is redirected from the “bypassing” semiconductor path T2-T3 back into the capacitor, which then is charged up to the TIV. To ensure this commutation step and the turn off of T4, the capacitor voltage has been reversed to $U_{neg}$. Similar to the previous commutation, the maximum current can be obtained from

$$i \left( t_{UFDopen} + \frac{\pi}{2} \sqrt{\frac{L_{T3-C-T4}}{C}} \right) = U_{neg} \sqrt{\frac{C}{L_{T3-C-T4}}}, \quad (5.15)$$

with $L_{T3-C-T4}$ being the overall inductance of the T3–C–T4 loop.

Other limitations  The nominal current is bound by the continuous current rating of the semiconductors and the UFD on the NCP. For the semiconductors on the CCP, the component specific surge current rating is critical, because of the short operation time of a few milliseconds.

Internal Current Commutation Time

The internal current commutation time is the sum of both commutations, as derived above, the opening time of the UFD and the time required for charging the capacitor from $U_{neg}$ to the TIV:

$$\Delta t_{CC} = \frac{\pi}{2} \sqrt{\frac{L_{T1-C-T3}}{C}} + \Delta t_{UFDopening} + \frac{\pi}{2} \sqrt{\frac{L_{T3-C-T4}}{C}} + \Delta t_{C,TIV} \quad (5.16)$$

The time for charging the capacitor can be calculated using the following equation:

$$TIV = \frac{1}{C} \int_{t_{T4}}^{t_{T4} + \Delta t_{C,TIV}} i(\tau) d\tau \quad (5.17)$$

with the assumption that the capacitor is approximately discharged at the instant $t_{T4}$, when the commutation into T4 is completed.

5.3.2. Implemented Circuit Breaker Model

Several changes compared to the published Inj-C concept have been made in the implemented PSCAD model: Due to the adaption of the published topology to high voltage, the pre-charge capacitor voltage is reduced to allow a NCP semiconductor, which has to block the pre-charge voltage, of lower rating relative to the system voltage. Since a bipolar version of the circuit breaker has not been published yet, in this thesis an update for was developed that makes bipolar use possible, as shown in Figure 5.7. For this, the amount of semiconductors in the CCP is doubled but the number of passive elements (capacitor, inductors) remains unchanged. In contrast to the published breaker, charging the capacitor up to the TIV is not initiated simultaneously with the UFD opening but only after it is completed to ensure a safe operation.
of the circuit breaker. The negative voltage $U_{\text{neg}}$, to which the capacitor is charged, is actively controlled based on an estimation of the fault current making inductors in series with T2 and T3 in addition to the stray inductances unnecessary. This allows a slight reduction of both the internal current commutation time and the stress on components.

**NCP** In the nominal current path, a UFD is connected in series with two anti-parallel thyristor stacks D, each consisting of a matrix of 4 series and 3 parallel, rating for blocking a voltage of 17 kV (maximum blocking capability of 38.4 kV). The dimensions of the matrix are selected, so that the rated values exceed the pre-charge capacitor voltage that D has to block as well as the maximum current in the devices before commutation. The third parallel row of 4 thyristors is only installed for reliability, similar to the LCS in LCS-MB and LCS-C [HHJ14a].

**CCP** For unidirectional configuration, two branches, each consisting of two stacks of semiconductors are in parallel to the NCP. All four stacks consist of 75 thyristors in series, with a 5 kΩ/0.05 μF RCD snubber circuit in parallel and all directed from rectifier to inverter terminal. Both branches are connected via a capacitor $C$ of 15 μF in the middle and form an H-bridge configuration. The capacitor is pre-charged before operation to $U_{\text{pre}} = 16$ kV. Capacitance and pre-charge voltage are chosen to provide successful commutation according to the earlier derived formulas while at the same time balancing the internal current commutation time and the conduction losses during normal operation in D. The pre-charge voltage level can be reached by discharging the capacitor after a successful interruption from TIV to $U_{\text{pre}}$ with a discharging circuit, which is neglected in the model.

The first branch consists of the stacks T1 and T4. Next to both stacks an appending inductor of $\frac{L_{\text{stray}}}{2}$ is connected. In series with T1 an additional inductor of 50 μH is connected to slow down the commutation to allow a better control of the capacitor voltage reversal and $U_{\text{neg}}$. The second branch consists of semiconductor stacks T2 and T3, both modeled with a stray inductance of $\frac{L_{\text{stray}}}{2}$ in series.

For a bidirectional design, which is illustrated in Figure 5.7 two more branches of similar configuration, but anti-parallel, have to be installed.

**EAP** In the EAP, the default MOV, rated for 240 kV, which corresponds to a clamping voltage of 480 kV, is connected in series with the stray inductance.

**Influence of current reversal** In difference to the previously analyzed concepts, the implemented Inj-C circuit breaker control has to act different when the fault leads to a reversal of the current direction. In this case, the Inj-C breaker has to delay the first commutation stage until the current has changed direction, otherwise, charging $C$ to $U_{\text{neg}}$ is unsuccessful.
5.3.3. Simulation Results

\[ \Delta t_{CC, sim} = 0.016 \text{ ms} + 2 \text{ ms} + 0.036 \text{ ms} + 0.76 \text{ ms} = 2.81 \text{ ms} \] (5.18)

\[ \Delta t_{CC, ana} = 0.06 \text{ ms} + 2 \text{ ms} + 0.04 \text{ ms} + 0.7 \text{ ms} = 2.8 \text{ ms} \] (5.19)

Because of the relatively slowly voltage rise time, a time difference between the fault current peak and the maximum TIV of only 0.1 ms is observed. The fault current
suppression time from the TIV peak until the current falls below the leakage current level is 6.92 ms.
The first limit imposed on the fault current slope, the commutation of the current from the NCP to the CCP via the capacitor, occurs 0.06 ms after the trip signal, as predicted. Because of omitting the thyristor stacks’ resistance, the maximum current of 5.9 kA is 0.3 kA below the predicted value.
The second limit, the commutation from the path T2–T3 to the path T2–C–T4, of 9.36 kA occurs in the simulation 0.04 ms after the UFD has opened. The time delay equals the analytic prediction, but the maximum value exceeds the prediction of 8.76 kA by 0.6 kA, because the implemented control of $U_{neg}$ does not take the “over-charging” of C during the commutation from TB1–C–TB3 to TB2–TB3 into account and consequently overcharges the capacitor to 17.2 kV instead of the intended 16 kV.

**Stress on Components**

**NCP**  As expected, the UFD has to carry a maximum current of 2.4 kA, which corresponds to the detection level, and block a maximum voltage of 482 kV, corresponding to the MOV clamping voltage. The individual thyristors in D are exposed to a maximum current of 800 A with a maximum rate of rise of 78 A $\mu$s$^{-1}$ and a maximum voltage of 4079 V. The $\frac{dU}{dt}$ immediately after turn-off is $-4829$ V $\mu$s$^{-1}$ per semiconductor, caused by the voltage across the capacitor.

**CCP**  The thyristors have to carry currents ranging from 3 kA to 10 kA, with maximum rates of rise of current between 240 A $\mu$s$^{-1}$ to 540 A $\mu$s$^{-1}$. The maximum rates of rise of voltage measured across both thyristor sets, for normal and inverse operation, do not exceed 478 V $\mu$s$^{-1}$. These $\frac{dI}{dt}$ and $\frac{dU}{dt}$ values are due to the parallel snubber circuit.
The T2 and T4 stacks have to withstand a maximum voltage of 1.2 kV whereas T1 and T3 have to block 6.4 kV. This difference is due the position of the stack relative to the capacitor and the healthy, respectively, the faulted part of the network when the capacitor is charged to the TIV peak of 487 kV with a maximum current of 9.77 kA.

**EAP**  The varistor in the energy absorbing path has dissipate the remaining energy within 6.92 ms starting from a maximum current of 9.48 kA.

**5.3.4. Sensitivity Analysis**

In this section’s first part, the fault current margin for successful interruption is identified and the re-dimensioning for higher currents is discussed. In the second part, the sensitivity of the internal current commutation time to both a faster opening of the UFD or a smaller capacitance is investigated.

**Sensitivity to Fault Current**
Figure 5.9.: Inj-C interruption limits and prospective fault current, simple HVDC circuit \((t_{\text{fault}} = 0\, \text{ms}, U_N = 320\, \text{kV}, I_N = 2\, \text{kA}, L = 100\, \text{mH}, R_F = 0.01\, \Omega)\)

**Sensitivity of default dimensioning** As illustrated in Figure 5.9, while the first interruption limit still provides a considerable margin, the second is only 240 A above the simulated fault current at in the critical moment. When keeping the current at which the circuit breaker is signaled at 2.4 kA, the \(\frac{dI}{dt}\) must not exceed 3.3 kA ms\(^{-1}\) to ensure interruption. When keeping the rate of rise of current constant at \(\frac{dI}{dt} = 3.2\, \text{kA}\, \text{ms}\(^{-1}\)), the trip signal has to be given latest at 2.6 kA. However, in simulation, the circuit breaker is capable of interrupting the fault when the trip signal is given at 2.9 kA, and the internal current commutation time decreases by 0.01 ms to 2.8 ms. The small increase in speed is due to the shorter voltage rise time because of the higher charging current. The reason for the successful interruption is, that the negative voltage across the capacitor is overcharged to \(U_{\text{neg}} = 17.5\, \text{kV} > 16\, \text{kV}\) above the nominal rating of D.

To successfully interrupt this fault current, when the trip signal is given at 3.6 kA, the negative voltage must be at least \(U_{\text{neg}} = 19\, \text{kV}\). To maintain the desired reliability, the extension of D by one thyristor in series (six in total) is necessary. As for the previous adjustment of the fault case, the internal current commutation time decreases in comparison to the default case, by 0.07 ms. Similarly, this change is caused by the faster charging of the capacitor due to the higher current. As expected, a slightly larger thyristor stack does not affect the internal current commutation time in the default fault case (signal at 2.4 kA, \(\frac{dI}{dt} = 3.2\, \text{kA}\, \text{ms}\(^{-1}\)).

For the case of a trip signal given at 1.2 kA, using the same rate of rise of current as in the previous cases, the interruption is successful, but takes 0.09 ms longer than in the default case. As for the above cases, this is due to the voltage rise time’s dependence on the fault current.
Upgrading for higher fault currents To upgrade the Inj-C circuit breaker for higher fault currents, the capacitor pre-charge voltage ($U_{\text{pre}}$) and the threshold level for the last commutation ($U_{\text{neg}}$) have to be increased according the analytically derived formulas. As a result, additional devices have to be added in series to the thyristor stack D on the NCP to cope with the increased blocking voltage level. This leads to higher conduction losses during normal operation. For example, upgrading the interruption capability by 1 kA results in a 2 kV increase of the capacitor voltage. This merits D 6 additional thyristors (for each direction stacked 1 in series, 3 in parallel). At the nominal current of 2 kA, additional losses of 2.7 kW are caused (25%).

Breaker Speed Sensitivity

Mechanical switch opening time Assuming a UFD that opens in 1.6 ms (−20%), but without additional modifications, the internal current commutation time decreases by only 0.29 ms, 0.11 ms less than the improvement of the UFD. The reason is the simultaneously increasing voltage rise time. However, by additionally reducing the capacitor size from 15 µF to 10 µF, not only the breaker operation time reduces by 0.4 ms, but the voltage rise time decreases by 0.16 ms. This improves the internal current commutation time, compared to the default case, by 0.56 ms to 2.24 ms.

Other variables To reduce the internal current commutation time for a given fault current and the default UFD opening time, the voltage rise time must be reduced by using a smaller capacitance $C^*$. With a given stray inductance, this comes at the cost of a higher capacitor voltage and blocking capability $U_{\text{neg}}^*$, such that $U_{\text{neg}}^* \sqrt{C^*} = U_{\text{neg}} \sqrt{C}$ is fulfilled (see Equation 5.15). For an exemplary doubling of the voltage to $U_{\text{neg}}^* = 32$ kV, the capacitance can be reduced by a factor of four, i. e. about 4 µF. By doing so, the voltage rise time is reduced by 0.53 ms to 0.22 ms. However, the number of components in the thyristor stack D increases by a factor of two, doubling the normal operation conduction losses. As originally proposed in the publication [WWR+14], charging the capacitor to the TIV can already be initiated during the UFD opening, as long as the voltage always stays below the withstand voltage of gap between the UFD’s contacts during the contact separation process. For example, to reach the TIV at 2.1 ms after signaling, which is at earliest 0.8 ms after the UFD achieved full blocking capability, charging $C$ can be started 1.15 ms after the trip signal (Equation 5.17). Because of the smaller current at 1.15 ms, $U_{\text{neg}}$ must be 12 kV and the number of series connected thyristors can be reduced to 3. This modification obviously is only possible if the UFD is capable to open under voltage and if its withstand voltage as a function of opening distance and time is known precisely. As such a capability has not been published yet for an HVDC zero current switch, the default model is optimized for the trade-off of low losses and a high speed.
5.3.5. Features

Pre-activation The Inj-C circuit breaker concept allows pre-activation up to the commutation stage from TB2–TB3 to TB2–C–TB4. If no trip order is given and the circuit breaker is supposed to commutate the current back into the NCP, first the initial pre-charge voltage across the capacitor has to be restored. This can be done by beginning the commutation step TB2–TB3 to TB2–C–TB4, but interrupting it in time by turning on D.

Current limiting The Inj-C concept does not provide the current limiting feature.

Open–Close–Open An Open–Close–Open sequence can be performed immediately after the first opening, the time it takes to reclose the UFD can be bridged by closing T1 and T4. If the fault is cleared, the current is commutated back into the NCP by closing the UFD and turning on D. If the fault is not cleared, T3 is turned on, resulting in a commutation of the current into the capacitor, which is charged to the TIV level. For current interruption, the standard switching sequence now can be carried out (see Section 3.2.3).

5.3.6. Discussion

After the 2 ms it takes to open the UFD, the proposed design for the Inj-C circuit breaker concept manages to neutralize the fault and build up the TIV within 0.8 ms. This time delay is caused by the large capacitor bridging both branches of the CCP. The capacitor size and the negative voltage, to which it is charged, necessary to interrupt a specific fault current (cf. Equation 5.15), have a strong influence on the voltage rise time as well as the conduction losses during normal operation because of the increasing necessary blocking capability of the semiconductors in the NCP. Whilst a large capacitor and a smaller negative voltage results in lower losses in nominal operation due to a smaller thyristor stack D, a smaller capacitance increases the losses but reduces the internal current commutation time. The sensitivity analysis in Section 5.3.4 showed, that the UFD is the key component for time optimization, as for both, the faster opening of the UFD as well as starting to build up the TIV during the contact separation of the UFD, a significant increase in speed can be achieved. In any case, the trade-off between a fast interruption and low losses in nominal operation, and therefore the dimensioning of D and C, are highly sensitive to the maximum interruptible fault current. The featured pre-activation and Open–Close–Open capability allow the circuit breaker to fulfill more than the key requirements imposed by HVDC grids.
5.4. Inj-PG

Figure 5.10.: Functional bidirectional layout of Inj-PG (bidirectional; neither showing snubber circuits in parallel to semiconductor stacks nor stray inductances)

5.4.1. Analytical Description

The analytic description of the Inj-PG concept, as shown in Figure 5.10, had been derived in the scope of this work before the concept’s inventors published [WBMC15] during the final stage of this work. Following their publication, minor changes have been adapted, so that the presented formulas in this chapter are in accordance with the analysis of Wang et al..

Maximum Interruptible Current

The maximum interruptible current in the Inj-PG circuit breaker concept is defined by the current injected from the pulse generator along the damping branch and the VI back to the pulse generator’s capacitor and can be derived as [WBMC15]:

\[
i_{DB} = \frac{0.5 \cdot \sqrt{\frac{L_{PG}}{C_{PG}}}}{0.5 \cdot R_{DB} + R_{PG} + \sqrt{\frac{L_{PG}}{C_{PG}}}} \cdot i_{PG}
\]  

(5.20)
with the factor 0.5 arising from the current sharing between the two damping branches (one from ground to the bus-sided terminal, the other from ground to the line-sided terminal of the circuit breaker) required for bidirectional operation. With the smallest possible value for \( R_{PG} = \frac{L_{PG}}{C_{PG}} \) to ensure the turn-off of the PG semiconductor and zero damping branch resistance [Mar11], the current in the damping branches is defined as

\[
\hat{i}_{DB} = \frac{1}{4} \cdot \hat{i}_{PG},
\] (5.21)

The maximum current occurring in the pulse generator is defined by the transformation of electric energy stored in the capacitor into magnetic energy in the capacitor as

\[
\hat{i}_{PG} = \sqrt{\frac{C_{PG}}{L_{PG}}} \cdot U_N,
\] (5.22)

defined by the system voltage up to which the capacitor is charged and the dimensioning of the LC circuit. Consequently, the maximum current that can be interrupted in the VI is defined by the maximum current in the damping branch, using the smallest possible \( R_{PG} \):

\[
\hat{i}_{DB} = \frac{1}{4} \cdot \hat{i}_{PG}.
\] (5.23)

Employing a resistance in the damping branch has two purposes, (1) the overall resistance for the energy dissipation in the EAP is increased by \( R_{DB} \) and (2) the overshoot of the injected pulse \( \hat{i}_{DB} \) over the fault current in the VI and the resulting \( \frac{dI}{dt} \) can be adjusted.

To prevent a current leaking through the damping branches in case of a pole-to-ground fault, the employment of non-linear resistors, i.e. an MOV, is preferred to ohmic resistors for bipolar networks [WBMC15]. A non-linear behavior however has to be respected in Equation 5.20.

**Internal Current Commutation Time**

The internal current commutation time is approximately

\[
\Delta t_{CC} = \Delta t_{VI\text{-opening}} + \Delta t_{I_{DB, peak}} + \Delta t_{C,TIV}
\] (5.24)

As reasoned in [WBMC15], the delay from triggering the PG semiconductors to the peak of the damping branch current is approximately twice the rise time of the current in the pulse generator. The pulse generator rise time is defined as the time from zero to maximum current in the pulse generator, occurring when the capacitor is discharged. Because of the rectifying semiconductors, the damping branches only start conducting after a reversal of the capacitor voltage and with increasing voltage in opposite direction, the current through the damping branches increases almost
similarly to the earlier generated current in the pulse generator:

$$\Delta t_{DB,peak} = 2 \cdot \Delta t_{PG} = 2 \cdot \frac{\pi}{2} \cdot \sqrt{C_{PG} L_{PG}}. \quad (5.25)$$

The VI opens the NCP latest at the moment of $I_{DB,peak}$ and subsequently redirects the fault current onto the capacitor. Therefore the time for charging the capacitor is obtained from

$$U_{TIV} = \frac{1}{C} \int_{t_{IDB,peak}}^{t_{IDB,peak} + \Delta t_{c,TIV}} i(\tau) \, d\tau, \quad (5.26)$$

with $t_{IDB,peak} = t_{trip} + \Delta t_{VI opening} + \Delta t_{IDB,peak}$. When using MOV in the damping branch, as discussed in the previous chapter, the clamping voltage level increases accordingly and so does the voltage rise time. Furthermore, a larger MOV will delay the injection of the damping branch current because the damping branches only start conducting after the reverse capacitor voltage has exceed their clamping level.

### 5.4.2. Implemented Circuit Breaker Model

The implemented model is of the circuit breaker is mainly based on the design and test results published in [GV11, Mar11, WM13, WM14, WBMC15] which aims at fast operation for a similar fault current.

**NCP** Two mechanical switches are required in the NCP for bidirectional operation [Mar11]. Both have to separate their contacts under load, and, due to the bidirectional operation, each has to be able to withstand the TIV, which is defined by the EAP’s clamping voltage. $8 \times 40.5\, \text{kV}$ VIs are connected in series to fulfill this requirement. The voltage distribution is assumed to be homogeneous.

**CCP** The first functional branch of the CCP is the pulse generator. For the pulse generator, the proposed dimensions of series connected $30\, \text{kV}$ modules [WM14] are scaled up to one single $320\, \text{kV}$ unit. To withstand the TIV, the turn-off semiconductor PG consists of a stack of 75 series connected thyristors with RCD snubbers. As a result of the upscaling, the overall inductance in the pulse generator results in $156.7\, \mu\text{H}$. Subtracting the branches stray inductance of approximately $50\, \mu\text{H}$, primarily due to the semiconductor stack, a $106.7\, \mu\text{H}$ inductance is required in the pulse generator. To maintain the same pulse duration and peak current in the pulse generator, as proposed, a capacitor of $6.56\, \mu\text{F}$ is required. The pulse generator is only upscaled to simplify the model, in practice a modular design is preferred, for simple adjustment for different system voltages and because of the reduced insulation requirements for each of the series connected modules, e.g. several high-capacitive capacitors with smaller voltage ratings instead of one single capacitor of small capacitance rated for the EAP overall clamping voltage level. The diode stack consists of conservative 144 units to withstand the TIV. Because of
the additional resistance of the damping branch MOV. $R_{PG}$ is set to $4\Omega$, $0.8\Omega$ below the earlier explained minimum value.

In the damping branches, MOVs with a clamping voltage level of 60 kV are connected in series with diode stacks of the same rating as the previously described stack. The rating of the MOV is set to keep the overshoot of the injected current over the prospective fault current below 50% to avoid very high $\frac{di}{dt}$ in the VIIs while at the same time keeping the EAP clamping voltage close to the default of 480 kV to maintain comparability with the other investigated solution.

An inductor, connected between $R_{PG}$ and the pulse generator, accounts for the parasitic inductance into the current path during the second commutation stage.

To allow the injected current to return to $C_{PG}$ after the arc in the VI is extinguished, diode stacks of 144 series connected units are implemented in parallel to the VI, conducting in opposite direction of the interrupted fault current.

**EAP** The EAP consists of two parts. First, an MOV and a stray inductance, which are connected in parallel to $R_{PG}$ and $C_{PG}$. This MOV must limit the current to the leakage level, when nominal voltage is applied, and is dimensioned for a clamping voltage level of 480 kV. Second, the respective damping branch connected to the faulty side of the network with a 30 kV MOV.

Due to the series connection of the two MOV, the TIV peak reaches 540 kV and exceeds the other circuit breakers’ peaks by 60 kV.

### 5.4.3. Simulation Results

As shown in Figure 5.11, immediately after the VI has finished opening, the pulse generator is fired. Subsequently, currents are injected through both damping branches, and the current $i_{DB}$ injected in opposite direction of the fault current extinguishes the arc in the fault-sided VI whereas the current in direction of the fault current leads to a current increase in the VI on systems healthy side. The injected current exceeds the fault current in the VI by more than 5 kA and commutates into the parallel diode after arc extinguishing to charge the pulse generator capacitor again. Subsequently to the interruption the voltage across the breaker rises to 540 kV as predicted, due to the commutated fault current.

**Operation Speed and Maximum Current**

The total measured break time is 8.26 ms. The simulation results in a breaker operation time of 2.62 ms and a voltage rise time of 0.32 ms, hence the internal current commutation time sums up to $\Delta t_{CC} = 2.94$ ms. The predictions for $\Delta t_{DB,\text{peak}} = 0.1$ ms as well as for the charging of the capacitor $\Delta t_{C,TIV} = 0.33$ ms are acceptable 0.01 ms to 0.02 ms deviation to the simulation results.

The time difference between the current and the voltage peak is 0.05 ms, due to the capacitor size and the high TIV.
Figure 5.11.: Inj-PG path currents and circuit breaker voltage, simple HVDC circuit 
($t_{fault} = 0\,\text{ms}, \, U_N = 320\,\text{kV}, \, I_N = 2\,\text{kA}, \, L = 100\,\text{mH}, \, R_F = 0.01\,\Omega$)

The maximum current, which can be extinguished in the VI 2.6 ms after the trip signal, is 16.6 kA. Because of the damping branches non-linear resistance, this limit even slightly above the approximately predicted maximum of $\frac{1}{4}i_{PG} = 16.1\,\text{kA}$, defined by the maximum current in the pulse generator $\dot{i}_{PG} = 64.3\,\text{kA}$.

Stress on Components

NCP  Whilst the VI on the healthy side of the circuit only is required to carry a high surge current of 28.92 kA, the VI on the faulted side has to extinguish the arc at zero current. The maximum current through the latter VI rises to 10.56 kA before the pulse is injected. At the moment of current zero, the rate of rise of current in the the VI is $\frac{dI}{dt} = 625\,\text{A}\,\mu\text{s}^{-1}$ and the following rate of rise per 40.5 kV vacuum interrupter is $\frac{dU_{TIV}}{dt} = 208\,\text{V}\,\mu\text{s}^{-1}$, calculated from the maximum TIV of 542 kV and the voltage rise time.

The interruption in the VI is assumed to be successful, because the resulting $\varepsilon = \frac{dU_{TIV}}{dt} \cdot \frac{dI}{dt} = 130.6\,\text{kVA}\,\mu\text{s}^{-2}$ is below the reported maximum value of $140\,\text{kVA}\,\mu\text{s}^{-2}$ [Sla08].
The diodes in the CCP are exposed to maximum currents of 5.7 kA to 34.6 kA with maximum rates of rise of 1 A µs⁻¹ to 2.2 A µs⁻¹, but as the high currents are surge currents during the current injection phase, these are not considered critical ($I_{FSM} \geq 110$ kA for pulses of 10 ms). For all diodes, the $\frac{dU}{dt}$ is below 1.6 kV µs⁻¹ after switching to blocking mode. For the diode parallel to the VI on the faulty side and the adjacent damping branch diode, relatively high maximum voltage level of 3766 V and 3349 V, respectively, are observed. These maximum values occur when the TIV peak across the circuit breaker is reached. As the diode’s maximum blocking capability is 5 kV, about 30 percent above the observed peaks, additional diodes can be connected in series to provide higher reliability and redundancy.

The thyristor PG, which triggers the pulse generator, operates at a maximum surge current of $i_{PG} = 64.3$ kA with a maximum $\frac{di}{dt}$ of 3 kA ms⁻¹. As reported by [WM14], whose dimensioning was adopted for the pulse generator, these stresses can be handled without difficulty.

For a modular pulse generator, in which the voltage is shared across several modules, the same statement holds for the stresses on the inductor and capacitor in the pulse generator, which have to operate at the same peak current level.

5.4.4. Sensitivity Analysis

In this section, the Inj-PG’s sensitivity to different currents and to adjustments of components is discussed. First, the fault current margin for successful interruption is identified and the re-dimensioning for higher currents as well as the circuit breakers most current-sensitive components are discussed. In the second part, the sensitivity of the internal current commutation time to a faster opening of the VI is investigated.

Sensitivity to Fault Current

Sensitivity of default dimensioning As illustrated in Figure 5.12, the Inj-PG’s maximum interruptible current exceeds the default fault current by 5.8 kA, which is the only fault current limitation during the interruption process. Consequently, assuming the default $\frac{di}{dt}$, a trip signal must be given at latest at a current of 8.2 kA. For a detection and signaling at 2.4 kA interruption is successful for a rate of rise of current up to 5.4 kA ms⁻¹.

This observation makes it obvious, that in both investigated cases of a 0.5 kA and a 1.2 kA higher current in the moment of the trip signal, interruption is successful without any modifications needed. As expected, the measured internal current commutation time decreases by 0.01 ms and 0.03 ms, respectively, compared to the default trip threshold, because of the shorter voltage rise time due to the higher fault current level.
Figure 5.12.: Inj-PG interruption limits and prospective fault current, simple HVDC circuit 
\( t_{\text{fault}} = 0 \, \text{ms}, U_N = 320 \, \text{kV}, I_N = 2 \, \text{kA}, L = 100 \, \text{mH}, R_F = 0.01 \, \Omega \)

For the case of a smaller nominal current with the trip signal given at 1.2 kA, the charging of the capacitor up to the TIV takes 0.04 ms longer. Based on the \( \varepsilon = 118.4 \, \text{kVA} / \mu \text{s}^2 \), the VI can interrupt the fault current in this case too. The calculated \( \varepsilon \) is smaller than in the default case, as \( \frac{dU}{dt} = 630 \, \text{A} / \mu \text{s} \) is only slightly larger whilst the \( \frac{dI_{\text{TIV}}}{dt} = 188 \, \text{V} / \mu \text{s} \) is smaller, because of the longer voltage rise time.

**Upgrading for higher fault currents** To achieve the interruption of higher fault current, only the MOV in the damping branch has to be reduced. To increase the interruption capability by 1 kA, the MOV rating has to be decreased to 25 kV. Because EAP rating decreases at the same time, the fault current suppression time will increase (for interruption of the default case by 0.27 ms).
The Inj-PG circuit breaker was proposed and tested in the modular design with a specific component dimensioning. Individually adjusting the inductor and capacitor in the pulse generator is not elaborated in detail in the scope of this work, because such a realization of the circuit breaker concept would loose the advantage of a modular pulse generator, that it can be used for a wide range of system voltages and fault currents.

**Breaker Speed Sensitivity**

**Mechanical switch opening time** For a 20% faster opening of the VI (from 2.5 ms to 2 ms\(^2\)) a breaker with the default dimensioning is capable to interrupt the fault

\(^2\)As the VI have to open under load, they are assumed to open slower than the UFD solution.
current with a
\[ \varepsilon = \frac{dI_{cz}}{dt} \cdot \frac{dU_{TIV}}{dt} = 642 \, \text{A/µs} \cdot 182 \, \text{V/µs} = 116.9 \, \text{kVA/µs}^2, \] (5.27)
which is still below the mentioned limit. The internal current commutation time improves by 0.45 ms to 2.49 ms, almost the improvement of the mechanical opening mechanism, while the voltage rise time increases by 0.05 ms.

**Other variables** For the Inj-PG circuit breaker concept, no further variables are varied, as the proposed pulse generator dimensions already were discussed and tested in previous works.

### 5.4.5. Features

**Pre-activation** By opening the VI as soon as a fault is detected locally, pre-activation is possible. Due to the use of circuit breakers rather than disconnectors in the nominal path, no commutation process has to be performed first. Hence, the mechanical device can be operated immediately. If a trip signal is given, the pulse generator is fired as soon as the VI has opened. If no trip signal is received, the VI is closing under load again.

**Current limiting** The Inj-PG concept does not provide a current limiting functionality.

**Open–Close–Open** To allow an Open–Close–Open sequence, the circuit breaker has to fulfill two requirements. First, the VI must be capable to close with the system voltage across its terminals and must endure the inrush current, but according to the current making capability given in datasheets, this is no critical constraint. Second, before closing and re-opening, \( C_{PG} \), charged to the TIV during the interruption process, must be discharged to the system voltage quickly. This may require an additional fast discharge unit, e.g. a TSG with a resistor, in parallel to the capacitor. For a modular pulse generator, each module has to be equipped with a discharge unit.

### 5.4.6. Discussion

When the contacts of the VIs reached the required distance 2.5 ms after the trip signal, a pulse of above 16 kA is injected to commutate the current out of the NCP to the pulse generator capacitor which is charged to the TIV peak. Whilst the time until pulse injection is independent of the fault current, the voltage rise time depends on the fault current and is in the range of a few hundred microseconds for the simulated fault case. Even though a relatively high current is injected into the VI, the resulting \( \frac{dI_{cz}}{dt} \) does not impose difficulties for the VI current breaking of neither small nor large fault currents, due to the sufficiently slow voltage rise time.
The components of the pulse generator are exposed to a high surge current of 60 kA, but as test have shown, these stresses are not critical [WM14]. A faster fault current suppression time can be achieved by increasing the clamping voltage of the MOV in the damping branches, but such an adjustment comes at the cost of a higher blocking capability of the VI and the parallel connected diode stacks. Upgrading the Inj-PG circuit breaker for higher fault currents is simply realized by reducing the aforementioned rating of the damping branch MOV up to approximately 20 kA (no damping branch MOV). For even higher currents, re-dimensioning the pulse generator has to be considered. To achieve a faster internal current commutation time, improving the opening mechanism of the VI is expected to be most efficient. Even though the investigated Inj-PG design only offers pre-activation but no further features, it is capable to interrupt relatively high currents in comparison to most of the other investigated solutions below 3 ms and fulfills the key requirements for HVDC circuit breakers.
5.5. Inj-LC

![Functional bidirectional layout of Inj-LC (without stray inductances)](image)

**Figure 5.13.:** Functional bidirectional layout of Inj-LC (without stray inductances)

### 5.5.1. Analytical Description

**Maximum Interruptible Current**

The maximum interruptible current is defined by the first peak of the oscillation, which is triggered as soon as the VI has opened completely.

The capacitor in the CCP branch is charged to the system voltage $U_N$. Consequently, the peak current of the injected oscillation can be approximated by the conversion of the electric energy in the capacitor into magnetic energy in the inductor

$$\hat{i}_{inj} = U_N \cdot \sqrt{\frac{C}{L}}. \quad (5.28)$$

Damping through the resistance of the arc in the VI is assumed to be relatively small and is neglected in this equation.

Furthermore, the interruption capability of the VI imposes a limit on the $\frac{dI}{dt}$ in the NCP at current zero, hence limiting the injected current. The rate of rise of current in the VI $\frac{dI_{ez}}{dt}$ is calculated by the difference of the rate of rise of the prospective fault current $i$ and the rate of rise of the counter-injected current pulse $i_{inj}$ at the moment of current zero in the VI $t_{ez}$.

$$\frac{dI_{ez}}{dt} = \frac{dI}{dt} - \frac{\hat{i}_{inj}}{\sqrt{LC}} \cdot \cos \left( \arcsin \left( \frac{I(t_{ez})}{\hat{i}_{inj}} \right) \right) \quad (5.29)$$
For the VI specific $\varepsilon$, the rate of rise of voltage after current zero for the VI can be approximated by the following formula:

$$\frac{dU_{TIV}}{dt} \approx \frac{U_{TIV}}{\Delta t_{C,TIV}} \tag{5.30}$$

with $\Delta t_{C,TIV}$ explained in the next paragraph.

**Internal Current Commutation Time**

The internal current commutation is the sum of the VI opening time, the time delay from triggering the pulse injection until the arc in the VI is extinguished and the time required to charge the CCP capacitor to the TIV level. This can be approximated by

$$\Delta t_{CC} = \Delta t_{Vopening} + \Delta t_{ez} + \Delta t_{C,TIV} \tag{5.31}$$

with $\Delta t_{Vopening}$ given by the VI’s parameters. For a high frequency pulse, with $\frac{1}{2\pi\sqrt{LC}} > 10$ kHz, the delay until arc extinction can be approximated by $\Delta t_{ez} \approx \frac{\pi}{2} \sqrt{LC}$. The time until the capacitor voltage reaches the TIV peak is calculated from

$$U_{TIV} = \frac{1}{C} \int_{t_{ez}}^{t_{ez} + \Delta t_{C,TIV}} i(\tau) d\tau, \tag{5.32}$$

with $t_{ez} = \Delta t_{Vopening} + \Delta t_{ez}$.

**5.5.2. Implemented Circuit Breaker Model**

The dimensions of the Inj-LC circuit breaker model are based on [SZJ+15], whose proposed values were approximately scaled up for 320 kV. [SZJ+15] is chosen as a reference as this group has already performed extensive research on the Inj-LC concept [SJM+10, ZSJ+14], also covering the VI and the TSG. The implemented bidirectional topology, illustrated in Figure 5.13 is similar to the one presented in Chapter 3.

**NCP** In the NCP, solely the default VI set of 8 series connected units is used.

**CCP** The CCP is a series connection of a triggered spark gap, which allows immediate turn on, an inductor of 375 $\mu$H and a capacitor of 0.6 $\mu$F and the default stray inductance. The resonant circuit is dimensioned to reach a peak value of approximately $\hat{i}_{inj} = 12$ kA and an oscillation frequency of 10 kHz as proposed. The combination of this high frequency and the small capacitor is not dimensioned to meet the proposed VI limits ([Sla08]), but since the authors of the adopted dimensions have investigated VIs to some extent as well, a successful interruption at the first current zero crossing is assumed. An alternative dimensioning is proposed later in this chapter.
In the EAP, the default MOV, rated for 240 kV, which corresponds to a clamping voltage of 480 kV, is connected in series with the stray inductance.

### 5.5.3. Simulation Results

![Figure 5.14. Inj-LC path currents and circuit breaker voltage, simple HVDC circuit (\(t_{\text{fault}} = 0\) ms, \(U_N = 320\) kV, \(I_N = 2\) kA, \(L = 100\) mH, \(R_F = 0.01\) Ω)](image)

In Figure 5.14, the currents in the functional paths as well as the voltage across the circuit breaker are shown. The interruption of the current in the NCP, which happens shortly after the VI opening is completed, takes place around 2.5 ms after the trip signal.

Furthermore, a strong oscillation of a current of approximately 8 kA is observed between the CCP and the EAP. As explained in [SZJ+15], this oscillation occurs because the TSG is not capable to extinguish the arc by itself. Due to the resistance of the MOV the current and voltage oscillations are damped and disappear after approximately 5 ms.

**Operation Speed and Maximum Current**

The Inj-LC circuit breaker needs a break time of 9.82 ms to bring the fault current to the leakage current level. The breaker operation time is 2.53 ms. Due to the short voltage rise time of 29 μs, the time delay between the current and TIV peak is a few microseconds and therefore negligible.

The analytically predicted internal current commutation time differs from the simulation result by 0.01 ms. This offset is mainly because the estimate of the time to charge
the capacitor to TIV does not account for the remaining charge on the capacitor if the arc is extinguished before the peak of the injected current, which happens for all but the fault current that are approximately equal to the peak of the injected current:

\[ \Delta t_{CC,sim} = \Delta t_{VIopening} + \Delta t_{cz} + \Delta t_{C,TIV} \]
\[ = 2.5 \text{ ms} + 0.017 \text{ ms} + 0.027 \text{ ms} = 2.55 \text{ ms} \] (5.33)
\[ \Delta t_{CC,ana} = 2.5 \text{ ms} + 0.017 \text{ ms} + 0.044 \text{ ms} = 2.56 \text{ ms} \] (5.34)

The maximum current peak of the first current pulse in the simulation equals the calculated 12.02 kA.

**Stress on Components**

**NCP** In the VI, a maximum current of 10.39 kA is observed before the current is interrupted. At the moment of arc extinction, \( \frac{dU}{dt} = 380 \text{ A/µs} \) is measured. In combination with a rate of rise of voltage per VI unit of \( \frac{dU}{dt} = 2.06 \text{ kV/µs} \) an \( \varepsilon = \frac{dU_{TIV}}{dt} \cdot \frac{dI_{cz}}{dt} = 782.8 \text{ kVA/µs}^2 \) results. This value exceeds the maximum reported value of 140 kVA/µs² by far, and therefore is likely to cause a re-ignition of the arc [Sla08]. Assuming a successful arc extinction, a maximum voltage across the VI of 510 kV is measured, after the commutation of the current into the CCP, which is caused by the previously described oscillation of the current between CCP and EAP.

**CCP** In the CCP, the maximum current in the components is 10.51 kA, which is necessary to extinguish the arc in the VI. The voltage across the capacitor rises with up to 17.5 kV/µs⁻¹ up to a voltage of 742.9 kV. This high voltage across the capacitors is an effect of the oscillation between the CCP and the EAP and is not directly applied across the circuit breaker terminals, as the inductor is energized at this instant and maintains a voltage of opposite direction.

**EAP** Due to the oscillation, a maximum current of 19.41 kA is measured in the MOV. This oscillation is damped within 5 ms after its occurrence. The MOV in the EAP requires in total 7.26 ms until the leakage current level is reached.

### 5.5.4. Sensitivity Analysis

In this section, the Inj-LC’s sensitivity to different currents and to adjustments of components is discussed. First, the fault current margin for successful interruption is identified and the re-dimensioning for higher currents as well as the circuit breakers most current-sensitive components are discussed. A formula to achieve successful current breaking in the VI is presented. Second, the sensitivity of the internal current commutation time to a faster opening of the VI is investigated.

**Sensitivity to Fault Current**
Sensitivity of default dimensioning As can be seen in Figure 5.15, the maximum interruptible current is 1.54 kA larger than the prospective fault current. For $\frac{df}{dt} = 3.2$ kA ms$^{-1}$, the trip signal has to be given before the fault current reaches 3.9 kA. Assuming a trip signal at 2.4 kV a current with a maximum rate of rise of 4.25 kA ms$^{-1}$ can be interrupted. Based on this results, it is clear that the tripping current level by 0.5 kA and 1.2 kA does not merit adjustments in terms of maximum interruptible current. For both cases, no change in the internal current commutation time ($\Delta t < 10$ µs) is observed. The $\frac{dl}{dt}$ decreases to 311 A µs$^{-1}$ and 186 A µs$^{-1}$, respectively, whilst the $\frac{dU_{TIV}}{dt}$ per unit increases to 2.28 V µs$^{-1}$ and 2.43 V µs$^{-1}$, respectively. Nevertheless, the $\varepsilon$ values of 709 kVA/µs$^2$ and 452 kVA/µs$^2$ still exceed the published VI capabilities, hence an interruption during the first current zero crossing is unlikely. When a smaller nominal current has to be interrupted, with the trip signal given at 1.2 kA, still no change in the internal current commutation time is observed. The obtained $\varepsilon = 479$ A µs$^{-1} \cdot 1.93$ V µs$^{-1} = 909$ kVA/µs$^2$ is larger than the previous values, since the injected current is basically independent from the trigger level, and a successful interruption is more unlikely.

Upgrading for higher fault currents To upgrade the Inj-LC circuit breaker design to interrupt a fault current higher than the interruption limit of the default breaker, the capacitance and the inductance have to be adjusted. Based on the previous findings, it is desirable to decrease the $\frac{dl}{dt}$ and $\frac{dU_{TIV}}{dt}$ to improve the conditions for the VI to interrupt the current at zero crossing. With reference to the default dimensioning,
this is best achieved by increasing the small capacitor and the large inductor to both increase the voltage rise time and reduce the frequency for a smaller $\frac{di_{cz}}{dt}$.

For the exemplary increase of the interruption capability by 1 kA, the capacitor has at least to be increased by 0.1 µF. When interrupting a current 1 kA larger than the default fault case, $\varepsilon$ is 726 kVA/µs² and the voltage rise time is 29 µs. For $C = 1$ µF and $L = 600$ µH, $\varepsilon$ is reduced to 367 kVA/µs² but the voltage rise time increase to 42 µs at the same time.

By using the initially derived formulas, an LC design that meets a desired $\varepsilon$ value can be derived by

$$\varepsilon \geq \frac{i_{inj}^2}{U_N \cdot C} \cdot \cos \left( \arcsin \left( \frac{i(t_{cz})}{i_{inj}} \right) \right) \times \frac{\Delta t_{C,TIV}}{8 \cdot TIV}$$  \hspace{1cm} (5.36)

Setting $L = 970$ µH and $C = 1.6$ µF, a breaker operation time of 2.56 ms and a voltage rise time of 0.07 ms is measured for the fault current trip signal given at 3.4 kA, and the $\varepsilon$ resulting from the simulation equals the intended 140 kVA/µs².

### Breaker Speed Sensitivity

**Mechanical switch opening time**  Provided a VI that can open within 2 ms, the LC circuit can be re-dimensioned for the smaller fault current of 8.8 kA to a maximum interruptible current of 10 kA (to cause 10 % to 20 % overshoot [Ska13]). To furthermore ease the VI operation, the formula presented in the previous section is applied. The obtained values for $L = 1125$ µH and $C = 1.1$ µF result in $\varepsilon = 121$ kVA/µs², a breaker operation time of 2.06 ms and a voltage rise time of 0.06 ms.

**Other variables**  The internal current commutation time of the initially proposed dimensioning exceeds the VI opening time by 0.06 ms. Thereof, 0.04 ms are required for charging the capacitor, and consequently this is the only variable which allows increasing the breaker speed. For the previously discussed negative effect of a smaller capacitor on the VI operation and the negligible speed improvement potential, this option is not investigated further.

### 5.5.5. Features

**Pre-activation**  The Inj-LC concept features pre-activation by opening the VI as soon as a fault is detected locally, since the breaker can cope with the fault current for a certain time. Subsequently, given the VI has opened, only the TSG has to be activated. If no trip signal is received, the VI is closing under load again.

**Current limiting**  For this circuit breaker, no current limiting functionality is available.
5.5 Inj-LC

**Open–Close–Open** To fulfill the Open–Close–Open feature, the same requirements as for the Inj-PG circuit breaker have to be fulfilled: The VI must provide the required current making capability and discharging the capacitor from the TIV level to a lower voltage might be necessary to reduce the overshoot of the injected current and hence the burden for the VI to interrupt. The discharging may require additional switches in combination with a low-ohmic connection to ground and discharge resistors.

5.5.6. Discussion

The proposed dimensioning of the Inj-LC circuit breaker, based on the [SZJ+15], operates very close to the mechanical opening of the VI and builds up the TIV only 0.06 ms after the required distance between the VI contacts is reached. Additionally, its maximum interruptible current provides a margin of 1.5 kA. However, the investigated dimensioning causes a very high ε in the VI for all investigated fault currents, making a successful extinction of the arc during the current zero crossing with very questionable. Since it is unsuitable to add parallel VI stacks to reduce the \( \frac{dI}{dt} \), a re-dimensioning of the CCP is suggested.

For a more reliable operation a dimensioning, which injects a pulse with a lower frequency and a higher voltage rise time, achieved with a larger capacitor and inductor, is recommended. However, as the referenced authors already investigated VIs to some extent, and since the re-dimensioning of the circuit breaker has almost no influence on the total interruption time (0.07 ms), the grid study is conducted with the default dimensioning, assuming a successful interruption at the first current zero crossing.
5.6. Osc-ES

![Functional bidirectional layout of Osc-ES](image)

Figure 5.16: Functional bidirectional layout of Osc-ES (greyed out components are activated only for breaking fault currents from right to left, without stray induc-tances)

5.6.1. Analytical Description

Maximum Interruptible Current

The maximum interruptible current is defined by the amplitude of the LC current due to the conversion of the electrical energy stored on the capacitor into magnetic energy in the inductor of the LC-circuit formed by the CCP with the NCP. The principle is similar to the passive resonance principle, only that a semiconductor switch is added, which replaces the arc for exciting the oscillation, to create an earlier current zero crossing.

By an initial blocking of the ES after the trip signal, the LC circuit is excited. This happens, because the fault current, now flowing through the MOV in parallel to the commutation switch ES, creates a considerable voltage drop over the NCP. This makes a part of the fault current commutate into the CCP, energizing both $L$ and $C$. The energy transfer occurs by balancing the path’s voltage drops $U_L + U_C = U_{ES}$ with $U_{ES}$ approximately equal to the MOV’s clamping voltage. As soon as the capacitor voltage is close to $U_{ES}$, the current in the CCP becomes zero and the ES is turned on again. The capacitor now discharges, leading to a current in opposite direction. In the moment of current zero in the LC path, immediately before turning the ES back on, the voltage across $L$ is stepped up by $U_{ES}$ and further energy is transferred into the LC circuit.

Each period more energy is injected into the LC circuit by turning the ES off for half the period. When turned off, the ES acts as a voltage source for the resonant circuit of approximately the MOV’s clamping voltage, which increases the capacitor peak voltage by $2 \cdot U_{ES}$ each period.

The amplitude of the LC current grows proportional to the voltage across the inductor.
For the VI to break the fault current, the injected current has to be of opposite direction. Consequently, the maximum interruptible current in period \( j \) is defined as

\[
\hat{i}_{LC,j} = (2j - 1) \cdot U_{ES} \cdot \sqrt{\frac{C}{L}}.
\] (5.37)

These peaks occur at

\[
t_j = \frac{T_{LC}}{4} + (j - 1) \cdot T_{LC} = \left( j - \frac{3}{4} \right) \cdot 2\pi \sqrt{LC}
\] (5.38)

The average increase of the maximum interruptible current from the initial trigger signal at \( t_{LC} = 0 \) can consequently be described by

\[
\hat{i}_{LC}(t_{LC}) = U_{ES} \left( \frac{t_{LC}}{\pi L} + 0.5 \sqrt{\frac{C}{L}} \right)
\] (5.39)

Which allows estimating the maximum interruptible current at a specific time, which obviously is only relevant after the VI has opened.

According to the above equation, the maximum interruptible current is theoretically unlimited with time. In practice, voltage drop along the ES damps the oscillation with increasing current, and capacitor voltage should not exceed its rating, in the range of \( 1.5 \cdot U_N \).

The overshoot of the injected current over the fault current can be controlled by decreasing the ES switching frequency from the LC eigenfrequency, once the desired off-set is achieved \([Ska13]\). This ensures safely interruptible \( \frac{dI}{dt} \) in the VI.

**Internal Current Commutation Time**

The internal current commutation time can be described by

\[
\Delta t_{CC} = \Delta t_{VI\text{opening}} + \Delta t_{cz} + \Delta t_{C,TIV}
\] (5.40)

The VI’s properties provide \( \Delta t_{VI\text{opening}} \). Assuming that the circuit breaker is dimensioned in a way so that the first pulse after the VI opening exceeds the rated fault current, the delay \( \Delta t_{cz} \) until arc extinguishing, a function of the frequency of the oscillation, is obtained from

\[
\Delta t_{cz} = p \cdot 2\pi \sqrt{LC} - \Delta t_{VI\text{opening}}
\] (5.41)

with \( p \) the number of oscillations obtained from \( \min_p \left( p \cdot 2\pi \sqrt{LC} \geq \Delta t_{VI\text{opening}} \right) \).

The time until the capacitor voltage reaches the TIV peak is calculated from

\[
TIV = \frac{1}{C} \int_{t_{cz}}^{t_{cz}+\Delta t_{C,TIV}} i(\tau) d\tau,
\] (5.42)
with \( t_{cz} = \Delta t_{\text{Vopening}} + \Delta t_{cz} = p \cdot 2\pi \sqrt{LC} \).

### 5.6.2. Implemented Circuit Breaker Model

The dimensions of the implemented bidirectional Osc-ES circuit breaker model, as shown in Figure 5.16, are adopted from the published information [Ska13].

#### NCP
In the NCP 8 × 40.5 kV stack of VIIs, each with a constant arcing voltage of 30 V, is connected in series with the ES. The ES consists of a 3 × 3 IGBT stack, but in difference to the LCS, no snubber but an MOV, rated for 5 kV and consequently clamping at around 10 kV, as proposed in [Ska13], is connected in parallel to achieve the intended growth of the current oscillation.

#### CCP
In the CCP, a capacitor of 1 µF, to allow a short voltage rise time, an inductor of 600 µH and the default stray inductance of 50 µH are connected in series. The stray inductance is not subtracted from the proposed inductor [Ska13] to reduce both the switching frequency and the \( \frac{di}{dt} \) as well as the resulting stress on the ES and the VI, respectively. The resulting series LC circuit’s eigenfrequency is 6.25 kHz.

#### EAP
In the EAP, the default MOV, rated for 240 kV, which corresponds to a clamping voltage of 480 kV, is connected in series with the stray inductance.

### 5.6.3. Simulation Results

In Figure 5.17, the circuit breaker’s characteristic voltage and current curves are shown for the default fault case. The oscillation of the LC circuit, which is excited immediately after the fault detection, increases within 2.5 ms to approximately 10 kA. A light decrease in the rate of rise of the oscillation amplitude is observed. Shortly after the VI opened, the fault current is first commutated into the CCP path and then into the EAP. The oscillation of the current continues for another 6 ms between the CCP and the EAP. The TIV also shows some oscillation around its peak value, however these have a relatively small amplitude compared to the TIV peak.

**Operation Speed and Maximum Current**

In the default case, an overall break time of 10.01 ms was measured, consisting of 2.61 ms breaker operation time, 0.05 ms voltage rise time and a fault suppression time of 7.35 ms. The time difference between the occurrence of peaks of current and TIV is negligible small (< 5 µs). As calculated, delay of the first pulse peak to be injected into the opened VI is 0.1 ms. The calculated \( \Delta t_{C,TIV} \) of 45 µs is 8 µs shorter than in the simulation. This is not surprising, because the calculated value does not account for a remaining negative charge in the capacitor when the VI arc is extinguished already before the peak of \( i_{LC} \).
The maximum current which the first pulse after VI opening can get to zero is 10.7 kA. This value is significantly below the expected peak of 12.94 kA. As can be seen in Table 5.1, the difference between the expected value and the simulation result increases over time. This is because the ES MOV voltage is slightly smaller than the expected clamping voltage, due to the non-linear characteristic of the MOV. Higher fault currents through the ES on the other hand cause a higher voltage drop along the ES because of the MOV U-I characteristic.

From Table 5.1 it can also be seen, that even after the first relevant pulse, the amplitude increases up 14.26 kA, 3.73 ms after the trip signal. This means the circuit breaker is capable of interrupting fault currents higher than the 10.7 kA of the first current pulse after VI opening if the rate of rise of the fault current is lower than the one of the divergent oscillation.

**Stress on Components**

**NCP** In the NCP, the ES IGBTs have to carry a maximum current of 6946 kA at the moment the last pulse, before arc extinction, which is well below the limit of 32 kA for a surge of 10 ms, specified in the datasheet. The IGBTs are required to block voltages up to 3329 kV per device and operate at high rates of rise of current and voltage of 7258 A μs⁻¹ and 6647 V μs⁻¹, which, even though no limits are specified in datasheets, likely have to be compensated by adequate snubber circuits. The turn on always has to be performed under voltage, close to $U_{MOV,ES}$, and when turning off, the instantaneous fault current has to be chopped. These requirements together with the switching frequency of 6.25 kHz cause considerable stress onto the ES. In contrast
Table 5.1.: Osc-ES: Comparison of calculated and simulated LC current peaks

<table>
<thead>
<tr>
<th>Pulse</th>
<th>Calculation</th>
<th>Simulation</th>
<th>Relative error</th>
</tr>
</thead>
<tbody>
<tr>
<td>j</td>
<td>̇i_{LC,j}</td>
<td>t_j</td>
<td>̇i_{LC,j}</td>
</tr>
<tr>
<td>1</td>
<td>0.04 ms</td>
<td>0.49 kA</td>
<td>0.04 ms</td>
</tr>
<tr>
<td>2</td>
<td>0.20 ms</td>
<td>1.18 kA</td>
<td>0.20 ms</td>
</tr>
<tr>
<td>3</td>
<td>0.36 ms</td>
<td>1.96 kA</td>
<td>0.36 ms</td>
</tr>
<tr>
<td>17</td>
<td>2.60 ms</td>
<td>10.70 kA</td>
<td>2.60 ms</td>
</tr>
<tr>
<td>20</td>
<td>3.08 ms</td>
<td>15.30 kA</td>
<td>3.08 ms</td>
</tr>
<tr>
<td>24</td>
<td>3.72 ms</td>
<td>18.43 kA</td>
<td>3.72 ms</td>
</tr>
</tbody>
</table>

to the other breaker concepts, the IGBTs have to perform more than 10 switching operations at a high frequency instead of only one, resulting in increased switching losses, which have to be considered when designing the IGBT stack.

The VI has to carry the same maximum current of 20.84 kA as the three parallel IGBT. The rate of rise of current in the moment of arc extinction at current zero is \( \frac{di_{cz}}{dt} = 94 \text{ A} \mu \text{s}^{-1} \), the subsequent TIV rises with a \( \frac{dU}{dt} \) of 1.28 kV \( \mu \text{s}^{-1} \) per device to a peak value of 501.5 kV, the resulting \( \varepsilon = \frac{dU_{TIV}}{dt} \cdot \frac{di_{cz}}{dt} = 120.3 \text{kVA/} \mu \text{s}^2 \) indicates manageable interruption conditions for the VIs in the NCP. The overshoot of the voltage over the EAP clamping level is caused by the overcharged capacitor and the ongoing oscillation between the CCP and the EAP, mentioned earlier.

CCP The maximum current in the passive CCP components is 10.66 kA. The capacitor is exposed to a voltage rise of up to 10.7 kV \( \mu \text{s}^{-1} \) with a voltage peak 729.8 kV. This overvoltage is caused by the ongoing oscillation between the CCP and the EAP respectively the magnetic energy in the inductor when the NCP is interrupted. The high voltages and currents are quite demanding and have to be respected in the capacitor design.

EAP The maximum current in the EAP is 19.57 kA and is caused by the oscillation that happens during the absorption of the remaining line energy. In total, the MOV in the EAP requires 7.35 ms to reduce the fault current to the residual level.

5.6.4. Sensitivity Analysis

In this section, the Osc-ES’s sensitivity to different currents and to adjustments of components is discussed. In the first part, the fault current margin for successful interruption is identified and the re-dimensioning for higher currents as well as the circuit breakers most current-sensitive components are discussed. In the second part,
the sensitivity of the internal current commutation time to a faster opening of the VI is investigated.

### Sensitivity to Fault Current

**Sensitivity of default dimensioning** Based on the interruption capability in the default fault case, as illustrated in Figure 5.18, the Osc-ES circuit breaker does not provide any significant margin for more severe fault currents. Even the subsequent peaks following the first pulse after VI opening do not allow the interruption of higher fault currents. The sensitivity analysis for different trip signals, gives another picture. For both cases of higher trip signal currents, 2.9 kA and a 3.6 kA, the implemented LCS-MB model successfully interrupts the fault current without an increase of the internal current commutation time or critical $\varepsilon$ for the VI. The reason for this, is the increase of the voltage $U_{MOV,ES}$ with an increasing fault current towards the ideal clamping voltage level. When approaching the ideal clamping voltage, the pulse amplitudes increase towards the predicted values for the corresponding capacitor voltage level. This exemplifies that the current interruption capability of the Osc-ES is a function of the actual fault current.

For the case of a smaller trip signal current of 1.2 kA, the same observations as for the previous cases are made, the internal current commutation time does not change significantly compared to the default case and the VI operates at an even smaller product of current and voltage slope at current zero ($\varepsilon = 101.9 \text{kVA}/\mu\text{s}^2$).
Upgrading for higher fault currents  To increase the maximum interruptible current, as described in Equation 5.39, both the LC circuit can be re-dimensioned and the rating of the ES can be increased. The first can be reached for example by reducing $L$, which has a stronger effect than adjusting $C$. To avoid an undesired higher switching frequency, which results in a larger $\frac{dI}{dt}$ and a higher stress on the ES, the capacitor has to be adjusted too. The advantage of increasing $U_{ES}$ is that the switching frequency can be maintained, but this requires additional series-IGBTs in the ES. Obviously, the increasing number of IGBT modules increases the conduction losses during normal operation at the same time.
In both of these options, due to the increasing overvoltage, the maximum permissible voltage of the capacitor imposes a design limit.

Breaker Speed Sensitivity

Mechanical switch opening time  For a 0.5 ms faster opening of the VI within 2 ms, the Osc-ES default model is capable to interrupt the fault current with a decreased internal current commutation time of 2.17 ms, which is a reduction of 0.49 ms, almost identical to the improvement in mechanical opening time. At the moment of current zero, $\varepsilon$ is considerably smaller than in the default fault case (98.5 kVA/µs² compared to 120.3 kVA/µs²), which makes the current interruption less demanding for the VIs. The voltage rise time remains almost unaffected.

Other variables  Further influencing factors for the Osc-ES (e.g. a higher switching frequency to achieve a faster pulse after contact opening) are not investigated in this thesis, since they are not expected to have a significant influence on the operation time of the breaker.
Even though the adjustment of the frequency towards a shorter delay $\Delta t_{cz}$ of the first pulse after the VI has opened, could improve the operation time, similar can be achieved by introducing a short initial delay before starting the excitation of the CCP.

5.6.5. Features

Pre-activation  Pre-activation is only possible to a limited extent. The VI opening can be initialized, but a trip signal has to received latest at the instant at which the LC excitation has to start to still achieve a current zero after the VI opening. Starting the divergent oscillation between the CCP and the NCP before a final trip order should be avoided due to the weak damping in the circuit breaker. An ongoing current oscillation will probably disturbs the power transmission along the unfaulted line in case of a false alarm.

Current limiting  The Osc-ES circuit breaker does not provide the current limiting feature.
Open–Close–Open  The Osc-ES circuit breaker will re-start the NCP-CCP oscillation if the VI is closed with the capacitor still charged. This has to be avoided in the case of re-closing the breaker onto a line with a cleared fault (O-C cycle). Fast discharging of the capacitor through a bleeding resistor on the other hand is not possible, as the capacitor is the only element capable of building up and maintaining the blocking voltage in the CCP. Consequently, re-opening can not be realized without introducing a large additional semiconductor stack.

5.6.6. Discussion

The Osc-ES circuit breaker concept operates in the default case close to the time required for the VI opening the internal current commutation time is $2.61 \text{ ms}$. Thereby, the highest stress is imposed on the ES IGBTs that have to switch under load and with a relatively high frequency of $6.25 \text{ kHz}$. The VI has to carry a current of $20.84 \text{ kA}$, however the stresses imposed on the VI during and post current zero are small so that a successful interruption appears possible under the tested conditions. Because of the ES MOV characteristics, the Osc-ES model is capable to interrupt both higher and smaller fault currents with the same speed as the default case and with acceptable VI requirements. The maximum permissible current during the interruption for the default design is $18.5 \text{ kA}$, and is primarily limited by keeping the maximum voltage of the capacitor below an assumed limit of $480 \text{ kV}$. To further increase the interruption capability, it is necessary to raise this limit. However, the costs and space requirements for capacitors capable of such high voltages are expected to increase considerably compared to the nominal design.

In terms of features, this circuit breaker does not provide many options to support the fault handling in the grid by other means than interrupting the current.
5.7. Comparison of the Breakers

5.7.1. Conduction Losses

Small conduction losses are important for an efficient energy transmission, as the reduce operation costs. This is the main motivation for not using pure semiconductor breakers, but hybrid circuit breakers. Even though the losses of the presented breakers are considerably smaller than those of comparable semiconductor breaker, significant differences between the hybrid topologies can be observed (cf. Table 5.2).

All but the Inj-PG and the Inj-LC concept use semiconductor devices in the NCP. To reduce the voltage drop along those semiconductors, a parallel connection of three series-stacks is realized for these solutions. LCS-MB, LCS-C and Osc-ES employ the same number of IGBTs and consequently cause similar losses during normal operation. By employing thyristors, which have a smaller on-state resistance than IGBTs, the Inj-C circuit breaker can operate causing less than half of the conduction losses of the three breaker concepts mentioned before.

The conduction losses in circuit breaker concepts using only mechanical switches in the NCP are negligibly small. For this reason, Inj-LC and Inj-PG are the most advantageous concepts in terms of losses in the closed state.

<table>
<thead>
<tr>
<th>Circuit Breaker</th>
<th>LCS-MB</th>
<th>LCS-C</th>
<th>Inj-C</th>
<th>Inj-PG</th>
<th>Inj-LC</th>
<th>Osc-ES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Losses</td>
<td>22.6 kW</td>
<td>22.6 kW</td>
<td>10.7 kW</td>
<td>-</td>
<td>-</td>
<td>22.6 kW</td>
</tr>
</tbody>
</table>

5.7.2. Circuit Breaker Speed

In Table 5.3, some of the measured times according to the definitions presented in Chapter 4 are listed for the six investigated concepts. In the following, the results for the different times are interpreted.

<table>
<thead>
<tr>
<th>Concept</th>
<th>( t_{\text{relay}} )</th>
<th>( \Delta t_{CC} )</th>
<th>( \Delta t(\hat{i} - TIV) )</th>
<th>( \Delta t_{FCS} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCS-MB</td>
<td>125.5 ( \mu )s</td>
<td>2.05 ms</td>
<td>0.00 ms</td>
<td>6.4 ms</td>
</tr>
<tr>
<td>LCS-C</td>
<td>125.5 ( \mu )s</td>
<td>3.04 ms</td>
<td>0.04 ms</td>
<td>7.72 ms</td>
</tr>
<tr>
<td>Inj-C</td>
<td>125.5 ( \mu )s</td>
<td>2.81 ms</td>
<td>0.1 ms</td>
<td>6.92 ms</td>
</tr>
<tr>
<td>Inj-PG</td>
<td>124.0 ( \mu )s</td>
<td>2.94 ms</td>
<td>0.04 ms</td>
<td>5.36 ms</td>
</tr>
<tr>
<td>Inj-LC</td>
<td>125.5 ( \mu )s</td>
<td>2.56 ms</td>
<td>0.00 ms</td>
<td>7.26 ms</td>
</tr>
<tr>
<td>Osc-ES</td>
<td>125.5 ( \mu )s</td>
<td>2.66 ms</td>
<td>0.00 ms</td>
<td>7.35 ms</td>
</tr>
</tbody>
</table>
5.7 Comparison of the Breakers

**Relay time** For all but the Inj-PG concept, an identical relay time $t_{\text{relay}}$, from fault inception until the trip signal is given, is observed. The 1.5 $\mu$s offset is due to the adjustments of the simplified HVDC circuit for this circuit breaker: To first allow fast charging of the internal capacitor and to later force the injected current through the damping branches instead of the the low-ohmic grounding, the ground connection is switched from low-ohmic to high-ohmic at the moment of fault occurrence. The sudden increase of resistance affects the leakage current through the EAP MOV to ground, and because of this and the internal stray inductance, an insignificantly smaller current increase is observed, leading to the shorter relay time.

A larger difference in the relay time between different breaker solutions would imply that breaker topologies affect the development of the fault even before triggering. In this case, it is very important for the protection control to know how the circuit breaker influences the fault current, to correctly decide how to treat the fault.

The same holds for the current-limiting feature, its use has to be coordinated with the protection control to avoid false decisions due to an unexpected development of the fault current. For the investigated circuit breaker solutions, no considerable influence on the fault current before triggering can be noticed. Other proposed circuit breaker concepts, using components that autonomously limit the fault current and build up a counter voltage, e.g. by placing superconductors or positive temperature coefficient resistors in the NCP, are expected to affect the fault current and consequently the fault detection.

**Internal current commutation time** The internal current commutation time $\Delta t_{\text{CC}}$ captures the core circuit breaker operation from the trip signal until the TIV peaks across the breaker terminals.

All six circuit breakers operate between 2.05 ms to 3.04 ms. The LCS-MB is clearly the fastest concept due to the fast operation of the semiconductor switch MB. While the difference to the second fastest device (Inj-LC) is quite considerable (about 0.5 ms), the five following concepts form a quite compact group with internal current commutation times between 2.56 ms and 3.04 ms.

The different internal current commutation times show clearly, that the use of the 0.5 ms slower VI instead of the UFD does not necessary lead to a slower operation time, since the slowest topology for the default fault case utilizes a UFD. However, due to the slower operation time, the concepts using VIs have a lower limit of 2.5 ms for the internal current commutation time and hence can never reach the speed of the LCS-MB. This illustrates that the operation time of the mechanical device is crucial. Depending on the development of UFD and fast VI, the gap between some of the topologies (e.g. LCS-MB and Osc-ES/Inj-PG) may close in the future.

**Delay between peak current and peak TIV** In a more realistic network model, the detection of the peak current can be difficult due to oscillations. For this reason, time measurements may use the TIV peak as a fix point instead of the current peak, as also done for the grid study conducted within the scope of this thesis. To get a
feeling for the difference between fault current and TIV peak $\Delta (\hat{i} - TIV)$ in a simple fault case without oscillating current surges, the difference in time between both is evaluated.

A relevant, but small difference can only be measured if the rise of the TIV is slowed down due to the use of a large capacitor (i.e., LCS-C, Inj-C and Inj-PG). For values below 1uF (i.e., LCS-MB, Inj-LC and Osc-ES), no significant delay is detected.

**Fault current suppression time** As defined in Chapter 4, the fault current suppression time $\Delta t_{FCS}$ is measured from the peak current (which in the default case corresponds quite accurately to the peak TIV) until the fault current intersects with the breaker specific leakage current level at nominal voltage. $\Delta t_{FCS}$ is defined by the rating of the employed MOV and the amplitude of the fault current when it is commutated into the EAP.

Except for Inj-PG all the solutions employ an MOV of similar rating. The $\Delta t_{FCS}$ between 6.4 ms to 7.72 ms verify the fault current suppression time’s dependence of the current amplitude respectively of the proportional $\Delta t_{CC}$.

In the Inj-PG solution, an additional 30 kV MOV is employed. This results in a significantly faster $\Delta t_{FCS}$ of 5.36 ms even though its maximum fault current is between the currents observed in Inj-C and LCS-C. The downside of the faster energy absorption is the requirement for a higher rating of all blocking elements, as already mentioned before. Furthermore, the time of the fault current peak or the TIV peak is considered to be more critical for a grid to stabilize, than the moment the fault current has fully decreased. Especially for this reason, the internal current commutation time was selected as the key characteristic to evaluate the different circuit breaker’s performance in terms of speed of operation.

### 5.7.3. Interruption Capability

All implemented circuit breaker models successfully interrupt the simulated fault case of a terminal fault with a current limiting inductor of 100 mH, for which they were dimensioned. Only the Inj-LC concept, whose dimensioning was adopted from [SZJ+15] violates the, according to [Sla08] rather conservative, VI constraints set for this work, however it is shown in Chapter 5 that these constraints can be respected using an adjusted dimensioning.

Aside from the detailed investigation of the interruption capability presented in this chapter, the results of multiple runs of the circuit breakers with a two-parameter variation summarize the differences in interruption capability. In Figure 5.4, the success of interruption is indicated for a variation of the trip signal current from 2.4 kA to 4.2 kA as well as a variation of the rate of rise of the fault current from 2.9 kA ms$^{-1}$ to 4 kA ms$^{-1}$, i.e., a variation of the current limiting reactor L, in series with the circuit breaker as shown in Figure 4.3, from 90 mH to 110 mH.

The current at the moment when the mechanical device has completed its opening process is not dependent on the topology, but only on the type of mechanical device (UFD: 2 ms, VI: 2.5 ms). The currents for the respective fault cases (as a function
Table 5.4.: Fault interruption capability of the circuit breakers, dimensioned for the default fault case, for different fault currents. Prospective fault currents in kiloampere at the moment when the mechanical devices (UFD and VI) have completed its opening process are listed in the matrix of LCS-MB and Osc-ES, respectively.

<table>
<thead>
<tr>
<th>Breaker</th>
<th>Δt_{CC}</th>
<th>LCS-MB</th>
<th>LCS-C</th>
<th>Inj-C</th>
<th>Inj-PG</th>
<th>Inj-LC</th>
<th>Osc-ES</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>dI/dt in kA/ms</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I_{0} in kA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCS-C</td>
<td>2.05ms</td>
<td>16kA / 2.05ms</td>
<td>9.62kA / 2.27ms</td>
<td>2.81ms</td>
<td>9.36kA / 2.10ms</td>
<td>16.6kA / 2.60ms</td>
<td>12.0kA / 2.53ms</td>
</tr>
<tr>
<td>Inj-PG</td>
<td>2.94ms</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Osc-ES</td>
<td>2.66ms</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
</tr>
</tbody>
</table>

LEGEND
Successful interruption
Critical interruption
Unsuccessful interruption

It can be seen, that LCS-MB, Inj-PG and Osc-ES interrupt all tested fault currents successfully. As outlined in previous sections, these circuit breakers, too, can only interrupt a limited range of currents.

The LCS-C on the other hand is only capable to interrupt the fault case it was designed for and smaller currents. Higher currents or current slopes are possible to interrupt, but only with a redesign of the breaker components. While it might not even require a considerable higher investment to create a breaker with a higher interruption capability, especially in the case of a growing or changing grid, some margin regarding the current interruption appears to be necessary especially for this breaker.

The Inj-C is able to interrupt a few fault currents above the default rating, but only because the circuit breaker control allows a slight overcharging of the circuit breakers capacitor above the rated value, which it must be capable of dealing with without taking damage.

The Inj-LC concept interrupts more than half of the tested fault cases in the simulation, but in all of these cases the ε requirements on the VI exceed the proposed value for the first current zero crossing. Even in the interrupted cases with the highest
### Table 5.5.: Effort of upgrading the circuit breakers for a higher fault current rating

<table>
<thead>
<tr>
<th>Circuit breaker</th>
<th>Key component</th>
<th>Design effort</th>
<th>Side effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCS-MB</td>
<td>IGBT</td>
<td>−</td>
<td>Costs</td>
</tr>
<tr>
<td>LCS-C</td>
<td>C in all branches</td>
<td>+/−</td>
<td>Operation time increase</td>
</tr>
<tr>
<td>Inj-C</td>
<td>Thyristor D</td>
<td>+</td>
<td>Conduction losses</td>
</tr>
<tr>
<td>Inj-PG</td>
<td>DB MOV</td>
<td>+</td>
<td>Break time increase</td>
</tr>
<tr>
<td>Inj-LC</td>
<td>VI capability → LC</td>
<td>+/−</td>
<td>Small current interruption</td>
</tr>
<tr>
<td>Osc-ES</td>
<td>Voltage rating ES</td>
<td>+</td>
<td>Insulation/Space</td>
</tr>
</tbody>
</table>

currents ε is larger than 220 kVA/µs² and hence almost twice as high as the suggested 140 kVA/µs² [Sla08]. The dimensioning causing the high $\frac{dI}{dt}$ was based on the aforementioned publications, however, in the scope of this work a dimensioning formula, to fulfill the VI specific $\epsilon$ and to achieve successful interruption, was derived.

In this context, it is worth mentioning, that for all three circuit breakers, LCS-C, Inj-C and Inj-PG, that employ relatively large capacitors, an increase of internal current commutation time of several tens of microseconds is observed when smaller currents are interrupted. For the other three solutions, with small capacitors of 1 µF or less, this is not observed.

Based on the results of the sensitivity analysis, the developed default design of LCS-MB, Inj-PG and Osc-ES is not only able to interrupt the fault current, but leaves a considerable margin for different trigger levels and changes in the rate of rise of the fault current. Whilst for LCS-MB the maximum interruptible current is mostly due to the intrinsic technology limit of the IGBT and therefore hardly adjustable for both higher and lower limits, Inj-PG and Osc-ES can be modified for smaller as well larger fault currents by using lower rated components or higher rated ones, respectively. Inj-C and LCS-C perform as expected, they interrupt the default fault current and smaller currents, Inj-LC’s interruption capability is considered insufficient with respect to the requirements on the VI.

### 5.7.4. Modification of Components

For all concepts, the effort of upgrading the circuit breaker to a higher fault current rating was analyzed, which is summarized in Table 5.5. For the LCS-MB the dependency on the IGBT technology sets a hard limit, and a higher current rating can only be achieved at high costs, either for additional IGBT stacks in parallel to the MB or by using improved devices. The circuit breakers LCS-C and Inj-LC can be modified to operate at higher currents, but in both cases almost the complete circuit breaker design has to be adjusted, and the adjustments come with a decrease in speed, respectively, the risk of not being able to interrupt small fault currents anymore. For Inj-C, Inj-PG and Osc-ES, only single components have to be adjusted, e.g. three additional thyristors in the Inj-C’s NCP, a smaller MOV or an increased voltage rating for the capacitor, to achieve a higher fault current rating, probably resulting in significantly
smaller costs than for the other concepts mentioned before. But even these rather uncomplicated adjustments come with certain disadvantages, such as increased conduction losses in the circuit breaker during normal operation, a longer time necessary for energy dissipation or higher insulation and space requirements. Nevertheless Inj-C, Inj-PG and Osc-ES can be upgraded to a higher fault current with less effort than LCS-MB, LCS-C and Inj-LC.

The opening time of the mechanical switch was identified as the main contributor to the internal current commutation time and therefore should be the focus of research to increase the circuit breaker speed. In this study, the effects of a 20% faster opening time are investigated with focus on the overall reduction of the internal current commutation time and the necessity for adjusting the circuit breaker dimensioning.

As listed in in Table 5.6, the UFD based concepts are able to improve their internal current commutation time at least by the reduction in opening time of 0.4 ms. By downsizing the capacitances in LCS-C and Inj-C, the voltage rise time is additionally reduced by 0.03 ms to 0.16 ms.

The VI concepts on the other hand can not be improved above the 0.5 ms shorter opening time, because the VI is always required to have opened completely before the current is completely commutated out of the NCP. Furthermore, the voltage rise time increases in all three VI-based circuit breakers because of the smaller fault current which has to charge a capacitor up to the TIV peak. Reducing the capacitance as a countermeasure is not practical with respect to the VI interruption requirements.

### 5.7.5. Conclusion

The different circuit breaker concepts have been compared with respect to conduction losses, their speed, the capability to interrupt different fault currents. Furthermore, the different efforts for upgrading for higher currents and the effect of faster opening of the mechanical switch have been investigated. The results make obvious that none of the investigated solutions is advantageous in all fields.

**Table 5.6.: Effects of a 20% faster mechanical switch opening (UFD: −0.4 ms, VI: −0.5 ms)**

<table>
<thead>
<tr>
<th>Circuit breaker</th>
<th>Adjustment</th>
<th>( \Delta t_{CC} )</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCS-MB</td>
<td>–</td>
<td>−0.40 ms</td>
<td>–</td>
</tr>
<tr>
<td>LCS-C</td>
<td>C1 (−300 ( \mu )F)</td>
<td>−0.43 ms</td>
<td>Smaller C → shorter voltage rise time</td>
</tr>
<tr>
<td></td>
<td>C2 (−20 ( \mu )F)</td>
<td>−0.56 ms</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C3 (−2 ( \mu )F)</td>
<td>−0.56 ms</td>
<td></td>
</tr>
<tr>
<td>Inj-C</td>
<td>C (−0.5 ( \mu )F)</td>
<td>−0.56 ms</td>
<td></td>
</tr>
<tr>
<td>Inj-PG</td>
<td>–</td>
<td>−0.45 ms</td>
<td>Smaller fault</td>
</tr>
<tr>
<td>Inj-LC</td>
<td>C (+0.5 ( \mu )F)</td>
<td>−0.44 ms</td>
<td>current → longer voltage</td>
</tr>
<tr>
<td></td>
<td>L (700 ( \mu )H)</td>
<td>−0.49 ms</td>
<td>rise time</td>
</tr>
<tr>
<td>Osc-ES</td>
<td>–</td>
<td>−0.49 ms</td>
<td></td>
</tr>
</tbody>
</table>
The LCS-MB’s default configuration is advantageous compared to the other circuit breakers concerning the interruption performance. But this literally comes at the price of high component costs and conduction losses in normal operation. Furthermore, its fault current rating can only be upgraded in discrete steps, since the number of parallel IGBTs is the limiting factor. Hence, discrete numbers of high voltage IGBT stacks have to be added, further increasing the costs of the MB.

The LCS-C circuit breaker is the slowest solution and its default configuration is not capable to interrupt higher currents since it already operates at its designed limit to achieve a low operation time. However, by adjusting the circuit breaker’s branches, higher ratings can be achieved, which in contrast to the LCS-MB can be done in a more continuous way. Decreasing the operation time of the UFD results in over-proportional gains in interruption speed. Due to the use of thyristors and passive elements, the reduced flexibility compared to the LCS-MB may be compensated by a lower price to a certain extent.

The current injection concept Inj-C performs similar to the LCS-C, upgrading the breaker to higher interruption levels is even easier. Additionally, it creates lower conduction losses in nominal operation than topologies using an LCS due to the use of a small thyristor stack in the main branch. The concept is expected to be costlier than the LCS-C, because it requires a higher number of thyristors.

The Inj-PG concept is able to interrupt fault currents over a wide range, conduction losses are negligibly small since the nominal current only flows through two mechanical devices and the topology offers simple upgrading. However, it is the second slowest solution with respect to the internal current commutation time. By employing a different EAP design, with a higher clamping voltage and consequently higher blocking requirements on the components, a lower fault current suppression time is achieved. Theoretically, the Inj-LC solution is the second fastest and provides the capability to interrupt currents over a wide range. Additionally, the effort for upgrading for higher currents only requires adjustments of the passive components and is estimated to be relatively cheap in comparison with additional switching devices. However, the concept, as proposed in the referenced publication, imposes very high demands on the VI, which probably can’t be fulfilled. By changing the size of the passive components in the LC circuit, in accordance to the proposed dimensioning formula, significantly lower demands on the VI can be achieved, but only at the cost of larger passive components and increasing internal current commutation times (0.07 ms for the investigated fault case).

Osc-ES is comparable to Inj-PG with the difference that interruption is faster but in return, relatively high losses occur during normal operation. Even though the basic topology is rather simplistic, the ES is probably the semiconductor element exposed to the most severe stresses, as it has switch multiple times at high frequency, in comparison to the solutions in other circuit breaker concepts. Consequently, much attention has to be paid to the design of the ES.
6. HVDC Circuit Breakers in MTDC Grids

In the previous chapter, circuit breakers have been investigated in an idealized fault case with a simple, linear rising fault current. In an HVDC multi-terminal network, the development of the fault current, which a circuit breaker has to interrupt, can be influenced in different ways, e.g. converter control and traveling wave phenomena. To analyze if the six selected circuit breaker concepts can operate successfully in an exemplary MTDC grid and to verify the validity of the results obtained in the simple HVDC circuit, the circuit breakers are tested in the MTDC network, as described in Chapter 4. In the following three sections, the circuit breakers’ performance as well as the grids reaction to the fault and its interruption are investigated for three different pole-to-pole faults. In the fourth section, the findings from the different fault cases are summarized and discussed.

6.1. Fault Case 1: Line Fault 100 km / 100 km

Fault case 1 is a pole-to-pole fault occurring in the middle of link “13”, 100 km from converters 1 and 3 in the middle of the line. Due to the reflections of the traveling wave at the current limiting inductors, the voltage across the inductors exceeds the system voltage level and consequently the rate of rise of the fault current increases for a certain time, compared to a similar fault omitting traveling wave phenomena.

6.1.1. Prospective Fault Current

In the following, the development of the fault current without breaker action is presented. Since both converter poles show the same reaction on the fault, only the positive pole is described. As presented in [LAB+15] and illustrated for both adjacent busses in Figure 6.1, the voltage at the circuit breakers (converter side, pole-to-ground) at both poles and busses falls to −150 kV with the arrival of the traveling wave, caused by the fault at the circuit breaker after 0.54 ms, resulting in an average rate of rise of the fault current of 3.4 kA ms$^{-1}$ in the first millisecond. In the second millisecond, due to wave reflections, the rate of rise is significantly reduced to 1.1 kA ms$^{-1}$. Over the first five milliseconds, during which all investigated circuit breakers are expected to reach the peak fault current, the average rate of rise of the fault current is 1.3 kA ms$^{-1}$ at bus 1.
Figure 6.1: Prospective voltage and current at bus 1 and bus 3 for a fault of type 1 \((t_{\text{fault}} = 0.7 \text{ s}, \text{pole-to-pole, 100 km from bus 1})\)

and \(1.5 \text{kA ms}^{-1}\) at bus 3, respectively. Current oscillation due to traveling wave phenomena appears to be remarkably stronger at bus 3 and has a visible impact on the fault current during the first 10 ms.

### 6.1.2. Breaker Performance

The key information about the interruption performance of the different circuit breaker concepts, such as the maximum fault current before interruption, the peak TIV across the circuit breaker, the internal current commutation time as well as the break time is listed in Table 6.1. The relay time of the protection control is \(0.06 \text{ ms}\) on both busses. In Figure 6.2, the fault currents for the different circuit breakers are shown for the first 15 ms after fault occurrence. The currents with a positive rate of rise of current are the ones observed at converter 1 (rectifier mode), the ones with a negative rate of rise of current are observed at converter 3 (inverter mode).

Comparing the circuit breakers at both busses, for all concepts, the maximum fault current is higher for the converter 3 side. This was expected, as the current at the rec-
ifier side changes direction and consequently has an initial offset of twice the nominal current. The current peaks in the circuit breakers at both ends of the faulted cable range from absolute values of 4 kA to 6.5 kA.

The TIV corresponds to the clamping voltage of the MOV with deviations of ±10 kV. For all but one circuit breaker concept, the internal current commutation times of the inverter and the rectifier circuit breaker vary only within 0.06 ms. Only the LCS-C concept has a significantly longer internal current commutation time when installed on the inverter side, which is caused primarily by the capacitor in the circuit breakers first timing branch. The capacitor starts getting charged by the decreasing nominal current, but as soon as the current changes direction, the opposing voltage of the timing branch causes the current to rush back into the NCP via the LCS snubber circuit and prevents the UFD from opening. As discussed previously, a more detailed UFD model will probably eliminate this effect.

This offset in $\Delta t_{CC}$ directly affects LCS-C’s break time as well, which is longer on the rectifier side than on the inverter side. For the other circuit breakers, the observed break time, from trip signal until the fault returns to the leakage current level for the first time, is shorter for the circuit breakers at rectifier side. This is a direct consequence of the fault current peak which is proportional to the energy that has to be dissipated, hence influencing the energy dissipation time.

<table>
<thead>
<tr>
<th>Concept</th>
<th>$i_1$</th>
<th>$U_{TIV,1}$</th>
<th>$\Delta t_{CC,1}$</th>
<th>$\Delta t_{brk,1}$</th>
<th>$i_3$</th>
<th>$U_{TIV,3}$</th>
<th>$\Delta t_{CC,3}$</th>
<th>$\Delta t_{brk,3}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCS-MB</td>
<td>5.5 kA</td>
<td>471 kV</td>
<td>2.1 ms</td>
<td>12.6 ms</td>
<td>3.9 kA</td>
<td>469 kV</td>
<td>2.1 ms</td>
<td>5.2 ms</td>
</tr>
<tr>
<td>LCS-C</td>
<td>6.5 kA</td>
<td>476 kV</td>
<td>3.7 ms</td>
<td>10.3 ms</td>
<td>6.3 kA</td>
<td>471 kV</td>
<td>4.9 ms</td>
<td>12.6 ms</td>
</tr>
<tr>
<td>Inj-C</td>
<td>5.6 kA</td>
<td>471 kV</td>
<td>3.4 ms</td>
<td>9.2 ms</td>
<td>4.9 kA</td>
<td>469 kV</td>
<td>3.4 ms</td>
<td>6.9 ms</td>
</tr>
<tr>
<td>Inj-PG</td>
<td>6.2 kA</td>
<td>531 kV</td>
<td>3.1 ms</td>
<td>7.2 ms</td>
<td>5.2 kA</td>
<td>530 kV</td>
<td>3.2 ms</td>
<td>6.7 ms</td>
</tr>
<tr>
<td>Inj-LC</td>
<td>6.1 kA</td>
<td>488 kV</td>
<td>2.6 ms</td>
<td>7.3 ms</td>
<td>4.5 kA</td>
<td>480 kV</td>
<td>2.7 ms</td>
<td>6.7 ms</td>
</tr>
<tr>
<td>Osc-ES</td>
<td>6.0 kA</td>
<td>483 kV</td>
<td>2.7 ms</td>
<td>7.8 ms</td>
<td>4.3 kA</td>
<td>476 kV</td>
<td>2.7 ms</td>
<td>7.5 ms</td>
</tr>
</tbody>
</table>

For a increased “leakage level threshold” of 10 A: $\Delta t_{brk,1} = 6.72$ ms

### Post-Interruption Phenomena

For the break time of the circuit breakers on the inverter side, the only outlier is explained with the LCS-C’s commutation principle and the UFD model.

On the rectifier side, the break time of several circuit breakers does not correlate with the peak fault current. This is due to the interaction between the MTDC network and the circuit breaker in the last milliseconds of the breaking operation, when the fault current approaches the leakage current level. Furthermore, a closer look is taken at the ongoing oscillation which can be seen in Figure 6.2. In Figure 6.3, the currents through the circuit breakers on the positive pole of converter 1 are shown as they
approach the indicated leakage current level.
The current through LCS-MB decreases strongly towards the leakage current level, but remains slightly above this level for another 6 ms, most probably due to a grid specific low-frequency resonance, mentioned in [LAB+15]. According to the used definition, this leads to a significant increase in break time. However, depending on the operation speed and interruption capability of the residual current switch, which is not modeled here, the instance of galvanic separation of the faulty part of the line may not be influenced by such a phase. Hence, taking into account the increased break time only for a comparison may be misleading.

For the Inj-C breaker, a small peak current but a relatively long break time is observed, caused by the large capacitor, which delays the peak current and the energy dissipation as the long $\Delta t_{CC}$ reflects. Additionally, for all breaker concepts a significant current oscillation is observed during the energy dissipation process. In the case of Inj-C this oscillation, caused by the incoming, already slightly damped, reflected waves, prevents the decreasing current from crossing the leakage current level at around 8.5 ms after

Figure 6.2.: Circuit breaker currents at bus 1 (upper half, solid lines) and bus 3 (lower half, dashed lines) for a fault of type 1 ($t_{fault} = 0.7$s, pole-to-pole, 100 km from bus 1)
6.1 Fault Case 1: Line Fault 100 km / 100 km

Figure 6.3.: Circuit breaker currents at bus 1, when reaching the leakage current level, for a fault of type 1 ($t_{\text{fault}} = 0.7$ s, pole-to-pole, 100 km from bus 1)

the fault for the duration of another traveling wave of approximately 1 ms.
Comparing Inj-LC and Osc-ES, the fault current in the Inj-LC intersects with the leakage current level slightly faster than Osc-ES, even though the observed maximum current is higher. However, due to the Inj-LC’s smaller inductance and resistance the maximum peak occurs shortly before the smaller peak in the Osc-ES fault current and this time offset if kept throughout the energy dissipation, which is also faster for the Inj-PG due to its higher rated EAP.
Furthermore and more importantly, for both circuit breakers a strong ongoing oscillation of approximately 50 A is observed after the fault current crossed the leakage current level, while the fault currents of the other breakers are above leakage current level for a maximum of two traveling wave oscillations after reaching leakage level for the first time. This oscillation occurs between the circuit breakers at both poles, namely their LC branches, the converter capacitor as well as the system inductances and capacitances, only weakly damped by the line and fault resistance.
6.1.3. Grid Reaction

Voltages at Buses 1 and 3

As an indicator for the severity of the disturbance of the grid, the maximum and minimum voltage between the positive and the negative pole (nominal value: 640 kV) after the fault occurrence are measured at the adjacent converter station busses. In Table 6.2, the respective peak values for the pole-to-pole voltages are listed. Across all circuit breakers concepts and both busses, the most severe peaks are −81 kV and 916 kV, respectively. When employing LCS-MB or LCS-C circuit breakers, the voltage deviation at the rectifier station, converter 1, is less severe than at the inverter station. For the other circuit breakers concepts, the positive and negative deviation are more severe at the rectifier station. Based on these observations, no clear correlation of the bus voltage peaks with neither the operation mode of the converter nor with the circuit breaker operation time nor with the circuit breaker peak current is identified.

As Figure 6.4 shows, the bus voltages of the majority of the circuit breaker concepts follow similar resonances after having returned above a pole-to-pole voltage level of 400 kV. The maximum amplitude of the oscillating voltage, occurring within the first 10 ms after the fault, appears to have only small influence on the post fault stabilization (after several tens of milliseconds) of the grid which seems to be mainly influenced by the grid parameters and converter controls. At converter 1, a variation of up to 325 kV between the different circuit breakers minima is observed. But as it can be seen, the bus voltages of all circuit breaker cases, except LCS-C, are exposed to a similar oscillation, and the offset between four different voltage curves in Figure 6.4 is below 10 kV after 40 ms. The oscillation of the bus voltage in the LCS-MB case is slightly phase shifted and of an approximately 15 kV smaller amplitude after 40 ms. The LCS-C bus voltage is phase shifted, too, but in the opposite direction than LCS-MB and has an approximately 20 kV larger amplitude and a 20 kV offset.

At converter 3, similar to converter 1, the bus voltages of the all but the LCS-C case become more and more similar with time, the band within which the bus voltages are is reduced to about 10 kV after 40 ms. Furthermore the voltage of this five cases oscillates with a similar frequency. The bus voltage in the LCS-C case exhibits a much more severe voltage drop and is exposed to more than one resonance which show a high peak to peak voltage of around 200 kV after 40 ms.

| Table 6.2.: Fault case 1: Post-fault pole-to-pole bus voltage maxima and minima |
|-----------------|-------|------|-------|-------|-------|-------|
|                | LCS-MB| LCS-C| Inj-C | Inj-PG| Inj-LC| Osc-ES|
| max($U_{bus1}$) | 764 kV| 853 kV| 843 kV| 903 kV| 849 kV| 855 kV|
| max($U_{bus3}$) | 916 kV| 914 kV| 748 kV| 723 kV| 836 kV| 843 kV|
| min($U_{bus1}$) | 302 kV| −23 kV| 108 kV| 20 kV | 89 kV | 44 kV |
| min($U_{bus3}$) | 225 kV| −81 kV| 220 kV| 303 kV| 225 kV| 227 kV|
Figure 6.4.: Bus voltages at bus 1 (upper plot) and bus 3 (lower plot) for a fault of type 1
\((t_{\text{fault}} = 0.7 \text{ s}, \text{pole-to-pole, 100 km from bus 1})\)

**Currents in Unfaulted Links**

The converter’s capacitor and the adjacent links are the first sources for the increasing current in case of a fault. As several fault detection schemes are partly or fully based on a current threshold [HHJ14a, LAB+15], the change in current in the adjacent links is inspected.

During normal operation, the three adjacent links “12”, “14” and “34” carry very small currents below 0.5 kA, because the main links “13” and “24” offer the shorter and therefore lower resistive path for the direct transmission of the main part of the energy from converter 1 to 3 and converter 2 to 4, respectively.

The peak currents observed in the three HVDC links adjacent to the faulted link as well as the steady state current levels before the fault’s occurrence are listed in Table 6.3. The overshoot of the fault current over the nominal current, which is relevant for a current based detection, is shown in Figure 6.5 together with the internal current commutation time of the respective adjacent circuit breaker. Even though the absolute current peaks in Table 6.3 between 1 kA to 2.5 kA appear to be moderate compared to the faulted line, in some cases they even exceed the nominal pre-fault current by
more than a factor of 9 which may impose challenges on a local current based fault detection scheme.

Table 6.3.: Fault case 1: Peak currents in adjacent links

<table>
<thead>
<tr>
<th></th>
<th>pre-fault</th>
<th>LCS-MB</th>
<th>LCS-C</th>
<th>Inj-C</th>
<th>Inj-PG</th>
<th>Inj-LC</th>
<th>Osc-ES</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>i_{12}</td>
<td>$</td>
<td>0.22 kA</td>
<td>1.18 kA</td>
<td>2.50 kA</td>
<td>2.00 kA</td>
<td>2.38 kA</td>
</tr>
<tr>
<td>$</td>
<td>i_{14}</td>
<td>$</td>
<td>0.54 kA</td>
<td>0.74 kA</td>
<td>2.04 kA</td>
<td>1.56 kA</td>
<td>1.93 kA</td>
</tr>
<tr>
<td>$</td>
<td>i_{34}</td>
<td>$</td>
<td>0.45 kA</td>
<td>1.77 kA</td>
<td>3.20 kA</td>
<td>1.93 kA</td>
<td>1.90 kA</td>
</tr>
</tbody>
</table>

By putting the links’ current peaks into relation with the respective circuit breaker’s internal current commutation time, it becomes clear that for all but the LCS-MB concept, the relative and absolute rise in current decreases from link “13” over “14” to “34”. For the LCS-MB concept, link “34” is more severely affected than “14”.

Figure 6.5.: Internal current commutation time of the circuit breakers at bus 1 and bus 3, peak currents in adjacent lines relative to the pre-fault current level for a fault of type 1 (pole-to-pole, 100 km from bus 1)

6.1.4. Discussion

For fault case 1 in the MTDC network, it is observed that the circuit breakers have to operate at currents significantly lower than their rating. Even though this conditions look less severe than the ones in the simple HVDC circuit fault case (cf. Chapter 5),
the operation times of the circuit breakers are longer. The main reason is, that the smaller current, which is caused by a significant decrease of $\frac{dI}{dt}$ after about 1 ms due to traveling wave effects, requires more time to charge the internal capacitors up to the TIV. This is underlined by the observation, that the time increase is more severe for circuit breakers with relatively larger capacitors. For most of the circuit breaker topologies, a similar operation speed on the rectifier and the inverter side was observed.

The post-fault oscillation in the Inj-LC and Osc-ES concept may have an influence on the performance of a residual current switch, that needs to be considered. For the other circuit breakers, bringing the current down to the leakage current level, which a residual current switch is capable of interrupting, is achieved in a reasonable time.

With respect to the stabilization of the bus voltages after a fault interruption, results suggest that differences in circuit breaker operation time below 1 ms, which is the case for the investigated solutions, do affect the stabilization of the bus voltages only to a small extent and only during the first tens of milliseconds.

For a fault 100 km from both busses in the middle of line “13” the investigated circuit breakers were capable to interrupt the fault current at amplitudes of below 7 kA and build up the TIV within 5 ms. All but LCS-C, which requires considerably longer time to build up the TIV at smaller fault currents due to its capacitor cascade, returned the fault current below the leakage current level within 10 ms to allow the system to return to a stable state of operation.

### 6.2. Fault Case 2: Line Fault 25 km / 175 km

The second fault occurs 25 km away from the in-feeding rectifier (converter 1) respectively 175 km from the one in inverter mode (converter 3), where the current changes direction in case of a fault. This fault case was chosen to investigate the influence of higher and lower frequency traveling wave oscillations on the interruption performance of the selected circuit breakers.

#### 6.2.1. Prospective Fault Current

In contrast to fault case 1 (Figure 6.1) that occurs in the middle of line “13”, the frequency of the voltage wave oscillation, which is reflected at the current limiting reactor as well as the fault location, differs between both busses of the faulted line in fault case 2, as shown in Figure 6.6, because of the different distance of converter 1 and 3 to the fault.

At bus 1, the first voltage wave arrives after 0.13 ms, resulting in a maximum voltage drop of $-254$ kV. Due to this first surge, the fault current rises relatively steep at a rate of $5.4$ kA ms$^{-1}$ for the first 0.28 ms. Afterwards, due to further reflections, the rate of rise is decreased. For the five milliseconds after the fault inception at the circuit breaker, an average rise of rate of the fault current of $1.5$ kA ms$^{-1}$ is observed.

At bus 3, the voltage falls to $-92$ kV during the first surge, which arrives at the cir-
circuit breaker 0.9 ms after the fault occurrence. During the 2 ms of negative voltage, the average rate of rise of the fault current is 2.9 kA ms$^{-1}$. Similar to the development of the fault current at the other side of the fault location, at bus 3 the rate of rise then also decreases considerably. During the first five milliseconds of the fault current, the average rate of rise is only 1.1 kA ms$^{-1}$.

### 6.2.2. Breaker Performance

After a relay time of the protection control of 0.02 ms for the steep voltage drop at bus 1 and 0.15 ms at bus 3, the circuit breakers at the respective busses are triggered. As for fault case 1, the shape of the rising fault current in the different circuit breakers is defined by the grid topology and fault location but by the circuit breaker itself, as the circuit breaker currents, measured at the circuit breaker’s converter side terminal, in comparison to the prospective fault current in Figure 6.7 show. The breaker characteristic data for the fault interruption is listed in Table 6.4. As for case 1, the circuit breakers at converter 1 have to interrupt a higher fault cur-
rent, ranging from 5.8 kA to 7 kA, than the circuit breakers at converter 3 (4.8 kA to 5.7 kA), because of the initial offset of the inverter current of twice the nominal current. However, the maximum fault currents observed in all the circuit breakers is significantly below their interruption capabilities.

The circuit breakers build up the peak TIV within ±20 kV of the clamping voltage of their EAP MOV. For most of the circuit breaker concepts, the maximum voltage is about 10 kV below the clamping voltage. This was expected, since the fault currents are lower than the design limit of breakers’ dimensioning.

The internal current commutation time as well as the break time (after subtracting the difference in relay time) of the inverter- and rectifier-side breakers are almost equal for LCS-MB, Inj-LC and Osc-ES. For the LCS-C concept at the inverter side, a very long internal current commutation time of 6.81 ms is observed because of the time required for charging all three internal capacitors with the relatively small fault current, as already observed in the grid fault case 1.

For Inj-C, a shorter commutation time was measured at converter 3 than at con-


Table 6.4.: Fault case 2: Breaker performance

<table>
<thead>
<tr>
<th>Concept</th>
<th>$i_1$</th>
<th>$U_{TIV,1}$</th>
<th>$\Delta t_{CC,1}$</th>
<th>$\Delta t_{brk,1}$</th>
<th>$i_3$</th>
<th>$U_{TIV,3}$</th>
<th>$\Delta t_{CC,3}$</th>
<th>$\Delta t_{brk,3}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCS-MB</td>
<td>5.8 kA</td>
<td>472 kV</td>
<td>2.1 ms</td>
<td>6.6 ms</td>
<td>4.8 kA</td>
<td>470 kV</td>
<td>2.1 ms</td>
<td>6.3 ms</td>
</tr>
<tr>
<td>LCS-C</td>
<td>7.0 kA</td>
<td>478 kV</td>
<td>3.8 ms</td>
<td>10.3 ms</td>
<td>5.2 kA</td>
<td>468 kV</td>
<td>6.8 ms</td>
<td>12.8 ms</td>
</tr>
<tr>
<td>Inj-C</td>
<td>6.0 kA</td>
<td>471 kV</td>
<td>3.1 ms</td>
<td>7.2 ms</td>
<td>4.8 kA</td>
<td>460 kV</td>
<td>2.7 ms</td>
<td>7.2 ms</td>
</tr>
<tr>
<td>Inj-PG</td>
<td>6.4 kA</td>
<td>458 kV</td>
<td>3.1 ms</td>
<td>7.3 ms</td>
<td>5.7 kA</td>
<td>345 kV</td>
<td>3.2 ms</td>
<td>6.6 ms</td>
</tr>
<tr>
<td>Inj-LC</td>
<td>6.4 kA</td>
<td>489 kV</td>
<td>2.6 ms</td>
<td>7.0 ms</td>
<td>4.8 kA</td>
<td>481 kV</td>
<td>2.6 ms</td>
<td>6.8 ms</td>
</tr>
<tr>
<td>Osc-ES</td>
<td>6.4 kA</td>
<td>484 kV</td>
<td>2.6 ms</td>
<td>7.9 ms</td>
<td>4.8 kA</td>
<td>477 kV</td>
<td>2.6 ms</td>
<td>7.6 ms</td>
</tr>
</tbody>
</table>

verter 1. The circuit breaker at converter 3 is already able to force the fault current to decrease by building up a slightly smaller TIV than at converter 1 because of the smaller fault current and the lower energy in the grid inductances to be dissipated. In case of the Inj-PG circuit breaker, the small fault current leads to an even further decrease of the TIV across the capacitor, because of the series connected resistor. As a result, building up 345 kV is sufficient to initiate the decrease of the fault current to the leakage level.

**Post- Interruption Phenomena**

Aside from the already explained LCS-C operation and the oscillation in the Inj-LC and the Osc-ES concept, which was already discussed for fault case 1, no further irregularities during and after the energy dissipation stage are observed. As can be seen in Figure 6.8, the oscillating current sill has a magnitude of around 50 A 15 ms after the fault occurrence.

**6.2.3. Grid Reaction**

**Voltages at Busses 1 and 3**

In Table 6.5, the maximum and minimum voltage, observed after the fault occurrence, are listed for the inverter and the rectifier side for each circuit breaker. The most severe values observed are $-91$ kV for LCS-C and $1041$ kV for LCS-MB, respectively. Both these values occur at the inverter station. The difference between the maximum and the minimum voltage is higher at the inverter station for LCS-MB and LCS-C, whereas for the other four solutions the difference is higher at the rectifier station. In general, the deviation of the peak values of the different circuit breakers is less severe for those employed at the rectifier station.

In Figure 6.9, it can be seen that the bus 1 voltages of Inj-C, Inj-PG, Inj-LC and Osc-ES show similar resonances, the bus voltage for these breakers follows a similar curve, only Inj-PG has an approximately 20 kV larger amplitude. LCS-MB and Inj-PG both are less affected by the resonance of faster frequency, which the other concepts are
exposed to but follow the slope of the slower underlying resonance, LCS-MB with an approximately 60 kV smaller amplitude than Inj-PG. On bus 3, LCS-MB, Inj-C and Inj-PG follow the same curve very close to each other, whereas Inj-LC and Osc-ES, following the same low frequency resonance, are significantly less exposed to the high frequency oscillation. The frequencies of LCS-C’s oscillations mismatch with those observed for the other breakers from 15 ms past the fault on. The LCS-C’s peak to peak voltage difference after 40 ms is approximately 200 kV whereas for the other concepts only 70 kV to 100 kV are observed. This higher volatility of the bus voltage is likely to delay the systems return to stable operation compared to other solutions.

**Currents in Unfaulted Links**

As can be seen in Table 6.6, the peak currents measured in the adjacent links range from 1.2 kA to 3.1 kA. It is notable that the three lowest current peaks (1.2 kV to 1.7 kV), are observed for the LCS-MB concept whilst the peak currents for all other circuit breaker solutions lie above 1.7 kA. This observation represents the observed
### Table 6.5: Fault case 2: Post-fault pole-to-pole bus voltage maxima and minima

<table>
<thead>
<tr>
<th>Circuit Breaker</th>
<th>LCS-MB</th>
<th>LCS-C</th>
<th>Inj-C</th>
<th>Inj-PG</th>
<th>Inj-LC</th>
<th>Osc-ES</th>
</tr>
</thead>
<tbody>
<tr>
<td>max($U_{bus1}$)</td>
<td>851 kV</td>
<td>814 kV</td>
<td>858 kV</td>
<td>871 kV</td>
<td>953 kV</td>
<td>948 kV</td>
</tr>
<tr>
<td>max($U_{bus3}$)</td>
<td>1041 kV</td>
<td>984 kV</td>
<td>766 kV</td>
<td>791 kV</td>
<td>867 kV</td>
<td>876 kV</td>
</tr>
<tr>
<td>min($U_{bus1}$)</td>
<td>335 kV</td>
<td>28 kV</td>
<td>110 kV</td>
<td>60 kV</td>
<td>49 kV</td>
<td>26 kV</td>
</tr>
<tr>
<td>min($U_{bus3}$)</td>
<td>281 kV</td>
<td>-94 kV</td>
<td>276 kV</td>
<td>307 kV</td>
<td>281 kV</td>
<td>284 kV</td>
</tr>
</tbody>
</table>

### Figure 6.9: Bus voltages at bus 1 (upper plot) and bus 3 (lower plot) for a fault of type 2 ($t_{fault} = 0.7$ s, pole-to-pole, 25 km from bus 1)
6.2 Fault Case 2: Line Fault 25 km / 175 km

correlation between the circuit breaker’s internal current commutation time and the peak value to which the adjacent currents rise. Figure 6.10 illustrates this observation, it shows the commutation time next to the relative current overshoot. The relative current peak for all the circuit breakers and all the adjacent links is above two times the steady state value, link “12” having the strongest relative overshoot.

Table 6.6.: Fault case 2: Peak currents in adjacent links

<table>
<thead>
<tr>
<th></th>
<th>pre-fault</th>
<th>LCS-MB</th>
<th>LCS-C</th>
<th>Inj-C</th>
<th>Inj-PG</th>
<th>Inj-LC</th>
<th>Osc-ES</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>\hat{i}_{12}</td>
<td>$</td>
<td>0.22 kA</td>
<td>1.59 kA</td>
<td>2.56 kA</td>
<td>2.23 kA</td>
<td>2.52 kA</td>
</tr>
<tr>
<td>$</td>
<td>\hat{i}_{14}</td>
<td>$</td>
<td>0.54 kA</td>
<td>1.23 kA</td>
<td>2.11 kA</td>
<td>1.75 kA</td>
<td>2.06 kA</td>
</tr>
<tr>
<td>$</td>
<td>\hat{i}_{34}</td>
<td>$</td>
<td>0.45 kA</td>
<td>1.70 kA</td>
<td>3.07 kA</td>
<td>1.87 kA</td>
<td>1.97 kA</td>
</tr>
</tbody>
</table>

Figure 6.10.: Internal current commutation time of the circuit breakers at bus 1 and bus 3, peak currents in adjacent lines relative to the pre-fault current level for a fault of type 2 (pole-to-pole, 25 km from bus 1)

6.2.4. Discussion

All circuit breakers successfully disconnect the faulted cables from both terminals at low fault currents, and for each circuit breaker the internal current commutation time is similar at both busses. In general, the TIV levels are lower, some even do not reach
the MOV clamping voltage, which however does not negatively affect the operation. As for the previously discussed case, the ongoing oscillation in both circuit breaker concepts with LC CCP requires special attention regarding both the residual current switch as well as the voltage control of the converter capacitor.

Regarding the stabilization of the bus voltages, especially for converter 1, the results illustrated in Figure 6.8 indicate that while the current breaking itself may have an influence on resonances, the topology of the circuit breaker appears not to be of significant influence, since the development of the voltage for this fault case is quite similar for the selected breakers. Only for the long operation of LCS-C on bus 3, the bus voltage is disturbed extraordinarily during the first 15 ms.

The investigation of the adjacent links shows that the observed current increase in case of a fault depends on a circuit breaker’s speed. As the current in adjacent lines reaches peaks above reasonable limits for current based fault detection (above 2 kA [HHJ14a]), such a detection scheme should only be used for triggering pre-activation, if available. In combination with a voltage based detections scheme for the overall trip order, low interruption times can be achieved while maintaining selectivity.

6.3. Fault Case 3: Terminal fault / Line Fault 200 km

Fault case 3 simulates a fault at the cable-sided terminal of the circuit breakers at converter 1, which causes the MTDC’s most severe fault current to occur at this circuit breaker, according to [LAB+15].

6.3.1. Prospective Fault Current

In Figure 6.11, the currents and pole-to-ground voltage at both terminals of the faulted cable are shown for the case of no circuit breaker operation.

For the circuit breaker at bus 1, at whose terminal the fault occurs, the voltage immediately drops to zero at fault occurrence and remains there, no traveling waves are observed because no cable is modeled between the fault and the current limiting reactor. Due to the voltage drop along the reactor, the fault current through the breaker rises with $2.5 \text{ kA ms}^{-1}$ during the first millisecond and an average of $1.6 \text{ kA ms}^{-1}$ over the first 5 ms.

The voltage wave takes 1.08 ms to arrive at the current limiting reactor of bus 3 and causes the voltage to drop to $-77 \text{kV}$ during the first surge, resulting in a rate of rise of current of $2.6 \text{ kA ms}^{-1}$. The rate of rise of current decreases after about 2 ms, which is the time when the traveling wave, reflected at bus 3 hits the fault location again and raises the potential at the breaker terminal, reducing the voltage across the current limiting reactor. During the first 5 ms after the fault inception, an average rate of rise of $1.4 \text{ kA ms}^{-1}$ is observed, because the current rise slows down considerably after the first surge due to reflected wave phenomena.
Figure 6.11.: Prospective voltage and current at bus 1 and bus 3 for a fault of type 3 ($t_{\text{fault}} = 0.7\text{ s}$, pole-to-pole, at the bus 1 circuit breaker terminals)

### 6.3.2. Breaker Performance

The protection control requires a relay time of 0.05 ms at bus 1 and 1.2 ms at bus 3. The control at bus 1 triggers faster because of the steeper drop of the voltage at the circuit breaker terminal.

The peak current measured in the circuit breaker at bus 1 is larger than in the circuit breaker at bus 3 for all investigated circuit breaker concepts, because of the different slopes of the prospective fault currents (cf. Figure 6.12). The respective peak currents in the bus 1 circuit breaker range from 6.3 kA to 7 kA, those at bus 3 from 4.9 kA to 5.8 kA, and are listed in Table 6.7.

For the internal current commutation time, discrepancies of more than 0.1 ms between the bus 1 and the bus 3 circuit breaker are observed for the LCS-MB and the LCS-C concept. Delays in LCS-MB are caused by leakage current through the snubber circuit optimized for a different fault rating. For the LCS-C concept, the snubber circuit plays a minor role, the previously discussed charging time of the capacitors and the polarity reversal of the inverter current are the main reason for the discrepancies.
The Inj-PG concept’s TIV stands out at both busses with peaks of only 236.55 kV and 329.8 kV, measured from pole to ground on the healthy side of the circuit breaker. The first value is even below the poles system voltage level, but as the the circuit breakers interrupt the current and return it to the leakage level and the bus voltages stabilize above 600 kV this is not investigated further.

When accounting for the different relay times, the measured break times approximately correspond to the observed internal current commutation time and the EAP rating as expected and the times at bus 1 approximately match those at bus 3 with a maximum difference of 0.5 ms to 1 ms.

**Post-Interruption Phenomena**

Similarly to the previous fault cases when using Inj-LC or Osc-ES, oscillations in the path $L−CCP−cable−fault−cable−CCP−L−VSC$ capacitor occur at both ends of the faulted line for these two circuit breaker concepts. In Figure 6.13, the oscillating
In Table 6.7. the currents through the the positive pole bus 1 circuit breaker are shown for the different circuit breaker concepts. After 15 ms, the weakly damped oscillation amplitude is still at $100 \text{ A (Inj-LC)}$ and $200 \text{ A (Osc-ES)}$, respectively. The amplitude of the oscillations in bus 3 have a similar amplitude compared to those in bus 1 even though theoretically they are exposed to a higher damping through the cable’s resistivity.

### Volatges at Busses 1 and 3

In Table 6.8, the maximum and minimum pole-to-pole voltages, occurring at bus 1 and bus 3 for the different circuit breaker concepts, are illustrated. Whilst the variation of both maximum and minimum voltages at bus 1 is approximately $100 \text{ kV}$, strong discrepancies between the peak values of up to $350 \text{ kV}$ are observed at bus 3. The voltages at bus 1, shown in the upper plot of Figure 6.14, follow the same curve from $20 \text{ ms}$ past the fault occurrence on. LCS-MB has the smallest resonance amplitude, followed by Inj-C, Osc-ES and Inj-LC as well as Inj-PG, the latter with an approximately $10 \text{ kV}$ larger amplitude. LCS-C follows this voltage curve as well, but with a slight delay of less than $1 \text{ ms}$ and a DC offset of $20 \text{ kV}$.

The discrepancies between the different maximum and minimum voltages at bus 3 occur only within the first $10 \text{ ms}$ after the fault inception probably due to the different transient impact of traveling wave effects. From $15 \text{ ms}$ after the fault inception on, the circuit breaker voltages show a high frequency, low amplitude oscillation. The voltage curves of LCS-MB, Inj-C, Inj-LC and Osc-ES are almost identical, Inj-PG’s voltage curve is slightly delayed. Only the LCS-C concept, which has the highest maximum to minimum difference, too, is exposed to another resonance of smaller frequency of unclear origin.

### Currents in Unfaulted Links

The currents in the adjacent lines rise from their nominal values between $0.22 \text{ kV}$ to $0.54 \text{ kV}$ up to $2.75 \text{ kA}$, as presented in Table 6.9. A common link which has to carry the highest of the adjacent currents can not be identified for the different circuit breaker concepts. However, as Figure 6.15 clearly shows, the highest transient current

<table>
<thead>
<tr>
<th>Concept</th>
<th>Circuit breaker at converter 1</th>
<th>Circuit breaker at converter 3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$i_1$</td>
<td>$U_{TIV,1}$</td>
</tr>
<tr>
<td>LCS-MB</td>
<td>6.4 kA</td>
<td>473 kV</td>
</tr>
<tr>
<td>LCS-C</td>
<td>7.0 kA</td>
<td>479 kV</td>
</tr>
<tr>
<td>Inj-C</td>
<td>6.3 kA</td>
<td>472 kV</td>
</tr>
<tr>
<td>Inj-PG</td>
<td>6.7 kA</td>
<td>237 kV</td>
</tr>
<tr>
<td>Inj-LC</td>
<td>6.6 kA</td>
<td>490 kV</td>
</tr>
<tr>
<td>Osc-ES</td>
<td>6.5 kA</td>
<td>484 kV</td>
</tr>
</tbody>
</table>
peak in relation to the nominal current occurs in link “12” for all circuit breakers. By comparing both, the relative increase as well as the absolute current measured in a specific link with the internal current commutation time of the adjacent breaker, a correlation between the current overshoot in the link and the circuit breakers’ speed can be identified.

6.3.3. Discussion

The six different circuit breakers all operate successfully in the terminal fault simulation. The differences in speed between the breakers operating at bus 1 and those at bus 3 are within acceptable margins. The Inj-PG circuit breaker successfully breaks the current without building up a TIV above the system voltage. The conditions, under which this effect occurs are not investigated further within the scope of this thesis. However, it should be covered when investigating the concept in more detail. A residual oscillation with an amplitude of 100 A to 200 A is observed for the Inj-LC
Table 6.8.: Fault case 3: Post-fault pole-to-pole bus voltage maxima and minima

<table>
<thead>
<tr>
<th></th>
<th>LCS-MB</th>
<th>LCS-C</th>
<th>Inj-C</th>
<th>Inj-PG</th>
<th>Inj-LC</th>
<th>Osc-ES</th>
</tr>
</thead>
<tbody>
<tr>
<td>max($U_{bus1}$)</td>
<td>891 kV</td>
<td>826 kV</td>
<td>868 kV</td>
<td>892 kV</td>
<td>953 kV</td>
<td>960 kV</td>
</tr>
<tr>
<td>max($U_{bus3}$)</td>
<td>1025 kV</td>
<td>990 kV</td>
<td>778 kV</td>
<td>747 kV</td>
<td>919 kV</td>
<td>920 kV</td>
</tr>
<tr>
<td>min($U_{bus1}$)</td>
<td>154 kV</td>
<td>21 kV</td>
<td>102 kV</td>
<td>10 kV</td>
<td>36 kV</td>
<td>22 kV</td>
</tr>
<tr>
<td>min($U_{bus3}$)</td>
<td>300 kV</td>
<td>−24 kV</td>
<td>294 kV</td>
<td>313 kV</td>
<td>300 kV</td>
<td>302 kV</td>
</tr>
</tbody>
</table>

Figure 6.14.: Bus voltages at bus 1 (upper plot) and bus 3 (lower plot) for a fault of type 1 ($t_{fault} = 0.7$ s, pole-to-pole, at the bus 1 circuit breaker terminals)
Table 6.9.: Fault case 3: Peak currents in adjacent links

<table>
<thead>
<tr>
<th></th>
<th>pre-fault</th>
<th>LCS-MB</th>
<th>LCS-C</th>
<th>Inj-C</th>
<th>Inj-PG</th>
<th>Inj-LC</th>
<th>Osc-ES</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_{12}$</td>
<td>0.22 kA</td>
<td>2.00 kA</td>
<td>2.62 kA</td>
<td>2.26 kA</td>
<td>2.61 kA</td>
<td>2.35 kA</td>
<td>2.42 kA</td>
</tr>
<tr>
<td>$i_{14}$</td>
<td>0.54 kA</td>
<td>1.50 kA</td>
<td>2.17 kA</td>
<td>1.78 kA</td>
<td>2.15 kA</td>
<td>1.87 kA</td>
<td>1.95 kA</td>
</tr>
<tr>
<td>$i_{34}$</td>
<td>0.45 kA</td>
<td>1.72 kA</td>
<td>2.75 kA</td>
<td>1.85 kA</td>
<td>2.00 kA</td>
<td>1.76 kA</td>
<td>1.76 kA</td>
</tr>
</tbody>
</table>

Figure 6.15.: Internal current commutation time of the circuit breakers at bus 1 and bus 3, peak currents in adjacent lines relative to the pre-fault current level for a fault of type 3 (pole-to-pole, at bus 1)

and the Osc-ES concept after the energy dissipation. This oscillation may impose special requirements on a residual current switch. The voltages at the busses are stabilized within a similar time range for most of the investigated solutions, independent of the circuit breakers speed. Only the LCS-C, whose operation is delayed due to the small fault current, needs a considerably longer time to stabilize the voltage at bus 3.

From the investigation of the current peaks in the adjacent links, it can be seen that the magnitude of the current peak in these links correlates with the circuit breaker operation time, but even for the fastest of the simulated circuit breakers, the current in at least one of the adjacent links exceeds the circuit breakers rated nominal value of 2 kA and therefore current based fault detection would probably lead to unintended activation of the breakers in the adjacent lines. Using this detection only for pre-activation in combination with a more elaborate selective fault detection scheme may
be suitable to maintain fast operation and selectivity.

6.4. Findings of the Grid Study

In this chapter, the interruption performance of six circuit breaker concepts is evaluated for an exemplary MTDC network. This is done to compare the analytically derived performance and the interruption capability in a simple fault case (cf. Chapter 5) with a more realistic DC grid. Furthermore, the effects of the operation of the different circuit breakers on the healthy part of the MTDC network were investigated.

6.4.1. Circuit Breaker Performance

In all three investigated fault cases, both the nominal current and the rate of rise of the fault current are smaller than in the nominal fault case, investigated in Chapter 5. All circuit breaker concepts are able to operate in the MTDC network and the maximum current in the breaker is significantly below all breakers interruption capability. The internal current commutation time is the key indicator for comparing the circuit breakers speed of operation for a given EAP rating. In Figure 6.16, the average internal current commutation time for the three fault cases is illustrated for each circuit breaker concept. The ends of the black bar indicate the maximum and minimum internal current commutation time which was observed in one the grid study, the orange bar represents the analytically derived times (cf. Chapter 5).

For LCS-MB, Inj-LC and Osc-ES, the average internal current commutation time is almost identical to the expected value and the maximum deviation from the average value is below 1 ms. The Inj-PG concept operates with an insignificantly small speed variation in the MTDC grid, but an offset of approximately 1 ms is present, due to the smaller fault current and the consequently longer voltage rise time. The Inj-C circuit breaker operates in its best MTDC case as fast as expected from the simplified HVDC circuit, but in the worst case it operates 0.6 ms slower, which equals an internal current commutation time increase of +20% compared to the default fault case. The average internal commutation time is 0.2 ms slower than the predicted value. For the LCS-C, the average observed operation takes 1.6 ms longer than the circuit breaker investigation suggested. In its best MTDC case, the delay was only 0.7 ms, in its worst 3.7 ms. These observations equal an increase of the internal current commutation time by 25% to 225% compared to the ideal case. These deviations as well as their variation considerably exceed the observations made for other concepts. The longer times were consistently observed for the breakers at bus 3 where the fault current crosses zero and changes polarity. The, in comparison to bus 1, smaller fault current requires significantly longer time to charge the capacitor $C_{TB2}$ up to the trigger voltage level and even the charging of the Arming Branch capacitor takes considerably longer time, as can be calculated using formulas 5.10 and 5.11.

These results, especially of the three last discussed concepts, LCS-C, Inj-C and Inj-PG, confirm that the use of larger capacitors increases the internal current commutation
Figure 6.16.: Average internal current commutation time of all fault cases and busses by circuit breaker. The ends of the black bars indicate the maximum and minimum internal current commutation time observed for the specific circuit breaker. Orange bars indicate the analytically derived ideal current commutation times

time, more specifically the voltage rise time, considerably at small, non linear fault currents with a decreasing rate of rise of current due to the slower charging process.

6.4.2. Breaker Specific Network Behaviour

For all six circuit breaker concepts, the effect on the current in the adjacent links as well as on voltage at the adjacent busses during the interruption process was investigated.

In case of a fault, the currents in the adjacent links increase proportionally to the fault current and feed into the faulted link. When the circuit breaker was signaled and the internal current commutation has passed, the fault current decreases, and so do the currents in the adjacent links, at least towards their new post-fault steady state level. Consequently, as the study of the three fault cases confirmed, the peak current in adjacent links is proportional to the circuit breaker’s speed. This may become an issue if the current in the adjacent lines rises to a level, where it causes the local protection to initiate a breaker operation. Here, it may be possible to ensure selectivity of the protection with pre-activation, as offered by all investigated circuit breakers.

For all of the concepts, the peak current in at least one of the adjacent links exceeds the nominal current rating of most of the circuit breakers (2 kA). This clearly shows
that a fault protection based purely current threshold, as implemented in the basic HVDC network, would most probably result in a false alarm and trigger circuit breakers unnecessarily. Such a protection concept is not practical, whereas the implemented voltage based protection scheme provided short relay times and reliable detection. Nevertheless, a current based protection scheme may be used if the circuit breaker features pre-activation, to protect the components and to allow fast selective current breaking if necessary.

With respect to the bus voltage, measured by the converter controls between the two poles, no clear correlation to the employed circuit breaker is identified. Even though the different circuit breaker topologies affect the voltage within the first milliseconds by discharging the converter capacitor into the fault, the minimum and maximum voltage peaks, illustrated in Figure 6.17, are not proportional to the individual breaker specific times. The LCS-MB concept for example, has the shortest internal current commutation time in all investigated cases and the voltage at bus 1 deviates the fewest in all three fault cases when employing this circuit breaker. At bus 3, the highest overvoltage is observed for the fastest circuit breaker, LCS-MB, in two out of three cases, and for four of the five other, slower, circuit breakers smaller peak-to-peak differences are observed. This finding is probably due to transients caused by the fast switching speed of the semiconductors. Only when comparing the minimum pole-to-pole voltages of all circuit breakers and fault cases, as shown in Figure 6.18, a tendency towards lower minima with increasing internal current commutation time can be observed.

It is expected that, within the operation time of the fastest circuit breaker, the converter capacitor discharges to a very large extent into the fault, which causes approximately similar deviations for all circuit breakers. Subsequently it is mainly up to the converter control to recover from this discharge and hence, the post interruption voltage stabilization is very similar for the different circuit breakers, too.

It is also worth noting, that the maximum and minimum voltage only have very little effect on the bus voltage stabilization. As outlined for the different cases previously, most of the circuit breaker specific bus voltage equal out around 40 ms after the fault inception and are subject to a resonance of more than one frequency [LAB+15].
Figure 6.17: Minimum and maximum pole-to-pole bus voltages of all investigated cases (Upper plot bus 1, lower plot bus 3, for each circuit breaker from left to right fault case 1 to 3, 100 km from bus 1, 25 km from bus 1, at bus 1)
Figure 6.18.: Minimum and maximum pole-to-pole bus voltages of all investigated cases plotted against the internal current commutation time
7. Comparison HVDC Circuit Breakers

In this chapter, the combined findings for the fault interruption in the simplified fault case (Chapter 5) and the grid study (Chapter 6) are presented to identify the potential of the selected circuit breakers for future applications.

7.1. Circuit Breaker Speed

The time in which a circuit breaker is able to interrupt a fault current in an MTDC network is critical for a continuous operation of the network. To reduce disturbances in both adjacent HVDC links and AC systems as well as to avoid instable operation conditions for the converter stations close to the fault, circuit breakers have interrupt the fault within a few milliseconds.

The analysis of the circuit breakers in Chapter 5 promises internal current commutation times within 2 ms to 3 ms for the simplified fault case and the selected dimensioning. As all of the investigated solutions employ mechanical switches in the NCP, the shortest achievable operation time is determined by the opening time of the mechanical switch (UFD: 2 ms, VI: 2.5 ms).

Still, only two of the investigated concepts operate within 0.1 ms of this limit, LCS-MB and Inj-LC. For the other solutions, a time difference between the circuit breaker’s specific internal current commutation time and the opening of its mechanical switch between 0.16 ms to 1.04 ms is observed. This delay is primarily caused by and proportional to the size of the employed capacitor(s) which has (have) to be charged above the system voltage to stop the fault current, as summarized in Table 7.1.

Table 7.1.: Internal current commutation time, opening of mechanical switch, capacitor size

<table>
<thead>
<tr>
<th></th>
<th>LCS-MB</th>
<th>LCS-C</th>
<th>Inj-C</th>
<th>Inj-PG</th>
<th>Inj-LC</th>
<th>Osc-ES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Δt_{mech}</td>
<td>2 ms</td>
<td>2 ms</td>
<td>2 ms</td>
<td>2.5 ms</td>
<td>2.5 ms</td>
<td>2.5 ms</td>
</tr>
<tr>
<td>Capacitor(s)</td>
<td>-</td>
<td>7 µF</td>
<td>15 µF</td>
<td>6.5 µF</td>
<td>0.6 µF</td>
<td>1 µF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>120 µF</td>
</tr>
<tr>
<td>Δt_{CC} - Δt_{mech}</td>
<td>0.05 ms</td>
<td>1.04 ms</td>
<td>0.81 ms</td>
<td>0.44 ms</td>
<td>0.06 ms</td>
<td>0.16 ms</td>
</tr>
</tbody>
</table>

*Only the LCS-C’s Timing Branch 2 and Arming Branch capacitors affect the internal current commutation time for different fault currents. First C_{TB2} = 120 µF is charged to 48 kV before C_{AB} is charged to the TIV peak.*
When employed in the MTDC network, half of the circuit breakers operate almost with the same speed as in the nominal case, as shown in Figure 6.16. Only for the three solutions which use larger capacitors, namely Inj-PG, Inj-C and LCS-C, an increasing prolongation of the ideal internal current commutation time was observed with increasing size of the capacitor. This observation can be explained with the relatively small fault current which has to charge the capacitor to create a counter voltage, showing that the size of the capacitor increases the sensitivity of a circuit breakers internal current commutation time changes in the fault current level.

In the MTDC network, the maximum current peak in the links adjacent to the faulted line was identified to be proportional to the internal current commutation time of the circuit breakers. Furthermore, as shown in Figure 6.18 and already identified by Bucher and Franck ([BF16]), a trend towards lower minimum terminal voltages can be observed for decreasing internal current commutation times. When comparing the internal current commutation times to the maximum terminal voltages or the subsequent stabilization of the bus voltages, no clear trend can be identified.

Aside from the differences in internal current commutation time discussed in the previous section, all the circuit breakers were able to isolate the faulted line in all investigated fault cases in the MTDC in the range of 10 ms to allow the converter controls to return the network to a stable operation. Only the voltage based protection scheme prevented the circuit breakers of other links from tripping, whereas a current based detection scheme is likely to have triggered the circuit breakers of un-faulted lines as well.

### 7.2. Range of Application

The range of application of the circuit breakers in terms of maximum fault current has been analyzed and simulated in Chapter 5 and summarized in Section 5.7.3 with the finding that all but the Inj-LC circuit breaker are capable of interrupting currents below their rating. As explained in the previous section, for some of the circuit breaker concepts lower fault currents lead to an increased internal current commutation time. As outlined in Section 5.5, the Inj-LC concept imposes very high requirements on the interruption capability of the employed VI for the rated case already. The sensitivity analysis showed, that these demands increase further when interrupting smaller fault currents because of the steeper $\frac{dI_{cz}}{dt}$. For the smallest current interrupted in the MTDC network, 4.5 kA, an $\varepsilon$ of 617 kV/\(\mu\)s\(^2\) results. This exceeds the assumed limit of 140 kV/\(\mu\)s\(^2\) [Sla08] by far. If the VI technology can not fulfill these requirements, the dimensions of the circuit breaker have to be adjusted, e.g. for a VI specific $\varepsilon$ according to the proposed equation 5.36.

The other two circuit breaker concepts employing VI, Inj-PG and Osc-ES, impose lowers or significantly lower requirements. Inj-PG injects a pulse of smaller frequency and consequently smaller $\frac{dI_{cz}}{dt}$ and employs a larger capacitor for a smaller $\frac{dU}{dt}$, leading to an $\varepsilon = 82$ kV/\(\mu\)s\(^2\) for the smallest current of 5.2 kA interrupted in the MTDC network. For the Osc-ES solution, the oscillating current amplitude is controlled for
an approximately constant $\frac{di}{dt}$ to ensure the interruption. Only LCS-MB, Inj-PG and Osc-ES have a considerable margin for interrupting fault currents above the standard ratings they were dimensioned for ($I_N = 2 \, \text{kA}$, $\frac{di}{dt} = 3.2 \, \text{kA} \, \mu \text{s}^{-1}$, trip signal at 2.4 kA). In case the fault currents exceed the circuit breakers’ interruption capability, either the series connected current limiting reactor can be increased, or the circuit breaker must be upgraded. An upgrade for higher fault current ratings was estimated to be relatively simple and without mayor investments for Osc-ES, Inj-PG and Inj-C, whereas for the other solutions considerably higher efforts or costs are expected, as summarized in Table 5.5. Last but not least, current oscillations between circuit breaker and grid after interruption have to be considered for the Inj-LC and the Osc-ES concept. These disturbances on the one hand put additional requirements on a residual current switch, used to provide a galvanic insulation, and on the other hand may affect the converter control negatively as the oscillations influence the converter capacitor, too. For the Inj-LC this issue can be solved by employing turn-on semiconductors in the CCP, as proposed by [KCHM15], but for the Osc-ES no practical solution was identified.

### 7.3. Features

The potential of the different circuit breakers to overcome the relay time, and especially the commutation delay for a trip signal if given by remote controller, and to allow a fast continuation of the power transmission in case of a momentary fault was investigated qualitatively. As listed in Table 7.2, all of the investigated circuit breakers allow pre-activation based on a local fault detection scheme. Limiting the current during the pre-activation phase is only featured by the LCS-MB circuit breaker. To perform a fast Open–Close–Open sequence, to resume operation after a momentary fault is only possible out of the box with the LCS-MB and the Inj-C concepts. LCS-C, Inj-PG and Inj-LC have to be modified for this purpose, e.g. equipped with a fast discharging unit. Osc-ES does not provide this feature.

<table>
<thead>
<tr>
<th></th>
<th>Pre-activation</th>
<th>Current limiting</th>
<th>O-C-O</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCS-MB</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>LCS-C</td>
<td>Yes</td>
<td>Limited</td>
<td>discharge $C_s$</td>
</tr>
<tr>
<td>Inj-C</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Inj-PG</td>
<td>Yes</td>
<td>No</td>
<td>close VI under $U_N$, discharge $C$</td>
</tr>
<tr>
<td>Inj-LC</td>
<td>Yes</td>
<td>No</td>
<td>close VI under $U_N$, discharge $C$</td>
</tr>
<tr>
<td>Osc-ES</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>
7.4. Breaker Design

Even though this work does not evaluate the design costs of the different circuit breakers, a short qualitative overview on the used components is given in the following.

**LCS-MB** The LCS-MB circuit breaker requires a high number of turn-off semiconductors to provide more than twice (because bidirectional) the TIV rating. Turn-off semiconductors are expected to be the most costly of the considered semiconductors and cause a higher voltage drop and consequently conduction losses (cf. Table 4.2). The general circuit breaker topology is relatively simple, but the control and employment of the semiconductors, e.g. the large number of gate driving circuits that have to be controlled, is expected to be demanding. The nominal losses occurring in the NCP have to be considered in cost comparison.

**LCS-C** The LCS-C circuit breaker concept mainly uses turn-on semiconductors, whose rating in total has to exceed four times the TIV. However, this is still expected to be cheaper than the turn-off semiconductors in the LCS-MB solution [DGC11]. The passive components must be dimensioned carefully as they strongly influence the interruption capability. The control of the multi-branch design requires several metering and control units, and the grading of the voltage across the capacitors is expected to be challenging. Even though the multi-branch design makes it possible to use large capacitances for smaller voltages only, the overall amount of capacitors is high and will be reflected in the costs of the solution. As for LCS-MB, the conduction losses in the NCP are not negligible.

**Inj-C** The Inj-C circuit breaker, with two turn-off semiconductor branches bridged by one capacitor, relies on a total semiconductor rating of above eight times the TIV. Their costs are expected to be in the range of the LCS-MB semiconductors. The, in comparison to the other concepts relatively large, capacitor has to be rated for the TIV as well, probably resulting in large space requirements. A fast and reliable control for the different semiconductor stacks is required. The nominal conduction losses on the NCP are about half of those occurring in LCS-MB and LCS-C.

**Inj-PG** The Inj-PG design requires turn-on semiconductors rated for the TIV level as well as diodes with a total rating of above five times TIV. When realizing the Inj-PG design in a modular way, as proposed in [WM13], ensuring a simultaneous control of the turn-off semiconductors may be challenging but the insulation requirements for the passive components are reduced. The nominal losses in the mechanical VIs are negligible, but the control of the synchronous operation of a, compared to the UFD technology, large number of series connected mechanical switches as well as the grading of the voltage and its rate of rise across the units is expected to be a major challenge.
Inj-LC  In the Inj-LC circuit breaker, no semiconductors but only mechanical switches and passive components are employed, making this concept presumably relatively cheap. On the other hand, the same challenges with respect to the VIs arise as for the Inj-PG concept.

Osc-ES  The principle design of the Osc-ES concept is rather simple, with only passive components on the CCP. But as for Inj-LC and Inj-PG, the series connection of VI is assumed to be challenging. The ES on the NCP, turn-off semiconductors, is similar to the LCS in LCS-MB and LCS-C in terms of costs and conduction losses. However, in contrast to the LCS concepts, the ES needs a faster control for resonant switching and higher stress as well as switching losses than in the LCS are expected.
8. Conclusion and Outlook

For this work, six promising DC circuit concepts were selected out of the most relevant publications to investigate their applicability in HVDC systems. With this intention, the interruptible current and the operation time of these concepts were derived analytically and detailed circuit breaker models, compatible for simulation in different networks, were developed to verify the analytical findings by simulations. The simulations were divided into two parts. In the first, a simple test circuit, creating a linear rate of rise of the fault current, was implemented. The second consists of an exemplary MTDC network, which was used to investigate grid related phenomena like the influence of traveling wave effects on the breaker performance. Additionally, technological challenges and limitations of the used components and the design were elaborated. In the following paragraphs, the main findings are summarized and interpreted.

Limitations of Investigated Circuit Breakers

Based on the analysis of the circuit breakers’ operation principles, the topologies were dimensioned to interrupt fault currents of at least up to 10 kA within minimum time. The observed internal current commutation times, from breaker signaling to the TIV peak, were in the range of 2 ms to 3 ms for each breaker. The main contributing factors for this time are the operation time of the mechanical switch as well as the charging time of capacitors used in the respective topologies. The latter one is largely affected by both the capacitance of the capacitor as well as the height and rate of rise of the fault current. As the capacitor influences the maximum interruptible current in all but the LCS-MB solution, the improvement of the mechanical opening time of the UFDs and VIs was identified as the most rewarding optimization for faster operation. The components that define the maximum interruptible current are different for each circuit breaker and are listed in Table 5.5. In general, except for LCS-MB, higher current ratings can be achieved by the series connection of additional respectively fewer components. In contrast, for the LCS-MB concept, the semiconductor current carrying capability imposes a hard limit, which may only be exceeded by adding another stack of turn-off semiconductors in parallel to the MB.

For all investigated solutions, increasing the interruption capability comes with a trade-off, ranging from significantly higher costs (LCS-MB), to increasing nominal conduction losses (Inj-C) to a decrease in speed (Inj-PG, LCS-C), to increasing insulation requirements (Osc-ES) or at the costs of problems with the interruption of smaller currents (Inj-LC) with respect to the technological limits of the VI technology. Aside from the $\frac{dI}{dt} - \frac{dU}{dt}$ characteristic, which were identified as a critical limit for current interruption in case of the Inj-LC concept, the application of VI in HVDC
circuit breakers is assumed to be the main challenge for all the VI-based circuit breakers, mostly in terms of series connection in combination with fast opening and voltage grading, which has not been realized yet to the extent necessary for the investigated voltage level.

From an economical point of view, the conduction losses and therefore the application of semiconductors in the NCP should be reduced to minimum, e.g. by using the thyristor technology instead of turn-off semiconductors (Inj-C) or wide-bandgap semiconductors, which are still in development but promise improvement in terms of higher ratings and lower losses. However, the available semiconductor technology can be used in the circuit breakers, preferably in the current commutation path, without their limits negatively affecting the switching procedure or reducing the interruption limits in a critical way.

For some of the circuit breaker concepts, especially LCS-C, the assumed stray inductance was found to have significant influence on the dimensioning of the circuit breakers and on the interruptible current and therefore must be well-known and defined for an optimal design.

**Performance of Circuit Breakers in MTDC Networks**

All circuit breakers were capable to interrupt the three fault cases tested in the investigated 4-terminal MTDC network that is expected to be representative for future small offshore grids. Furthermore, faster circuit breakers with shorter fault current neutralization times were found to reduce the peak surge current in the adjacent lines feeding into the fault. However, higher circuit breaker speed does not affect the transient voltage peaks or its stabilization, which seems to be controlled by the converter stations independently of the employed circuit breakers.

For all circuit breakers, the operation took longer than in the simplified test circuit. The smaller fault current of the MTDC network, which showed a considerable decrease in rate of rise of fault current, required a larger time for the circuit breakers to charge their internal capacitors to the required voltage levels. For some circuit breaker concepts, e.g. LCS-C, the MTDC study showed, that the internal commutation is highly sensitive towards the fault current, which confirmed findings of the simpler test circuit. This sensitivity may be a significant disadvantage compared more robust circuit breakers, such as LCS-MB or Inj-PG in case of a larger MTDC network with a wider variation of possible fault currents and may limit the use of the respective circuit breakers to smaller networks with a smaller variety of possible fault currents or these circuit breakers necessitate additional measures to ensure safe and fast operation in all possible fault situations. Additionally, the conducted study clearly shows that a strictly linear rising fault current, as frequently referred to when testing or simulating HVDC circuit breakers, may indicate significantly higher interruption capabilities than can be realized in grid applications. Hence, it has to be pointed out that, especially for topologies that rely on the charging of large capacitances, low or decreasing rates of rise of fault current can be considerably more challenging than comparably high rates of rise or signaling thresholds.
As outlined in Chapter 7, another finding of the MTDC study are oscillations in circuit breaker concepts with resonant circuits in the CCP in the case of pole-to-pole faults along the low-ohmic fault, the circuit breaker on the opposite pole and the converter capacitor, occurring after the interruption of the current in the NCP in case the CCP cannot be disconnected (Osc-ES, Inj-LC). These oscillations have to be taken into account when specifying the interruption capability of the residual current switch. Furthermore, when using these circuit breakers, the possible reactions of a specific converter control to these oscillations have to be studied.

All of the circuit breakers feature pre-activation to a certain extent, but as time is critical and signal propagation delays from remote control are in the range of milliseconds [Buc14], it is more likely that circuit breakers in MTDC networks will rely on local fault detection concepts, e.g. [SR14], and therefore the pre-activation feature is not expected to be a necessity. The capability of performing a fast Open–Close–Open operation however is expected to be necessary for HVDC power transmission with overhead lines, as momentary faults are frequent and more likely to occur on these lines than on cables. Most of the investigated circuit breakers, except for LCS-MB and Inj-C, do not provide this feature by default but at least require additional modifications, such as fast discharging circuits for the capacitors, to quickly restore the pre-fault state.

Regarding the grid study, it has to be stressed out that the properties of individual MTDC networks will most probably vary considerably from each other. Hence, every MTDC grid can only be understood as exemplary and while it may be used to point out specific effects, due to differences in topology and implementation, e.g. number of terminals, length of links and cable properties as well as converter control, general statements should be derived carefully from such grids.

Nevertheless, the performance of the selected circuit breakers in the MTDC network study shows a large correspondence with expectations based on the analytical investigation. This suggests that all the investigated circuit breakers can theoretically be employed in MTDC networks with faults in the investigated range. The selection of a concept will be largely based on network specific requirements, such as the maximum interruption time, demands for special features (O-C-O capability, current limiting) and last but not least the necessary investment.

Outlook

This work provides a fundamental case study of six different promising HVDC circuit breaker concepts, which represent a variety of possible interruption principles for direct current. Simulations show, that these circuit breakers are in principle applicable in MTDC networks. The individual properties of the circuit breaker concepts make them suitable for different networks. However, before installing one of the solutions in a real grid, further studies have to be conducted and it may be necessary to improve some of the component ratings.

The VIs interrupter technology, which is used in three of the investigated solutions, provides advantageous interruption characteristics compared to gas circuit breakers.
This is for example due to the ability to interrupt steeper current slopes and better insulation properties for small gaps compared to gas circuit breakers, which makes vacuum interrupters more suitable for fast opening. Nevertheless, fast opening has up to now only been reported for single units, however for higher voltage ratings series connections of several VIs will be necessary. This in turn is rather challenging, since not only an equal voltage distribution during the transient opening phase has to be ensured, but also a precise synchronization of the mechanical operation is necessary. UFD prototypes, in contrast, already have achieved opening times of 2 ms and reportedly are capable to withstand HVDC voltages. However, both technologies are new in this field of application and elaborated investigations of their long-term reliability are required.

The conducted MTDC grid study showed, that interruption capabilities derived from a simplified HVDC network, assuming a linear rising fault current without accounting for traveling voltage waves, can differ significantly from the circuit breakers capabilities in a more realistic network. This shows the importance of fault current envelopes and the development of representative test circuits. For future simulations, this finding can be used to derive more suitable test cases that do not necessitate the complexity of a grid simulation but cover all important aspects of the current interruption.

To evaluate a specific circuit breaker’s functionality in a prospective MTDC grid with a specific converter model, an elaborate analysis should also cover the effects of the fault and the respective neutralization time on the connected AC grids. Furthermore, the circuit breaker’s specific worst case fault should be identified as proposed in [SR14]. Such investigations were omitted in the scope of this work as the outcomes depend to a large extent on the converter model and control, respectively. This hinders the comparison of different concepts, but will be compulsory for the planning of a specific MTDC grid.

From the system perspective, the MTDC network study suggests, that the disturbance of the bus voltage is similar for fast circuit breakers which build up the TIV within 2 ms to 3 ms. Based on this finding, converter development should consider control mechanisms that ensure a fast voltage stabilization after a successful fault interruption based on the disturbances observed for the circuit breaker concepts.

A shortcoming of this work’s MTDC study is the restriction to HVDC cables, as the transient waves of faults in overhead lines travel at significant higher speed and the line parameters induce different fault current curves [SR14]. For subsequent circuit breaker studies in MTDC networks it is recommended to include different link types, as in [BF16].
Bibliography


List of Acronyms

AC Alternating current
CB Circuit breaker
CCP Current commutation path
CSC Current-source converter
CZ Current zero
DB Damping branch
DC Direct current
EAP Energy absorbing path
ES Excitation Switch
HVDC High voltage direct current
IGBT Insulated-Gate Bipolar Transistor
LCS Load Commutation Switch
MB Main breaking unit
MMC Modular Multi-Level Converter
MOV Metal-oxide varistor
MTDC Multi-terminal direct current
NCP Nominal current path
PG Pulse generator
TIV Transient interruption voltage
TSG Triggered spark gap
UFD Ultra-Fast Disconnector
VI Vacuum interrupter
VSC Voltage-source converter

Circuit Breaker Acronyms

LCS-MB Load Commutation Switch - Main Breaking Unit
Osc-ES Divergent Oscillation - Excitation Switch
LCS-C Load Commutation Switch - Capacitor
Inj-LC Current Injection - LC Circuit
Inj-PG Current Injection - Pulse Generator
Inj-C Current Injection - Capacitor
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A. Supplementary data DVD

A.1. Description

The enclosed supplementary data DVD contains the PSCAD models developed for this thesis to foster further research of DC circuit breaker solutions as well as to allow re-use and improvement of the existing models. The results of all mentioned simulation scenarios, discussed in this thesis, are provided as MATLAB files to ease subsequent data processing. Furthermore, the MATLAB functions developed and used for data import, conversion and processing are included on the supplementary data DVD.

A.2. Content

The supplementary data DVD contains three folders, 1 Simulation models (PSCAD), 2 Data import and processing (MATLAB) and 3 Simulation results (MATLAB)

A.2.1. Simulation models (PSCAD)

1 Simplified HVDC Circuit

For the simplified HVDC circuit, two sets of the investigated circuit breaker models are provided. In the detailed circuit breaker models components are modeled with protective elements and the currents and voltages of all components as well as their rates of rise are measured. The simplified circuit breaker models only provide the components essential for the circuit breaker operation and measurements are reduced to the path currents and the circuit breaker voltage.

In both cases, the simplified HVDC circuit simulation environment is almost similar, including measurements of the system voltages and currents as well as of the times as described in Chapter 4.

To run the simulation of one of the circuit breaker concepts, the PSCAD case file with the concept’s name as well as the appending PSCAD library file, contained in the respective folder, have to be loaded into PSCAD.

2_0 HVDCGridTestSystem [Leterme et al 2015]

The unmodified HVDC grid Test system, as obtained from www.esat.kuleuven.be/electa/hvdcresearch/hvdc-test-grid in September 2015, is stored on the supplementary data DVD as a backup version.
2_1 MTDC Simulation – Circuit Breakers without residual current switch – Snapshots at 700ms

The MTDC network simulation files, whose results have been discussed in Chapter 6, are provided for each of the circuit breaker concepts. To run a specific fault case with one of the circuit breakers, the PSCAD case file of the circuit breaker concept’s name has to be loaded into PSCAD. A snapshots of the moment of fault occurrence can be loaded as well, to start the simulation from this specific time to reduce the time necessary for simulation. The fault case to be simulated is specified by setting the fault case element in the cable 13 module to the respective fault case number.

2_2 MTDC Simulation – Circuit Breakers with residual current switch – Snapshots at 700ms

To allow a clear identification of the instant when the leakage current is reached, circuit breaker models with a residual current switch, as described in Section 4.2.6, are provided.

To run the MTDC network simulation of one of the circuit breaker concepts, the respective PSCAD case file has to be loaded into PSCAD. To allow less simulation effort, snapshots of the moment of fault occurrence are provided, from which the simulation can be started to avoid simulating the start up of the grid. To simulate one of the three investigated fault cases, the fault case element in the Cable 13–module has to be set to the according fault case number.

A.2.2. Data import and processing (MATLAB)

For importing the PSCAD simulation output into MATLAB, several MATLAB function files were developed or extended.

importPSCADdata.m Imports all stored PSCAD output data into a MATLAB struct file and plots the channels, each in a single graph.

importPSCADchannels.m Imports selected channels of the PSCAD output data into a MATLAB struct file and optionally plots the channels, each in a single graph.

importMTDCCase.m Imports the PSCAD output data of an MTDC network simulation into a MATLAB struct file and identifies the channels’ modules. Channels are plotted in graphs by identified group and unit.

PSCADdataCutter.m Extracts selected channels between a defined start and end point from a struct file.

Volt_Cur_plotAlign.m Creates uniform plots of the circuit breaker voltage and path currents, recommended to use with output of PSCADdataCutter.m.
A.2.3. Simulation results (MATLAB)

The struct files, containing all measurements obtained from simulation of the different fault scenarios, are included on the supplementary data DVD.

For the simplified HVDC circuit, the circuit breaker specific results are provided for both the detailed circuit breaker models and the simplified circuit breaker models.

For the MTDC simulation, simulation results for each circuit breaker in each of the three investigated fault cases are included for both models, with residual current switch and without residual current switch.
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