Highly Efficient Pulse Modulator System with Active Droop Compensation for Linear Colliders

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Abstract

At the European Organization for Nuclear Research (CERN) a new type of particle accelerator, the Compact Linear Collider (CLIC), is currently investigated. For the acceleration concept, 1230 radio frequency amplifiers, so called klystrons, are deployed. Each of the 1230 klystrons requires a pulse modulator system. Therefore, the concept of a 29 MW pulsed modulator system for driving a single klystron is investigated in this thesis.

High demands are set on the pulse modulator system. Particularly, the high pulse energy, the short pulse rise time in relation to the flat-top interval and the high repeatability of the output voltage during the pulse flat-top are challenging. The concept of the proposed modulator system is based on the storage of energy in a main capacitor bank, pulse generation via solid state switches and the translation of the voltage level utilizing a pulse transformer. The modulator system can be divided into three major parts which are the medium voltage charging system, the droop compensation system including the pulse generation units and the pulse transformer. To meet the demanding specifications, it is essential to optimize all three parts of the modulator system.

The highest impact on the repeatability of the modulator’s output voltage is exerted by the charging voltage precision of the main capacitor bank prior to the pulse interval. Thus, a high power, medium voltage capacitor charging unit is designed, which ensures a highly repeatable capacitor charging voltage. The charging concept is based on a modular approach with six interleaved charging modules, operating in boundary conduction mode. The operation principle and predicted performance is validated with a 240 kW prototype system. An efficiency of 96.3% for a single charging unit has been obtained. Further, a repeatability analysis of the charging concept, that investigates the impact of various parameters on the repeatability is conducted. The analysis results that with the chosen design a highly precise charging voltage of $\sigma = 7.3 \, \text{ppm}$ standard deviation in relation to the charging voltage level is achievable.

In order to compensate the voltage droop in the main capacitor bank during the pulse interval, a high dynamic, active droop compensation system with low output current ripple is desired. Thus, a new converter topology is proposed in this thesis, which meets the requested
system dynamics. With a modular approach of 24 interleaved bouncer converters, grouped into four pulse units, a current ripple of below 1% per pulse unit is realized. The operation principle during the pulse, the recharging process and the converter interleaving has been validated. Additionally, the repeatability of a single charging unit for open loop and current mode control (CMC) operation of the bouncer modules is investigated. The analysis results, that with CMC the charging precision of the bouncer modules’s input voltage can be relaxed by a factor of 20 maintaining equal system repeatability. Combining this analysis with the repeatability analysis of the main capacitor bank’s charging voltage, an overall system repeatability below 100 ppm can be derived. Since the pulse transformer design must show a high conversion efficiency and a short pulse rise time, a multi objective pulse transformer optimization procedure is proposed in this work. The procedure models the parasitics of the pulse transformer for a broad range of geometries, considers all major loss components and includes an isolation model for the pulse transformer. The sensitivity on parameters of the overall transformer design is investigated and an optimal transformer design for CLIC is derived. The validity of the procedure is shown by a full scale transformer prototype, where ten consecutive pulses under nominal conditions were demonstrated. A 4 µs pulse time to flat-top has been achieved with an ohmic load.

In conclusion, this thesis designs, optimizes and realizes the different parts of the 29 MW pulse modulator system in such a way that the demanding specifications for an application in the future Compact Linear Collider are met.
Kurzfassung


An das Pulsmodulatorsystem werden hohe Anforderungen gestellt. Insbesondere die hohe Pulsenergie, die kurze Pulsanstiegszeit im Verhältnis zur Pulsdauer und die wiederholgenaue Pulsausgangsspannung (PPR) während des Pulsdachintervals sind herausfordernd. Das vorgestellte Pulsmodulatorkonzept basiert auf der Speicherung der Pulsenergie in einer zentralen Kapazitätsbank, der Erzeugung von Pulsen mithilfe von Halbleiterschaltern und auf einem Pulstransformator, der die Anpassung an die benötigte Pulsausgangsspannung vornimmt. Das Pulsmodulatorsystem kann in drei Teile untergliedert werden: eine Kondensatorladeeinheit auf Mittelspannungsebene, ein Kompensationssystem, welches die Pulsform bereitstellt und dabei den Spannungsabfall in der Kapazitätsbank ausgleicht, und ein Pulstransformator. Um die hohen Anforderungen an das Pulsmodulatorsystem zu erfüllen, müssen die verschiedenen Teilsysteme auf die jeweiligen Anforderungen optimiert werden.

Den größten Einfluss auf die Wiederholgenauigkeit der Pulsausgangsspannung übt die Ladespannung der Kapazitätsbank zu Beginn des Pulsdintervals aus. Daher wird in dieser Arbeit eine Kondensatorladeeinheit mit hoher Ladeleistung entwickelt, die eine wiederholgenaue Ladespannung der Kapazitätsbank liefert. Das Ladekonzept basiert auf sechs Ladeeinheiten, die zeitlich versetzt einander im Grenzleitungsmodus arbeiten. Das Funktionsprinzip und die vorhergesagte Effizienz werden mit einem 240 kW Prototypensystem bestätigt, wobei die Effizienz einer einzelnen Ladeeinheit 96,3 % beträgt. Des Weiteren wird in dieser Dissertation eine Wiederholgenauigkeitsanalyse der Kondensatorladeeinheit durchgeführt, in der die Einflüsse verschiedener Parameter auf die wiederholgenaue Ladespan-
nung untersucht werden. Die Analyse zeigt, dass mit den realisierten Parametern eine Standardabweichung der Ladespannung bezogen auf das Ladespannungslevel von \( \sigma = 7.3 \text{ ppm} \) erreicht werden kann.


Zusammengefasst werden in dieser Dissertation die verschiedenen Teilsysteme eines 29 MW Pulsmodulatorsystems entworfen, optimiert und umgesetzt, sodass diese die anspruchsvollen Spezifikationen für den Einsatz im zukünftigen Linearbeschleuniger CLIC erfüllen.
Abbreviations

2D ... Two Dimensional
AC ... Alternating Current
ADC ... Analogue Digital Converter
BCM ... Boundary Conduction Mode
BNC ... Bayonet Neill Concelman
CERN ... European Organization for Nuclear Research
CLIC ... Compact Linear Collider
CMC ... Current Mode Control
CRC ... Cyclic Redundancy Check
CSM ... Charge Simulation Method
CSPI ... Cooling System Performance Index
CUT ... Core Under Test
DAC ... Digital Analogue Converter
DC ... Direct Current
EtherCAT ... Ethernet for Control Automation Technology
FEM ... Finite Element Method
FFT ... Fast Fourier Transform
FPGA ... Field Programmable Gate Array
FTS ... Flat-Top Stability
HV ... High Voltage
IGBT ... Insulated Gate Bipolar Transistor
ITER ... International Thermonuclear Experimental Reactor
LHC ... Large Hadron Collider
LI ... Lightning Impulse
MOSFET ... Metal-Oxide-Semiconductor Field-Effect Transistor
MTBF ... Mean Time Between Failure
PCB ... Printed Circuit Board
OV ... Overvoltage
OC ... Overcurrent
P-controller ... Proportional Controller
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>PETS</td>
<td>Power-Extraction and Transfer Structures</td>
</tr>
<tr>
<td>PFL</td>
<td>Pulse-Forming Line</td>
</tr>
<tr>
<td>PFN</td>
<td>Pulse Forming Networks</td>
</tr>
<tr>
<td>PI-controller</td>
<td>Proportional-Integral Controller</td>
</tr>
<tr>
<td>PLC</td>
<td>Programmable Logic Controller</td>
</tr>
<tr>
<td>POF</td>
<td>Polymer Optical Fiber</td>
</tr>
<tr>
<td>PPR</td>
<td>Pulse Repeatability</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>SHV</td>
<td>Save High Voltage</td>
</tr>
<tr>
<td>SNF</td>
<td>Swiss National Foundation</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>SwissFEL</td>
<td>Switzerland’s X-Ray Free-Electron Laser</td>
</tr>
<tr>
<td>SPRC</td>
<td>Series-parallel resonant converter</td>
</tr>
<tr>
<td>SFP</td>
<td>Small Form-Factor Pluggable</td>
</tr>
<tr>
<td>SI</td>
<td>Switching Impulse</td>
</tr>
<tr>
<td>TCM</td>
<td>Triangular Current Mode</td>
</tr>
<tr>
<td>VT</td>
<td>Voltage-Time</td>
</tr>
<tr>
<td>ZVS</td>
<td>Zero-Voltage Switching</td>
</tr>
</tbody>
</table>
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This thesis focuses on the development of a pulse power modulator system. Pulse power has a broad field of applications such as in the medical field (e.g., proton therapy \[1\]), in the industrial field (e.g., liquid food sterilization \[2\]) and in science (e.g., SwissFEL and ITER \[3\] \[4\]) leading to various different energy transmission concepts. The term *pulse power modulator system* describes a system, which transfers energy from the system’s input to its output load during a short time span, the pulse interval. Subsequently, the power transmission is interrupted for a certain period, the pulse pause.

The general structure of a pulse power modulator system is depicted in Fig. 1.1. The pulse modulator is connected to the alternate current (AC) grid. Usually, the energy intake at the system’s input is constant. Since the transferred energy during the pulse interval is typically higher than the energy intake during that time, an energy storage element is required. The majority of systems applies a capacitor bank for energy storage and thus, necessitates a conversion stage from alternate...
to direct current (AC/DC stage). In most cases, the pulse pause is significantly larger than the pulse width and both states are alternated with a certain frequency. In order to generate this alternating pattern, the modulator requires a pulse forming system. Since the pulse forming system does often not directly produce the desired output pulse shape, a pulse correction stage can be applied. This correction stage can be connected to the pulse forming system in series or in parallel. Finally, the desired pulse shape is transferred to the load at the output of the pulse modulator.

In the following, the application for the realized pulse power modulator system and the given specifications are presented.

1.1 Specifications of investigated pulse power modulator system

The pulse modulator system designed and developed in this thesis is constructed for the European Organization for Nuclear Research (CERN). At CERN, a new type of particle collider, the so called Compact Linear Collider (CLIC), is investigated.

The new particle collider CLIC features collision energies in the range of tera-electron volt (TeV). The accelerated particles in CLIC are electrons and its antiparticles (positrons), which belong to the particle class of the leptons. A lepton accelerating structure presents a complementary experiment to the existing Large Hadron Collider (LHC) that is based on the acceleration of hadrons (protons or lead ions). Compared to the existing LHC collider where hadrons can be accelerated and collided on a circular path, the acceleration of leptons in CLIC requires a linear acceleration path due to the light mass of the particles.

For such a linear collider, klystrons are used to accelerate the particles. A klystron can be viewed as a converter which transforms electrical energy into radio frequency ($RF$) power. The obtained $RF$ power is then utilized to accelerate the particle beam.

In a classical acceleration scheme, the klystrons to provide their produced RF power to drive the main particle beam. If such a classical scheme had been selected, up to 35000 accelerating klystrons would have been required to provide the collision energy for CLIC [5]. Since this high number of klystrons is not feasible in practice, a new acceleration scheme is investigated at CERN. The new acceleration scheme
Figure 1.2: Schematic overview of the Compact Linear Collider (CLIC)\textsuperscript{[5]}. The acceleration principle is based on an energy transfer from a drive beam to the main beam.
is based on the energy transfer from a drive beam to the main beam by power-extraction and transfer structures (PETS). Due to this new acceleration principle, the number of klystrons can be reduced to 1230. An overview of the CLIC acceleration scheme and structure is given in Fig. 1.2.

The required electrical power for each klystron during the pulse interval is 29 MW, that needs to be provided by a pulse power modulator system. Therefore, a total number of 1230 pulse modulators systems will be required for the final CLIC system. The focus of this thesis is the design, investigation and construction of a single 29 MW pulse power modulator system. This pulse power modulator system will then be provided to CERN and thereafter be employed in a first feasibility study of CLIC, which is not in the scope of this thesis.

Different klystrons with various specifications are investigated at CERN regarding their feasibility for the new linear collider. Hence, the pulse modulator system developed in this thesis has to be designed in such a way that it can supply the entire voltage and current range of interest. The resulting specifications of the pulse modulator system

<table>
<thead>
<tr>
<th>Numbers of klystrons</th>
<th>$N_{\text{klystron}}$</th>
<th>1230</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse voltage range</td>
<td>$V_{\text{pulse,range}}$</td>
<td>150 ... 160 ... 180 kV</td>
</tr>
<tr>
<td>Pulse current</td>
<td>$I_{\text{pulse,range}}$</td>
<td>193 ... 181 ... 161 A</td>
</tr>
<tr>
<td>Primary voltage range</td>
<td>$V_{\text{prim,range}}$</td>
<td>2.5 ... 2.66 ... 3 kV</td>
</tr>
<tr>
<td>Primary current range</td>
<td>$I_{\text{prim,range}}$</td>
<td>11.6 ... 10.86 ... 9.66 kA</td>
</tr>
<tr>
<td>Load range (eq. $R$)</td>
<td>$R_{\text{load,range}}$</td>
<td>777 ... 883 ... 1118 Ω</td>
</tr>
<tr>
<td>Designed peak power</td>
<td>$P_{\text{peak}}$</td>
<td>35 MW</td>
</tr>
<tr>
<td>Required power</td>
<td>$P_{\text{out}}$</td>
<td>29 MW</td>
</tr>
<tr>
<td>Rise + settling time</td>
<td>$t_{\text{settle}}$</td>
<td>8 µs</td>
</tr>
<tr>
<td>Flat-top length</td>
<td>$t_{\text{flat}}$</td>
<td>140 µs</td>
</tr>
<tr>
<td>Flat-top stability</td>
<td>$FTS$</td>
<td>0.85 %</td>
</tr>
<tr>
<td>Highest overshoot</td>
<td>$os$</td>
<td>1 %</td>
</tr>
<tr>
<td>Repetition rate</td>
<td>$Rep_r$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Total efficiency</td>
<td>$\eta_{\text{ges}}$</td>
<td>90 %</td>
</tr>
<tr>
<td>Pulse repeatability</td>
<td>$PPR$</td>
<td>$\leq$ 100 ppm</td>
</tr>
</tbody>
</table>
including the specified operation range are listed in tab. 1.1. The modulator system has tight specifications regarding the pulse flat-top stability and voltage overshoot. Due to the high number of pulse modulators, but a limited power supply at CERN, the efficiency from grid to klystron including the pulse efficiency has to exceed 90%. Furthermore, a highly demanding pulse repeatability below 100 ppm is required. There exist several types of pulse power modulator systems. Therefore, in the following, the state of the art is summarized and the most suitable pulse modulator topology for the given CLIC specifications is selected.

1.2 Pulse modulators-state of the art

Pulse power modulators are utilized in a broad range of applications. Their electrical energy ranges from mJ to MJ with pulse intervals from ns up to ms[6]. Their repetition rate varies from single shot to several thousand pulses per second [6]. In the following, an overview on five common modulator topologies for klystron loads is given:

- Line-type modulators, such as pulse-forming line (PFL) and pulse forming networks (PFN)
- Modulator concepts with a single high voltage switch
- Modulators based on the Marx principle
- Modulators with pulse transformers
- Resonant topologies with a medium frequency transformer and a passive rectifier stage

1.2.1 Line type modulators

A pulse forming line type modulator (PFL) makes use of the parasitic elements in an electrical transmission line [7, 8]. The basic structure is displayed in Fig. 1.3a). Since the inductance and capacitance per unit length of a transmission line are limited, pulses are typically in the ns-range to keep a reasonable modulator size [9, 11].

To overcome the size limitation of PFL modulators, pulse forming network type modulators (PFN) model the parasitics of a transmission
INTRODUCTION

Figure 1.3: a) Pulse forming line type modulator (PFL) with the impedance of the transmission line matched to the complex load. b) Pulse forming network type modulator (PFN), which models the transmission line characteristic with concentrated elements.

line with concentrated elements i.e., capacitors, inductors and resistances, as displayed in Fig. 1.3b). Applying this technique, also pulse lengths in the 100 us range are achievable [12]. There are different methods arranging the components and considering non-linear load behavior [12-14]. The resonances between the different elements must be coordinated since a rectangular pulse shape at the load is desired. A challenge presents the flat top ripple of the output pulse, as for a perfect rectangular shape an infinite number of harmonics would be required, which would result in an infinite number of circuit elements. In order to address this issue, inductors of different stages can be coupled (Guillemin type E), thus, improving the pulse shape [15, 16]. Another approach is to use a switched converter to compensate the PFN ripple on the flattop [17].

Since all components must withstand the desired output voltage, typically PFN modulators are limited to an output voltage of 10-20 kV. For higher output voltages, PFN modulators are either combined with Marx generators or with pulse transformers [16, 18, 19].
1.2.2 Modulators with single high voltage switch

Another concept for pulse modulators presents the application of a single high voltage (HV) pulse switch, which is depicted in Fig. 1.4. The advantage of such a concept is its simple modulator structure. A major drawback of this topology is, that all system components are subjected to the high output voltage level. This requirement is especially challenging for the pulse switch. But also the capacitor charging unit must feature a high voltage isolation. Therefore, the entire modulator is usually placed in oil [20, 21]. If air is applied as insulation media, a large isolation distance to the surrounding will result.

One class of high voltage switches are the triggered spark gap switches. The devices consist of two main electrodes with spherical shape, which can withstand a high electrostatic field. Additionally, a trigger electrode, which is at a floating potential, is placed either inside the spheres or in the gap of the spheres [22]. The inter-electrode insulator is mainly gaseous (e.g., SF6, vacuum, hydrogen, air) but also water has been applied as insulator [9, 22, 25]. To turn the switch on, the trigger electrode is set on a potential, which causes an electric breakdown to one of the main electrodes followed by an inter-electrode breakdown. Since the spark gap switch rise time is very short, they are mostly applied for...
short pulses (ns-range) with high repetition rate $[26]$. Spark gap switches require electric arcing. Hence, their lifetime is limited due to erosion of the electrodes. This is especially the case with higher pulsed energies, limiting the number of pulses to the range of $10^4 - 10^6 \ [25, 27, 29]$. Another option present solid state based switches. Since commercially available silicon dies do not show a voltage rating above 6 kV, they must be arranged in series for higher output voltages $[30]$. To additionally provide high pulse energy, arrays of switches are applied $[31]$. Further, hybrid solutions exist, which combine a high voltage switch with a pulse transformer $[30, 32]$. In a series connection of solid state devices, however, it must be ensured that all stages switch at the same time in order to avoid an excessive overvoltage occurring at one of the stages. Therefore, snubber and balancing circuitry as well as special gate drive techniques are required, which complicates the modulator structure $[33, 34]$. In such a series connection, switches must be applied, which turn into a short circuit in case of a failure. Then, the operation of the entire series connection will still be feasible in case of a failed stage, if a voltage safety margin is foreseen.

### 1.2.3 Marx generator based topologies

For a very broad range of pulse power systems, modulators based on the Marx topology are applied. The Marx topology, which consists of several identical cells, is sketched for a three cell modulator in Fig. 1.5. Each cell is composed of a capacitor, two switches and a diode. For charging, the auxiliary switches $S_{21} - S_{23}$ are closed and the capacitors are charged to $V_{charge}$ via the $D_{11} - D_{13}$ with the cell capacitors $C_{11} - C_{13}$ in parallel connection. In order to generate the pulse voltage, the auxiliary switches are opened and $S_{11} - S_{13}$ are closed. In this case, all cell capacitors are connected in series to provide the higher pulse voltage $V_{out}$. The advantage of this concept is that the isolation voltage of the switches in each cell must only withstand the charging voltage level $V_{charge}$ as long as the cells are isolated to ground potential. Other than in case of a direct series connection of switches, as described in the last paragraph, the Marx cell switches must not turn on synchronously, which reduces the gate design effort. For low duty cycle or short pulse lengths
**Figure 1.5:** Marx principle sketched for a three cell example with solid state switches. The capacitors $C_{11} - C_{13}$ are charged in parallel by closing $S_{11} - S_{13}$. Subsequently, they are discharged via the load $R_1$ in a series connection by opening $S_{11} - S_{13}$ and closing $S_{21} - S_{23}$.

the auxiliary switch can be replaced by a resistor or an inductor [35]. Originally, Marx cells were build with spark gap switches, which are increasingly replaced by solid state switches as they offer higher reliability. Additionally, with the application of solid state devices the cell capacitors must not be entirely discharged as it would be the case when applying spark gap switches. This feature enables a better controllability of the output pulse. Since the Marx cells are connected in series during the pulse, they can be stacked on top of each other, which drastically reduces the isolation voltage of adjacent cells. The isolation requirement towards the environment, however, is increasing for each cell number as well as the parasitic capacitance towards ground poten-
tial. There exist Marx concepts with an air insulation and modulators where all cells are entirely placed in oil [36–39].

In order to compensate the voltage droop during the pulse, the cells can be successively activated. The activation of a regular cell during the pulse interval would lead to a high ripple in the flattop voltage. Thus, special correction cells are designed, which either feature a lower charging voltage or modulate their output voltage by switching operation [40] [41].

1.2.4 Modulators based on pulse transformers

Pulse transformers have been investigated since the 1940ties [42] [43]. Due to the inherent leakage inductance $L_\sigma$ of the transformer, pulse rise times start in the range of 500 ns. In order to provide a high conversion efficiency, at least a pulse length of several $\mu$s is required [44]–[47]. Further applications can be found for pulses in the 100 $\mu$s range up to several ms [48]–[50].

Since for klystron loads a unipolar voltage pulse is required, in many cases pulse transformer are equipped with a reset circuit. This circuit allows to double the magnetic flux swing, thereby reducing the core size [51] [52]. The matrix transformer presents a special arrangement of a pulse transformer, where the secondary winding encloses several cores. This arrangement features an improved rise time in comparison to series or parallel connected transformers [46]. In Fig. 1.6 a matrix transformer with active bias circuit and variable number of magnetic cores enclosed by the secondary winding is depicted.

1.2.5 Resonant topologies

The modulator group of resonant topologies makes use of the resonance magnification occurring in an oscillating circuit. There exist the series-resonant, the parallel-resonant and the combination of both, the series-parallel resonant converter (SPRC). The SPRC is applicable for a broad load and input voltage range [53]. For pulsed power applications, a medium frequency transformer is usually incorporated to adapt to the desired voltage level and a rectifier stage is applied to obtain a unipolar pulse [54]–[56]. A schematic drawing of the SPRC is depicted in Fig. 1.7. In many cases the transformer parasitics are incorporated in the design of the resonant tank [57]. Since the transformer is subjected to an AC voltage, the duration of the pulse is not coupled to the
Figure 1.6: Schematic drawing of a matrix transformer, where the secondary winding encloses several cores. On each core leg, a pulse switch with active bias circuit is mounted. The active bias circuit allows to double the flux swing in case of an unipolar voltage excitation.

transformer’s cross sectional area and size. Additionally, the voltage droop during the pulse interval can be compensated by adjusting the duty cycle or the exiting switching frequency. Therefore the SPRC can provide a broad range of pulse lengths starting in the ms-range. Typically, the rectified output voltage features an AC-voltage ripple. Thus, a high voltage output capacitance is required, to keep the pulse
voltage ripple in the specified voltage band (see Fig. 1.7). Due to the output capacitance, more energy is required to reach a certain pulse voltage level. In order to keep the output capacitance small and the rise time short, higher switching frequencies of the SPRC module can be applied. However, higher switching frequencies result in higher converter and transformer losses. Therefore, typical pulse rise times of resonant converters are in the range of 100 µs.

1.3 Pulse modulator topology selection

In this paragraph, the previously introduced five pulse modulator topologies are evaluated with respect to CLIC specifications (tab. 1.1) and the most suitable topology is selected.

For the required pulse length of 140 µs, PFL type modulators are not suitable as feasible pulse lengths are in the range of ns. Also resonant topologies can be excluded from further considerations, due to their long rise time of the pulse.

Since the flat top ripple must be small ($FTS < 0.85\%$), modulators based on solid state switches are favored in comparison to PFN type modulators.

For CLIC, a mean time between failure of $MTBF > 100000\, h$ is desired which corresponds to a number of pulses in the range of $10^{10}$. Therefore, the spark gap technology in general, implemented in any of...
the possible modulator topologies, is not a feasible option. Instead, the selected topology must rely on solid state based pulse switches. In order to avoid a high isolation requirement of the entire modulator, the single high voltage switch topology is ruled out. From this short evaluation, two modulator concepts remain: the Marx converter and the pulse transformer based modulator, both employing solid state switches. In the next paragraph, the final modulator topology selected for the CLIC specifications is derived.

1.3.1 Comparison of Marx cell and pulse transformer based modulator

![Simplification of the pulse transformer transfer function. During the pulse rise time the magnetizing inductance $L_m$ and the iron losses $R_{Fe}$ are neglected. The klystron is approximated by a resistive load $R_{Load}$.](image)

The Marx topology allows a series connection of devices without the usual effort of series connected semiconductor devices. Therefore, it is to be preferred in comparison to a single HV-switch topology. Due to the cell based structure, it is simpler to adapt a design to different pulse lengths, which offers more flexibility as a transformer based solution. However, in order to reach a comparable modulator size, the Marx cells must be immersed in oil, which complicates the maintenance of the semiconductors. Additionally, in comparison to a pulse transformer with solid state switches, the Marx generator has a more complex structure.

Since Marx generators can be directly connected to the load, their leakage inductance $L_\sigma$ is typically lower than the one of a pulse transformer design, presuming a low inductive design of each Marx cell and its interconnection. A low leakage inductance reduces the pulse rise time and thereby increases the pulse efficiency. However, the lower leakage inductance is only advantageous in terms of pulse efficiency, if a matching of $L_\sigma$ with its distributed capacitance $C_d$ is achieved. Therefore,
in the following, the optimal relation between \( C_d \) and \( L_\sigma \) is derived for CLIC specifications, considering a simplified transfer characteristic of the modulator.

To compare both modulator systems, the pulse shape is derived from a simplified circuit diagram depicted in **Fig. 1.8**, which is modeled as a second order delay element with resistive load.

In this case, the damping of a rectangular pulse voltage shape can be described by [46]

\[
d = \frac{1}{2 \cdot R_l} \sqrt{\frac{L_\sigma}{C_d}}. \tag{1.1}
\]

The time constant \( T \) is obtained by

\[
T = \sqrt{L_\sigma \cdot C_d}. \tag{1.2}
\]

To limit the overshoot voltage of the pulse, a damping coefficient \( d \approx 1 \) must be realized. Considering an optimally damped system with \( d = 1 \), the relation between \( C_d \) and \( L_\sigma \) yields

\[
L_\sigma = 4 R_l^2 \cdot C_d. \tag{1.3}
\]

For \( d = 1 \), the pulse voltage rises with aperiodic limit according to

\[
V(t) = V_p - V_p \left( 1 + \frac{t}{T} \right) \cdot e^{-t/T}. \tag{1.4}
\]

The flat-top period begins as soon as the pulse has reached its output voltage \( V_p \) minus half the flattop band voltage \( (V = (1 - 0.5 \cdot FTS) \cdot V_p) \). Since the maximum time to flattop \( t_{\text{settle}} \) is defined, the following relation is found by inserting (1.2) and (1.3) in (1.4):

\[
\frac{FTS}{2} = \left( 1 + \frac{t_{\text{settle}}}{\sqrt{C_d} \cdot 2 \cdot R_l} \right) \cdot \exp \left( -\frac{t_{\text{settle}}}{\sqrt{C_d} \cdot 2 \cdot R_l} \right). \tag{1.5}
\]

Solving (1.5) with CLIC specifications leads to maximal parasitic values of \( C_{d,\text{max}} = 470 \) pF and \( L_{\sigma,\text{max}} = 2347 \) \( \mu \)H.

As the leakage inductance is in the mH range, it becomes obvious that an additional external inductance would be required for the Marx generator to obtain a pulse with sufficient damping. For the pulse transformer, a leakage inductance in the mH range is achievable by simply increasing the number of turns.
Although in general a Marx generator features a smaller leakage inductance than a pulse transformer based modulator, in a modulator system with CLIC specification this advantage is not applicable as a leakage inductance in the mH range is required for an efficient damping of the pulse. Therefore, the transformer based solution is selected, thus, avoiding the disadvantage of immersing the semiconductor devices into oil. A further analysis on the selected transformer configuration and winding arrangement is conducted in section 4.1.

1.4 Thesis outline

As described in the previous section, a transformer based pulse modulator topology was selected for CLIC specifications. The proposed pulse modulator system is sketched in Fig. 1.9. The system can be subdivided in three major parts with an additional overall communication system. Each of the parts is described in a chapter in this work.

The first part is the medium voltage charging system, which transfers energy from the 400 V AC grid to the main capacitor bank of the pulse units. It consists of a distribution transformer, which decouples the modulator from the grid, followed by an AC/DC source. The AC/DC source is realized as a full bridge active rectifier stage, which produces a DC link voltage of 750 V. In order to transform the DC link voltage to the required level of the main capacitor bank (2.4-3 kV), six interleaved high dynamic DC/DC boost converters are employed. The capacitor charging system is capable of transferring a maximum power of 240 kW and features a precise output voltage charging. The medium voltage charging system is presented in section 2.

The droop compensation system, described in section 3, represents the second part of the modulator system. It compensates the droop of the main capacitor bank during the pulse interval and is composed of four pulse units, which are magnetically coupled via the pulse transformer. A pulse unit in turn consists of a switching unit and six interleaved active bouncer modules in series to the main capacitor bank $C_{main}$. The switching units provide the required primary voltage pulse to the pulse transformer. The switching unit is composed of a main pulse switch with an active bias circuit. The six active bouncer
Figure 1.9: Schematic overview of the proposed 29 MW pulse modulator system for CLIC consisting of three major parts: The medium voltage charging system, the droop compensation system and the pulse transformer. The overall modulator communication system ensures a proper operation of the complete modulator system.
modules compensate the voltage droop in $C_{\text{main}}$ during the pulse by adapting their output voltage level accordingly.

The pulse transformer constitutes the third part of the system. The pulse transformer, outlined in section 4, transforms the primary voltage pulse to the required output voltage level. Since the pulse transformer is the most dynamic system component, a multi objective design procedure was developed to optimize its transfer characteristics.

For a proper functioning of the pulse modulator system, the capacitor charging system, the pulse unit and the pulse transformer cannot be operated independently. Instead, they have to be linked via a modulator communication system and combined to the final pulse power modulator system, which is described in section 5.

1.5 Objectives and contributions

In this thesis, the concept of a 29MW pulse modulator system for the application in a linear collider is investigated. The modulator system must provide 29 MW of pulsed power for a broad range of klystron loads. The modulator system can be grouped into three major parts, which are the medium voltage charging system, the droop compensation system and the pulse transformer. Especially demanding for the pulse modulator system are the high pulse power, the short pulse rise time in relation to the flat-top interval, the requirement for a highly repeatable output voltage during the pulse flat-top and a high conversion efficiency. Therefore, the major objectives of this thesis are 1) the development of a suitable system concept for the pulse power modulator complying with all specifications of tab. 1.1, 2) the design of a high precision, medium voltage capacitor charging system, 3) the optimization of the pulse transformer regarding a short time to flat-top interval, 4) the design of a high dynamic active droop compensation system enabling a flat pulse top and 5) ensuring a high pulse to pulse repeatability of the modulator’s output voltage. In the following, the corresponding contributions of this thesis are described.

Development of a 29 MW pulsed modulator system concept: A pulse modulator system, which is able to meet the demanding specifications (i.e., short rise time, high pulse to pulse repeatability, high efficiency),
requires a sophisticated system concept. Thus, system parameters such as voltage levels, current ripple, communication and interconnection between subsystems are investigated and a suitable overall system design is developed. The derived modulator system is applicable for a wide range of klystron loads.

*High power, medium voltage capacitor charging unit with high charging precision:* In order to obtain a repeatable pulse voltage as desired for the CLIC modulator, it is essential to charge the main capacitor bank of the modulator to a precise voltage prior to the pulse interval. Therefore, the concept of a high power, medium voltage capacitor charging unit with high precision is investigated and a full scale prototype system is designed in this thesis. The operation principle and predicted performance of this charging system is validated with a 240 kW prototype system consisting of six capacitor charging units and a central control unit. An efficiency of 96.3\% of a single charging unit at peak power could be achieved.

*Low ripple active droop compensation system with high dynamics:* Due to the long flat-top length of the pulse (140 \( \mu \)s), an active droop compensation system is required, also referred to as bouncer system. Active bouncer concepts for pulse modulators were applied prior to this work e.g., in [61]. However, for CLIC much higher pulse dynamics, a lower current ripple and higher pulse power are required. Therefore, a new topology is proposed which meets the required system dynamics. The low current ripple is realized by grouping 24 bouncer modules into four pulse units, magnetically coupled via the pulse transformer, and applying a 6-fold interleaving with each pulse unit. Additionally, in order to reduce the complexity of the modulator system, a combined scheme for charging the capacitor bank of the pulse modulator and the bouncer system is developed and verified with prototype measurements.

*Multi objective pulse transformer optimization procedure:* A transformer design, which ensures a high conversion efficiency with a short time to the flat-top interval, and which is applicable for a broad load range at the same time, presents a major challenge. To meet these two demands, a multi objective optimization procedure for pulse transformers is developed in this work. The introduced procedure is capable of modeling the transformer parasitics for a broad range of geometries by
applying conductor arrays and the charge mirroring method (CSM). With the derived parasitics, the pulse shape is optimized considering the non-linear behavior of the klystron load and an external set of pulse constraints. Also, all major effects contributing to the electric and magnetic losses are considered as well as a new isolation model for the transformer is included. With application of the procedure, the parameter sensitivity on e.g., core material and transformer oil is investigated and the load range behavior of a selected design is derived. Also, the efficiency of an existing pulse transformer prototype designed for SwissFEL could be improved by 16.6%. Further, the full scale transformer prototype, realized in this thesis, confirms the optimization results of the procedure. Single pulses under nominal conditions are demonstrated and a time to flat-top interval of 4 µs with an ohmic load is achieved. Generally, there is the demand to replace mineral oil in pulse transformers by environmentally friendly oils. Therefore, the influence of such an oil replacement on the transformer design is investigated in this thesis. To consider the oil replacement in the isolation model of the optimization procedure, a method which scales high voltage breakdown data on standard impulse forms to the desired application is proposed.

*Pulse to pulse repeatability:* The pulse to pulse repeatability during the pulse flat-top is crucial for the future CLIC modulator. That is why all active system components have to be analyzed regarding their influence on the repeatability of the modulator system. In order to examine the different effects influencing the charging voltage repeatability of the medium voltage charging system, a repeatability analysis is conducted considering arbitrary capacitive loads and charging voltage steps. With the realized system, the standard deviation of the main capacitor bank’s charging voltage is calculated to $\sigma_{V_{\text{out}}} = 22 \text{ mV} = 7.3 \text{ ppm}$ in relation to a charging voltage level of 3 kV. Additionally, the effects of switching jitters and the influence of duty cycle control and current mode control (CMC) in open loop are derived for a single pulse unit consisting of six interleaved bouncer modules, a pulse switch and a capacitor bank. It is shown, that keeping equal system repeatability the application of CMC allows to relax the demands on the charging voltage precision of the bouncer modules by a factor of 20. With the conducted analyses a repeatability below 100 ppm is derived for the modulator’s output voltage, which meets the highly demanding specification.
1.6 List of publications

During the course of the project, the findings were published in international conferences and journals.

In the following, an overview of publications that are included as chapters in this thesis is given. Thereafter, further publications are listed in chronological order.

1.6.1 Publications included in this thesis

Table 1.2: List of publications included as a section in this thesis.

<table>
<thead>
<tr>
<th>Section</th>
<th>Publication</th>
</tr>
</thead>
<tbody>
<tr>
<td>section 3</td>
<td></td>
</tr>
<tr>
<td>section 4</td>
<td></td>
</tr>
</tbody>
</table>
1.6.2 Further publications

- Blume, S.; Gerber, D.; Biela, J., "High precision, low ripple 3kV capacitor charger", in Proc. of the IEEE Power Modulator and High Voltage Conference (IPMHVC), 5-9 July 2016


Medium voltage charging system

In order to charge the main capacitor bank of the droop compensation system (see section 1.9), a high power, medium voltage charging system with high charging accuracy is required. The charging system is supplied from the 400V AC-grid. Besides the required charging accuracy also the high fluctuation in power due to the pulsed load presents a challenge for the system, since the grid distortion is to be minimized.

Figure 2.1: Schematic overview of the medium voltage charging system which consists of a distribution transformer, two active rectifier stages in parallel connection and a capacitor charging system. The capacitor charging system includes six charging units, which are operated by a central capacitor charging control unit.
In order to cope with these requirements, a two stage approach was
selected which is depicted in Fig. 2.1. The first input stage consists
of a distribution transformer with a subsequent AC/DC source, com-
posed of two active rectifier stages in parallel connection. Such active
rectifiers are commonly applied for driving motors and due to the high
produced quantities the price per kW is moderate. The AC/DC source
supplies a nominal DC voltage level of 750 V. In the second stage of the
medium voltage charging system, the DC voltage is stepped up to the
required primary pulse voltage level (2.5-3 kV). For this task, a capac-
itor charging system was developed, which consists of six interleaved
capacitor charging units. The six capacitor charging units are operated
by a central capacitor charging control unit.
In the following, the AC/DC source and the capacitor charging system
are described in detail.

2.1 AC/DC source

The AC/DC source is a standard industry component. That’s why the
structure is only briefly described followed by an explanation of the
specific modification conducted in the course of this project.

<table>
<thead>
<tr>
<th>Description</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>250 kVA</td>
</tr>
<tr>
<td>Primary input</td>
<td>3 x 400 V</td>
</tr>
<tr>
<td>Secondary output</td>
<td>3 x 400 V</td>
</tr>
<tr>
<td>Iron losses</td>
<td>2330 W</td>
</tr>
<tr>
<td>Copper losses</td>
<td>700 W</td>
</tr>
<tr>
<td>Conversion efficiency</td>
<td>98.8 %</td>
</tr>
<tr>
<td>Switch group</td>
<td>Dyn5</td>
</tr>
<tr>
<td>Dimensions</td>
<td>907 x 845 x 567 mm</td>
</tr>
<tr>
<td>Weight</td>
<td>890 kg</td>
</tr>
<tr>
<td>Degree of protection</td>
<td>IP20</td>
</tr>
</tbody>
</table>
2.1.1 AC/DC source hardware

The AC/DC source consists of a distribution transformer and two Acpos multi 8BVP1650 active rectifiers in parallel connection, depicted in Fig. 2.2. Each active rectifier is capable of providing 120 kW. The active rectifiers can be operated in passive configuration, which results in a DC voltage level of 560 V. However, the passive operation mode is not foreseen for a high power transmission and therefore limited to a 15 kW operation. In active operation, the voltage level can be selected in the range 620-800 V, with nominal rated power of 240 kW at a DC output level of $V_{DC} = 750$ V.

The distribution transformer, which provides the isolation to the AC grid, is displayed in Fig. 2.3 with selected parameters listed in tab. 2.1.
Figure 2.3: 250 kVA distribution transformer in *Dyn5* configuration applied for isolating the pulse modulator from the AC grid.

**Modifications of the AC/DC source**

The common application of the AC/DC source is the provision of a DC link voltage for motor drives. Therefore, the standard AC/DC source was modified to enable an application in a pulsed power system.

In continuous pulse operation, the recharging process of the main capacitor bank needs to be interrupted during the pulse interval. This interruption in charging power is required in order to obtain a repeatable voltage during the pulse interval. A definition of the term *repeatability* is given in section 2.4. Therefore, the medium voltage charging system at the output of the AC/DC source is deactivated during the pulse interval. For the AC/DC source, this operation results in a phase with continuous power consumption at the output for 19.8 ms, which is interrupted for a period of \( t_{int} = 200 \mu s \). This pattern is repeated with a frequency of 50 Hz. Since the control time constant of the AC/DC source is 7 ms, it is unable to react on the power interruption. Therefore, the AC/DC source is equipped with a DC-link capacitance value of 21.5 mF and hence, the DC-link voltage is stabilized during the interruption of power consumption. At nominal power, the AC/DC source provides a DC current of \( I_{DC,max} = 320 \) A. During \( t_{int} \), the DC link voltage is only increased by 3 V, which corresponds to a 0.4 % volt-
Figure 2.4: Control scheme of the two active rectifier stages. The master converter features a $PI$ control structure and transmits its setpoint to the slave converter.

Angle fluctuation. Thus, the AC/DC source with the additional DC-link capacitors can continue to operate with a constant power level.

In a standard application of the AC/DC source, the two rectifying units in parallel connection are separately controlled. Since for standard applications, the DC link voltage stability is not critical, both units feature a simple proportional regulator, which leads to a static deviation of the DC link voltage. When the AC/DC source was tested with 50% of its rated power, the DC link voltage deviation already exceeded $\Delta V_{DC\text{link}} = 20\, \text{V}$.

That’s why the control scheme of the source was modified to a $PI$ structure. In order to ensure a current balancing of the two parallel rectifying units, a master slave configuration was implemented. The data exchange is provided via the internal bus of the AC/DC source with a cycle time of $T_{\text{cycle}} = 400\, \mu\text{s}$. The resulting control scheme is depicted in Fig. 2.4. The master unit features a $PI$ control structure and transmits its current reference to the slave unit. The internal controller of the slave unit is deactivated by choosing a very small $k_p$. The AC/DC source was tested in the modified configuration with an
electronic load up to 100 kW. The test showed a reduction in voltage fluctuations to $\Delta V_{DClink} = \pm 1$ V.

The applied AC/DC source is normally operated with the *Ethernet POWERLINK* data transmission protocol. Since the modulator’s overall communication system is based on the protocol *EtherCAT*, the source was reconfigured as EtherCAT slave. The corresponding overall communication system is further described in section 5.1.

2.2 Capacitor charging system

The high precision capacitor charging system consists of six capacitor charging units operating in interleaved boundary conduction mode (BCM). Its specifications are listed in Table 2.2. To realize the six-fold interleaving of the capacitor charging units, a central control unit, which communicates via optical fiber with each single unit, is designed. The operation mode and charging principle is based on [47].

In the following, the operation principle of a single charging unit is briefly described. Since a comparison of different charging principles can be found in [47], a comparison is not provided in this paragraph. Thereafter, the hardware design is outlined with emphasis on high voltage and high frequency considerations. Furthermore, the applied communication protocol is presented. Additionally, a definition of the pulse to pulse repeatability is given as it is a central specification for CLIC. Then, an extension to the charging repeatability analysis in [62] is proposed. Compared to their analysis, the proposed approach in this thesis

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>750 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>2.5-3 kV</td>
</tr>
<tr>
<td>Peak current</td>
<td>140 A</td>
</tr>
<tr>
<td>Module output power</td>
<td>40 kW</td>
</tr>
<tr>
<td>Number of units</td>
<td>6</td>
</tr>
<tr>
<td>Total charging power</td>
<td>240 kW</td>
</tr>
<tr>
<td>Switching frequency :</td>
<td></td>
</tr>
<tr>
<td>Nominal power</td>
<td>70 kHz</td>
</tr>
<tr>
<td>Zero active power</td>
<td>$\approx 240$ kHz</td>
</tr>
</tbody>
</table>
Figure 2.5: a) Schematic drawing of a single capacitor charging unit with additional snubber capacitances for operation in boundary conduction mode (BCM). b) The five different time intervals of BCM. Top: the time dependent inductor current $i_L$. Bottom: the snubber capacitance voltage of the series connected MOSFETs $V_{Cs,tot}$ and of the series connected diodes $V_{Cd,tot}$.

considers a variable number of charging cycles. Finally, measurements of the single charging unit and of the interleaved capacitor charging process are presented.

2.2.1 Operation Principle

A schematic drawing of a capacitor charging unit is depicted in Fig. 2.5 a). It is a standard boost topology with series connected semiconductors and additional snubber capacitances. The capacitor charging units operate in boundary conduction mode, which allows zero voltage switching (ZVS)\(^{[63]}\). The snubber capacitances are added to ensure a safe operation of the series connected MOSFETs and to increase the converter ZVS operating range\(^{[64]}\).

The operation of the charging unit can be divided in five intervals, which are schematically depicted in Fig. 2.5 b). In the first interval $T_1$, the MOSFET switches are turned on and a current is build up in the inductor with a slope $di/dt = \frac{V_{BC,in}}{L}$. At this point in time, the snub-
ber capacitances of the switches $C_{S,1−n}$ are discharged with $V_{Cs,\text{tot}} = 0$ and the snubber capacitances of the diodes $C_{D,1−n}$ are charged with the output voltage $V_{Cd,\text{tot}} = V_{BC,\text{out}}$. When the inductor current reaches its desired peak, the switches $S_{1−n}$ are turned off and in time interval $T_2$, a resonant transition occurs between the inductor and both snubber capacitances, which results in $V_{Cs,\text{tot}} = V_{BC,\text{out}}$ and $V_{Cd,\text{tot}} = 0$. Once the resonant transition is completed, the interval $T_3$ starts and the inductor current decreases with the slope $\frac{di}{dt} = \frac{V_{BC,\text{out}} - V_{BC,\text{in}}}{L}$. Once the inductor current $I_L$ becomes negative another resonant transition occurs ($T_4$). During interval $T_4$, $C_{D,1−n}$ are charged and $C_{S,1−n}$ are discharged. Once $C_{S,1−n}$ are entirely discharged, the negative current continues to flow via the parasitic diodes of the MOSFETs. In the fifth interval $T_5$, the switches $S_{1−n}$ are turned on and begin to conduct. As long as the current still shows a negative sign at the switches’ turn on, the ZVS condition is met, which reduces the turn on losses significantly.

### 2.2.2 Capacitor charging unit hardware design

Due to BCM operation of the capacitor charging unit, the switching frequency varies in dependency on the operation point. The operation point is dependent on the input and output voltage as well as on the transferred power. If no active power transfer is required, the converter must continue to operate and must provide reactive power in order to maintain ZVS conditions. The switching frequency in this operation point is high with 240 kHz, thus, leading to increased gate supply losses. At the maximal transferred power, the current peak is up to 140 A, which induces high conduction losses, while the operation frequency remains high with 70 kHz. Another challenge for the design presents the high voltage isolation requirement combined with the high frequency excitation.

Therefore, the selection of the major components of a single capacitor charging unit is described in the next paragraph, followed by the description of the high voltage isolation and the mechanical arrangement of the prototype.

#### Semiconductor selection

Due to the high converter switching frequency, MOSFETs were selected, which offer a significant loss reduction when operated in ZVS. In order
Table 2.3: Losses in the semiconductor devices at nominal power of 40 kW with a switching frequency of 70 kHz. The losses are composed of switching, reverse recovery and conduction losses.

<table>
<thead>
<tr>
<th>Device</th>
<th>Switching/reverse recovery losses single device</th>
<th>Conduction losses single device</th>
<th>Total losses of all devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>CoolMOS C7</td>
<td>23.3 W</td>
<td>35.2 W</td>
<td>936 W</td>
</tr>
<tr>
<td>APT75DQ120B</td>
<td>9.5 W</td>
<td>72 W</td>
<td>326 W</td>
</tr>
</tbody>
</table>

...to provide the required voltage and current, eight 650 V-MOSFET devices were arranged in series and two in parallel. Since a high current rating of the device is required, the CoolMOS C7 from Infineon was selected. The switching and conduction losses were calculated according to \[65\]. The 3 kV blocking capability of the diodes is achieved using four 1.2 kV-devices in series. Due to the series connection, an avalanche rated device with a low leakage current is selected, which offers a fast recovery time and a high forward current; the APT75DQ120B from Microssemi \[66\]. Semiconductor losses for nominal power operation are listed in tab. 2.3.

Selection of snubber capacitances

The series connection of switches requires additional measures in the circuit layout, in order to prevent a failure due to voltage imbalances in the stages. To cope with static voltage imbalances, discharge resistors are utilized. During switching operation, transient voltage imbalances might also occur due to jitters in the optical gate signal path. To limit this effect, snubber capacitances are applied, which stabilize the drain source voltage for the required time period.

The snubber value \( C_{\text{snub}} \) was selected according to

\[
C_{\text{snub}} = \int_0^{t_{\text{jit}}} \frac{I(t)}{\Delta V} dt \leq \frac{I_{\text{peak}} \cdot t_{\text{jit}}}{\Delta V},
\]

were \( t_{\text{jit}} \) is the worst case jitter, \( \Delta V \) the maximal allowed voltage difference of the delayed stage and \( I_{\text{peak}} \) the highest current occurring in BCM operation.
Assuming equal voltage balancing results in a reverse voltage of 375 V per stage. To limit the highest voltage transient of a single stage to $V_{\text{max}} = 500$ V a voltage difference of $\Delta V = 125$ V is selected. With assumed worst case values of $t_{\text{j,pt}} = 20$ ns and $I_{\text{pk,a}} = 180$ A a required value of $C_{\text{snub}} = 28.8$ nF per stage results, which would lead to a total snubber capacitance value of $C_{\text{snub,tot}} = 3.6$ nF.

Since the snubber capacitance are in parallel to the non-linear output capacitances of the MOSFETs, the possible area of ZVS switching can be increased [62]. The dependency of the ZVS boundary on the total snubber value is depicted in Fig. 2.6. The selected total snubber value is $C_{\text{snub,tot}} = 7$ nF, which is distributed over $C_{\text{snub,S}} = 47$ nF per MOSFET stage and $C_{\text{snub,D}} = 4.4$ nF per diode stage. With $C_{\text{snub,tot}}$ and a minimum voltage of the AC/DC source of 620 V (see section 2.1), the ZVS condition can still be met with half the output voltage. For preconditioning the klystron load, this operation point is required, since an immediate operation at nominal voltage leads to arcing of the klystron. The snubber capacitor losses were calculated according to
Table 2.4: Parameter of snubber capacitors. Ten capacitors in parallel were used for each MOSFET stage, whereas for each diode stage two capacitors in series and four in parallel were arranged.

<table>
<thead>
<tr>
<th>Snubber capacitor applied for the switches</th>
<th>Voltage rating</th>
<th>1000 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance value</td>
<td>4.7 nF</td>
<td></td>
</tr>
<tr>
<td>(\tan(\delta))</td>
<td>1e-3</td>
<td></td>
</tr>
<tr>
<td>Power rating case</td>
<td>0.45 W</td>
<td></td>
</tr>
<tr>
<td>Losses (2.2)</td>
<td>0.16 W</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Snubber capacitor applied for the diodes</th>
<th>Voltage rating</th>
<th>1000 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance value</td>
<td>2.2 nF</td>
<td></td>
</tr>
<tr>
<td>(\tan(\delta))</td>
<td>1e-3</td>
<td></td>
</tr>
<tr>
<td>Power rating case</td>
<td>0.33 W</td>
<td></td>
</tr>
<tr>
<td>Losses (2.2)</td>
<td>0.21 W</td>
<td></td>
</tr>
</tbody>
</table>

\[ P_{\text{snub}} = \int_0^{\infty} \omega C_{\text{snub}} \cdot V(\omega) \cdot \tan(\delta) \, d\omega, \quad (2.2) \]

where \(\tan(\delta)\) is the capacitor loss tangent and \(V(\omega)\) the frequency dependent voltage of the snubber capacitance. The component ratings and the calculated losses are listed in tab. 2.4.

Inductor design

Due to the high switching frequencies, ferrite N87 was selected as inductor core material. The inductor was optimized considering skin and proximity losses [67]. The core losses were calculated according to [68]. The air gap model was derived from [69] and the applied thermal model of the boost inductance was modeled according to [70]. Forced cooling, provided by three 230 V-AC coolers, is considered with the heat transfer coefficient \(\alpha\) of the surface [71]. A conservative value of \(\alpha = 20 \text{ W/(m}^2\text{K)}\) was assumed.

The selected inductor winding are two litz wire conductors in parallel (each 4000 strands, \(d_s = 0.05 \text{ mm}\)). In order to reach the desired inductance value, there are two inductors connected in series, each consisting of four U-cores and four I-cores forming an E-core. The resulting parameters and temperatures of the inductance are listed in tab. 2.5.
Table 2.5: Inductance parameters of capacitor charging unit.

<table>
<thead>
<tr>
<th>Inductance value per core</th>
<th>30 µH</th>
</tr>
</thead>
<tbody>
<tr>
<td>No cores in series</td>
<td>2</td>
</tr>
<tr>
<td>Number of turns per core</td>
<td>7</td>
</tr>
<tr>
<td>Air gap</td>
<td>6 mm</td>
</tr>
<tr>
<td>Core material</td>
<td>N87 ferrite</td>
</tr>
<tr>
<td>Single core shape</td>
<td>U 93/76/30 / I 93/28/30</td>
</tr>
<tr>
<td>$P_{core,tot}$</td>
<td>26 W</td>
</tr>
<tr>
<td>$P_{wind,tot}$</td>
<td>40 W</td>
</tr>
<tr>
<td>$T_{ambient}$</td>
<td>30°C</td>
</tr>
<tr>
<td>$T_{core}$</td>
<td>50°C</td>
</tr>
<tr>
<td>$T_{winding}$</td>
<td>97°C</td>
</tr>
</tbody>
</table>

Components for BCM operation

In order to operate the capacitor charging unit in BCM, the converter peak current must be controlled. To allow a fast turn off, the measured current signal is compared to a voltage reference created by an 12-bit parallel digital analogue converter (DAC), controlled via the FPGA. Due to the high peak current values and high switching frequencies, the choice of suitable current sensors is limited. Therefore, a sensor based on the magneto resistive effect $CDS4125ACC$ was selected, which offers a high bandwidth even at a high RMS current [72]. The sensor also features an over-current detection, which provides a safe turn off even in case of a DAC or comparator failure.

As previously mentioned, the converter must continuously provide reactive power, to maintain its ZVS capability. Therefore, a minimum current value is required, which is obtained by [64]:

$$I_{L,min} \geq \sqrt{\frac{C_{eq} \cdot V_{out} (V_{out} - 2 \cdot V_{in})}{L}},$$  \hspace{1cm} (2.3)

where $V_{in}$ and $V_{out}$ are the input and output voltage, $L$ is the boost inductance and $C_{eq}$ is the equivalent output capacitance of the converter. With the selected parameters, $I_{L,min} = 22.9$ A results.
In order to guarantee ZVS operation and to enable the phase shift control of several interleaved capacitor charging units as described in [47], the current zero crossing of each unit is required as a reference signal. The detection is based on a fast saturating current transformer, which is always in saturation, except during the zero crossing of the current. Since the entire BH-loop is traversed in every switching cycle, excessive losses occur in the magnetic core, especially in low power operation. Therefore, a z-shape core material VC 6025Z of VACCUM-SCHMELZE was chosen [73], which offers a small and almost squared hysteresis loop.

High voltage, high frequency isolation

The high voltage, high frequency charging unit operation requires particular considerations, which are briefly summarized in this paragraph. Due to the high operating power, the semiconductors are mounted on a water cooled heat sink. As insulating material of the heat sink aluminum oxide $\text{Al}_2\text{O}_3$ was selected, due to its high electrical strength and its excellent heat transfer characteristic (1.5 mm $\text{Al}_2\text{O}_3$-plate $\alpha = 1.66 \text{ W K/cm}^2$).

In order to avoid an electric breakdown over time, the creepage distances were respected according to [74]. To reduce the voltage stress in the design further, the heat sink was isolated towards the converter housing and set to the input voltage potential, thus the voltage difference to the 3 kV output potential is reduced.

In order to isolate the different gate supply voltages of the series connected MOSFETs, a custom made gate transformer was designed with epoxy coating as isolating material. The isolation capacity was checked performing a partial discharge measurement. The partial discharge level was limited to 1 pC for an excitation AC voltage with a 4.5 kV-RMS level.

For the sake of a compact arrangement of the series connected MOSFETs, the gate supply was realized on a separate printed circuit board (PCB) depicted in Fig. 2.7. To isolate the gate signal, the HFBR-3810MSZ from Avago Technologies was selected, which features an optical transmission line within a single housing. Due to the high voltage transients induced by the switching operation, the shielded version of the opto-coupler was applied.

The high voltage high frequency excitation also affects the PCB lay-
out. In order to avoid an inter-layer breakdown of the main PCB, copper traces with fluctuating potentials were not overlapped with traces on static potential. Further, the inter-layer isolation thickness was selected according to

$$E = \frac{0.25}{d_{req}} + 1.66, \quad d_1 \leq d \leq d_2,$$

where $E$ is the electrical field in kV/mm and $d_{req}$ the thickness of the isolation material in µm, with values between $d_1 = 30 \, \mu$m and $d_2 = 750 \, \mu$m \cite{75}. This formula is valid for a homogeneous electrical field \cite{75} with frequencies up to 10 MHz and is applicable for the desired application. In case of a homogeneous electrical field, (2.4) can be transformed to

$$d_{req} = \frac{V_{hf} - 0.25}{1.66},$$

where $V_{hf}$ is the applied high frequency voltage. For the desired application the minimum inter-layer isolation thickness results to $d_{req} = 165 \, \mu$m. To include a safety margin, the PCB inter-layer thickness was selected to $d_{app} = 460 \, \mu$m.

**Capacitor charging unit prototype**

The converter is depicted in Fig. \ref{fig:2.8}. On its backside, three 230 V AC coolers are mounted to cool the two series connected inductors. The optical fibers for the communication and the water hoses are connected
**Figure 2.8:** Capacitor charging unit. On the left hand side the inductor is situated cooled by three AC-Coolers. The semiconductors are water-cooled with feed-throughs below the optical fibers of the communication link.

on the left half of the front side, whereas the input and output voltages are fed in on the right half. The voltage feed-throughs are isolated towards the housing in order to allow a central grounding point on the low voltage side of the modulator, which is the transformer tank.

The output capacitors are distributed over the entire length of the PCB, to reduce the commutation path during switching operation. Providing a low inductive connection to the capacitive load, high voltage BNC cables are applied, which are in turn connected via SHV terminals to the PCB.

Since a short circuit might occur in the pulse modulator, the capacitor charging unit must survive a shorting of its output. Between input and output a fast 4.5 kV diode $D_{56S40}$ from Infineon is mounted (reverse recovery time of $t_{rr} = 3.3\, \mu s$). This diode starts to conduct in case of a shorted output. In order to protect the $D_{56S40}$ with an $I^2t$ of $I^2t = 7200\, \text{A}^2\text{s}$, the positive input rail is secured with a NH1 fuse, ($I_{nom} = 80\, \text{A}$, gPV) with an $I^2t$ value of $I^2t = 2750\, \text{A}^2\text{s}$. The placement of the diode in the converter is depicted in Fig. 2.9a) and the corresponding circuit diagram is displayed in Fig. 2.9b).
is limited by the inductance of the charging unit. After the inductance has saturated, the current is shared between the $D56S40$ and the four series connected $APT75DQ120B$. Since the maximal forward voltage of the $D56S40$ is $4.15 \text{ V}$, the forward voltage of each $APT75DQ120B$ results in $1.1 \text{ V}$, which limits the current to values in the safe operating area.

### 2.3 Control scheme of the capacitor charging system

A central capacitor charging control unit, which will be described in section 5.1.3, regulates the six capacitor charging units. The resulting control structure of this charging control unit is depicted in Fig. 2.10, which consists of three different parts:

- The charging controller computes a current reference value $I_{set}$ from an input and output voltage measurement. The interleaving controller transforms $I_{set}$ to the individual converter reference current, in order to obtain the desired phase shifting of the charging units. To compute the actual phase shift, the current zero crossing instance of each charging unit is provided. All required operation data is exchanged via an optical communication interface in a star connection.

In the following, the different parts are described in more detail.


2.3.1 Charging controller

The state machine of the charging controller, depicted in Fig. 2.11, consists of seven states. At the beginning of the recharging phase, the charging controller is in the idle state. Once a charging signal is received, the capacitor bank is charged with all charging units operating in interleaved mode. The charging controller continuously calculates the required current value $I_{req}$, which would be necessary to charge the capacitor bank to a predefined set point voltage $V_{out, set}$. The related equations have been derived in [17]. As long as $I_{req}$ exceeds the maximal allowed current value $I_{max}$, the current reference value $I_{set}$ is limited to $I_{set} = I_{max}$. All charging modules remain in the charging mode interleaved until the capacitor voltage $V_{out}$ exceeds a given threshold voltage $V_{out} > V_{th,1}$. Then, the non-interleaved charging mode is activated, which leaves a single charging unit active. At this point, $I_{req} > I_{max}$ still applies. The output voltage measurement is filtered with a digital FIR filter to increase the signal to noise ratio (SNR). The FIR filter features a pass band corner frequency of 1 kHz, which corresponds to a time delay of 60 $\mu$s. Since the filter time delay would lead to a voltage overshoot, a second voltage threshold $V_{th,2}$ is implemented, where the state machine transitions to the state charge retention. In this state, the converter operation pauses for a given time interval $t_{wait}$.
in order to allow the filtered voltage measurement to reach its actual value. Then, the converter performs a single charging cycle in *charge 1 cycle*. In the following, the charging controller switches between the states *charge retention* and *charge 1 cycle* until a trigger signal from the central pulse control unit is received (see section 5.1). Then, the required charging current is computed again and a final charging cycle is executed. The finalization of the charging process is signaled to the central pulse control unit, which then can enable the next pulse interval.

### 2.3.2 Communication interface

In order to avoid ground loops, all required data are transmitted via plastic optical fiber to the centralized capacitor charging control unit. The applied communication interface is based on a bidirectional serial link. The serial data are 8B10B encoded, which features

- DC balancing
Due to the small run length, sufficient transitions occur in the data stream, which allows to perform a clock data recovery. In order to securely detect single bit faults and burst errors in the data stream, a cyclic redundancy check (CRC) is included. The communication link principle is depicted in Fig. 2.12 for both transmission channels.

The transmitted frame from the central capacitor charging control unit $TX_{DataCU}$ consists of the current reference and three control bits with a total length of 2 bytes. The received data frame $RX_{DataCU}$ has a length of five bytes, containing the input and output voltage measurement, an error byte and a status byte. The zero crossing signal of each converter unit is directly sent via fiber optics to the control unit.

Two symbols, which do not occur in the decoded data stream, are applied to indicate the start and end of a data package. The resulting length of the entire package including the CRC checksum is 50 Bit for the transmitting and 70 Bit for the receiving frame. With an optical transmission path, the data can be transmitted over a distance with minimal interference and high reliability.

**Figure 2.12:** Communication link principle for a master and a slave unit with two transmission channels indicating the optical transmission path.
Figure 2.13: Schematic representation of the interleaving controller. The charging controller provides a reference current value $I_{set}$. By adding the corresponding $\Delta I_{slave}$ from the $N$ interleaving controllers, the slave reference current value $I_{set,slave}$ is obtained.

transmission rate of 50 MBd/s, the current reference value is updated every $1 \mu$s.

2.3.3 Interleaving controller

The structure of the interleaving controller is depicted in Fig. 2.13. The first charging unit acts as master. For each of the slave units, the period time $T$ and the time shift of its zero crossing in relation to the master’s zero crossing signal $\Delta T$ is derived. The phase error calculation is pipelined, starting with the converter with the lowest index. For each slave unit an interleaving controller is implemented, which corrects the current reference value $I_{set}$, provided by the charging controller, by $\Delta I_{slave}$.

The current reference value from the charging controller is synchronized with the master’s zero crossing signal. Since up to eight converters can be operated interleaved, the induced delay by the internal calculation and the data transmission can exceed the phase shifting time interval. In this case a time delay of one switching cycle occurs for the reference value. Especially for the units with a small phase shift angle, the optimal control parameters selected in [63] would lead to an unsta-
Figure 2.14: Closed loop transfer function of the interleaving model, including the time delay $G_{td} = \frac{1}{z}$ caused by the optical data transmission. The interleaving controller $G_c$ features a PI structure. $G_d$ is the disturbance and $G_p$ the plant transfer function. The delay of one switching cycle can be considered by extending the interleaving model with a delay element $G_{td} = \frac{1}{z}$. The extended model is depicted in Fig. 2.14, where $G_d$ is the disturbance and $G_p$ the plant transfer function. The interleaving controller $G_c$ features a PI structure. The resulting transfer function leads to a modified stable parameter space of the control variables $K_{i,n}$ and $K_{p,n}$. The resulting settling time of the interleaving controller, considering the delay of one switching cycle, is depicted in Fig. 2.15 for all stable combinations of $K_{i,n}$ and $K_{p,n}$. With a selected settling time of 12 switching cycles, $K_{i,n} = 0.065$ and $K_{p,n} = 0.3655$ result.

2.4 Definition of pulse to pulse repeatability

For a linear collider, it is essential that the accelerated particles always collide at the level of the detector, which is situated at the center of the two opposite acceleration channels. For CLIC, the particles are accelerated from both sides over a length of 50 km and must collide in a comparatively small observation window. If consecutive voltage pulses transmitted to the klystron load differ in their shape, the acceleration profile will be modified, which can lead to a shift of the collision point outside of the detector. Therefore, a demanding pulse to pulse repeatability $PPR \leq 100$ ppm is specified, which requires special considerations in the modulator design.
In this paragraph, a definition of the pulse to pulse repeatability $PPR$ is provided to facilitate an understanding of the related analyses conducted in this thesis. $PPR$ requires that consecutive pulses do not differ in their flat-top shape. An illustration of a flat top period of two different pulses is given in Fig. 2.16. Other than in case of voltage accuracy, for $PPR$ the voltage shape itself is not constrained as long as the difference in amplitude does not violate the flat-top stability criteria. The pulse to pulse repeatability refers to a certain number of consecutive pulses. Therefore, long term effects, such as temperature drifts, can be neglected.

In order to determine the $PPR$, the flat-top shape of $N$ consecutive pulses is compared for the entire flat top period for $k$ runs. The highest voltage deviation of two pulses out of a set of $N$ pulses is considered as the $PPR$ in the first run. In the next run, a new pulse is added and the first pulse is removed from the analysis, thus keeping the number $N$ of investigated pulses constant. Since the pulse shapes are influenced by probabilistic effects, the voltage differences will naturally fluctuate. Therefore, the voltage standard deviation $\sigma_{Vout}$ in each time step of the pulse can be derived, allowing to estimate the probability that the $PPR$ remains within a certain limit. The coherence is visualized in Fig. 2.16. An important fact to notice is that, the higher the pulse

\[\begin{array}{c|c|c|c|c|c|c|c|c|c|c|c}
K_{i,n} & 0 & 0.05 & 0.1 & 0.15 & 0.2 & 0.25 & 0.3 & 0.35 & 0.4 & 0.45 & 0.5 \\
K_{p,n} & 0 & 0.1 & 0.2 & 0.3 & 0.4 & 0.5 & 0.6 & 0.7 & 0.8 & 0.9 & 1 \\
\end{array}\]

\textbf{Figure 2.15:} Settling time of the interleaving controller in switching cycles in dependence on its control parameters $K_{i,n}$ and $K_{p,n}$. The data transmission delay of one switching cycle is included in the analysis.
gradient during flat-top is, the more difficult it becomes to limit the PPR. So one key factor of a low PPR is to limit the voltage fluctuations within a single pulse flat-top interval.

The most influencing parameter on the PPR is the charging voltage repeatability on the primary side, since it directly influences the output voltage via the transformer. Therefore, the charging voltage repeatability is analyzed in section 2.5. This analysis shows, that the signal to noise ratio of the primary voltage measurement has the highest impact on the PPR.

Other than for short pulse modulators (pulse length 1 – 5 µs), CLIC

![Figure 2.16: Visualization of the pulse to pulse repeatability definition. It describes, how two pulses differ in their voltage shape during the flat-top period. During a high gradient phase of the pulse their voltage difference ∆V_{out1} is higher than in a low gradient phase with voltage difference ∆V_{out2}. In red, the voltage band is depicted, in which ±3σ = 99.7% of the pulses are expected.](image)
MEDIUM VOLTAGE CHARGING SYSTEM

requires a droop compensation. In this work, an active bouncer system is applied, which allows a flexible droop compensation, at the cost of inducing non-repeatability into the system. Therefore, two different PPR analyses are conducted in section 3.5 and section 3.7. For the droop compensation system, a low switching jitter, a low noise active bouncer current measurement and a low induced ripple on the pulse output voltage are the key factors to achieve a low PPR.

2.5 Charging voltage repeatability of main capacitor bank

A demanding design parameter of CLIC is the pulse to pulse repeatability, which should be below 100 ppm. As will be shown in section 3.7, the repeatability of the main capacitor charging voltage exerts the highest influence on the system repeatability. Therefore, in this section, the charging voltage repeatability is analyzed.

A charging precision analysis for a boost converter operating in BCM has been conducted in [62]. It was found that the charging voltage repeatability is influenced by the noise of the input and output voltage measurement, by the current measurement noise and by switching jitters of the MOSFETs. This analysis, however, was based on the assumptions that the controller always detects correctly and that only a final charging cycle is required to reach the desired output voltage level. Therefore, their precision analysis only considered the last charging cycle.

The increase in output voltage ∆V_{out} of a single charging cycle can be described by [62]

\[ \Delta V_{out} = V_{in} - V_{out} + \sqrt{\frac{L^2}{C_{load}^2} \cdot (I_{L,s}^2 - I_{L,min}^2)} + (V_{out} - V_{in})^2 \] (2.6)

I_{L,s} is the set module current and C_{load} the capacitive load. I_{L,min} is obtained according to (2.3). With CLIC parameters ∆V_{out} = 42.4 mV results, which corresponds to 14 ppm of the desired charging voltage level. Due to measurement noise, calculation errors occur in the charging controller which might lead to a transition into the final charging step too early, i.e., several
Figure 2.17: Extended charging voltage repeatability analysis. The initial population of input and output voltage has a size of $N_{\text{init}} = 600000$. The charging controller calculates, whether or not it can reach the set point voltage in a last charging cycle. If this is the case, the voltage values will be stored; otherwise another charging cycle is simulated. Finally, a last charging cycle is simulated with all stored voltages values, which leads to the final output voltage distribution.

cycles before the desired voltage set point can be reached. This will especially be the case, if the charging step $\Delta V_{\text{out}}$ is small.
That is why the precision analysis in [62] is extended to consider an arbitrary number of charging cycles, thereby allowing to consider various
loads and transmitted charge per cycle.

The approach for the extended charging voltage repeatability analysis is depicted in Fig. 2.17. The calculation begins with an initial population of input and output voltage data points (population size $N_{init} = 600000$). The resulting input parameters for the charging controller are obtained by adding noise to the initial population and considering the measurement value quantization due to digitalization. With these quantized voltage values, the charging controller calculates according to (2.6), whether or not $I_{req} < I_{max}$. For all cases, where this condition is met, the output voltage values without noise are stored to a database. For the other points, a charging cycle is simulated, where the controller value is set as comparator reference for the current measurement. In this calculation step, the current measurement noise and switching jitters are considered. The resulting capacitor output voltage distribution is considered as the new initial population for the next charging cycle. This procedure is iterated until 99.9% of the first initial population is added to the database.

Then, the last charging cycle is simulated for all voltage values from

---

**Figure 2.18**: Charging voltage distribution for a high (92.5 dB) and a low (65 dB) SNR of the output voltage measurement.
The voltage level of the initial population has to be selected in such a way, that even with a high measurement distortion no data point can reach the final charging cycle in the first iteration. On the contrary, the voltage level must be selected close enough to the voltage set point to limit the calculation effort.

The initial voltage levels are therefore chosen such, that the reference value of the controller is higher than the maximum current value, considering that input and output voltage measurements are distorted by \( \mu + n \cdot \sigma_{in,\text{out}} \). The parameter \( \sigma_{in,\text{out}} \) is the standard deviation of the respective measurement. The higher \( n \) is chosen, the lower the probability that the controller indicates a last charging cycle, even though it will not be able to reach the set point voltage.

Two cases are investigated in the following, which are

- high SNR of the output voltage measurement (92.5 dB)
- low SNR of the output voltage measurement (65 dB).

A charging voltage distribution for the final charging cycle is depicted in Fig. 2.18 for a high (92.5 dB) and a low (65 dB) SNR of

\[ \sigma_{V_{\text{out}}} \text{(mV)} \]

\[ \text{Input Voltage SNR (V)} \]

\[ \text{Output Voltage SNR (V)} \]

\[ \sigma \]

\[ V_{\text{out}} \]

\[ \text{Database equal to the previously described charging cycles. In the following, the final output voltage distribution is analyzed.} \]
the output voltage measurement. It can be observed that with lower SNR, the standard deviation of the charging voltage increases drastically. With a low SNR, the controller signals in many cases a premature final charging cycle, which is why the final charging voltage has a lower mean in comparison to the high SNR case. In Fig. 2.19, the dependency on the input and output voltage measurement SNR is depicted. It can be observed, that the input voltage SNR does not affect the charging precision, whereas the output voltage SNR exerts an strong influence of factor seven in the investigated range of 80-100 dB.

In order to predict the charging repeatability for CLIC, the digital signal to noise ratio (SNR) of the transmitted input measurement and the external output measured were recorded. In order to improve the SNR of the output voltage measurement, as the dependency on the repeatability is strong, a digital FIR filter was implemented, increasing the SNR (see section 2.3.1). For switching jitters and current measurement, worst case values were assumed. All considered values for the analysis are summarized in tab. 2.6. With $V_{\text{in}} = 750 \text{ V}$, $V_{\text{set}} = 3000 \text{ V}$ and the filtered output voltage measurement, a $\sigma_{V_{\text{out}}} = 22 \text{ mV}$ can be achieved, which corresponds to 7.3 ppm. For the entire operation range listed in tab. 2.2, $\sigma_{V_{\text{out}}}$ is calculated. The results are depicted
Table 2.6: Measured signal to noise ratio (SNR) of converter measurements.

<table>
<thead>
<tr>
<th>Value</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured input voltage SNR</td>
<td>68 dB</td>
</tr>
<tr>
<td>Measured output voltage SNR</td>
<td>82 dB</td>
</tr>
<tr>
<td>Measured output voltage SNR with digital FIR filter</td>
<td>92.5 dB</td>
</tr>
<tr>
<td>Current measurement SNR (assumed)</td>
<td>60 dB</td>
</tr>
<tr>
<td>$\sigma_{\text{switch}}$ (assumed)</td>
<td>5 ns</td>
</tr>
</tbody>
</table>

in Fig. 2.20 which show that the standard deviation is smallest for the highest output voltage and lowest input voltage level. This result is plausible, since the transmitted charge per charging cycle decreases, the higher the difference between input and output voltage becomes.

Figure 2.21: a) 240 kW capacitor charging prototype system. b) Thermal image of converter’s top view after continuous 40 kW operation.
2.6 Verification by measurements

In this paragraph, the working principle of the capacitor charging units is verified by measurements on the realized prototype system, depicted in Fig. 2.21 a). At first, the single converter operation is presented, followed by an interleaved capacitor charging with six charging units.

Measurements on a single capacitor charging unit

Each single capacitor charging unit was tested with a resistive load at nominal voltage levels and nominal output power of 40 kW. The resulting thermally stable component temperatures are depicted in Fig. 2.21 b). In order to reduce the temperature hot spot occurring in the area of the diodes, small heat sinks were added on top of the PCB, reducing the hot spot temperature from 94 °C to 78 °C. An efficiency of approximately \( \eta_{mess} = 96.3 \% \) was measured. The derived losses of semiconductors, snubbers and inductor in section 2.2 sum up to \( P_{V_{tot}} = 1.344 \text{ W} \) in the measured operation point, which corresponds to \( \eta_{calc} = 96.64 \% \). Therefore, the conducted measurement is in good agreement with the derived converter losses.

Interleaved charging of capacitor bank

The interleaved charging of a 3 mF capacitor bank is depicted with two charging units in Fig. 2.22 a). In order to simulate the recharging process, the 6 mF capacitor bank is charged from 2.7 kV to 3 kV, which corresponds to a 36 MW pulse for \( t_p = 150 \mu s \). The recharging interval requires 39.1 ms. With maximal charging power of 240 kW the recharging process for the final 29 MW – 140 \( \mu s \) – pulse would require a time of \( t_{rech} = 17.145 \text{ ms} \) for the 6 mF capacitor bank. This recharging time offers the possibility to deactivate the charging system during the pulse interval and allows several single charging cycles with a subsequent waiting interval, in order to increase the voltage precision. This operation mode is visualized with a set charging time of 80 ms. The charging controller performs several separate charging cycles, to retain its voltage level until the trigger signal is received. Then, a final charging cycle is executed.
Figure 2.22: a) Interleaved charging process of 3 mF capacitor bank, which is charged from 2.7 kV to 3 kV. Two charging units operate with 35 kW input power each, which results in a recharging time of $t_{rech} = 40$ ms. b) Charging process of 3 mF capacitor bank with activated trigger mode.
In order to be able to record the interleaved capacitor charging with six interleaved charging units, the charging power of each unit was reduced by adapting the set point current to $I_{\text{peak}} = 50$ A. The resulting charging voltage profile for the 3 mF capacitor bank is depicted in Fig. 2.23 together with the average charging current and charging power. The charging process with a mean charging power of 84 kW requires 65 ms. The corresponding interleaved currents of the charging units are displayed in Fig. 2.24. It can be observed, that the currents are shifted with the desired phase shift angles of 60 °. The difference in current amplitude is caused by limited bandwidth of several of the utilized measurement probes.
Figure 2.24: Charging module currents during six fold interleaved charging operation of Fig. 2.23. The 60 degree current phase shift is clearly visible for all six charging units.
The droop compensation system is the most sophisticated part of the modulator. It comprises four identical pulse units, depicted in Fig. 1.9, each connected to a transformer core leg. These four pulse units in turn are composed of a switching unit, a capacitor bank and an active bouncer system. The switching unit transforms the primary DC voltage into the desired pulse shape. Since during the pulse, a voltage droop occurs in the capacitor bank, the pulse voltage would fall below the specified voltage band. Thus, a system is required, which can compensate the voltage droop for the entire specified load range of CLIC, while the voltage ripple on the output voltage pulse must remain small. These requirements are met by the active bouncer system, consisting of six bouncer modules per pulse unit.

In the following, section 3.1 presents a brief the state of the art of bouncer circuits, followed by the description demands on the CLIC bouncer system including the topology selection. Thereafter, the design procedure of a single bouncer module is presented in section 3.6, in which the concept and operation principle of an active bouncer in series to the main capacitor bank is described. The analysis of a single module is further detailed in section 3.2 with emphasis on the current measurement of the module. Furthermore, in section 3.3 the applied control scheme, current mode control (CMC), is presented and compared to standard duty cycle control. The single module operation and recharging process via the series connected main capacitor bank is described in section 3.7 and the pulse unit arrangement as well as measurements of the interleaved bouncer module operation are presented in section 3.4. Additionally, a repeatability analysis of a single pulse unit is conducted.
In section 3.7, this analysis is performed for open loop control and in section 3.5 for the current mode control operation.

3.1 Bouncers in solid state modulators

In most pulse power modulators, the pulse energy is provided by a capacitor bank. In order to limit its size, bouncer circuits are commonly used, which compensate the droop of the main capacitor bank. For short pulses with a range of a few microseconds, passive bouncer circuits are applied, which mostly make use of a \( L-C \) resonance \[76, 77\]. For low power applications also \( L-R \) bouncers are employed \[78\]. Passive bouncer circuits are electrically connected in series to the main capacitor bank and in a transformer based solution are placed either on the primary side, the secondary side or with a separate winding \[52, 77\]. For long pulse modulators, passive concepts are applied but also active solutions based on multi phase buck converters have been proposed, since the pulse length is sufficiently large for switching cycle based correction of the pulse voltage \[61, 79, 80\].

3.1.1 Demands on the CLIC bouncer system

The challenges for the CLIC bouncer system concern the fast pulse settling time \( t_{\text{settle}} = 8 \mu s \) and the high pulse energy.

The selected active bouncer system for CLIC is mounted on the primary side of the transformer as depicted in Fig. 3.1 a). The system is placed in series to the main capacitor bank, which reduces the demands on the the blocking voltage capability of the semiconductors. At the same time, the connection in series to the main capacitor bank requires an increased current load capacity of the bouncer system, since besides the current \( i_b \), which is required to charge the output capacitance of the bouncer system \( C_{\text{Bout}} \), also the load current \( i_l \) must be provided.

The short pulse settling time \( t_{\text{settle}} \) is especially demanding for the bouncer system, since the output current must change from zero to nominal value within this period. In order to achieve the required current rate of change, a low inductance value and a very high converter bandwidth would be required.

Assuming a standard buck topology with \( n_{\text{ph}} \) interleaved phases and an input voltage of \( V_{\text{Bin}} = 450 \text{ V} \), the highest applicable inductance value
would result in
\[
L_b = \frac{n_{ph} \cdot V_{Bin} \cdot t_{settle}}{I_{prim}} = 3e^{-7} \cdot n_{ph}. \quad (3.1)
\]

The highest current ripple \( \Delta I_L \) of a buck converter in continuous conduction mode (CCM) with steady state conditions occurs at a duty cycle of \( D = 0.5 \), which is described by
\[
\Delta I_L = 0.25 \frac{V_{Bin}}{L_b \cdot f_s}, \quad (3.2)
\]

where \( f_s \) is the switching frequency. With \( f_s = 100 \text{ kHz} \) the current ripple results to \( \Delta I_L = 3750 \text{ A} / n_{ph} \), which corresponds to 31.25\% of the nominal primary current in case of a single bouncer module (\( n_{ph} = 1 \)). If the current ripple was kept below \( \Delta I_L \geq 50 \text{ A} \), 75 bouncer modules would be required, or the switching frequency would have to be increased. Additionally, the bouncer system would need a high controller bandwidth, as it must react very fast on a 100\% load change. Since the voltage oscillations are to be minimized during the pulse flat-top, the controller design for such a system would be very demanding.
Therefore, standard DC-DC converters as e.g. proposed in [61][80] seem to be impractical for the given CLIC specifications. In order to avoid the high bandwidth requirement due to the short \( t_{\text{settle}} \), we proposed a new topology in section 3.6 [81], which consists of a half bridge converter with an additional short circuit switch \( S_{cs} \) as depicted in Fig. 3.1b). Due to \( S_{cs} \), a required current level can be built up in the inductance \( L_b \) prior to the pulse interval. The major advantage of this concept is, that the required current is provided directly at beginning of the pulse and no ramp up dynamics of the bouncer system have to be considered. The bouncers’ output capacitances \( C_{Bout} \) can directly be charged at beginning of the pulse interval with the foreseen current value, compensating the main capacitor’s voltage droop. Therefore, the inductance value can be chosen independently of \( t_{\text{settle}} \), which also offers a reduction in the number of deployed interleaved bouncer modules. As the required current value is provided by the bouncer system at the beginning of the pulse interval, \( t_{\text{settle}} \) is determined by the characteristics of the transformer and only marginally influenced by the dynamic behaviour of the bouncer system. By choosing a half bridge converter topology, the transmitted energy to the bouncer’s output capacitance \( C_{Bout} \) during the pulse interval can be recovered, resulting in an increased system efficiency.

An in depth analysis of the bouncer module operation is described in section 3.7. In the following paragraph, the design aspects of a single bouncer module are outlined.

### 3.2 Design aspects of a bouncer module

The concept of the active bouncer system is detailed in section 3.6 including the different operation phases and the selection of the required components. However, during the course of the project an increase in the power capability of the modulator was requested, which also imposed a modification of the active bouncer system. Thus, the adapted design is briefly presented in this paragraph. Since the output voltage ripple is influencing the repeatability of the modulator, a worst case output voltage ripple analysis is conducted in section 3.6. This analysis is complemented in this paragraph by considering the the actual measured inductance values of the bouncer modules, showing a drastic ripple reduction in comparison to the previously conducted worst
Table 3.1: Single bouncer module specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{Bin}$</td>
<td>450 V</td>
</tr>
<tr>
<td>$V_{Bout}$</td>
<td>0-300 V</td>
</tr>
<tr>
<td>$I_{b,nom}$</td>
<td>520-632 A</td>
</tr>
<tr>
<td>$C_{B,\text{out}}$</td>
<td>66 $\mu$F</td>
</tr>
<tr>
<td>$C_{B,\text{in}}$</td>
<td>2 mF</td>
</tr>
<tr>
<td>$L_{B}$</td>
<td>31 $\mu$H</td>
</tr>
<tr>
<td>$L_{B,\text{max}}$</td>
<td>33 $\mu$H</td>
</tr>
</tbody>
</table>

case assumption. Additionally, the onboard current measurement of a bouncer module is analyzed in detail, since it is a key component for the selected control scheme and exerts a major influence on the pulse to pulse repeatability of the entire modulator system.

3.2.1 Hardware design of a bouncer module

The design procedure of an active bouncer module is described in detail in section 3.6.

According to the final CLIC specifications, which were adapted during the course of the project, the modulator must be capable to provide a primary current of up to $I_{\text{pulse}} = 12$ kA. To keep the voltage droop limited to $\Delta V_{\text{main}} = 300$ V, the value of the main capacitor bank $C_m$, deployed in a single pulse unit, had to be increased by 50% to 1.5 mF. The increase in pulse current capability of the modulator also influences the design of the bouncer modules. Keeping equal relation of $C_m$ and $C_{B,\text{out}}$ as described in section 3.6, a total current requirement for all bouncer modules results to $I_{b,\text{tot}} = 15$ kA. Therefore, the number of modules is increased from 20 to 24, which leads to the specifications of a single bouncer module listed in tab. 3.1. Additionally, the number of high side and short circuit switches ($S_{hs}$ and $S_{cs}$) is increased from five to six.
Bouncer inductor design

After the pulse phase (see Fig. 3.33), the remaining energy in the inductances $L_B$ of the bouncer modules, is transmitted via a resonance transition to the output capacitors $C_{B,\text{out}}$. In order to keep the output voltage limited to $V_{Bout,\text{max}}$ the maximum inductance value $L_{B,\text{max}}$ is obtained by

$$L_{B,\text{max}} = \frac{C_{B,\text{out}} \cdot (V_{Bout,\text{max}}^2 - V_{Bout,\text{end}}^2)}{(I_{b,\text{nom}} + 0.5 \cdot I_{\text{rip,\text{max}}})^2},$$  \hspace{1cm} (3.3)

where $V_{Bout,\text{end}}$ is the charged voltage level at the end of the pulse, $C_{B,\text{out}}$ the output capacitance, $I_{\text{rip,\text{max}}}$ is the ripple current $I_{b,\text{nom}}$ the nominal current.

The highest current mean value $I_{b,\text{nom}}$ of the operation range occurs with a primary pulse voltage level of 2.5 kV, where the output voltage increase due to the resonance transition is less critical for the pulse switches. Therefore, the limiting factor for $L_{B,\text{max}}$ is the reverse blocking voltage of the short circuit switches $V_{\text{rev}} = 650 \text{ V}$, which limits $V_{Bout,\text{max}}$. In order to operate below $V_{\text{rev}}$ with a safety margin, the bouncer’s output voltage is limited to $V_{Bout,\text{max}} = 550 \text{ V}$. With this output voltage boundary, a maximal current ripple of $I_{\text{rip}} = 40 \text{ A}$ and parameters of tab. 3.1 the maximal bouncer inductance value results in $L_{B,\text{max}} = 33 \mu\text{H}$. To remain below $L_{B,\text{max}}$ even with component tolerances, the inductance value of the bouncer module was designed to $L_B = 31 \mu\text{H}$.

The inductor design for the active bouncer module must consider a high pulse current with a peak value of up to 670 A as well as the superimposed high frequency component due to the switching frequency of 100 kHz. At the same time, a low inductance value of $L_B = 31 \mu\text{H}$ is required, which limits the number of applicable turns. In order to reduce the large magnetic cross sectional area, resulting from the demand of a high current with low number of turns, a core material with a high saturation flux density is selected.

The chosen core material is Metglas alloy 2605SA1, which offers a high saturation flux density of 1.56 T and moderate high frequency losses. An optimization of the inductor was conducted taking into account skin and proximity losses as well as magnetic core losses. The investigated core shape is an E-core. Since the required inductance air gap is large,
Table 3.2: Results of the bouncer inductor optimization considering skin, proximity and magnetic core losses. Temperatures according to the applied thermal model are listed.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance value</td>
<td>31 $\mu$H</td>
</tr>
<tr>
<td>Number of turns</td>
<td>10</td>
</tr>
<tr>
<td>Number of conductors</td>
<td>2 in parallel</td>
</tr>
<tr>
<td>Number of strands</td>
<td>1050</td>
</tr>
<tr>
<td>Strand diameter</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>Total air gap</td>
<td>10 mm</td>
</tr>
<tr>
<td>Distributed air gap (calc)</td>
<td>5 mm</td>
</tr>
<tr>
<td>Distributed air gap (realized)</td>
<td>5 mm</td>
</tr>
<tr>
<td>Core material</td>
<td>Metglas alloy 2605SA1</td>
</tr>
<tr>
<td>$P_{core}$</td>
<td>2 W</td>
</tr>
<tr>
<td>$P_{prox}$</td>
<td>1 W</td>
</tr>
<tr>
<td>$P_{skin}$</td>
<td>8.6 W</td>
</tr>
<tr>
<td>$T_{ambient}$</td>
<td>40 °C</td>
</tr>
<tr>
<td>$T_{core}$</td>
<td>74.5 °C</td>
</tr>
<tr>
<td>$T_{winding}$</td>
<td>86 °C</td>
</tr>
</tbody>
</table>

a 3D air gap model was applied according to [69]. Additionally, a thermal model according to [82] was employed. Since the selected cooling fans feature a low power rating, a conservative heat transfer coefficient of $\alpha = 15$ W/(m$^2$K) was assumed. The results are listed in tab. 3.2. It can be observed, that the skin losses, that include DC losses, are dominant. Due to the few turns the proximity losses are small. The inductance was realized with a distributed air gap. In order to reach the desired inductance value, the air gap of the realized inductors had to be increased in comparison to calculations to $l_{gap} = 6$ mm per side. In order to simplify the arrangement and to reduce tolerances in the inductance value, a custom coil former was designed, which incorporates the air gap as well as the connection to the converter housing.

Semiconductor analysis

The bouncer operation requires a high unipolar pulse current and therefore omits soft-switching techniques such as triangular current mode
Table 3.3: Losses distributed in $S_{hs}, S_{ls}, S_{cs}, D_{hs}, D_{ls}$
(see schematic in Fig. 3.20)

<table>
<thead>
<tr>
<th>Loss</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{Shs}$</td>
<td>37.6 W</td>
</tr>
<tr>
<td>$P_{Sls}$</td>
<td>3 W</td>
</tr>
<tr>
<td>$P_{Scs}$</td>
<td>1 W</td>
</tr>
<tr>
<td>$P_{Dhs}$</td>
<td>1.8 W</td>
</tr>
<tr>
<td>$P_{Dls}$</td>
<td>6.7 W</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>50.1 W</td>
</tr>
</tbody>
</table>

(TCM). That is the reason why MOSFETs were excluded from further considerations. Due to the high operating frequency during the pulse interval, an IGBT with low switching losses is required, which safely turns off a pulse current higher than its nominal current rating. The $IKW40N65F5$ with copacked diode from Infineon was selected, which suited the given requirements best at the point of comparison. In order to facilitate the cooling for the 24 bouncer modules, air forced cooling was foreseen. Since the bouncer operation requires a much higher current in buck mode than in boost mode, six high side switches and two low side switches were applied, with additional four low side diodes, the $IDW40E65D1$. The required short circuit switch for the current ramp up phase is composed of six $IKW40N65F5$ in parallel. Switching and conduction losses were calculated according to [83] and are listed in tab. 3.3. Even though in a single high side switch ($S_{hs}$) losses of only 6 W on average occur, they are concentrated on the short pulse interval. Therefore, a time dependent loss analysis was conducted for a pulse interval based on a Foster model, with parameters selected from the data sheet. The conditions were chosen as described in section 3.6.7. The thermal cycling of the high side switch $S_{hs}$ results in $\Delta T_j = 24^\circ$, even though its average junction temperature increases by only $\Delta T_{j,av} = 1.4^\circ$. The transient temperature analysis shows, that the number of high side switches in parallel can not be reduced; otherwise excessive temperature cycling would lead to a reduced life time of the devices.
3.2.2 Impact of component tolerances on current ripple

Since the pulse to pulse repeatability as described in section 2.4 is influenced by the flatness of the pulse, the output voltage ripple, induced by the active bouncer modules is to be minimized. In section 3.6 an output voltage ripple analysis is conducted, which assumes a worst case inductance tolerance of 20% and a worst case jitter in the optical gate path of $t_{jit} = 5$ ns. Both parameters influence the current ripple of the bouncer system as well as the investigated output voltage ripple. In section 3.7 a measurement of the jitter in the optical gate path of $S_{hs}$ is conducted, which results in a standard deviation of the switching point of $\sigma_{t,jit} = 150$ ps. Since the measured influence of the jitter is much lower than originally assumed, its influence on the current ripple of the active bouncer system is minor. Therefore, jitters in the optical gate path are neglected in the following current ripple analysis.

23 inductance values of the bouncer modules have been measured, in order to investigate production tolerances. The estimation of the mean inductance value from the samples results to $L_{av} = 31.5 \, \mu\text{H}$ with an estimated variance of $s^2 = 0.0059 \, \text{pH}$. The corresponding standard deviation results to $\sigma = 0.243 \, \mu\text{H}$, which is a relative deviation of $\Delta L_{rel} = 0.773 \%$.

In order to visualize the effect of deviating inductance values, a pulse unit with six interleaved bouncer modules is investigated. The current and output voltage ripple in case of a steady state operation for a single switching period are computed for the entire duty cycle range. The six converters are assumed to operate with ideal phase shifting of $60^\circ$.

There are four different cases investigated regarding bouncer inductance tolerances:

- ideal
- measured values best case
- measured values worst case
- worst case globally

In the ideal case, all inductors feature equal inductance value with $L_{av} = 31.5 \, \mu\text{H}$. In best case arrangement, the inductors with closest inductance value are considered to operate with a phase shift of 180
degree, which will be referred to as opposite position. In the worst case arrangement, the highest and the lowest inductance value are arranged in opposite position. Finally, since for the entire CLIC project more than 1300 modulators are required, it is assumed that in a global worst case the inductors with values $(1 + n\sigma) \cdot L_{av}$ are in opposite position to the inductors with $(1 - n\sigma) \cdot L_{av}$. $n$ is selected to $n = 3$.

In all four cases, the current ripple in dependency on the duty cycle is depicted in Fig. 3.2. It can be observed, that in a best case arrangement of the inductors, the current ripple is very close to the ideal case. By worst case arrangement, the current ripple increases by 20% and for the globally worst case the increase amounts to 41%.

The difference in current ripple is amplified on the pulse unit’s output voltage, which is due to the series connection, directly visible on to the primary pulse voltage. Fig. 3.3 shows that with ideal inductor
arrangement, the voltage ripple deteriorates by 2.4 %, for worst case arrangement by 269 % and for the globally worst case by 417 %. The analysis reveals further, that due to the small production tolerances, the output voltage ripple for six interleaved bouncers can be kept for the lower primary pulse voltage level of 2.5 kV in a globally worst case below 6 ppm. By intelligent arrangement this value can even be reduced to 1.3 ppm. Therefore, no further ripple correction algorithms are required as e.g. proposed in [84]. Furthermore, it can be stated that an individual 6-fold interleaving of each pulse unit is sufficient to keep the primary output voltage ripple in the ppm range. Therefore, a 24-fold interleaving of the bouncer modules, achieved by a coupling of the four pulse units via the pulse transformer, is not a must, but still desirable.

Figure 3.3: Resulting output voltage ripple of a single pulse unit with 6 interleaved bouncer modules for the entire duty cycle range. Depicted are the four investigated cases.
Table 3.4: Desired bouncer current measurement features.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>value</th>
<th>unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower cutoff frequency (-1dB)</td>
<td>10</td>
<td>Hz</td>
</tr>
<tr>
<td>Upper cutoff frequency (-1dB)</td>
<td>1</td>
<td>MHz</td>
</tr>
<tr>
<td>Current range</td>
<td>-200 to 800</td>
<td>A</td>
</tr>
</tbody>
</table>

It should be noted, that thermal effects, influence of jitters and a variation in output voltage during an interleaved switching period, were not considered, which might deteriorate the output voltage ripple value resulting from this analysis. However, the interleaved voltage ripple is expected to remain in a dimension, where its influence on the repeatability is almost negligible, even when considering the mentioned effects.

The ripple analysis in this paragraph is limited to a single switching period. Effects influencing the pulse to pulse repeatability can however accumulate over several interleaved switching periods. Thus, repeatability analyses of a pulse unit for the entire pulse interval are conducted in section 3.7 and in section 3.5.

3.2.3 Current measurement of bouncer module

The onboard current measurement of the single bouncer module is presented in detail, since it is a requirement for the applied control scheme and exerts a significant impact on the repeatability of the modulator, which will be shown in section 3.5. At first, the measurement principle is explained. Thereafter, the optimization procedure of the current transformer is presented, which selects the number of turns depending on the external constraints and on the selected core material. Finally, a noise analysis of the current measurement’s analogue chain is conducted.

Measurement principle

The current measurement must feature a wide operation range, while offering a high frequency bandwidth. Current transformers are very well suited to fulfill these demands. The desired requirements for the current measurement are listed in tab. 3.4. The desired upper cutoff
frequency results from the 100 kHz switching operation, whereas the desired lower frequency should enable the current measurement to determine the pulse flat-top correctly. Since a pulse current is measured, the measurement core can be demagnetized during the pulse pause, which allows to drastically decrease its size.

The measurement principle is depicted in Fig. 3.4. It includes a bidirectional switch, two Zener diodes connected in opposite direction, the current transformer with its parasitics and the resistive burden. During the pulse interval, the bidirectional switch is closed. The transformer induces an N-times smaller current $i_s$ into the measurement circuit. The voltage at the resistive load is proportional to $i_s$ as long as the magnetizing current via $L_m$ remains small, which defines the lower cutoff frequency of the measurement circuit. The upper cutoff frequency is defined by the resonance frequency of the current transformer. During the pulse pause, the magnetizing current $i_m$, which is build up during the pulse interval, would have to be dissipated via the resistive burden. The time constant of such an $R−L$ circuit is in the ms-range. In order to realize a fast demagnetization of the magnetic core, the bidirectional switch is opened and the current $i_m$ is forced to discharge via the Zener diodes. The resulting reverse voltage of $V_{rev} = 3$ V leads to a fast current decay of $i_m$. Due to the reverse connected diodes and the
Table 3.5: Selected components and the resulting features of the current measurement

<table>
<thead>
<tr>
<th>Parameter</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Burden resistor value</td>
<td>200 mΩ</td>
</tr>
<tr>
<td>Number of turns</td>
<td>85</td>
</tr>
<tr>
<td>Core dimensions</td>
<td>25.3x14.8x10 mm</td>
</tr>
<tr>
<td>Core material</td>
<td>T38-SIferrite</td>
</tr>
<tr>
<td>Main inductance $L_m$</td>
<td>77.3 mH</td>
</tr>
<tr>
<td>RMS current density winding</td>
<td>3.98 A/mm²</td>
</tr>
<tr>
<td>Peak flux density</td>
<td>0.209 mT</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>2.353 mV/A</td>
</tr>
<tr>
<td>Magnetizing current</td>
<td>0.15 %</td>
</tr>
<tr>
<td>Power dissipation $P_{R,l}$</td>
<td>0.12 W</td>
</tr>
<tr>
<td>Demagnetization time</td>
<td>0.33 ms</td>
</tr>
</tbody>
</table>

In order to reach a high upper cutoff frequency, the number of turns was minimized, while fulfilling all listed constraints, thus minimizing the distributed capacitance of the winding $C_d$. The selected parameters and components are listed in tab. 3.5 together with the resulting features of the current measurement.

In order to verify the transfer characteristic of the current measurement, a frequency sweep was conducted with an impedance analyzer.
Figure 3.5: Transfer characteristic of current measurement depicted on a semilogarithmic scale. Additionally, the ideal sensitivity and the deviation in transfer characteristic of -1 dB are indicated. The -1 dB line is intersected at 2 Hz and 960 kHz.

The resulting transfer function is depicted in Fig. 3.5. It can be observed, that the transfer characteristic is very linear from $10^1 - 2 \cdot 10^5$ Hz. The -1 dB cutoff frequency at the lower and upper end are 2 Hz and 960 kHz respectively. The upper cutoff frequency is still well above the switching frequency of 100 kHz, which is why a deviation to the desired specifications of tab. 3.4 is accepted.

Noise analysis of current measurement

Since the repeatability is an important system parameter, a noise analysis of the current measurement analogue chain is modeled with a circuit simulation tool. Thereafter, the analysis is verified by converter measurements.

The investigated analogue chain is depicted in Fig. 3.6. It consists of an instrumentation amplifier, with an amplification of 1.7981. Since bipolar currents have to be measured, but the measurement range is
asymmetrical (see. tab. 3.4), the output of the instrumentation amplifier is shifted with an offset voltage of $V_{offs} = 816 \text{ mV}$. The signal is then decoupled by a voltage follower and filtered with a first order low pass filter, before it reaches the positive input of the comparator.

The noise analysis is conducted with *Multisim*, resulting in a frequency dependent output noise power density depicted in Fig. 3.7. It

**Table 3.6:** Current measurement noise parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Oscilloscope</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage sensitivity</td>
<td>10 mV/div</td>
<td>517 $\mu$V</td>
</tr>
<tr>
<td>Time scaling</td>
<td>1 ms/div</td>
<td></td>
</tr>
<tr>
<td>Sample rate</td>
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<td></td>
</tr>
<tr>
<td>Standard deviation noise (av)</td>
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<td>8 $\mu$V</td>
</tr>
<tr>
<td>Number samples</td>
<td>49000</td>
<td></td>
</tr>
<tr>
<td>Standard deviation on samples</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard deviation noise oscilloscope</td>
<td></td>
<td>489 $\mu$V</td>
</tr>
</tbody>
</table>
Figure 3.7: Frequency dependent output noise power density. The noise intake reduces for frequencies exceeding the cutoff frequency of the low pass filter $f_{\text{cut}} = 1.95$ MHz.

can be observed, that the noise intake reduces from $f_{\text{cut}} = 1.95$ MHz, which is the cutoff frequency of the first order low pass filter. With this analysis, a total noise at the comparator input of $\sigma_n = 196 \, \mu V$ results. If the low pass filter cut off frequency would be lowered by a decade, $\sigma_n$ could be reduced to 71 $\mu V$. With the filter cutoff frequency close to the switching frequency, the turn off point in time of the comparator will be affected. Since measurement immunity to noise is more important than its accuracy, the low pass filter is one of the parameters, which could be adjusted in the future to increase the pulse to pulse repeatability further.

In order to verify the noise analysis of the analogue chain, the voltage deviation on the comparator input $\sigma_{\text{comp}}$ was measured on the bouncer module with parameters listed in tab. 3.6. The oscilloscope itself shows a standard deviation of $\sigma_{\text{oszi}}$, which is in the same range than the measured parameter. Assuming that the voltage noise of both sources is independent, the actual comparator input noise $\sigma_{\text{comp}}$ can be derived
by

\[ \sigma_{\text{comp}} = \sqrt{\sigma_{\text{meas}}^2 - \sigma_{\text{oszi}}^2}, \]  

which results in \( \sigma_{\text{comp}} = 168 \mu V \). The noise measurement and the previously conducted simulation show a close match. The simulation tool matches the measurement exactly, when a filter cut off frequency of \( f_{\text{cut}} = 1.4 \text{ MHz} \) is assumed. So differences can very well be explained by component tolerances or additional parasitic capacitances in the real design.

The noise of the current transformer was not considered in this analysis. Therefore, in section 3.5 a total measurement noise of \( \sigma_{\text{comp}} = 200 \mu V \) will be assumed as worst case assumption in the following analyses.

### 3.2.4 Bouncer communication

All 24 bouncer modules are included in the high level communication structure (see section 5.1.1) as EtherCAT slave. Via this data link, parameters can be adapted if a load change is required, or the feed-forward strategy must be refined. Furthermore, the error handling is simplified, since all converter errors are centrally indicated. However, this data link features cycle times in the ms range and therefore can not be applied for data exchange during the pulse. Thats why, in addition, all bouncer modules are controlled by a central pulse control unit (see section 5.1.2). Each module receives the master data together with the master clock and transmits its own data together with its local clock. The data are transmitted via optical fiber with a rate of 25 Mbit/s and feature a 6B8B encoding. The transmitted data values feature a length of two data packages, which results in a data update rate of 640 ns. With 6B8B encoding, there exist three words, which do not occur in the data stream. These words are used to exchange status signals and to align the data stream.

### 3.3 Current mode control

Besides the standard duty cycle control, each bouncer module offers the possibility to operate with current mode control (CMC), which is also known as current programmed control [85]. At first the CMC method is briefly described, followed by the advantages and drawbacks in com-
3.3.1 Operation principle of CMC

The converter’s inductor current is measured and compared to a reference value $I_{\text{ref}}$. Once $I_{\text{ref}}$ is exceeded, the switches are turned off and the inductor current decreases. The turn on point of the switches is independent from the current value and occurs with a fixed frequency. The principle of CMC is depicted in Fig. 3.8 for a fixed current reference value $I_{\text{ref}}$. Since the turn on time and the peak value of the current are fixed, the mean current of a period $I_{\text{av},x}$ of a period $x$ can vary.

Due to the fixed frequency, CMC offers a simple and repeatable current interleaving, which is crucial for the output voltage ripple reduction (see section 3.2.2). This is an advantage to other current control schemes such as tolerance band control, where the switching frequency is variable. In order to keep the current ripple low in this case, an interleaving controller would be required, which increases the system complexity and might induce more non-repeatability in the system. Therefore, tolerance band control is excluded from further analysis and the focus is set on the comparison between CMC and standard duty cycle control:
CMC in comparison to duty cycle control comprises the following advantages:

- Simplification of the transfer function
- Higher dynamics
- Inherent over current protection
- Improved current sharing for interleaving of converters

The occurring drawbacks are:

- Additional current measurement required
- Additional logic required
- Instability for duty cycles $D \geq 0.5$
- Spikes induced by the switching operation lead to an unwanted turn off

In the following sections CMC is compared to duty cycle control regarding all listed advantages and drawbacks.

### 3.3.2 Advantages of CMC

**Simplification of the transfer function**

The simplification of the transfer function applying CMC is exemplary analyzed for a system with a single bouncer module, neglecting the
pulse transformer, as depicted in Fig. 3.9 a) and b). The averaged converter models are applied according to [85]. For duty cycle control, the bouncer module’s input voltage is simplified to a voltage source. The open loop transfer function $G_{duty}$ for duty cycle control, which describes the conversion from the averaged bouncer input voltage $D V_{in}$ to the output voltage $V_{out}$, can be described by

$$G_{duty}(s) = \frac{V_{out}}{D V_{in}} = \frac{s \cdot C_m R_l}{C_{Bout} C_m L R_l \cdot s^3 + (C_{Bout} + C_m) L \cdot s^2 + s \cdot C_m R_l + 1}.$$  \hspace{1cm} (3.5)

For CMC, the inductor current can be simplified to a current source as depicted in Fig. 3.9 b) . This simplification is justified, since the bouncer current ripple is smaller than 6.5% of the mean inductor current value. The open loop transfer function $G_{CMC}$, describing the relation from the mean inductor current $\bar{I}_L$ to the output voltage $V_{out}$, can be obtained by

$$G_{CMC}(s) = \frac{V_{out}}{\bar{I}_L} = \frac{C_m R_l}{(C_{Bout} C_m \cdot s + (C_{Bout} + C_m)}.$$  \hspace{1cm} (3.6)

Due to the simplified open loop transfer function, caused by the reduction in poles, as depicted in Fig. 3.10 the phase margin is increased, as well as the gain at lower frequencies. The increased phase margin offers a better tolerance to component variations and parameter variations due to e.g., temperature drift.

**Higher dynamics**

Comparing the systems of Fig. 3.9 it is obvious, that in CMC the current is controlled, which is proportional to the output capacitor charge $Q_{C_{Bout}}$. In duty cycle control, the voltage ratio is controlled, which is proportional to the integral of the charge $\int Q_{C_{Bout}}$. Therefore, the higher dynamics are achieved with CMC.

**Inherent over current protection**

Since in CMC, the peak current is controlled, this method inherently limits the inductor current. As an analogue comparator is applied, the delay between detection of the current value and turn off the switch is reduced in comparison to a standard current measurement with an analogue digital converter (ADC).
Figure 3.10: Open loop transfer characteristic of the simplified systems depicted in Fig. 3.9a) and b). It can be observed, that the system for CMC offers a higher gain at lower frequencies and a higher phase margin than the system operated with duty cycle control.

**Improved current sharing for interleaved converters**

For analysis of the current sharing, a standard buck topology, operating in continuous conduction mode, is investigated.

For duty cycle control, the ripple current $I_{\text{rip}}$ is zero-mean in steady state operation and the following relation exists with the average current $I_{\text{av}}$

$$\int_0^T I_{\text{rip}} \cdot I_{\text{av}} = 0.$$  \hspace{1cm} (3.7)

This allows the superposition of both quantities. Applying duty cycle control, the RMS-current $I_{\text{RMS}}$ can be therefore described by

$$I_{\text{RMS}} = \left(1 + \frac{k}{\sqrt{3}} \right) \cdot I_{\text{av}},$$ \hspace{1cm} (3.8)
where $k$ is the ratio of ripple current $I_{\text{rip}}$ and mean current $I_{\text{av}}$.

Assuming a fixed operation frequency, a converter with an decreased inductance value of $L'$ in comparison to the reference value $L_{\text{ref}}$ with

$$L' = (1 - x) \cdot L_{\text{ref}}$$  \hspace{1cm} (3.9)

will be subjected to a higher RMS current $I'_{\text{RMS}}$ with

$$I'_{\text{RMS}} = \frac{1 + \frac{k}{\sqrt{3}(1-x)}}{1 + \frac{k}{\sqrt{3}}} \cdot I_{\text{RMS}}.$$  \hspace{1cm} (3.10)

Assuming $k$ and $x$ to 20%, which are plausible values, $I_{\text{RMS}}$ of the converter with lower inductance value is increased by 2.6%.

With the current mode control scheme, the measured current value is compared to a fixed reference value, which limits the peak current to equal level for all inductance values of the interleaved converters. The RMS-current $I_{\text{RMS,CMC}}$ can therefore be described by

$$I_{\text{RMS,CMC}} = I_{\text{peak}} - \frac{I_{\text{rip}}}{2} + \frac{I_{\text{rip}}}{\sqrt{3}} = I_{\text{peak}} + 0.0774 \cdot I_{\text{rip}}.$$  \hspace{1cm} (3.11)

Since the peak current $I_{\text{peak}}$ remains equal, the RMS current differs in dependence on the variation in inductance value $x$ and with $I_{\text{rip}} = k \cdot I_{\text{peak}}$ according to

$$I'_{\text{RMS,CMC}} = \frac{1 + 0.0774 \cdot \frac{k}{(1-x)}}{1 + 0.0774 \cdot \frac{k}{I_{\text{RMS,CMC}}}} I_{\text{RMS,CMC}}.$$  \hspace{1cm} (3.12)

Assuming again $k$ and $x$ to 20%, an increased $I'_{\text{RMS,CMC}}$ of only 0.38% results compared to the 2.6% increase in case of duty cycle control.

Besides the lower $I_{\text{RMS}}$ current difference, which allows a better match of the semiconductors, current mode control also simplifies the design of the magnetic components. Since the peak current value is fixed, a change in inductance value is less critical, when operating at the border of the linear region of the B-H loop.

### 3.3.3 Drawbacks of CMC

Applying current mode control requires a current measurement as well as additional circuitry. For protection reasons, due to the high pulsed
currents, a current measurement is required. Thus, the additional effort is limited to a high speed comparator. The resulting higher dynamics more than justify that cost. For duty cycles $D \geq 0.5$, CMC becomes instable, which can however be avoided by implementing an artificial ramp. A profound analysis of the influence of the artificial ramp can be found in section 3.3.5. Due to voltage spikes caused by converter switching, especially for small duty cycles, the comparator might send a turn off signal too early. In order to eliminate this error, the comparator’s turn off signal can be omitted for a certain time after the turn on of the switch. The so-called leading edge blanking is described further in section 3.3.5.

3.3.4 Conclusion of comparison

The advantages of CMC in comparison to duty cycle clearly outweigh the drawbacks. Furthermore, the drawbacks of CMC can be compensated with little more effort in programming software. Especially the high dynamics of CMC are essential to provide a high dynamic control loop. Even without a feedback loop, CMC offers a stabilizing effect, since the peak current value and the switching period are kept constant. Therefore, CMC is also suitable for open loop operation as will be shown in section 3.5.

3.3.5 Application of current mode control for CLIC

In order to apply CMC during the pulse, two effects have to be considered, which are the instability for duty cycles $D > 0.5$ and the distortion of the comparator signal due to high voltage transients. Both effects will be discussed in the following paragraphs. Additionally, the feedforward strategy for the CMC implementation on the bouncer module is briefly described.

**CMC for $D \geq 0.5$**

A characteristic of current mode control is that it becomes instable for duty cycle values $D > 0.5$, since then current perturbations are increased with subsequent periods [85]. The periods of the bouncer with
DROOP COMPENSATION SYSTEM

duty cycle $D \geq 0.5$ are limited due to the short pulse interval and therefore stability is less of an issue.
The increasing perturbations, however, lead to harmonic distortion, which occur with the operating frequency of a single bouncer module, thus impairing the ripple reduction originating from the module interleaving. In order to cancel the distortion, an artificial slope compensation is applied, whereby the current reference value starts with an offset, which is decreasing with a predefined slope rate during the entire switching period. A stability analysis for different slope rates can be found in [85].

In the following, different slopes of the artificial ramp $m_{r,x}$ are analyzed with respect to the disturbance reduction ratio $|\alpha|$ [85], which determines the factor by which a distortion is diminished per subsequent switching period and can be derived by

$$|\alpha| = \left| \frac{V_{B_{\text{out}}}}{L} - m_{r,x} \right| \left| \frac{V_{\text{in}}}{L} - V_{B_{\text{out}}} \right| m_{r,x}.$$  (3.13)

There are three different slopes compared, which are

- $m_{r,1} = \frac{V_{\text{in}}}{L}$
- $m_{r,2} = \frac{V_{B_{\text{out}}}}{L}$
- $m_{r,3} = \frac{0.5V_{B_{\text{out}}}}{L}$.

The resulting $|\alpha|$ is depicted for all three slopes in Fig. 3.11 Since $|\alpha|$ is the rate by which the distortion is decreasing, a smaller $|\alpha|$ leads to a faster correction of the distortion. It can be observed, that choosing $m_{r,2}$ always results in $|\alpha| = 0$, which means that all distortions are directly canceled within the next switching period. Comparing $m_{r,1}$ to $m_{r,3}$, we can observe that for duty cycles $d \geq 0.5$ the slope $m_{r,1}$ provides the better distortion correction. From this analysis it would be most beneficial to chose $m_{r,2}$, a slope related to the output voltage. In case of CLIC, however, the output voltage is changing rapidly per switching cycle, $\Delta V_{B_{\text{out}}} \approx 21$ V. Since the system operates in a broad load range, the slope rate would have to be adapted to each operation point and also would have to be set differently for each bouncer module due to the interleaved operation. Since also deviations between
Figure 3.11: Disturbance reduction ratio $|\alpha|$ in dependence of the duty cycle for steady state operation. Indicated are three different gradients of the slope compensation ramp.

Precalculated and real value are to be expected due to the fast changing output voltage, the slope $m_r,1$ related to the input voltage of the bouncer module is selected.

**Leading edge blanking**

Since for turning off the switch a comparator signal is used, CMC is susceptible to voltage spikes induced by the switching operation, which can lead to a premature turn off signal. Due to the high operation frequency, fast IGBTs are applied, which feature high voltage transients when switching, thus causing the unwanted distortion. In order to suppress the influence of the distortions, the comparator turn off signal is ignored for a certain time interval $t_{leb}$ after the turn on operation of the switch, which is also referred to as leading edge blanking.

For CLIC, the minimal turn on time of the switch $t_{on,min}$, which
occurs in the operation, is obtained by

\[ t_{on,\text{min}} = \frac{0.5 \cdot \Delta V_{out} \cdot T_p}{V_{Bin}} = 0.233 \, \mu s \tag{3.14} \]

The selected leading edge blanking time had to be chosen to \( t_{leb,\text{min}} = 0.26 \, \mu s \). Since the required turn on time of the switch linearly increases with each subsequent period, only the first switching period of the bouncer is affected, which therefore does not deteriorate the error correction capability of the CMC operation.

**Feed-forward strategy**

Since the CLIC modulator system operates in a steady operation point, a high amount of the system behavior is known in advance. In order to reduce the amount of correction required by the controller, or to be able to operate without feedback loop, a feed-forward strategy is applied. The applied simplified converter model neglects the pulse transformer influence and assumes an ohmic load, as depicted in Fig. 3.9. In order to keep the primary voltage constant, all six interleaved bouncer modules must charge their output capacitance \( C_{b,\text{out}} \) at the same rate as the main capacitance \( C_m \) is discharged, as already described in detail in section 3.6. Therefore, the required mean inductor current \( I_{L,\text{nom}} \) can be described by

\[ I_{L,\text{nom}} = \frac{6 \cdot C_{b,\text{out}} + C_m}{C_m} \cdot \frac{V_{prim}}{R_l} \tag{3.15} \]

Since for CMC, the current peak value is required, which calculates in steady state operation to

\[ I_{\text{peak}}(t) = I_{L,\text{nom}} + \frac{\Delta I_L(t)}{2}, \tag{3.16} \]

the ripple current \( \Delta I_L \) must be considered. The inductor ripple of the bouncer is equivalent to the buck converter in CCM and is described by

\[ \Delta I_L = D \cdot (1 - D) \frac{T_s \cdot V_{Bin}}{L} \tag{3.17} \]

In Fig. 3.12 the bouncer current ripple is depicted in dependency on the pulse duration and shows a maximum in ripple current of 36.2 A.
Figure 3.12: Precalculated bouncer current ripple amplitude in dependency on the pulse duration. Depicted is the operation point with $I_{L,nom} = 468$ A and bouncer module’s output voltage range $V_{Bout,range} = 0 − 262$ V.

at $106 \mu s$. Assuming a constant bouncer input voltage $V_{Bin}$ the ripple current is obtained by

$$\Delta I_L(t) = \left(1 - \frac{V_{Bout}(t)}{V_{Bin}}\right) \cdot T_s \cdot \frac{V_{Bout}(t)}{L}, \quad (3.18)$$

where $T_s$ is the switching period and $V_{Bout}(t)$ the time dependent bouncer output voltage. $V_{Bout}(t)$ can be described by

$$V_{Bout}(t) = \left(\frac{6 \cdot C_{b,out}}{6 \cdot C_{b,out} + C_m} \cdot I_{L,nom}\right) \cdot \frac{t}{C_{b,out}}. \quad (3.19)$$

Combining (3.19), (3.18) and (3.16) leads to a precalculated time dependent peak current

$$I_{peak}(t) = I_{L,nom} + \frac{T_s \cdot 6 \cdot I_{L,nom}}{2 \cdot L (6 \cdot C_{b,out} + C_m)} \left(t - \frac{6 \cdot I_{L,nom} \cdot t^2}{(6 \cdot C_{b,out} + C_m) \cdot V_{Bin}}\right).$$

This time dependent peak current value is implemented as feed forward quantity on each bouncer module. The parameters of the equation
can be adapted depending on the operation point via the PLC communication. Via the fast optical link, the desired mean current value $I_{L,nom}$ can be adapted during the pulse interval.
3.4 Verification by measurements

The final arrangement of one of the four pulse unit is depicted in Fig. 3.13. The main capacitor bank is placed at the bottom. On top of the six bouncer modules, the discharge circuitry is positioned, which discharges and grounds all capacitors in the system in case of a modulator system turn off. To obtain a low inductive design, the pulse unit is connected to its corresponding pulse switch via a three layer busbar.

The operation of the pulse unit is validated with two bouncer modules operating at nominal power with a phase shift of 180°, with corresponding measurements depicted in Fig. 3.14. Measurements of a single bouncer module operation are presented in section 3.7.

![Interleaved bouncer module operation](image)

**Figure 3.14:** Pulse measurement with two bouncer modules operating at nominal power with a phase shift of 180°. The figure displays the combination of the main capacitor bank’s and the bouncer modules’ output voltage at the resistive load $V_{load}$ and the corresponding currents $I_B$ of bouncer modules 1 and 2.
Figure 3.13: Back side of the pulse unit with current busbar for a low inductive connection to the pulse modules. Front side of the pulse unit consisting of a main capacitor bank at the bottom and six bouncer modules. The discharge circuitry is placed at the top.
3.5 Repeatability analysis of a pulse unit

One of the main influences on the pulse to pulse repeatability (PPR, see section 2.4) of the modulator system is the behavior of the active system components during the pulse.

In practice, a certain klystron load is given and the modulator system always operates under equal load conditions. Hence, the control during the pulse can be accomplished by open loop control. The benefit of this control strategy is the much simpler design as no data transmission during the pulse interval is required. Additionally, deviations due to measurement distortions are inherently non existent. In this case, the remaining influences on the PPR are the initial voltage distributions of the system at the beginning of the pulse and the deviations in the switching instances due to jitters in the optical path of the gate signal. That’s the reason why a repeatability analysis of a pulse unit in open loop control is conducted in section 3.7.4.

Besides the open loop control, there is the possibility to operate the bouncer modules in current mode control (see section 3.3). Due to the involved current measurement in CMC, the repeatability of the pulse unit is influenced. Therefore, in this section, a repeatability analysis of a pulse unit is conducted considering the influence of CMC. Further, the results are compared to the findings in section 3.7.4.

When applying CMC, there are two additional influences, which must be considered in comparison to open loop control. The first is the noise on the current measurement, which is a source of non-repeatability. The second influence is the error correction capability of current deviations resulting from the previous switching periods. These two effects are analyzed in the following.

3.5.1 Influence of noise on the current measurement

In order to obtain the influence of the current measurement on the repeatability of a pulse unit, a simplified system is investigated on a single bouncer module. The DAC reference voltage is assumed to be ideal. In this case, the comparator turn off point in time only deviates due to noise induced on the current measurement.

The measured voltage noise on the current measurement, derived in section 3.2.3, is converted to a current noise considering the sensi-
Figure 3.15: Standard deviation of the bouncer module’s output voltage $\sigma_{Vp,\text{single}}$ per switching cycle in dependency on the output voltage level.

The activity of the current measurement according to tab. 3.5, resulting in $\sigma_{Ib} = 0.0850$ A. In order to derive the dependency between the deviation of the comparator’s turn off signal and the noise on the current measurement, a single period was investigated for the entire output voltage range 0-300 V. The current signal with the super positioned measurement error is compared to the reference signal with slope compensation ramp (see section 3.3.5). The point in time where the reference signal is surpassed defines the comparator’s turn off point. The hysteresis of the comparator was assumed to be repeatable and, therefore, is not considered in this analysis. Each switching period was computed with 10,000 independent runs and the standard deviation of the comparator’s turn off point $\sigma_{t,off}$ was derived. $\sigma_{t,off}$ is transformed into a standard deviation of the bouncer module’s output voltage $\sigma_{Vp,\text{single}}$ per switching cycle according to

$$\sigma_{Vp,\text{single}} = \frac{V_{Bin} \cdot t_{\text{per}}}{L_B \cdot C_{B,\text{out}}} \cdot \sigma_{t,off}. \quad (3.20)$$

The resulting $\sigma_{Vp,\text{single}}$ in dependency on the output voltage level $V_{Bout}$ is visualized in Fig. 3.15. It becomes clear, that the higher the output
Table 3.7: Parameters for determining the standard deviation of the pulse unit.

<table>
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<td>V</td>
</tr>
<tr>
<td>Bouncer input voltage (open loop)</td>
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<td>V</td>
</tr>
<tr>
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<td>V</td>
</tr>
<tr>
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<td></td>
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</tr>
<tr>
<td>$S_{hs,\text{off}}$</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>$N_{\text{sample}}$</td>
<td>2000</td>
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<td></td>
</tr>
</tbody>
</table>

Voltage is, the higher the deviation in the comparator’s turn off point becomes due to the noise on the current measurement. This effect leads to a higher $\sigma_{V_{p,\text{single}}}$ and is caused by the slower gradient of the inductor current for higher output voltages, which increases the probability of an early comparator turn off.

Assuming a worst case scenario, where all six bouncer modules of a pulse unit show the same voltage deviation in their subsequent interleaved switching periods, the highest output voltage deviation in a 10 $\mu$s interval would result to $\sigma_{V_{p,\text{single}}} = 5$ mV, according to (3.20) with $C'_{B,\text{out}} = 6 \cdot C_{B,\text{out}}$. This additional voltage deviation, caused by the noise on the current measurement, corresponds to negligible 1.67 ppm in relation to the primary voltage level of 3 kV. Thus, its influence is too small to deteriorate the repeatability of the pulse unit within a single switching period of a module.

Besides increasing the standard deviation of the pulse voltage due to measurement noise, the current measurement provides an error correction capability. Therefore, in the next paragraph this effect is investigated for a pulse unit with six interleaved modules and compared to the results with the pulse unit operated with duty cycle control in open loop.
3.5.2 Influence of the current measurement correctional behavior

In order to compare CMC to open loop control, the repeatability analysis is conducted with the approach and the specifications described in section 3.7.4. In a first analysis, all system voltages are assumed to be ideal and the current measurement noise as well as switching jitters in the bouncer modules are considered only. Other than in section 3.7, instead of a worst case jitter, the measured jitter standard deviation of $\sigma_s = 150\,\text{ps}$ is applied for the analysis. The results are depicted in Fig. 3.16, where the standard deviation of the primary pulse voltage $\sigma_{tj,pu}$ is visualized for the entire pulse length. It can be observed, that in CMC operation, the standard deviation of the primary pulse voltage increases earlier, but with a lower gradient. The correction capability of the measurement is not creating a benefit, since the voltage deviations induced by the switching jitters are by more than factor ten smaller in comparison to the turn off deviations caused by the noise on the current measurement.
Figure 3.17: Standard deviation of the primary pulse voltage $\sigma_{t_j,pu}$ for duty cycle control ($\sigma_{duty,Vbin=150\,ppm}$) in open loop and CMC ($\sigma_{CMC,Vbin=3000\,ppm}$) with parameters listed in tab. 3.7.

However, the correction capability of the bouncer current due to the CMC operation will exert a strong influence, if additionally variations in the system voltages are considered. Other than in section 3.7.4 the predicted charging accuracy of section 2.5 is considered here ($\sigma_{V_{out}} = 22\,mV$), which is by more than a factor of two lower. Thus, the standard deviation of the bouncer module’s input voltage $\sigma_{V_{bin}}$ can be chosen higher. The applied parameters are listed in tab. 3.7. In Fig. 3.17 the standard deviation of the primary pulse voltage $\sigma_{t_j,pu}$ is depicted for a standard deviation of the input voltage in case of open loop control with $\sigma_{duty,V_{bin}(t=0)} = 150\,ppm$ and in case of CMC with $\sigma_{CMC,V_{bin}(t=0)} = 3000\,ppm$. Even though $\sigma_{CMC,V_{Bin}(t=0)} = 20 \cdot \sigma_{duty,V_{Bin}(t=0)}$, the $\sigma_{t_j,pu}$ is in equal range. Thus, the application of CMC is essential in order to enable a relaxation of the precision requirement for the bouncer modules’ input voltage. Applying CMC, the precision requirement can even be relaxed such, that the onboard voltage measurements of each bouncer module can be applied for determining the voltage level during the recharge interval.
Besides relaxing the voltage precision requirement of the bouncer module’s input voltage, CMC can correct deviations in the main capacitor bank voltage to a certain extent. This effect is visualized in Fig. 3.18 where the results from section 3.7.4 Fig. 3.45 are compared to a CMC controlled version with equal parameters as listed in tab. 3.13. Additionally, $\sigma_{tj,pu}$ is displayed for the case with duty cycle control in open loop, if just $\sigma_{V\text{Main}(t=0)}$ is distorted by $\sigma_{V\text{Main}(t=0)} = 15$ ppm. Considering the entire pulse duration, the correction capability is visible, which is why CMC offers the lowest value $\sigma_{C\text{MC}}$ after an interval of 30 $\mu$s. Since the correction capability of CMC is not counteracting the $\sigma_{V\text{Main}(t=0)}$ at the beginning of the pulse, the voltage precision requirement of the main capacitor bank can not or only marginally be relaxed.

In conclusion of this repeatability analysis follows, that for CLIC the application of CMC is highly recommendable in comparison to duty cycle control in open loop. Besides the better current sharing and the

![Figure 3.18: Standard deviation of the primary pulse voltage $\sigma_{tj,pu}$ for duty cycle control in open loop ($\sigma_{duty}$) and CMC ($\sigma_{C\text{MC}}$) with parameters listed in tab. 3.13. Additionally, $\sigma_{tj,pu}$ is visualized in case of $\sigma_{V\text{Main}(t=0)} = 15$ ppm with all other system parameters considered to be ideal.](image-url)
faster overcurrent turn off capability (see section 3.3), especially the possibility to relax the bouncer modules’ voltage precision requirement justifies the additional effort in circuitry and software.
3.6 Design Procedure of an active Bouncer for an ultra precise long pulse solid state modulator

Sebastian Blume and Juergen Biela
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Abstract

Long pulse modulator systems like the electron-positron compact linear collider (CLIC) with a pulse length of 140 $\mu$s require a bouncer for voltage drop compensation. In this paper, an active bouncer system, consisting of four bouncer modules, in series to the main capacitor bank, is investigated. The system’s transfer function including the matrix pulse transformer is analysed and the output voltage ripple induced by the bouncer system is designed to be smaller than 5 ppm due to demanding repeatability requirement of CLIC. Based on a loss analysis is conducted resulting in a total bouncer system volume of 52 dm$^3$ and a reduction in the global efficiency (grid to klystron) of the modulator system of only 0.45 %.

3.6.1 Introduction

The electron-positron compact linear collider (CLIC), with a pulse length of 140 $\mu$s, requires a compensation of the output voltage drop in order to limit the size of the main primary capacitor bank. The CLIC system specifications, displayed in Tab.3.8 are very challenging regarding system efficiency and pulse repeatability. The proposed concept, displayed in Fig.3.19 is based on a pulse transformer with semiconductor switches, due to its simple, highly reliable structure and its short circuit protection capability. Due to the long pulse length, a passive bouncer solution would require large components. Therefore, an active bouncer system is investigated. In [61], an active bouncer for long pulse modulators has been analyzed. The bouncer for the CLIC system, however, requires higher power, higher dynamics and a significantly lower current ripple of the bouncer than the system in [61], since the bouncer influences the pulse shape and therefore must also meet the extremely high requirements on the pulse repeatability.
Figure 3.19: Overview of the proposed solid state modulator for CLIC.

Charging system connected to the 400 V grid. Each pulse module is supplied by a main capacitor bank in series with an active bounce system. All four systems are charged with one switching unit. Each pulse module is supplied by a main capacitor bank in series with an active bounce system. There are active bias units connected in parallel to each switching unit. These are active bias units connected in parallel to each switching unit. In order to double the possible flux swing, there are active bias units connected in parallel to each switching unit. In order to double the possible flux swing, there are active bias units connected in parallel to each switching unit. Each pulse module is supplied by a main capacitor bank in series with an active bounce system. All four systems are charged with one charging system connected to the 400 V grid. Each pulse module is supplied by a main capacitor bank in series with an active bounce system. There are active bias units connected in parallel to each switching unit. These are active bias units connected in parallel to each switching unit. In order to double the possible flux swing, there are active bias units connected in parallel to each switching unit. In order to double the possible flux swing, there are active bias units connected in parallel to each switching unit. Each pulse module is supplied by a main capacitor bank in series with an active bounce system. All four systems are charged with one	
Table 3.8: Modulator Specifications for CLIC

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>150 kV</td>
</tr>
<tr>
<td>Pulse output power</td>
<td>24 MW</td>
</tr>
<tr>
<td>Flat-top length</td>
<td>140 µs</td>
</tr>
<tr>
<td>Rise time</td>
<td>3 µs</td>
</tr>
<tr>
<td>Flat-top stability FTS</td>
<td>0.85 %</td>
</tr>
<tr>
<td>Pulse to pulse repeatability</td>
<td>10 ppm</td>
</tr>
<tr>
<td>Repetition rate</td>
<td>50 Hz</td>
</tr>
<tr>
<td>System efficiency (grid to klystron)</td>
<td>&gt; 90 %</td>
</tr>
</tbody>
</table>

In the paper first, a short overview of the proposed CLIC modulator system is given in section 3.6.2. Thereafter, the topology of the active bouncer is presented and system constraints are identified in section 3.6.3. Furthermore, in section 3.6.4, the bouncer’s output ripple is investigated in dependency on the number of interleaved modules and a worst case scenario for component tolerances is identified. Additionally, in section 3.6.5, the influence of the matrix transformer is considered deriving the entire system transfer function. Then, a bouncer configuration, which suits the ripple requirement, is derived in section 3.6.6. Finally, a system analysis regarding volume and efficiency is conducted in section 3.6.7.

3.6.2 Modulator concept

The investigated system, depicted in Fig. 3.19, is based on a solid state modulator with a pulse transformer, realized as matrix transformer outperforming transformers connected in series or parallel. The system consists of four primary switching units in parallel, which are magnetically coupled over two cores. On the secondary voltage level, the two cores enclosed by the secondary winding can be seen as a series connection, since their fluxes add to the secondary flux. In parallel connection to each switching unit an active bias circuit is included to reduce the core size. In order to use semiconductor switches without series or parallel connection, the chosen primary voltage level is \( v_p = 3 \text{kV} \), resulting in a total primary current of \( i_{p,ges} = 8000 \text{A} \). The considered switching units are 4.5 kV-1200 A-IGBT modules, which are operated with a pulse current of \( i_{p,mod} = 8 \text{kA/4=2 kA} \). The 4 active bouncer
modules are connected in series to the main capacitor bank. By increasing the voltage of the bouncer’s output capacitance, the voltage drop in the main capacitor bank is compensated, which results in a constant output voltage.

The desired pulse repeatability of 10 ppm in Tab. 3.8 corresponds to an output voltage band of 1.5 V. The system repeatability mainly depends on the precision of the charging units, on the jitter in the switching units and on the repeatability of the active bouncer.

The repeatability of an active system is affected by the output voltage ripple and switching jitters according to [88]. In a first step, the voltage ripple is focused in this paper. Therefore the active bouncer is designed to induce an output voltage ripple smaller than half the allowed voltage band, corresponding to 0.75 V. The influence of jitter on the repeatability will be focused in future publications.

In the following section the chosen bouncer topology and its integration into the system is discussed for one of four equal switching units.

### 3.6.3 Active bouncer topology

The active bouncer is based on an interleaved buck-boost converter, which is displayed in Fig. 3.20. It operates during the pulse in buck mode since $v_{CB,\text{out}}$ starts at 0 V and rises to $V_{B,\text{max}}$. Due to series connection to the main capacitor bank, the converter has to provide the pulse load current of $i_l=2\text{kA}$. In addition to $i_l$, a current $i_b$ must be provided to charge $C_{b,\text{out}}$. The current in one interleaved branch $i_m$
and the output voltage $v_{CB,\text{out}}$ are depicted in Fig. 3.21 for one pulse cycle. In order to provide the required current $i_l + i_b$, the output capacitor is bypassed during $T_1$ by closing the switch $S_{cs}$. $T_2$ begins, when the required current level is reached. $S_{cs}$ is opened while the main switching unit closes. The load current $i_l$ is then passing through the main capacitor bank and the klystron load, while $i_b$ is increasing the voltage of $C_{b,\text{out}}$. During the pulse, the switching frequency is $f_{s,\text{buck}}=100\,\text{kHz}$, to minimize the output ripple. After the pulse, at beginning of $T_3$, the main switch opens and the stored energy of inductors $L_b$ is transferred via the diode $D_{LS}$ to $C_{b,\text{out}}$. Since at this moment the voltage of $C_{b,\text{out}}$ is higher than the voltage of $C_{b,\text{in}}$, a resonant transition occurs, where the current swings back over $D_{HS}$. To obtain high efficiency, the remaining energy in $C_{b,\text{out}}$ is fed back in $T_5$ after a waiting period, $T_4 = 100\,\mu\text{s}$, via operating the bouncer in boost mode with $S_{LS}$ and $D_{HS}$. Since the ripple is uncritical during this time period, the switching frequency is chosen to $f_{s,\text{boost}}=20\,\text{kHz}$. To restore the initial state of $C_{b,\text{out}}$, it is entirely discharged via $S_{cs}$ in $T_6$.

**Energy constraints of system**

As described in the previous chapter, the entire stored energy in the bouncer inductances is transferred during $T_3$ to $C_{b,\text{out}}$. Therefore, the inductance value is limited in dependency on the output capacitor size and the blocking voltage of the switches.

In addition to that, arcing of the klystron load has to be considered as it occurs during normal system operation. In worst case the arcing takes place just after turn on of the switching units, when the main capacitor bank is still fully charged to $V_{\text{main}}=3\,\text{kV}$ and the bouncer inductances transfer the stored magnetic energy into the output capacitor $C_{b,\text{out}}$, resulting in a voltage rise $V_{B,\text{max}}$.

The switching units are affected by $V_{\text{main}}+V_{B,\text{max}}$, limiting $V_{B,\text{max}}$ to 500 V, since the 4.5 kV-switches should not be stressed further. If the arcing is detected fast enough, $C_{b,\text{out}}$ could be shortened by $S_{cs}$ and therefore the voltage stress for the switching units could be reduced. But to ensure high system life time, $V_{B,\text{max}}$ should not be exceeded even in the event of an arc detection failure.

Because of these system constraints and smaller switching losses, the use of 650 V switches is favored. This choice limits the bouncer input voltage to $V_{b,\text{in}} = 450\,\text{V}$. The chosen output voltage range is set to $V_{b,\text{out}}=0 – 300\,\text{V}$, which defines the voltage drop of the pulse to 10% and
Figure 3.21: Current in one interleaved module $i_m$ (Fig. 3.20) and the capacitor output voltage $C_{b,\text{out}}$ for one pulse cycle.

fixes the size of the main capacitor bank to $C_{\text{main}} = 1 \text{ mF}$. In Fig. 3.22 the maximal inductance value $L_{\text{max}}$ is depicted in dependency on $C_{b,\text{out}}$. A higher capacitance value leads to an increased ripple attenuation as will be shown in section 3.6.4 but also increases the required capacitor charging current $i_b$, which leads to higher losses. Therefore, the capacitance value is chosen to $C_{b,\text{out}} = 250 \mu\text{F}$ resulting in $L_{\text{max}} = 6.4 \mu\text{H}$ (Fig. 3.22).

3.6.4 Interleaving

To analyze the output ripple of the active bouncer, the ripple dependency is at first analyzed for the ideal case of equal inductance values. In a second step the worst case for component tolerances of the switches is identified.
Figure 3.22: Maximal inductance value $L_{max}$ in dependency on bouncer output capacitance $C_{b,\text{out}}$

**Ideal interleaving**

In case of equal inductance values the current ripple $\Delta I_{\text{rip}}$ is reduced by

$$\Delta I_{\text{rip}} \sim \frac{1}{N^2},$$  \hspace{1cm} (3.21)

where $N$ is the number of interleaved branches. This assumption is valid, if the stored magnetic energy in the inductors is kept constant. Then the inductance values of the interleaved branches increase proportional to $N$, reducing the ripple by factor $N$. With ideal interleaving and a phase shift $\Phi_k$

$$\Phi_k = \frac{k \cdot 2 \pi}{N}, \quad \text{for } k = 1, \ldots, N \hspace{1cm} (3.22)$$

the ripple is additionally reduced by factor $N$. Since the resulting ripple has a fundamental frequency of $N \cdot f_s$, the output capacitor ripple is proportional to

$$\Delta V_{\text{rip}} \sim \frac{1}{N^3}. \hspace{1cm} (3.23)$$
Interleaving including tolerances

In reality, the active bouncer output ripple is affected by jitter of the switches and component tolerances of the inductance values. To consider both effects, the current waveform of each interleaved branch is analyzed in the time domain. The resulting output current is obtained by summing up all branch currents $i_k$, which are calculated according to \[89\]

\[
 i_k(t) = \frac{V_1 (1-D)}{L_k} t - \frac{V_1 D (1-D)}{2 L_k f_s} , \quad 0 < t < \frac{D}{f_s} + t_{jit} \tag{3.24}
\]

\[
 -\frac{V_1 D (1-D)}{2 L_k f_s} t - \frac{V_1 D}{L_k} , \quad \frac{D}{f_s} + t_{jit} < t < \frac{1}{f_s} . \tag{3.25}
\]

$V_1$ is the input voltage, $f_s$ the switching frequency, $L_k$ inductance value of the $k$-th interleaved branch, $\Phi_k$ the corresponding phase shift and $t_{jit}$ is the switching jitter.

The inductance values are subjected to component tolerances $L \pm \Delta L$. The worst case occurs when all branches, in which the switching point occurs in the first half of the switching period, as depicted in Fig.3.23 a) for $D = 0.5$, have a value of $L + \Delta L$ and the other branches an inductance value of $L - \Delta L$. The resulting output current ripple in dependency on the duty cycle is displayed in Fig.3.23 b).

In order to reduce the ripple, the inductance values could be measured at start-up of the converter. The switching times can then be rearranged, so that branches with higher inductance value are followed by branches with lower inductance value, therefore reducing the ripple. In that case the highest ripple at switching frequency occurs when only one inductance value is too high while all other values are too low and therefore resorting while keeping the phase shift $\Phi_k$ for all branches equal is not affecting the output ripple. The resulting branch currents in this case and the output current ripple are depicted in Fig.3.23 c) and d).

Further means reducing the ripple are proposed in \[84\] and \[91\], but for worst case analysis only the simple resorting is considered.

### 3.6.5 Consideration of matrix pulse transformer

Since the proposed solid state modulator contains four active bouncers, it would be advantageous to additional interleave their voltage ripples.
This interleaving differs from the classical interleaving described in section 3.6.4 where the inductance values are proportional to the number of interleaved modules. Additionally, the branches are not directly interleaved, but coupled via the matrix transformer transfer function. The transfer function of the transformer is mainly influenced by its parasitics. Therefore, at first the transformer parasitics are calculated, then the circuit model of the matrix transformer is described. In a next step possible deviation in the transformer parasitics are considered and the transfer function for each bouncer module is derived.
Calculation of transformer parasitics

The considered matrix transformer is designed with the CLIC specifications with the fixed constraint of two cores and four primary windings according to the algorithm in [90]. The transformer parasitics, the leakage inductance and the distributed capacitance, where obtained by application of the charge simulation method (CSM) [92]. The resulting transformer geometry is depicted in Fig. 3.24. In order to define the transfer function of the matrix transformer in addition to the parasitics, the frequency dependency of the ohmic resistance has to be taken into account. The ohmic resistance of the primary and secondary windings were calculated taking skin and proximity losses into account for the geometry in Fig. 3.24 [67]. The primary winding is realized as foil conductors, the secondary windings as round conductors. The total resistance of the windings related to the primary side is displayed in Fig. 3.25. It was assumed in the calculation, that the connection of the transformer to the switching units outside the tank results in an additional length of \( l_{add} = 2 \text{ m} \). Further effects such as resistance of connectors are not considered, which would increase the
DROOP COMPENSATION SYSTEM

Fig. 3.25: Ohmic resistance of primary and secondary winding resistance referred to primary voltage level in dependency on the switching frequency.

Ohmic resistance further.

Electrical circuit model of matrix transformer

The proposed matrix transformer with four switching units and two cores, depicted in Fig. 3.19 can be considered as two transformers connected in series on the secondary side, since the primary flux of each core is added to the secondary flux. On each core there are two primary windings mounted, which corresponds to a parallel connection of fluxes. The resulting circuit model is depicted in Fig. 3.26. The primary side

<table>
<thead>
<tr>
<th>Table 3.9: Component values of pulse transformer</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R'_{load}$</td>
</tr>
<tr>
<td>$L'_{\sigma,1}$</td>
</tr>
<tr>
<td>$L'_{\sigma,2}$</td>
</tr>
<tr>
<td>$C'_{d,1}$</td>
</tr>
<tr>
<td>$C'_{d,2}$</td>
</tr>
<tr>
<td>$L_{gen,1}$</td>
</tr>
<tr>
<td>$L_{gen,2,3,4}$</td>
</tr>
</tbody>
</table>
Figure 3.26: Equivalent circuit diagram of a matrix pulse transformer referred to the primary voltage level. \( V_{rip,1} - V_{rip,4} \) represent a voltage ripple induced by the corresponding active bouncer.

is modeled as a voltage source with a ripple. Each pulse module with bouncer circuit has a parasitic inductance due to connection, which are assumed to be \( L_{gen,x} = 100 \text{ nH} \) for each connection. Since the magnetizing inductances of the cores are high compared to the leakage inductances, they are neglected. The distributed capacitances \( C_{d,1} \) and \( C_{d,2} \), the leakage inductances \( L_{\sigma,1} \) and \( L_{\sigma,2} \) are obtained from calculations according to [90]. In an ideal case all component values would be equal for each primary voltage source. In reality there also are tolerances due to variation in construction. It is assumed for worst a case analysis, that the parasitics of both cores have a ratio

\[
\frac{C_{d,1}}{C_{d,2}} = \frac{L_{\sigma,1}}{L_{\sigma,2}} = \frac{C + 20\%}{C - 20\%} = \frac{L + 20\%}{L - 20\%} = 1.5 : 1 \quad (3.27)
\]

In addition \( L_{gen,1} \) is assumed to be 10\% higher than the other parasitic inductances. The values are listed in Table 3.9. The resulting four transfer functions \( G_1(s) - G_4(s) \) are depicted in Fig. 3.27, which shows that \( G_3(s) \) and \( G_4(s) \) have a higher resonance frequency due to the assumed difference in stray components. All transfer functions are not
**Figure 3.27:** Transfer function bouncer voltage ripple to secondary voltage ripple of matrix transformer according to the circuit diagram in Fig. 3.26 with parameters of Tab. 3.9.

**Figure 3.28:** Transfer function bouncer current ripple to secondary voltage ripple considering the bouncer’s output capacitance $C_{b,\text{out}}$. Critically damped in their respective resonance frequency and therefore an unwanted ripple amplification could occur. By considering the entire transfer function of the system from bouncer current ripple to secondary voltage ripple as depicted in Fig. 3.28 the amplification at resonance frequency of the transformer is compensated by the attenuation of the bouncer’s output capacitance $C_{b,\text{out}}$. Therefore, the worst case scenario remains a current ripple at switching frequency in Fig. 3.23 c) as was previously described in section 3.6.4.
### 3.6.6 Ripple analysis

The ripple analysis is conducted for one duty cycle for the entire duty cycle range. The output voltage ripple is calculated in dependency on the number of interleaved branches per bouncer module and in dependency on the component tolerances. The four bouncer modules are interleaved via the matrix transformer with the component tolerances described in section 3.6.5. For worst case analysis one inductance value of a branch of the bouncer with lowest damping, which is the bouncer with the transfer function of $G_1(s)$, is to high by $\Delta L$ and all other inductances are too low by $\Delta L$.

In addition, jitter for the switches are considered. The jitter influences the voltage ripple, by changing the switching point of time and therefore the branch current. For worst case analysis, all switches, which are supposed to switch in the second half of the period (e.g. Fig. 3.23) are affected by the same jitter, therefore inducing a ripple at switching frequency. A jitter value of 5 ns is considered.

![Figure 3.29: Voltage ripple in dependency on number of modules and inductance variation with worst case assumption including switching jitters.](image-url)
Table 3.10: Optimization results inductance and system efficiency

<table>
<thead>
<tr>
<th>Inductance</th>
<th>4 x Metglas AMCC32</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N$</td>
<td>8</td>
</tr>
<tr>
<td>$d_{\text{turn}}$</td>
<td>5 mm</td>
</tr>
<tr>
<td>$W_a$</td>
<td>8.4 cm$^2$</td>
</tr>
<tr>
<td>$A_c$</td>
<td>6.4 cm$^2$</td>
</tr>
<tr>
<td>$d_{\text{airgap}}$</td>
<td>3.9 mm</td>
</tr>
<tr>
<td>$V_{\text{ind}}$</td>
<td>302.6 cm$^3$</td>
</tr>
<tr>
<td>$P_{\text{ind}}$</td>
<td>10.45 W</td>
</tr>
<tr>
<td>$P_{\text{ind,tot}}$</td>
<td>52.25 W</td>
</tr>
</tbody>
</table>

3.6.7 Efficiency analysis

The results are depicted in Fig. 3.29. In case of a deviation of ±15% in inductance value a number of 5 interleaved branches per module, corresponding to a 20-fold interleaving on system level, would be sufficient to stay below the requested voltage ripple of 0.75 V. In the following a bouncer module is analyzed with 5 interleaved branches for the voltage levels and switching frequencies defined in section 3.6.3.

At first, the inductors are optimized considering core losses and high frequency losses due to skin and proximity effect [67]. Due to a low duty cycle amorph cores are chosen. The core arrangement are E-cores with air gap. The results are displayed in Tab. 3.10. For the analysis of switching and conduction losses IGBT $IGW50N65H5$ and Diodes $IDW40E65D1$ of Infineon are used according to data sheet values. In order to ensure high system reliability the thermal cycling was limited to $\Delta T = 25^\circ$, resulting in parallel connection of five diode and five IGBT chips per bouncer branch as well as five chips for the short circuit switch, leading to a total of 30 IGBT chips and 25 diode chips. A section of the steady state thermal pulse cycle for all components is displayed in Fig. 3.30.

In Fig. 3.31 a) volume distribution for a single bouncer module is depicted. The heat sink volume $V_{\text{cooling}}$ is obtained according to [93] assuming a CSPI value of 5. The considered capacitances are $E53.R11$–$314T20$ from Electronicon. It shows that the bouncer input capacitances $V_{\text{Cin}}$ are dominant in volume, because they have to provide high current while avoiding a high voltage drop.
Without voltage drop compensation at system level, the main capacitor bank would require a capacitance of 44 mF instead of 4 mF to reach the FTS criteria of Tab.3.8, which would lead to an additional volume of 690 dm$^3$ considering just the volume of 126 units of 3 kV-capacitors $E51.S35-354R20$ from Electronicon. The total volume of all active bouncer modules is 52 dm$^3$, therefore the reduction in volume results to 638 dm$^3$.

The loss distribution is displayed in Fig.3.31 b). The dominant losses $P_{S,D}$ occur in the diodes and switches. One bouncer module has a conversion efficiency of $\eta = 91\%$. Because the bouncer modules transfer only 5\% of the entire pulse energy, the global efficiency (grid to klystron) is only reduced by 0.45\%.

### 3.6.8 Conclusion

A design procedure of an active bouncer for an long pulse modulator meeting the specification of CLIC is presented in this paper. The investigated system is based on a pulse transformer with four bouncer modules in series to the main capacitor bank (Fig.3.19). The active bouncer is a buck-boost topology with 5 interleaved branches per mod-
Figure 3.31: Distribution for a single bouncer module: a) Total volume consisting of heat sink $V_{cooling}$, input capacitor $V_{Cin}$, output capacitor $V_{Cout}$ and inductance volume $V_L$ b) Total power consisting of transferred power $P_{trans}$ and system losses in switches and diodes $P_{S,D}$, in inductances $P_L$ and losses in both input and output capacitances $P_{Cin,out}$.

ule, leading to a 20-fold interleaving via the pulse transformer on system level. With a switching frequency of 100 kHz during output pulse the secondary voltage ripple induced by the bouncer is below 0.75 V (5 ppm) at 15% component tolerances and switching jitters of 5 ns. The bouncer module efficiency was calculated to be 91%, lowering the system efficiency (grid to klystron) by 0.45%.

Acknowledgment

The authors would like to thank project the partners SNF (project number 144324) and CERN very much for their strong financial support of the research project.
3.7 Control of an active bouncer for an ultra precise $140 \, \mu s$-solid state modulator system

Sebastian Blume, Andreas Jehle, Yves Schmid and Juergen Biela
17th European Conference on Power Electronics and Applications (EPE’15 ECCE-Europe), Page(s): 1 - 11, September 2015
DOI: 10.1109/EPE.2015.7311737

Abstract

In pulse modulator systems, bouncers are used for droop compensation of the main capacitor voltage. In this paper, the control of an active bouncer in a pulse modulator is described and the charging via a main charging system is analyzed. Six interleaved bouncer modules are situated on the primary side in series to the main capacitor bank, forming together with a pulse switch the pulse unit. To reduce the system complexity, the pulse unit is recharged with a single charging source. The proposed methods are verified by converter measurements on a single bouncer module. Additionally, a repeatability analysis of the pulse unit is performed and dependencies on initial voltages and switching jitters are derived. It is shown that in case of an open loop control and a standard deviation of the initial main capacitor voltage of $\sigma_{V_{Main}(t=0)} = 15 \, \text{ppm}$ and the initial bouncer input voltage of $\sigma_{V_{Bin}(t=0)} = 75 \, \text{ppm}$ a pulse repeatability of $PPR < 100 \, \text{ppm}$ is achievable in 99.7% of the time.

3.7.1 Introduction

At the moment a new type of particle accelerator, the Compact Linear Collider (CLIC), is investigated at CERN. The modulator concept for providing a pulsed flat-top voltage to the klystrons of CLIC, consists of three stages. In the first stage a DC voltage of 750 V is produced from the low voltage grid by an active rectifier unit. The voltage is transformed to $V_{prim} = 2.4 - 3 \, \text{kV}$ by six interleaved boost converters and the energy is stored in a main capacitor bank. Four pulse units in parallel generate then the required pulse, which is converted to 150-180 kV by a pulse transformer.

In order to avoid overdimensioning the main capacitor bank, bouncer
Figure 3.32: Overview of the solid state modulator for CLIC. There are four identical pulse units on the primary side connected via a pulse transformer with two cores to the klystron load. Each pulse unit consists of a switching unit, supplied by a main capacitor bank in series with an active bouncer system. Each active bouncer system consists of six interleaved bouncer modules. The main capacitor bank and the bouncer system are charged with one charging system, consisting of an active rectifier unit and six interleaved boost converters, connected to the 400 V-AC grid. Additionally, specifications of CLIC are listed.
systems are applied in pulse modulators to compensate the main capacitor voltage droop. Passive bouncer systems have been proposed e.g. in [79], where an LC circuit is placed on the primary side and in [77], which proposed a LC bouncer on the secondary side. For long pulse modulators a lower LC-resonant frequency is required. Therefore, the passive components would be spacious and a switching jitter of the switch, which activates the LC bouncer resonance, would have large influence on the flat-top voltage. Therefore, for long pulses active bouncer systems based on power electronic converters are applied, which add a voltage in series to the main capacitor thereby allowing a more flexible voltage droop compensation. Additionally, they are able to adapt to different loads and can be used for pulse shaping [61]. Active bouncer systems in series to the main capacitor bank have been proposed e.g. in [61], which is based on an interleaved buck converter, and in [80], which considers a multilevel topology. The drawback of these solutions is that they have to cope with a 100 % change in load current within the required time to flat-top voltage (see Fig 3.32). Therefore, the basic concept of an interleaved buck-boost topology with short circuit switch has been proposed in [94], which is able to provide the required current rate of change. In this paper an active bouncer converter is realized based on the analysis of [94] and its control during the pulse intervals as well as the charging processes are presented.

One of the most challenging requirements of CLIC is the pulse to pulse repeatability, i.e. how similar two pulses are in their flat-top voltage. The specified modulator repeatability must remain below 100 ppm. General methods determining the repeatability have been investigated in [88] and [95]. In this paper the repeatability of a modulator subsystem is derived by combining jitter measurements with a circuit simulation, so that a sensitivity analysis of the influencing factors, which are switching jitters and initial voltage distributions, can be performed. First, in section 3.7.2 the initial precharge phase and the seven time intervals of the pulse phase of the active bouncer are explained and the required equations are derived. Then, the findings are validated by converter measurements in section 3.7.3. Thereafter, in section 3.7.4, a repeatability analysis is performed combining switching jitter measurements with a circuit simulation. This analysis is applied to a single pulse unit, consisting of six interleaved bouncer modules, a main capacitor bank and a switching unit, which reveals the impact of influencing
3.7.2 Bouncer control and charging process

The modulator system for CLIC is depicted in Fig. 3.32. There are four pulse units connected to a matrix transformer. Each pulse unit comprises six parallel connected bouncer modules in series to the main capacitor bank. In order to compensate the voltage droop in the main capacitor during the pulse interval, the bouncer modules increase their output voltage. Due to the series connection, the bouncer modules must provide the primary pulse current as well as a charging current for their output capacitors. To provide the required pulse current fast enough, this current is build up prior to the pulse interval in the bouncer module inductance [94]. In order to reduce the modulator system complexity, the bouncer modules are charged together with the main capacitor bank with one charging system. Therefore, the initial precharge phase, when all capacitors are discharged, and the pulse operation, both depicted in Fig 3.33, are investigated in this section.

Initial precharge phase

The initial precharge phase, which occurs at system startup when all capacitors are discharged, can be divided into three intervals: 1) capacitive voltage divider, 2) boost operation of the bouncer converter and 3) a pulse phase without contribution of the bouncer modules to the output pulse. In the following, these three intervals are explained.
Figure 3.34: (a) First interval of the initial precharge phase: capacitive voltage divider equivalent. (b) Second and third interval: energy transfer from $C_{b,out}$ to $C_{b,in}$ via a boost operation until $C_{main}$ reaches the system voltage $V_{sys}$. Subsequently an equivalent boost operation after a pulse without bouncer contribution and then an equivalent boost operation after a pulse without bouncer contribution. Subsequently an equivalent boost operation after a pulse without bouncer contribution and then an equivalent boost operation after a pulse without bouncer contribution.
Initial precharge phase: interval 1-capacitive voltage divider
The charging system charges the six bouncer modules in series with the main capacitor bank to the nominal system voltage $V_{sys}$ ($V_{sys} = V_{main} + V_{Bout}$). Each bouncer module has an input capacitance $C_{b,in}$ and an output capacitance of $C_{b,out}$.

During the first interval of the precharge phase (Fig. 3.34a), the bouncer branch input and output voltages $V_{Bin,1}$ and $V_{Bout,1}$ and the main capacitor voltage $V_{Main,1}$ can be described by a capacitive divider:

\[
V_{Bin,1} = V_{Bout,1} = V_{sys} \cdot \frac{C_m}{C_m + 6 \cdot (C_{b,in} + C_{b,out})}, \tag{3.28}
\]

\[
V_{Main,1} = V_{sys} \cdot \frac{6 \cdot (C_{b,in} + C_{b,out})}{C_m + 6 \cdot (C_{b,in} + C_{b,out})}. \tag{3.29}
\]

For the specifications given in Fig 3.11 this results in $V_{Main,1} = 2,159$ V and $V_{Bin,1} = V_{Bout,1} = 261$ V at the end of interval 1.

Initial precharge phase: interval 2-boost operation
In the second interval (Fig. 3.34b), each bouncer module actively transfers energy from $C_{b,out}$ to $C_{b,in}$, since it is operating as a boost converter. If the bouncer lowers its voltage at the same rate as the main capacitor voltage $V_{Main}$ rises, the system voltage remains constant and with assumed constant charging power $P_{charge}$ a constant charging current $I_{charge}$ results. The time required until $V_{Main}$ reaches the desired system voltage $V_{sys}$ and $V_{Bout} = 0$ is

\[
T_{charge} = \frac{(V_{sys} - V_{main,1}) \cdot C_m}{I_{charge}} = \frac{V_{Bout,1} \cdot C_m}{I_{charge}}. \tag{3.30}
\]

During this interval the energy $E_1$ stored in the six output capacitors $C_{b,out}$ after the first interval and additionally the energy $E_2$ obtained during $T_{charge}$ can be transferred to the six $C_{b,in}$. The energies result in

\[
E_1 = 0.5 \cdot 6 \cdot C_{b,out} \cdot V_{Bout,1}^2, \tag{3.31}
\]

\[
E_2 = I_{charge} \cdot T_{charge} \cdot \frac{V_{Bout,1}}{2} = 0.5 \cdot C_m \cdot V_{Bout,1}^2.
\]

With these two energies and the already stored energy in the six input capacitors $C_{b,in}$ after the first charging interval, the resulting bouncer
input voltage at the end of interval 2 is

\[ V_{\text{Bin, fin}} = V_{\text{sys}} \cdot \frac{C_m}{\sqrt{(C_m + 6 \cdot (C_{b, in} + C_{b, out})) \cdot 6 \cdot C_{b, in}}} \]  

(3.32)

With parameters of tab. 3.11 this results in a final bouncer module input voltage of \( V_{\text{Bin, fin}} = 281.1 \) V.

With a reduced input capacitance value of \( C_{b, in} = 1.15 \) mF a voltage of \( V_{\text{Bin, fin}} = 466 \) V could be achieved. But an adaption of the capacitance value is not flexible and it is critical to provide the required energies for different operating points as required for the CLIC prototype system (see Fig. 3.32). Therefore, a third interval can be used to charge \( C_{b, in} \), if the desired bouncer input voltage \( V_{\text{Bin, fin}} \) is not reached after the second interval.

**Initial precharge phase: interval 3-pulse phase without contribution of bouncer modules** Since the klystron load does not directly operate with HF-power after a system startup, there is a ramp up phase after a system start, where the system specifications such as the flat-top stability are uncritical.

During this ramp up phase, the bouncer modules do not have to provide energy to the load (\( V_{\text{Bout}} = 0 \) V). The main pulse current \( I_{\text{main}} \) is conducted via the antiparallel diodes of the short circuit switch \( S_{sc} \) and the main capacitor is discharged during the pulse. After the pulse

<table>
<thead>
<tr>
<th>Table 3.11: Bouncer module specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Turn ratio transformer</td>
</tr>
<tr>
<td>Nominal system voltage</td>
</tr>
<tr>
<td>Bouncer module input capacitance</td>
</tr>
<tr>
<td>Bouncer module output capacitance</td>
</tr>
<tr>
<td>Main capacitance</td>
</tr>
<tr>
<td>Bouncer inductance</td>
</tr>
<tr>
<td>Bouncer inductor current mean</td>
</tr>
<tr>
<td>Bouncer input voltage</td>
</tr>
<tr>
<td>Bouncer output voltage</td>
</tr>
<tr>
<td>Pulse duration</td>
</tr>
</tbody>
</table>
**Figure 3.35:** a) Pulse unit, which consists of six interleaved bouncer modules in series to a main capacitor bank and a pulse switch. Each bouncer module consists of a half bridge $S_{hs}$ and $S_{ls}$, an inductance $L_b$ and an additional short circuit switch $S_{cs}$. b) Bouncer module voltages and current during its continuous pulse operation, which can be divided into seven time intervals ($T_1...T_7$).
interval, during the recharging process, a boost operation is executed as described in the previous section. Consequently, the input voltage of the bouncer modules increases after each pulse until it reaches its set point value.

During the ramp up phase the klystron can be operated with a reduced pulse power. If 50\% of the nominal power is assumed, each diode must conduct a pulse current of $I_{main,D} = 41.66 \text{ A}$, since there are six bouncer modules with each six short circuit switches $S_{cs}$ in parallel. With the transient thermal resistance of the $IKW50N65F5$ \[96\], the junction temperature rise is $\Delta T_{j,c} = 26 ^\circ \text{C}$ during the pulse. In the pulse pause the junction temperature approximately approaches the ambient temperature again. Since the ramp up phase does only occur sporadically, the thermal cycling of the diodes is uncritical for the modulator life time. Once the input capacitances of the bouncer modules have reached their set point value, no further boost operation is executed and the short circuit switches $S_{sc}$ are closed. The main capacitor $C_{main}$ can then be charged to nominal system voltage of $V_{sys}$. Thereafter, the modulator system is ready for the regular pulse operation, which is described in the next section.

Pulse operation

Once both capacitances $C_m$ and $C_{b,in}$ have reached their nominal values, the modulator system is operational for its standard pulse operation. This operation is divided into seven time intervals ($T_1...T_7$), as depicted in Fig. [3.35b]), which will be explained with equations for a single bouncer module in the following.

Pulse phase: precharge interval ($T_1$) In order to provide the required current in the pulse interval, a current is build up in inductor $L_B$ by closing the high side $S_{hs}$ and the short circuit switch $S_{scs}$. Further details can be found in [94].

Pulse phase: wait for pulse interval ($T_2$) Since there are in each of the four pulse units six bouncer modules in parallel, tolerances of the inductance values have to be considered. In order to obtain similar module currents, each converter is equipped with an on board current measurement. When a bouncer branch current exceeds the set point value, its high side switch $S_{hs}$ is opened, which forces the inductor
current over the free wheeling path of $S_{scs}$ and $D_{ls}$ (see. Fig. 3.33). The current value only decreases slightly in this interval. If the precharge interval length $T_1$ is adapted to the highest inductor value, an almost ideal current sharing will be achieved. The inductor currents show an almost identical mean current value. The remaining difference in current due to different inductance values is the ripple amplitude, which is superimposed on the mean current value by the switching operation.

**Pulse phase: pulse interval ($T_3$)** During the pulse phase, the bouncer modules are interleaved, in order to induce only a small ripple on the flat-top voltage. The current is controlled by pulse width modulation in open loop control. The pulse width modulation is realized with precalculated duty cycle values. Since the output voltage is constantly changing, not the duty cycle value at the beginning of the switching period is selected, but the duty cycle value, which would be necessary at half the switching period. All bouncer modules have a fixed predefined phase shift of the switching period during the pulse interval, which ensures the required high interleaved switching frequency. Each bouncer module is equipped with an optical communication link, which allows to adapt the duty cycle values for every single pulse, if e.g. a load drift must be compensated.

By applying a control method without feedback loop the system repeatability is only dependent on the switching jitters and the initial voltage values as will be shown in section 3.7.4.

**Pulse phase: resonant interval ($T_4$)** After the pulse interval, the pulse switch $S_{Main}$ is closed. During the pulse the energy $E_{pulse}$ is transferred from the bouncer input capacitor to the load and to the output capacitance. Additionally, there is still energy $E_{ind}$ stored in the bouncer’s inductance $L_b$. This energy $E_l$ is also transferred to the output capacitance and results in a resonant interval. The bouncer input voltage at the beginning of the resonant interval $V_{Bin}(t = t_{res})$ is obtained by subtracting the entire transferred energy $E_{trans} = E_{pulse} + E_{ind}$ from the stored energy and can be approximated by

$$V_{Bin}(t = t_{res}) = V_{Bin}(t = 0) - \sqrt{\frac{2}{C_{b, out}} \cdot \left(0.5 \cdot L_b \cdot (I_b(t = t_{res}))^2 + \frac{I_m \cdot t_{pulse} \cdot V_{Bout,1}}{2}\right)},$$  \hspace{1cm} (3.33)
where \( t_{\text{pulse}} \) is the duration of the pulse interval, \( V_{\text{Bout},1} \) is the desired bouncer output voltage right after the pulse interval and \( I_b(t = t_{\text{res}}) \) is the inductor current at the end of the pulse interval. The energy in the inductor \( L_b \) is transferred to the output capacitance \( C_{b,\text{out}} \). The maximal output voltage can therefore be described by

\[
V_{\text{Bout,max}} = \sqrt{V_{\text{Bout},1}^2 + \frac{L_b}{C_{b,\text{out}}} \cdot \left( I_m - \frac{I_r(t = t_{\text{res}})}{2} \right)^2}. \tag{3.34}
\]

Since, the output voltage \( V_{\text{Bout}} \) is higher than the input voltage \( V_{\text{Bin}} \), after the energy of \( L_b \) has been transferred, the energy swings back via the inductance and the high side diodes \( D_{hs} \). This results in a final output voltage of

\[
V_{\text{Bout,fin}} = V_{\text{Bout,max}} - \left( V_{\text{Bout,max}} - V_{\text{Bin}}(t = t_{\text{res}}) \right) \cdot \left( \frac{2 \cdot C_{b,\text{in}}}{C_{b,\text{in}} + C_{b,\text{out}}} \right). \tag{3.35}
\]

after the resonant transition and a bouncer input voltage of

\[
V_{\text{Bin,fin}} = V_{\text{Bin}}(t = t_{\text{res}}) + \left( V_{\text{Bout,max}} - V_{\text{Bin}}(t = t_{\text{res}}) \right) \cdot \left( \frac{2 \cdot C_{b,\text{out}}}{C_{b,\text{in}} + C_{b,\text{out}}} \right). \tag{3.36}
\]

With values of table 3.11 the voltages are \( V_{\text{Bout,fin}} = 378.6 \text{ V} \), \( V_{\text{main,fin}} = 2139.7 \text{ V} \), \( V_{\text{sys,fin}} = 2516 \text{ V} \) and \( V_{\text{Bin,fin}} = 433.6 \text{ V} \) at the end of \( T_4 \).

\textbf{Pulse phase: interpulse recharging interval} \((T_5)\) \hspace{1cm} After the resonant interval, the system voltages have reached stable values. Now the charging source is activated and the recharging process is initialized. At first, the recharging process is considered without taking into account converter losses, to facilitate understanding. It is assumed, that the charging source charges with a constant current \( I_{\text{charge}} \) until a fixed voltage set point \( V_{\text{set}} = V_{\text{sys,nom}} \). The transferred energy of the bouncer’s input capacitor \( C_{b,\text{in}} \) can be divided into two parts. The energy \( E_1 \) transferred to the load and the energy \( E_2 \), which is still stored in \( C_{b,\text{out}} \). Via a boost operation the energy \( E_2 \) can be recuperated. The energy \( E_1 \) transferred to the load
from the bouncer’s input capacitance and the energy $E_m$ transferred to the load from the main capacitance $C_m$ are

\begin{equation}
E_1 = I_{\text{pulse}} \cdot t_{\text{pulse}} \cdot \frac{V_{\text{Bout},1}}{2},
\end{equation}

\begin{equation}
E_m = I_{\text{pulse}} \cdot t_{\text{pulse}} \cdot \left( V_{\text{sys}} - \frac{V_{\text{Bout},1}}{2} \right).
\end{equation}

where $I_{\text{pulse}}$ is the pulse current, $t_{\text{pulse}}$ the pulse duration, $V_{\text{sys}}$ the system voltage and $V_{\text{Bout},1}$ is the output capacitance voltage right after the pulse.

In the recharge process, the entire energy $E_m$, which was previously transferred to the load from the main capacitor, is recharged with the energy $E_r$ resulting in

\begin{equation}
E_r = I_{\text{charge}} \cdot t_{\text{charge}} \cdot \left( V_{\text{sys}} - \frac{V_{\text{Bout},1}}{2} \right) = E_m,
\end{equation}

which leads to

\begin{equation}
I_{\text{pulse}} \cdot t_{\text{pulse}} = I_{\text{charge}} \cdot t_{\text{charge}} = Q_r
\end{equation}

Since the bouncer is recharged by the same charging current due to the series connection by inserting (3.40) in (3.31) it becomes obvious, that the entire energy $E_1$ is also recharged. According to this ideal consideration all voltages reach their starting values after the recharging process.

If losses are taken into account it becomes obvious, that the bouncer input voltage $V_{\text{Bin}}$ decreases with each pulse cycle since the total converter losses are higher than the losses occurring in the main capacitor bank $C_m$. In order to provide the missing energy to the bouncer input capacitance $C_{b,in}$, the increased output voltage after the resonant interval must be exploited.

In this case, the increased bouncer output voltage $V_{\text{Bout,fin}}$ and thus an increased system voltage $V_{\text{sys,fin}}$, obtained in section 3.7.2 lead to a different recharging energy $E'_1$. If it is assumed that the bouncer output voltage is decreased at the same rate than the main capacitor voltage increases, $E'_1$ can be described by

\begin{equation}
E'_1 = E_1 + \Delta E = Q_r \cdot (V_{\text{Bout,fin}} - V_{\text{Bout},1}) + Q_r \cdot \left( \frac{V_{\text{Bout},1}}{2} \right)
\end{equation}

\begin{equation}
= V_{\text{Bout},1} \cdot C_{\text{Main}} \cdot \left( V_{\text{Bout,fin}} - \frac{V_{\text{Bout},1}}{2} \right).
\end{equation}
With this recharging energy $E'_1$, the stored energy in the output capacitor $E_2$ and the remaining energy in the input capacitor a maximal bouncer input voltage $V_{Bin,\text{recharge}}$ at the end of the recharging phase could be achieved according to

$$V_{Bin,\text{recharge}} = \sqrt{\frac{1}{C_{Bin}} (C_{Main} (2 \cdot V_{Bout,1} \cdot V_{Bout,\text{fin}} - V_{Bout,1}^2) + \frac{C_{b,\text{out}} \cdot V_{Bout,\text{fin}}^2 + C_{b,\text{in}} \cdot V_{Bin,\text{fin}}^2}{\ldots}}$$

resulting in $V_{Bin,\text{recharge}} = 457.5 \text{ V}$. Therefore, by exploiting the voltage sharing due to the resonance, the additional transferred energy $\Delta E$ can compensate the converter losses. This charging operation however, requires a charging source with adjustable voltage reference, since during most of the recharging interval, the voltage set point must be increased to $V_{sys,\text{fin}}$. In the end, however the main capacitance must only be recharged to $V_{sys,\text{nom}}$. Therefore, the next interval is required.

**Pulse phase: discharge interval** ($T_6$) In order to avoid overcharging the main capacitor bank, the output capacitor of the bouncer module is shorted, once the desired bouncer module input voltage $V_{Bin}$ is reached. Since the energy loss due to shortening of $C_{B,\text{out}}$ should be minimized, the increased system voltage $V_{sys,\text{fin}}$, is only applied for a certain percentage of the recharge interval, which is necessary to compensate all occurring losses. Then, the system voltage setpoint is reduced to $V_{sys,\text{nom}}$ and the bouncer output capacitor $C_{b,\text{out}}$ is discharged to the required value $V_{Bout} = V_{sys,\text{nom}} - V_{main}$. Thereafter, the recharge process is continued by discharging $V_{Bout}$ at the charging rate of $V_{Main}$. Once the output capacitance is shorted, the remaining $C_{main}$ is charged to its setpoint value.

**Pulse phase: wait for next pulse interval** ($T_7$) The charging source stops its operation, once the main capacitor voltage set point value is reached and sends a command to the pulse unit control, which starts the next precharging interval $T_1$.

### 3.7.3 Measurement results

For validating the findings of section 3.7.2 a bouncer module prototype was built with specifications according to tab.3.12. This prototype, depicted in Fig.3.35 a), is equipped with an input voltage, an output
Table 3.12: Parameters for testing and comparison between measured values (Fig.3.38) and calculations according to (6-9).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{sys,nom}$</td>
<td>400 V</td>
<td></td>
</tr>
<tr>
<td>$R_{load}$</td>
<td>0.8 $\Omega$</td>
<td></td>
</tr>
<tr>
<td>$I_{load}$</td>
<td>500 A</td>
<td></td>
</tr>
<tr>
<td>$C_{b,in}$</td>
<td>2 mF</td>
<td></td>
</tr>
<tr>
<td>$C_{b,out}$</td>
<td>67.3 $\mu F$</td>
<td></td>
</tr>
<tr>
<td>$C_m$</td>
<td>240 $\mu F$</td>
<td></td>
</tr>
<tr>
<td>$L_B$</td>
<td>24 $\mu H$</td>
<td></td>
</tr>
<tr>
<td>$R_{load}$</td>
<td>0.8 $\mu H$</td>
<td></td>
</tr>
<tr>
<td>$I_m$</td>
<td>625 A</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Calculated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{Bin}(t = 0)$</td>
<td>445 V</td>
<td>445.2 V</td>
</tr>
<tr>
<td>$V_{Bin}(t = t_{res})$</td>
<td>426.1 V</td>
<td>425.8 V</td>
</tr>
<tr>
<td>$V_{Bin,fin}$</td>
<td>428.5 V</td>
<td>427.5 V</td>
</tr>
<tr>
<td>$V_{Bout,1}$</td>
<td>265.1 V</td>
<td>265.8 V</td>
</tr>
<tr>
<td>$V_{Bout,max}$</td>
<td>460 V</td>
<td>454 V</td>
</tr>
<tr>
<td>$V_{Bout,fin}$</td>
<td>394 V</td>
<td>413.1 V</td>
</tr>
</tbody>
</table>

voltage and a current measurement connected via SPI to the control board. The current measurement principle is a current transformer with active reset circuit [97]. This method enables measuring high currents with a small core, since the current DC bias is reset during the pulse pause. In order to allow fast over-current turn off, the measured current is compared to a DAC reference value and in case of an over current the IGBTs are turned off.

At first, measurement results of the initial precharge phase are presented. Thereafter, single pulse operation is tested and the interpulse recharging interval is analyzed.

**Initial precharge phase**

The first and second interval of the initial precharge phase are investigated with a single bouncer module in series with a main capacitor bank of $C_{main} = 720 \mu F$ and a system voltage $V_{sys} = 1000 \text{ V}$, which
Figure 3.36: Interval 1 and 2 of initial precharge phase according to Fig. 3.34 showing high agreement to (3.32).

according to (3.32) leads to $V_{Bin, fin} = 305$ V. The result, depicted in Fig. 3.36, shows high agreement to the predicted voltage.

In order to verify the additional third interval of the precharge phase, measurements were conducted with a 50 Hz pulse operation with component values listed in tab.3.12. This test setup is also used for all following measurements. The charging process to $V_{Bin} = 450$ V is depicted in Fig. 3.37. The measurement also shows, that by applying pulse phases without contribution of the bouncer modules, any desired bouncer initial input voltage can be selected, as long as the number of cycles required does not exceed the ramp up phase of the klystron and neither the maximum reverse voltage of the switches nor the rated capacitor voltage is surpassed.

Pulse operation

In order to verify the correct operation of the bouncer, single pulse measurements were performed, covering the time intervals $T_1 - T_4$ (see Fig 3.35). In Fig 3.38 the waveforms are depicted. The measured val-
Figure 3.37: Interval 3 of initial precharge phase during the ramp up phase of the klystron in a 50 Hz operation. 80 cycles are required to reach the desired bouncer module initial input voltage of $V_{Bin} = 450$ V.

Values are compared to the calculated values according to (6-9). They show high agreement with slightly lower values due to parasitic resistance, but $V_{Bout, fin}$, which results in a higher voltage than predicted. In this case, the parasitic resistance results in less energy transmission in the resonant interval from the output capacitance to the input capacitance, which explains the higher measured value.

Interpulse recharging

In the final system, the pulse unit will be charged by a high bandwidth DC-DC converter. In order to test the recharging process in principal, a charging source with variable voltage set point was used, which has a much lower bandwidth then the charging source of the final system. The recharge operation is depicted in Fig 3.39. The bouncer input voltage $V_{Bin}$ starts at 441.7 V, the system voltage at $V_{sys} = 400$ V. After the pulse, the system voltage is increased to 500 V, while the bouncer input voltage was discharged to 420 V. During the recharge
process the bouncer output voltage decreases, transmitting energy to the input capacitance, while the system voltage of the series connection $V_{Bout} + V_{main}$ remains constant. Fig. 3.39 also indicates that after the recharging process with $V_{Bin} = 446.8$ V the initial bouncer input voltage is even exceeded.

**Continuous operation**

The converter was tested with a 50 Hz repetition rate at with testing conditions. The converter was operated continuously for 50 minutes at ambient temperature ($T_A = 30 ^\circ$C) with temperature curves of critical components depicted in Fig. 3.40. They indicate, that the maximal temperature occurs at the inductor with $T_{max} = 57 ^\circ$C, which is in an uncritical range.
Figure 3.39: Recharge operation of the bouncer module with the bouncer’s input voltage $V_{Bin}$, output voltage $V_{Bout}$, system voltage $V_{sys}$, and the inductor current $i_b$.

### 3.7.4 Repeatability

For particle accelerators it is crucial to produce a repeatable flat-top pulse to pulse voltage. Therefore, in this section a repeatability analysis is performed. At first the scope of the analysis is defined. Thereafter the required pulse to pulse repeatability is described. Subsequently, the applied procedure is presented. Finally, the influence of the single non-repeatable sources are derived and parameters for the investigated system repeatability are selected.

#### Scope of analysis

The block diagram of the entire modulator system is depicted in Fig. 3.32. It is assumed that passive components do not influence the system repeatability significantly. Therefore, only switched components are considered since due to their switching jitter they induce non repeatability into the system.
Since the charging system is not active during the pulse, it only affects the repeatability with the initial charging voltages. This effect can be taken into account by adding noise to the initial capacitor voltages of the system.

Since there are four identical pulse units connected in parallel via the transformer, the repeatability of only one subsystem is analyzed. The subsystem consists of six interleaved bouncer modules in series with a main capacitor bank and a switching unit (Fig.3.35a). In a controlled system without feedback loop the pulse to pulse repeatability only depends on the initial conditions and the switching jitters. Since all bouncer converters as well as the switching units are built equally it is a valid assumption that they all show equal jitter distributions.

**Required pulse repeatability**

The pulse repeatability requirement for CLIC is $PPR < 100$ ppm. In order to derive the $PPR$ of a modulator system, the standard deviation $\sigma_{tj}$ of the flat-top voltage must be computed at any given point in time of the pulse. The highest standard deviation from all time samples $\sigma_{tj,\text{max}}$ must be considered [95]. Thereafter, the $PPR$ can be derived in dependence of the tolerance interval $\alpha$.

$$PPR = \alpha \cdot \sigma_{tj,\text{max}}$$

In this paper $\alpha$ is chosen to $\alpha = 6 \rightarrow \pm 3\sigma$, so in 99.7% of the pulses the worst voltage spread at any given time of the pulse stays within the voltage band specified by the repeatability. With the flat-top voltage of
Figure 3.41: Measured signal delay between FPGA and collector emitter voltage (5V amplitude). Depicted is the falling edge with a mean of $\mu = 284.88\text{ ns}$ and a standard deviation $\sigma = 147.8\text{ ps}$ with a sample number of $N_{\text{sample}} = 50000$.

3 kV, which is the highest voltage of the operation range in Fig. 3.32, a $PPR < 100\text{ ppm} = 300\text{ mV}$ results and a $\sigma_{tj,max} < 50\text{ mV}$ must be achieved.

Repeatability analysis

The entire pulse to pulse repeatability of the pulse unit (Fig. 3.35a) depends on the initial voltage $V_{Bin}(t = 0)$ of the bouncer input capacitor, the initial main capacitor voltage $V_{Main}(t = 0)$ and the switching jitter of $S_{hs}$, $S_{cs}$ and $S_{main}$. The initial voltage of the bouncer output capacitor is not considered in this analysis, since it is shorted by $S_{cs}$ after the recharging process. Therefore, the voltage distribution will be small compared to the other charged voltages.

A circuit simulator is used to model the pulse unit. For simplification an ohmic load instead of a klystron is assumed. The switching jitter distributions were derived by converter measurements by analyzing the...
signal skew between the FPGA gate signal and the collector-emitter voltage with a 5 V amplitude. In order to be able to estimate the standard deviation for each measurement $N_{sample} = 50000$ were taken. The switching jitter values for the turn off skew of the high side switch is exemplary depicted in Fig.3.41.

The circuit simulator model is executed 2000-times. The pulse voltage fluctuation $\Delta u_{pulse}$ of the model is set to a voltage band of $\Delta u_{pulse} = 2$ V. For each run, the system voltages as well as the jitter of each switching operation are chosen from the normal distributions with specified standard deviations and the pulse voltage is sampled every 100 ns. The output voltage samples of all runs are then used to estimate a time dependent pulse distribution of $\sigma_{tj}$.

**Initial voltages**  To estimate the influence of the initial voltages $V_{Bin}(t = 0)$ and $V_{Main}(t = 0)$, the circuit simulation was applied with ideal conditions, but with a single voltage being subjected to varying initial conditions. The simulation was running with a fixed time step of 100 ns, since only the starting conditions were varied. In Fig.3.42 the estimated $\sigma_{tj}$ of the pulse voltage over the pulse length is displayed in dependency.

**Figure 3.42:** Influence of main capacitor starting voltage deviation $\sigma_{V_{Main}(t=0)}$ on pulse standard deviation.
on the main capacitor voltage standard deviation $\sigma_{V_{\text{Main}}(t=0)}$, which is varied between 10 ppm and 100 ppm. As can be expected, the standard deviation of the pulse at the beginning equals the main capacitor voltage deviation. During the pulse its value decreases slightly, since a higher initial voltage leads to a higher pulse current, which has a balancing effect. Since the circuit simulation is a linear transfer function, the linear transformation for normally distributed variable is applicable which is:

$$X \sim N(\mu, \sigma^2), Y = b + cX, c \neq 0 \Rightarrow Y \sim N(b + c \cdot \mu, c^2 \cdot \sigma^2)$$ (3.43)

This relation is also met in Fig 3.42, where the pulse voltage standard deviation scales linearly to the initial main capacitor voltage standard deviation.

The investigation of the initial bouncer input voltage distribution is conducted for two cases. In the first case, it is assumed that all bouncer input capacitors are charged together using a single precise voltage measurement. In the second case each bouncer module uses
its onboard voltage measurement to only charge its individual input capacitance. According to the arithmetic mean of independent normally distributed variants, which corresponds to the parallelization of bouncer modules,

$$\sigma_n^2 = \frac{1}{n^2} \sum_{i=1}^{n} \sigma_i^2 \quad (3.44)$$

it would be expected that the influence on the pulse standard deviation is reduced by $\sqrt{6}$, since there are six bouncer modules in parallel.

In Fig.3.43 the estimated $\sigma_{tj}$ of the pulse voltage over the pulse length is displayed for both invested cases for a initial input voltage standard deviation of 100 ppm, which corresponds to the previous assumption. Therefore, the onboard measurements could be by factor $\sqrt{6}$ less precise in charging accuracy than a single measurement. However, in the following analysis a precise voltage measurement for the six parallel bouncer modules is assumed to reduce system complexity.

With the bouncer input voltage distribution the maximum of $\sigma_{tj}$ occurs at a pulse length of 75 $\mu$s. That is the case, because a higher bouncer input voltage influences the pulse voltage indirectly (two energy storage elements, $L_b$ and $C_{Bout}$). Therefore, different voltage initial values begin to influence the pulse with a time delay. Here, a balancing effect can also be observed.

**Jitter of high side and short circuit switch** The circuit simulator runs with a fixed time step. In order to limit the error in the final distribution assumption to values smaller than 5% a step size was chosen of $t_{step} = 75$ ps, which is half the standard deviation of the smallest investigated jitter. Switching jitters for $S_{hs}$ and $S_{cs}$ were analyzed from $\sigma_{S_{hs}+S_{cs}} = 150$ ps to $\sigma_{S_{hs}+S_{cs}} = 1000$ ps with results depicted in Fig.3.44. They show, that the influence of the switching jitter increases until 100 $\mu$s, then it remains constant. The reason for that is that the voltage difference at the beginning of the pulse is small due to the limited number of so far occurred switching cycles. At a later point of the pulse, the voltage curves, due to more switching cycles, differ more leading to a higher standard deviation.

**Repeatability of pulse unit** The repeatability of an entire pulse unit ($pu$) is derived by assuming the parameters listed in tab. 3.13.
DROOP COMPENSATION SYSTEM

Figure 3.44: Influence of switching jitter $\sigma_{hs}$ combined with $\sigma_{cs}$ on pulse standard deviation.

Even though smaller jitter values were measured for $S_{hs}$ and $S_{sc}$ (Fig. 3.44) worst case values were assumed. The circuit simulator was applied with a fixed time step of 75 ps. Since the previous investigated influences are independent of each other, the standard deviation of the pulse unit can also be derived by combining the results according to

$$
\sigma_{tj,pu} = \sqrt{\sigma_{tj,Vbin(t=0)}^2 + \sigma_{tj,VMain(t=0)}^2 + \sigma_{tj,Shs+Scs}^2 + \sigma_{tj,Smain}^2}
$$

(3.45)

The time dependent standard deviation during the pulse is depicted in Fig. 3.45 together with the calculated standard deviation according to (3.45). They show high agreement with deviation smaller 1%. This deviation results due to the limited number of simulation runs. Together with the linear scaling of effects according to (3.43) for any linear combination of influences the standard deviation of the pulse voltage can be predicted.

With the selected parameters, the maximal standard deviation is $\sigma_{tj,max} = 49.1$ mV, which is below the derived requirement of section 3.7.4 and therefore a pulse to pulse repeatability $PPR < 100$ ppm of the pulse unit is achievable in 99.7% of the time. Beneficial for the system is,
that the different maxima of the investigated effects occur in different intervals of the pulse.

Table 3.13: Value List of assumed parameters for determining the standard deviation of the pulse unit.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$\mu$</th>
<th>$\sigma$</th>
<th>unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bouncer input voltage</td>
<td>450</td>
<td>0.0337</td>
<td>V</td>
</tr>
<tr>
<td>Main capacitor voltage</td>
<td>3000</td>
<td>0.045</td>
<td>V</td>
</tr>
<tr>
<td>$S_{hs, on}$ (worst case)</td>
<td></td>
<td>1</td>
<td>ns</td>
</tr>
<tr>
<td>$S_{hs, off}$ (worst case)</td>
<td></td>
<td>1</td>
<td>ns</td>
</tr>
<tr>
<td>$S_{cs, on}$ (worst case)</td>
<td></td>
<td>1</td>
<td>ns</td>
</tr>
<tr>
<td>$S_{cs, off}$ (worst case)</td>
<td></td>
<td>1</td>
<td>ns</td>
</tr>
<tr>
<td>$S_{main, on}$</td>
<td></td>
<td>1</td>
<td>ns</td>
</tr>
<tr>
<td>$N_{sample}$</td>
<td></td>
<td>2000</td>
<td></td>
</tr>
</tbody>
</table>
3.7.5 Conclusion

In this paper, the control and charging process of an active bouncer module for a pulse modulator system is investigated. In order to allow a combined charging with the main capacitor bank with a single source, the initial precharge phase, consisting of three phases is analyzed. Subsequently, the seven different time intervals of the pulse operation are evaluated and the relevant system voltages are derived. The operation of the converter during the pulse as well as during the charging intervals is then verified by measurements. Additionally, the pulse to pulse repeatability of an entire pulse unit, consisting of six interleaved bouncer modules, a main capacitor and a pulse switch is investigated. Switching jitters were obtained by measuring the signal skew of the FPGA signal and the collector-emitter voltage. The influence of initial voltages on the pulse repeatability is derived and a standard deviation of $\sigma_{V_{Main}(t=0)} = 45\, \text{mV}$ and $\sigma_{V_{Bin}(t=0)} = 33.7\, \text{mV}$ is selected. With these selected values and the assumed worst case jitter distribution of the switches with $\sigma_{\text{switches}} = 1\, \text{ns}$ a standard deviation of the pulse voltage during the flat-top can be achieved, which is below the required $\sigma_{tj,\text{max}} = 50\, \text{mV}$ thus ensuring in 99.7% of the pulses a repeatability of $PPR < 100\, \text{ppm}$.

Acknowledgments

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In this chapter, the pulse transformer and its corresponding optimization procedure is described.

In section 4.1, the impact of important design parameters on the efficiency of a pulse transformer is assessed, assuming simplified geometries. Thereafter, the pulse transformer optimization procedure is presented and all corresponding submodules are explained in detail in section 4.2. In section 4.6, the focus is set on the applied parasitics calculation of the procedure, validating it by comparison to 2D-FEM based analyses and a measured pulse of a modulator prototype. Furthermore, in section 4.7, the selected isolation distances of the pulse transformer are evaluated. A method is proposed, which validates the obtained isolation distances from the optimization procedure by analyzing the most critical electrical field path. The analysis compares the electrical field path to scaled high voltage breakdown data. Additionally, the sensitivity of the optimal transformer design on important system parameters such as core material, number of primary turns or klystron operating voltage are evaluated. In section 4.3, the final pulse transformer prototype for CLIC specifications is described, the analysis of the final design is conducted in section 4.4 and the corresponding pulse measurements are presented in section 4.5.
4.1 Qualitative assessment on pulse transformer efficiency

For CLIC the aim is to design a pulse transformer with high conversion efficiency. This aim can be best achieved by a short pulse rise time. As shown in section 1.3.1, the pulse rise time is determined by the transformer parasitics $L_\sigma$ and $C_d$. These parasitics are influenced by several parameters of the design process. Exemplary, in this paragraph, three design parameters are investigated, which are

- Transformer winding arrangement
- Primary voltage level of the transformer
- Number of secondary turns.

There exist various ways to arrange the transformer windings as well as numerous possibilities to choose the primary voltage level and vary the number of secondary turns. In order to provide an understanding of the impact of these three parameters on the transformer’s performance, their basic relations are derived from simplified geometries. Special emphasis is set on $L_\sigma$ in this analysis, since it is affected by all three investigated parameters. It is pointed out, that due to the simplified assumptions the analysis might not be comprehensive for the entire range of applications. However, it is intended to provide an intuition of the dependency on these parameters with the presented approximations. Based on this analysis, the chosen winding arrangement and the selected primary voltage level for the CLIC modulator is made plausible.

4.1.1 Winding arrangement

At first, the winding arrangement on a single magnetic core is investigated, followed by an analysis of the multi core arrangement selected in this project. The analysis is limited to single layer arrangements of the secondary winding, due to the high voltage application. This winding arrangement also features a simple construction and in offers in general a low $L_\sigma$. 

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Figure 4.1: Four different connection principles of a transformer with windings on both core legs: a) primary and secondary side in series, b) primary side in series and secondary side in parallel, c) primary side in parallel and secondary side in series and d) primary and secondary side in parallel.

Winding arrangement on single core

In pulse transformer design, U shaped cores are usually applied with two core legs. The cores differ from the standard M core shape, applied for distribution transformers, since they are not connected to the AC grid. If a pulse with low power rating is required, both windings can be mounted on a single transformer leg, thereby allowing a simple modulator structure. If a high power application is desired, both transformer legs can be equipped with windings, which will marginally increase the transformer’s volume. In this case, more components are required, but the current rating of a single winding as well as of the corresponding pulse switch can be reduced.

There are four basic winding configurations possible, which are depicted in Fig. 4.1 a)-d). In the configurations a) and b) the primary windings are connected in series. Since on the primary side the current typically is much higher than on the secondary side, the primary windings are mostly connected in parallel as displayed in c) and d). Thus, configu-
rations a) and b) are not considered further. In the following, c) and d) are compared to a winding arrangement with both windings on a single transformer leg:

In configuration c) the two secondary windings are connected in series, which allows to halve the original number of secondary turns $n_s$ to $n_s' = \frac{n_s}{2}$. Therefore, the core window height $h_c$ can be reduced to $h_c'$, which is defined by

$$h_c' = n_s' \cdot (d_s + d_w) + d_{iso} = \frac{n_s}{2} \cdot (d_s + d_w) + d_{iso}, \quad (4.1)$$

where $d_{iso}$ is the isolation distance of secondary winding to the magnetic core, $d_w$ the secondary turn diameter and $d_s$ the distance between two secondary turns. For single layer winding arrangements $n_s \cdot (d_s + d_w) \gg d_{iso}$ applies, which reduces the winding height to $h_c' = \frac{h_c}{2}$. Due to the core window height reduction also the core size is reduced, while the leakage inductance $L'_\sigma = L_\sigma$ remains constant. However, since the main goal is to reduce $L_\sigma$ to achieve a fast pulse rise time, the windings can also be distributed over the original winging height $h_c'' = h_c$. Then the resulting $L''_\sigma$ is reduced by factor of two $L''_\sigma = \frac{L_\sigma}{2}$.

In d) the secondary windings are connected in parallel. Since each winding corresponds to the winding arrangement on a single transformer leg, the mounting effort is doubled. Maintaining $L'_\sigma = L_\sigma$ constant, the number of secondary turns per secondary winding can be increased by factor $\sqrt{2}$, which reduces the core cross-sectional area $A_c$ by equal factor, since $L_\sigma \sim n_s^2; n_s \sim 1/A_c$.

Keeping the number of secondary turns per winding constant $n_s' = n_s$, $L''_\sigma$ is reduced by factor of two ($L''_\sigma = \frac{L_\sigma}{2}$) due to the parallelization of the two secondary windings.

For driving klystron loads, a unipolar voltage pulse is required, and therefore the windings can be adapted from a parallel to a cone shaped arrangement, with its profile depicted in Fig. 4.2 for configurations c) and d). Since in Fig. 4.2 (c) on one core leg only voltages up to half of the pulse voltage occur, the isolation distance on this transformer side can be reduced. This leads to two differently constructed secondary windings [98].

In case of Fig. 4.2 (d), an equal cone shape arrangement can be selected for both core legs.
Figure 4.2: Arrangement of the secondary windings in a cone shape for connection principle of Fig. 4.1 c) and d). In c) two different secondary windings must be arranged, whereas in d) both are equally constructed. In both cases the leakage flux area can be reduced by factor of two compared to a parallel winding arrangement. Furthermore, in d) one transformer side remains entirely on GND potential.

If the distance between primary and secondary winding is linearly increased with the occurring voltage difference, the area between the windings can be reduced by factor of two in both arrangements. Thus, in both cases $L''''$ is reduced by factor of two in comparison to a parallel winding arrangement with equal distance on both legs [46]. A drawback of this arrangement is the increased constructional effort of the windings.

An additional advantage of d) is, that there exists a transformer side with zero voltage potential on both core legs. This fact allows to construct a secondary winding, which has no supportive connection on the high voltage side, thereby avoiding an electric breakdown, due to creepage pathways on the surface of connecting solid materials.

Summing up the comparison equal reduction in leakage inductance can be achieved with both connection methods. Arrangement d) exhibits the following advantages over arrangement c):

▶ Secondary winding on both transformer legs can be equally constructed
Secondary winding is free-floating on the high voltage side. The following drawbacks occur:

- Higher constructional effort due to mounting of two secondary windings with \( n_s \) turns (number of mountable turns doubled)
- Higher constructional effort due to the free-floating winding arrangement.

This analysis shows, that for the pulse transformer design, both transformer legs should be utilized for the voltage conversion as well as the cone shape winding arrangement. In this configuration the leakage inductance can be reduced by factor of four in comparison to a single leg, parallel winding arrangement \( L''_\sigma = \frac{1}{4} \cdot L_\sigma \). Also, the primary windings should be connected in parallel. The secondary winding interconnection, however, can not in principle be favored to Fig. 4.1 c) or d) and depends on external constraints such as maximal winding height or secondary winding current.

In this project, the possibility of a free-floating high side potential was considered, to be worth the additional constructional effort, which is why arrangement d) with cone shape winding was selected for the following multi core arrangement.

Series and parallel connection of pulse transformers

As for CLIC a high output pulse power is required, multiple transformers can be connected in series or in parallel in order to reduce the power rating of the primary side components.

A favorable connection type is the matrix transformer, where the secondary winding encloses all cores (see Fig. 1.6). In this configuration a smaller product of leakage inductance \( L_\sigma \) and distributed capacitance \( C_d \) is obtained, which reduces the pulse rise time compared to series or parallel connected transformers. A comparison for different connection principles can be found in [46]. An intrinsic feature of the matrix transformer is that the number of secondary turns \( n_s \) is described by

\[
n_s = \frac{n_p \cdot n}{n_c}, \tag{4.2}
\]

where \( n \) is the voltage ratio of the transformer, \( n_p \) the number of primary turns and \( n_c \) the number of cores. Therefore, also a fractional
turns ratio can result, which is why this winding configuration is also known as fractional turn transformer. Such an arrangement is very valuable for an optimization procedure, since it allows to control the number of secondary turns with two parameters and is therefore more flexible for a matching of the transformer parasitics. Hence, a matrix transformer in arrangement Fig. 4.2 d) is chosen as basis for the optimization procedure detailed in section 4.2.

4.1.2 Primary voltage level

Another important design parameter is the primary voltage level $V_p$, as it determines the turns ratio $n$ of the transformer. In this paragraph, it is investigated, whether or not its variation influences the efficiency of the pulse transformer.
For this purpose, the impact of \( V_p \) on the transformer parasitics is analyzed, which are the distributed capacitance \( C_d \) and \( L_\sigma \). There exists the following relation between the parasitics and the pulse rise time \( t_r \) approximating the klystron load by a resistive element:

\[
t_r \sim \sqrt{L_\sigma \cdot C_d}.
\] (4.3)

The rise time in turn is related to the pulse efficiency, whereby a direct relation of \( V_p \) and the efficiency of the transformer is obtained.

In order to derive the basic relation between \( V_p \) and the pulse rise time, a simplified winding arrangement in the two-dimensional space is assumed, which is depicted in Fig. 4.3. A single primary and a secondary winding are displayed inside the core window. \( n_s \) is assumed to be constant. With \( n_s = const \) also the assumption of \( A_c = const \) is justified (\( A_c \sim 1/n_s \)), which leads to equal construction of the secondary winding for the entire primary voltage level range. To further simplify the analysis, it is assumed, that in the transformer the electrical field between the windings is homogeneous. In this case, the required isolation distance \( d_{iso} \) between two potentials \( V_1 \) and \( V_2 \) for a maximal allowed electrical field \( E_{max} \) is obtained by:

\[
d_{iso} = \frac{V_1 - V_2}{E_{max}} = \frac{\Delta V}{E_{max}}.
\] (4.4)

Applying (4.4) to the capacitance \( C \) of a plate capacitor, results in the following relation:

\[
C = \epsilon_0 \epsilon_r \frac{A \cdot E_{max}}{\Delta V} \sim \frac{1}{\Delta V}.
\] (4.5)

In order to derive the relation between \( V_p \) and the distributed capacitance \( C_d \), the electrical \( E_{elec} \) energy comprised in a geometry can be investigated, since \( C_d \sim E_{elec} \). Considering the arrangement depicted in Fig. 4.3 the entire electrical energy \( E'_{elec} \) in the two dimensional space can be simplified to an arrangement of plate capacitors. Neglecting boundary electrical fields \( E'_{elec} \) results in

\[
E'_{elec} = 0.5 \cdot (C_{ps} \cdot (V_s - V_p)^2 + C_{sc} \cdot (V_s - V_c)^2 + C_{pc} \cdot (V_p - V_c)^2)
\] (4.6)
where $V_p$ and $V_s$ are the primary and secondary voltage levels; $V_c$ is the voltage of the core, which is set to $V_c = 0$. $C_{ps}$, $C_{cs}$ and $C_{pc}$ are the equivalent capacitances for all turns of the respective winding. Since the secondary voltage level is fixed, it can be described by $V_s = n \cdot V_p$. To obtain a homogeneous electrical field, the distance between both windings $d_{ps}$ relates to the distance between core and primary winding $d_{pc}$ by $d_{ps} = (n - 1) \cdot d_{pc}$.

In the next step, the impact of an increase of $V_p$ by factor $k$ can be analyzed with $V'_p = k \cdot V_p$. In order to keep the maximal electrical field $E_{max}$ in the design constant, $d_{pc}$ is increased to $d'_{pc} = k \cdot d_{pc}$, thereby decreasing $d_{ps}$ to $d'_{ps} = (n - k) \cdot d_{pc}$. In this case the capacitance $C_{ps}$ changes to $C'_{ps} = 1/(n - k) \cdot C_{ps}$ and $C_{pc}$ results to $C'_{pc} = 1/k \cdot C_{pc}$. (4.6) can then be rewritten as

$$E'_{elec} = 0.5 \cdot \left( \frac{C_{pc}}{(n - k)} \cdot (n - k)^2 \cdot V_p^2 + C_{sc} \cdot (V_s)^2 + \frac{C_{pc}}{k} \cdot (k)^2 \cdot V_p^2 \right)$$

$$= 0.5 \cdot \left( C_{pc} \cdot n \cdot V_p^2 + C_{sc} \cdot (V_s)^2 \right)$$

We can observe, that $E'_{elec}$ is independent on the primary voltage level increase of factor $k$. Therefore, for the entire primary voltage level range, equal electric energy is comprised in the arrangement and thus $C_d$ remains constant.

In a parallel winding arrangement the assumption of a homogeneous electrical field is not given, since the pulse transformer is grounded at one end. By selecting a cone shape winding, as applied in this project, a homogeneous electrical field $E_{hom}$ between the windings is obtained. The relation is displayed in Fig. 4.4. The electrical field in the area between the secondary windings can be neglected.

The electric field between primary and secondary winding will remain constant, if the opening the angle of the primary winding $\alpha$ is adapted to the increased primary voltage level. Also, the electric field $E_s$ between top of the secondary windings and core remains equal. The only change is the electric field $E_p$ caused by the top of the primary winding towards the core. Since the isolation distance to the core is determined by the secondary voltage level, in most cases $E_p$ can be neglected. Therefore, the assumption of a distributed capacitance $C_d$ independent of the selected primary voltage level is valid.
Figure 4.4: Simplified electrical field distribution for a transformer with cone shape winding arrangement. The electrical field between the windings and the core is homogeneous at the sides. For variations in the primary voltage level $E_{hom}$ will remain constant, if the angle of the primary winding $\alpha$ is adapted accordingly. At the high voltage side of the windings, the electrical field is inhomogeneous and mainly determined by the secondary voltage potential, leading to $E_s$. In the area between the two secondary windings the electrical field can be neglected.

The simplified geometry, depicted in Fig. 4.3 can also be applied for analyzing the impact of a change in $V_p$ on $L_\sigma$. The following relation applies

$$n_p \sim V_p; I_p \sim \frac{1}{V_p} \Rightarrow n_p \cdot I_p = const,$$

which fixes the area in the core window covered by the primary winding, assuming constant current density. A single layer arrangement of
both windings with equal winding height is assumed, covering most of the core window height.

In this case it can be approximated, that the entire magnetic leakage flux $\Phi_\sigma$ is concentrated in the area between primary and secondary winding. If the primary winding is moved closer to the secondary winding, $\Phi_\sigma$ is decreased linearly and with it also $L_\sigma$. The magnetic flux lines in the area between core and primary winding, mostly close around both windings, thereby contributing to the main flux $\Phi_m$. The leakage inductance $L_{\sigma,k}$ of a $k$-fold increased primary voltage therefore relates to the reference leakage inductance $L_{\sigma,1}$:

$$L_{\sigma,k} = \frac{(n-k)}{(n-1)} L_{\sigma,1}. \quad (4.8)$$

With (4.43) in section 4.1.2 the dependency of the pulse rise time $t_r(k)$ on increase of the primary voltage level $V_p$ by factor of $k$ can be described by

$$t_r(k) \sim \sqrt{\frac{(n-k)}{(n-1)}}. \quad (4.9)$$

If we assume a primary voltage level of $V_p = 3 \text{kV}$ for CLIC, then the turns ratio $n$ results to $n = 60$. With a voltage increase by factor of $k = 5$ ($V'_p = 15 \text{kV}$), the rise time marginally reduces by 3.5% compared to the one of the originally selected $V_p$.

In real pulse transformer design additional effects such as insulation material, applied transformer oil, field shape rings or inhomogeneous electrical fields must be considered, which exert considerably higher influence on the pulse performance than the variation in primary voltage level. Therefore, in the authors opinion, the influence of the primary voltage level on the pulse transformer’s efficiency can be neglected.

On the overall modulator design, however, the primary voltage level, exerts a significant influence:

The higher the voltage level, the higher is the isolation requirement of the pulse switches, which requires a series connection of devices. As already mentioned in section 1.2.2 a series connection of devices, complicates the modulator structure and therefore is not advisable.

The selection of primary voltage level is therefore driven by the availability of highly reliable, high power switches with a sufficient voltage blocking capability, which can be applied for pulsed operation.
The primary voltage level chosen in this project is made plausible in the following:

The modulator specifications demand a connection to the 400 V AC grid. Since an active rectifier stage is applied, the smallest achievable DC link voltage is 560 V. In order to operate in an active controlled mode with power factor correction, a DC link voltage level of at least 620 V is required. Nominal output power of an active rectifier stage is obtained at a DC link voltage level of 750 V. As the repeatability requirement for CLIC is demanding, a precise capacitor charging unit is required. Due to the high pulse voltage, a step up converter is preferable in comparison to a step down converter. In order to efficiently transfer the required charging power, soft switching techniques such as the boundary conduction mode (BCM) must be applied for the step up converter. BCM requires an output voltage, which is more than factor two higher than the input voltage. Thus, the primary input voltage must be selected to $V_p > 1.5 \text{kV}$.

Suitable for the pulse switches are press pack IGBTs from traction applications, which offer a high reliability. To reach the blocking voltage capability, single IGBT dies are applied, thereby avoiding a series connection of semiconductors. Since the press pack IGBTs are designed for high power applications, they can also easily cope with the high primary pulse current. Available devices feature voltage levels of 6.5 kV, 4.5 kV and 2.5 kV, which allow a corresponding primary voltage level for the modulator of 4.5 kV, 3 kV and 1.5 kV. Since the devices with lower blocking voltage offer a faster turn on time, the primary voltage level for this application is selected to 3 kV and the 5SNA1250B450300 IGBT from ABB is chosen.

### 4.1.3 Secondary number of turns

The specified CLIC output voltage-time product leads to a large core cross-sectional area $A_c$. In order to reduce $A_c$ the number of secondary turns $n_s$ can be increased ($A_c \sim 1/n_s$). The increase in $n_s$ influences the transformer parasitics ($C_d$ and $L_{\sigma}$) and the pulse rise, which in turn relates to the efficiency of the transformer as derived in the previous paragraph. Therefore, the impact of $n_s$ on the pulse rise time $t_r$ is evaluated in this paragraph with a simplified 2D geometry, depicted in Fig. 4.5.
Figure 4.5: Top view of a winding arrangement of a transformer half. The core cross-sectional area is quadratic with length $a$. $d_{iso}$ determines the isolation distance of the secondary winding to tank and the core leg. $l_{av, ind}$ describes the mean length of related to the leakage inductance $L_\sigma$ and $l_{av, cap}$ the mean length of the area related to the distributed capacitance $C_d$.

$L_\sigma$ increases with the square of $n_s$ and linearly with the stray flux area $A_\sigma$ ($L_\sigma \sim A_\sigma \cdot n_s^2$). Due to the 2D geometry analysis, the dependency on height is neglected. This assumption will be valid, if the winding height $h_c$ is set equal for all variations of $n_s$. The leakage flux $\Phi_\sigma$ is estimated to only occur in the area between primary and secondary winding. By increasing $n_s$, $L_\sigma$ will increase quadratically, but since $A_c$ decreases ($A_c \sim 1/n_s$), also the stray flux area $A_\sigma$ decreases. Assuming a quadratic cross-sectional area $A_c = a^2$, then the relationship $a \sim 1/\sqrt{n_s}$ results. The dependency of the leakage inductance is then obtained by

$$L_\sigma \sim n_s^2 \cdot 4 \cdot (a + d_{iso}) \sim n_s^2 \cdot 4 \cdot \left( \frac{1}{\sqrt{n_s}} + d_{iso} \right),$$

(4.10)
where $d_{iso}$ is the isolation distance.

In the simplified geometry, a homogeneous electrical field distribution in all four directions is assumed. This approximation will hold, if the secondary winding has equal distance to the tank walls and to the second core leg. Since in this case the center of the electric energy is the secondary winding itself, the relation of distributed capacitance $C_d$ and $n_s$ is defined by

$$C_d \sim 4 \cdot (a + 2 \cdot d_{iso}) \sim 4 \cdot \left( \frac{1}{\sqrt{n_s}} + 2 \cdot d_{iso} \right). \quad (4.11)$$

Inserting (4.10) and (4.11) in (4.43) and neglecting $d_{iso}$ for $a >> d_{iso}$, results in

$$t_r \sim \sqrt{n_s}. \quad (4.12)$$

The more secondary turns are applied, the smaller $a$ results and at a certain point $d_{iso}$ must be considered.

In the extreme case of $a << d_{iso}$, $t_r \sim n_s$ results. So for the entire geometry range the rise time $t_{r,2}$ for a given secondary turn number of $n_{s,2}$, can be related to a reference design with $n_{s,1}$ and rise time $t_{r,1}$ by

$$\sqrt{\frac{n_{s,2}}{n_{s,1}}} \cdot t_{r,1} \leq t_{r,2} \leq \frac{n_{s,2}}{n_{s,1}} \cdot t_{r,1}. \quad (4.13)$$

In a real transformer design, other effect such as the klystron load, the selected winding arrangement, and inhomogeneous field distributions exert influence on the rise time. However, the provided analysis offers a first, helpful approximation of the relation between the pulse rise time and the secondary number of turns. A more detailed analysis of the pulse rise time is outlined in section 4.2.4.

With a higher number of secondary turns, the core and thereby the transformer volume decrease, but also the pulse efficiency declines, which is a dominant factor in the loss share of the pulse transformer. Hence, a sophisticated balancing of the two parameters (transformer efficiency and volume) is crucial, which can best be analyzed by an optimisation procedure.

Therefore, in the next section an optimization procedure for pulse transformers is presented.
4.2 Pulse transformer optimization procedure

As previously derived in section 1.3 a modulator concept based on a matrix transformer is selected for CLIC.

Solid state modulators with matrix transformers have been investigated prior to this work [47, 50]. However, these previous works focused on meeting the pulse requirements by precalculating the transformer parasitics. The parasitics were obtained by 2D-FEM or by simplified analytical calculations. The applied analytical calculations, however, are not suitable for arbitrary winding geometries.

The challenge for the CLIC modulator system is not only to design a transformer with high conversion efficiency, but also to operate the system in a broad load range (see Tab. 1.1). These demands necessitate the application of an optimization procedure. Thus, in this thesis, a global approach optimizing the pulse shape and transformer volume for an arbitrary winding geometry is proposed. This optimization procedure is able to deliver an optimal transformer design for a given volume and predicts the pulse behavior for the desired operating pulse range.

Table 4.1: Application driven user input data. There exist three categories: 1) current and voltage levels, 2) pulse shaping parameters and 3) the peak value of the electrical field to derive the isolation distances.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse voltage maximum</td>
<td>$V_{\text{pulse, max}}$</td>
</tr>
<tr>
<td>Pulse current maximum</td>
<td>$I_{\text{pulse, max}}$</td>
</tr>
<tr>
<td>Desired pulse voltage</td>
<td>$V_{\text{pulse, opt}}$</td>
</tr>
<tr>
<td>Desired pulse current</td>
<td>$I_{\text{pulse, opt}}$</td>
</tr>
<tr>
<td>Primary voltage level</td>
<td>$V_{\text{prim}}$</td>
</tr>
<tr>
<td>Flat-top length</td>
<td>$t_{\text{flat}}$</td>
</tr>
<tr>
<td>Maximal rise time</td>
<td>$t_{\text{r}}$</td>
</tr>
<tr>
<td>Maximal time to flattop</td>
<td>$t_{\text{settle}}$</td>
</tr>
<tr>
<td>Maximal overshoot</td>
<td>$os$</td>
</tr>
<tr>
<td>Desired Flattop stability</td>
<td>$FTS$</td>
</tr>
<tr>
<td>Magnetization time</td>
<td>$t_{\text{pre}}$</td>
</tr>
<tr>
<td>Maximal electrical peak field</td>
<td>$E_{\text{max}}$</td>
</tr>
</tbody>
</table>


Optimization procedures provide four major advantages to the designer:

▶ They deliver an optimal design for a given set of constraints, and therefore can cope with varying specifications.
▶ The designer can also vary constraints, such as volume, and obtain for every point an optimal design resulting in a pareto front.
▶ They offer the possibly to investigate the sensitivity of the optimal design on variations in parameters such as isolation distance, transformer oil or magnetic core material.
▶ The designer can evaluate a fixed optimal design on variations of external parameters e.g. load range as desired in the case of CLIC.

There are several requirements which were taken into account designing the optimization procedure for a pulse transformer:

▶ An optimization cycle should not exceed a certain time limit in order to perform investigations in a reasonable time frame
▶ The procedure should be applicable to a broad range of transformer geometries and pulse applications
▶ The procedure must be flexible in all important parameters of high voltage pulse transformer design

In order to fulfill the first requirement and to allow a reasonable overall computing time, the optimization cycle was limited to a few seconds. This constraint requires the usage of analytical approximations to derive important parameters such as the transformer parasitics or the electrical peak field occurring in the design. Analytical approximations for transformer parasitics were conducted in [46], but they are not applicable for arbitrary geometries. The chosen approach in this thesis is based on the charge mirroring method (CSM) and is described in section 4.2.2. The application of the CSM enables the procedure to cope with a broad range of winding arrangements.

In order to allow a broad range of applications, parameters in three different categories can be chosen, which exert the most influence on the design and are listed in \textbf{tab. 4.1}. In the first category, not only the desired current and voltage level, which should be optimized, can
be set but also the maximal values of the operating range. The second category consists of the pulse shaping parameters, which are application driven. Additionally, in order to define the isolation distances of the design, the desired maximum value of the electrical field can be selected. This peak value is either known prior to the optimization by the designer, or it can be obtained in an iterative process by checking of the isolation distances as described in section 4.7.3. Additionally, to allow a higher flexibility in the design process, a choice of three different core materials and two transformer oils is provided.

The procedure incorporates eight optimization variables, listed in Table 4.2. Due to the matrix transformer approach, where the secondary winding encloses several cores, besides the number of primary turns $n_p$, also the number of cores $n_c$ is a degree of freedom (see (4.2)). With selection of $n_p$ and $n_c$ the number of secondary turns $n_s$ results, which leads to a minimal secondary winding height $h_{s,min}$. There exist three additional parameters defining the arrangement of the secondary winding, which are the additional winding height $h_{s,add}$, the distance to primary winding or to the core on its high voltage side $d_{w,hs}$ and the distances on its low voltage side $d_{w,ls}$. The two different distances are distinguished since a unipolar pulse excitation, which is common for pulse applications, allows a cone shaped winding arrangement. If desired by the designer, also a parallel winding arrangement can be selected. A single layer secondary winding arrangement is assumed as default. If required, also an arbitrary winding geometry can be investigated by providing the 2D-position of each turn including the corresponding voltage potential and conductor current. The secondary turn

<table>
<thead>
<tr>
<th></th>
<th>( n_p )</th>
<th>( n_c )</th>
<th>( h_{s,add} )</th>
<th>( d_{w,hs} )</th>
<th>( d_{w,ls} )</th>
<th>( r_r )</th>
<th>( w_{Ac} )</th>
<th>( B_{ap} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of primary turns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of cores</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Additional secondary winding height</td>
<td></td>
<td></td>
<td>( h_{s,add} )</td>
<td>( mm )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Winding distance on high voltage side</td>
<td></td>
<td></td>
<td>( d_{w,hs} )</td>
<td>( mm )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Winding distance on low voltage side</td>
<td></td>
<td></td>
<td>( d_{w,ls} )</td>
<td>( mm )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Field shape ring radius</td>
<td>( r_r )</td>
<td>( mm )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Width of single core leg</td>
<td>( w_{Ac} )</td>
<td>( mm )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Applied limit of flux density</td>
<td>( B_{ap} )</td>
<td>( T )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
with the highest voltage potential is foreseen as electrical field shaping ring. Since the electrical field shaping has an influence on the electrical field distribution and therefore on the transformer parasitics, the field shape ring radius $r_r$ also is an optimization parameter. Finally, two parameters related to the magnetic core influence the design: $w_{Ac}$ describes the width of single core leg and shapes the core geometry, whereas the applied flux density limit $B_{ap}$ defines the utilization rate of the magnetic core.

A schematic overview of the optimization procedure is given in Fig. 4.6. The global optimizer receives two parameter sets, which are the application driven user input data (see tab. 4.1) and a fixed material parameter set (e.g., relative permittivity of transformer oil). Additionally, the transformer volume can be constrained. With the optimization variables of tab. 4.2 the transformer geometry is created in the geometry submodule, respecting the volume specification. The electrical field distribution of the resulting geometry is then checked by determining the peak value of the electrical field, which must remain below the user threshold. If this threshold is exceeded, the optimizer will abort calculations and choose a new variable set; otherwise the pulse shape submodule will supervise if the pulse constraints can be met. If constraints are met, pulse losses will be calculated and all other submodules will derive their corresponding losses. As the total transformer losses are the procedure’s objective, the minimal losses under volume, electrical and pulse constraints are obtained.

In a post optimization process the electrical design is verified, by checking of the isolation distances (see section 4.7.3). If the most critical electrical field path of the design is below the field path for a certain breakdown probability (breakdown probability is a user input), a valid pulse transformer design is obtained.

In the following sections, the submodules of the optimization procedure are described according to the structure given in Fig. 4.6. It has to be noted, that the applied optimization procedure is limited to a modulator concept with a pulse transformer. No other concepts are taken into account, e.g., resonant converters or converters based on the Marx structure, which might for certain system requirements be more beneficial. Additionally, the models have only been validated in two different real size pulse transformers. Therefore, in order to avoid data extrapolation, the procedure is limited to flat-top pulse lengths in the range of $3 \text{us} \leq t_{flat} \leq 140 \text{us}$.
Figure 4.6: Optimization procedure structure with integrated submodules. The procedure minimizes the losses of a pulse transformer respecting volume, electrical and pulse constraints. Additionally, the obtained design is validated with a post-optimization process.
Figure 4.7: Simplified electrical circuit diagram. The two pulse modules of each core are connected in parallel. All \( n \) cores are electrically connected in series. The two secondary windings enclosing all cores show a parallel connection. Stray components of the transformer are neglected in this representation.

The geometry of the pulse transformer is derived from the eight optimization variables, presented in the previous paragraph.
The winding arrangement was defined in section 4.1.1 to a parallel connection on both transformer sides and is applied for the matrix transformer concept, visualized in Fig. 1.6. Since the secondary winding encloses several magnetic cores the flux $\Phi$ of each core is added, which represents a series connection of the primary pulse modules on different cores. Neglecting differences in stray components, the two primary pulse modules on the same core generate equal flux and their magnetomotive forces $\Theta$ add up, which can be represented by an electric parallel connection. A simplified electrical circuit diagram of the matrix transformer concept is depicted in Fig. 4.7.

The cross-sectional area of each single magnetic core can be defined by

$$A_c = \frac{v_{\text{max}} (t_{\text{flat}} + t_{\text{add}})}{2 B_{\text{ap}} n_p FF},$$

(4.14)

where $FF$ is the filling factor of the cut tape-wound core, $t_{\text{flat}}$ the flat-top length of the pulse, $t_{\text{add}}$ the considered additional pulse length due

![Diagram of pulse transformer](image)

**Figure 4.8:** Geometric setup of the transformer: a) Geometric variables in the core window. b) Geometric variables between core and tank wall including cooling pipes. [94]
to rise and fall time, $B_{ap}$ the selected flux density of the procedure. Since the CLIC modulator must operate in a broad load range (see tab. 1.1), the cross-sectional area is derived for the maximal specified voltage $v_{max}$. Due to an active reset circuit, the flux swing $B_{ap}$ can be doubled compared to unipolar excitation (see section 4.2.6).

The opening angle of the cone is defined by the distances to the primary winding, given by the optimization variables $d_{w,hs}$ and $d_{w,ls}$ (see tab. 4.2) and the secondary winding height $h_s$. On top of each secondary winding an electrical field shaping ring is situated with radius $r_r$. On the low voltage side of the winding, which is situated at the top end, the magnetic cores are attached to the tank cover. All required feedthroughs are also connected to this cover. This arrangement simplifies the maintenance of the transformer, since the tank cover with the attached cores can simply be lifted from the tank without removing any connections. In order to attach the cores to the tank cover a steal bar is required, which results in a spacing between the cores of $d_{cores}$.

The area outside the core is equally structured as the core window, except that the distance between field shape ring and oil tank wall is enlarged by $d_{add}$, leading to smaller capacitance values of the transformer, lower breakdown probabilities of the entire design, but to higher tank volume.

All further geometry relations are described in tab. 4.4 with the related parameters listed in tab. 4.3. Additionally, a visualization is given in Fig. 4.8.

**Pulse transformer cooling concept**

The pulse transformer cooling concept is realized by grounded cooling pipes inside the tank. Since the positioning of these pipes is relevant, as they contribute to the distributed capacitance of the transformer, they are considered in the electric field calculations. To minimize their influence, they are positioned at the low voltage side of the windings, which is in the chosen arrangement above the winding. The cooling pipes of the prototype are positioned in the middle between beginning of the winding and minimum oil level, where the heated oil from the high voltage side of the winding flows due to convection.
Table 4.3: Geometry variables which define the transformer shape. \textit{calc} indicates, that these parameters are derived from other parameters. \textit{param} indicates, that it is a material selective value.

<table>
<thead>
<tr>
<th>Description</th>
<th>variable</th>
<th>name</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximal secondary voltage</td>
<td>$v_{\text{max}}$</td>
<td>180</td>
<td>kV</td>
</tr>
<tr>
<td>Height single core</td>
<td>$h_{\text{core,ges}}$</td>
<td>calc</td>
<td>m</td>
</tr>
<tr>
<td>Width single core</td>
<td>$b_{\text{core,ges}}$</td>
<td>calc</td>
<td>m</td>
</tr>
<tr>
<td>Core window width</td>
<td>$h_c$</td>
<td>calc</td>
<td>m</td>
</tr>
<tr>
<td>Core window height</td>
<td>$b_c$</td>
<td>calc</td>
<td>m</td>
</tr>
<tr>
<td>Core leg cross section area</td>
<td>$A_c$</td>
<td>calc</td>
<td>m$^2$</td>
</tr>
<tr>
<td>Core leg length</td>
<td>$d_Ac$</td>
<td>calc</td>
<td>m</td>
</tr>
<tr>
<td>Pulse flat-top length</td>
<td>$t_{\text{flat}}$</td>
<td>140</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Additional pulse length</td>
<td>$t_{\text{add}}$</td>
<td>8</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Filling factor of core material</td>
<td>$FF$</td>
<td>param</td>
<td></td>
</tr>
<tr>
<td>Distance between cores</td>
<td>$d_{\text{cores}}$</td>
<td>50</td>
<td>mm</td>
</tr>
<tr>
<td>Distance secondary windings in core window</td>
<td>$d_{\text{sw}}$</td>
<td>15</td>
<td>mm</td>
</tr>
<tr>
<td>Distance secondary winding to core bottom</td>
<td>$d_{\text{b,s}}$</td>
<td>10</td>
<td>mm</td>
</tr>
<tr>
<td>Primary winding foil thickness</td>
<td>$d_s$</td>
<td>calc</td>
<td>mm</td>
</tr>
<tr>
<td>Secondary winding height</td>
<td>$h_s$</td>
<td>calc</td>
<td>mm</td>
</tr>
<tr>
<td>Secondary turn diameter</td>
<td>$d_{t,s}$</td>
<td>calc</td>
<td>mm</td>
</tr>
<tr>
<td>Secondary winding suspension thickness</td>
<td>$d_{s,s}$</td>
<td>calc</td>
<td>mm</td>
</tr>
<tr>
<td>Primary foil thickness</td>
<td>$d_{f,p}$</td>
<td>calc</td>
<td>mm</td>
</tr>
<tr>
<td>Distance primary winding core</td>
<td>$d_{cp}$</td>
<td>10</td>
<td>mm</td>
</tr>
<tr>
<td>Distance primary winding to core top</td>
<td>$d_{t,p}$</td>
<td>10</td>
<td>mm</td>
</tr>
<tr>
<td>Distance primary winding to core bottom</td>
<td>$d_{b,p}$</td>
<td>10</td>
<td>mm</td>
</tr>
<tr>
<td>Primary winding height</td>
<td>$h_p$</td>
<td>calc</td>
<td>mm</td>
</tr>
<tr>
<td>Distance core tank top</td>
<td>$d_{ct,\text{top}}$</td>
<td>50</td>
<td>mm</td>
</tr>
<tr>
<td>Distance core tank bottom</td>
<td>$d_{ct,\text{bot}}$</td>
<td>10</td>
<td>mm</td>
</tr>
<tr>
<td>Additional distance to tank wall</td>
<td>$d_{\text{add}}$</td>
<td>40</td>
<td>mm</td>
</tr>
<tr>
<td>Tank length</td>
<td>$l_{\text{tank}}$</td>
<td>calc</td>
<td>m</td>
</tr>
<tr>
<td>Tank height</td>
<td>$h_{\text{tank}}$</td>
<td>calc</td>
<td>m</td>
</tr>
<tr>
<td>Tank width</td>
<td>$w_{\text{tank}}$</td>
<td>calc</td>
<td>m</td>
</tr>
<tr>
<td>Tank volume</td>
<td>$V_{\text{tank}}$</td>
<td>calc</td>
<td>m$^3$</td>
</tr>
</tbody>
</table>
Table 4.4: Derivation of geometry variables, listed in tab. 4.3 from predefined user data, optimization variables and material parameters.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{c,eff}$</td>
<td>$A_c \cdot FF$</td>
</tr>
<tr>
<td>$d_{Ac}$</td>
<td>$\frac{A_c}{w_{Ac}}$</td>
</tr>
<tr>
<td>$d_{s,min}$</td>
<td>$\frac{d_{t,s}}{2} \cdot \exp \left( \frac{2 \cdot v_{max}}{n_s \cdot d_{t,s} \cdot E_{max}} \right)$</td>
</tr>
<tr>
<td>$h_{s,min}$</td>
<td>$n_s \cdot (d_{s,min} + d_{t,s})$</td>
</tr>
<tr>
<td>$b_c$</td>
<td>$4 \cdot r_r + d_{sw} + 2 \cdot d_{w,hs} + 2 \cdot d_{cp} + 2 \cdot d_{prim}$</td>
</tr>
<tr>
<td>$h_{s,min}$</td>
<td>$n_s \cdot d_{s,min}$</td>
</tr>
<tr>
<td>$h_s$</td>
<td>$h_{s,min} + h_{s,add}$</td>
</tr>
<tr>
<td>$h_c$</td>
<td>$d_{w,hs} + h_s + d_{b,s}$</td>
</tr>
<tr>
<td>$h_p$</td>
<td>$h_c - d_{t,p} - d_{b,p}$</td>
</tr>
<tr>
<td>$h_{coreges}$</td>
<td>$h_c + 2 \cdot d_{Ac}$</td>
</tr>
<tr>
<td>$b_{coreges}$</td>
<td>$b_c + 2 \cdot d_{Ac}$</td>
</tr>
<tr>
<td>$w_{tank}$</td>
<td>$b_c + 2 \cdot d_{Ac} + 2 \cdot d_{add} + 2 \cdot (2 \cdot d_{w,hs} + d_{cp} + n_p \cdot d_{prim} + 2 \cdot r_r)$</td>
</tr>
<tr>
<td>$h_{tank}$</td>
<td>$d_{ct,top} + d_{ct,bot} + h_c + 2 \cdot d_{Ac}$</td>
</tr>
<tr>
<td>$l_{tank}$</td>
<td>$n_c \cdot w_{Ac} + (n_c - 1) \cdot d_{cores} + 2 \cdot (2 \cdot d_{w,hs} + d_{cp} + n_p \cdot d_{prim} + 2 \cdot r_r + d_{add})$</td>
</tr>
<tr>
<td>$V_{Tank}$</td>
<td>$w_{tank} \cdot h_{tank} \cdot l_{tank}$</td>
</tr>
<tr>
<td>$l_{corew}$</td>
<td>$n_c \cdot w_{Ac} + (n_c - 1) \cdot d_{cores}$</td>
</tr>
<tr>
<td>$l_{out}$</td>
<td>$2 \cdot (b_c + 2 \cdot d_{Ac} + 2 \cdot (d_{cp} + n_p \cdot d_{prim}) + 2 \cdot (d_{w,ls} - d_{s,s} + 0.5 \cdot (d_{w,hs} + d_{s,s} - d_{w,ls}))$</td>
</tr>
</tbody>
</table>
4.2.2 Transformer parasitics modeling

In section 4.1 it was made plausible, that deriving the transformer parasitics are crucial in pulse transformer design. For analyzing the pulse shape, which will be described in detail in section 4.2.4, the distributed capacitance $C_d$ and the leakage inductance $L_\sigma$ of the transformer must be derived. In [46] simplified analytical equations were proposed for both parameters. However, these equations are only valid for certain geometries (e.g. long winding height compared to the winding distance) and contain assumptions such as a centered field shape ring between magnetic core and oil tank.

Consequently, in this section analytical methods are described to calculate the distributed capacitance and the leakage inductance for a matrix transformer with flexible geometry.

At first, the method for calculating $C_d$ is introduced, followed by the calculation method of $L_\sigma$.

Calculation Method of Distributed Capacitance $C_d$

In order to estimate the distributed capacitance $C_d$ of a pulse transformer, the geometry is analyzed in the two dimensional space to obtain the capacitance per unit length $C'_d$, which is then multiplied with its associated length $l_{cap}$ according to

$$C_d = C'_d l_{cap}. \quad (4.15)$$

All formulas in this and the next paragraph therefore relate to the two dimensional space.

The entire distributed capacitance $C'_d$ of a system is related to the entire electrical energy $W'_{el,tot}$ by

$$C'_d = \frac{2 W'_{el,tot}}{v_s^2}, \quad (4.16)$$

where $v_s$ is the voltage potential, the capacitance is charged to, which is in this application the secondary voltage potential of the transformer.

a) Calculation method via the electrical field: According to Coulomb's law, the magnitude of the electrical field in a two dimen-
sional space $|E(x, y)|$ caused by a line charge $\lambda_1$ can be described by

$$|E(x, y)| = \frac{1}{2\pi \epsilon} \cdot \frac{|\lambda_1|}{x^2 + y^2}. \quad (4.17)$$

The magnitude of the line charge $|\lambda_1|$ can be derived with its relation with the voltage potential $\Phi(x, y)$. The potential $\Phi(x, y)$ of $N$ conductors with line charges $\lambda_k$ and x-coordinates $a_k$ and y-coordinates $b_k$ and radius $R$ can be described by

$$\Phi(x, y) = C + \sum_{k=1}^{N} \frac{\lambda_k}{2\pi \epsilon} \ln \left( \frac{(x - a_k)^2 + (y + b_k)^2}{(x - a_k)^2 + (y - b_k)^2} \right). \quad (4.18)$$

To calculate the line charges $\lambda_k$, the known potentials of the $N$ turns at their surface $\Phi(a_k - R, b_k - R)$ are substituted in (4.18), forming a linear equation array. With (4.17) the derived line charges $\lambda_k$ can then be used to obtain the magnitude of the resulting electrical field $|E(x, y)|$, which is for $k$ line charges determined by

$$|E(x, y)| = \sqrt{E_x^2 + E_y^2} = \frac{|\lambda_k|}{2\pi \epsilon}.$$  

$$\sum_{k=1}^{N} \left( \left( \frac{x - a_k}{(x - a_k)^2 + (y - b_k)^2} - \frac{x - a_k}{(x - a_k)^2 + (y + b_k)^2} \right)^2 + \left( \frac{y - b_k}{(x - a_k)^2 + (y - b_k)^2} - \frac{y + b_k}{(x - a_k)^2 + (y + b_k)^2} \right)^2 \right)^{0.5}. \quad (4.19)$$

The magnitude of the electrical field $|E(x, y)|$ is known at any given point of the geometry outside of the conductors’ radii. Therefore, the electrical energy $W_{elec}$ of a surface can be calculated via the corresponding surface integral:

$$W_{elec} = 0.5 \epsilon \int \int |E_{ges}(x, y)|^2 dx dy \cdot l_{Rx}. \quad (4.20)$$

This approach is of interest, since also information about the electrical field of the geometry is provided, which is required for an analysis of the electrical field distribution (see section 4.2.3). However, since the electrical field must be calculated in a small grid to obtain the desired accuracy of $W_{elec}$, the calculation time is not suitable for application in an optimization procedure. Especially for large transformer geometries,
where the number of required points for calculation of $W_{elec}$ increases drastically, this approach is not feasible. Therefore, a matrix approach based on conductor arrays is described in the following paragraph, which is implemented instead to determine $C_d'$. 

**b) Calculation method via the capacitance matrix:** In order to analyze the transformer parasitics, the winding geometry is simplified by approximating the primary foil winding by $n$ circular conductors, equally distributed over the primary winding height $h_p$. A homogeneous current distribution over the $n$ conductors is assumed. $n$ is chosen to be $n_s$ in order limit the distance between to adjacent line conductors. The field shape ring is considered as a conductor with larger radius. In case of the investigated system, the primary and secondary windings are grounded at one end.

With a multi-conductor system in the two dimensional space, which is displayed in Fig. 4.9 a) for four conductors, the relation between potential $\Phi'$ and charge $Q$ is described by

$$[Q] = [p]^{-1} \cdot [\Phi'] = [c] \cdot [\Phi'],$$

(4.21)

where $[p]$ describes the potential coefficients and $[c]$ the capacitance coefficients.

In the investigated geometry, the conductors are surrounded by the magnetic core and the metal oil tank, which are both connected to the ground potential. The influence of these surfaces on the electric field distribution is considered by applying the charge simulation method (CSM) [99]. Each conductor is mirrored in four direction. To describe the influence of the core window correct, the mirror charges have alternately positive and negative signs as displayed in Fig. 4.9 b). In the procedure, there are $N = 99$ mirrored charges considered for each conductor.

In a two dimensional space the potential coefficient $p_{ij}$ between conductor $i$ and $j$ can be described based on the superposition principle [92] by

$$p_{ij} = \frac{1}{2\pi\epsilon_0\epsilon_r} \left( \ln \left( \frac{r_{ij}}{r_c} \right) + \sum_{mp_j=mn_j=1}^{N/2} \ln \left( \frac{r_{i,mp_j}}{r_{i,mn_j}} \right) \right), \quad i \neq j,$$

(4.22)
where \( r_{ij} \) is the distance from conductors \( i \) to conductor \( j \), \( r_{i,mp} \) the distance of conductor \( i \) to all positive mirror charges and \( r_{i,mn} \) to all negative mirror charges of conductor \( j \).

In case of \( i = j \) the potential coefficient is obtained by

\[
p_{ii} = \frac{1}{2\pi\varepsilon_0\varepsilon_r} \left( \sum_{mp_i=mn_i=1}^{N/2} \ln \left( \frac{r_{i,mp_i}}{r_{i,mn_i}} \right) \right),
\]

where \( r_r \) is the radius of the conductor, \( r_{i,mp} \) the distance of conductor \( i \) to all its positive mirror charges and \( r_{i,mn} \) to all its negative mirror charges.

To obtain the partial capacitances between conductors \( C'_{ij} \), at first the potential coefficient matrix \([p]\) has to be inverted. This inversion leads to the capacitance coefficients matrix \([c] = [p]^{-1}\). The partial capacitance per unit length between two conductors \( C'_{ij} \) and the capacitance to the surrounding potential \( C'_{i\infty} \), can be obtained by

\[
C'_{ij} = -c_{ij} \quad \text{and} \quad C'_{i\infty} = \sum_{j=1}^{n} c_{ij}.
\]

The \( n_s \) secondary turns are considered as line conductors with a voltage potential \( v_{ks} \) of the \( k \)-th secondary conductor of

\[
v_{ks} = v_s \frac{k - 1}{n_s - 1}, 1 \leq k \leq n_s,
\]

where \( v_s \) is the secondary voltage potential of the transformer. The considered voltage potential \( v_{js} \) of the primary \( j \)-th conductor is obtained by

\[
v_{jp} = v_p \frac{j - 1}{n_s - 1}, 1 \leq j \leq n_s,
\]

where \( v_p \) is the primary voltage potential.

The total distributed capacitance per unit length \( C'_d \) based on the secondary voltage potential \( v_s \) is derived from the total stored electric energy \( W_{el,tot} \) of the investigated geometry. \( W_{el,tot} \) can be obtained by summing up the electric energy stored in each of the partial capacitances:

\[
W_{el,tot}' = \frac{2}{v_s^2} \sum_{j=1}^{n} 0.5 C'_{i,j} (v_i - v_j)^2 \quad \text{and} \quad C'_d = \frac{2 W_{el,tot}'}{v_s^2}.
\]
Figure 4.9: a) Resulting capacitances of a geometry with four conductors showing individual potential and charge in relation to a potential, which is situated at infinity. b) Three wires in a geometry limited in each direction with a grounded surface. These surfaces are considered by applying mirror charges in each direction, which show alternately positive and negative charge. [94]

Since for most pulse transformers the relation $v_s/v_p \gg 1$ is valid, the primary windings can also be considered as entirely grounded. Then, the mirroring axis shifts from the grounded core leg to the position of the primary winding. This simplification reduces the computation time since only half of the turns must be considered. If the primary winding is placed very close to the core and the distance to the secondary winding is large enough, the error will be negligible (e.g., for Fig. 4.40 smaller than 2%). As a broad application of the optimization procedure is desired, the additional computational effort is accepted and all conductors are considered.

As the geometry of the investigated matrix transformer is symmetrical, there are only two different winding geometries of interest:

a) the distributed capacitance $C'_{d,cw}$ inside the core window

b) the distributed capacitance $C'_{d,ct}$ between core and tank wall.

To obtain the total distributed capacitance $C'_{d,tot}$ of the pulse trans-
former, equation (4.15) is multiplied by \( l_{cap} = l_{core} \) for a) and by \( l_{out} \) for b) (see. tab. 4.4) and both results are added.

**Calculation of leakage inductance**

![Image of magnetic flux lines and box mirroring](image)

**Figure 4.10:** a) Resulting magnetic flux lines of two conductors with opposite current flow. b) Box mirroring of the conductors by considering the magnetic core as magnetic mirror.

The leakage inductance \( L_\sigma \) is obtained analogous to (4.15) by multiplying the inductance per unit length \( L'_\sigma \) with its associated length \( l_{ind} \):

\[
L_\sigma = L'_\sigma l_{ind}.
\]

(4.28)

The chosen calculation method is based on a multi conductor system. Equal simplification of the winding geometry is conducted as was previously applied for the calculation of the distributed capacitance.

In a multi conductor system, the magnetic flux per unit length \( \Phi'_B \) is defined by

\[
[\Phi'_B] = [L'] \cdot [I].
\]

(4.29)

Due to the two-dimensional analysis, it is not of interest how the conductors are connected as turns [100]. The external inductance \( L'_{ij,ex} \) caused by the external H-field between two circular conductors with equal radius can be described by

\[
L'_{ij,ex} = \frac{\mu r}{2\pi} \ln \left( \frac{d_{ij}}{r_c} \right) \quad i \neq j,
\]

(4.30)
were $d_{ij}$ is the distance between the two conductors, and $r_c$ the conductor’s radius. The internal inductance caused by the conductor itself can be described by

$$L'_{i,i} = \frac{\mu_r}{8\pi}$$

(4.31)

The core has a very high permeability $\mu_r$ and therefore can be seen as a magnetic mirror [101]. The arrangement of the mirror conductors is depicted in Fig. 4.10. Other than for the mirror charges, the direction of the current flow remains equal for the mirror conductors. Considering the mirror conductors, the total self inductance $L'_{ii,box}$ can be described by

$$L'_{ii,box} = \frac{\mu_r}{2\pi} \left( \frac{1}{4} + \sum_{m_{cj}=1}^{N} \ln \left( \frac{d_{i,m_{ci}}}{r_c} \right) \right),$$

(4.32)

where $d_{i,m_{ci}}$ is the distance of conductor $i$ to all its mirror conductors. Equivalently, the external inductance is obtained by

$$L'_{ij,ex} = \frac{\mu_r}{2\pi} \ln \left( \frac{d_{ij}}{r_c} + \sum_{m_{cj}=1}^{N} \ln \left( \frac{d_{i,m_{cj}}}{r_c} \right) \right) \quad i \neq j,$$

(4.33)

where $d_{ij}$ is the distance of conductor $i$ to conductor $j$, $d_{i,m_{cj}}$ the distance of conductor $i$ to all mirror conductors of conductor $j$. $N = 103$ mirrored conductors are considered for each turn in the optimization procedure.

Outside the core window, the turns are only mirrored in one direction at the axis of the core. This single axis mirroring is applied, since the surrounding oil tank has a lower permeability than the magnetic core. Additionally, the distance from the winding to the tank wall is higher than its distance to the magnetic core. In this case, the number of mirrored conductors reduces to $N = 1$. If a homogeneous current distribution over all conductors is assumed, the total inductance per unit length of the geometry can be obtained by

$$L'_{\sigma} = \sum_i \sum_j L'_{ij}.$$

(4.34)

In order to obtain the leakage inductance $L'_{\sigma}$ of an investigated design, $L'_{\sigma}$ must be equally multiplied with its associated length as described for $C_d$. 

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4.2.3 Determination of the peak electrical field value

Right after the geometry of the pulse transformer has been defined, the resulting peak value of the electrical field is analyzed to avoid electrical field enhancement in the design (see Fig. 4.6). The arrangement of the 2D-geometry is simplified by neglecting the secondary winding suspension. This simplification is reasonable, since the relative permittivity of the selected oil MIDEL 7131 (\(\epsilon_{r,MIDEL} = 3.2\)) does not drastically differ from the suspension material FR4 (\(\epsilon_{r,FR4} = 4\)). In this simplified arrangement, the resulting electrical field is continuous. In this case, the peak value of the electrical field occurs at the surface of the secondary turns.

There are two different calculation methods implemented for deriving the peak value of the electrical field:

The first method is an approximation of the geometry by a cylindrical capacitor, which is depicted in Fig. 4.11 a). This method can be selected, if the peak value of the electrical field is known to occur at the turn with highest voltage potential, which is a valid assumption for most of the designs with a single layer arrangement of the secondary winding. In a cylindrical capacitor, the highest electrical field \(E_{max}\) occurs at the inner radius \(r_r\) and is defined by

\[
E_{max}(r_r) = \frac{v_s}{r_r} \left(\frac{d_{w,hs}}{r_r}\right) \ln\left(\frac{d_{w,hs}}{r_r}\right), \tag{4.35}
\]

where in this application \(v_s\) is the secondary voltage level and \(d_{w,hs}\) the distance to the primary winding on the high voltage side of the secondary winding.

This simple approximation offers the fastest computation time, and in arrangements with a large core window with equal distances to all sides, the estimated peak value of the electrical field is only \(\approx 2\% - 5\%\) lower than reference value obtained by a 2D FEM analysis. Since this deviation can increase for different transformer arrangements, this rapid calculation method is only implemented to obtain a first estimate.

For a more accurate calculation, the second method offers a calculation of the peak electrical field with the relations presented in section 4.2.2. In section 4.2.2 it was described, that the electric energy of the transformer is derived via the capacitance matrix method, since deriving the electrical field for a high number of points in the entire core window...
Figure 4.11: a) Approximation of geometry with a cylindrical capacitor. b) The electrical field is analyzed in $P = 20$ contour points equally distributed over the conductor’s surface. $K = 16$ line charges are arranged inside the conductor displaced from the center by distance $\Delta \lambda = 0.04 \cdot r_c$.

would lead to a high computational effort. In order to derive the peak value of the electrical field of the design, however, only relatively few points on the conductors’ surfaces have to be determined. Therefore, the formulas (4.18) and (4.19) are applied for each considered secondary turn. Equal to section 4.2.2, the grounded surfaces are taken into account by mirror charges. In order to derive a more accurate electrical field value on the conductor’s surface, $K = 16$ line charges per conductor are considered inside its circumference [102]. They are displaced from the center of the conductor by distance $\Delta \lambda = 0.04 \cdot r_c$, where $r_c$ is the radius of the conductor. For each conductor, the electrical field is analyzed in $P = 20$ points equally distributed over the conductor’s circumference, as shown in Fig. 4.11 b). There are three different variants of the second calculation method selectable:

In the first variant, only the grounded core and the two field shape rings are considered. The relation is depicted in Fig. 4.12 a). This simplification will be adequately accurate, if the field shape rings are mounted centrally over the secondary winding. In this case, their distance to the primary winding is smaller than the distance of the other secondary turns, which also feature a high voltage potential. Due to
the smaller distance of the field shape rings to the primary winding, the electrical field is the highest on their surface, even though their diameter is large compared to the diameter of the other secondary turns.

Since the position of each field shape ring can be freely adapted and displaced from the center of the secondary winding, in the second variant, the turns with a voltage higher than a desired voltage $v_{s,min}$ can be considered as displayed in Fig. 4.12 b).

In the last variant, all turns of the geometry are considered, which requires the highest computational effort, but also offers the highest accuracy.

For CLIC specifications, the second variant of the second calculation method with $V_{s,min} = 120 \text{kV}$ is selected.

### 4.2.4 Pulse shape submodule

The function of the pulse shape submodule is to determine, whether nor not the pulse respects the given set of pulse requirements. If the
pulse does not comply with the specifications, a penalty will be set and all further calculations will be aborted. Otherwise, the pulse efficiency is calculated, which is the ratio between the transferred energy to the klystron during the flat-top interval and the entire provided pulse energy.

It was shown, that the non-linear behavior of the klystron load influences the pulse form strongly due to a higher damping compared to a resistive load [46]. To accurately model the pulse shape, the transfer characteristic of a klystron can be considered, which is defined by

\[ i_{klys}(t) = k \cdot v_{klys}^{1.5}(t), \quad k = \frac{I_{klys,nom}}{V_{klys,nom}^{1.5}}, \quad (4.36) \]

where \( k \) is the perveance, \( i_{klys}(t) \) and \( v_{klys}(t) \) are the time dependent values of current and voltage. \( I_{klys,nom} \) and \( V_{klys,nom} \) are the respective values of the klystron’s operation point. In Fig. 4.13 the voltage pulse with a klystron load is exemplarily compared to a resistive load for a nominal pulse voltage of \( V_{pulse} = 150 \text{kV} \) with a selected perveance of \( k = 3.33 \frac{\mu A}{V^{1.5}} \). It displays, that the klystron load characteristic leads to a higher damping of the pulse. Therefore, a klystron load requires a higher distributed capacitance \( C_d \) to obtain a critically damped pulse.

Figure 4.13: Comparison of the output voltage of a resistive load and a klystron load with perveance for a nominal pulse voltage of \( V_{pulse} = 150 \text{kV} \).
So far, the influence of the klystron was either neglected assuming a purely resistive load, a piecewise linearization on the transfer function was applied or a correction term of the damping was considered. \cite{46,103}. For an optimization procedure with a broad load spectra, however, a piecewise linearization for every operation point is impractical. Therefore, the pulse behavior is analyzed in the time domain, solving the non-linear differential equations numerically. Due to the time domain analysis, the model is able to cope with any provided non-linear load function.

Additionally, the primary voltage can be considered as a time dependent function, allowing to integrate the rise and fall times of the primary pulse switches $t_{r,s}, t_{f,s}$ as well as the voltage droop in the primary capacitors $\Delta v_{cap}$ during the pulse flat-top period $t_p$. Especially for short pulse modulators, where the rise time of the switches typically is in the same decade as the pulse rise time, the pulse shape is influenced significantly and therefore must be considered. The applied voltage signal $v_1(t)$ is defined according to

$$v_1(t) = \begin{cases} 
\frac{v_p}{t_{r,s}} \cdot t & , 0 \leq t \leq t_{r,s} \\
v_p - \frac{\Delta v_{cap}}{(t_p)} \cdot (t - t_{r,s}) & , t_{r,s} < t \leq t_{r,s} + t_p \\
(v_p - \Delta v_{cap}) \cdot \left(1 - \frac{t - (t_{r,s} + t_p)}{t_{f,s}}\right) & , t_{r,s} + t_p < t \leq t_{r,s} + t_p + t_{f,s} \\
0 & , otherwise, 
\end{cases}$$

(4.37)

where $v_p$ is the desired primary pulse voltage level.

The applied circuit model for analyzing the pulse shape is derived from \cite{104}, based on the secondary voltage potential and depicted in
The winding resistance $R_{11}$ is calculated in the winding loss model (section 4.2.5). The transformer magnetizing inductance $L_m$ is obtained from the core loss submodule (section 4.2.7). The transformer parasitics $L_\sigma$ and $C_d$ are obtained from analytical calculations described in section 4.2.2. Further estimated parameters are the primary inductance of the switching modules $L_{11}$, an additional secondary capacitance $C_{add}$ due to the klystron tank and the high voltage cable capacitance $C_{add}$. All estimated parameters are listed in tab. 4.5.

Considering these circuit elements the nonlinear differential equations result in:

$$M1: v'_1(t) = R'_{11} \cdot i_{ges}(t) + (L_\sigma + L'_{11}) \cdot \frac{di_{ges}(t)}{dt} + v_s(t) \quad (4.38)$$

$$K1: i_{ges}(t) = \frac{1}{C_d + C_{cab} + C_{add}} \cdot \frac{dv_l(t)}{dt} + \frac{1}{R_{fe}} \cdot v_s(t) + k \cdot v_s^{1.5}(t) + i_m(t) \quad (4.39)$$

$$i_m(t) = \frac{1}{L_m} \cdot \int v_s(t), \quad (4.40)$$

where $v_s(t)$ is the secondary pulse voltage, $i_m(t)$ the magnetizing inductor current and $i_{ges}(t)$ the total secondary current.

By solving (4.38)-(4.40), the pulse shape of the transformer is obtained during rise time, the flat-top period and the fall time until the first zero crossing of the pulse voltage $t_{zc}$. The magnetization period can be considered by choosing an initial value for the magnetizing current $i_m(t = 0)$, which is defined by

$$i_m(t = 0) = v_m \cdot t_{pre}. \quad (4.41)$$

Since the differential equations do not consider the diode characteristic of the klystron load, they are not valid after the first zero crossing $t_{zc}$ of the pulse voltage $v_s$. At this time instance, there is still energy stored in the magnetizing inductance, which will be transferred into the active reset circuit capacitor $C_m$ (see section 4.2.6). It is a valid assumption, that this energy can be retrieved by the active reset circuit, except losses occurring in its components [46]. Therefore, losses occurring during the magnetizing and demagnetization periods are separately considered in the active reset circuit loss model.
Implementation of the pulse constraints

In order to save computational effort and thereby reduce the optimization cycle time, in a first step the equations (4.38)-(4.40) are only solved for a short time period $t_{\text{control}}$. During this time interval, the adherence of the pulse constraints is controlled. $t_{\text{control}}$ is defined by

$$t_{\text{control}} = t_{\text{settle}} + t_{\text{add}},$$

where $t_{\text{settle}}$ the settling time and $t_{\text{add}}$ is chosen to $t_{\text{add}} = 2 \mu s$.

The resulting pulse signal, depicted in Fig. 4.35, is compared in every time step with the predefined overshoot voltage $v_{os}$ and the two boundaries of the voltage band $v_{p,h}$ and $v_{p,l}$, which are defined by

$$v_{p,h} = v_p + \frac{FTS}{2},$$
$$v_{p,l} = v_p - \frac{FTS}{2},$$

where $FTS$ is flat-top stability specification (see tab. 1.1).

If the signal crosses the voltage boundary of the overshoot specification $V_{\text{max}}$, the calculation will be terminated and a high penalty will be set. As long as the signal exceeds the upper voltage level $v_{p,h}$ or falls below the lower boundary $v_{p,l}$ of the voltage band, the reference time $t_{\text{ref}}$ is increased. At the end of the investigated time interval $t_{\text{control}}$, the value of $t_{\text{ref}}$ indicates the beginning of the flat top period $t_{\text{flat}}$. For $t_{\text{ref}} > t_{\text{settle}}$, a penalty is set. This is also the case for $t_{\text{ref}} > t_{\text{rise}}$, with the relation:

$$t_{\text{rise}} = t(v = 90\% \cdot v_s) - t(v = 10\% \cdot v_s).$$

Once a penalty is set, the optimization cycle is terminated. In order to ensure that the algorithm converges to the desired design space, the penalties increase with their difference from the desired set point value. For the voltage overshoot the penalty is the higher, the shorter the time is to exceed the given limit. In case of $t_{\text{rise}}$ and $t_{\text{settle}}$, the penalty is the higher, the higher the difference to the respective set point value results.

If the pulse complies with all given pulse specifications, the pulse shape is again derived with (4.38)-(4.40) for the entire pulse length. Then, the pulse efficiency $\eta_{\text{pulse}}$ is computed according to

$$\eta_{\text{pulse}} = \frac{E_{\text{flattop}}}{E_{\text{entire}}},$$

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where $E_{\text{flattop}}$ is the usable pulse energy during the flat-top period and $E_{\text{entire}}$ is the entire pulse energy from the beginning of the pulse until its first zero crossing $t_{zc}$.

Even though in many cases a certain rise time of the pulse is specified, it would advisable to specify the time to flat-top as optimization criteria, since it is the variable which directly relates to the pulse efficiency and determines the pulse length, which must finally be applied. As specifications for the CLIC modulator consider the time to flat-top $t_{\text{settle}}$ (see tab. 1.1), the rise time penalty is disabled for the optimization with CLIC parameters.

### 4.2.5 Winding loss submodule

In this submodule, the winding losses due to the pulse excitation are derived. The effects, which cause the frequency dependent winding losses (skin and the proximity effect), and their related formulas are described in [67] and therefore are not detailed in this paragraph.

In order to estimate the frequency losses in the conductor due to the pulsed current, a trapezoidal approximation of the pulse is applied for the fast Fourier transform ($FFT$) analysis. The magnitude of the $n$-th Fourier coefficient $|C_n|$ of a repetitive trapezoidal pulse is defined by

$$|C_n| = \frac{2 I_p}{n \pi} \cdot |\sin (n \pi t_{flat}/t_{rep})| \cdot \left| \frac{\sin (n \pi t_{rise}/t_{rep})}{n \pi t_{rise}/t_{rep}} \right| \tag{4.45}$$

where $t_{rise}$ is the pulse rise time, $t_{flat}$ the pulse length and $t_{rep}$ the pulse repetition period. $I_p$ is the pulse current of the respective winding.

For calculation the proximity effect losses, the secondary circular turns are transformed to a sheet conductor as described in [67]. A simplified geometry is estimated, in which the windings cover the entire height $h_c$ of the core window.

### Selection of winding diameters for CLIC specifications

In order to minimize winding losses caused by the skin effect, the secondary winding diameter for CLIC specifications was investigated.
The skin depth $\delta$ is defined by [67]

$$
\delta = \frac{1}{\sqrt{\pi \mu_0 f \sigma}}.
$$

(4.46)

If frequencies up to the frequency of $f_p = \frac{1}{t_{\text{flat}} + t_{\text{rise}}}$ are considered, which is the first zero in the frequency spectra of the trapezoidal (see (4.45)), the skin depth results in $\delta = 0.79$ mm. To obtain a high utilization rate of the conductor’s cross-section, the conductor’s diameter should therefore be limited to $d_{c,\text{max}} = 2 \cdot \delta = 1.58$ mm.

Two solid conductors in parallel with a diameter of $d_c = 1.3 \cdot \delta = 1.32$ mm are selected for the transformer prototype, which remain below $d_{c,\text{max}}$ and at the same time limit the root mean square (RMS) current density of the secondary winding to $j_{sec} = 3$ A/mm$^2$.

For the primary windings foil conductors were applied with a thickness of $d_p = 0.5$ mm. The RMS current density at the smallest width of the primary winding results to $j_{prim} = 3.25$ A/mm$^2$.

### 4.2.6 Active reset circuit submodule

In this submodule of the optimization procedure, the losses due to the active reset circuit are derived. The active reset circuit allows a doubling of the magnetic flux swing, thereby reducing the magnetic core volume. A detailed analysis of different reset circuits is provided in
A schematic of the realized reset circuit is displayed in Fig. 4.14 a). The corresponding voltage and current waveforms with active reset circuit are depicted in Fig. 4.14 b). To achieve the doubling of the magnetic flux swing, the core is subjected to a negative magnetizing voltage $V_m$ prior to the pulse for the time interval $t_{pre}$ by closing the magnetizing switch $S_m$. As no inverse beam current can flow in the klystron load, the klystron can be approximated as a non-linear resistance with a diode in series. Therefore, a magnetizing current $i_m$ is built up in the magnetizing inductance $L_m$ of the transformer. The magnetizing voltage $V_m$ is chosen in such a way, that the magnetic flux density reaches the desired negative value $-B_{max}$ during the interval $t_{pre}$, also considering that the maximum reverse voltage of the klystron must not be exceeded. During the pulse interval $t_p$, $S_m$ is opened and $S_p$ is closed. The flux density changes from $-B_{max}$ to $B_{max}$ as well as $i_m$ reverts its sign. After the pulse interval, the remaining magnetizing current in $L_m$ is reduced to zero by the freewheeling path of $D_m$ and the energy is transferred back to $C_m$.

For the applied loss calculation, it is assumed that the entire stored magnetic energy $L_m$ can be retrieved after the pulse except for losses in the diode $D_m$. Likewise, during the magnetization phase only losses occurring in $S_m$ are considered, neglecting losses of cables and capacitor $C_m$. The magnetic core losses during this interval are considered in section 4.2.7. Further, a steady state operation of the pulse transformer is presumed were the magnetization interval $t_{pre}$ equals the demagnetization interval $t_{de}$, which leads to

$$t_{pre} = t_{de} = \frac{V_p \cdot t_p}{2 V_m}, \quad (4.47)$$

were $V_m$ is the magnetization voltage, which is a user input parameter. The procedure controls, that the desired $V_m$ on the primary side does not exceed the assumed reverse voltage of the klystron $V_{rev} = 25$ kV:

$$|V_m| \leq \left| \frac{V_{rev}}{n} \right|. \quad (4.48)$$

With an assumed constant magnetization voltage $V_m$, the magnetization peak current $\hat{I}_m$ can be obtained by

$$\hat{I}_m = \frac{V_m t_{pre}}{L_m}, \quad (4.49)$$
The loss energy per active active reset cycle $E_{\text{act}}$ then results in

$$E_{\text{act}} = 0.5 \cdot V_m \cdot \left( \frac{I_{m}}{\sqrt{3}} \cdot (V_{cc} + U_f) + \frac{I_{m}^2}{3} \cdot (R_{on,s} + R_{on,d}) \right),$$  \hspace{1cm} (4.50)

where $V_{cc}$ is the collector emitter voltage and $R_{on,m}$ the on-state resistance of $S_m$, $U_f$ is the forward voltage and $R_{on,d}$ the on-state resistance of $D_m$.

**Improved short circuit handling due to the active reset circuit**

During the regular modulator operation, a secondary short circuit can occur due to arcing of the klystron gun. The energy intake, which can be survived during such a shorting of the klystron load, is limited to 20-40 J, which is why special emphasis must be set on a fast over current detection and a fast turn off of the pulse switches in such an instance.

Besides the doubling in magnetic flux swing, the active bias circuit also contributes to the short circuit handling of the modulator system. The relations are explained based on the schematic drawing provided in Fig. 4.14 a). In case of a gun arcing, a short circuit current $i_{\text{short}}$ begins to build up, only limited by the leakage inductance $L_\sigma$. Without the active bias circuit, $i_{\text{short}}$ will be dissipated in the klystron load, once the pulse switch $S_p$ is turned off, since there only exists the freewheeling path via $L_m$ and the klystron load.

With the active bias circuit, in parallel to $L_m$ an additional path via $D_m$ and $C_m$ is obtained, which reduces $i_{\text{short}}$ due to the inverse voltage $V_m$ much faster and also absorbs short circuit energy in $C_m$. Thus, the energy intake of the klystron load in case of an arc is significantly reduced in comparison to a system without active bias circuit.

**Parameters of the active reset circuit for CLIC**

The procedure derives its calculations from the user input of the magnetization voltage $V_m$. When designing the active reset circuit, other considerations such as the capacitor voltage after a short circuit and the required capacitance value for a certain magnetization time have to be taken into account. Design considerations of the active reset circuit were adapted from [47] to the CLIC specific pulse length.
The maximal magnetization voltage for CLIC results according to (4.48) in $V_{m,\text{max}} = 403$ V. Therefore, the capacitors MKP1848C72550JY5 from Electronicon are selected with a voltage rating $V_{C,\text{max}} = 500$ V. In Fig. 4.15 the required magnetization time is displayed in dependence on the magnetization capacitance value for different initial magnetizing voltages $V_m$ in the range of 200 – 400 V. It becomes clear, that at least a voltage level of $V_m = 250$ V should be selected to keep the capacitance value limited. Another constraint, which must be considered, is that even after a short circuit the maximal reverse voltage $V_{m,\text{max}}$ must not be exceeded. This constraint results in an upper voltage limit $V_{up}$ of

$$
V_{up} = \sqrt{0.5 \cdot \frac{E_{\text{short}}}{C_r} - V_{m,\text{max}}^2},
$$

(4.51)

where $E_{\text{short}}$ is the energy intake of one active reset circuit during a secondary short circuit.

Assuming in worst case a turn off delay of $t_d = 6 \mu s$, the energy intake per active reset circuit results in $E_{\text{short}} = 7$ J. $E_{\text{short}}$ is derived from a circuit simulation. With a selected capacitance value of $C_m = 1.5$ mF,

**Figure 4.15**: Required magnetization time in dependence on the magnetization capacitance for different initial magnetizing voltages $V_m$ in the range of 200 – 400 V.
V_up = 380 V is obtained. In Fig. 4.16 the required magnetization time for the selected C_m is displayed in dependence of the applied voltage. Since the reduction of magnetization time in the voltage range 300-400 V is not significant, V_m = 300 V is selected as operating voltage, which offers a safety margin to V_{m,max} = 403 V and fixes the magnetization time to t_{pre} = 860 μs.

4.2.7 Core loss submodule

In pulse transformer design, the most important core material properties are the losses, the maximum flux density and the weight. The investigated core excitation is a rectangular voltage shape. Since the considered load is a klystron, which shows an inherent diode characteristic, an active bias circuit is applied (see section 4.2.6), which results in a bipolar voltage shape.

Core Loss measurement setup

In order to investigate the influence of different core materials with the optimization procedure, accurate magnetic loss models are required.
Since the applied pulse shape strongly differs from standard sinusoidal waveforms, measurement data with this specific excitation profile is required.

To investigate the core losses with pulsed excitation for different core materials, a converter was designed with its schematics depicted in Fig. 4.17. The core under test (CUT) is connected in between two half bridges, connected at the lower end. The selected switches are STY139N65M5 by ST Microelectronics. Both half bridges are controlled via an FPGA, which allows different excitation profiles. However, the selected voltage waveform was set according to Fig. 4.14 b) and (4.47). The converter prototype for the core loss measurements is depicted in Fig. 4.18. The DC voltages are supplied by external voltage sources. In order to facilitate the recoding of a measurement series, a user interface in LABVIEW was implemented, which allows the control of the external voltage sources and computes the core losses from the recorded primary current $I_{\text{meas}}$ and secondary voltage $V_{\text{meas}}$ according to [101]. The investigated materials are amorphous Metglas (2605SA1), 3% grain oriented silicon iron with 50µm and 100µm thickness and a nanocrystalline material (VITROPERM 500F). The flux swing is varied from $\Delta B_{\text{min}} = 0.25 \, \text{T}$ to the respective saturation flux density of the material.

From the core loss measurements, the magnetic loss energy per pulse and the corresponding mean relative permeability $\bar{\mu}_r$ are obtained. For these two parameters value arrays are integrated in the optimization...
procedure. Intermediate values are interpolated.

The core loss submodule provides besides the magnetic losses also the magnetizing inductance value $L_m$ according to

$$L_m = \mu_0 \bar{\mu_r} n_s^2 \cdot \frac{A_{c, eff}}{l_{eff}},$$  \hspace{1cm} (4.52)

### 4.2.8 Pulse switch submodule

In this submodule, the losses of the pulse switches are computed. Since in most pulse application for klystron loads the repetition frequency $f_{rep}$ is low, only conduction losses are considered in the loss model of the procedure.

The applied current pulse form is composed of the primary load current $I_p$ and the magnetizing current $I_m$ of the transformer. Since a magnetization period is applied prior to the pulse, the primary pulse current begins with the value $I_p = -\hat{I}_m$ (see (4.49)) and continuously increases until it reaches the value $I_p = \hat{I}_m$ at the end of the pulse interval (a steady state operation of the active reset circuit is assumed). Then, the average power $P_{av}$ transferred by the pulse switches can be described
by

\[
P_{av} = \frac{1}{T} \cdot \int_0^{t_p} V_p(t) \cdot I(t)dt
\]

\[
= \frac{V_p}{T} \cdot \int_0^{t_p} (I_p - I_m + \frac{2I_m \cdot t}{t_p}) dt
\]

\[
= \frac{V_p}{T} \cdot \left[ (I_p - I_m) \cdot t + \frac{I_m \cdot t^2}{t_p} \right]_0^{t_p}
\]

\[
= V_p \cdot I_p \frac{t_p}{T}.
\]

Equation (4.53) shows, that in case of an active bias circuit the average transferred power during the pulse \( P_{av} \) is independent on the magnetizing current \( I_m \). The total RMS current during the pulse \( I_{RMS,tot} \) can be obtained by

\[
I_{RMS,tot} = \sqrt{I_{RMS,p}^2 + I_{RMS,m}^2} = \sqrt{I_{RMS,pulse}^2 + \hat{I}_m^2} \tag{4.53}
\]

Assuming \( \hat{I}_m = 0.25 \cdot I_p \), which would be a high value for \( \hat{I}_m \), the increase in \( I_{RMS,tot} \) would just result to 1%. Therefore, the influence of the magnetizing current is neglected and the loss energy per pulse of the pulse switches \( E_{ps} \) is derived according to

\[
E_{ps} = V_{CE,sat}(I_p) \cdot I_p \cdot t_p, \tag{4.54}
\]

where \( V_{CE,sat}(I_p) \) is the collector emitter saturation voltage at the chosen pulse current \( I_p \).

**Arrangement and thermal behavior of pulse switches for CLIC**

In the optimization procedure, the current capability and the voltage rating of the selected pulse switch are not considered. Therefore, in this paragraph the arrangement and the thermal behavior of the applied pulse switches are discussed.

The chosen high voltage pulse switches are the press pack IGBTs 5SNA1250B450300 with specifications listed in *tab. 4.6*. To limit the voltage stress of the IGBT, the highest primary voltage level is set to
PULSE TRANSFORMER

**Figure 4.19:** Water cooled pulse switch press pack, consisting of a 5SNA1250B450300 IGBT for the pulse interval, a 5SNA070045B0301 IGBT for the magnetization interval with corresponding magnetization capacitors $C_m$.

$V_p = 3\, \text{kV}$. As magnetization switch the 5SNA070045B0301 is selected, which features equal package than the pulse switch, but there are less IGBT chips and more diode chips integrated. Both switches are arranged in a water cooled press pack stack as depicted in **Fig. 4.19**. This press pack stack was already applied in a previous pulse applica-

**Table 4.6:** Selected datasheet values of the 5SNA1250B450300.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$R_{th,1}$</th>
<th>$R_{th,2}$</th>
<th>$R_{th,3}$</th>
<th>$R_{th,4}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}$</td>
<td>2.882 K/kW</td>
<td>3.178 K/kW</td>
<td>0.641 K/kW</td>
<td>0.586 K/kW</td>
</tr>
<tr>
<td>$I_{dc}$</td>
<td>4.5 kV</td>
<td>201.5 J/K</td>
<td>18.4 J/K</td>
<td>8.6 J/K</td>
</tr>
<tr>
<td>$I_k$ (10 µs)</td>
<td>1.25 kA</td>
<td>3.178 K/kW</td>
<td>0.641 K/kW</td>
<td>0.586 K/kW</td>
</tr>
<tr>
<td>$V_{ce,sat,typ}$</td>
<td>3.4 V</td>
<td>0.641 K/kW</td>
<td>8.6 J/K</td>
<td>2.2 J/K</td>
</tr>
<tr>
<td>$V_{ce,sat,max}$</td>
<td>3.7 V</td>
<td>8.6 J/K</td>
<td>2.2 J/K</td>
<td></td>
</tr>
<tr>
<td>$C_1$</td>
<td>201.5 J/K</td>
<td>0.641 K/kW</td>
<td>8.6 J/K</td>
<td></td>
</tr>
<tr>
<td>$C_2$</td>
<td>18.4 J/K</td>
<td>0.641 K/kW</td>
<td>8.6 J/K</td>
<td></td>
</tr>
<tr>
<td>$C_3$</td>
<td>8.6 J/K</td>
<td>2.2 J/K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_4$</td>
<td>2.2 J/K</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 4.20: a) Thermal model of IGBT 5SNA1250B450300 with indicated temperatures of junction $T_j$, heat sink $T_{hs}$ and ambient temperature $T_A$. $P_{\text{pulse}}$ consists of a time interval $t_{\text{pulse}}$ with value $P_{\text{max}}$ and a time interval $t_{\text{pause}}$ with zero value. This pattern is repeated with frequency $f = \frac{1}{t_{\text{wdh}}}$. b) Junction temperature $T_j$ plotted over time for a 140 $\mu$s-pulse with $I_{\text{pulse}} = 2\,\text{kA}$ and $I_{\text{pulse}} = 3\,\text{kA}$ at a primary voltage level of $V_p = 3\,\text{kV}$.

tion [47] and pulse switches were shown to be capable of turning off a short circuit up to 7.6 kA at 3 kV [107]. Modifications for the desired application were carried out on the magnetization capacitance $C_m$ and on the busbar connection. Since the required pulse length for CLIC is significant larger than the modulator system in [47], the thermal behavior of the pulse switch is analyzed according to the thermal model depicted in Fig. 4.20 a) with parameters listed in tab. 4.6. The time dependent value of the junction temperature $T_j$ is illustrated in Fig. 4.20 b) for a $t_p = 140\,\mu$s-pulsed current with 2 kA and 3 kA at a pulsed voltage of $V_p = 3\,\text{kV}$. The analysis clearly shows, that a 3 kA pulse current results in a slight increase of the junction temperature $T_j$ compared to a 2 kA pulse current. From the thermal point of view, the switch would remain below a thermal cycling of $\Delta T = 10^\circ$ even for pulse currents up to 12 kA. However, the rated short circuit current, which can be turned off in a $t_k = 10\,\mu$s interval is $I_k = 5\,\text{kA}$. In order to limit the short circuit energy, dissipated in the switch during a arcing of the klystron, the pulse current is limited to $I_{p,\text{max}} = 3\,\text{kA}$ for CLIC specifications, which results in a minimum number of four switching units and two magnetic cores for the optimization procedure.
4.3 Pulse transformer prototype

For the final prototype, the pulse transformer design derived in section 4.7.5 was adapted. The executed changes together with their reasoning are briefly summarized in the following, which are:

a) Change of magnetic core material
b) Position of field shaping ring
c) Distance between magnetic core and tank cover
d) Inclusion of a differential mode filter for the secondary windings

a) For the pulse transformer, a laminated core is applied. A laminated core consists of many thin layers of magnetic material, which are isolated from each other in order to limit occurring eddy current losses. The core material previously selected in section 4.7.2 was amorphous Metglas (2605SA1), which features a small interlaminar isolation voltage [108]. This material property might lead to a voltage breakdown of a single laminate in the desired pulsed application, which then increases the voltage stress on the remaining laminates. Over time, all laminates might be affected, which then would deteriorate the properties of the magnetic core. That’s why the magnetic core material was changed to silicon iron with a bandwidth of 50 $\mu$m.

b) The field shape ring is attached to the secondary winding suspension. Due to constructional reasons, the field shape ring could not be arranged in alignment with the opening angle of the secondary winding, but is placed centrally on top of the winding. The distance between the field shape ring and the primary winding (see Fig. 4.8) is kept constant (45 mm), resulting in an increase of the distance between secondary and primary winding to 49 mm. This change in secondary winding arrangement leads to an increase in leakage inductance in comparison to the original arrangement of $L'_\sigma = 1.06 \cdot L_\sigma$.

c) Furthermore, the distance between magnetic cores and oil tank cover was increased, since a steel bar was required to carry the core weight, which is attached with screws to the tank cover. The attachment requires additional space, which does not affect the performance of the pulse transformer, but increases its tank volume.
d) To improve the current sharing of the two parallel connected secondary windings, a differential mode filter was integrated in the return path of the secondary winding.

The realized pulse transformer prototype is depicted in Fig. 4.21. To ease the handling the magnetic cores as well as all mechanical and electrical connections are connected to the top plate of the oil tank. The HV side of the secondary winding is free-floating, thereby avoiding creepage paths via solid connections.

**Figure 4.21:** Realized pulse transformer prototype. The HV side of the secondary winding is free-floating, thereby avoiding creepage paths via solid connections.
Figure 4.22: Visualization of the electrostatic and magnetostatic 2D-FEM analysis for the final prototype: a) Norm of the magnetic field in kA/m b) Norm of the electrical field in kV/mm.

4.4 Analysis of the final design

Even though the general validity of the transformer parasitics calculation has been shown in section 4.6, it is advisable to verify the obtained results of the procedure again for the final prototype system, prior to its realization. The major changes towards the realization of the prototype system have been listed in section 4.3. In the following paragraphs the analytical parasitics calculation (see section 4.2.2) is compared to a 2D-FEM and 3D-FEM analysis. Further, the insulation design (see section 4.7) is checked for the realized gap distances of the prototype system.

4.4.1 Validation of the parasitics calculation

To verify the analytical parasitics calculation, the results for the final prototype system are compared with an electrostatic and a magnetostatic 2D-FEM analysis. with the results visualized in Fig. 4.22. For both methods the electric and magnetic energy per unit length is listed in tab. 4.7 for the area inside the core window and the area outside the core window. Both methods show a close match with errors below 10% in all four cases. In order to derive the entire comprised energy of the
Table 4.7: Comparison of the analytical parasitics calculation and 2D-FEM simulations for the electric and magnetic energy per unit length comprised in the final transformer prototype.

<table>
<thead>
<tr>
<th></th>
<th>Core window</th>
<th>Core to tank wall</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E'_{elec,2DFEM}$ (J/m)</td>
<td>4.29</td>
<td>2.932</td>
</tr>
<tr>
<td>$E'_{elec,calc}$ (J/m)</td>
<td>4.57</td>
<td>3.168</td>
</tr>
<tr>
<td>relative error $E'_{elec}$ (%)</td>
<td>+6.53</td>
<td>+8.05</td>
</tr>
<tr>
<td>$E'_{mag,2DFEM}$ (J/m)</td>
<td>10.96</td>
<td>4.48</td>
</tr>
<tr>
<td>$E'_{mag,calc}$ (J/m)</td>
<td>10.59</td>
<td>4.46</td>
</tr>
<tr>
<td>relative error $E'_{mag}$ (%)</td>
<td>-3.38</td>
<td>-0.45</td>
</tr>
</tbody>
</table>

Geometry, the energies per unit length have to be multiplied with their corresponding length, which are derived according to Table 4.4, resulting in $l_{corew} = 0.5072$ m and $l_{out} = 2.481$ m.

Figure 4.23: Visualization of the electrostatic 3D-FEM analysis with three 2D cuts. Depicted is the norm of the electrical field $|E|$ in kV/mm.
Table 4.8: Total comprised electric energy and peak electrical field value of the final transformer prototype derived by the analytical approach, by 2D-FEM and 3D-FEM simulations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{elec,3DFEM}$ (J)</td>
<td>9.510</td>
</tr>
<tr>
<td>$E_{elec,2DFEM}$ (J)</td>
<td>9.450</td>
</tr>
<tr>
<td>$E_{elec,calc}$ (J)</td>
<td>10.178</td>
</tr>
<tr>
<td>Relative error 2D-FEM to 3D-FEM (%)</td>
<td>-0.6</td>
</tr>
<tr>
<td>Relative error calc to 3D-FEM (%)</td>
<td>+7.02</td>
</tr>
<tr>
<td>Relative error calc to 2D-FEM (%)</td>
<td>+7.02</td>
</tr>
<tr>
<td>$E_{peak,3DFEM}$ (kV/mm)</td>
<td>10.4</td>
</tr>
<tr>
<td>$E_{peak,2DFEM}$ (kV/mm)</td>
<td>10.57</td>
</tr>
<tr>
<td>$E_{peak,calc}$ (kV/mm)</td>
<td>10.08</td>
</tr>
<tr>
<td>Relative error 2D-FEM to 3D-FEM (%)</td>
<td>+1.63</td>
</tr>
<tr>
<td>Relative error calc to 3D-FEM (%)</td>
<td>-3.08</td>
</tr>
<tr>
<td>Relative error calc to 2D-FEM (%)</td>
<td>-4.6</td>
</tr>
</tbody>
</table>

In addition, a comparison with a 3D FEM analysis of the geometry, depicted in Fig. 4.23 is performed for the electrostatic analysis. With the comparison to the 3D FEM analysis, the derived lengths of the geometry $l_{corew}$ and $l_{out}$ can be validated as well as the derived peak electrical field value. For all three different methods the peak electrical field and the total comprised electric energy is listed in tab. 4.8. The peak electrical field of the analytical calculation shows similar values (relative error < 5 %) to both FEM analyses and therefore offers a good approximate applicable in an optimisation procedure. Considering the similarity of the 2D-FEM and the 3D-FEM result, the applied geometric lengths $l_{corew}$ and $l_{out}$ seem to present a valid approximate of the three dimensional energy distribution.

4.4.2 Evaluation of the insulation design

In this section, the insulation design is evaluated in detail for the final prototype transformer. In order to determine suitable isolation distances for a given design, it is in a first step important to derive the degree of homogeneity of the electrical field. To measure the degree of homogeneity, the Schwaiger’s
utilization factor $\eta_S$ can be derived, which is obtained by \[109\]

$$\eta_S = \frac{E_0}{E_{\text{max}}}, \quad (4.55)$$

where $E_{\text{max}}$ is the peak electrical field, and $E_0$ the electrical field in case of a homogeneous electrical field distribution, which is determined by $E_0 = V/d$. There are three different degrees of inhomogeneity distinguished according to \[109\]:

1. very little inhomogeneous: $0.8 \leq \eta_S < 1$

2. little inhomogeneous: $0.2 \leq \eta_S \leq 0.8$

3. inhomogeneous: $\eta_S \leq 0.2$

Since the standard breakdown tests such as the ASTM D 3300 are performed with small gap distances, the resulting withstand voltage has to be adapted in order to derive a suitable value for larger oil gaps, which occur in the real size transformer. For 50 Hz-AC voltages, the most common adaption scheme is the Weidmann curve \[110\], where the electrical field strength, at which partial discharge inception occurs in a one minute 50 Hz-AC excitation, is plotted against the oil gap distance. In dependence on the degree of inhomogeneity $\eta_S$ there are three different methods proposed to determine the withstand voltage $V_{\text{wts}}$: \[109\]

In case of a very little inhomogeneous electrical field ($0.8 \leq \eta_S \leq 1$), the electrical field strength $E(d)$ at distance $d$ is determined and the withstand voltage is derived by

$$V_{\text{wts}} = E(d) \cdot d. \quad (4.56)$$

For little inhomogeneous fields the electrical field along the gap length must be integrated, in order to determine its value at the gap length $d$. The withstand voltage $V'_{\text{wts}}$ then calculates to

$$V'_{\text{wts}} = \int_0^d E(x)dx = E(d) \cdot d. \quad (4.57)$$

For inhomogeneous electrical fields the determination of the cumulative electrical field strength is proposed in \[111\], which calculates the mean
electrical field for different intervals along the oil gap length. This method was selected to analyze the electrical field distribution of the transformer prototype. The cumulative electrical field strength \( E_m(z) \) is obtained by

\[
E_m(z) = \frac{1}{z} \int_{x_1}^{z} E(z') dz'.
\]  

(4.58)

For CLIC a particular pulse voltage excitation is applied, which differs from the standard 50 Hz-AC excitation drastically. Furthermore, an environmentally friendly ester oil is employed instead of the standard mineral oil. That's why, a method is proposed, which scales available breakdown data on small gaps to the desired application. This method is described in detail in section 4.7.

It should be noted that other than in [111], where the Weidmann curve (partial discharge inception voltage) is used as reference line, in section 4.7 the 1% breakdown probability of a Weibull distribution is applied. Additionally, in section 4.7, the volume effect and the voltage-time product of the pulse voltage excitation are considered. It is stated in [109] that the Weidmann curve corresponds to the probability of a Weibull distribution below 2%. That's why both approaches seem to address a breakdown probability in a comparable range. However, the similarity of the 1% breakdown probability and the partial discharge inception voltage in ester oil has not been validated by measurements and must therefore be applied with precaution.

Additionally, it is pointed out that the applied breakdown data in section 4.7 are evaluated for natural ester oil (FR3), whereas in the final prototype a synthetic ester (MIDEL7131) is selected. This is the case, due to a lack of available breakdown data for larger oil gap distances.

Table 4.9: Comparison of breakdown voltages for natural ester (FR3) and synthetic ester (MIDEL7131) with a gap distance of \( d = 3.8 \text{ mm} \) according to [112]. Listed are the lightning impulse test (LI), the switching impulse test (SI) and 50 Hz-AC excitation.

<table>
<thead>
<tr>
<th></th>
<th>Midel7131</th>
<th>FR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>LI(kV)</td>
<td>208.8</td>
<td>202.8</td>
</tr>
<tr>
<td>SI(kV)</td>
<td>169.2</td>
<td>169.7</td>
</tr>
<tr>
<td>AC(kV)</td>
<td>103.2</td>
<td>101.8</td>
</tr>
</tbody>
</table>
in case of synthetic ester. In a comparative study between both different ester oils, conducted in [112], it was shown, that for the lightning impulse, the switching impulse and the standard 50Hz-AC excitation, both ester oils show comparable breakdown voltages. For the sake of completeness the comparison of [112] is listed in tab. 4.9

**Isolation distance examination of the transformer prototype**

For the final prototype the most critical field path is again evaluated according to section 4.7. In order to determine the Schwaiger factor, the peak electrical field value of the transformer design $E_{\text{peak}} = 10.6\, \text{kV/mm}$, depicted in Fig. 4.24 is related to the electrical field in an assumed homogeneous electrical field distribution. Considering the distance between field shape ring to primary winding $E_1$ results to $E_{0,1} = 3.75\, \text{kV/mm}$ with corresponding $\eta_{S,1} = 0.3538$ (according to

![Electrical field norm (kV/mm)](image)

**Figure 4.24:** Geometric magnification of the lower left corner of the core window. Basis is the electrostatic 2D-FEM analysis of Fig. 4.22 b). Indicated are two lines $E_1$ and $E_2$, along which the electric field is analysed. Indicated is the peak electrical field value $E_{\text{peak,2D FEM}} = 10.57\, \text{kV/mm}$. 

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Figure 4.25: Analysis of the most critical electrical field path along the gap distance. $E_{mitt}$ is the derived cumulative electrical field strength according to [111]. $E_{crit}$ is the most critical field shape line of the prototype according to a 2D-FEM analysis. $E_{max}$ is the maximal allowed electrical field value based on scaled high voltage breakdown data. $E_{int}$ is the integral of $E_{crit}$, which is required for the analysis according to (4.57).

(4.55)). Taking into account a diagonal line from the field shape ring to the corner of the core window, $E_2$, results to $E_{0,2} = 2.69 \text{kV/mm}$ with corresponding $\eta_{S,2} = 0.2538$. Both values are still considered as little inhomogeneous, but $\eta_{S,2}$ is close to being considered inhomogeneous. Therefore, the cumulative electrical field strength method is applied, since it demands lower electrical field values along the oil gap in comparison to (4.57) and therefore presents the safer choice. Several field shape lines are evaluated and $E_1$ was determined to be the most critical. The electrical field along the line $E_1$ is therefore compared to the scaled high voltage breakdown data according to the procedure of section 4.7. The results are listed in Fig. 4.25. With the cumulative electrical field strength method of (4.58) the remaining safety factor of $E_1$ is $q_1 = 1.1$, whereas with (4.57) a safety factor of $q_2 = 1.9$ results. Since with both different analyses the safety factor remains above unity for the entire gap length, the design of the prototype transformer is considered as valid.
4.5 Verification by measurements

In order to validate the proposed pulse transformer optimization procedure, measurements were conducted on the realized prototype, depicted in Fig. 4.26 which are compared in this section to the predicted values.

4.5.1 Impedance measurement

In order to determine the transformer parasitics $C_d$ and $L_\sigma$, the primary windings were short-circuited and the impedance characteristic was measured from the secondary side of the transformer in open circuit configuration. For the impedance measurement, the transformer was placed in the tank without transformer oil. The measurement chain included the HV cable. The capacitance of the HV cable and the measurement setup was determined to 360 pF. The comparison between predicted and measured values is listed in tab. 4.10 which shows high agreement to the predicted values by the optimization procedure.
4.5.2 Pulse measurements

In order to cross check the transformer parasitics of the impedance measurement, single pulse measurements are conducted in open circuit configuration and with an ohmic load of $R_l = 981 \, \Omega$.

The pulse measurements in open circuit configuration are performed with and without oil at an output pulse voltage level of 24 kV. They are executed to determine the magnetizing inductance $L_m$ and the resonance frequency of the transformer $f_{res}$. $f_{res}$ is related to the trans-
Figure 4.27: Comparison between the predicted pulse shape of the optimization procedure and a 24 kV pulse measurement in air with two active switching units mounted on a single transformer core. The prediction and the measurement show high agreement.

former parasitics according to

\[ f_{res} = \frac{1}{2 \cdot \pi \sqrt{C_d \cdot L_\sigma}}. \]  

(4.59)

Ohmic load measurements are conducted for a 24 kV output pulse in with the transformer in air and a 60 kV output pulse with the transformer immersed in oil. The comparison between the predicted pulse rise time of the optimization procedure and the pulse measurement is depicted in Fig. 4.27 for air and in Fig. 4.28 for oil. Both comparisons show high agreement. In Fig. 4.28 the active magnetization circuit can be noted, which magnetizes the core with 2 kV prior to the pulse interval. Further, a voltage overshoot of about 5% occurs, since the transformer is designed for a klystron load, which provides a higher damping for the pulse.

In order to obtain a first indication of the voltage withstand capability, several single pulses and a pulse burst at maximal primary voltage level of 3 kV were conducted, which corresponds to a secondary voltage level of 186 kV. Since a secondary voltage measurement was not foreseen for the dummy load in oil, only the secondary current was
Figure 4.28: Comparison between the predicted pulse shape of the optimization procedure and a 60 kV pulse measurement in air with four active switching units and active magnetization circuit. The prediction and measurement show a highly similar pulse shape.

Figure 4.29: The high current overshoot results from the antiparallel diode, connected in series to the resistive load. This diode has been integrated, in order to emulate the klystron behavior during the magnetization interval. The current droop is about 40 %, which is due to a smaller applied primary total capacitance of 960 μF and due to the fact, that the droop compensation system is not connected.

For pulse transformer design, the prediction of the pulse shape as well as the voltage withstand capability of the transformer are the most important goals to achieve. Due to the high agreement between predicted and measured pulse shape, the optimization procedure is viable to meet the first goal. From the HV pulse measurements, also a first indicator on the validity of the isolation model, which is included in the procedure, and the isolation distance verification model (see section 4.7) can be derived.
Figure 4.29: Measured secondary pulse current for a pulse with the maximal primary voltage level of $V_{prim} = 3\, \text{kV}$.

Figure 4.30: Comparison between a single active secondary winding and both secondary windings active for a 24 kV-pulse in air.

4.5.3 Current sharing of the secondary windings

Since the two secondary windings are connected in parallel, an asymmetric pulse current sharing might occur, when the pulse switches show
different turn on times. In order to minimize this effect, a differential mode filter was included in the current return path of the secondary windings. If the pulse switches of the first secondary winding, turn on faster than the ones of the other winding, the leakage inductance value, which prevents the current to rise, will be increased by the inductance value of the differential mode filter until its saturation. If switches of both windings turn on at equal time instance, the inductance of the filter is not operative and the pulse rise time is not affected. In order to investigate the effect of the differential mode filter, a pulse was measured with a single active secondary winding. The measured pulse rise time is depicted in Fig. 4.30 and compared to the measurement in Fig. 4.27. It can be observed, that the rise time of the pulse increases drastically. On the one hand this increase is related to a doubling in $L_\sigma$ due to the missing parallel connection of the secondary windings, on the other hand the differential mode filter adds additional inductance. The total leakage inductance was determined to $L_\sigma = 3.34 \text{ mH}$ which is a factor of 2.5 higher than in case of two active secondary windings.
4.6 Optimal transformer design for ultra precise solid state modulators

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Abstract

In this paper a procedure for optimal transformer design with a variable set of constraints for pulse transformers with a pulse range of 3-140 $\mu$s is presented. During the optimization procedure the pulse shape is analyzed in the time domain ensuring that the pulse constraints, such as rise time and overshoot are met. For accurate prediction of the pulse shape, analytical approaches are proposed to estimate the distributed capacitance and leakage inductance of the transformer. The analytical approach is verified by 2D-FEM simulations and measurements. The optimization procedure takes pulse, core, winding, demagnetization losses and losses of the primary switches into account. First, the procedure is applied to an existing pulse transformer with specifications for SwissFEL. An improvement of 16.6% in conversion efficiency is achieved in comparison to the existing design. In a second step, the procedure is applied to specifications of the Compact Linear Collider (CLIC), which demands high conversion efficiency. The resulting optimal transformer consists of three cores with five primary turns and requires a tank volume of 0.915 m$^3$. In an optimal configuration an overall conversion efficiency of 97.7% is achieved for the considered system including pulse losses.

4.6.1 Introduction

Pulse power converter systems are used in a wide range of applications and have to comply with various system requirements, such as output power, flat-top length, and pulse repetition. In addition, the requirements for the pulse shape, rise time, pulse repetition accuracy, flat-top stability and overshoot are highly application dependent as can be seen in two different sets of selected requirements listed in tab. 4.11 one for a short pulse system, the SwissFEL, and one for a long pulse system,
Table 4.11: Specifications for two different modulator systems

<table>
<thead>
<tr>
<th></th>
<th>SwissFEL</th>
<th>CLIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flat-top length</td>
<td>3</td>
<td>140  µs</td>
</tr>
<tr>
<td>Output voltage</td>
<td>370</td>
<td>150 kV</td>
</tr>
<tr>
<td>Output power</td>
<td>120</td>
<td>24 MW</td>
</tr>
<tr>
<td>Rise &amp; fall times</td>
<td>1</td>
<td>3  µs</td>
</tr>
<tr>
<td>Pulse repetition</td>
<td>100</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Primary circuit DC-link voltage</td>
<td>3</td>
<td>3 kV</td>
</tr>
<tr>
<td>Voltage overshoot</td>
<td>-</td>
<td>1 %</td>
</tr>
<tr>
<td>Flat-top stability FTS</td>
<td>&lt;1</td>
<td>0.85 %</td>
</tr>
<tr>
<td>Modulator global efficiency</td>
<td>-</td>
<td>90 %</td>
</tr>
</tbody>
</table>

the Compact Linear Collider (CLIC).
In general, pulse power conversion systems can be divided into four main groups. The first group are line-type modulators, such as pulse-forming networks (PFN) [113]. Secondly, transformer-free systems are based on a single high voltage switch or on the Marx-generator principle [114]. The third group is based on pulse transformers [115], often realized with solid state switches [46]. Finally, there exist resonant topologies for pulses in the millisecond range [116], [117].

This paper focuses on systems with a pulse transformer and solid state switches for a pulse range of 3 µs to 140 µs. This technology provides high reliability due to its simple structure and reliable short circuit protection.

Solid state modulators with matrix transformers have been investigated in [118], [119] and [77].

Due to the varying specifications, the pulse power conversion systems must be adapted for its individual purpose. In order to ensure for every redesign the optimal conversion system, which meets all specifications, optimization procedures can be applied. To allow a reasonable overall computing time, one optimization cycle should not exceed one second. Thus, analytical approximations are used to calculate the transformer parasitics. Analytical approximations have already been conducted in [46], but they are not applicable for arbitrary geometry.

Therefore, improved analytical approximations are proposed in this paper, which are suitable for a broader range of transformer geometries. They are then integrated in an optimization procedure maximizing the
efficiency of the pulse transformer under the constraints of electrical and pulse requirements including switching unit. At first, an overview of the investigated system is given in section 4.6.2. Subsequently, the optimization procedure is presented in section 4.6.3, which analyzes the pulse shape in the time domain and controls the pulse specifications. In addition, the algorithm contains several models estimating pulse, core, winding, active reset circuit losses and losses of the primary switches. Thereafter, in section 4.6.3 an analytical approach for estimation of the leakage inductance and the stray capacitance is proposed, which is suitable for a variable pulse transformer geometry. Both approaches are compared to 2D-FEM simulations and in addition validated with a measurement of an existing pulse transformer. Finally in section 4.6.4 the optimization procedure is conducted for specifications of SwissFEL. The resulting pulse shape is compared to the pulse shape with parameters derived from an existing pulse transformer with equal specifications. In a second step the procedure is applied for the specifications of CLIC and the results are presented.

4.6.2 Overview of investigated system

The investigated system is a matrix transformer [119] as shown in a simplified schematics in Fig. 4.31. In a matrix transformer the secondary winding encloses all cores leading to a turns ratio $n$, which is defined by

$$n = \frac{v_s}{v_p} \frac{1}{n_c}, \quad (4.60)$$

where $n_c$ is the number of cores, $v_p$ the primary voltage and $v_s$ the secondary voltage. A cone winding arrangement is chosen, because it outperforms a parallel winding arrangement in terms of leakage inductance [86]. Each core has two legs leading to two identical transmission systems, which are connected in parallel. The number of cores is variable. For each core leg, a switching unit, composed of the main capacitor bank $C_m$ and the main switch $S_m$, is considered. Additionally, an active reset circuit per core leg is taken into account ($C_r$, $S_r$ and $D_r$), which will be described further in section 4.6.3. Due to a high ratio of $v_s/v_p$, only the primary leakage inductance $L_{\sigma 1}$, due to the loop comprising main capacitor and switching unit, the primary copper resistance $R_{11}$ of this loop and the secondary capacitance $C_{sec}$ are con-
considered for this transformer setup. Additionally, the leakage inductance $L_\sigma$ and the distributed capacitance $C_d$ of the transformer are taken into account as well as the non-linear klystron load $R_{klys}$.

### 4.6.3 Optimization procedure

The aim of the proposed optimization procedure is to provide a transformer design which suits the selected requirements. This could be a limited overshoot, a limited rise time, a fixed number of primary windings or other certain geometry constraints. As displayed in **tab. 4.11** the CLIC System has demanding specifications regarding modulator global efficiency, from grid to the klystron load. Therefore, in this paper the optimization procedure is not only designed to meet the pulse requirements but also to find a solution with highest system efficiency. In the following subsections, the optimization procedure is described.
Figure 4.32: Optimization procedure: The global optimizer receives system specifications and material limits. The transformer parasitics are calculated analytically. Losses are determined for each model, which are transformed in equivalent components for pulse analysis in the time domain.

briefly, followed by the detailed description of each loss model.

Structure of the Optimization Procedure

The optimization procedure consists of several models as depicted in Fig. 4.32  The global optimizer runs with a set of six optimization
variables: number of primary turns $n_p$, number of cores $n_c$, secondary winding height $h_s$, distance between secondary and primary windings $d_w$, width of the core cross-sectional area $w_{Ac}$ and opening angle of the cone $\alpha$.

In addition, a set of fixed parameters are given such as constants or predefined geometric distances, e.g. the distance between core and tank. These parameters and the optimization variables define the geometry of the transformer and its surrounding tank. Once the geometry is determined, its parameters are used to calculate all required components for the analysis of the pulse shape. At first, the distributed capacitance $C_d$ and the leakage inductance $L_\sigma$ are calculated, as explained in section 4.6.3. Secondly, the winding losses are computed and the ohmic copper resistance $R_{11}$ of the primary side is transferred to the pulse shape analysis. Then, the core losses are calculated and the ohmic resistance $R_{Fe}$ is defined as well as the magnetizing inductance $L_h$. With $L_h$ the magnetizing current at the beginning of the pulse $I_{premag}$ is derived.

With all these parameters the pulse shape is analyzed in the time domain. During this step the optimizer compares the shape with a set of external constraints such as rise time or overshoot. If all the constraints are met, the pulse losses (as described in section 4.6.3) are calculated. The magnetizing current $I_{demag}$ at the end of the pulse is fed back to the active bias loss model, which then calculates the demagnetization losses. Finally, losses of each model are combined to obtain the total losses of the given parameter set.

At the end of the optimization procedure, the algorithm supplies a transformer configuration, where all demanded pulse requirements are met and highest efficiency is achieved.

Geometric transformer setup

In the first step of the optimization procedure, the geometry of the transformer depending on the set of optimization parameters is defined as basis for the analytical calculations. The correlation of geometric parameters is displayed in Fig. 4.33. The entire geometry is defined by few parameters in order to built it as compact as possible while avoiding field enhancement. Therefore, the minimal distance $d_{w, \text{min}}$ between the conductor with the highest voltage potential of the secondary winding and the primary winding must be derived. The same distance is applied between this conductor and the grounded core. The conductor with
the highest secondary voltage potential is usually realized as a field shape ring with radius $r_r$. In order to estimate the resulting electrical peak field, the geometry is approximated as a cylindrical capacitor (see Fig. 4.33), where the highest electrical field occurs at the inner radius $r_r$ and is defined by

$$E(r_r) = \frac{v_s}{r_r} \frac{1}{\ln\left(\frac{d_w}{r_r}\right)}, \quad (4.61)$$

where $v_s$ is the applied secondary voltage, $d_w$ the outer and $r_r$ the inner radius of the cylinder. Therefore, the minimal allowed distance $d_{w,min}$ between the windings can be calculated as

$$d_{w,min} = r_r \exp\left(\frac{v_s}{r_r E_{peak}}\right), \quad (4.62)$$

where $E_{peak}$ is the maximal tolerable peak electric field in oil. This peak field occurs only at the surface of the field shape ring. An average
electrical field between the windings \( E_{av} \), when a homogeneous field is assumed, is defined by

\[
E_{av} = \frac{(v_s - v_p)}{(d_w - rr)}.
\]  

(4.63)

Calculating the average electrical field \( E_{av} \) of the analyzed transformer geometries would result in much lower values than the peak electric field \( E_{peak} \), which is shown in Fig. 4.40 and Fig. 4.41. Because the electrical field in case of the analyzed geometries is inhomogeneous, only the peak electric field is considered and set as constraint. A value of \( E_{peak} = 20 \text{kV/mm} \) is assumed for short pulses of a few microseconds and for longer pulses in the 100 microsecond range the value is set to \( E_{peak} = 12 \text{kV/mm} \).

The cross-sectional area of each single core can be defined by

\[
A_c = \frac{v_p t_{flat}}{2 B_{max} n_p F_c},
\]

(4.64)

where \( F_c \) is the filling factor of the cut tape-wound core and \( B_{max} \) the desired flux density. The other geometry parameters, displayed in Fig. 4.33 are

\[
b_c = 2 r_r + 2 d_w + 2 d_{tp} + 2 d_{prim},
\]

(4.65)

\[
h_{s,min} = n_s d_{s,min} \cos(\alpha_{max}),
\]

(4.66)

\[
h_c = d_w + h_s + d_{top},
\]

(4.67)

\[
d_{Ac} = \frac{A_c}{w_{Ac}}.
\]

(4.68)

The area outside the core is equally structured as the core window, except that the distance between field shape ring and oil tank is enlarged by \( d_{add} \), leading to smaller capacitance values of the transformer, but to higher tank volume. Therefore, the value of \( d_{add} \) is set externally.

**Transformer cooling** The transformer is considered to be in a tank filled with standard transformer oil, to allow a more compact design. The cooling is realized by grounded cooling pipes. The positioning of these pipes is important, as they contribute to the distributed capacitance of the transformer. To minimize their influence, they are positioned at the level of the lower voltage turns. To allow an effective
cooling, the transformer is placed upside down as shown in Fig. 4.33 into the tank. Consequently, the cooling pipes are positioned at the top close to the tank wall, where the heated oil flows due to convection. Even though the ground plate needs to be enforced to carry the transformer weight, this configuration is chosen as it has the additional advantage of wiring being led through the top, thereby avoiding oil leakage.

Winding losses

The winding losses, due to skin- and proximity effect were subject in a number of publications, e.g. [67]. In order to estimate the skin depth in the conductor, the pulse current is approximated as a trapezoid and a FFT analysis is conducted. For calculating the proximity effect losses, the secondary circular windings are transformed to a sheet conductor as shown in [67]. A simplified geometry is assumed, in which the windings cover the entire height of the core window.

Pulse shape analysis

For the design of a pulse transformer, it is crucial to predict the resulting pulse shape. Therefore, in this chapter the time-domain circuit model for pulse prediction is introduced, followed by the pulse constraint implementation and description of the algorithm’s penalty arrangement.

Time domain circuit model

Because the klystron load $R_{klys}$ is non-linear and influences the pulse shape significantly [86], the pulse shape is evaluated in the time-domain. The applied circuit model is derived from [104], based on the secondary voltage potential and depicted in Fig. 4.34. This circuit model includes the mentioned parameters $C_d$, $L_\sigma$, $L_h$, $R_{Fe}$, $R_{klys}$, $L_{\sigma 1}$, and $R'_{11}$. On the secondary side a capacitance $C_{sec} = 100\,$pF, due to klystron load and measurement equipment, is considered.

Due to the time domain analysis, the model is able to cope with any given non-linear load function. However, for the klystron the load function is defined by

$$i_k(t) = k v_k^{1.5}(t) \quad \text{and} \quad k = \frac{I_{k,\text{nom}}}{V_{k,\text{nom}}^{1.5}}, \quad (4.69)$$
where $k$ is the perveance, $I_{k,nom}$ and $V_{k,nom}$ are the nominal, $i_k(t)$ and $v_k(t)$ the time-dependent values of current and voltage of the klystron. In order to consider the rise and fall times of the primary switches as well as the voltage drop in the primary capacitances $\Delta v_{cap}$ during flat-top, the voltage signal $v'_1(t)$ is applied as a time dependent function. This circuit model is not applicable during demagnetization of the transformer. But it is a valid assumption, that the energy stored in the transformer can be retrieved by the active bias circuit, except losses occurring in its components [46]. Therefore, losses during the pre- and demagnetization periods are considered in the active bias circuit loss model.

**Pulse losses** Because the klystron load cannot be initiated until the voltage complies with the flat top stability criteria, a part of the transferred energy of the pulse is lost. In [120] the ratio between an ideal pulse and an real pulse has been defined as pulse efficiency. Since in this paper the pulse shape is analyzed in the time domain, the energy lost before the klystron can be activated and the energy lost during the fall time of the pulse can be computed. These losses will be referred to as pulse losses in the following.

**Implementation of the pulse constraints** During the optimization procedure the pulse constraints are surveyed. If the pulse exceeds a constraint, a penalty will be set. The pulse behavior is analyzed in the time domain with a non-linear differential equation system, which is solved analytically. A possible pulse shape with constraints is displayed in Fig. 4.35.
The resulting pulse signal is compared in every time step with the pre-defined overshoot voltage and the voltage band. If the signal crosses the overshoot voltage boundary, the calculation will be terminated. As long as the signal exceeds the upper voltage or falls below the lower voltage of the voltage band, the time vector $t_{ref}$ is increased. Because of that, $t_{ref}$ indicates the beginning of the flat top period $t_{flat}$. In order to minimize the computation time the analysis is only conducted for the period of time of

$$t_{controll} = t_{rise} + t_{settle} + t_{add},$$  \hspace{1cm} (4.70)$$

where $t_{rise}$ is the rise time, $t_{settle}$ the settling time and $t_{add} = 2 \mu s$. If $t_{ref}$ is higher than $t_{rise} + t_{settle}$, a penalty will be set. This will also be the case, if $t_{rise}$, which is derived from the pulse signal, is exceeded. In order to ensure that the algorithm converges to the predefined design space, the penalties increase with their difference from the set point value.
Core losses

The considered material for the pulse transformer is Metglas (amorphous alloy 2605SA1) because it offers a good compromise between low losses, high saturation flux density and costs. For a rectangular voltage, resulting in different gradients of the magnetic flux density $dB/dt$, losses can be predicted by the improved generalized Steinmetz equation (iGSE) [68]. In case of a pulse transformer with active bias circuit, which allows to double the magnetic flux density swing, the energy loss per pulse $E_v$ is described by

$$E_v = k_1 A_{c, eff} l_{eff} (2B_{max})^{\beta - \alpha} \cdot \left( t_{premag} \frac{B_{max}}{t_{premag}} \right)^{\alpha} + t_{flat} \left( \frac{2B_{max}}{t_{flat}} \right)^{\alpha} + t_{demag} \left( \frac{B_{max}}{t_{demag}} \right)^{\alpha},$$  

(4.71)

where $\alpha$, $\beta$ and $k_1$ are the Steinmetz parameters, $A_{c, eff}$ the effective cross-sectional area, $l_{eff}$ the effective magnetic length, $t_{premag}$ and $t_{demag}$ the pre- and demagnetization time, $t_{flat}$ the flat-top length and $B_{max}$ the desired magnetic flux density, which was set for the design procedure to $B_{max} = 1.2$ T.

Steinmetz parameters are based on curve fitting and the considered pulse range from 3 to 140 $\mu$s is wide. Therefore, parameter sets for three different ranges as displayed in tab. 4.12 are derived from measurements. The test core is an AMCC 367S core, which has an effective cross-sectional area of 5.29 cm$^2$ and a magnetic length of 43.78 cm. The core is cut to consider the losses, which also occur in the original-sized core. The schematics of the measurement setup and a photo are depicted in Fig. 4.37. The losses were calculated as described in [101] and are displayed in Fig. 4.36. The premagnetization period was chosen by a factor of 7.5 larger than the pulse width.

To estimate the magnetizing inductance $L_h$ as proposed in [46], the

<table>
<thead>
<tr>
<th>Pulse width</th>
<th>3 – 10 $\mu$s</th>
<th>25 – 75 $\mu$s</th>
<th>100 – 300 $\mu$s</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha_{steinmetz}$</td>
<td>1.82</td>
<td>1.643</td>
<td>1.248</td>
</tr>
<tr>
<td>$\beta_{steinmetz}$</td>
<td>2.06</td>
<td>2.645</td>
<td>1.8</td>
</tr>
<tr>
<td>$k_{1,steinmetz}$</td>
<td>0.064</td>
<td>0.462</td>
<td>10.69</td>
</tr>
</tbody>
</table>
Figure 4.36: Measured core losses for a pulse with pre- and demagnetization in dependence of the flux density swing $\Delta B$ and the pulse length. Due to the active reset circuit, the possible maximal flux density swing is doubled. The premagnetization time higher by the factor of 7.5 compared to the pulse length. The test core of amorphous alloy 2605SA1 has an effective cross-sectional area of $5.29 \, \text{cm}^2$ and a magnetic length of $43.78 \, \text{cm}$.

The mean relative permeability $\mu_r$ must be estimated in each measuring point, which is dependent on flux density swing and pulse length, leading to:

$$\mu_r = \frac{\Delta B}{\mu_0 \Delta H}.$$  (4.72)

Active Reset Circuit Loss Model

An active reset circuit as realized in [46] was already displayed in Fig. 4.31. This circuit on the one hand allows to double the flux density swing, which decreases the core volume, on the other hand contributes to the short circuit handling of the converter system. In case of klystron gun arcing, the short circuit current flows through the antiparallel diode $D_r$. Because of the inverse voltage of $C_r$, this current
is reduced faster than if it was only discharged over the diode. It is assumed that all the stored magnetic energy in the transformer can be retrieved by the active reset circuit, except for losses in the switch $S_r$ during premagnetization and losses in the diode during $D_r$ demagnetization.

**Losses of main switches**

Because of high reverse voltage and high current ratings are required, there are only IGBTs as main switches considered. The loss energy $E_{IGBT}$ of an IGBT is defined by

$$E_{IGBT} = V_{CE,sat} I_{prim} t_{flat} + E_{on} + E_{off}, \quad (4.73)$$

where $E_{on}$ is the energy loss during turn on, $E_{off}$ during turn off and $V_{CE,sat}$ the saturation collector emitter voltage. Typical values from datasheet are assumed [121].

**Calculation of parasitics**

In section 4.6.3 it is pointed out that for analyzing the pulse shape, the distributed capacitance $C_d$ and the stray inductance $L_\sigma$ are critical parameters. In [46], simplified analytical equations were proposed for both parameters. However, these equations are only valid for certain geometries and contain assumptions such as a centered field shape ring between transformer and oil tank. Therefore, these are not suitable for

![Figure 4.37: a) Simplified schematics of core loss measurement setup b) Picture of core loss measurement setup](image)
a flexible geometry in an optimization procedure. Consequently, in this section analytical methods are proposed to calculate the distributed capacitance and the stray inductance for a matrix transformer with flexible geometry. The only assumption made is that the core as well as the primary and secondary windings are grounded at one end. This is the case for most pulse transformers in order to obtain a defined potential between the windings [46].

Firstly, the method for calculating \( C_d \) is introduced, followed by the calculation method of \( L_\sigma \). Secondly, these methods are compared to 2D FEM simulations. In addition, the simulations are verified with measurements of an existing pulse transformer.

**Calculation of distributed capacitance** In order to estimate the distributed capacitance \( C_d \) of a pulse transformer, the geometry is analyzed in the two dimensional space to obtain the capacitance per length \( C'_d \), which is then multiplied with its associated length. The \( n_s \) secondary turns are considered as line conductors with a voltage potential \( v_k \) of the \( k \)-th conductor of

\[
v_k = v_s \frac{k - 1}{n_s - 1}, 1 \leq k \leq n_s,
\]

where \( v_s \) is the secondary voltage potential of the transformer. The primary windings are realized as foil conductors and are considered for the analytical calculation as entirely grounded. This simplification leads to a slightly higher capacitance, but the error is negligible (e.g. for Fig. 4.40 smaller than 2%) because

\[
V_s/V_p \gg 1.
\]

In a multi-conductor system in two dimensional space, which is displayed in Fig. 4.38(a) for four conductors, the relation between potential \( \Phi' \) and charge \( Q \) is described by

\[
[Q] = [p]^{-1} \cdot [\Phi'] = [c] \cdot [\Phi'].
\]

In case of the pulse transformer, the conductors are surrounded by the grounded core and the oil tank. The influence of these surfaces is considered applying the charge simulation method [99]. Each conductor is mirrored in each direction to consider the influence of the grounded surfaces. To describe the resulting electrical field correct, the
Figure 4.38: a) Resulting capacitances of a geometry of four wires with individual potential and charge in relation to a potential which is situated at infinity b) Three wires in a geometry limited in each direction with grounded surfaces. These grounded surfaces are considered by applying mirror charges in each direction. The mirror charges have alternately positive and negative signs.

Mirror charges have alternately positive and negative signs as displayed in Fig. 4.38 b). For fast computation time, only $N = 24$ mirrored charges are considered for each conductor.

In a two dimensional space the potential coefficient $p_{ij}$ between conductor $i$ and $j$ can be described based on the superposition principle as

$$p_{ij} = \frac{1}{2\pi\epsilon_0\epsilon_r} \left( \ln(r_{ij}) + \sum_{m_p_j = m_n_j = 1}^{N/2} \ln \left( \frac{r_{i,m_p_j}}{r_{i,m_n_j}} \right) \right), \quad i \neq j, \quad (4.77)$$

where $r_{ij}$ is the distance between two conductors, $r_{i,m_p_j}$ the distance of conductor $i$ to all positive mirror charges and $r_{i,m_n_j}$ to all negative mirror charges of conductor $j$.

In case of $i = j$ the potential coefficient is obtained by

$$p_{ii} = \frac{1}{2\pi\epsilon_0\epsilon_r} \left( \ln(r_r) + \sum_{m_p_i = m_n_i = 1}^{N/2} \ln \left( \frac{r_{i,m_p_i}}{r_{i,m_n_i}} \right) \right), \quad (4.78)$$
where $r_r$ is the radius of the conductor, $r_{i,mp}$ the distance of conductor $i$ to all its positive mirror charges and $r_{i,mn}$ to all its negative mirror charges.

To obtain the partial capacitances between conductors the potential coefficient matrix $[p]$ has to be inverted, to obtain the capacitance coefficients $[c]$. The partial capacitance per unit length between two conductors $C'_{ij}$ and the capacitance per unit length to the surrounding potential $C'_{i\infty}$, can be obtained by

$$C'_{ij} = -c_{ij} \quad \text{and} \quad C'_{i\infty} = \sum_{j=1}^{n} c_{ij}. \quad \text{(4.79)}$$

The total distributed capacitance per unit length $C'_d$ based on the secondary voltage potential $v_s$ is derived from the total stored electric energy $W'_{el,tot}$ of the geometry, which is calculated by summing up the electric energy of each partial capacitance:

$$W'_{el,tot} = \sum_{j=1}^{n} 0.5 C'_{ij} (v_i - v_j)^2 \quad \text{and} \quad C'_d = \frac{2 W'_{el,tot}}{v_s^2}. \quad \text{(4.80)}$$

**Calculation of leakage inductance** The leakage inductance $L_\sigma$ is derived by multiplying of the inductance per unit length $L'_\sigma$ in the two
dimensional space with its associated length. The approach used in this paper is based on a multi conductor system. The geometry is simplified as shown in Fig. 4.39, where the primary winding is approximated by \( n_s \) circular conductors, equally distributed over the primary winding height \( h_p \). The field shape ring is approximated by a smaller circular conductor. The secondary winding conductors are then rearranged, to keep the secondary winding height \( h_s \) constant.

In a multi conductor system, the magnetic flux per length is defined by

\[
\Phi'_i = \sum_j L'_{ij} \cdot I_j. \tag{4.81}
\]

Due to the two-dimensional analysis, it is not of interest how the conductors are connected as turns [100]. Therefore, one primary turn and one secondary turn can be combined to a double circuit line. If the radius \( r_{rr} \) is small compared to the distance \( d_1 \) between the two conductors, the self inductance per unit length \( L'_{11} \) of a double circuit line can be defined by [122]

\[
L'_{11} = \frac{2\Phi'_1}{i_1} = \frac{\mu_0}{\pi} \ln \left( \frac{d_1}{r_{rr}} \right). \tag{4.82}
\]

The mutual inductance per unit length, which is caused by current \( i_1 \) of double circuit line \( l_1 \) in \( l_2 \) as displayed in Fig. 4.39 b) can be described by [122]

\[
M' = \frac{L'_{21}}{i_1} = \frac{\mu_0}{2\pi} \ln \left( \frac{r_{12} r_{21}}{r_{11} r_{22}} \right). \tag{4.83}
\]

Because in the chosen arrangement is it assumed that all conductors carry equal current, the total inductance per unit length of the geometry can be obtained by

\[
L'_\sigma = \sum_i \sum_j L'_{ij}. \tag{4.84}
\]

The core has a very high permeability \( \mu_r \) and therefore can be seen as a magnetic mirror, where the conductors are mirrored as shown in [101]. For fast computation only 8 mirrored conductors are considered for each turn. Outside the core, the conductors are only mirrored in one direction at the axis of the core, because the surrounding oil tank has a lower permeability and the distance to the windings is much higher than between windings and core.
Figure 4.40: FEM simulation for a long pulse transformer geometry with a peak electrical field of $E_{\text{peak}} = 12\, \text{kV/mm}$ and an average field of $E_{\text{av}} = 3.2\, \text{kV/mm}$.

Figure 4.41: FEM simulation for a short pulse transformer geometry with a peak electrical field of $E_{\text{peak}} = 16\, \text{kV/mm}$ and an average field of $E_{\text{av}} = 4\, \text{kV/mm}$.

Validation by 2D FEM simulations  In order to validate the analytical approaches of $C_d'$ and $L'_\sigma$, the results are compared to 2D-FEM simulation. In Fig. 4.40 a matrix transformer geometry for long pulses and in Fig. 4.41 a geometry for short pulses is displayed, each with the resulting magnetic and electric field. 2D-FEM simulations of these two different geometries are compared in tab. 4.13 with $C_d'$ and $L'_\sigma$ for the core window and the space between core and tank.
It can be seen that the difference between 2D-FEM simulations and calculation is smaller than 6%. This indicates that, although simplifications are applied, the accuracy is still high. For further validation analytical calculation results are compared to measurement data in the next section.

Verification with measurements

To validate the proposed analytical calculations of $C_d$ and $L_\sigma$, the calculations are compared to measurements of an existing pulse transformer. The pulse transformer is realized for the specifications in tab. 4.11 b) and corresponds to Fig. 4.41 and Fig. 4.42.

At first it is described in detail how $C_d$ and $L_\sigma$ of the pulse transformer are obtained from analytical calculations, followed by a comparison of the approach with 2D-FEM and measurements.

Parasitics in dependence on geometry

Because the distances between core and tank wall differ at the front, the rear and the side of the pulse transformer, the distributed capacitance per unit length $C'_d$ is calculated for 3 different regions and the core window, which are indicated in Fig. 4.42. These values are then multiplied with the average length of the corresponding region.

The stray inductance does not depend on the distance between core and tank wall, because almost of the magnetic energy is comprised in

<table>
<thead>
<tr>
<th>Table 4.13: Comparison between analytical approach and 2D FEM simulations for the core window and the area between core and tank (Fig. 4.40 and 4.41)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fig. 4.40</strong></td>
</tr>
<tr>
<td>$C'_{d,FEM}(pF/m)$</td>
</tr>
<tr>
<td>$C'_{d,Calc.}(pF/m)$</td>
</tr>
<tr>
<td>$L'_{\sigma,FEM} (\mu H/m)$</td>
</tr>
<tr>
<td>$L'_{\sigma,Calc.}(\mu H/m)$</td>
</tr>
</tbody>
</table>
the area between primary and secondary winding. Therefore, only two different regions are considered: the first inside the core window and the second outside of the core. As average length of the second region the central point between primary and secondary winding is multiplied with the corresponding length, which is indicated with $l_{L',\sigma 2}$.

The results for $C_d$ and $L_\sigma$ in dependence on the area are depicted in tab. \[4.14\]

**Comparison** To validate the proposed analytical calculations further to pulse measurements of an existing pulse transformer were performed. In a first measurement, the primary inductance of a switching unit is determined to be $L_{11} = 90$ nH, which can be transferred to the secondary side with respect to the number of cores and the turn ratio to $L'_{11} = 119$ $\mu$H.

The transformer is then measured with a resistive load of $R_l = 1000$ $\Omega$ at a pulse voltage of $V_s = 189$ kV. The measured pulse shape is then compared with a second order delay element, which can be used to describe the pulse shape at the beginning of the pulse \[46\]. The second order delay element considers the calculated parasitics and in addition
Table 4.14: Distributed capacitance and stray inductance in dependence on the area

<table>
<thead>
<tr>
<th></th>
<th>$C_d'$(pF/m)</th>
<th>Length (m)</th>
<th>$C_d$(pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1$</td>
<td>59.62</td>
<td>0.99</td>
<td>59.0</td>
</tr>
<tr>
<td>$R_2$</td>
<td>60.20</td>
<td>0.525</td>
<td>31.6</td>
</tr>
<tr>
<td>$R_3$</td>
<td>51.17</td>
<td>2.38</td>
<td>121.78</td>
</tr>
<tr>
<td>$R_4$</td>
<td>48.7</td>
<td>0.525</td>
<td>25.57</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>$L_\sigma'$(µH/m)</th>
<th>Length (m)</th>
<th>$L_\sigma$(µH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1$</td>
<td>144.89</td>
<td>0.99</td>
<td>143.44</td>
</tr>
<tr>
<td>$R_2 + R_3 + R_4$</td>
<td>47.945</td>
<td>3.03</td>
<td>145.27</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>2D-FEM Calculations</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{\sigma,ges}$</td>
<td>291.23</td>
</tr>
<tr>
<td>$C_{d,ges}$</td>
<td>230.0</td>
</tr>
</tbody>
</table>

the rise time of the switches of $T_r = 200$ ns.

In Fig. 4.43 the measurement data are compared with the pulse shape with results of 2D-FEM analysis and calculation. Both results show high correspondence to measurements and to each other.

4.6.4 Application of the proposed optimization procedure

Specifications of SwissFEL

The proposed optimization procedure is conducted with specifications of the SwissFEL (tab. 4.11). At first the pulse shape is predicted by using the geometry parameters of the investigated pulse transformer, depicted in Fig. 4.42. The parasitics are taken from section 4.6.3, assuming a klystron load and an additional secondary capacitance of $C_{sec} = 50$ pF. In a second step the algorithm is conducted with equal assumptions, but with unconstrained optimization parameters. Only two optimization parameters, $n_c$ and $w_{Ac}$ are preset: Because of the high required power of 120 MW at least 12 pulse switches are required. Therefore $n_c = 6$ is used in the algorithm, since there are two switching units per core. The minimum core width is preset to have equal width as the used IGBT modules $w_{Ac} = 140$ mm, which is also the case for
the existing transformer, in order to allow a direct connection of the modules and to minimize the primary inductances.

The results of the comparison are displayed in tab. 4.15. The first column lists the results when the optimization parameters correspond to the investigated pulse transformer. In the second column the results are displayed, when the parameters are optimized to high conversion efficiency.

It can be seen that, the optimization procedure results in similar core geometry, but increases the secondary winding height, reduces the distance at the bottom of the windings and increases the number of primary turns to two. Due to a higher number of turns, the leakage inductance and therefore the rise time as well as the damping of the pulse is increased. On the contrary, the time to flat-top is reduced, because the pulse with parameters of the investigated transformer overshoots and complies later with the flat-top criteria as shown in Fig. 4.44, where a section of both pulse shapes is displayed. Thus, by applying the optimization procedure an increase in conversion efficiency including pulse

---

**Figure 4.43:** Measured pulse shape in comparison with predicted pulse shape by analytical calculations and 2D-FEM simulations.
Table 4.15: Comparison between optimization constrained to parameters of existing pulse transformer and optimization with unconstrained parameters.

<table>
<thead>
<tr>
<th>Parameters of transformer</th>
<th>Unconstrained parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary turns</td>
<td>1</td>
</tr>
<tr>
<td>Number of cores</td>
<td>6</td>
</tr>
<tr>
<td>Secondary winding height</td>
<td>13.0</td>
</tr>
<tr>
<td>Distance bottom windings</td>
<td>4.22</td>
</tr>
<tr>
<td>Distance top windings</td>
<td>8.94</td>
</tr>
<tr>
<td>Core window height</td>
<td>30.2</td>
</tr>
<tr>
<td>Core window width</td>
<td>20.2</td>
</tr>
<tr>
<td>Distance core tank</td>
<td>23.75</td>
</tr>
<tr>
<td>Tank volume</td>
<td>0.6384</td>
</tr>
<tr>
<td>Rise time</td>
<td>0.635</td>
</tr>
<tr>
<td>Time to flat-top</td>
<td>2.24</td>
</tr>
<tr>
<td>Conversion efficiency</td>
<td>53</td>
</tr>
</tbody>
</table>

losses from 53 % to 61.8 % can be achieved with corresponds to an relative improvement of 16.6 %.

The proposed optimization procedure is therefore well suited to improve the design process of a pulse transformer.

Specifications of CLIC

The proposed optimization procedure is in a second step executed for the specifications of the CLIC system (see. tab. 4.11). The optimization results are displayed in tab. 4.16. A section of the pulse shape is depicted in Fig. 4.45 a). In an optimal configuration, the pulse does not exceed the voltage band of the FTS and therefore immediately reaches the flat-top criteria.

The distribution of the losses per pulse is displayed in Fig. 4.45 b), showing the dominance of the pulse losses with 61 %, followed by the core losses with 22 % and a share of the other loss components of 18 %. The 2D-FEM analysis is displayed in Fig. 4.40 and the resulting transformer is depicted in Fig. 4.46.
Figure 4.44: Section of pulse shape with specifications of SwissFEL with parameters of the investigated pulse transformer and pulse shape resulting from the optimization procedure with unconstrained parameters. Both displayed pulses have an equal starting point and a pulse width of 3 $\mu$s.

4.6.5 Conclusion

In this paper, a general procedure for pulse transformer optimization is presented, considering a given set of pulse specifications. The optimization parameters include number of primary turns, number of cores, secondary winding height, distance between secondary and primary windings, width of the core cross-sectional area and opening angle of the winding cone. In the procedure the total losses consisting of pulse, core, winding, active bias circuit losses and losses of the primary switches are minimized.

Due to the non-linear klystron load, the pulse shape is analyzed in the time domain, ensuring that the given pulse constraints are met. For core loss estimation, measurements on a test core are performed for pulse lengths in the range of $3 - 300 \mu$s.

In addition, analytical calculations of the transformer parasitics are
Table 4.16: Optimization results for matrix transformer with specifications of CLIC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary turns</td>
<td>5</td>
</tr>
<tr>
<td>Number of cores</td>
<td>3</td>
</tr>
<tr>
<td>Secondary winding height</td>
<td>38.93 cm</td>
</tr>
<tr>
<td>Core window width</td>
<td>10.94 cm</td>
</tr>
<tr>
<td>Distance core tank</td>
<td>14.94 cm</td>
</tr>
<tr>
<td>Tank volume</td>
<td>0.9596 m³</td>
</tr>
<tr>
<td>Rise time</td>
<td>2.85 µs</td>
</tr>
<tr>
<td>Conversion efficiency</td>
<td>97.7 %</td>
</tr>
<tr>
<td>$L_\sigma$</td>
<td>721.27 µH</td>
</tr>
<tr>
<td>$C_d$</td>
<td>380.96 pF</td>
</tr>
<tr>
<td>$L'_{\sigma}$</td>
<td>41.6 µH</td>
</tr>
<tr>
<td>$C_{sec}$</td>
<td>100 pF</td>
</tr>
</tbody>
</table>

proposed and verified with 2D-FEM simulations as well as pulse transformer measurements.

The procedure is then applied to investigate an existing pulse trans-

Figure 4.45: Optimal configuration of matrix transformer with specifications of CLIC: a) Resulting pulse with pulse requirements. b) Distribution of the system losses.
former with specifications of SwissFEL, in order to validate the method and to optimize the existing design. The resulting transformer parameters of the optimisation procedure lead to a shorter time to flat-top and improve the system conversion efficiency by 16.6%. Finally, the procedure is conducted for a long pulse system with the specifications of CLIC optimizing the overall efficiency. An overall conversion efficiency of 97.7% including pulse losses is achieved.

Acknowledgment

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4.7 Design and optimization procedure for high voltage pulse power transformers

Sebastian Blume, Michael Jaritz and Juergen Biela
DOI: 10.1109/TPS.2015.2448351

Abstract

A design and optimization procedure for high voltage pulse transformers is presented. The procedure is enhanced by integration of core loss measurements under pulsed excitation, by electrical peak field calculations and by checking of the isolation distances comparing them to scaled high voltage breakdown data. The procedure is applied with specifications of the Compact Linear Collider (CLIC) and the sensitivity of system parameters such as number of primary turns, core material, transformer oil and high voltage cable length is investigated by comparing their Pareto fronts. With amorphous core material the highest efficiency is achieved. Replacing mineral oil by natural ester results in an efficiency reduction of 0.5% and an increase in cable length from 1.5 m to 5 m reduces the efficiency by 0.6%. Finally, the optimized transformer’s pulse shape is investigated over the entire load range.

4.7.1 Introduction

In the design process of pulse transformers, optimization procedures not only allow an optimal design, but can also be applied for a sensitivity analysis of system parameters. Additionally, a performance evaluation of the transformer regarding different loads can be derived.

For fast computations the procedures are either based on 2D-FEM [98], on analytical formulas [86] or a combination of both [50]. In [81] a design procedure has been presented that calculates the transformer parasitics analytically, analyzes the pulse shape in the time domain and determines the transformer geometry for an optimal pulse shape. In this paper several improvements to that procedure are presented, which are highlighted in Fig. 4.47.

At first in section 4.7.2 the integration of core loss data under pulsed excitation in the procedure is described. Thereafter, in section 4.7.3...
Figure 4.47: Optimization procedure with indication of new features. The core loss measurement integration, the electrical peak field calculation at the conductor surfaces within the optimization cycle and the examination of the isolation distances from scaled impulse breakdown data in an additional process.
the integrated electrical surface field calculation as well as the post-optimization process examining the isolation distances are explained. Furthermore, in section 4.7.4 a sensitivity analysis of the transformer design is investigated for specifications of the compact linear collider (CLIC) by varying system parameters such as magnetic core material, number of primary turns, transformer oil and high voltage cable length. Finally, a performance evaluation of the derived pulse transformer is conducted investigating the influence on the pulse shape when different klystron loads are connected.

### 4.7.2 Core loss measurement data

As the selection of magnetic core material has a drastic influence on the transformer performance, three suitable core materials are investigated, which are amorphous Metglas (2605SA1), 3% grain oriented silicon iron with 100µm thickness and a nanocrystalline material (VITROPERM 500F).

For the transformer design the most important core material properties are the losses, the maximum flux density and the weight. Since core loss data is usually based on sinusoidal excitation, the losses under pulsed excitation are measured using smaller sized cut C-cores. The measurement setup is sketched in Fig. 4.48a). The measurement method is described in detail in [101]. The flux swing is varied from $\Delta B_{\text{min}} = 0.25$ T to the respective saturation flux density of the material. The applied pulse shape is depicted in Fig. 4.48b) with parameters listed in Tab. 4.17. The loss energies per pulse in dependence on the magnetic flux swing $\Delta B$ resulting from the bipolar pulse excitation are listed in Tab.
Table 4.17: Specification of core loss measurements under pulsed excitation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Nano-crystalline</th>
<th>Amorphous</th>
<th>SiFe3% (100µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cross-sectional area (mm²)</td>
<td>795</td>
<td>704</td>
<td>748</td>
</tr>
<tr>
<td>Mean magnetic length (mm)</td>
<td>432</td>
<td>373</td>
<td>507</td>
</tr>
<tr>
<td>Saturation flux density $B_{sat}$ (T)</td>
<td>1.2</td>
<td>1.56</td>
<td>2</td>
</tr>
<tr>
<td>Maximum flux density $B_{max}$ (T)</td>
<td>1.0</td>
<td>1.2</td>
<td>1.5</td>
</tr>
<tr>
<td>Premagnetization time $t_{pre}$ (ms)</td>
<td>1.05</td>
<td>1.05</td>
<td>1.05</td>
</tr>
<tr>
<td>Pulse duration $t_p$ (ms)</td>
<td>0.14</td>
<td>0.14</td>
<td>0.14</td>
</tr>
<tr>
<td>Demagnetization time $t_{de}$ (ms)</td>
<td>1.05</td>
<td>1.05</td>
<td>1.05</td>
</tr>
</tbody>
</table>

The lowest losses occur with the nanocrystalline material. Compared to the nanocrystalline core the amorphous core shows higher magnetic losses by a factor of 2.8, the silicon iron core even higher losses by a factor of 13.2.

By integrating the measurement data, the procedure is extended by an additional free design parameter, which is the magnetic flux swing $\Delta B$. The maximum allowed unipolar flux density $B_{max}$ in the optimization procedure, also listed in Tab. 4.17, is chosen in the linear region of the BH-loop. In section 4.7.4 the influence of these three magnetic core materials on the transformer design is discussed.

4.7.3 Isolation distance in pulse transformers

In high voltage pulse transformer design it is crucial to carefully select the required isolation distances. On the one hand small isolation distances reduce the leakage inductance thereby maximizing efficiency and limiting the transformer size, on the other hand partial discharge must be avoided and long life time of the transformer is desired.

In order to achieve an optimal balance for these contradicting requirements, a two stage approach is presented in this paper. In the first stage, the peak electrical field is limited within the optimization cycle to obtain a suitable transformer design with a certain oil gap distance. In the second stage, in a post-optimization process, the resulting oil gap distances are checked by analysis of the most critical field path.
Table 4.18: Loss energies (J/m³) per pulse according to specifications of Table 4.17

<table>
<thead>
<tr>
<th>$\Delta B$</th>
<th>Nano-crystalline 500F</th>
<th>Amorphous (2605SA1)</th>
<th>SiFe3% (100µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25</td>
<td>0.21</td>
<td>0.77</td>
<td>2.52</td>
</tr>
<tr>
<td>0.5</td>
<td>0.85</td>
<td>3.16</td>
<td>11.28</td>
</tr>
<tr>
<td>0.75</td>
<td>1.94</td>
<td>6.42</td>
<td>26.10</td>
</tr>
<tr>
<td>1</td>
<td>3.21</td>
<td>10.71</td>
<td>45.13</td>
</tr>
<tr>
<td>1.25</td>
<td>4.86</td>
<td>15.44</td>
<td>66.20</td>
</tr>
<tr>
<td>1.5</td>
<td>6.32</td>
<td>20.58</td>
<td>91.95</td>
</tr>
<tr>
<td>1.75</td>
<td>8.01</td>
<td>25.53</td>
<td>119.79</td>
</tr>
<tr>
<td>2</td>
<td>9.26</td>
<td>31.36</td>
<td>160.80</td>
</tr>
<tr>
<td>2.25</td>
<td>9.72</td>
<td>36.83</td>
<td>197.65</td>
</tr>
<tr>
<td>2.5</td>
<td>-</td>
<td>44.49</td>
<td>238.39</td>
</tr>
<tr>
<td>2.75</td>
<td>-</td>
<td>51.62</td>
<td>289.51</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>60.95</td>
<td>340.40</td>
</tr>
<tr>
<td>3.25</td>
<td>-</td>
<td>-</td>
<td>409.13</td>
</tr>
</tbody>
</table>

Peak electrical field for arbitrary winding geometries

In order to obtain a suitable transformer design, the procedure must be equipped with an electrical field model, which is accurate and fast enough to be evaluated within an optimization cycle. In order to achieve these two requirements an analytical electrical field model based on the 2D-charge simulation method (CSM) is implemented [99]. Grounded surfaces, such as the tank wall, can be considered in the CSM by charge mirroring [81]. For the sake of speed, the electrical field is only calculated on the conductor surfaces of the secondary winding. In order to reach high accuracy, 16 contour points per secondary turn are considered. Detailed description of the applied method is given in [102]. The peak electrical field is compared to 2D-FEM, reaching deviations smaller than 5%.

With the chosen approach, the procedure is able to derive and limit the maximum peak electrical field on each conductor. In order to check the design result, not only the resulting peak electrical field must be limited, but also the most critical electrical field path of the resulting
Isolation distance examination

In a high voltage transformer, breakdown mechanisms depend on many parameters and influences. Since in most cases there only exists breakdown data for small gaps under certain excitations, in this paper a procedure is presented which adapts available breakdown data to a real size pulse transformer. The procedure is depicted in Fig. 4.49. At first, a method is presented which allows a scaling from standard breakdown data to a given pulse shape. Thereafter, the adaption of the breakdown data to high withstand probabilities at an increased volume is described. Additionally, a method is presented how inhomogeneous electrical fields occurring in the design can be evaluated. Finally, a transformer design with specifications of CLIC is compared to scaled breakdown data of mineral and ester oil.

Pulse shape

The most investigated voltage impulse shapes are the switching impulse (SI) and the lightning impulse (LI). In [123] non-standard LI waveforms were investigated for pulses with different lengths. It was found that the breakdown voltage does not correlate with the wavefront time, but with the time the pulse exceeds a certain voltage. The highest correlation resulted when voltages up to 80% of the crest value were considered. Therefore, in order to obtain a comparative measure, the voltage time product ($VT$) is applied described by

$$VT = \int_{t_1}^{t_2} V(t) dt,$$

$$t_1 = (V = 0.8 \cdot V_{max} \land \frac{dV}{dt} > 0),$$

$$t_2 = (V = 0.8 \cdot V_{max} \land \frac{dV}{dt} < 0) \quad (4.85)$$

$$SF_{(SI/LI)} = \frac{V_{br(SI/LI)}}{V_{br,pulse}}. \quad (4.86)$$

where $V(t)$ is the time-dependent pulse voltage and $V_{max}$ the crest value of the pulse. SI and LI of ester and mineral oil have been compared for a 3.8mm-gap with standard sphere-sphere electrodes applying the standard ASTM D 3300 method, listed in Table 4.19 [112]. $VT$ values of SI and LI are interpolated to obtain the mean breakdown voltage of
Figure 4.49: Isolation distance examination: The most critical field path is compared to scaled switching impulse (SI) and lightning impulse (LI) breakdown data on its entire path length.

the desired pulse shape as well as a scaling factor $SF$. Since the $VT$ of the desired pulse shape is closer to the $VT$ of the lightning impulse, the breakdown data from [124] and [112] is applied with the corresponding $SF_{LI}$ in the following sections for the negative lightning impulse since a klystron is connected as load.

**Volume effect and withstand probability** To derive a breakdown probability for a given voltage, breakdown data is approximated with
Table 4.19: Comparison of SI, LI and investigated pulse shape (breakdown data from [112]).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LI</th>
<th>SI</th>
<th>pulse</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{max}}$ (kV/mm)</td>
<td>180</td>
<td>180</td>
<td>180</td>
</tr>
<tr>
<td>Rise time ($\mu$s)</td>
<td>1.2</td>
<td>250</td>
<td>5</td>
</tr>
<tr>
<td>Time to half value of wave tail ($\mu$s)</td>
<td>50</td>
<td>2500</td>
<td>-</td>
</tr>
<tr>
<td>Voltage time product ($VT$) (Vs)</td>
<td>1.72</td>
<td>157</td>
<td>27</td>
</tr>
<tr>
<td>$V_{\text{br},50%}$ (ester) (kV/mm)</td>
<td>208.8</td>
<td>169.2</td>
<td>207.3</td>
</tr>
<tr>
<td>$V_{\text{br},50%}$ (mineral) (kV/mm)</td>
<td>243.9</td>
<td>184.3</td>
<td>234.2</td>
</tr>
<tr>
<td>$SF_{(SI/LI)}$ (LI, SI to pulse) (ester)</td>
<td>-</td>
<td>1.007</td>
<td>0.816</td>
</tr>
<tr>
<td>$SF_{(SI/LI)}$ (LI, SI to pulse) (mineral)</td>
<td>-</td>
<td>1.041</td>
<td>0.787</td>
</tr>
</tbody>
</table>

a Weibull distribution [109]

$$P(V) = 1 - \exp \left( -\frac{V}{\alpha} \right)^\beta,$$  \hspace{1cm} (4.87)

which is dependent on the scale parameter $\alpha$, the shape parameter $\beta$ and the applied voltage $V$. Since the geometry scale in breakdown tests is much smaller than in the real size transformer the volume effect has to be considered. The withstand probability of a volume, which is $n$-times a given volume $V_1$, is obtained by [125]

$$1 - P_n = (1 - P_1)^n,$$ \hspace{1cm} (4.88)

where $P_1$ is the breakdown probability for the given volume $V_1$ and $P_n$ is the breakdown probability for a volume of size $n \cdot V_1$. The breakdown probability of a volume, which is $n$-times the tested one, can therefore be described by [125]

$$P_n(V) = 1 - \exp \left[ -\left( \frac{n \cdot V_1}{\alpha} \right) \right]^\beta$$ \hspace{1cm} (4.89)

In order to adapt the small scale breakdown data to the given transformer geometry, the affected volume must be derived and a desired breakdown probability must be selected. With these parameters maximum electrical field values $E_{\text{max}}$ for the chosen transformer geometry
dependent on the gap distance can be derived. In [112] a 1% breakdown probability is proposed as a design criteria, which is also applied in this paper. Since in this application a unipolar pulse is applied, the high electrical field only occurs in a small part of the transformer volume, which is then considered as the affected volume. The considered volume is further described in section 4.7.3.

Inhomogeneous electrical fields In pulse transformers, the electrical field is inhomogeneous in many cases. To reduce the inhomogeneity field stabilizers are used to lower the peak electrical field usually occurring at the turn with the highest voltage potential. In the optimization procedure a geometry is investigated, in which the secondary turn at the highest voltage potential is realized as field stabilizer by increasing its radius. Even though the peak electrical field is reduced by stabilizers, the resulting electrical field of the geometry remains inhomogeneous to a certain extent.

In order to achieve a compromise between an excessive peak electrical field and an overly conservative design, a method is applied proposed in [109], which calculates the mean electrical field for different intervals along the oil gap length. The resulting electrical field $E_m$ can be
described by

\[ E_m(z) = \frac{1}{z} \int_{x_1}^{z} E(z') \, dz', \] (4.90)

where \( x_1 \) is the beginning of the oil gap, \( E(z') \) is the electrical field at point \( z' \) and \( z \) is the the interval length of the investigated path. This resulting \( E_m \) must remain below the desired maximum value \( E_{max} \) for homogeneous electrical fields for the entire interval length. In the following section a transformer design is examined with the proposed method depicted in Fig. 4.49.

**Application in high voltage pulse transformer design**

In order to check the isolation distance of a transformer design, the optimization procedure is applied with specifications of CLIC (Table 4.20) with a maximum peak electrical field at the conductor surface of \( E_{peak} = 10 \text{kV/mm} \). The resulting geometry is analyzed with 2D-FEM and depicted in Fig. 4.50a), which derives an peak electrical field value equal to the procedure’s value. The zoomed view of the picture shows that the peak electrical field occurs on top of the field shape ring, which is in this case the secondary turn with the highest potential. The red line in Fig. 4.50a) indicates the most critical field path \( E_{crit} \) of the transformer design. Most of the transformer volume is only subjected to electrical fields smaller than \( E = 5 \text{kV/mm} \) and therefore is not considered as affected volume. For safety reasons, the entire area indicated in the green rectangle in Fig. 4.50a) is taken into account for calculating the affected volume, assuming that all field paths in this area are equal to the most critical one \( E_{crit} \). In Fig. 4.50b) \( E_{crit} \) and \( E_m \) (4.90) are depicted for \( E_{peak} = 10 \text{kV/mm} \). They are compared to the scaled breakdown data of mineral and ester oil for gap lengths of 3.8-150 mm (4.89) leading to \( E_{max} \) curves. Scaled \( E_{max} \) values of the 3.8 mm-gap are used as upper limit to avoid data extrapolation. In both cases the calculated \( E_m \) remains below the maximum electrical field \( E_{max} \). Additionally, a design was investigated with CLIC specifications and a maximum peak electrical field limitation of \( E_{peak} = 12 \text{kV/mm} \). The resulting most critical field path, also indicated in Fig. 4.50b), intersects with the \( E_{max} \)-curve of natural ester, but not with the mineral oil curve. Therefore, higher peak electrical fields and thereby smaller isolation distances can be applied if mineral oil is selected in the design.
Table 4.20: Selected specifications of the compact linear collider (CLIC). Nominal values are underlined.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse voltage range</td>
<td>$V_{kn,\text{range}}$</td>
<td>150 ... 160 ... 180</td>
<td>kV</td>
</tr>
<tr>
<td>Pulse current</td>
<td>$I_{kn,\text{range}}$</td>
<td>193 ... 181 ... 161</td>
<td>A</td>
</tr>
<tr>
<td>Primary voltage range</td>
<td>$V_{\text{prim,range}}$</td>
<td>2.5 ... 2.66 ... 3</td>
<td>kV</td>
</tr>
<tr>
<td>Primary current range</td>
<td>$I_{\text{prim,range}}$</td>
<td>11.6 ... 10.86 ... 9.66</td>
<td>kA</td>
</tr>
<tr>
<td>Load range (eq. $R$)</td>
<td>$R_{\text{load,range}}$</td>
<td>777 ... 883 ... 1118</td>
<td>Ω</td>
</tr>
<tr>
<td>Required power</td>
<td>$P_{\text{out}}$</td>
<td>29</td>
<td>MW</td>
</tr>
<tr>
<td>Rise + settling time</td>
<td>$t_{\text{settle}}$</td>
<td>8</td>
<td>μs</td>
</tr>
<tr>
<td>Flat-top length</td>
<td>$t_{\text{flat}}$</td>
<td>140</td>
<td>μs</td>
</tr>
<tr>
<td>Flat-top stability</td>
<td>$FTS$</td>
<td>0.85</td>
<td>%</td>
</tr>
<tr>
<td>Highest overshoot</td>
<td>$os$</td>
<td>1</td>
<td>%</td>
</tr>
<tr>
<td>Total efficiency</td>
<td>$\eta_{\text{ges}}$</td>
<td>90</td>
<td>%</td>
</tr>
</tbody>
</table>

4.7.4 Sensitivity analysis

Optimization procedures allow the designer to evaluate the sensitivity of system parameters. The reference pulse transformer complies with the CLIC specifications listed in Table 4.20. The isolation distances are adapted to the specified maximum voltage $V_{\text{max}} = 180$ kV, even though the pulse shape is optimized for $V_{kn} = 160$ kV. Due to the primary current of $I_{\text{prim}} \leq 10$ kA at least four switching units are required and since the system complexity should be minimized, the number of magnetic cores is chosen to $N_c = 2$.

In the following sections, the sensitivity of the core material, the number of primary turns, the transformer oil and the high voltage cable length is investigated.

Core material sensitivity

In order to compare the three investigated core materials in a design, the optimization procedure was set to maximize the efficiency without any volume constraints and the number of primary turns was fixed to $n_{\text{prim, min}} = 4$ to obtain equal flux swing when choosing an equal cross sectional area of the core.

The optimization results are listed in Table 4.22. For the nanocrystalline and the amorphous material, the procedure selects a high flux density, whereas with silicon iron only 75% of the possible flux density
Table 4.21: Pulse transformer data

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volume tank (m$^3$)</td>
<td>0.91</td>
</tr>
<tr>
<td>Critical affected volume (m$^3$)</td>
<td>0.033</td>
</tr>
<tr>
<td>Peak electrical field calc (kV/mm)</td>
<td>10</td>
</tr>
<tr>
<td>Peak electrical field 2D-FEM (kV/mm)</td>
<td>10</td>
</tr>
<tr>
<td>Field shape ring diameter (mm)</td>
<td>12</td>
</tr>
<tr>
<td>Oil gap (mm)</td>
<td>52</td>
</tr>
</tbody>
</table>

is selected. This effect is due to the significantly higher core losses of silicon iron. Therefore, the total efficiency of the transformer is reduced by almost 1%. Even though the nanocrystalline material shows lower core losses by factor 2.5, its transformer efficiency does not exceed the one of the amorphous material. This is due to the fact that the share of the core losses is smaller than 10% for both materials. Since the maximum flux density of the nanocrystalline material is smaller than the one of the amorphous material, the resulting transformer volume is increased. The increased volume results in higher $L_\sigma$, thereby extending the rise time. This effect lowers the pulse efficiency, which overcompensates the lower core losses. Therefore, for CLIC specifications, the amorphous core material is identified as the most suitable and will be selected in all further analyzes.

**Primary turn selection**

In the previous section the optimization procedure was applied for maximizing the efficiency. In the design process, however, a compromise between highest efficiency and smallest volume has to be achieved. Therefore, the procedure was adapted to minimize the volume for a given efficiency limit. The efficiency limit is then varied, resulting in a Pareto front.

In order to determine the number of primary turns, the Pareto front of a transformer design with three primary turns was compared to a design with four primary turns. The comparison is depicted in Fig.4.51. In case of three primary turns the efficiency is marginally higher than for four turns. The drawback of that solution is the usage of more core material, which results in higher system weight and in higher costs.
**Table 4.22:** Comparison of Core Materials with Specifications of CLIC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Nanocrystalline (VITROPERM 500F)</th>
<th>Amorphous Metglas (2605SA1)</th>
<th>SiFe3% (100µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{flattop}$ (µs)</td>
<td>4.77</td>
<td>4.36</td>
<td>4.53</td>
</tr>
<tr>
<td>Transformer volume (m³)</td>
<td>1.57</td>
<td>1.05</td>
<td>1.04</td>
</tr>
<tr>
<td>$B_{ex}/B_{max}$ (%)</td>
<td>95</td>
<td>100</td>
<td>75</td>
</tr>
<tr>
<td>Core losses $P_{core}$ (kW)</td>
<td>0.184</td>
<td>0.482</td>
<td>2.28</td>
</tr>
<tr>
<td>Total losses $P_{tot}$ (kW)</td>
<td>5.92</td>
<td>5.37</td>
<td>8.45</td>
</tr>
<tr>
<td>$B_{ex}$ (T)</td>
<td>0.95</td>
<td>1.2</td>
<td>1.1250</td>
</tr>
<tr>
<td>Core volume (m³)</td>
<td>0.35</td>
<td>0.2391</td>
<td>0.2545</td>
</tr>
<tr>
<td>Total core weight (T)</td>
<td>2.57</td>
<td>1.71</td>
<td>1.952</td>
</tr>
<tr>
<td>System efficiency (%)</td>
<td>96.82</td>
<td>96.93</td>
<td>96.0</td>
</tr>
</tbody>
</table>

**Figure 4.51:** Comparison of Pareto fronts with 3 and 4 primary turns.

of the transformer. Therefore, the number of primary turns is set to $n_{prim} = 4$ for the considered design.
Transformer oil sensitivity

In modulator systems there is an increasing demand to replace mineral oil with more environmentally friendly oils such as natural esters. Therefore, the influence of such an oil replacement is investigated. In addition to the distributed capacitance of the transformer $C_d$, the high voltage cable length connecting the transformer to the klystron load is taken into account with a length of $l_{HV} = 1.5$ m, resulting in an additional capacitance of $C_{d,cable} = 153$ pF. Also an additional capacitance of $C_{add} = 100$ pF due to klystron tank and high voltage divider is assumed.

In a first comparison, equal isolation distances are applied for both oils ($E_{\text{max}} = 10$ kV/mm). The oils still differ in their relative permittivity ($\epsilon_{r,\text{mineral}} = 2.2$, $\epsilon_{r,\text{ester}} = 3.2$). In order to reach highest pulse efficiency, i.e. the ratio between the entire pulse and the part of the pulse which complies with the flat-top criteria, a critical damped pulse is required. Therefore, the procedure matches the distributed capacitance $C_d$ and the leakage inductance $L_\sigma$ for a given set of external constraints. The results are displayed in Fig.4.52 which show that for mineral oil a higher volume is needed at lower efficiencies. The mineral oil curve only slightly surpasses the one of ester oil for volumes higher than $V = 0.88$ m$^3$. The lower $\epsilon_r$ and therefore the lower $C_d$ of mineral oil is not beneficial, since it would also require a reduced $L_\sigma$ for an efficient rise time. Since the winding distance cannot be reduced due to the required isolation distance, $L_\sigma$ can only be decreased by increasing the height of the winding, which leads to a higher transformer volume.

In a second step, the maximum electrical peak field is set for mineral oil to $E_{\text{max}} = 12$ kV/mm (c.f. section 4.7.3). In this case, the isolation distances can be decreased, which leads to a better match between $L_\sigma$ and $C_d$ and therefore to an efficiency increase of 0.5%.

Since for the CLIC system the usage of mineral oil is a concern, the efficiency decrease is accepted and the natural ester oil is selected.

HV cable length selection

Since the klystron load is placed in a separate oil tank, the influence of a high voltage cable length is investigated. The additional cable length leads to an increased $C_d$ and therefore has to be considered in the design by increasing the leakage inductance. Since a halogen free cable is required, the $C2236/LS$ is selected with specifications listed in
Table 4.23 Both oils are investigated with a minimal cable length of $d_{\text{min}} = 1.5\, \text{m}$ and compared with a cable length of $d_{\text{max}} = 5\, \text{m}$, which was specified to be the maximal distance to the klystron load. The results are depicted in Fig. 4.53. For both oils the additional cable length leads to an efficiency decrease of 0.6%. In case of the mineral oil the lower $C_d$ due to the lower $\epsilon_r$ can almost compensate the additional cable capacitance and results in a similar curve than ester oil with a short cable length. As could be expected the shortest cable length results in the highest efficiency and therefore is chosen for CLIC. This investigation is performed to show the influence of constructional limitations which would require a certain HV cable length. Even though the performance decreases with a higher cable length, the highest possible efficiency can be achieved, if the cable length is considered in the pulse transformer design process.

4.7.5 Performance evaluation

In the previous chapter a sensitivity analysis has been performed. For CLIC a pulse voltage range is specified with a desired optimal voltage, which is underlined in Table 4.20. Therefore, in a first step a design for

Figure 4.52: Pareto limit of pulse transformer with 1) ester oil with $E_{\text{max}} = 10\, \text{kV/mm}$ 2) mineral oil with $E_{\text{max}} = 10\, \text{kV/mm}$ and 3) mineral oil with $E_{\text{max}} = 12\, \text{kV/mm}$.
Figure 4.53: Pareto limit of pulse transformer with 1) ester oil and \(l_{HV} = 1.5\) m, 2) ester oil and \(l_{HV} = 5\) m, 3) mineral oil and with \(l_{HV} = 1.5\) m and 4) mineral oil and \(l_{HV} = 5\) m.

...the required optimal voltage is selected on the Pareto front. In a second step the chosen design pulse shape is evaluated for the entire specified load range.

CLIC design selection

In order to provide the desired pulse voltage range flexibility listed in Table 4.20, the designed transformer must respect the highest possible current \(I_{\text{max}}\) as well as the highest possible voltage \(V_{\text{max}}\). Since the primary voltage of the used IGBT modules is limited to \(V_{\text{prim, max}} = 3\) kV, the turns ratio is defined to \(n = 60\). The isolation distances of the transformer as well as the cross sectional area of the core have to be adopted to \(V_{\text{max}}\). The windings in contrast have to be designed for \(I_{\text{max}}\). In Fig. 4.54(a) the Pareto front for the desired voltage is depicted. In order to respect the high efficiency requirement of the entire modulator system, a transformer efficiency value (including pulse efficiency) close to \(97\%\) is selected, which is indicated on the curve. The resulting pulse transformer is depicted in Fig. 4.54(b).
Table 4.23: High voltage cable specifications (C2235/LS)

<table>
<thead>
<tr>
<th>Outside diameter</th>
<th>38.23</th>
<th>mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Impedance</td>
<td>61</td>
<td>Ω</td>
</tr>
<tr>
<td>Capacitance</td>
<td>102</td>
<td>pF/m</td>
</tr>
</tbody>
</table>

Pulse shape analysis for the entire load range

A flexible load range does not only require an adaption of the transformer geometry, but also influences the pulse shape. During the rise time of the pulse, the damping for a resistive load $R_l$ can be described by

$$d \sim \frac{1}{2R_L} \cdot \sqrt{\frac{L_\sigma}{C_d}},$$

where $L_\sigma$ is the leakage inductance and $C_d$ the distributed capacitance. Smaller loads therefore result in higher damping. Since the possible load change is higher than 40%, the pulse shape is affected significantly and it is not possible to design a transformer, which complies with the tight specifications of Table 4.20 in the entire load range. The resulting pulse shapes for the optimized voltage and the minimum and maximum voltage with a klystron load are depicted in Fig. 4.55. It shows that in the 180 kV-case the pulse is under-damped with an over-
**Figure 4.55:** Comparison of pulse shapes of a 180 kV-, 160 kV-, and 150 kV-pulse with klystron load and a pulse transformer optimized on $V_{kn} = 160$ kV.

shoot of $os_{180kV} = 6.5\%$ and the pulse meets the flattop criteria after $t_{flat,180} = 8\, \mu s$, whereas in the 150 kV-case the pulse is over-damped and the flattop criteria is met after $t_{flat,180} = 9\, \mu s$. In case of the minimum voltage a longer HV cable could be chosen to reduce the damping and therefore reduce the rise time. In case of the highest voltage a klystron must be chosen which can cope with the higher overshoot or additional measures have to be taken such as a reduction in switching speed of the IGBTs.

### 4.7.6 Conclusion

In this paper, an enhanced pulse transformer optimization procedure is presented. The procedure controls the electrical peak field in the entire geometry. It is explained how the isolation distances in pulse transformers can be checked by scaling breakdown data from standard LI or SI tests. With the procedure, the influence of the number of primary turns, the core material, the transformer oil and high voltage cable length on the transformer design are investigated by identifying the Pareto limits. It is demonstrated that amorphous core material
is most suitable for CLIC specifications. Additionally, is it shown that replacing mineral oil with natural ester decreases the efficiency by 0.5% and a 3.5 m longer high voltage cable length results in an efficiency reduction of 0.6%. Finally, a transformer design optimized for 160 kV is selected and the pulse shape is analyzed for the entire load range. The investigation shows that in the 180 kV-case the overshoot is $os_{180\text{kV}} = 6.5\%$ and the time to flattop $t_{flat,180} = 8 \mu s$, whereas in the 150 kV-case an overshoot $os_{150\text{kV}} = 0\%$ with a time to flattop of $t_{flat,150} = 9 \mu s$ results.

**Acknowledgment**

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5

Pulse power modulator system

In the previous chapters, the three major parts of the pulse modulator system have been described: the medium voltage charging system, the droop compensation system, consisting of four pulse units, and the pulse transformer. In this chapter, the communication system for the different components is presented, as well as their assembly to a final modulator system.

5.1 Modulator communication structure

In this paragraph, the modulator communication structure is briefly presented. At first, the high level communication structure is shown, followed by the central pulse control unit and the capacitor charging control unit.

5.1.1 Central communication structure

The central PLC is situated in the capacitor charging rack. The high level communication is based on the EtherCAT (Ethernet for Control Automation Technology) protocol from BECKHOFF. The different components of the modulator system are connected to the central unit in two separate control channels, which are depicted in Fig. 5.1. The first control channel addresses the central pulse control unit and each of the 24 bouncer modules. In the second channel, the AC-DC source and the capacitor charging control unit are connected. The individual capacitor charging units are not integrated in the high level communication structure, since their relevant operation data is provided by the
Figure 5.1: Central PLC communication structure, which consists of two communication channels. The first channel controls the central pulse control unit and all 24 bouncer modules. In the second channel, the AC/DC source and the capacitor charging control unit are addressed. Furthermore, the auxiliary supply, cooling fans and safety relays are controlled.

Visualization of modulator system

In order to facilitate the manual control of the modulator system, the central PLC is equipped with a human interface, which visualizes the different components described in the previous section. The submodules are grouped in different tabs, depicted in Fig. 5.2, which reduces the amount of visible information at a time. Since a lot of data is exchanged, especially for the bouncer submodules, only a single bouncer module is displayed at a time. In order to be able to equally change data of several bouncer modules, a copy target function is implemented, which stores the desired changes. From the copy target the new values can then be transferred to a different bouncer module or to all modules.

5.1.2 Central pulse control unit

The central pulse control unit monitors the modulator operation during the pulse period. Its communication structure is visualized in Fig. 5.4 a). In order to be able to react fast on an occurring system fault and to be robust against noise, plastic optical fibers are used for communication within the system. Thus, four optical fibers are connected per bouncer module, in addition to the EtherCAT link. Also,
the four switching units are optically linked, consisting of a main pulse and a magnetization switch. Additionally, four voltage measurements are connected via a 125 MBit SFP link, allowing to control the primary voltage level of each pulse unit during the pulse interval. In order to react quickly on a voltage breakdown during the pulse phase in either the transformer or the klystron load, the secondary load current is monitored with an overcurrent and undercurrent threshold. Furthermore, to synchronize the modulator operation with the klystron load, an external trigger signal is received as well as several status signals are exchanged. Additionally, an optical link to the capacitor charging control unit is established, which is described in the next paragraph.

In order to cope with the high number of required optical ports and to allow flexibility in case of changes in the control structure, a backplane board was designed. This board allows to vertically insert interface cards, which provide the desired functionality. The design features a total number of 151 input and output pins, which includes 18 differential pairs. There are 20 slots for vertical interface cards.

Figure 5.2: Visualization of the general overview of the modulator system in the PLC. In total, there exist 6 different visualisation tabs of subcomponents.
Figure 5.3: Visualization of the bouncer submodule in the PLC. 35 different parameters can be adjusted and 3 different measurements can be displayed, which are recorded during the pulse interval. Since all 24 Bouncer modules feature equal control and feedback data, only a single module is displayed at a time. The desired bouncer module can be selected in a drop down menu.

5.1.3 Central capacitor charging control unit

The central capacitor charging control unit communicates via polymer optical fiber (POF) to all six capacitor charging units. Its communication interface was described in section 2.3.2. For this unit, the selected hardware is equal to the central pulse control unit depicted in Fig. 5.5, but with different communication cards. A schematic overview of the communication structure is depicted in Fig. 5.4(b). The central capacitor charging control unit features an optical link to the central pulse control unit besides the optical communication with the capacitor charging units. With this link, the charging is enabled and the voltage level can be switched between two voltage set points. The switching of the set point voltage is required, due to the combined recharging process of main capacitor bank and bouncer modules described in section 3.7.3.
Additionally, a *charging done* signal is transmitted to the central pulse control unit, when the desired capacitor voltage level is reached.

**Figure 5.4:** Communication structure of a) central pulse control unit b) central capacitor charging control unit.

**Figure 5.5:** Backplane design, which is applied for the central pulse control unit and the capacitor charging control unit. The design features a total number of 151 input and output pins, which includes 18 differential pairs. There are 20 slots for vertical interface cards available.
5.1.4 Modulator safety concept

The modulator safety concept includes three levels of protection. The first level present the safety features on each submodule, which are the capacitor charging units, the active bouncer modules and the pulse units. The second safety level is realized with both central control units, whereas the third level is executed with the central PLC. In the following, the different levels are explained in further detail.

Submodule based safety features

The safety features for each submodule type are different, which is why they are described for 1) the capacitor charging unit, followed by 2) the pulse unit and 3) the active bouncer module. A schematic overview of the modulator system with its involved measurements is depicted in Fig. 5.6.

1) Each capacitor charging unit is equipped with a temperature sensor, situated at the magnetic core of the inductor, with a current measurement as well as with an input and output voltage measurement. To detect an overvoltage (OV) at the output or an overcurrent (OC) in the inductor with a minimal time delay, analogue comparators are used with a fixed voltage reference. The comparators directly signal a surpassing of the given limits to the control board. Furthermore, there are in total ten faults that can be deduced from the onboard measurements by the FPGA control board, which are listed in tab. 5.1.

2) The pulse unit, described in section 4.2.8, features a gate control board per switch, which are connected via POF to the central pulse control unit. Each gate control board is equipped with a voltage measurement and a current measurement, which derives the current rate of change. The detectable errors are listed in tab. 5.2.

3) Each bouncer module features a temperature sensor, situated at the main heat sink, a current measurement as well as an input and output voltage measurement. To limit the inductor current, a comparator is applied with a variable DAC reference value. Eleven faults can be detected by the onboard control board, which are listed in tab. 5.3. Each bouncer module features an EtherCAT link to the central control unit, which transmits a collective fault signal. Since the EtherCAT cycle time is too slow to act within a single pulse interval, an intermediate safety level consisting of the two control units is required, which is faster addressable via POF. This safety level is explained in the fol-
Intermediate safety level features

The aim of the intermediate safety level is to distribute an error occurring in one of the submodules to all other active submodules. This task is executed by the central pulse control unit and the central capacitor charging unit. The communication to the corresponding submodules is realized in both cases via POF in a star connection. In addition, both central units are connected with each other via a POF-link to signal a collective fault of their submodules. This configuration allows a short reaction time of the modulator in case of an error occurring in a single submodule. Furthermore, the central pulse control unit is equipped with a voltage measurement per pulse unit, which supervises the primary DC voltage level. Additionally, a current measurement on the secondary side of the pulse transformer is integrated to detect a short


**Table 5.1:** Fault description of a single capacitor charging unit.

<table>
<thead>
<tr>
<th>Type of fault</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>On time</td>
<td>Switch is turned on too long</td>
</tr>
<tr>
<td>Off time</td>
<td>Switch is turned off too long</td>
</tr>
<tr>
<td>Current threshold</td>
<td>Current does not decrease after turn off</td>
</tr>
<tr>
<td>Input voltage</td>
<td>Input voltage time product deviates</td>
</tr>
<tr>
<td>Output voltage</td>
<td>Output voltage smaller than input voltage</td>
</tr>
<tr>
<td>Zero voltage switching</td>
<td>Measured voltages do not allow ZVS operation</td>
</tr>
<tr>
<td>Zero crossing polarity</td>
<td>Zero crossing measurement has wrong polarity</td>
</tr>
<tr>
<td>Over-temperature</td>
<td>Temperature limit exceeded</td>
</tr>
<tr>
<td>OV</td>
<td>Voltage limit exceeded</td>
</tr>
<tr>
<td>OC</td>
<td>Current limit exceeded</td>
</tr>
</tbody>
</table>


circuit during the pulse interval in the modulator or in the klystron load.

**Top level safety features**

The central PLC presents the highest safety level of the modulator system and therefore also provides the interface to human interaction. The different faults are visualized in a graphical surface. In case of an occurring fault, there are three possible system reactions. For less critical faults, e.g., *Next pulse unsure*, all submodules are simply turned off and the modulator awaits the re-enabling by the user. For more

**Table 5.2:** Fault description of a single gate control board of a pulse unit.

<table>
<thead>
<tr>
<th>Type of fault</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS</td>
<td>Power supply error</td>
</tr>
<tr>
<td>Over-temperature</td>
<td>Temperature limit exceeded</td>
</tr>
<tr>
<td>OC</td>
<td>Current limit exceeded</td>
</tr>
<tr>
<td>di/dt</td>
<td>Current rate of change too high</td>
</tr>
<tr>
<td>IC</td>
<td>Collector current detected after turn off</td>
</tr>
<tr>
<td>Turn on fault</td>
<td>$V_{ce}$ remains high after turn on</td>
</tr>
<tr>
<td>Turn off fault</td>
<td>$V_{ce}$ remains low high after turn off</td>
</tr>
</tbody>
</table>
**Table 5.3:** Fault description of a single active bouncer module.

<table>
<thead>
<tr>
<th>Type of fault</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Discharge fault</td>
<td>To much energy remains in output capacitor</td>
</tr>
<tr>
<td>Next pulse unsure</td>
<td>Output voltage still not discharged</td>
</tr>
<tr>
<td>Ramp up fault</td>
<td>Current increases to fast in ramp up interval</td>
</tr>
<tr>
<td>On time</td>
<td>High side switch is turned on too long</td>
</tr>
<tr>
<td>No voltage increase</td>
<td>No output voltage increase in pulse interval</td>
</tr>
<tr>
<td>Voltage increase</td>
<td>Output voltage increase too high</td>
</tr>
<tr>
<td>Over-temperature</td>
<td>Temperature limit exceeded</td>
</tr>
<tr>
<td>Undervoltage</td>
<td>Input voltage too low</td>
</tr>
<tr>
<td>OV input</td>
<td>Input voltage limit exceeded</td>
</tr>
<tr>
<td>OV output</td>
<td>Output voltage limit exceeded</td>
</tr>
<tr>
<td>OC</td>
<td>Current limit exceeded</td>
</tr>
</tbody>
</table>

Severe errors such as a secondary short circuit it is not sufficient to simply turn off all active modules. In this case the energy from the grid would continue to flow via the active rectifier into the point of the electrical short. Therefore, the entire modulator system can be disconnected from the grid with a main circuit breaker. In addition, the system must transfer in a safe state after an error, in which all remaining energy is removed. Therefore, discharge and grounding relays are attached at all relevant voltage levels (see Fig. 5.6), which are activated subsequently by a severe error or an emergency shutdown.
5.2 Modulator pulse to pulse repeatability

Since the pulse to pulse repeatability (PPR), defined in section 2.4, is an important specification for the CLIC modulator system, the different findings are summarized in this paragraph and the PPR of the overall modulator system is derived based on the conducted analyses.

In section 3.7.4 it was found that in order to achieve $PPR < 100$ ppm with high probability, the maximal standard deviation $\sigma_{tj,max}$ of the pulse voltage for any given point in time of the flattop interval has to be lower by a factor six, resulting in $\sigma_{tj,max} < 16.67$ ppm. In the analyses conducted in section 3.5 and section 3.7.4 a single pulse unit was investigated, neglecting the influence of the pulse transformer. The system requirement were derived for a primary voltage standard deviation of the pulse unit of $\sigma_{tj,pu} \leq \sigma_{tj,max}$. In the following, the extension from the PPR of a single pulse unit to the PPR of the overall modulator system is derived.

If all four pulse units were charged individually, all system parameters would be independent from another. Assuming the initial voltage and jitter distributions to be normally distributed with equal quantity for all four pulse units, the standard deviation of the secondary pulse voltage $\sigma_{tj,sec}$ results in

$$\sigma_{tj,sec} = \frac{n}{2} \sqrt{\sigma_{tj,Vbin(t=0)}^2 + \sigma_{tj,VMain(t=0)}^2 + \sigma_{tj,Shs+Scs}^2 + \sigma_{tj,Smain}^2}$$

$$= n \cdot \frac{\sigma_{tj,pu}}{2},$$

(5.1)

according to (3.44) and (3.43), where $n$ is the voltage ratio of the transformer. Since the secondary pulse voltage ($V_{sec} = n \cdot V_{pu}$) has to meet the PPR requirement, the demands on $\sigma_{tj,pu}$ can be relaxed by a factor of two. Yet, all main capacitors of the four pulse units are charged with a single charging system. Hence, the independence for $\sigma_{tj,VMain(t=0)}$ is not given and for this effect a reduction of factor two is not valid. However, for all other components in (5.1) independence can be assumed due to separate gate and measurement signals. Therefore, the influence of these components on the overall modulator’s output voltage is reduced by a factor of two in comparison to the previous findings in section 3.5 and section 3.7.4.

In section 3.5 it was found that applying the CMC control scheme the requirement on $\sigma_{tj,Vbin(t=0)}$ can be relaxed to $\sigma_{tj,Vbin(t=0)} \leq 3000$ ppm.
Since the influence of the switching jitters ($\sigma_{tj,Shs+Scs}$ and $\sigma_{tj,Smain}$) has already been determined to be minor in the analysis of a single pulse unit, the PPR of the modulator system will mostly be determined by the initial charging voltage distribution of the main capacitor bank. In section 2.5, a charging voltage repeatability analysis was conducted, which resulted in a charging voltage precision of 7.3 ppm. This high precision is achieved due to the high SNR of the output voltage measurement, the low transmitted charge in relation to the size of the capacitor bank and two subsequent charging cycles with independent measurement values. This result ($\sigma_{tj,max} = 7.3 \text{ ppm}$) offers a safety factor higher than two to the desired $\sigma_{tj,max} < 16.67 \text{ ppm}$.

It has to be stated, that even though noise and jitter measurements were included in the PPR analyses, the derived results were not validated with final output pulse voltage measurements. Also, neither the influence of the magnetizing interval (see section 4.2.6), nor the influence of the pulse transformer was considered in the analyses. However, the influence of these neglected components is expected to be minor. Additionally, effects which might occur in continuous high voltage operation were not considered, such as e.g., induced voltage spikes in the measurements due to switching operation or an unbalanced flat-top voltage. Such effects might deteriorate the result at first, but countermeasures can be applied to diminish their effect. For example, the influence of voltage spikes could be attenuated by an increased shielding of the involved measurement systems. The possible unbalanced flat-top voltage could be improved by fine tuning of the droop compensation system.

That’s the reason why in the authors opinion the conducted analyses clearly show how the different influences contribute to the PPR of the modulator system and which parameters would have to be improved, if the PPR had to be increased. Further, a first but solid prediction of the modulator’s PPR is provided, which states that the desired $PPR < 100 \text{ ppm}$ is clearly achievable with the designed modulator system.
5.3 Modulator system

The final assembly of the pulse transformer with its four pulse units is depicted in Fig. 5.7. The pulse switches are directly mounted on the transformer tank cover and are connected to the primary winding feed-throughs. In order to minimize the primary inductance of the assembly, the main capacitors, situated at the bottom of the stacks, as well as the active bouncer modules are connected via a bus bar to the pulse switches. On top of the bouncer modules the discharge relays are integrated, which also provide the HV-connections to the capacitor charging system. Above the discharge relays, the auxiliary supply is situated for all active components as well as the safety circuitry of the modulator system. On top of the pulse switches, the magnetization capacitors are mounted.
Figure 5.7: Assembly of the pulse transformer with its four pulse units. The pulse switches are directly mounted on the transformer top plate. On top of the bouncer modules are the discharge relays, the safety circuitry and the auxiliary supply situated.
6

Conclusion and Outlook

6.1 Conclusion

In this thesis, a high efficient pulse modulator system was designed that is capable of transmitting a 29 MW – 140 µs pulse for a broad range of loads. The system consists of three parts, which are the 240 kW medium voltage charging system, the active droop compensation system with a total number of 24 active bouncer modules and the pulse transformer.

For CLIC, a pulse with highly repeatable output voltage is crucial. Therefore, the charging source is required to provide a repeatable output voltage at the main capacitor bank while minimizing the distortion on the 400 V AC grid, induced by the pulsed operation. The applied medium voltage charging system consists of an AC/DC source and a 3 kV capacitor charging system. In order to be able to provide the required charging power, the capacitor charging system consists of six interleaved capacitor charging units operating in boundary conduction mode (BCM). BCM offers a zero voltage switching operation which reduces switching losses and allows to precisely control the transferred charge. At nominal power, a 96.3% conversion efficiency of a single capacitor charging unit was achieved.

In order to reach the repeatable output voltage, the capacitor charging system switches into single unit operation at the end of the recharging process. In this operation mode, the charge transmitted to the main capacitor bank per switching cycle reduces to a relative voltage increase of $\Delta V = 14 \text{ ppm}$. In this thesis, a charging precision analysis was conducted which considers the measurement noise and switching jitters of
CONCLUSION AND OUTLOOK

a single capacitor charging unit. Due to the small $\Delta V$ during the single operation mode, the charging analysis must consider subsequent charging cycles to provide reliable results. Therefore, the proposed charging precision analysis also includes the influence of subsequent charging cycles on the output voltage distribution. The analysis showed that a charging voltage with $\sigma_{V_{\text{out}}} = 22 \text{ mV} = 7.3 \text{ ppm}$ standard deviation is achievable.

Four pulse units, which are connected to the pulse transformer, provide the desired shape of the primary pulse voltage. In order to compensate the voltage droop of the main capacitor bank, an active droop compensation system, a so called bouncer system, was designed and tested. This bouncer system can cope with the fast required load current step of 12 kA within the pulse rise time. For the bouncer system, a modular approach was chosen, leading to 24 modules, distributed in groups of six over the four pulse units. The applied topology of a single bouncer module features a half bridge with an additional short circuit switch. With this topology, the required pulsed load current can be established prior to the pulse. The bouncer modules operate with the current mode control scheme (CMC). CMC offers an interleaved operation of modules by phase shifting of the turn-on instances. Since the bouncer system operates with a switching frequency of 100 kHz per module during the pulse, the voltage ripple on the output pulse is minimized. The bouncer inductance values show a small standard deviation of $\sigma_{L_{\text{rel}}} = 0.77 \%$. Therefore, with a six-fold interleaving per pulse unit, the output voltage ripple is reduced to the ppm range.

A repeatability analysis of a single pulse unit operated in CMC was conducted. The analysis revealed, that the precision of the bouncer modules’ input voltage can be relaxed by a factor of 20 in comparison to standard duty cycle control without feedback loop, keeping equal system repeatability. This effect is attributed to the error correction capability of the integrated current measurement in CMC operation. Due to the relaxation of the charging precision, the onboard voltage measurement of the bouncer modules can be applied for the recharging process, which simplifies the system complexity.

The pulse transformer is the third major component of the modulator system. Especially challenging is the time to flat top criteria for the given pulse length. In order to provide a high conversion efficiency and
an optimal pulse shape, a pulse transformer optimization procedure was developed in this thesis. The procedure is able to consider a broad range of core and winding geometries. The transformer parasitics are derived with accurate analytical approximations and the resulting pulse shape is controlled in the time domain. Applying the optimization procedure, the influence of important system parameters such as the selection of the core material and the behavior in dependency on the load range can be derived. The designed optimization procedure is applicable for high voltage pulse transformers for pulses in the broad range of $3 - 140 \mu s$. Additionally, the isolation distances of an optimized transformer design can be verified by a proposed method based on scaling of standard impulse breakdown data. The procedure has been validated with a full scale transformer prototype, where single pulses with 29 MW were demonstrated. A time to flat-top of $t_{\text{settle}} = 4 \mu s$ has been achieved with an ohmic load.

In summary, all different parts of the modulator system have been designed according to their demanding specifications and been tested individually at nominal voltage levels in a single pulse operation. Combining the repeatability analysis of the main capacitor bank’s voltage and the repeatability analysis of a pulse unit, a pulse to pulse repeatability of the modulator’s output voltage below 100 ppm can be derived.
6.2 Outlook

In this thesis, a 29 MW pulse modulator system was developed. All components of the final modulator system were designed, constructed and tested at nominal operation conditions in a single pulse operation. In the future, the final modulator system has to be tested in a continuous 50 Hz operation. Then, the predicted pulse to pulse repeatability of the overall modulator system derived from the repeatability analysis in this thesis can be verified by measurements.

This work presents the first pulse modulator prototype for investigating the CLIC acceleration concept. Since a high number of pulse modulators is required for the realization of CLIC, several improvements are proposed for a future modulator series. The realized modulator system was designed to operate in a broad load spectra, since several different klystron loads are under evaluation at CERN. The klystrons are situated in a separate oil tank connected via a HV cable. Once the optimal operation point of the klystron load is determined, the pulse transformer optimization procedure could be applied to re-evaluate the pulse transformer. The re-evaluation will increase the transformer’s efficiency and decrease its volume. Additionally, the klystron load could be integrated into the pulse transformer tank, thereby reducing the distributed capacitance $C_d$ of the design and the total system volume.

For the charging system as well as for the droop compensation system, a modular approach was selected. In order to increase the mean time between failure of the modulator system, additional modules could be employed, thus, leading to parallel redundancy. In case of a module failure, the affected module could simply be deactivated while the other modules continue to operate. The replacement of the affected modules could then be realized in predefined service intervals.

The droop compensation system offers a wide range of possible operating frequencies during the pulse, which is 50-120 kHz for a single bouncer module. The dependency of the modulator’s PPR on a variation in bouncer module operating frequency could be investigated to derive the optimal switching frequency. The active bouncer system is operated in open loop with CMC operation. Due to the optical communication link to the central pulse control unit, the control loop could be closed on the primary side by integrating the fast and repeatable voltage measurement system developed by CERN.
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Curriculum Vitae

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