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POST-ARC CURRENT MEASUREMENT IN MECHANICAL CIRCUIT BREAKERS FOR HVDC APPLICATIONS

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Abstract.
Post-arc currents contain valuable information on the breaker's performance. In this paper, the dimensioning procedure for a measurement system for such currents, based on a diode clamped shunt resistor is presented. Based on synthetic low and high power tests, the performance of a mock-up is evaluated. Finally, the post-arc current of a model gas circuit breaker, designed for use in DC applications, is measured.

Keywords: post-arc current, mechanical circuit breaker, small current measurement system.

1. Introduction

Mechanical gas circuit breakers are widespread in HVAC networks and may also be used as the mechanical component of HVDC switchgear. Due to the crucial role in the safe and reliable operation of electrical grids, a detailed investigation of their interruption behavior is of importance. The critical moment for interruption is the time around current zero. Measures like the arc resistance at or shortly before current zero as well as the post-arc current can be used to estimate the interruption capability of the tested breaker [1]. Hence, a precise measurement of the arc current around zero provides important information.

The main challenge for the measurement of post-arc currents is their low amplitude and short duration (air / SF_6: ≤ 20 / 1 A, ≤ 25 / 1 µs) compared to the fault current. In the past, a number of measurement systems have been introduced for this task [2–5]. These are based on different principles, such as Rogowski coils, resistive shunts in combination with pyrotechnic or semiconductor switches or the Faraday effect.

With recent improvements in semiconductor technology and digital data acquisition systems (DAQ), it has become easier and considerably more economic to assemble a post-arc current measurement system. This is especially interesting for the investigation of mechanical circuit breakers in HVDC breaker topologies. The smaller fault current level and drastically reduced arcing times allow for new, simpler constructions of such measurement systems. However, realizing a high bandwidth measurement system with sufficient accuracy in the desired low-current range still requires a sophisticated selection of components and design process.

2. Experimental setup

In this section, the realization of a small current measurement system (SCMS) as well as the used low and high power test circuits are described.

2.1. Measurement system

To precisely measure currents in the milliampere or single digit ampere range before and after a zero crossing, measurement systems are needed that limit the output signal during high current phases. One approach are systems based on a parallel connection of shunt resistors and anti-parallel diodes (cf. Figure 1) [4].

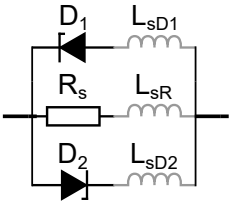

Figure 1. Measurement system consisting of a shunt (R_s) and two anti-parallel diodes (D_1, D_2) as well as corresponding paraisitic inductance (grey).

The anti-parallel connected diodes do not conduct significant amounts of current below a certain threshold voltage (forward voltage V_F). Consequently, the voltage across the measurement system can be considered proportional to the total current in a defined range $\pm I_0$ with:

$$I_0 = V_\mathrm{F}/R_\mathrm{s} \qquad \text{and} \qquad I_\mathrm{D}(V_\mathrm{F}) \leq x \cdot I_0\,, \quad (1)$$

where R_s is the selected shunt resistance, I_D is the forward biased diode current and x is the desired accuracy, e.g. 1%.

Once this voltage is exceeded, i.e. the current rises to a higher level, the forward biased diode will take over a larger and larger share of the current. This results in a drastically decreased rise of voltage, effectively limiting the output voltage of the measurement system. Due to this effect, the input range of the DAQ can be adjusted accordingly and the range around current zero can be recorded with increased accuracy.

Shunt resistance and diode threshold voltage can be selected to match the desired measurement range. The static voltage-current characteristic defines both the width of the measurement range ($\pm V_F$) as well as the clipping capability (forward slope resistance r_f, peak forward current). Additionally, the whole system needs to be suitable for high frequencies for a fast commutation of the current from and into the shunt (stray inductance, reverse recovery, package inductance). Often, a trade-off has to be made, as high power diodes are not suitable for high frequencies and vice versa. Due to high requirements regarding bandwidth and low output voltage of the system, it is of crucial importance to consider parasitic components and non-ideal behavior of diodes.

As the total current carrying capability of the system can be increased by a parallel assembly of multiple units, Schottky and fast recovery diodes are preferable to high power diodes. However, to avoid thermal runaway of parallel connected diodes, a considerable safety margin is important. If the application requires conducting very high currents, additional high power diodes in parallel may be necessary [4].

2.2. Test circuits

The presented measurement system can be realized in various ways, especially due to the large variety of available diodes. Hence, using separate testing methods for selecting suitable components and testing the complete system under realistic conditions is beneficial.

2.2.1. Low power testing

For a first evaluation of different types of diodes and system assemblies, a pre-charged, low voltage LC-circuit is used. It is tuned to a resonance frequency in the double digit kilohertz range and delivers currents that exceed the selected linear range of the assembly by at least a factor of five. Using this test setup, the maximum rate of rise of current can easily be adjusted to identify the dynamic limit performance of different types of diodes and assemblies. Due to the damping of the circuit, multiple current zero crossings with decreasing rates of rise of current (ROROC) are observed in each measurement. This allows to determine the performance of the system for different conditions. Once a suitable assembly is identified, it can easily be scaled up to the desired current level using parallel connections.

The main drawback of this test setup is that it is not possible to create currents with an amplitude similar to the expected currents of a circuit breaker test. Consequently, the diodes cannot be tested with the low-ohmic shunts that are used in real applications of the measurement system.

2.2.2. High power testing

Once a suitable diode configuration is identified, a verification of a scaled up version with a low-ohmic shunt and parallel connections of multiple diodes has to be performed. This can be done in a circuit breaker test bench, if the parameters of voltage and current can be adjusted sufficiently.

For this paper, a resonant circuit with a pre-charged capacitor is used (Fig. 2). After charging the capacitor C to the desired level, the test can be initiated by closing $AUX\ SW$. The current shape can be influenced by choosing proper values for L, C and the pre-charge voltage. The transient recovery voltage across the DUT is controlled by adjusting R_{TRV} and C_{TRV}. For further details and a description of the used model circuit breaker, refer to [6].

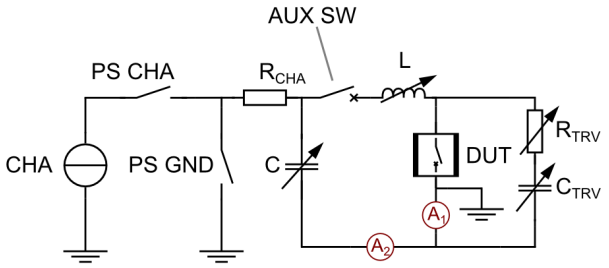

Figure 2. Schematic of circuit breaker test bench. A_1: SCMS, A_2: Reference (Pearson 4418).

3. Determining performance limits

3.1. Low power performance

Fig. 3 shows the signals of the reference current probe (Pearson 110) and the voltage across a SCMS test assembly, obtained during a low power test. The dotted line in Fig. 3 (b) represents a theoretical setup with perfect clipping behavior for currents above I_0.

For the SCMS test system, both the limited output signal during high current as well as the linear relation between current and output voltage during low current phases can clearly be seen. Due to the damped periodic test current, changes in the behavior for different ROROCs around zero can be observed. In this case, the tested combination of diodes and resistors shows a linear behavior for all tested ROROCs with a stable linear range of approximately $\pm 300\,mV$. However, the clamping behavior for higher currents is not very pronounced.

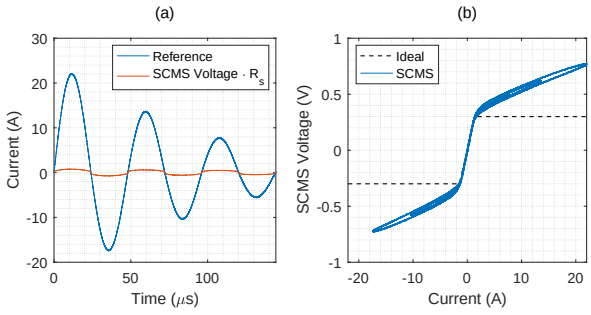

Figure 3. Example of reference current probe and SCMS signals as a function of time (a) and as a function of each other (b).

Using the described setup, tests have been conducted with a number of different assemblies including a variety of diode types (Schottky, FRED, different packages). In the following, the impact of undesired, non-ideal behavior of circuit elements is investigated. The measurements to illustrate them are obtained with modified setups to pronounce their impact on the behavior of the circuit.

3.1.1. Impact of parasitic inductance

Fig. 4 illustrates the measured voltage drop across the SCMS for two assemblies as a function of the reference current measurement. While the diodes used are identical for both setups, leads have been lengthened to artificially increase the parasitic inductance in the diode paths (a) and in the shunt path (b).

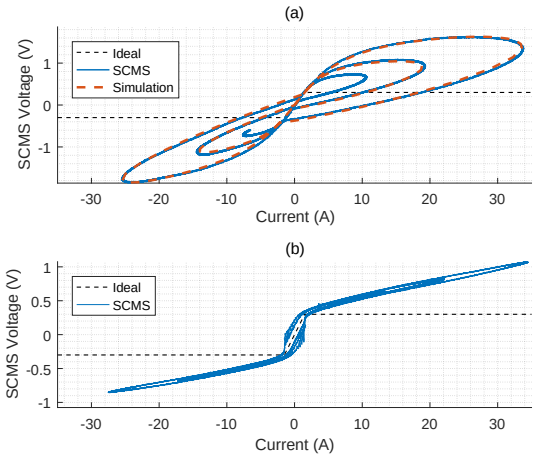

Figure 4. SCMS signal, using lengthened leads to increase inductance in (a) diode and (b) shunt paths.

The impact on the SCMS behavior can clearly be observed when comparing with Fig. 3 (b). In general, parasitic inductance causes an additional voltage drop in the respective branch, depending on both sign and absolute value of the ROROC. This leads to a decreased commutation speed out of and into the respective branch.

In case of the diode branch, for currents approaching zero this reduces the linear range of the measurement system as the current commutation into the shunt is delayed. In contrast, after zero crossing (i.e. the conditions of post-arc currents), the linear range is increased due to a slower commutation into the diode branch. The behavior of the circuit can be reproduced with good accuracy in a simplified simulation, only consisting of the RLC test circuit, simple diode models (V_F, r_F) and stray inductance (cf. Fig. 4 (a)). In this example, the parasitic inductance is considerably below 1 µH. When measuring a post-arc current, care has to be taken that the measurement range for the current approaching zero is large enough to extract ROROC or arc resistance shortly before zero. Hence, only the peak value of rate of rise of fault current before zero ($\mathrm{d}i/\mathrm{d}t_\mathrm{M}$) is of concern:

$$L_{\mathrm{D}\,1,2} < \frac{V_\mathrm{F}}{\mathrm{d}i/\mathrm{d}t_\mathrm{M}} \tag{2}$$

For the shunt resistor branch, the situation is quite different. As can be seen in Fig. 4 (b), the additional voltage drop impacts the linear measurement range. The combination of relatively low output voltage and high rates of change in current make this branch sensitive to the influence of stray inductance. For an error below 1% of the measurement range, the parasitic inductance limit can be in the nanohenry range. This requires high quality resistors and a suitable geometry of the assembly.

3.1.2. Impact of diode properties

In addition to stray inductance, semiconductor properties play an important role for the performance of the measurement system. On the one side, the static current-voltage characteristic of the diodes defines the linear measurement range as well as the clipping capability for high currents (cf. section 2). A series connection can increase the measurement range, however undesired dynamic effects increase correspondingly. On the other side, the bandwidth of the SCMS is influenced by the dynamic behavior of the selected diodes.

The commutation of current from the diode branches into the shunt is impacted by reverse recovery. As explained in section 3.1, this problem can be avoided with the use of either Schottky or fast recovery diodes with recovery times in the low two digit nanosecond range.

Forward recovery on the contrary impacts the commutation from the shunt branch into the diode branches, as the forward biased diodes take some time to become completely flooded with charge carriers. The effect can be seen in Fig. 5, where distinct peaks in the voltage across the SCMS are visible.

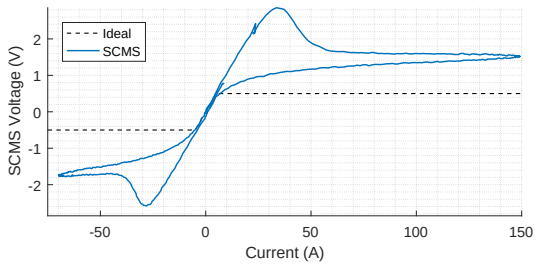

Figure 5. SCMS signal, using a diode with pronounced forward recovery characteristic as a function of reference current.

After recovery, the voltage drops back to the clamping level. While this effect does not impact the current measurement in the linear range, the over voltage due to forward recovery can reach significant levels. To remain in the measurement range of the DAQ and avoid damages to the recording equipment, diode data sheets should be consulted to estimate worst case forward recovery voltages.

3.2. High power performance

After evaluating different components with low power testing, a demonstrator SCMS was assembled to verify that findings can be transferred to high power levels. The system consists of 4 pairs of anti-parallel diodes, each with a 500 A surge current limit, and a 20 mΩ coaxial shunt resistor.

Results of a first high frequency, high current test are illustrated in Fig. 6. As can be seen from subfigure (a), even for high ROROCs, parasitic inductance in the diode branches (connection, package) is not a problem (cf. Fig. 4 (a)). For rates of change of current up to about 12 kA/ms, forward recovery is also negligible. In the zoomed area (subfigure (b)), only a slight overshoot can be seen for the higher ROROC.

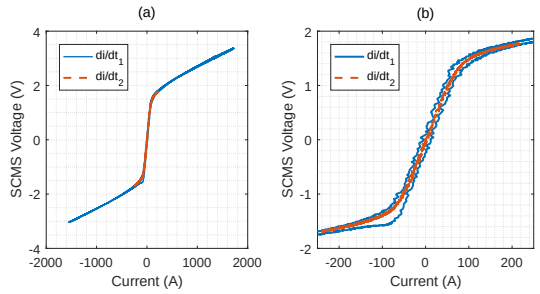

Figure 6. High power testing, peak ROROC: $\mathrm{d}i/\mathrm{d}t_1$*:* 11.8 kA/ms, $\mathrm{d}i/\mathrm{d}t_2$*:* 1.9 kA/ms*, (b) detail of (a).*

The limiting factor for performance in this case is the stray inductance in the shunt path. For 11.8 kA/ms, a hysteresis of the curve can be observed (cf. Fig. 4). Using this, the stray inductance can be estimated to about 28 nH. With a linear range of about 1.2 V, the mock-up can be used up to 2.1 kA/ms with less than 5% error, illustrating the scalability of the system.

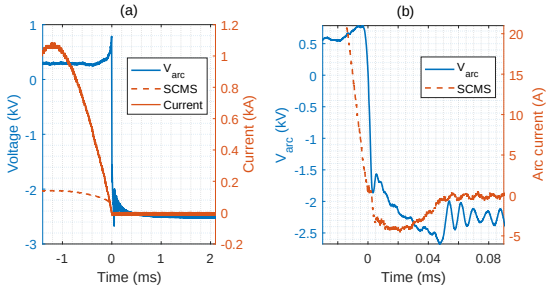

Figure 7. Post arc current measurement with SCMS

Finally, the demonstrator was used in an interruption test of a model gas circuit breaker. The breaker is used to investigate the behavior of mechanical switches as part of HVDC circuit breaker topologies [6]. To model the current as seen by the mechanical circuit breaker during interruption of DC faults, a high frequency oscillatory circuit is used. The breaker is designed for a medium voltage application and uses air at 6 bar as cooling medium.

Fig. 7 shows arc voltage and current (SCMS and reference current probe) of the complete measurement (a), as well as a close-up, illustrating the current zero crossing (b). A post-arc current with an Amplitude of about 4 A and duration of roughly 50 µs can clearly be seen. The signal is not filtered and still contains the capacitive current from the oscillation of circuit breaker stray capacitance and circuit inductance. However, as can be seen on the right-hand side of Fig. 7 (b), this is relatively small.

4. Conclusion

In this paper, dimensioning criteria for a shunt and diode based small current measurement system, suitable to record post-arc currents in high voltage circuit breakers, are discussed. Influencing factors are illustrated with measurements and impacts on measurement of post-arc currents are highlighted. Finally, a demonstrator is used to show the suitability of the dimensioning process.

The presented system has been scaled for the investigation of ultra-fast mechanical breakers, intended for DC systems. Hence, due to longer arcing times and higher fault current amplitudes, further up-scaling would be necessary for a use in HVAC systems. Sufficient bandwidth and sensitivity for measuring post-arc currents in SF_6 can be archived, however, verification tests are recommended.

To conclude, if basic rules are followed and parts are carefully chosen, a diode clamped shunt provides a high-precision, low-cost post-arc measurement system.

Acknowledgements

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