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Abstract

Reliability represents a very important factor for the design of Silicon Carbide (SiC) power metal oxide semiconductor field effect transistors (MOSFETs). Ruggedness of the device during abnormal operating conditions like the short circuit (SC) and avalanche conduction (during unclamped inductive switching - UIS) is an important aspect of reliability. Often, variation in design parameters to improve ruggedness during SC and UIS show negative impact on the nominal operating performance. This paper presents a comprehensive analysis of the impact of modification of p-base doping on the performance of a 1.2 kV SiC MOSFET during SC and UIS by means of TCAD simulations. The improvement in MOSFET ruggedness by optimizing the p-base doping and its influence on the nominal operating performance is evaluated.

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1. Introduction

The design of a SiC power MOSFET for a given current and voltage rating is optimized to have low on-state resistance ($R_{ds(on)}$) for maximizing the performance in the nominal operating conditions [1]. Design parameters such as cell pitch, channel length, doping of channel and JFET regions in the cell have influence on ruggedness during abnormal operating conditions like SC [2,3]. As current limitation is crucial during SC, most often design optimization for SC has a trade off with the on-state performance. Another design parameter that can be optimized for better SC ruggedness is the p-base region in SiC MOSFETs, which is emphasized in this work. The p-base doping (also called acceptor concentration N_a) is usually chosen in a way to achieve the desired threshold voltage, blocking capability avoiding reach-through breakdown and to achieve desired current conduction in the body-diode mode during nominal operating conditions [1]. Nevertheless, p-base doping below the N+source region influences the parasitic bipolar junction transistor (BJT) latch and thereby the ruggedness of the device under abnormal operating conditions like SC and UIS.

2. Mixed mode TCAD simulations

To simulate the SC and UIS, a half pitch cell of the MOSFET (a commercial 1.2 kV, 80 mΩ SiC MOSFET (C2M0080120)) operating at drain current I_d = 20 A with gate voltage V_{gs} = 20 V to turn-on and V_{gs} = -5 V to turn-off has been modelled using Synopsys Sentaurus structure editor and simulated to match the datasheet characteristics [4]. The simulations include the material parameters of 4H-SiC, an exponential trap distribution at the SiC/SiO_2 interface, mobility models to include surface degradation effect, doping dependence effect, high field saturation effect, and impact ionization model to include avalanche effects. The doping concentrations of the different regions of the MOSFET cell used to fit the datasheet characteristics are shown in Fig. 1. The static on-state characteristics match with the measurements at T = 300 K when the p-base doping is N_a = 1e18 cm^{-3}. Three test structures are designed using the structure editor by varying the p-base doping such as: reduced p-base doping, N_a = 5e17 cm^{-3} (referred as lowP), increased p-base doping N_a = 2e18 cm^{-3} (referred as highP), reference p-base doping N_a = 1e18 cm^{-3} (referred as Ref). The Gaussian implantation profile for a given depth, varying the p-base doping correspondingly varies the lateral doping profile along the channel which affects the V_{th}. The lateral doping profile is shown in Fig. 3. In addition, an optimized p-base doping with high p-base (N_a = 2e18 cm^{-3}) and low channel doping (N_a = 5e17 cm^{-3}) by counter doping is evaluated. The mixed mode simulation set ups for SC and UIS are shown in Fig. 1 and Fig. 8. These structures have been simulated for static on-state performance, dynamic switching performance, SC and UIS at initial temperature T = 300 K using the same simulation conditions and models. Thermodynamic transport model in Sentaurus sdevice has been used to compute the lattice temperature in the mixed-mode simulations.

3. Impact of p-base doping on SC

SC type 1 or a hard switching fault (HSF) is considered in this work. During a HSF event, drain bias equals to the dc-link voltage V_{ds} = 800 V (for 1.2 kV devices) at turn-on. Therefore, the device operates in the saturation region and I_d rises to more than 10 times the nominal operating current I_d = 20 A. Because of high currents and simultaneous high voltage, power dissipated in the device is very high leading to self - heating of the device and junction temperature rise [6].

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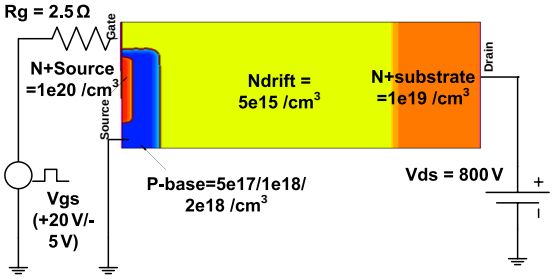

Fig. 1. Mixed mode SC simulation schematic.

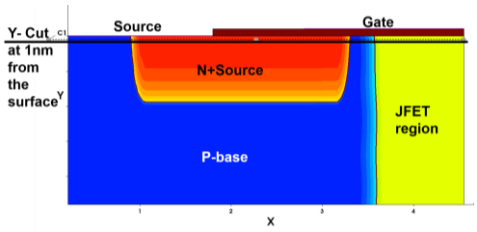

Fig. 2. Cross section showing the cut made to plot the doping profile in the half pitch MOSFET cell.

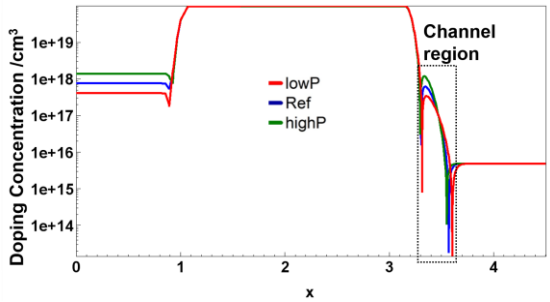

Fig. 3. Doping profile of the three test structures along the cut shown in Fig. 2.

As T increases, I_d initially increases (see Fig. 4) due to the positive temperature coefficient of mobility of the MOS channel until it reaches a peak and then starts to decrease due to the mobility reduction dominated by phonon scattering[7,8]. With low peak I_d, the heat dissipated in the device can be reduced, as the heat generated per unit volume in the device is the product of I_d and the applied voltage V_{ds} over the heat generation volume Δ (cm^3). Thus, the short circuit figure of merit depends on peak I_d and therefore minimizing I_d increases the short circuit withstand time (SCWT) as mentioned in [9]. When the three test structures were simulated for a given interface traps and mobility degradation models for HSF with a short circuit duration of t_{sc} = 5 µs with V_{ds} = 800 V and V_{gs} = 20 V, the peak I_d of highP is approximately 30 % lower than the Ref, while that of lowP is 15 % more than the Ref. The total current density in the cells at their respective peak I_d is shown in Fig. 5

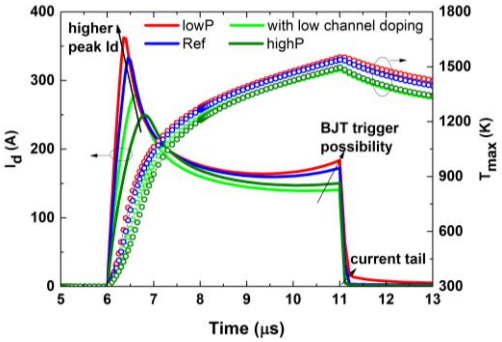

Fig. 4. SC I_d and T_{max} of the test structures with different p-base doping (V_{ds} = 800 V, V_{gs} = 20 V/-5 V, initial T = 300 K, t_{sc} = 5 µs).

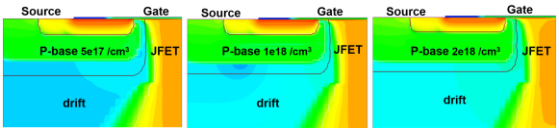

Fig. 5. Total current density at the time of peak Id with different p-base doping (scale in Fig. 6)

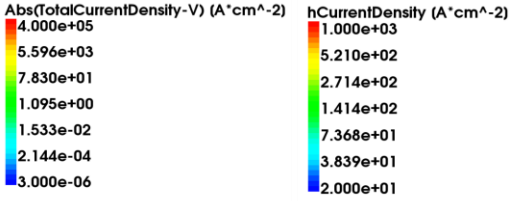

Fig. 6. Color scaling for Fig. 5 (Left) for Fig. 6 (Right).

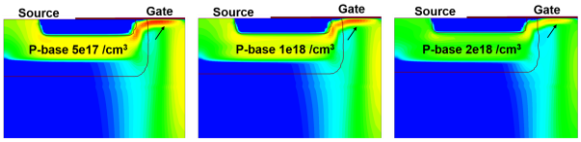

Fig. 7. Leakage currents at SC turnoff with different p-base doping (scale in Fig. 6).

where highP demonstrates low current density in the JFET region. Due to such low currents, the maximum temperature (T_{max}) reached during SC in highP is 150 K less than the temperature in the Ref structure (see Fig. 4). As the intrinsic carriers are generated by the local increase in temperature (critical temperature for SiC to generate intrinsic carriers T_{max} = 1500 K) in the JFET region, lower temperature means lesser leakage currents reaches [8]. Also, lowP has a higher resistance for the hole current flowing horizontally below the N+ source. Thus, the voltage drop necessary for N+source-p-base junction forward bias is achieved earlier leading to the turn-on of the parasitic BJT, which can be observed as the positive slope in the SC I_d in Fig. 4. The lower the p- base doping, the higher is the positive slope of the I_d. This

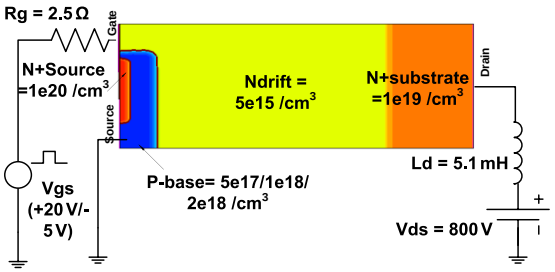

Fig. 8. Mixed mode UIS simulation schematic.

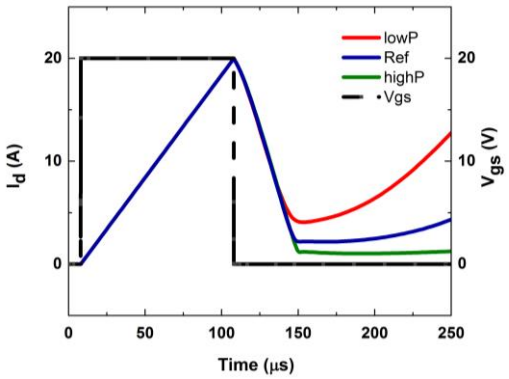

Fig. 9. UIS I_d curves with different p-base doping (V_{ds} = 800 V, V_{gs} = 20 V/-5 V, I_d = 20 A, L_d = 5.1 mH, E = 1.02 J, initial T = 300 K).

is because, more holes tend to move along the p-base region beneath the N+source to reach the source contact as seen in Fig. 7 favouring increase in voltage drop. The leakage currents in the device at SC turn-off for all the three structures are plotted in Fig. 7. The highP demonstrates lower leakage currents. The shielding of the N+ source region with higher p-base doping also reduces the leakage currents through the gate and field under the gate-oxide. Hence such a structure is more rugged limiting the gate-voltage reduction caused by the degradation of gate oxide [10].

4. Impact of p-base doping on UIS

During UIS (see Fig. 8), the current from the inductive load (L_d) conducts through the drain-source of the MOSFET after the gate is turned off. This forces the MOSFET to conduct in avalanche mode generating carriers for conduction via impact ionization [1] with an overvoltage across drain-source terminals. Here, L_d = 5.1 mH is first charged to a current of I_d = 20 A (energy E = 1.02 J) by turning on the MOSFET at V_{gs} = 20 V. Then, the gate is turned off, driving the DUT into avalanche conduction dissipating the stored energy onto the MOSFET. Fig.

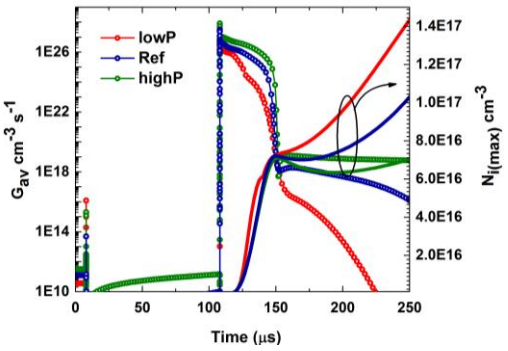

Fig. 10. Plot of avalanche carriers (G_{av}) and intrinsic carrier ($N_{i(max)}$) generation during UIS with different p-base doping.

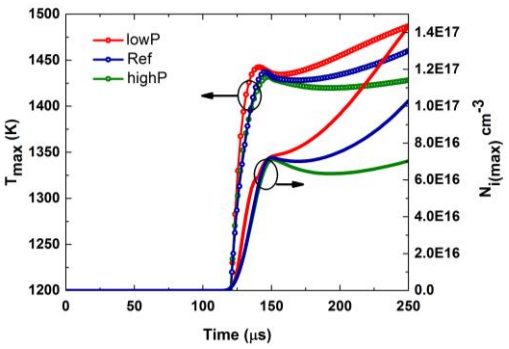

Fig. 11. Plot of temperature (T_{max}) and the corresponding intrinsic carrier generation ($N_{i(max)}$) during UIS with different p-base doping.

9 shows the UIS gate voltage and drain currents of the three test structures. At the end of the avalanche pulse (t_{av} = 160 µs), the lowP structure demonstrates an increased leakage current. The simulated carrier generation, both intrinsic ($N_{i(max)}$) and avalanche generated (G_{av}) are plotted for all the three structures in Fig. 10. The temporal profile of the junction temperature (T_{max}) is shown in Fig. 11. For an increase in T_{max} from 1400 K-1500 K, $N_{i(max)}$ in the lowP structure increases from 7e16 cm^{-3} to 1.4e17 cm^{-3} while that in the Ref structure increases only to 1e17 cm^{-3} and the highP remains at 7e16 cm^{-3} (see Fig. 11). The G_{av} is decreasing during the post avalanche phase as temperature is rising. This is because impact ionisation decreases with an increase in temperature [1]. During destructive failures, the V_{ds} collapses, turning off impact ionization. At the end of the avalanche duration, a positive feedback between T_{max} and $N_{i(max)}$ will keep the current increasing creating a thermal runaway. In an n-channel MOSFET, electrons are the majority carriers and so, lower p-base doping means lesser holes and so lower recombination of $N_{i(max)}$ carriers leaving behind more carriers across the base region. More carriers lead to an increase in

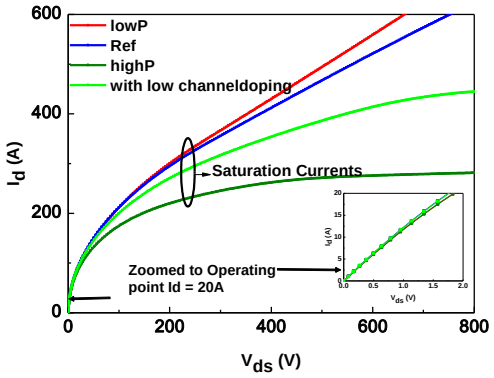

Fig. 12. On-state characteristics with different p-base doping.

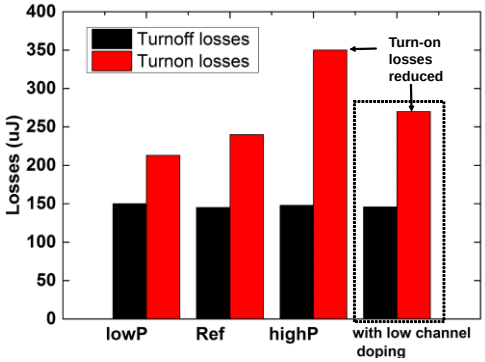

Fig. 13. Switching losses with different p-base doping.

diffusion currents. This increases the voltage drop below the N+source leading to minority carrier injection and the parasitic BJT is turned on, subsequently increasing the leakage currents which is not the case with a higher p-base doping. Therefore, the MOSFET with higher p-base doping under the N+source is more robust.

5. Impact of p-base doping on static conduction and dynamic switching performance

Fig. 12 shows the on-state characteristics at V_{gs} = 20 V for the different p-base doping without the influence of self-heating. It can be observed that at the operating current of I_d = 20 A, there is just 5 % increase in the on-state voltage drop when N_a is increased from N_a = 1e18 cm^{-3} to 2e18 cm^{-3}. Interestingly, I_d differs by larger values in the saturation region ($V_{ds} > V_{gs} - V_{th}$) for different p-base doping (see Fig. 12) which is crucial during SC. The threshold voltage V_{th} is increased with increase in p-base doping. This is because the effective voltage required to create charge in the channel ($V_{gs} - V_{th}$) is reduced with increased channel doping leading to an increased channel resistance (R_{ch}) [1]. Also the higher the p-base doping, the larger is the depletion in the JFET region, meaning the JFET resistance (R_{JFET}) is higher due to lower effective current conduction region. At larger $V_{ds,}$ the higher p-base doping can shield the channel from the high electric field in the drift region [1]. Thus, the channel length modulation factor (λ) is also reduced. This favours better current saturation. The body diode of the highP needs higher voltage for conduction. Nevertheless, at higher currents, the p-base of the highP injects holes earlier than the Ref reducing the diode mode conduction loss. The p-base doping profile is a box profile with three Gaussian profiles, and the vertical p-n junction (between p-base and n-JFET) has no weak-spot affecting the blocking capability (V_{BR}). Furthermore, V_{BR} is above 1.5 kV for all the three structures. The conduction loss due to $R_{ds(on)}$ increase, is increased by 5% at the operating current of I_d = 20 A for an increase in N_a from N_a = 1e18 cm^{-3} to 2e18 cm^{-3}. Further increase in p-base doping alone resulted in further reduction in SC current peaks but with a pronounced increase in $R_{ds(on).}$ In terms of dynamic performance, the three test structures were simulated for double pulse switching test (DPST) circuit. The switching losses in the turn-on and turn-off transitions are calculated by integrating the product of current I_d and voltage V_{ds} during the switching transition. It can be observed that during switching, the turn-off loss are reduced 1% by increase in p-base doping while the turn on loss increase by 25% with the increase in p-base doping. A compensating behaviour of turn-on and turn-off loss on the total losses is not observed. Instead, turn-on loss dominate leading to an increase in overall losses by 24 % with increase in p-base doping from N_a = 1e18 cm^{-3} to 2e18 cm^{-3}(see Fig. 13). The threshold voltage increase being the main cause for such an increase in switching loss, an optimized structure with counter doped channel region that has low peak channel doping (equal to 5e17 cm^{-3}) to bring down the threshold voltage increase caused by increase in p-base doping, has been simulated. It shows that the switching loss and conduction loss can be decreased by 19% and 5% respectively (see Fig. 12 and Fig. 13 with low channel doping). The SC I_d of such an optimised doping is also plotted in Fig. 4.

6. Measurements and interpretation

A commercial TO247 packaged SiC-MOSFET C2M0080120D has been used as the device under test (DUT). SC test has been performed to subject the

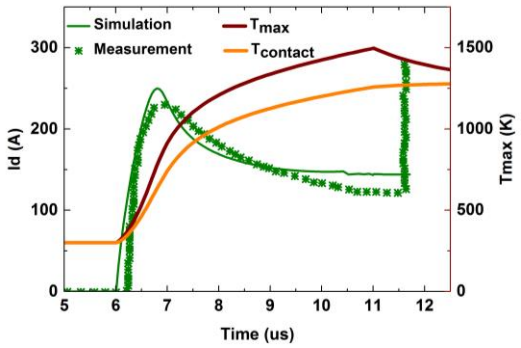

Fig. 14. Measured and simulated SC I_d of C2M0080120 with V_{ds} = 800 V, V_{gs} = 20 V, t_{sc} =5 µs, T = 300 K plotted together with the temperatures extracted from TCAD simulations.

DUT to a dc voltage of V_{ds} = 800 V. At initial temperature of T = 300 K and with the gate bias of V_{gs}= 20 V, the device failed destructively after a short circuit pulse time of t_{sc} = 4.5 µs. The measured I_d curve is shown in Fig. 14. The maximum temperature (T_{max}) inside the device and the temperature close to source contact ($T_{contact}$) extracted from the TCAD simulations are also plotted in the Fig. 14. It shows that the temperature reaches 1000 K at the contact which is above the melting point of the contact metal. For the given operating conditions, neither simulation nor measurement show a positive slope of I_d and thus BJT latch failure mode is not observed. Thus the reason for failure might be thermal or contact metal melting as mentioned in [5]. The measured and simulated I_d curves obtained after single pulse avalanche test for the DUT at an intial T = 300 K, V_{ds} = 800 V and V_{gs} = 20 V with a load inductance L_d = 5.1 mH are shown in Fig. 15. The energy dissipated in the device was 1.02 J.

7. Conclusion

This paper presents the SC capability and avalanche ruggedness of 1.2 kV SiC MOSFETs with varied p-base doping based on electro-thermal TCAD simulations. Simulations prove that the p-base region has a significant influence on limiting the saturation I_d, avalanche and intrinsic carrier generated leakage currents. These are essential for improving the ruggedness of the device against BJT latch and thermal failures. SC and UIS measurement I_d curves of C2M0080120D has been presented in comparison with the simulation. Higher p-base doping is considered to improve both the SC and avalanche ruggedness of SiC MOSFETs. However, a lower p-doping in the channel region is essential for a

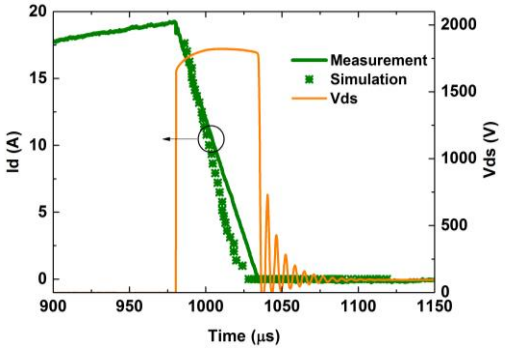

Fig. 15. Measured and simulated UIS I_d with a L_d = 5.1 mH and E = 1.02 J with an initial temperature T = 300 K.

minimum trade-off on the nominal operating performance.

8. Acknowledgement

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