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99.3% Efficient Three-Phase Buck-Type All-SiC SWISS Rectifier for DC Distribution Systems

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Abstract—DC power distribution systems for data centers, industrial applications and residential areas are expected to provide higher efficiency, reliability and lower cost compared to ac systems. Accordingly they have been an important research topic in recent years. In these applications an efficient power factor correction rectifier, supplying a dc distribution bus from the conventional three-phase ac mains is typically required. This paper analyzes the three-phase buck-type unity power factor SWISS Rectifier showing that its input current THD can be improved significantly by interleaving. The dc output filter is implemented using a current compensated Integrated Common Mode Coupled Inductor which ensures equal current sharing between interleaved half bridges and provides common mode inductance. Based on the analysis an high efficient 8 kW, 4 kWdm⁻³ (64 Wm⁻³) lab-scale prototype converter is designed using SiC MOSFETS. Measurements taken on a hardware prototype confirm a full power efficiency of 99.16% and a peak efficiency of 99.26%.

I. INTRODUCTION

Over the last decades the power demand of intrinsic dc loads, such as information and communication technology equipment, data centers, electric vehicle battery charging, LED lighting, etc. increased substantially. Furthermore renewable energy sources such as PV modules, fuel cells and battery storage are also based on dc. Therefore, dc distribution systems are expected to give advantages in terms of efficiency, reliability and/or cost as the total number of conversion stages can be reduced. Consequently, dc power supply and distribution systems for information and communication technology equipment, electric vehicle traction battery fast charging and dc microgrids have been a major topic in research and industry in recent years and corresponding standards have been created [1–9].

In these applications loads, with typically tens of kilowatts or more, are supplied from a dc bus with ≈ 400 V which is powered from the conventional 400 V or 480 V rms three-phase ac mains. Due to the high power levels sinusoidal ac input currents, in-phase with the mains voltage are required. As the dc bus voltage is lower than the amplitude of the full-wave rectified three-phase line-to-line voltage, two-stage systems are normally used which consist of a boost-type power factor correction (PFC) rectifier front end providing ≈ 800 V dc and a subsequent step-down dc-dc converter. Buck-type PFC rectifiers, which allow a direct conversion from the three-phase ac mains to a dc bus with lower voltage, are an advantageous alternative offering potentially lower losses, volume and cost [11].

The schematic of the three-phase buck-type SWISS Rectifier introduced in [10] is shown in Fig. 1(a). It consists of an ac-side EMI input filter, an Input Voltage Selector (IVS) and two series-connected buck-type dc-dc converters S_{xp}, D_{yp} and S_{nz}, D_{ny}. Note that all diodes and switches in the IVS are commutated at mains frequency only, therefore basically no switching losses occur in the IVS. Hence, diodes with a low forward voltage drop, or MOSFET-based synchronous rectifiers can be used in the IVS. The IVS output voltages \( u_{x}, u_{y}, u_{z} \) are piece-wise sinusoidal as the input phase with highest potential is connected to node \( x \), the one with lowest potential to \( z \) and the remaining phase to node \( y \).

In this paper the conventional (single buck converter output stage), cf. Fig. 1(a), and interleaved SWISS Rectifier, cf. Fig. 1(b), are compared regarding their ac input and dc

![Fig. 1](image-url)
output properties in Section II. The implemented prototype converter is presented in Section III, including measurement results.

II. SWISS RECTIFIER

A. Non-Interleaved SWISS Rectifier

In Fig. 1(a) the SWISS Rectifier with two coupled dc output inductors $L_{cm}$ (common mode) and $L_{dm}$ (differential mode) is shown. As the dc load is connected between output nodes $p$ and $n$ of the converter and has no connection to the star point $N$ of the ac mains $i_p = i_n$ can usually be assumed and the differential mode inductor alone would be sufficient. However, this is not the case if the load is, for example, a widespread dc distribution bus, potentially including physically large backup batteries which can have a significant capacitance $C_{cm}$ to ground. This creates a conduction path for high frequency common mode (cm) currents $i_{cm}$ from the output nodes $p$ and $n$ to the grounded star point $N$ as shown in Fig. 1, which is also the case if dedicated cm capacitors are added to the converter as part of a cm filter, which is typically required to comply with EMI regulations.

Simulation results for a conventional non-interleaved 8 kW SWISS Rectifier specified in Table I are shown in Fig. 2(a). It can be seen that the ac input currents $i_x$, $i_y$, $i_z$ show a significant switching frequency ripple and distortions with an amplitude of $\approx 6$ A at every 60° mains voltage sector boundary. Detailed simulation results for the vicinity of the first sector boundary at $\omega t \approx 60^\circ$ are shown in Fig. 3(a).

These distortions are due to the switching frequency voltage ripple on the filter capacitors $C_{x,y,z}$ as described in [12]. As $u_x$, $u_y$ and $u_z$ are piece-wise sinusoidal due to the IVS operation, $C_{x,y,z}$ create reactive power at the ac input which typically has to be limited to a few percent of the converter’s rated output power, which limits the capacitance value of $C_{x,y,z}$. As the SWISS Rectifier is a buck-type topology the input currents $i_x'$, $i_y'$ and $i_z'$ of the dc-dc converter are discontinuous which, in connection with the limited capacitance of $C_{x,y,z}$ results in a high switching frequency ripple of $u_x$, $u_y$ and $u_z$, cf. Fig. 3(a).

B. SWISS Rectifier with Interleaved Output Stages

To reduce the input current and voltage ripples either the ac input filter capacitance and inductance can be increased or a higher switching frequency can be used. Both options increase volume, losses and cost of the converter system. In order to overcome these disadvantages two interleaved dc-dc converters can be used as output stage to reduce the input and output current ripples [13]. The schematic of the resulting system, denominated as interleaved SWISS Rectifier in the following, is shown in Fig. 1(b) where two individual bridge legs $S_{xp1}$ / $D_{yp1}$ and $S_{xp2}$ / $D_{yp2}$ are used for the p side dc-dc converter stage and $S_{nz1}$ / $D_{yn1}$, $S_{nz2}$ / $D_{yn2}$ are used for the n side. By using the same duty cycle but 180° phase shifted carriers for the pulse width modulation of $S_{xp1}$ and $S_{xp2}$ the high frequency components of the resulting input current $i_x'$ have twice the frequency and half the amplitude compared to the non-interleaved case as shown in the detailed simulation results in Fig. 3(b).
and inner differential mode.

Fig. 4. Simplified circuit diagram of (a) the conventional and (b) the interleaved SWISS Rectifier where the IVS and the dc-dc converters are replaced by equivalent voltage sources split into common mode, outer- and inner differential mode.

Note that the interleaved buck converters can be controlled such that the individual dc-dc converter currents are split equally, i.e. \( i_{p1} = i_{p2} \) and \( i_{n1} = i_{n2} \) except for a switching frequency ripple. This implies that current compensated filtering of the dc-dc converter output voltages can be accomplished with close-coupled inductors. Ideally they carry no dc flux component and can be implemented without an air-gap, leading to a larger inductance value, similar to a cm inductor. Typically this is implemented with so called Intercell Transformers (ICTs) [14–16], were the interleaved SWISS Rectifier would require two ICTs, one for the p and one for the n side bridges. However, the two ICTs and the cm inductor \( L_{cm} \) can be integrated into a single four winding magnetic device in the following denominated as Integrated Common Mode Coupled Inductor (ICMCI) as shown in Fig. 1(b) and Fig. 4(b).

C. Integrated Common Mode Coupled Inductor - ICMCI

In order to analyze the properties of the ICMCI the SWISS Rectifier’s input filter, IVS and dc-dc converters are replaced by equivalent voltage sources which define the potentials of the non-interleaved SWISS Rectifier lead to high switching frequency ripples of the input filter capacitor voltages \( u_a \) and \( u_y \). As \( u_a \) and \( u_y \) cannot intersect due to \( D_{p1} \) and \( S_{p1} \), a distortion of the mains currents \( i_a \) and \( i_y \) results [12]. In case of an interleaved SWISS Rectifier the amplitude of \( i_a \) and \( i_y \) is reduced and the frequency is doubled which leads to a significant reduction of the ripples in \( u_a \) and \( u_y \).

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Note that $u_{cm,hf}$ is the switching frequency component of the converter’s cm voltage $u_{cm}$ as given by (1). Solving the system of equations given by (6) to (9) with respect to the ICMCI’s winding voltages yields

\begin{align}
    u_{w,p1} &= u_{idm,p}/2 + u_{cm,hf}, \quad (10) \\
    u_{w,p2} &= -u_{idm,p}/2 + u_{cm,hf}, \quad (11) \\
    u_{w,n1} &= -u_{idm,n}/2 - u_{cm,hf}, \quad (12) \\
    u_{w,n2} &= u_{idm,n}/2 - u_{cm,hf}. \quad (13)
\end{align}

It can be seen that the ICMCI’s winding voltages are defined only by the switching frequency cm voltage and the inner dm voltages, while the outer dm voltage is applied only to the differential mode inductor $L_{dm}$ and the dc output $u_{pn}$.

Simulation results of the ICMCI’s winding voltages and the outer dm voltage for nominal operation are shown in Fig. 5(b). Compared to a non-interleaved SWISS Rectifier, as shown in Fig. 5(a), the (outer) dm voltage applied to $L_{dm}$ is reduced which leads to a significant reduction of the peak-to-peak ripple in $i_{odm}$ compared to $i_{dm}$. The same holds for the cm current $i_{cm}$.

A drawing of the resulting switching frequency voltage and current waveforms is shown in Fig. 6 for $0^\circ \leq \omega t \leq 30^\circ$. It can be seen that the ICMCI’s winding voltages $u_{w,p1}$, $u_{w,p2}$, $u_{w,n1}$ and $u_{w,n2}$ are periodic with the switching frequency, while the voltage $u_{odm,hf}$ applied to $L_{dm}$ shows twice that frequency due to harmonic cancellation.

III. RECTIFIER PROTOTYPE

For power supply systems which are operated 24/7, as in data centers, a high efficiency is desirable to minimize the cost of conversion losses and cooling and hence the operating costs of the system [17]. Furthermore a high efficiency over a wide range of output currents is desirable in applications where redundant supplies are used resulting in a nominal operation at half of the rated power or less. Therefore, a system which achieves an efficiency of $> 99\%$ for $P > P_{rated}/3$ for the operating condition listed in Table I was designed.

Silicon carbide (SiC) MOSFETs are selected due to their low conduction and switching losses and high blocking voltage rating (1.2 kV) compared to Si IGBTs and Si MOSFETs [18, 19]. Nanocrystalline core material (FINEMET) is used for dm inductor $L_{dm}$ due to its high saturation flux density ($\approx 1.2$ T) and lower losses compared to amorphous alloys. For the current compensated ICMCI core 3C94 ferrite material is used due to its lower core losses. A symmetrical, cube-type core as shown in Fig. 7 is used for the ICMCI. This shape is achieved by using four conventional C cores.

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**TABLE II**

<table>
<thead>
<tr>
<th>COMPONENTS USED IN THE HARDWARE PROTOTYPE</th>
<th>ICMCI</th>
<th>$L_{dm}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>4 x U46/40/28-3C94</td>
<td>F3CC25</td>
</tr>
<tr>
<td>Wire</td>
<td>0.4 x 15 mm</td>
<td>2.4 x 6 mm</td>
</tr>
<tr>
<td>Turns</td>
<td>4 x 20</td>
<td>2 x 15</td>
</tr>
<tr>
<td>Volume</td>
<td>420 cm$^3$</td>
<td>249 cm$^3$</td>
</tr>
<tr>
<td>Losses</td>
<td>5.6 W</td>
<td>2.9 W</td>
</tr>
</tbody>
</table>

$D_{sk}$, $D_{ka}$ C2M0025120 $P_{loss} = 1.8$ W
$S_{ky,k}$ C2M0080120 $P_{loss} = 0.8$ W
$S_{kp1,2}, S_{kp2,1,2}$ C2M0025120 $P_{loss} = 4.9$ W
$D_{kp1,2}, D_{ky1,2}$ C2M0025120 $P_{loss} = 1.0$ W
The calculated efficiency of the rectifier for $U_{pn} = 400$ V as function of dc load current $I_l$ is shown in Fig. 11, together with measurement results taken using a Yokogawa WT3000 power analyzer. It can be seen that the measurement results of the prototype converter match the calculated efficiency expressed by (9).

The calculated losses of the rectifier’s main components (cf. (a)) for nominal operation ($U_{pn} = 400$ V, $I_l = 20$ A) are shown in (b) (1 dm$^3 = 1$ l). The control losses include DSP/FPGA, gate drivers, fans and auxiliary supply. The corresponding volumes in dm$^3$ are shown in (b) (1 dm$^3 = 1$ l).
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ACKNOWLEDGMENT

REFERENCES


[9] ETSI, “Environmental Engineering (EE); Power Supply Interface at the Input to Telecommunications and Datacom (ICT) Equipment; Part 3: Operated by Rectified Current Source, Alternating Current Source or Direct Current Source up to 400 V; Sub-part 1: Direct Current Source up to 400V,” EN 300 132-3-1, Feb 2012.


