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Volume Optimization of a 30 kW Boost PFC Converter Focusing on the CM/DM EMI Filter Design

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Keywords

<<EMC/EMI>>, <<Modulation Strategy>>, <<Power factor correction>>,
<<Three-phase system>>

Abstract

PFC converters are widely used in industrial drive systems. The modulation scheme and the topology of the converter have a considerable impact not only on the switching losses, but also on the volume of the passive components, i.e. the EMI filter (CM and DM) and the DC link capacitors. In order to evaluate this impact, different modulation schemes for 2L and 3L topologies are analysed in this paper based on comprehensive converter optimizations. In these optimizations also a model for the EMI filter is included and the optimal converter volume including the EMI filter is evaluated for the different topologies and modulation schemes. Thus, significant differences in the converter volume can be observed for the different modulation schemes. Also the impact of SiC semiconductors on the system performance is analysed. The *3L-NPB* modulation scheme with a NPC topology offers the best compromise of heat sink, EMI filter and DC link capacitor volume.

1 Introduction

3-phase boost Power Factor Correction (PFC) converters are widely used in industry to supply electrical systems, as for example drive, photovoltaic or telecommunication systems, from the mains. There, the PFC converters have to ensure a high power factor and, in order to not disturb other electrical devices, have to comply with harmonic regulations at low frequencies ($f \leq 700\,\text{Hz}$, LF) and EMI regulations

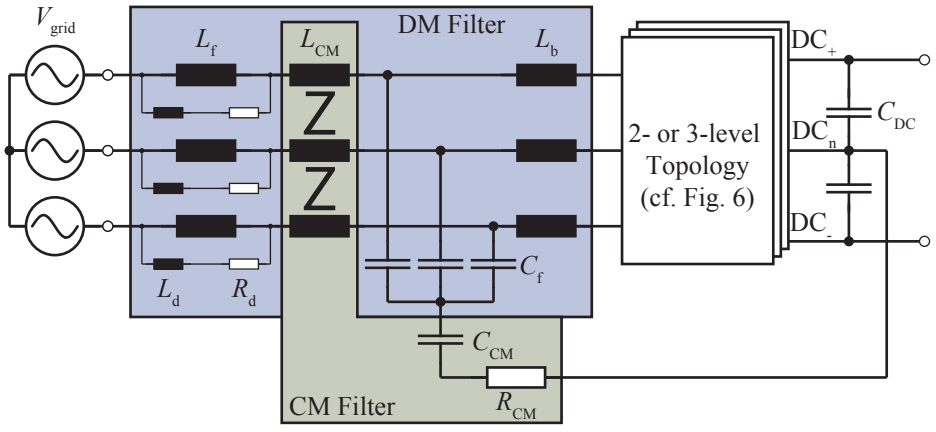

Figure 1: 3-phase boost PFC converter with CM and DM EMI filter. The topologies for the PFC converter are described in section 3 / Fig. 6.

at high frequencies (150 kHz $\leq f \leq$ 30 MHz, HF) [1]. Applying a suitable modulation scheme with a sufficiently high switching frequency ensures that the PFC typically complies with the LF regulations. However, the HF noise has to be attenuated by an additional electromagnetic interference (EMI) filter, which has a considerable impact on the converter volume [2]. Fig. 1 shows the schematic of a 3-phase boost PFC converter with a typical common mode (CM) and differential mode (DM) EMI filter.

In [3], such an EMI filter including both CM and DM filter has been optimized for a sinusoidal modulation scheme with a superimposed third harmonic and a Neutral Point Clamped (NPC) topology (cf. Fig. 6c). In [4], the modulation scheme has been optimized with respect to the switching losses for a NPC topology but the EMI filter has been neglected. In [5], the modulation scheme has been optimized with respect to the CM voltage generation for a 2-level topology. However, if the optimization is only focused on one of these aspects (filter, switching losses, CM generation), it could worsen other aspects and therefore the overall system design.

Therefore, in this paper, all of these aspects are combined with the goal to optimize the design of a three-phase boost PFC converter including the EMI filter (cf. Fig. 1) with respect to volume. The optimization considers also limits in the medium frequency range (700 Hz $\leq f \leq$ 150 kHz, MF) and is performed for different topologies and modulation schemes. The total volume consists of the volumes of the CM and DM filter, the boost inductor, the heat sink to cool the semiconductor losses and the DC link capacitors. The considered specifications of the converter for the optimization results are given in table I.

In section 2, the considered optimization procedure for the PFC converter design is outlined, the boundary conditions of the optimization are set and the volume estimation formulas are given. In section 3, the investigated modulation schemes and switching topologies are described. In section 4, the results of the optimization are presented.

2 Optimization Procedure

The considered optimization procedure shown in Fig. 2 is based on the DM filter optimization presented in [6] and extended by a CM filter model / optimization (highlighted in Fig. 2). The input of the optimization is the system specification which includes the AC and DC voltage, output power, inductor / capacitor materials, topology including semiconductor devices and modulation scheme. The optimization varies the CM and DM filter parameters as well as the switching frequency in order to minimize the volume of the converter. For reducing the computing time, the optimization routine is implemented in a cascaded structure. There, the switching frequency f_s has the biggest influence on the converter design and is therefore in the most outer loop. As the DM filter has a higher volume than the CM filter it is in a more outer loop than the CM filter. In [6], the following DM filter design parameters were optimized:

1. The boost inductance L_b (trade-off between boost inductor volume and filter volume).
2. The filter resonance frequency ω_0 (trade-off between filter volume and attenuation).
3. The frequency location of the maximum filter output impedance ω_m (trade-off between damping capability and volume of the damping element).
4. The maximum value of the filter output impedance Z_m (trade-off between inductor and capacitor volume of the filter).

In addition, the following CM filter design parameters are optimized in this work:

1. The CM filter resonance frequency ω_cm (trade-off between filter volume and attenuation).
2. The maximum value of the CM filter output impedance Z_cm (trade-off between inductor and capacitor volume of the CM filter).

Besides the EMI filter parameters, also the switching frequency f_s is optimized (trade-off between volume of the passive components, i.e. EMI filter and DC link capacitor, and heat sink volume).

In the following section 2.1, the EMI standards which set the limits in the optimization procedure are described. Thereafter, the DM and CM equivalent circuit of the converter are described in section 2.2. If a converter design complies with the standards, the total volume of the converter is estimated, which is described in section 2.3.

Table I: Specifications of the investigated bidirectional three-phase boost PFC converter.

AC Voltage (ph-ph)	400 V
DC Voltage	800 V
Power	30 kW

Table II: Parameters for estimating the volume of the capacitors.

Component	Series	k_1	k_2
C_f	*EPCOS B3292x*	22.96 $\mathrm{cm^3F^{-1}V^{-2}}$	2.24 $\mathrm{cm^3}$
C_CM	*EPCOS B3296x*	55.54 $\mathrm{cm^3F^{-1}V^{-2}}$	0.84 $\mathrm{cm^3}$
C_DC	*EPCOS B3277x*	4.95 $\mathrm{cm^3F^{-1}V^{-2}}$	4.24 $\mathrm{cm^3}$

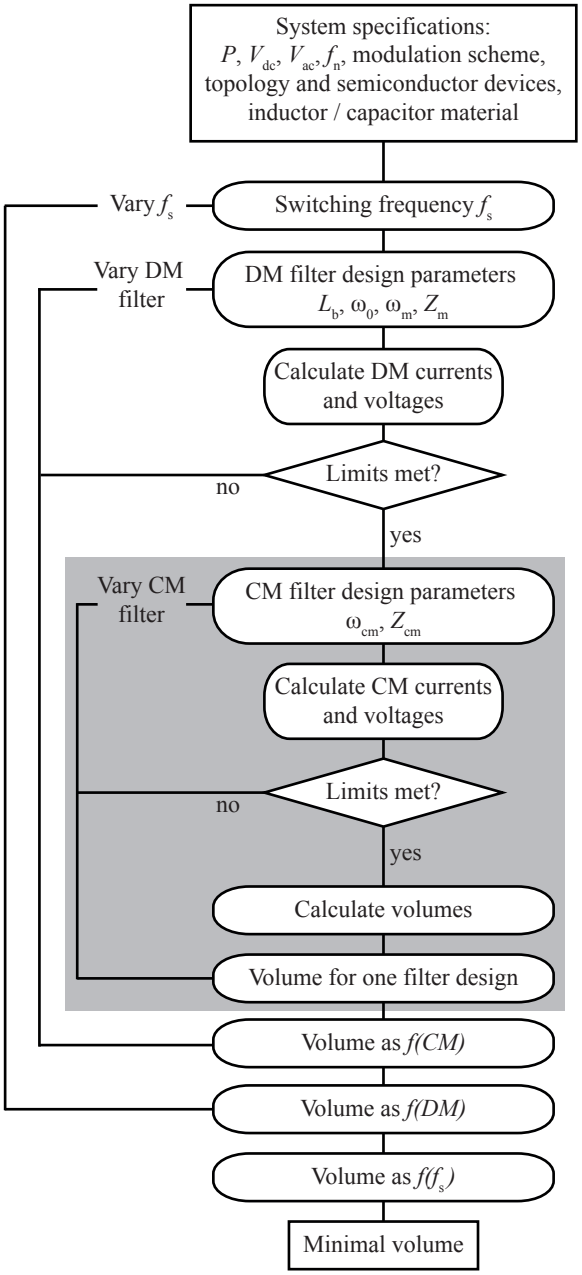

Figure 2: Flowchart of the cascaded optimization. The proposed CM filter optimization is highlighted.

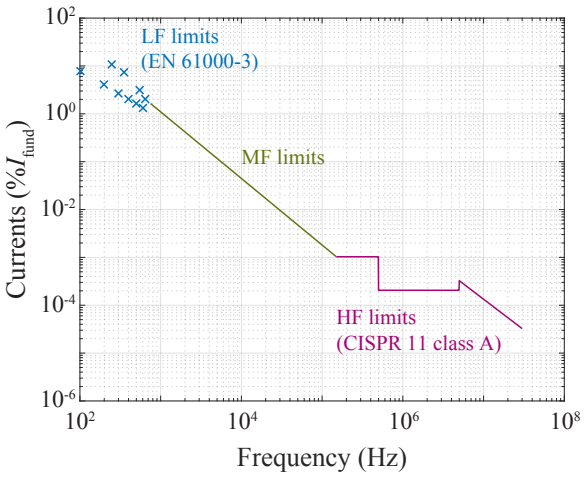

Figure 3: EMI limits used as a boundary in the optimization procedure.

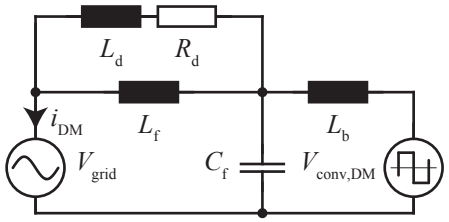

Figure 4: DM single phase equivalent circuit of a three-phase boost PFC converter.

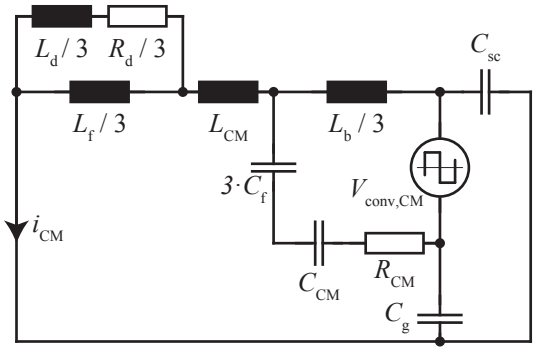

Figure 5: CM equivalent circuit of a three-phase boost PFC converter.

2.1 Standards and Stability

The LF and total harmonic distortion limits are taken from the EN 61000-3-12 standard and the HF limits from the CISPR 11 class A standard. In between, a logarithmic linear function from the LF to the HF limit is used. A standard in this frequency range does not need to be met yet, but could be expected in the future [1]. Fig. 3 shows the applied limits.

In order to avoid that the EMI filter affects the converter control behaviour, Middlebrook's stability criterion [7, 8] should be met. In [9], the criterion has been extended to 3-phase systems, which is used in the considered optimization procedure.

2.2 Converter Model

In this section, the DM and CM model of the converter are described. These models are used in the optimization procedure to check if the limits of section 2.1 are met.

Fig. 4 shows the schematic of the DM single phase equivalent circuit of the converter model. The waveform of the DM voltage source $V_{conv,DM}$ depends on the chosen topology and modulation scheme

Table III: Parameters to estimate the volume of the inductors.

Component	Core Material	Shape	k_1	k_2
L_b	*METGLAS Alloy 2605SA1*	E-Core	$266\,\mathrm{cm}^3\left(\mathrm{H}^{-1}\mathrm{A}^{-2}\right)^{\frac{4}{3}}$	$0\,\mathrm{cm}^3\mathrm{H}^{-1}\mathrm{A}^{-2}$
L_f	*METGLAS Alloy 2605SA1*	E-Core	$169\,\mathrm{cm}^3\left(\mathrm{H}^{-1}\mathrm{A}^{-2}\right)^{\frac{4}{3}}$	$64\,\mathrm{cm}^3\mathrm{H}^{-1}\mathrm{A}^{-2}$
L_CM	*Vitroperm 500F*	Toroid	$39\,\mathrm{cm}^3\left(\mathrm{H}^{-1}\mathrm{A}^{-2}\right)^{\frac{4}{3}}$	$15\,\mathrm{cm}^3\mathrm{H}^{-1}\mathrm{A}^{-2}$

(cf. section 3). Due to the magnetic coupling, the ideal CM filter components can be neglected in the DM design. Based on the results in [6], a single-stage parallel-RL damping topology for the DM filter was chosen in order to avoid resonances.

The CM equivalent schematic is shown in Fig. 5, where the waveform of the CM voltage source $V_\mathrm{conv,CM}$ also depends on the chosen topology and modulation scheme. C_g is the equivalent capacitance from the two DC link poles to ground, C_sc is the parasitic capacitance from the power semiconductors to the grounded heat sink, which varies depending on the used topology (cf. section 3). The CM filter capacitance C_CM is connected to the midpoint of the DC link because this placement allows an unlimited value of the CM capacitance. In contrast, if the CM capacitor would be connected to the ground, the CM capacitance would be limited to a few tens of nanofarads because of safety regulations, [3].

The resulting total grid current including HF ripple is calculated by adding the currents i_DM and i_CM in the frequency domain. The LF limits are checked with a Fourier transformation of the grid current, the MF and HF limits are checked with an line impedance stabilizing network (LISN) inserted at the grid interface. This allows to obtain the values which have to be expected also from a real measurement device, which is measuring the voltage over the LISN resistor with a quasi-peak detector [10].

2.3 Volume of the Passive Elements

If a converter design complies with the EMI standards, the volumes of the various components are estimated. The capacitor volume is estimated with

$$V_C = k_1 \cdot C\hat{V}^2 + k_2(\hat{V}) \tag{1}$$

from [6]. The parameters k_1 and k_2 are based on the *EPCOS B3292x* series for the DM filter capacitors C_f, the *EPCOS B3296x* series for the CM filter capacitor C_{CM} and the *EPCOS B3277x* series for the DC link capacitors C_{DC}. Table II shows the parameters for each series.

The inductor volume is estimated with

$$V_L = k_1 \cdot \left(LI^2\right)^{\frac{3}{4}} + k_2 \cdot LI^2 \tag{2}$$

also from [6]. The parameters k_1 and k_2 are based on the inductor optimization described in [6] where the ambient temperature is set to 55 °C and a heat transfer coefficient from the surface to ambient of $\alpha_\mathrm{surface} = 20\,\mathrm{W\,m^{-2}\,K^{-1}}$ (assuming that the inductor is in the air duct of the heat sink, [11]) and a maximum allowed surface temperature of 80 °C are assumed. Table III shows the core materials, shapes and parameters for the inductive components L_b, L_f, L_CM considered in the optimization. Note that L_b and L_f have different parameters although they are made of the same material and have the same basic shape, because the current in L_b has a high-frequency current ripple in addition to the 50 Hz current. The volume of L_d is neglected, as its volume is much lower than the other components.

2.4 Volume of the Heat Sink

Table IV shows the semiconductors which are considered in the optimization. They all have similar conduction losses to make a fair comparison of the different topologies. Note that the used IGBTs have built-in diodes and the 600 V diode is used only for the NPC topology (cf. 6c). The conduction and switching losses are calculated based on datasheet values. For the T-Type (TT) topology (cf. 6b) the switching losses have been extrapolated to the lower operating voltage. In addition, the switching losses differ from the data sheet as a diode with a lower voltage rating is used for the transition of the current. The datasheet curves have been adjusted linearly based on the measured data given in [12]. The maximum allowed junction temperature of the power semiconductors is set to $T_\mathrm{sc} = 125\,^\circ\mathrm{C}$, so that the maximum allowed heat sink temperature is

$$T_\mathrm{hs} = \min(T_\mathrm{sc} - P_\mathrm{chip,i} \cdot R_\mathrm{th,i}), i = 1...N \tag{3}$$

Table IV: Semiconductors considered in the optimization.

Type	Name
Si 1200 V IGBT	*Infineon IKW25N120T2*
Si 600 V IGBT	*Infineon IKW30N65ES5*
Si 600 V Diode	*Infineon IDW30E65D1*
SiC 1200 V MOSFET	*Cree C2M0025120D*
SiC 600 V MOSFET	*Microsemi APT130SM70B*
SiC 600 V Diode	*Infineon IDW30G65C5*

Table V: Generated peak DM voltage of the converter at the switching frequency for different modulation schemes.

Modulation	Peak DM voltage
2L-Sin	90 V
2L-C	145 V
3L-Sin	38 V
3L-OC	60 V
3L-C	59 V
3L-NPB	18 V

There, $P_{\text{chip,i}}$ is the power loss of a single chip and $R_{\text{th,i}}$ is its corresponding thermal resistance from junction to heat sink (including an insulation foil between semiconductor case and heat sink). The variable N defines the number of semiconductors mounted on the heat sink. The heat sink is assumed to have a Cooling System Performance Index [13] CSPI $= 10\,\text{W}\,\text{K}^{-1}\,\text{dm}^{-1}$ (forced air cooling) and therefore the volume can be calculated with

$$V_{\text{hs}} = \frac{\sum P_{\text{chip}}}{\text{CSPI} \cdot (T_{\text{hs}} - T_{\text{amb}})}. \tag{4}$$

3 Modulation Schemes

In this section, the investigated modulation schemes and topologies are described using a space vector (SV) transformation [14]. The voltage SVs define the generated DM voltage of the converter. The reference voltage SV is $V_{\text{conv}} = M \cdot \cos(\alpha)$, where M defines the length and α the angle of the SV. The CM voltage is included in the SV, but must be calculated separately based on the actually used voltage SVs and the modulation scheme.

The following sections 3.1 and 3.2 describe the investigated modulation schemes for the 2-level respectively the 3-level topologies. Section 3.3 compares the investigated modulation schemes analytically.

3.1 Modulation Schemes for the 2-Level Topology

The considered 2-level topology is shown in Fig. 6a for a single leg. The advantages of this 2-level topology are the low conduction losses, as only one semiconductor is conducting the current at a given time. The disadvantages are the higher switching losses and a higher current ripple in the converter current.

The simplest modulation scheme is a sinusoidal phase modulation, where the phase voltages follow a sinusoidal reference [15] and no CM voltage below the switching frequency is generated. This modulation scheme is denoted as *2L-Sin* (Sinusoidal) in the following.

The SV modulation method allows different modulation schemes, as the duration of the non-DM-voltage-forming switching states (1,1,1) and (-1,-1,-1) during a switching period can be altered without affecting the generated low-frequency DM voltage. This allows more complex modulation schemes to achieve for example an increased modulation index or reduced switching losses. One possibility to reduce the switching losses is to clamp the phase with the highest current during a switching period [15]. For example, if the switching state (-1,-1,-1) is omitted in sector 1, the first phase is clamped to the positive DC link voltage and no switching losses occur in this phase. However, a CM voltage below the switching frequency is generated as can be seen in Fig. 8. This modulation scheme is denoted as *2L-C* (Clamping) in the following.

3.2 Modulation Schemes for the 3-Level Topologies

For 3-level converters, the T-Type (TT) and the Neutral Point Clamped (NPC) topology (cf. Fig. 6b and c) are investigated. The NPC topology offers the lowest switching losses, but higher conduction losses as always two semiconductors conduct the current. The TT topology offers on the one hand lower conduction losses compared to the NPC topology as at some time instances only one semiconductor is conducting the current, but on the other hand higher switching losses than the NPC topology as the switches S_1 / S_4 must have a higher voltage rating. Both the NPC and TT topology generate basically the

same DM and CM converter voltage, but have a different value of the parasitic capacitance C_{sc} (cf. Fig. 5).

Again, the simplest modulation scheme is a pure sinusoidal phase modulation, where the phase voltages follow a sinusoidal reference and no CM voltage below the switching frequency is generated. This modulation scheme is denoted as *3L-Sin* (Sinusoidal) in the following.

Like in the case of a 2-level topology, the phase with the highest current can be clamped during a switching period in order to reduce the switching losses [4]. However, this generates the same CM voltage in the LF range as in the case of the 2-level topology (cf. Fig. 8). Additionally, the midpoint of the DC link is either charged or discharged during a switching period (cf. Fig. 7). Therefore, the DC link capacitance must be relatively high in order to limit the variation of the midpoint of the DC link, which increases the converter volume. This modulation scheme is denoted as *3L-OC* (Optimal Clamping) in the following.

If the clamping is altered between the phases with the highest and the second-highest current, the DC midpoint balance can be assured with a lower DC link capacitance value than for the *3L-OC* modulation scheme. However, this generates an additional CM voltage below the switching frequency. For example, if the clamping is changed after each switching period, a CM voltage generation at half of the switching frequency occurs. This modulation scheme is denoted as *3L-C* (Clamping) in the following.

The average current to the DC midpoint i_{mp} (cf. Fig. 6b and 6c) over one switching period can also be balanced by applying the modulation scheme presented in [16]. In 3-level systems, SVs with the same voltage forming vector, e.g. (1,0,0) and (0, -1, -1), have midpoint currents in the opposite directions, e.g. (1, 0, 0) has $i_{mp} = -i_a$ and (0, -1, -1) has $i_{\mathrm{mp}} = +i_a$, where i_a is the current of phase a. In order to balance the voltage, the SVs are chosen so that the average current to the midpoint equals to zero. This enables to lower the DC link capacitance value and therefore to reduce the DC link capacitor volume. This modulation scheme also lowers the CM voltage harmonics below the switching frequency considerably compared to the *3L-OC* modulation scheme (cf. Fig. 8). However, the switching losses increase as no phase is clamped. This modulation scheme is denoted as *3L-NPB* (Neutral Point Balanced) in the following.

3.3 Analytical Comparison

In the following, the considered modulation schemes and topologies are compared in terms of conduction losses, switching losses and CM voltage generation. There, the IGBT devices listed in table IV are considered. As a benchmark a 2L converter with *2L-C* modulation scheme is used. The conduction losses are calculated with the rms current through the switches. For comparing the switching losses, it is assumed that the losses depend linearly on the switched voltage and current. The 1200 V devices in the TT topology used for switching only 400 V are assumed to have 15% higher losses than 600 V devices, based on data sheet values. The CM voltage generation is calculated with

$$V_{\mathrm{CM,cmp}} = \sqrt{\sum_{f} V_{\mathrm{CM,fft}}(f)^2} \text{ for } f < f_s, \tag{5}$$

where $V_{\mathrm{CM,fft}}$ is the Fourier transformation of the CM voltage generated by the converter (cf. Fig. 8). Fig. 9 shows a comparison of the investigated modulation schemes in terms of semiconductor losses and

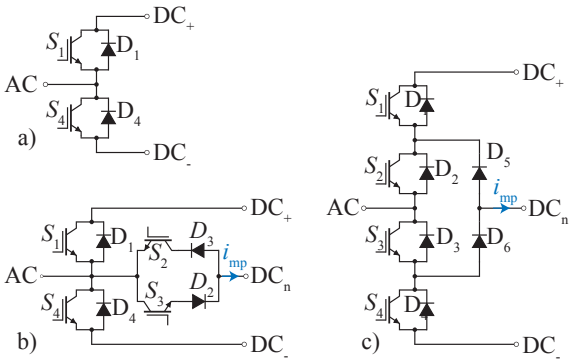

Figure 6: Investigated topologies: a) 2-level, b) 3-level TT and c) 3-level NPC.

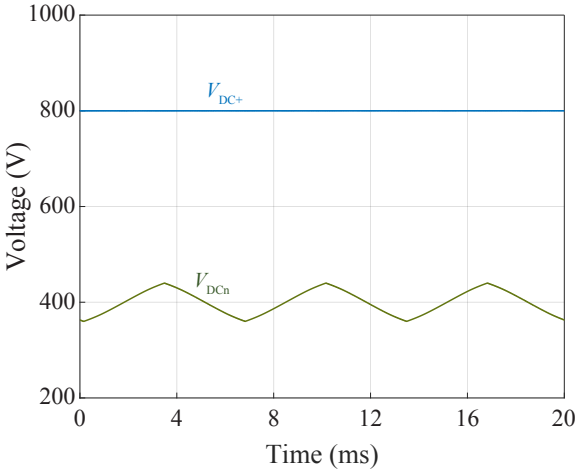

Figure 7: Midpoint voltage V_{DCn} and DC link voltage $V_{\mathrm{DC+}}$ of a converter using the *3L-OC* modulation scheme.

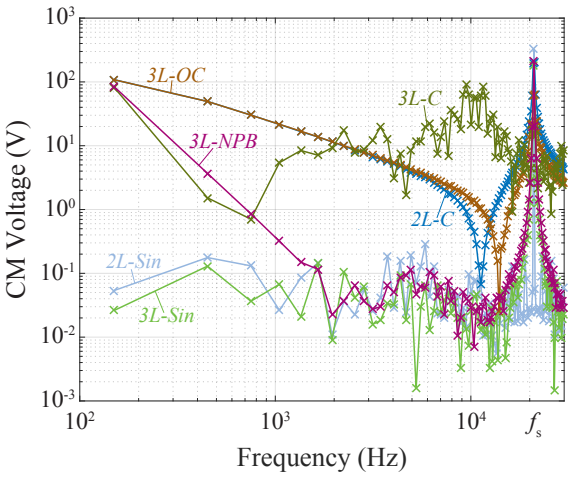

Figure 8: CM voltage for different modulation schemes with $M = 0.7$ and $f_s = 20\,\text{kHz}$.

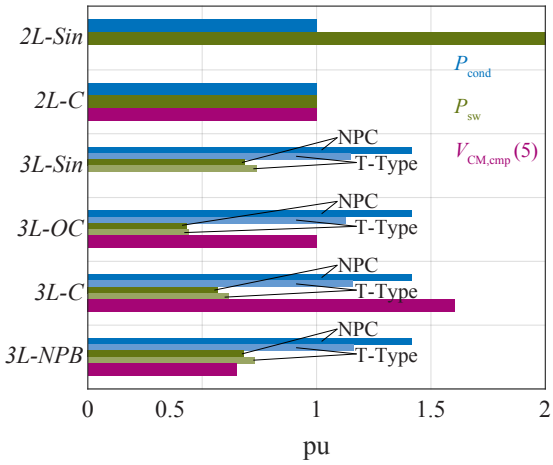

Figure 9: Comparison of the investigated modulation schemes in terms of semiconductor losses and CM harmonics below the switching frequency.

CM voltage. The 3L conduction and switching losses are subdivided into NPC topology (dark) and TT topology (light).

Table V shows the peak of the generated DM voltage at the switching frequency. The peak value depends on the modulation scheme while the location of this peak depends on the switching frequency. The results show that the modulation schemes with reduced switching losses have a higher peak than the other modulation schemes. This indicates that the advantage of the reduced switching losses due to clamping results in a higher peak voltage at the switching frequency. However, a higher DM voltage peak does not necessarily result in a large EMI filter, as the peak could be at a higher frequency so that the corner frequency of the filter could also be shifted to higher frequencies.

4 Optimization Results

In the following, the results of the converter optimization are shown and discussed separately for the heat sink, DC link capacitor and EMI filter volume. In addition, the total converter volume for silicon (Si) and for silicon carbide (SiC) devices are investigated.

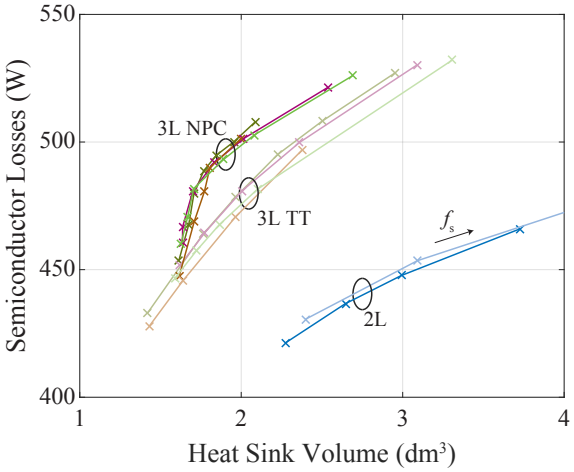

Figure 10: Optimization results for the semiconductor losses and the corresponding heat sink volume.

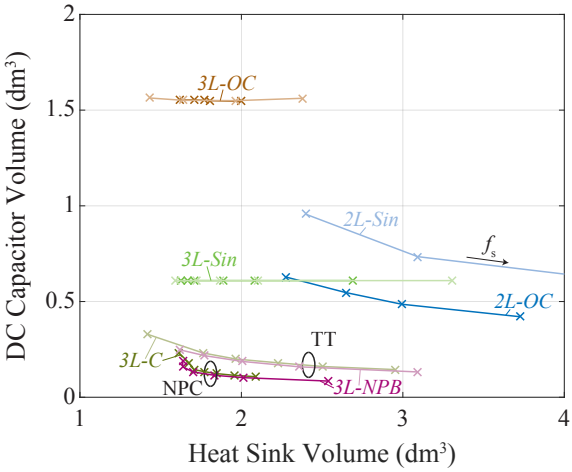

Figure 11: Optimization results for the DC link capacitor volume as a function of the heat sink volume.

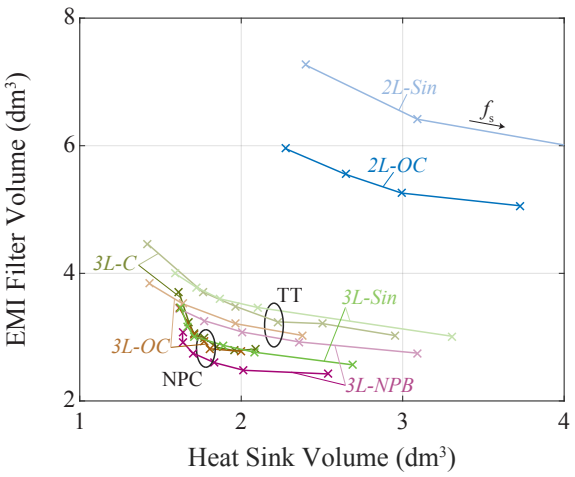

Figure 12: Optimization results for the EMI filter volume as a function of the heat sink volume.

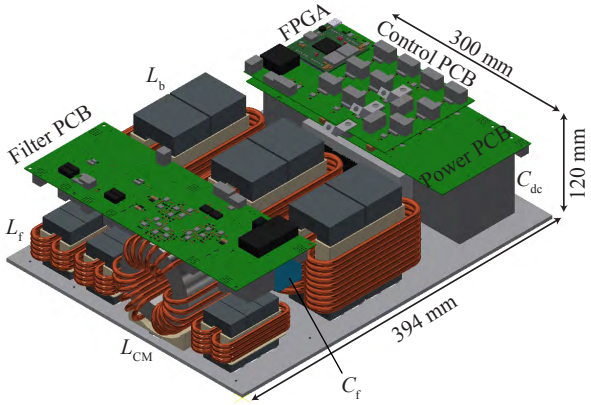

Figure 13: CAD picture of a 30 kW prototype.

4.1 Heat Sink Volume

The heat sink volume is not linearly dependent on the total semiconductor losses, as the maximum loss of one semiconductor might limit the maximal allowed heat sink temperature. Fig. 10 shows the semiconductor losses and the corresponding heat sink volume. There, the advantage of the NPC topology compared to the TT topology can be seen, since the losses are more evenly distributed among the semiconductor devices, which reduces the heat sink temperature and its volume. The 2L topology requires a bigger heat sink for the same semiconductor losses despite having less semiconductors because the maximal loss per device is bigger, lowering the required heat sink temperature and therefore increasing the heat sink volume. This limits the achievable switching frequency for a given heat sink. Note that the different modulation schemes result in the same heat sink volume at different switching frequencies due to the different switching losses. Therefore, the other converter component volumes are shown as a function of the heat sink volume and not the switching frequency in the following.

4.2 DC Link Capacitor Volume

Fig. 11 shows the DC link capacitor volume for the different modulation schemes as a function of the heat sink volume. It shows the big disadvantage of the *3L-OC* modulation scheme: The DC link capacitor volume is independent of the heat sink volume because it does not depend on the switching frequency. When the highest phase is clamped the midpoint current can only be controlled by the other two phase currents, which have the same algebraic sign during this clamping phase, so the midpoint of the DC link is either charged or discharged during the clamping period, which lasts typically 60° of the mains period. A similar behaviour can be seen in case of the *3L-Sin* modulation scheme, although at a smaller volume. In the case of the *3L-NPB* and the *3L-C* modulation schemes, the NPC switching topology shows a slight advantage, as higher switching frequencies can be achieved.

4.3 EMI Filter Volume

Fig. 12 shows the EMI filter volume for the different modulation schemes as a function of the heat sink volume. Note that the filter volume is not subdivided in DM and CM as some components (e.g. boost inductor) have an effect on the DM as well as on the CM attenuation and the decision how much DM and how much CM attenuation is needed is part of the optimization task [3]. The 2L topology results in an almost twice as big EMI filter volume as the 3L topologies. For the 3L topologies, one can see the superiority of the NPC topology, as it allows higher switching frequencies and therefore smaller EMI filter volumes. The *3L-NPB* modulation scheme offers the smallest EMI filter volume. Note that despite the higher achievable switching frequency of the *3L-C* and *3L-OC* modulation schemes, the EMI filter volume is bigger due to the higher DM peak and the considerable CM voltage below the switching frequency.

4.4 Total Converter Volume with Si Semiconductors

The left part of Fig. 14 shows the total volume of the converter with Si semiconductor devices as a function of the switching frequency for the different modulation schemes. Note that this volume is the sum of the boxed volumes of the single components. A real setup (cf. Fig. 13) will be significantly

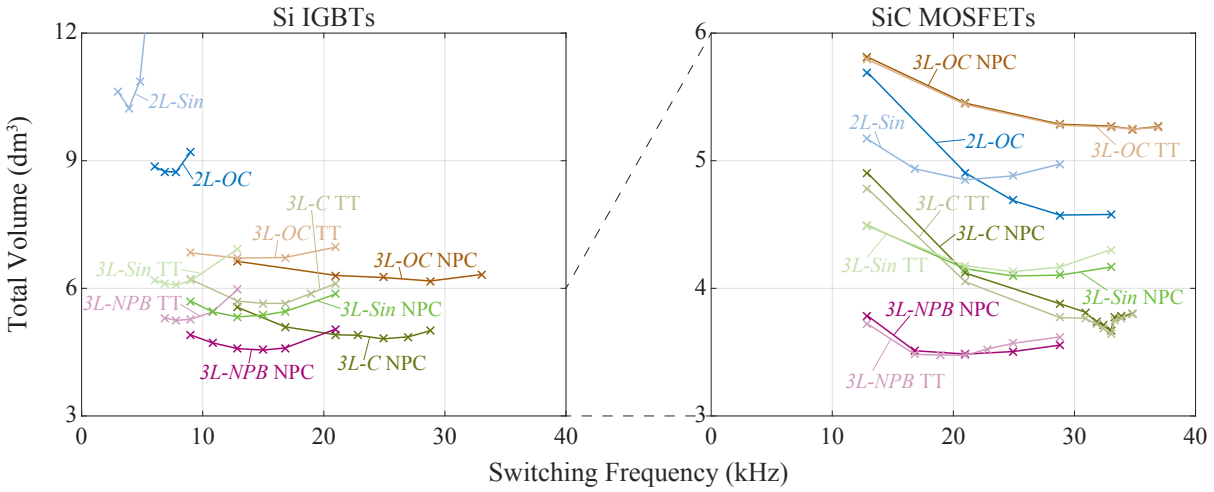

Figure 14: Optimization results of the total converter volume depending on the switching frequency. The left part are the optimization results with Si IGBTs, the right part with SiC MOSFETs.

larger, typically 150% [17]. The *3L-NPB* modulation scheme with NPC topology shows the best results and 2L systems are clearly outperformed. The volume of the *3L-NPB* modulation scheme with NPC topology is 4.55 dm^3 and for example 26.3% lower than the volume of the *3L-OC* modulation scheme with NPC topology, which is 6.17 dm^3. The left part of Fig. 15 shows the shares of the individual converter components on the total volume.

4.5 Total Converter Volume with SiC Semiconductors

With SiC devices, the switching losses are considerably lower, resulting in a smaller heat sink volume and higher achievable switching frequencies. The right part of Fig. 14 shows the optimization results for SiC devices. The TT and NPC topology result now in almost the same system volume. The share of the DC link capacitor volume in the total converter volume with the *3L-OC* and *3L-Sin* is considerably higher as the SiC devices enable lower heat sink volumes and higher switching frequencies. Therefore, the *3L-OC* modulation scheme is even outperformed by the 2L topology. The *3L-NPB* is still the best modulation scheme and even increases its advantage in contrast to the other modulation schemes as its biggest weakness are higher switching losses which are considerably reduced by using SiC semiconductors. The volume of the *3L-NPB* modulation scheme with TT topology is 3.48 dm^3 and for example 33.7% lower than the volume of the *3L-OC* modulation scheme with TT topology, which is 5.25 dm^3. In comparison to the optimization using Si semiconductors the volume drops by 24.5%. The right part of Fig. 15 shows the shares of the individual converter parts on the total volume.

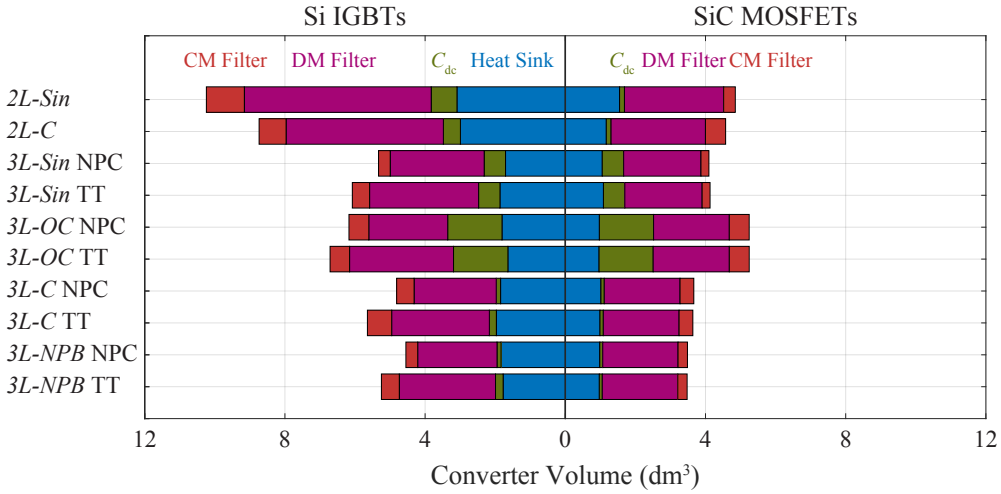

Figure 15: Shares of the individual converter parts in the total volume. The left part are the optimization results with Si IGBTs, the right part with SiC MOSFETs.

5 Conclusion

In this paper, the volume of a 30 kW PFC converter including the EMI filter is minimized for different topologies and modulation schemes. Choosing a modulation scheme is a trade-off between semiconductor losses and therefore heat sink volume and volume of the passive components. The comparison of the modulation schemes show that the *3L-NPB* modulation scheme with a NPC topology offers the best compromise of heat sink, EMI filter and DC link capacitor volume. With SiC semiconductors, the TT topology closes up to the NPC topology, while the *3L-NPB* modulation scheme increases its advantage compared to the other modulation schemes.

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