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High Output Voltage Precision PWM for Modular Multilevel Converters

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Keywords

≪Multilevel Converters≫, ≪Modulation strategy≫, ≪Pulse Width Modulation (PWM)≫

Abstract

Recently, modular multilevel conterters (MMC) are also considered for medium voltage (MV) applications, where the number of modules and the switching frequency are relatively low compared to high voltage (HV) applications. In this context, standard modulation methods can cause relatively large output voltage errors. This effect is amplified even more, if the value of the module capacitances is decreased to reduce cost and volume of the MMC. Large output voltage errors disturb the higher level closed loop control of the MMC significantly, such that control targets (e.g. keeping the circulating current zero) could not be met anymore. This paper analyses the output voltage error induced by the standard level shifted PWM method and proposes three approaches to reduce the error. All four methods are compared with respect to the error for different switching frequencies and arm currents. The effects on the closed loop performance of a current controller are investigated with time domain simulations.

1 Introduction

Originally, the Modular Multilevel Converter (MMC) has been mainly considered for HVDC or HVAC-grid applications [1, 2], as it can handle very high voltages with standard semiconductor devices. A typical structure of a three phase MMC consisting of 6 arms is shown in Fig. 1(a). Each arm represents a series connection of N modules (cf. Fig. 2(a)). For the design of the higher level control system (phase/circulating currents, arm/module voltages, ...), an arm is often substituted by a controlled voltage source and a variable capacitance as shown in Fig. 1(b) [3, 4, 5], in order to decouple the control system from the actual switching states of the modules. The modulator acts as a link between the higher level control and the switching states and provides the switching commands for the modules that generate the output voltage of the arm requested by the controller. In many standard modulation schemes [1, 6, 7], it is common practice to assume that all module voltages in one arm are equal to their mean value and thus neglect their differences when determining the duty cycle of the PWM. This enables a relatively simple modulation algorithm. Nevertheless, if the output voltage of an arm is not applied exactly as requested, the model with the controlled voltage sources as shown in Fig. 1(b) is not completely correct anymore. The difference between the actually applied output voltage and the requested one (in the following: modulation error) is a disturbance for the higher level control.

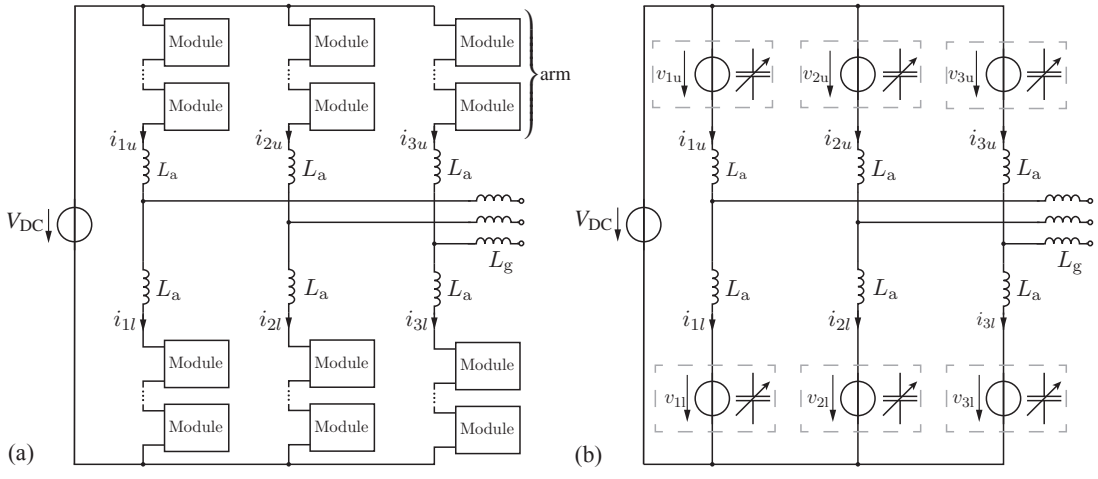

Fig. 1: (a) Three phase MMC with six arms. One arm consists of N modules. (b) The arms can be represented as (controllable) voltage sources and a variable capacitances.

In typical HV applications the high number of modules per arm and the rather high effective switching frequency enable small modulation errors resulting from the voltage deviations of the modules. However, the MMC is more and more considered also for medium voltage (MV) applications such as drives and active rectifiers [2, 8]. Here, the number of modules and the effective switching frequency are usually significantly lower compared to HV applications. This increases the duration in which module voltage deviations increase. If additionally the module capacitances are lowered within the given limits (see [9]) in order to reduce volume and cost, the deviations of the module voltages from the arms' mean module voltage increase even more.

Besides the rather static voltage differences between the individual module voltages, there is also a dynamic change in the module voltages during one switching interval of the PWM, as the module capacitors are charged or discharged by the current in the arm. Low switching frequencies, high currents and/or low module capacitances increase this effect. In addition, low module capacities require a highly dynamic control of the MMC in transients to prevent overvoltages in the modules.

In summary, the application of the well known standard level shifted PWM methods to MV MMCs can result in relatively large output voltage errors disturbing the higher level closed loop control. This can for example lead to undesired circulating currents in the steady state or overcurrents/overvoltages in transients. Hence, high precision modulation methods that reduce the error induced by the standard modulation method, which is denominated as method A in the following, are required.

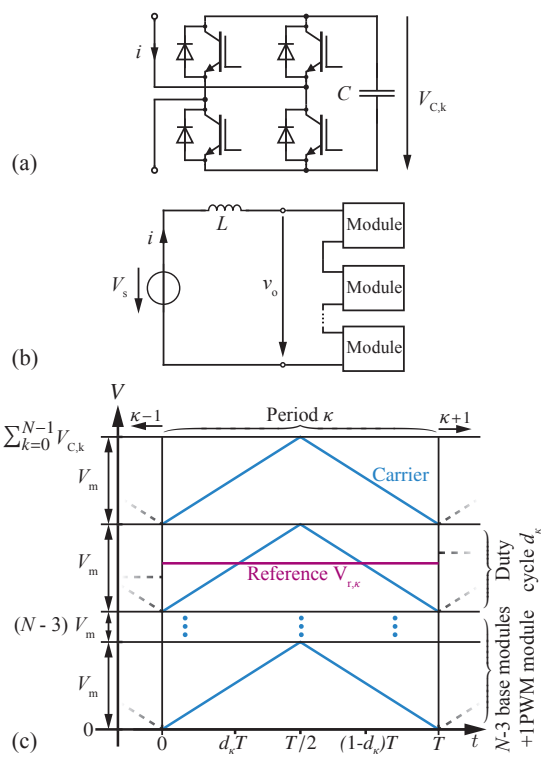

Fig. 2: (a) Full bridge realization of a single module. (b) Single arm setup. (c) Principle of the conventional level shifted MMC PWM. The reference $V_{r,\kappa}$ for the considered switching period κ defines both duty cycle d_κ of the PWM modules and the number of base modules as all module voltages are assumed to be equal to the mean module voltage $V_{C,m,\kappa}$. The PWM modules switch at $d_\kappa T$ or $(1-d_\kappa)T$ respectively.

A first step to a more precise modulation has been made in [10] by making the duty cycle dependant on the measured voltages of the individual modules (method B) in contrast to only considering the mean voltage of all modules. However, in [10] the error in the output voltage is only mentioned but not analysed in detail. Therefore in this paper, a detailed analysis of method B is presented. In addition, two advanced modulation methods C and D are presented in the following which estimate/predict the module voltages from their last available measurement and can thereby compensate the dynamic module voltage change. For all methods also the implementation complexity is investigated. The developed modulation methods use rather simple calculations that are easy to implement e.g. on FPGAs.

The paper is organized as follows: After a short introduction into conventional level shifted pulse width modulation for MMCs (section 2) and a review of the standard modulation method A, three more advanced methods (B, C and D) to perform the module selection and compute the duty cycle are developed in section 3. In section 4, the voltage-time-area error in the output voltage of one arm resulting from the four methods is analysed and evaluated. Here, different operating points in terms of the arm current, the number of modules, the mean module voltage, the switching frequency and the dynamic change of the arm current are considered. Section 5 shows how to generalize the proposed modulation methods on single or three phase MMCs before simulation results for a single phase MMC are shown in section 6. In section 7, a short comparison of the implementation effort of the methods on an FPGA is presented.

2 MMC Pulse Width Modulation

With level shifted PWM for MMCs a central controller assigns each of the MMC arms' modules to one of 3 categories. This module selection process is performed for every switching period (see Fig. 3, where the current switching period is denominated κ and has the length T). The 3 module categories are:

1. Base modules: Modules permanently inserted ('turned on') for the complete considered switching period κ.
2. PWM modules: There are 2 modules that generate the PWM part of the arm's output voltage. One of those so called PWM modules is bypassed ('turned off'), the other one is inserted during the considered period κ. The time instant when the events to bypass/insert the modules occur depends on the respective duty cycle d_κ for period κ.
3. All other modules are permanently bypassed during the complete switching period κ.

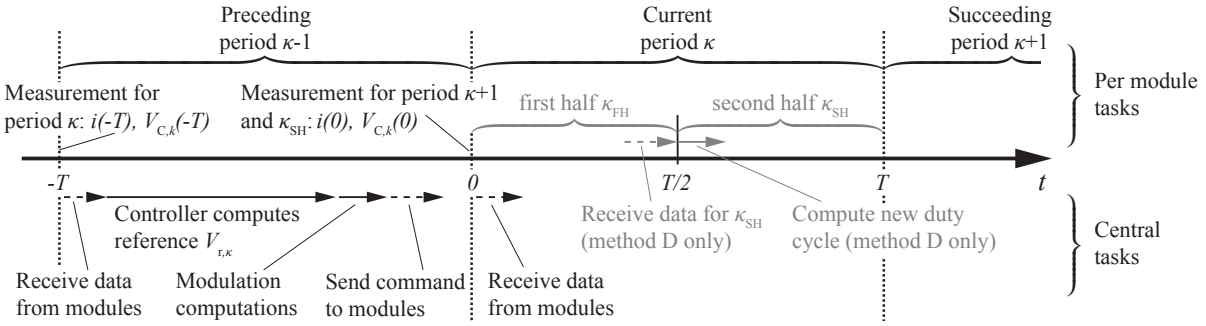

Fig. 3: Simplified timing of the measurements and computations necessary for the modulation/switching signal generation referring to the switching period κ. The arrows/tasks below the time line are executed centrally for all modules together. The ones above the time line are executed per module. The greyish tasks are performed for method D only.

The module selection process for period κ considers the individual modules' switching state (inserted or bypassed) in the preceding period $\kappa-1$ to avoid extensive switching (algorithm details are given e.g. in [10]) and the arm current direction (modules are charged or discharged) to keep all module voltages of an arm balanced. If the current is positive and would thus charge the inserted modules, the modules with the highest voltages have priority to be removed, those with the lowest voltages to be inserted [1, 6, 7].

Fig. 2(c) shows the principle often used for standard modulation schemes based on level shifted PWM. There is a triangle carrier for each of the N modules of the arm. Their levels are shifted by the mean module voltage $V_{\mathrm{m},\kappa} = \sum_{k=0}^{N-1} V_{\mathrm{C},k,\kappa}/N$, where $V_{\mathrm{C},k,\kappa}$ is the voltage of the k-th module for the κ-th period. With the number of modules (in Fig. 2(c) $N-2$) below the reference voltage $V_{\mathrm{r},\kappa}$ the number of base modules for the period κ can be derived. All but one of the modules below $V_{\mathrm{r},\kappa}$ are assigned to be base modules (in Fig. 2(c) $N-3$). The $(N-2)$-th module with the lowest/highest voltage will be bypassed within the switching period κ (PWM module). The duty cycle d_κ (or the time instance when the PWM modules are switched) is determined by the carrier that crosses $V_{\mathrm{r},\kappa}$ (cf. section 3 method A).

In this paper, the two individual PWM modules have a different carrier, as shown in the upper part of Fig. 4 for implementation reasons. The one being bypassed has a rising carrier c_{off} and the one being inserted a falling carrier c_{on}. As a consequence, duty cycles smaller than 0.5 result in the output voltage pattern shown in the middle part of Fig. 4(a). Duty cycles higher than 0.5 result in the output voltage pattern shown in the lower part of Fig. 4(b).

For the sake of brevity, in the following only one arm is considered as shown in Figure 2(b). There, the modules provide a time variant output voltage v_{o}, that is in series with an inductance L and a voltage source with the output voltage V_{s}. The generalisation of the developed modulation methods for single (two arms) or three phase (six arms) applications will be shown in sections 5/6.

3 Modulation Methods

In the following, the four different modulation methods A-D are described in detail. As shown in Fig. 4(b), the complexity increases from method A to D. Nevertheless assumptions are made that lead to rather simple equations instead of solving the complete set of differential equations of the respective LC circuits. Methods C and D are extensions of method B. Their increase of precision is a result of taking more effects into account and/or using more measured voltages/currents. For details on the timing of the measurements and the performed computations see Fig. 3.

Method A

With this relatively simple method which represents the standard for many modulation schemes, it is assumed that each module has a module voltage equal to the mean value of the arm's latest available module voltages $V_{\mathrm{m},\kappa} = {}^1\!/_N \sum_{k=0}^{N-1} V_{\mathrm{C},k}(-T)$. This assumption leads to a very simple way to determine how many base modules $n_{\mathrm{b},\kappa}$ should be inserted and how to choose the duty cycle d_κ for the switching period κ.

$$n_\kappa = \frac{V_{\mathrm{r},\kappa}}{V_{\mathrm{m},\kappa}} \qquad \Rightarrow \quad n_{\mathrm{b},\kappa} = \mathrm{floor}\{n_\kappa\} - 1 \qquad \Rightarrow \quad d_\kappa = \frac{(n_\kappa - n_{\mathrm{b},\kappa} + 1)}{2} \tag{1}$$

The modulation error of this method does not depend on the two duty cycle ranges shown in Figure 4(a). If $n_{\mathrm{b},\kappa}$ and d_κ are computed as stated in (1), it is ensured that $0 \le d_\kappa \le 0.5$.

Method B

In contrast to method A, the individual base and PWM modules are determined based on the last actually measured module voltages $V_{\mathrm{C},k}$ in method B. The carrier waveforms shown in Fig. 2(c) do not have all the same amplitude any more. Each carrier amplitude is equal to the respective module voltage. Therefore it matters, which modules

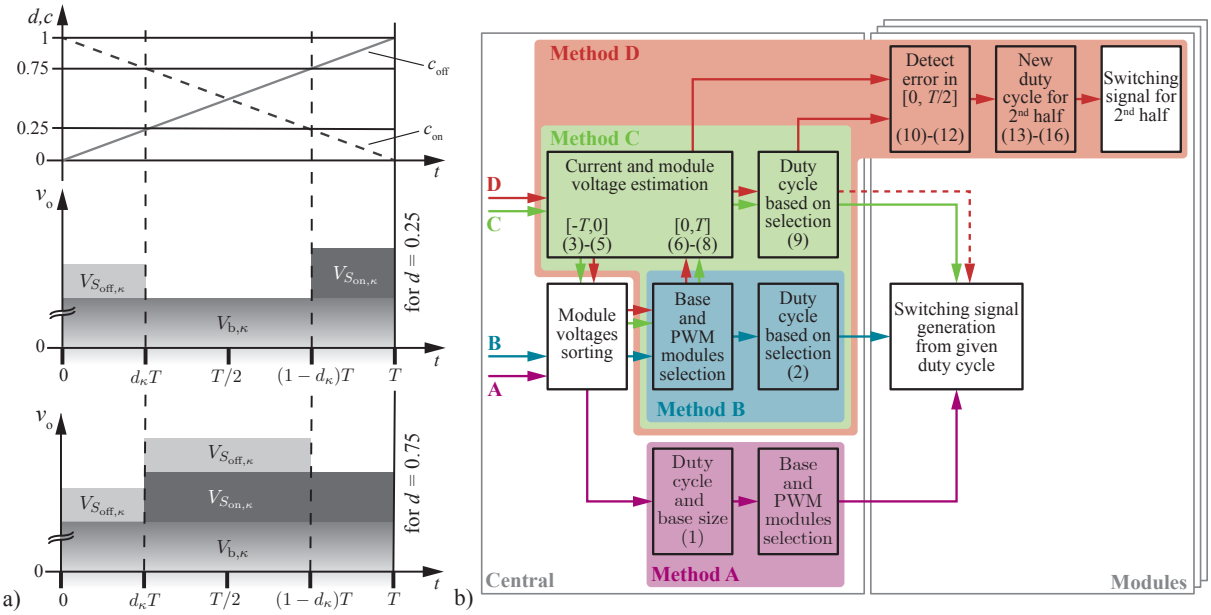

Fig. 4: (a) Result of the two ranges of the duty cycle d_κ on the arm's output voltage, where $V_{\mathrm{b},\kappa}$ is the base voltage. The upper part shows the carrier signals on the PWM modules. For the arms resulting output voltage waveform, the change in the individual module voltages has been neglected. (b) Overview on the four modulation methods. The numbers in the individual blocks show the equations applied.

are base modules and which modules are PWM modules in period κ, such that the selection of the base and the PWM modules has to be performed before determining the duty cycle d_κ. This is shown in Fig. 4(b) and is also valid for methods C and D. A possible algorithm for selecting the base and PWM modules is given in [10]. Compared to the selection algorithm for method A, method B uses an iterative approach, because the individual module voltages have to be summed up one after the other (according to their priorities as described above) to check whether enough/too much output voltage is generated or if more/less modules have to be inserted. After the selection of the base and PWM modules, the duty cycle can be computed. Note, that all values have to be measured at the beginning of period $\kappa-1$ at $t=-T$. The mean output voltage $\bar{V}_\kappa$ for period κ is

$$\bar{V}_\kappa = V_{\mathrm{b},\kappa} + d_\kappa \cdot \left(V_{S_{\mathrm{on},\kappa}}(-T) + V_{S_{\mathrm{off},\kappa}}(-T) \right) \qquad \text{, with } V_{\mathrm{b},\kappa} = \sum_{\forall k \in \text{ base in } \kappa} V_{\mathrm{C},k}(-T).$$

The applied duty cycle d_κ follows as

$$V_{\mathrm{r},\kappa} = V_{\mathrm{b},\kappa} + d_\kappa \cdot \left(V_{S_{\mathrm{on},\kappa}}(-T) + V_{S_{\mathrm{off},\kappa}}(-T) \right) \quad \Leftrightarrow \quad d_\kappa = \frac{V_{\mathrm{r},\kappa} - V_{\mathrm{b},\kappa}}{V_{S_{\mathrm{on},\kappa}}(-T) + V_{S_{\mathrm{off},\kappa}}(-T)}. \tag{2}$$

Method C

Method C is an extension of method B (Fig. 4(b)). It includes an approximation of the change of the module voltages during the preceding period $\kappa-1$ and the current period κ. First, an estimation of the module voltages at the beginning of period κ is performed. The estimation bases on the latest available measurement data from the beginning of the preceding period $\kappa-1$ and an estimation of the change of the module voltages $\Delta V_{\mathrm{C},k}$ during period $\kappa-1$. This voltage change is proportional to the mean current flowing in period $\kappa-1$. As this mean current is not known at the time of computation, an estimation is needed. Assuming that the output voltage of period $\kappa-1$ is equal to its reference voltage $V_{\mathrm{r},\kappa-1}$, the current $\hat{i}(0)$ at the end of the preceding period $\kappa-1$ is

$$\hat{i}(0) = i(-T) + \frac{V_{\mathrm{s},\kappa-1} - V_{\mathrm{r},\kappa-1}}{L} \cdot T. \tag{3}$$

Based on (3), the mean current during period $\kappa-1$ can be estimated to be equal to the mean value of $i(-T)$ and $\hat{i}(0)$:

$$\hat{i}_{\kappa-1} = \frac{i(-T) + \hat{i}(0)}{2} = i(-T) + \frac{V_{\mathrm{s},\kappa-1} - V_{\mathrm{r},\kappa-1}}{L} \cdot \frac{T}{2} \tag{4}$$

With this current estimation, the module voltages at the beginning of period κ can be computed based on the latest available measurement data at $t = -T$. For the modules switching during period $\kappa - 1$, the mean current $\hat{i}_\kappa$ from (6) is assumed to dis-/charge the capacitances only during the time the modules are actually inserted. Their voltage change is scaled with the duty cycle $d_{\kappa-1}$:

$$\hat{V}_{\mathrm{C},k}(0) = V_{\mathrm{C},k}(-T) + \Delta\hat{V}_{\mathrm{C},k,\kappa-1} \quad \text{with } \Delta\hat{V}_{\mathrm{C},k,\kappa-1} = \begin{cases} {}^{T}/_{C} \cdot \hat{i}_{\kappa-1} & k \in \text{ base in } \kappa-1 \\ {}^{T}/_{C} \cdot \hat{i}_{\kappa-1} \cdot d_{\kappa-1} & k = S_{\mathrm{on},\kappa-1} \text{ or } k = S_{\mathrm{off},\kappa-1} \\ 0 & \text{otherwise} \end{cases} \tag{5}$$

Here, C is the capacitance of a single module (assumed to be all equal for the sake of brevity). The base modules to generate $V_{\mathrm{b},\kappa}$ as well as the PWM modules for period κ can now be determined just as described for method B using the estimated voltages $\hat{V}_{\mathrm{C},k}(0)$ instead of the measured voltages $V_{\mathrm{C},k}(-T)$ (cf. Fig 4(b)).
To compute d_κ also the future change in the module voltages during period κ has to be considered. Here, the same approximation as in (3), (4) for the mean current (dis-)charging the modules is used, such that

$$\hat{i}_\kappa = \hat{i}(0) \; + \; \frac{V_{\mathrm{s},\kappa} - V_{\mathrm{r},\kappa}}{L} \cdot \frac{T}{2} \tag{6}$$

is the predicted mean current during period κ. Similar to (5) the mean value of the base voltage during period κ results in

$$\hat{V}_{\mathrm{b},\kappa} = \sum_{\forall k \in \text{ base in } \kappa} \hat{V}_{\mathrm{C},k}(0) \; + \; \hat{i}_\kappa \cdot \frac{T}{2} \cdot \frac{N_{\mathrm{b},\kappa}}{C}, \tag{7}$$

where $N_{\mathrm{b},\kappa}$ is the number of base modules in κ. For the modules switching during period κ the same assumptions as in (5) are made, such that their mean voltages are predicted as

$$\hat{V}_{S_{\mathrm{off},\kappa}} = \hat{V}_{S_{\mathrm{off},\kappa}}(0) + d_\kappa \cdot \frac{T}{2} \cdot \frac{\hat{i}_\kappa}{C} \,, \qquad\qquad \hat{V}_{S_{\mathrm{on},\kappa}} = \hat{V}_{S_{\mathrm{on},\kappa}}(0) + d_\kappa \cdot \frac{T}{2} \cdot \frac{\hat{i}_\kappa}{C}. \tag{8}$$

With these expressions, the mean output voltage for period κ is approximated as

$$\bar{v}_{\mathrm{o},\kappa} = \hat{V}_{\mathrm{b},\kappa} + d_\kappa \cdot \left(\hat{V}_{S_{\mathrm{off},\kappa}} + \hat{V}_{S_{\mathrm{on},\kappa}} \right) = \hat{V}_{\mathrm{b},\kappa} + d_\kappa \cdot \left(\hat{V}_{S_{\mathrm{off},\kappa}}(0) + \hat{V}_{S_{\mathrm{on},\kappa}}(0) + d_\kappa \cdot T \cdot \frac{\hat{i}_\kappa}{C} \right). \tag{9}$$

One can now set this expression equal to $V_{\mathrm{r},\kappa}$ and solve it for d_κ.
As mentioned above, the module selection algorithm is the same as for method B just using the estimated module voltages for $t = 0$. As the duty cycle d_κ is now dependant on the estimation of the module voltages during κ, it might happen, that d_κ saturates at 0 or 1, as the module selection did not take this estimation into account. Therefore, the allowed duty cycle is restricted the during module selection process to $d_\kappa \in [\delta, 1-\delta]$ to leave some margin for module voltage changes. The value for δ has to be tuned manually dependant on the maximum current and the module capacitance C in the considered application.

Method D

The most advanced method D extends method C by a duty cycle correction for the module which is switching in the second half κ_{SH} of the period κ (cf. Fig. 3). It recomputes the duty cycle with new measurement data of the arm current/module voltages available at $t = {}^{T}/_{2}$. For the first half κ_{FH} all switching events are determined just as with method C (cf. Fig. 4(b)). The error in the voltage time area that evolves during the first half κ_{FH} of the switching period κ can be compensated by the module switching in the second half κ_{SH}. Here the actual current waveform during the switching period κ is important. As will be shown, the average current flowing in the second half κ_{SH} of the period might differ strongly from the one in the first half κ_{FH}, such that the assumptions made for the current for method C have to be modified. The arm current is continuously measured and thus one can determine the voltage change of the modules during the fist half period κ_{FH} with

$$\Delta\hat{V}_{\mathrm{C},\kappa_{\mathrm{FH}},k} = \begin{cases} {}^{1}/_{C} \cdot \int_0^{T/2} i(t)dt & k \in \text{base in } \kappa \text{ or } (k = S_{\mathrm{off},\kappa} \text{ and } d_\kappa > 0.5) \\ {}^{1}/_{C} \cdot \int_0^{T/2} i(t)dt & k = S_{\mathrm{off},\kappa} \text{ and } t \le d_\kappa T \text{ and } d_\kappa < 0.5 \\ {}^{1}/_{C} \cdot \int_0^{d_\kappa T} i(t)dt & k = S_{\mathrm{off},\kappa} \text{ and } t > d_\kappa T \text{ and } d_\kappa < 0.5 \\ {}^{1}/_{C} \cdot \int_{(1-d_\kappa)T}^{T/2} i(t)dt & k = S_{\mathrm{on},\kappa} \text{ and } t \ge (1-d_\kappa)T \text{ and } d_\kappa > 0.5 \\ 0 & \text{otherwise} \end{cases} \tag{10}$$

$\forall k \in [0,\dots,N-1]$. The measurements of all module voltages $V_{\mathrm{C},k}(0)$ are assumed to be known before half of the switching period has passed (see Fig. 3), such that the total module voltages can be computed with (10) as

$$\hat{V}_{\mathrm{C},k}(T/2) = V_{\mathrm{C},k}(0) + \Delta\hat{V}_{\mathrm{C},\kappa_{\mathrm{FH}},k} \qquad \forall k \in [0,\dots,N-1]. \tag{11}$$

With (10) and (11) an estimation of the actual output voltage $\hat{V}_{\mathrm{o},\kappa_1}$ during the first half of period κ can be performed:

$$\begin{aligned}\hat{V}_{\mathrm{o},\kappa_{\mathrm{FH}}} = & \sum_{\forall k \in \text{ base in } \kappa} \left(V_{\mathrm{C},k}(0) + \Delta\hat{V}_{\mathrm{C},\kappa_{\mathrm{FH}},k}/2\right) \\ & + \begin{cases} 2\cdot d_\kappa \cdot \left(V_{\mathrm{C},S_{\mathrm{off},\kappa}}(0) + \Delta\hat{V}_{\mathrm{C},\kappa_{\mathrm{FH}},S_{\mathrm{off},\kappa}}/2\right) & d_\kappa \le 0.5 \\ \left(V_{\mathrm{C},S_{\mathrm{off},\kappa}}(0) + \Delta\hat{V}_{\mathrm{C},\kappa_{\mathrm{FH}},S_{\mathrm{off},\kappa}}/2\right) + (2\cdot d_\kappa - 1)\cdot\left(V_{\mathrm{C},S_{\mathrm{on},\kappa}}(0) + \Delta\hat{V}_{\mathrm{C},\kappa_{\mathrm{FH}},S_{\mathrm{on},\kappa}}/2\right) & d_\kappa > 0.5 \end{cases}\end{aligned} \tag{12}$$

Here, the mean output voltage of the k-th module is assumed to be equal to the mean value of $V_{\mathrm{C},k}(0)$ and $\hat{V}_{\mathrm{C},k}(T/2)$. The PWM modules that switch during κ_{FH} are additionally scaled by two times the duty cycle $2\cdot d_\kappa$ (cf. Fig. 4), to account for their shorter insertion time. The factor of 2 is caused by looking at half of the switching period $T/2$ only, such that the duty cycle is virtually doubled compared to T.
The error of the output voltage in comparison with the reference voltage $V_{\mathrm{r},\kappa}$ is $V_{\mathrm{e},\kappa_{\mathrm{FH}}} = \hat{V}_{\mathrm{o},\kappa_{\mathrm{FH}}} - V_{\mathrm{r},\kappa}$, such that the reference voltage for the second half is

$$V_{\mathrm{r},\kappa_{\mathrm{SH}}} \;=\; V_{\mathrm{r},\kappa} - V_{\mathrm{e},\kappa_{\mathrm{FH}}} \;=\; 2\cdot V_{\mathrm{r},\kappa} - \hat{V}_{\mathrm{o},\kappa_{\mathrm{FH}}} \tag{13}$$

in order to compensate this error.
As shown in Fig 5, the current in the second half of the period can strongly differ from the current in the first half due to the current ripple. Therefore, an estimation of the mean current that (dis-)charges the modules during the second half of the period κ_{SH} is presented in the following. As a reference for the current at the end of the period, $i_{\mathrm{r}}(T)$, one can write

$$i_{\mathrm{r}}(T) = i(0) + \frac{V_{\mathrm{r},\kappa} - V_{\mathrm{s},\kappa}}{L}\cdot T, \tag{14}$$

where it is assumed that the reference voltage $V_{\mathrm{r},\kappa}$ is fulfilled at the end of period κ. The red curve in Figure 5 represents $^2/_T \int_0^t i(\tau) - i(0) d\tau$.

$$\alpha = \frac{2}{T}\int_0^{T/2} i(t) - i(0) dt \;-\; \frac{i(T/2) - i(0)}{2} \;=\; \frac{2}{T}\int_0^{T/2} i(t) dt \;-\; \frac{i(0) + i(T/2)}{2} \tag{15}$$

Eqn. (15) determines the mean value of the current in the first half of the period minus the mean value of the dashed green line connecting $i(0)$ and $i(T/2)$. The current waveform in the second half has very similar characteristics to the one of the first half, such that α can be used as a measure for the mean value of the current in the second half. Assuming that the current is equal to the reference current given in (14) in the end of period κ, the following equation

$$\hat{i}_{\kappa_{\mathrm{SH}}} = \frac{i_{\mathrm{r}}(T) + i(T/2)}{2} \;-\; \alpha \tag{16}$$

is a good approximation for the mean current during the second half κ_{SH} of the period (cf. Fig. 5). As α indirectly represents the current ripple that is caused by the voltage of the switched modules, the approximation can be improved, by scaling α with the voltage that is actually switched in the second half to get α_{SH}:

$$\alpha_{\mathrm{SH}} = \frac{V_{S_{\mathrm{on/off},\kappa}}(T/2)}{\hat{V}_{S_{\mathrm{off/on},\kappa}}(T/2)}\cdot\alpha_{\mathrm{FH}}$$

Here, α_{FH} represents the α from (15) and $\hat{V}_{S_{\mathrm{off/on},\kappa}}(T/2)$ from (10), (11) with $k = S_{\mathrm{off/on},\kappa}$.
Now, the duty cycle for the second half can be recomputed with the procedure from (6) - (9) using the corrected reference voltage V_{r,κ_2} from (13), the estimation

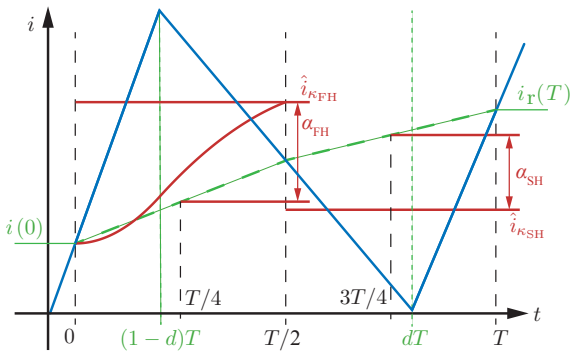

Fig. 5: Approximated current waveform (blue) during a switching period when considering one arm. Note that the slope from $t = 0\dots(1-d)T$ is not equal to the slope from $t = dT\dots T$. This is the result of the non equal module voltages of the PWM modules. Also the slope of the dashed green line is different for each half of the switching period.

of the module voltages $\hat{V}_{C,k}(T/2)$ from (10), (11) and the mean current estimation from (16).
The continuous current measurement can be realized centrally, so that the data is directly communicated to a central controller. Consequently, the duty cycle for the second half of the switching period is computed centrally. Another possibility is to install computational power and a current measurement on the modules, such that the module that switches in the second half κ_{SH} can compute its duty cycle locally. Often the computational power is anyway available due to the needs of the communication and the modules' local protection system (e.g. [11, 12]).

4 Comparison of the Output Voltage Errors

The resulting voltage errors of the four introduced PWM methods are analysed and evaluated for the following different conditions:

1. Variations of the switching frequency $f_{sw} = 1/T \in \{2, 5, 10, 15\}$ kHz
2. The arm current i at the beginning of the switching period and the reference voltage $V_{r,\kappa}$ are varied ($\rightarrow$ varying di/dt).
3. The module voltages $V_{C,k}$ randomly vary around a mean value $V_{C,m}$ with a maximum deviation ε, such that $V_{C,k} \in [V_{C,m} - \varepsilon, V_{C,m} + \varepsilon]\ \forall k$.
4. The module number N, the capacitance C per module and the inductance L are kept fixed.

With this analysis, the performance depending on the operation point can be shown for the different methods. The evaluation relies on a simulation, where the methods deal with the same current as well as module and reference voltages. In total 880,000 combinations were computed for each switching frequency. The simulations consider the single arm setup as shown in Fig. 2(b). All measurements (voltages and currents) are assumed to be ideal (no delays, infinite bandwidth), as well as the module capacitance and the inductance to be known exactly. The switches are assumed to be ideal.
Fig. 6 shows the absolute value of the mean error in the output voltage for all tested combinations:

$$V_{err} = \text{mean}\{\left| V_{r,\kappa} \cdot T - \int_0^T v_o(t)dt \right|\}/T$$

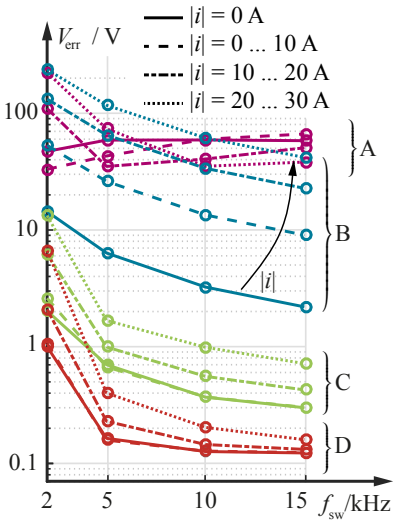

Fig. 6: Comparison of the modulation error for the four methods. The values correspond to the mean absolute value of the modulator error for 880,000 combinations per switching frequency. The error of the individual methods is plotted for different current ranges. Parameters: $N = 10$, $C = 162\,\mu$F per module and $L = 20$ mH. The mean module voltage $V_{C,m,\kappa}$ varies between $0.9 - 1.1$ kV The module voltage deviation ε is limited to 5 % of $V_{C,m,\kappa}$.

Looking at Fig. 6, it is clear, that methods C and D outperform methods A and B. Method B can only improve the results of method A, if the arm current stays below 10 A. For higher currents and switching frequencies below 10 kHz, method A is not worse or even better than method B. Of course this strongly depends on the maximum module voltage deviation $\varepsilon \cdot V_{C,m}$, the switching frequency and the current value. If possible, the sorting algorithm prefers to insert modules that have a voltage that is lower than the mean module voltage $V_{C,m}$, when the current is positive. Consequently, the assumption that all module voltages are equal to $V_{C,m}$ can be correct, because the module capacitances are charged since the last measurement and during the switching period κ. If the current becomes too high or the switching period is too long, this causes an 'overcompensation' of the ignored module voltage deviation, such that A is not better than B anymore (cf. A and B for $f_{sw} = 2$ kHz and $|i| = 20...30$ A). For too short switching periods, 'undercompensation' happens instead (cf. A and B for $f_{sw} = 15$ kHz and $|i| = 10...20$ A). Method C generally reduces the modulation error compared to method A and B by a factor of approx. $10 - 20$ (reduction by $90 - 95$ %). In addition, the error is much less dependant on the current. For method C, the switching frequency is a crucial factor: As the inductance L and the mean module voltage $V_{C,m}$ are the same for all switching frequencies, the current ripple linearly increases with $1/f_{sw}$. Equation (8) does not include the individual mean current for the PWM modules, which gets crucial for a current ripple becoming a considerable part of the mean current (cf. Fig. 5).
Method D has a by a factor of approx. $2 - 5$ (reduction by $50 - 80$ %) lower output voltage error than method C in all considered current ranges and switching frequencies. It reveals the same problems regarding the influence of the current ripple on the individual PWM modules as method C. Therefore, the error also increases with lower switching frequencies.

5 Application on Single or Three Phase MMCs

Every arm of a single or three phase MMC can be reduced to the single arm setup considered in the previous sections as will be exemplary shown for a single phase MMC in the following. The differences to the single arm setup in the previous sections are the additional voltage source v_g and the coupling of the two arms via L_g. Looking at Fig. 7, one can observe

$$\frac{V_\mathrm{dc}}{2} = v_\mathrm{u} + v_\mathrm{g} + \left(L_\mathrm{a}+L_\mathrm{g}\right)\cdot\frac{di_\mathrm{u}}{dt} - L_\mathrm{g}\cdot\frac{di_\mathrm{l}}{dt} \qquad \text{and} \qquad \frac{V_\mathrm{dc}}{2} = v_\mathrm{l} - v_\mathrm{g} + \left(L_\mathrm{a}+L_\mathrm{g}\right)\cdot\frac{di_\mathrm{l}}{dt} - L_\mathrm{g}\cdot\frac{di_\mathrm{u}}{dt},$$

given that $i_\mathrm{g} = i_\mathrm{u} - i_\mathrm{l}$. For each arm's output voltage v_u and v_l the reduction

$$(1+\frac{L_\mathrm{g}}{L_\mathrm{g}+L_\mathrm{a}})\cdot\frac{V_\mathrm{dc}}{2} - \frac{L_\mathrm{a}}{L_\mathrm{g}+L_\mathrm{a}}\cdot v_\mathrm{g} - \frac{L_\mathrm{g}}{L_\mathrm{g}+L_\mathrm{a}}\cdot v_\mathrm{l} = v_\mathrm{u} + \frac{L_\mathrm{a}^2+2L_\mathrm{a}L_\mathrm{g}}{L_\mathrm{g}+L_\mathrm{a}}\cdot\frac{di_\mathrm{u}}{dt} \tag{17}$$

$$\underbrace{(1+\frac{L_\mathrm{g}}{L_\mathrm{g}+L_\mathrm{a}})\cdot\frac{V_\mathrm{dc}}{2} + \frac{L_\mathrm{a}}{L_\mathrm{g}+L_\mathrm{a}}\cdot v_\mathrm{g} - \frac{L_\mathrm{g}}{L_\mathrm{g}+L_\mathrm{a}}\cdot v_\mathrm{u}}_{V_\mathrm{s}} = v_\mathrm{l} + \underbrace{\frac{L_\mathrm{a}^2+2L_\mathrm{a}L_\mathrm{g}}{L_\mathrm{g}+L_\mathrm{a}}\cdot\frac{di_\mathrm{l}}{dt}}_{L\cdot\frac{di}{dt}} \tag{18}$$

can be found. This is equivalent to a single arm as shown in Fig. 2(b), such that methods C and D can be applied here as well. For a three phase MMC the procedure is very similar.

6 Simulation Results

Simulation results for the single phase MMC setup given in Fig. 7 are shown in Fig. 8. All measurements and switches are assumed to be ideal. All modulators receive their reference values from equal control systems, where the circulating and the phase current are controlled by individual LQI-controllers.

For all four modulation methods the module voltages are well balanced. The voltage difference between the individual module voltages in one arm is relatively small at any time. The modulation error of the different modulation methods match the computations discussed in section 4. Methods A and B behave quite similar. Method B does not decrease the modulation error of method A, due to the low difference in the module voltages and the rather high arm currents. The dependence of the modulation error on the arm current is clearly visible. The effect of the modulation error on the closed loop performance is shown using the circulating current as an example. The circulating current is supposed to be controlled to $5.25\,\mathrm{A_{DC}}$ (too keep the AC and DC power equal). Here, the less random and thereby more static error of method B is beneficial, because the controller can compensate this.

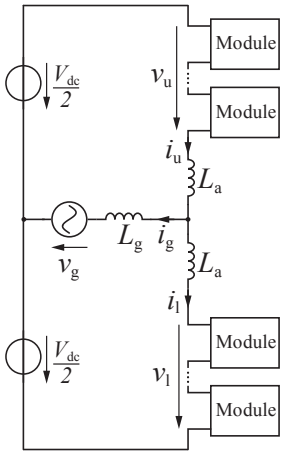

Fig. 7: Single phase MMC setup as used for the simulation model.

Method C shows a very good behaviour compared to A and B. The error is reduced by a factor of 10 - 20. This improves the closed loop performance a lot. Due to the much smaller disturbance, the controller is able to keep the circulating current much closer to its reference. The error of method C is dependant on the arm current slope. It has its maximum during the zero crossing and its minimum during the flat top of the phase current.

Compared to the very well performing method C, method D reduces the modulation error again by a factor of 5 - 10 with the result of eliminating the effect of the disturbance on the control of the circulating current. The error is now also independent of the arm current slope. At $t \approx 29\,\mathrm{ms}$ a larger error can be observed. This is due to the assumption that the recomputation of the duty cycle cannot be performed infinitely fast, such that for $0.45 < d_\kappa < 0.55$ no adjustment can be performed to the duty cycle d_κ in the second half, because the switching event may already have passed (cf. Fig. 3). Then larger errors result that become comparable to those of method C.

7 Implementation Effort

Methods A, B and C have been implemented for a single arm setup on an Altera Cyclone V FPGA. Table I gives an overview on the hardware effort for the implementation (Number of ALMs[1] can be seen as an example for the general trend) and the clock cycles needed for the computation. It includes a bubble sort algorithm, the module selection and the computations for the duty cycle but not the generation of the actual switching signals on gate level. The column for method D is an estimation based on the values for method C.

[1] Altera "Adaptive Logic Module" (cf. `https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/cyclone-v/cv_5v2.pdf`)

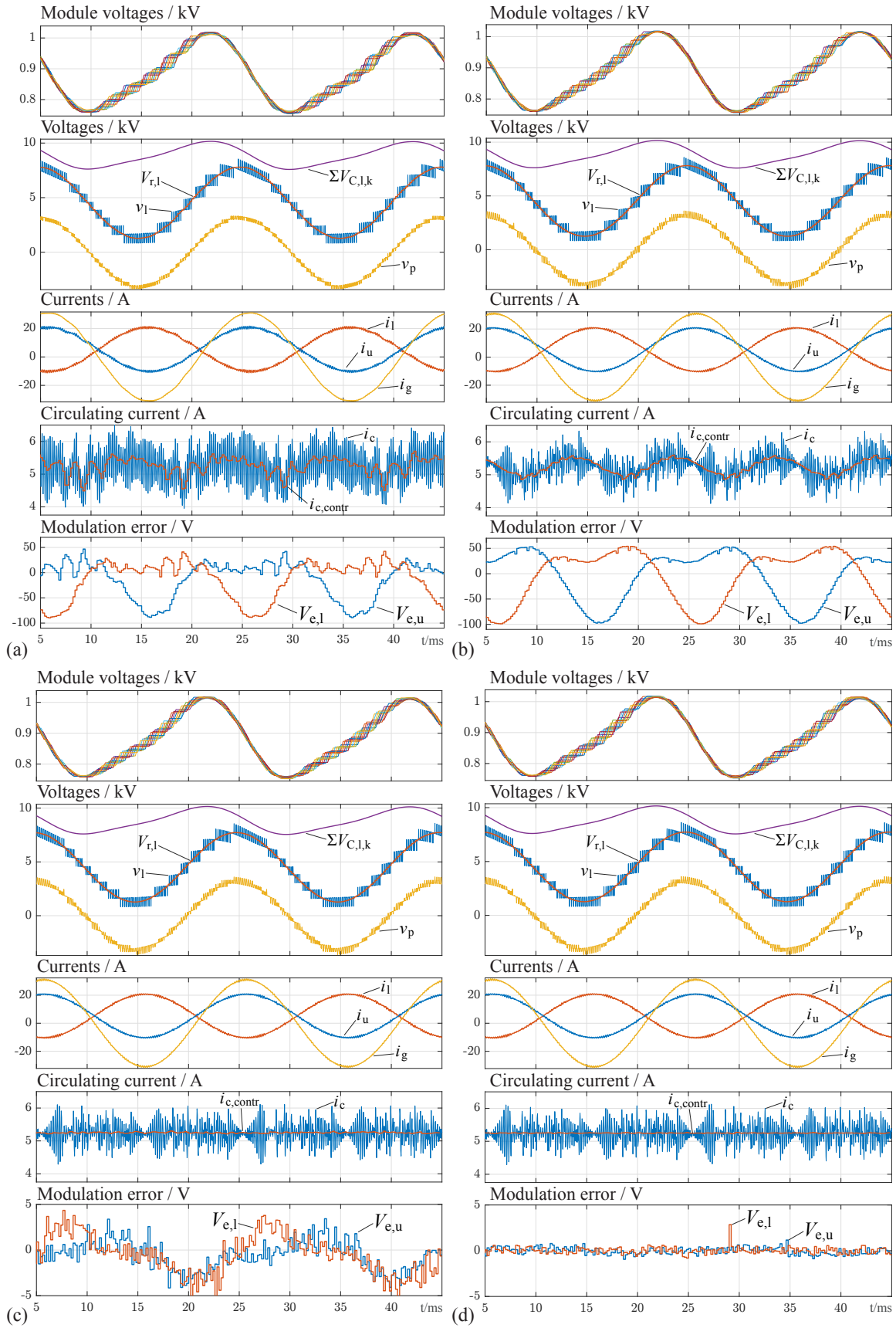

Fig. 8: Simulation results for the four modulation methods based on a single phase setup as shown in Fig. 7.
Converter data: $N = 10$ modules per arm, $T = 1/5\,\mathrm{kHz}$, $L_g = 20\,\mathrm{mH}$, $L_a = 20\,\mathrm{mH}$, $C = 162\,\mu\mathrm{F}$. Mind that (c) and (d) have a much smaller scaling of the modulation error compared to (a) and (b).

8 Conclusion

When decreasing the value of the module capacitances of an MMC and/or when applying high dynamic control on MMCs, modulators, that keep the modulation error in the output voltage small are required. In this paper, three advanced PWM modulation methods B, C and D are presented and compared with the standard level shifted PWM method A. The new methods rely on a prediction of the future output voltage regarding the arm current that (dis-)charges the MMC's module capacitances within one switching period. Depending on the converter's operating point, the proposed advanced modulation methods C and D reduce the mean error of the output voltage of an MMC arm by more than 95 % compared to the simpler methods A and B without requiring complicated computations. Method C does not even need a special measurement setup, since all input parameters are usually required for the higher level MMC control system anyway. Method D requires either a very fast control of the modules from a central control unit with a direct connection to each module or current sensing as well as computational power on the modules. This results in a error reduction of more up to 75 % compared to method C. The performance of all described methods has been evaluated using simulations of a single arm setup. As has been shown in time domain simulations, all methods can be used also in single or three phase systems without changing the basic concept. The simulations also show the exemplary effect of the reduction of the modulation error on the closed loop control of the circulating current.

Table I: Hardware effort and worst case computation time of the implementation of the modulation methods on an FPGA for $N = 15$ with $t_{\mathrm{clk}} = 8\,\mathrm{ns}$.

Method	ALMs	Computation time [clk-cycles]
A	935	$3+2N+N^2+\text{division}$
B	1420	$6+4N+N^2+\text{division}$
C	3635	$59+5N+N^2$
D	app. 6000	app. method C $+50+N$

References

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conf.*, vol. 3, June 2003.

[2] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. on Power Electronics*, 2015.

[3] H. Bärnklau, A. Gensior, and J. Rudolph, "A model-based control scheme for modular multilevel converters," *IEEE Trans. on Industrial Electronics*, vol. 60, no. 12, Dec 2013.

[4] L. Ängquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H. P. Nee, "Open-loop control of modular multilevel converters using estimation of stored energy," *IEEE Trans. on Industry Applications*, vol. 47, no. 6, Nov 2011.

[5] D. Siemaszko, A. Antonopoulos, K. Ilves, M. Vasiladiotis, L. Angquist, and H. P. Nee, "Evaluation of control and modulation methods for modular multilevel converters," in *Int. Power Electronics Conf. (IPEC)*, June 2010.

[6] Z. Li, F. Gao, F. Xu, X. Ma, Z. Chu, P. Wang, R. Gou, and Y. Li, "Power module capacitor voltage balancing method for a 350-kV/1000-MW modular multilevel converter," *IEEE Trans. on Power Electronics*, vol. 31, no. 6, June 2016.

[7] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. on Industrial Electronics*, vol. 57, no. 8, Aug 2010.

[8] J. Kolb, F. Kammerer, and M. Braun, "Dimensioning and design of a modular multilevel converter for drive applications," in *International Power Electronics and Motion Control Conf. (EPE/PEMC)*, 2012.

[9] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. on Power Electronics*, vol. 29, no. 1, January 2014.

[10] H. Fehr, A. Gensior, and S. Bernet, "Experimental evaluation of PWM-methods for modular multilevel converters," in *18th European Conf. on Power Electronics and Applications (EPE)*, 2016.

[11] C. Carstensen, R. Christen, H. Vollenweider, R. Stark, and J. Biela, "A converter control field bus protocol for power electronic systems with a synchronization accuracy of 5ns," in *17th Europ. Conf. on Power Electronics and Applications (EPE)*, Sept 2015.

[12] A. Hillers, H. Tu, and J. Biela, "Central control and distributed protection of the dsbc and dscc modular multilevel converters," in *IEEE Energy Conversion Congress & Expo (ECCE)*, Sept. 2016.