Flexible, Highly Dynamic, and Precise 30-kA Arbitrary Current Source

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Flexible, Highly Dynamic, and Precise 30kA Arbitrary Current Source

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***Abstract*—High power current sources with high dynamic performance, ultra-low current ripple and absolute reference tracking accuracy are key elements for magnets (bumper, septum) that are used in accelerators. Similar requirements are also encountered in plasma research applications in fusion reactors as well as plasma research for future HVDC circuit breakers. There, the current source must be able to drive resistive/inductive and highly fluctuating loads without any compromise in its performance. In this paper, such a flexible, dynamic and accurate current source, able to provide amplitudes up to 30kA and bipolar voltages up to 10kV is introduced. The system's operating concept is presented and its design procedure in order to fulfill a list of demanding specifications is demonstrated. In addition, a detailed description of its near-optimal, advanced control system is presented. Finally, the theoretical considerations are verified by extensive simulation results for various operating scenarios, including driving chaotic arc loads.**

***Index Terms*—Accelerator Magnets, Arc Modeling, Current Sources, Modular Power Converters, Plasma Sources, Power Supplies**

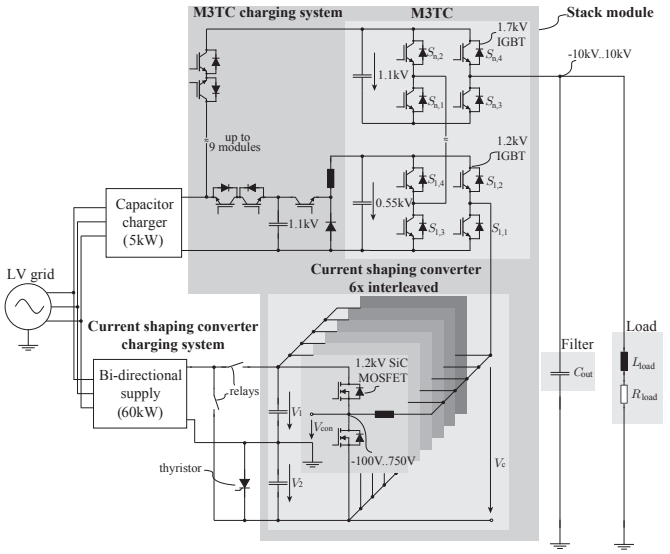

Fig. 1: Stack module of the proposed modular pulsed current source, with 1.5kA nominal current, ±10kV output voltage per stack. The full-scale source consists of 20 parallel stacks with a nominal current of 30kA.

I. Introduction

HIGH power current sources able to generate fast current gradients combined with ultra-low current ripple and absolute accuracy at steady state are required for generating the magnetic fields for beam deviation in accelerators with bumper and septum magnets [1]. These magnets typically are purely inductive loads with inductance values ranging between a few µH up to a few mH [2]. They require [3]–[6]:

a) Current amplitudes ranging between a few hundreds A up to tens of kA
b) Fast rise and fall times of some hundreds of µs
c) High precision at flat-top, often below 100ppm

For the generation of the high current gradient, a high output bipolar voltage is required while the flat-top current needs to be precisely controlled in order to avoid inaccuracies.

Similar requirements in terms of current rating, flat-top accuracy and rise/fall times are encountered in plasma confinement technologies for fusion applications where the position of the plasma is controlled via the magnetic field produced by large inductive loads [7], [8].

Likewise, Magnetic Resonance Imaging (MRI) systems have particularly high requirements with respect to their power supply system. In MRI systems, magnetic field gradients are generated with coils that typically have an inductance around 1mH). The quality of the image is related to the accuracy of the current that generates the magnetic fields, the resolution of the image is related to the current amplitude and the imaging duration is related to the current gradient through the coil [9]. Typically, several kA are needed with a current gradient higher than 2.5A/µs and an accuracy higher than 500ppm [10].

Furthermore, precise and highly dynamic current sources able to generate arbitrary current waveforms with similar requirements are required nowadays for research purposes on next generation DC circuit breakers [11], [12]. More specifically, the development and optimization of HVDC circuit breakers is particularly challenging because the chaotic behavior and the unknown properties of the DC-arc impose additional challenges in the development of accurate models for circuit breakers, that could facilitate a numerical optimization of the system [13], [14]. For accurate modeling, the properties of the DC-arc need to be investigated in order to gain a better understanding of its behavior [15]. However, DC-arc investigations require current sources with the ability to drive highly fluctuating dynamic loads (DC-arc). In [16] and [17], the operation of a small-scale current source is described along with the target requirements of a full-scale source.

Based on the mentioned applications, a set of specifications for a flexible, multi-purpose, modular current source has been determined, as shown in Table I. The investigated full-scale source consists of 20 stack modules connected in parallel. Each stack module increases the current capability of the system by 1.5kA. Apart from the full-scale specifications, Table I displays the specifications of a stack module. In [18] and [19], a novel topology that could be used as a current

TABLE I: Requirements for different applications and target specifications of the investigated flexible current source. A full-scale source consists of 20 parallel stack modules.

	Applications			Flexible current source	
Parameter	**Bumper/Septum magnets**	**MRI**	**HVDC circuit breakers**	**Stack module**	**Full-scale**
Nominal output current	**<35kA**	<2kA	30kA	1.5kA	30kA
Nominal output voltage	**<10kV**	<2kV	**10kV**	10kV	10kV
Output voltage polarity	**Bipolar**	**Bipolar**	Unipolar	Bipolar	Bipolar
Current gradient rise/fall	**<200A/µs**	<2.5A/µs	**200A/µs**	>10A/µs	>200A/µs
Flat top ripple	**100ppm**	500ppm	10000ppm	<100ppm	<10ppm
Flat top accuracy	**100ppm**	500ppm	100000ppm	<100ppm	<10ppm
Load type	L	L	**R/L/Dynamic**	R/L/Dynamic	R/L/Dynamic
Current waveform	**Controllable**	**Controllable**	**Controllable**	Controllable	Controllable

source converter for such applications has been introduced. There, a current-shaping converter, that controls the output current of the system, is used in series with a Modular Multilevel Marx-type converter (M3TC) in order to generate the required high output voltage. However, the relatively simple applied control method (interleaved PI control) limited the dynamic performance of the system and its robustness under load disturbances (e.g. dynamic loads).

Based on those results, a flexible, modular topology for generating high current pulses with high gradients during transient operation and ultra-low ripple during steady state, is presented in [20], where a novel control system is discussed. The combination of an optimal design and a near-optimal control enables the use of the topology's full potential and ensure that the requirements are met without compromising the stability of the system even in case of sudden load changes [21].

The contributions of this paper are: i) the description of the analytical design procedure of the current source in order to fulfill its dynamic and flat-top requirements, ii) the detailed presentation of its advanced control system in order to cope with various types of loads, without compromising its overall performance and iii) the verification of the theoretical considerations through detailed simulation results, including driving highly fluctuating loads (i.e. DC-arc). Additionally, the simulation results demonstrate the suitability of the designed current source in a wide range of applications.

This paper is structured as follows: Section II presents an overview of the converter system and its basic operating principle. Section III describes the analytic design procedure and the choice of the main parameters of the system. Section IV provides a description of the complete control system of the current source. In section V, the simulation results of the system under various operating conditions are shown. Finally, section VI summarizes the main conclusions and contributions of the paper.

II. Operating Principle

This section introduces the basic topology of a stack module of the current source (Fig. 1) and describes its basic operation principle. At first, each stack of the current source consists of a current-shaping converter connected in series with the Modular Marx-Type Multilevel Converter (M3TC). The current-shaping converter is responsible for controlling the current, shaping arbitrary current waveforms and is able to provide a highly dynamic current. On the other hand, the M3TC is responsible for generating a high staircase output voltage by inserting or bypassing the pre-charged capacitors. The equivalent circuit of Fig. 2 gives a simplified overview of the operation of the topology.

As current-shaping converter, a multi-phase interleaved 2-level buck-type converter with split DC-link is chosen. The split DC-link is used in order to allow controllability of the current waveform when the output voltage of the converter V_c is around 0V and enhances the dynamic performance of the system during step-down transients. In this way the buck-type converter can generate $V_{con} = \{V_1, -V_2\}$ with respect to the ground (midpoint). The interleaved concept helps in the minimization of the output current ripple, as shown analytically in section III.

In order to reduce the ripple and increase the controllability of the current (i.e. increased bandwidth), a high switching frequency is chosen (as shown in section III) and therefore SiC MOSFET devices are required. The total DC-link voltage is chosen to be 850V based on the available SiC MOSFET devices (breakdown voltage of 1.2kV). The input voltage levels $V_1 = 750\text{V}$ and $V_2 = 100\text{V}$ are chosen in order to allow sufficient controllability margin when the voltage V_c is around its operating limits $V_c = \{0, 550\text{V}\}$, as indicated in Fig. 2. In order to supply the high output power (maximum 15MW per stack) the input capacitors C_1 and C_2 are pre-charged by a

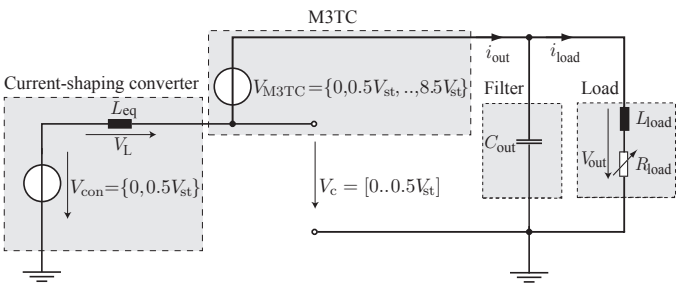

Fig. 2: Simplified equivalent circuit of a stack module of the proposed current source. The multi-phase current shaping converter can be modeled as a voltage source in series with an equivalent inductance, that is $L_{eq}=\frac{L_i}{n}$, where n is the number of interleaved phases. Likewise, the M3TC is modeled as a voltage source. Sidenote: The values within $\{...\}$ are discrete while the ones inside $[...]$ are continuous.

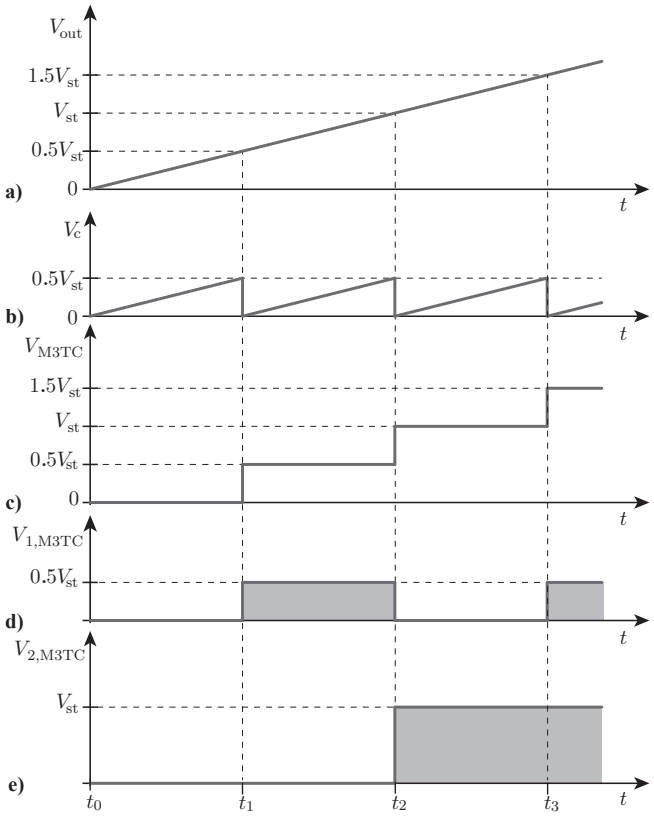

Fig. 3: Basic operating principle of the investigated current source. a) Output voltage V_{out}, b) Converter output voltage V_{c}, c) M3TC voltage V_{M3TC}, d) Voltage of the first stage of the M3TC $V_{1,\text{M3TC}}$, e) Voltage of the second stage of the M3TC $V_{2,\text{M3TC}}$.

bipolar power supply.

For the M3TC converter, up to 9 bipolar Modular Multilevel stages are connected in series, consisting in principle a solid-state Marx-type generator. The M3TC is only responsible for the generation of the staircase output voltage, so its dynamics are relatively slow. In this case, conventional silicon IGBTs are chosen as noted on Fig. 1. The stage voltage is chosen to be 1.1kV based on the commercial available silicon IGBT modules. In this way, the total output voltage of the M3TC can be designed to be between $\pm$0.55kV (if one stage is used) and $\pm$9.35kV (if 9 stages are used), in order to fit the needs of different applications. The capacitors of the M3TC stages are charged in parallel between pulses, by a low power capacitor charger, as shown in Fig. 1.

The basic operating principle of the current source is illustrated in Fig. 3. For generating for example a linearly rising output voltage V_{out}, first the converter output voltage V_{c} at t_0 is rising. At t_1, V_{c} reaches $0.5V_{\text{st}}$, which is the pre-charged value of the first stage of the M3TC. At that point, the first stage of the M3TC is turned on and V_{M3TC} becomes $0.5V_{\text{st}}$, while V_{c} collapses to zero. As V_{out} continues to increase, V_{c} increases. At t_2, V_{c} reaches again $0.5V_{\text{st}}$ and the first M3TC stage is turned off while the second stage, which is pre-charged to V_{st}, is turned on. Then, the voltage V_{M3TC} becomes equal to V_{st} and V_{c} collapses to zero. Likewise at t_3, V_{c} reaches $0.5V_{\text{st}}$, the first M3TC stage is turned on, and V_{M3TC} becomes $1.5V_{\text{st}}$.

III. Design Procedure

In this section the needed analytical considerations for the design procedure are given in order for a stack module of the current source to meet the requirements listed on Table I. The governing equations regarding the ripple calculations as well as the gradient calculations are shown, demonstrating the worst case conditions, and finally a feasible design space for a stack module with only one available bipolar M3TC stage is demonstrated.

A. Current Ripple

The current ripple of a single module of the current shaping converter shown in Fig. 1 is given by:

$$\Delta i_{\text{L,pp}} = \frac{1}{L f_{\text{s}}} \left(V_{\text{c}} + V_2\right) \left(1 - \frac{V_{\text{c}} + V_2}{V_1 + V_2}\right) \tag{1}$$

Assuming an interleaved operation of the current-shaping converter, the converter output current ripple $\Delta i_{\text{out,pp}}$ can be expressed as:

$$\Delta i_{\text{out,pp}} = D_{\text{i}}(1 - D_{\text{i}}) \frac{V_1 + V_2}{L_{\text{i}} f_{\text{s}}} \tag{2}$$

where D_{i} is given as:

$$D_{\text{i}} = \frac{V_{\text{c}} + V_2}{V_1 + V_2} - \frac{1}{n} \left\lfloor n \cdot \frac{V_{\text{c}} + V_2}{V_1 + V_2} \right\rfloor \tag{3}$$

As a worst case assumption, the amplitude of the output current's i_{out} first harmonic (at $\omega_{\text{h}} = 2\pi n f_{\text{s}}$) is assumed to be equal to the amplitude of the current ripple $\Delta i_{\text{out,pp}}$. The second order output filter $L_{\text{load}} C_{\text{out}}$ attenuates the ripple of the load current, which can be calculated by:

$$\Delta i_{\text{load,pp}} = \frac{\Delta i_{\text{out,pp}}}{\sqrt{(L_{\text{load}} C_{\text{out}} \omega_{\text{h}}^2 - 1)^2 + (R_{\text{load}} C_{\text{out}} \omega_{\text{h}})^2}} \tag{4}$$

From (4) the worst case ripple condition arises for the minimum L_{load} and the minimum R_{load}.

B. Current Gradient

Based on the equivalent circuit of Fig. 2, the current gradient that the converter can generate at its output depends on the voltage that can be applied across the equivalent inductance L_{eq}. It must also be noted that during pulsed changes, when there is no need for a controllable waveform, the M3TC capacitors can be inserted in order to either reduce or increase the output voltage V_{c} during step up or step down transients respectively. The worst-case voltage V_{c} can then be assumed in order to calculate the minimum achievable gradient.

Based on these considerations and assuming a time-optimal controller, the converter output current gradient can be calculated as:

$$\frac{di_{\text{out}}}{dt} = n \frac{V_{\text{con}} - V_{\text{c}}}{L_{\text{i}}} \tag{5}$$

The load current can be expressed in the frequency domain as:

$$i_{\text{load}}(s) = \frac{i_{\text{out}}(s)}{L_{\text{load}} C_{\text{out}} s^2 + R_{\text{load}} C_{\text{out}} s + 1} \tag{6}$$

The current-shaping converter's current i_{out} according to (5) is a ramp and acts as an input to the second order output stage.

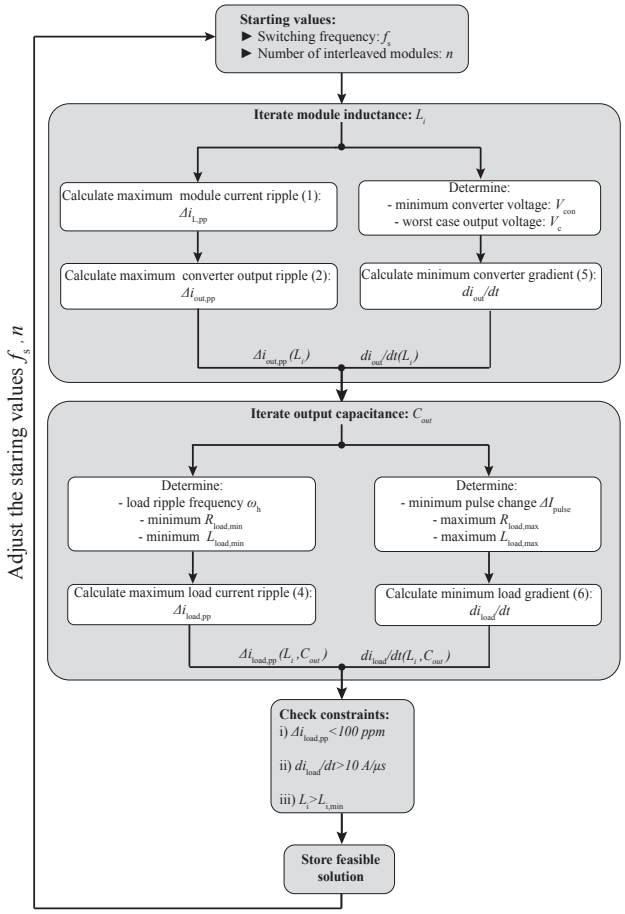

Fig. 4: Flow chart for the design of the current source for meeting the dynamic and flat-top constraints listed on Table I.

If ΔI_{pulse} is the step change in the reference current setting (pulse amplitude), the ramp input is expressed in the frequency domain as:

$$i_{\text{load}}(s) = \frac{\frac{di_{\text{out}}}{dt}}{s^2}\left(1 - e^{-s\frac{\Delta I_{\text{pulse}}}{\frac{di_{\text{out}}}{dt}}}\right) \tag{7}$$

The current gradient can be calculated analytically by solving (6) in the time-domain. It is found that the worst case scenario

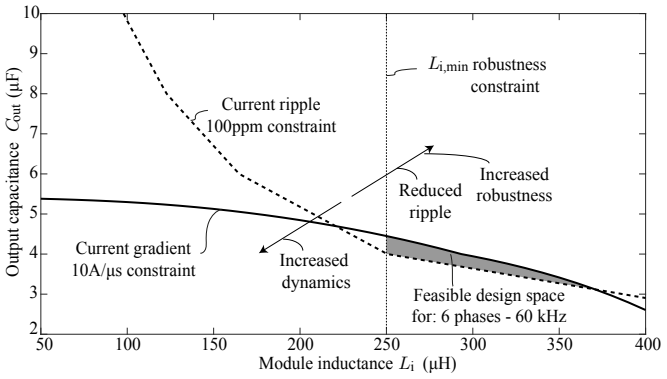

Fig. 5: Feasible design space for the system with one stack and one available bipolar M3TC stage, pre-charged to 550V. Increasing the number of M3TC stages and the number of stacks, increases the possible current gradient and decreases the load ripple.

TABLE II: Resulting parameters of a stack module system with one available bipolar M3TC stage.

Parameter	Symbol	Value
Rated output voltage	V_{out}	±1100V
Rated output current	I_{out}	1500A
Upper converter level	V_1	750V
Lower converter level	V_2	100V
Number of interleaved phases	n	6
Module inductance	L_{i}	250µH
Output capacitance	C_{out}	5µF
Switching frequency	f_{s}	60kHz
Resistive load (min. system)	R_{load}	0.01Ω .. 0.75Ω
Inductive load (min. system)	L_{load}	1µH .. 10µH

arises for the maximum L_{load} and R_{load} in the considered range and the minimum pulse amplitude setting ΔI_{step}.

C. Robustness

Considering highly fluctuating loads, such as HVDC-breakers, repetitive highly dynamic load changes must be expected and the robustness of the system is tested under extreme conditions. For example, in case of a voltage collapse, the slow switching M3TC IGBTs are not able to react fast and a high voltage is applied across the equivalent inductance L_{eq}, causing an over-current which could potentially trigger the protection mechanisms of the system. In order to increase the robustness, the individual module inductance L_{i} must be sufficiently large, setting an upper boundary on the allowable current rise.

In the present design, the maximum considered voltage fault is chosen to be $\Delta V_{\text{max}} = 1.5\text{kV}$ continuously applied across the inductor L_{eq}, for a time duration of $\Delta t = 10\mu\text{s}$, which represents the reaction time of the M3TC converter (turn-off/on delay, finite sampling times, etc.). If I_{max} is the maximum current that can be tolerated, the minimum phase inductance value can be calculated as:

$$L_{\text{i,min}} = n\frac{\Delta V_{\text{max}}\Delta t}{I_{\text{max}} - I_{\text{rated}}} \tag{8}$$

D. Design Space for Minimum Output Voltage Stack

The demonstrated design procedure (Fig. 4) was followed and as an example, the design space for a stack module system with one available bipolar M3TC stage charged to 550V) is shown in Fig. 5, for 6 interleaved modules and a switching frequency of 60kHz. As noted in Fig. 5, increasing the number of phases can lead to a significant decrease of the switching frequency to achieve the maximum current ripple requirements but also to an increased complexity. On the other hand, a higher switching frequency leads to increased controllability, which is an important factor for the robustness of the system. The chosen parameters are listed in Table II. It should be highlighted that for larger systems (higher output voltage, higher output current), the parameters of the system do not change and the system is extended either by increasing the number of M3TC stages or the number of paralleled stacks.

E. System performance limitations

The previous analysis and optimization of the system parameters relies on the assumption that the module inductors are ideal and therefore the inductance values L_{i} are equal. However, manufacturing and mechanical tolerances can result in differences between the inductance values L_{i}. In this case, the resulting output current ripple is expected to be higher than the calculated one. In [22], a sorting algorithm is proposed in order to minimize the output current ripple in interleaved systems with different individual module inductances. It should be clear however that even after the proposed ripple optimization, the converter output current ripple $\Delta i_{\mathrm{out,pp}}$ will be higher than the ideally calculated one, given by (2). In this case, the output filter capacitor C_{out} would need to be increased in order to attenuate the load current ripple $\Delta i_{\mathrm{load,pp}}$ and comply with the steady state ripple requirements of the system. To account for this case, the output capcitor is over-dimensioned in the final system.

Another limitation of the system arises from the energy storage requirements of the M3TC capacitors. Since the M3TC capacitors are not continuously charged, the maximum output voltage that the system can provide continuously throughout a pulse is not $10\mathrm{kV}$ but depends on the stage capacitance C_{st} and the load current i_{load}. A good compromise between performance and volume for the designed system can be the $100\mathrm{mF}/0.55\mathrm{kV}$ foil capacitors for the first M3TC stage and the $25\mathrm{mF}/1.1\mathrm{kV}$ for the rest of the M3TC stages. In Fig. 6, the maximum output voltage that can be supplied by the designed stack module source as a function of the output current and the pulse duration is shown, for the chosen stage capacitance values.

IV. Control System

A. Control of Current Shaping Converter

In [21], an advanced multi-phase hybrid controller which combines the time-optimality of a hysteretic controller with the robustness of an average current controller is presented and its ability to exploit the maximum capabilities of the converter system both when it comes to its transient (maximum current gradient) as well as its steady state (minimum current ripple) performance is explained.

This interleaved hybrid controller for multi-phase DC-DC converters is used in the presented current source in order to harness the full-potential of the topology and meet the specifications. Apart from the necessary high current gradient, the hybrid control concept provides the system with an excellent disturbance rejection capability which is essential during rapid load changes (e.g. in case of arcs). When a load disturbance occurs, the adaptive hybrid controller reacts by making use of the excellent properties of the hysteretic controller. Moreover, the use of the hysteretic control in transients makes the controller parameters less sensitive to the load parameters, which is advantageous in systems with unknown loads.

An overview of the control system is shown in Fig. 7. When the system is at steady state, the average current mode control (PI controller) is enabled along with the phase-shifting controller in order to achieve an interleaved operation. In case of a slow transient (e.g. slow ramp, sinusoidal waveform), the PI controller controls the current. When fast transients occur (e.g. pulse references), the adaptive hysteretic controller is enabled providing a time-optimal transient response. The interleaved operation for the duration of the transient is lost in order to provide the maximum possible current gradient and hysteretic band adaptations are employed in order to achieve approximately interleaved currents after the end of the tran-

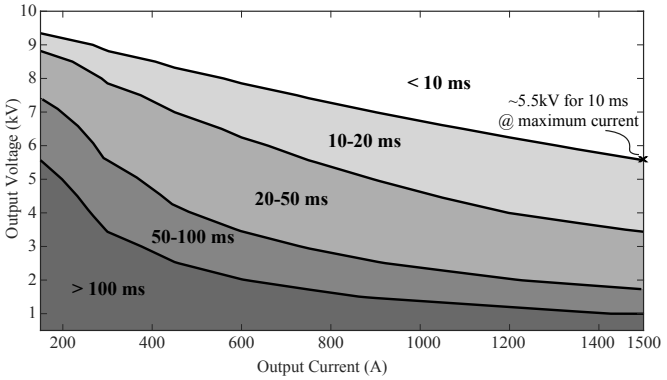

Fig. 6: Output voltage limitations of a single stack module as a function of the output current and the pulse duration. It can be noted that the system can deliver 5.5kV, for 10ms at the maximum operating pulsed current of 1.5kA. In order to increase the output voltage capabilities of the stack module, redundant stages need to be inserted, or larger capacitance values are required.

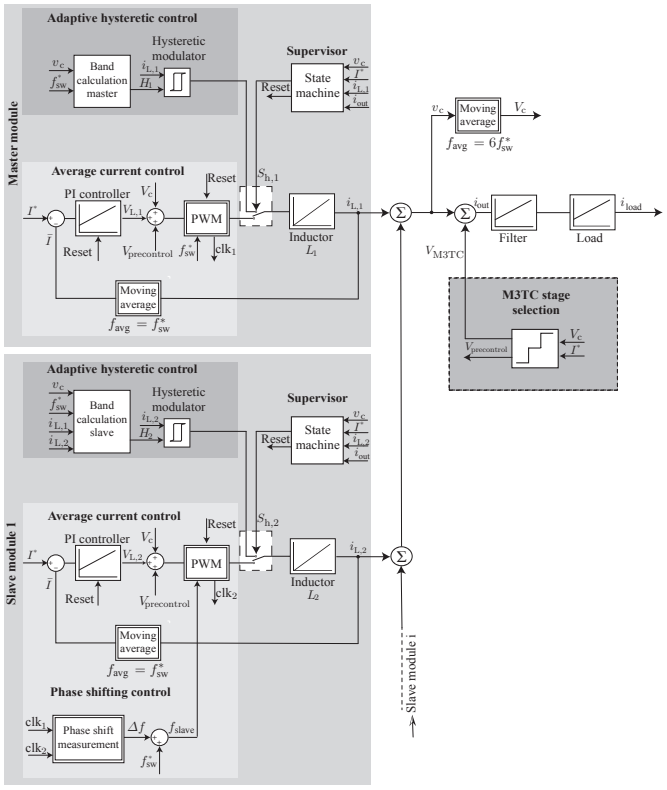

Fig. 7: Hybrid controller of a stack module. Two modules of the current-shaping converter are shown (the master and one slave module). Each slave module consists of: i) an average current mode controller which is enabled during steady state and slow transients, ii) an adaptive hysteretic mode controller which is enabled during fast transients and iii) a phase-shifting controller for optimal interleaving during steady state.

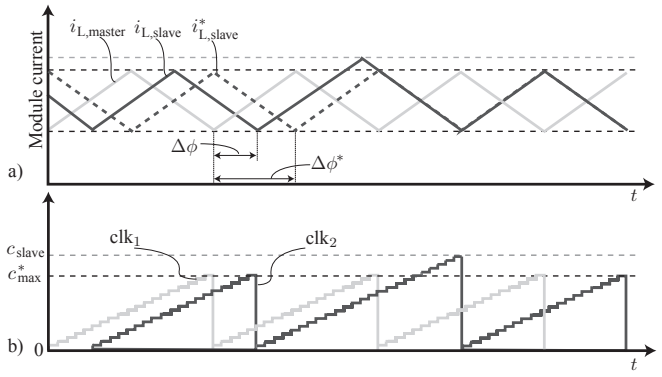

Fig. 8: Operation of the phase-shifting controller using only precise clock signals. a) Master and slave module currents b) Master and slave PWM clocks. In this scenario, the measured phase-shift $\Delta\phi$ is smaller than the reference phase-shift $\Delta\phi^*$ so the slave's PWM maximum counter c_{slave} is increased, decreasing the switching frequency, and shifting $i_{\text{L,slave}}$ to its reference position $i^*_{\text{L,slave}}$, within one period.

sient. When the system is at steady state, the controller returns to average mode control in order to maximize the accuracy of the current regulation and achieve precise interleaving [21].

The operation of the phase-shifting controller is depicted in Fig. 8. In order to achieve the needed precision the phase-shifting controller adjusts the switching frequency of the slave modules by comparing the respective PWM clocks with the clock of the master module. In this way possible imprecisions due to the current sensing circuitry of the individual modules do not affect the interleaving and the accuracy is enhanced. It should be noted that in the case of parallel connected sources, the interleaving of the master modules of each stack follows the same concept. This is particularly beneficial since only one clock signal (master's clock) has to be distributed to the control units of the paralleled stacks in order to achieve interleaving, eliminating the need for an expensive high bandwidth current sensor at the output of every stack.

B. M3TC State Machine

The state machine of the M3TC, implementing the basic principle described in Fig. 3, is shown in Fig. 9. This figure also depicts the switching actions during the level transitions in order to minimize the disturbance of the M3TC output voltage V_{M3TC} when two stages have to be switched synchronously. A commutation example from state 1 to state 2, is shown in Fig. 10 and the respective voltages of the M3TC stages are shown in Fig. 11, along with the status of the IGBT switches of the M3TC stages 1 and 2.

At state 1.1, switch $S_{2,2}$ is turned off, and the antiparallel diode of $S_{2,2}$ is conducting, resulting in no change in V_{M3TC}. After waiting for the interlocking time $T_{\text{int,s}}$ of the 1.7kV switch $S_{2,2}$, the state machine commutes to state 1.2, by turning on switch $S_{2,1}$. Due to the turn on delay time of switch $S_{2,1}$, the V_{M3TC} is not changing, and the state machine waits for $\Delta T_{\text{IGBT}} = T_{\text{d,s}} - T_{\text{d,f}}$, which is the delay time difference between the 1.7kV and the 1.2kV IGBT. In state 1.3 the state machine turns off switch $S_{1,1}$. During this state, a small disturbance is observed in the voltage of the M3TC due to the difference between the fall time of switch $S_{1,1}$ and the rise time of $S_{2,1}$ as can be seen in Fig. 11. At the end of state 1.3, switch $S_{2,1}$ is conducting and the voltage V_{M3TC} becomes equal to V_{st}. During state 1.3 the algorithm triggers the PI controller calculations and feed-forwards the voltage ($V_{\text{precontrol}}$) to the PI controllers, as shown in Fig. 9. In this way, the transient behavior of the PI is improved and the disturbance caused by the level change is minimized. After waiting for the interlocking time $T_{\text{int,f}}$ of the 1.2kV IGBT, the state machine commutes to state 2 by turning on switch $S_{1,2}$. In this way, the two simultaneous switching actions (turning on stage 2 and turning off stage 1) are almost synchronous resulting in only a minor remaining voltage disturbance of the V_{M3TC}, that is caused by the rise/fall times of the switches.

Furthermore, when a pulsed current is given as a reference, multiple M3TC stages can be directly turned on and the voltage of the M3TC is set to V_{preset}. This could be either the maximum available voltage (i.e. all stages turned on) or any other value depending on the dynamic performance requirements of the application. When the converter current i_{con} is settled, the voltage of the M3TC returns to the initial stage and the M3TC enters again the normal operation mode. A similar algorithm is followed in the case of negative output voltages or step-down pulsed references as shown in Fig. 9.

TABLE III: Controller parameters, non-idealities and parasitic components.

Parameter	**Value**
FPGA clock frequency	100MHz
PI controller clock frequency	60kHz
PI controller calculation delay	1µs
Hysteresis controller clock frequency	2MHz
M3TC state machine clock frequency	150kHz
Current sampling frequency	2MHz
Current sensor bandwidth	500kHz
V_{c} sampling frequency	2MHz
V_{c} voltage probe bandwidth	500kHz
V_{M3TC} sampling frequency	200kHz
ADC interface resolution	12bits
SiC MOSFET delay time	200ns
SiC MOSFET rise/fall time	70ns
SiC MOSFET interlocking time	500ns
1.2kV IGBT delay time $T_{\text{d,f}}$	800ns
1.7kV IGBT delay time $T_{\text{d,s}}$	1000ns
1.2kV IGBT rise/fall time $T_{\text{r,f}}$	150ns
1.7kV IGBT rise/fall time $T_{\text{r,s}}$	200ns
1.2kV IGBT interlocking time $T_{\text{int,f}}$	1800ns
1.7kV IGBT interlocking time $T_{\text{int,s}}$	2000ns
SiC MOSFET $R_{\text{ds,on}}$	8mΩ
IGBT $R_{\text{ce,on}}$	1mΩ
IGBT $V_{\text{ce,on}}$	2V
Module inductance parasitic ESR	2mΩ
Output capacitor parasitic ESR	10mΩ

V. Simulation Results

In this section, simulations results that verify the performance of the designed stack module are presented. Table III lists the main control parameters, non-idealities and parasitic components included in the simulations. It is worth noting

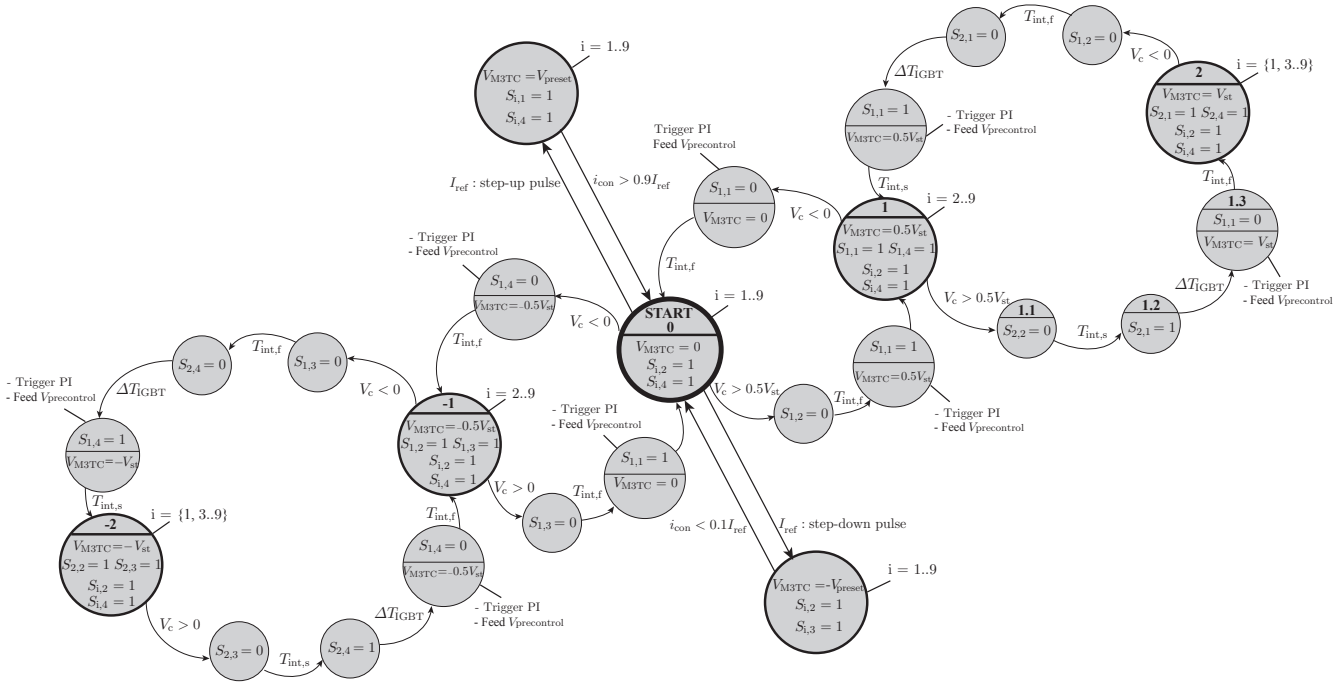

Fig. 9: State machine of the M3TC. The algorithm measures the voltage V_c and uses the reference current I_{ref}. When the voltage V_c exceeds the limits, the state machine changes the state, as described in section II. The modulation of the state machine is performed in order to minimize the jittering due to the interlocking time of the switches. during the state change, the state machine triggers the PI controller calculations, informing the controller for the eminent change in voltage, as shown in Fig. 7. In fast transients (i.e. pulses) the algorithm turns multiple stages on simultaneously ($V_{M3TC} = V_{preset}$), in order to achieve a higher gradient and returns to the first state once the converter current is settled.

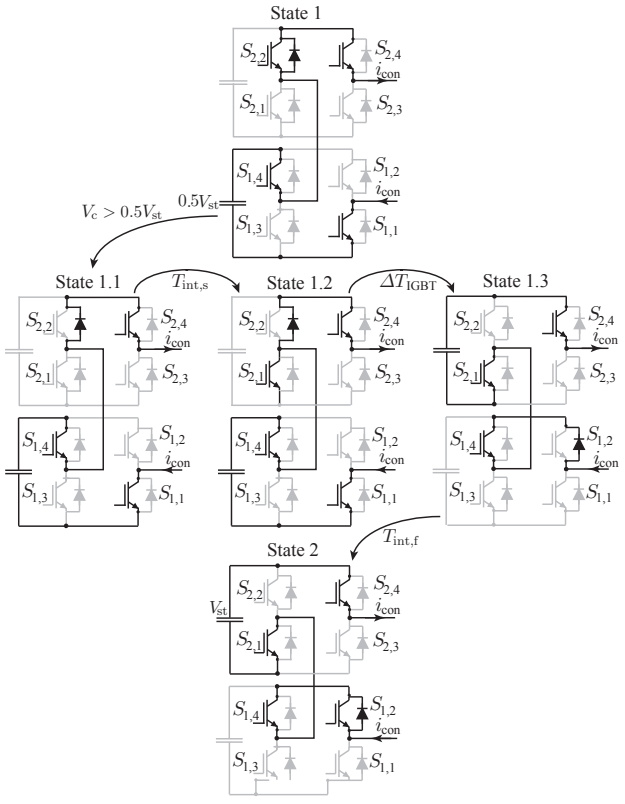

Fig. 10: State machine during commutation from state 1 to state 2, shown in Fig. 9. The intermediate states 1.1, 1.2 and 1.3 aim to minimize the disturbance of the M3TC voltage during the simultaneous switching of the two M3TC stages, by synchronizing their switching actions.

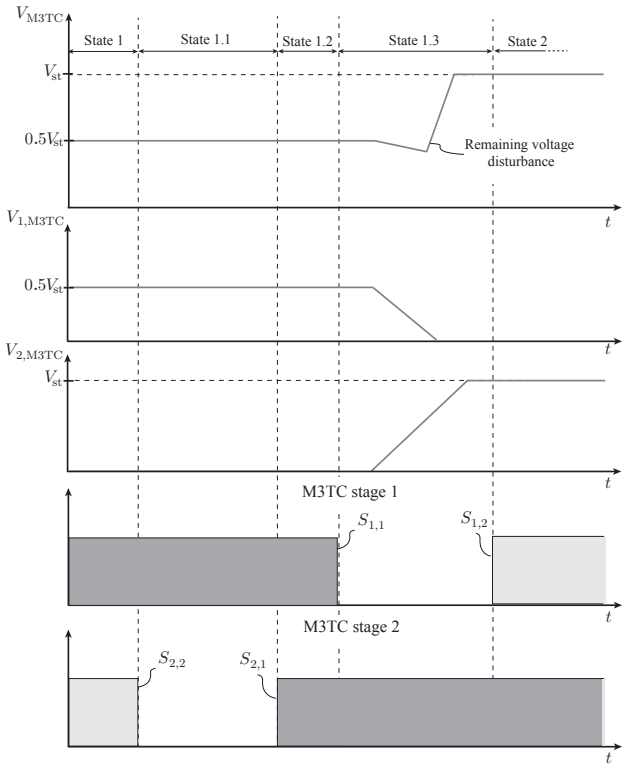

Fig. 11: M3TC voltages during commutation from state 1 to state 2, shown in Fig. 9. The commutation strategy shown in Fig. 10 ensures that the non-ideal switching causes only a small voltage disturbance during state 1.3. This disturbances is caused by the difference between the fall time of switch $S_{1,1}$ and the rise time of switch $S_{2,1}$.

that the power semiconductor interlocking times and rise/fall times have been also included since they play a significant role in the control of the M3TC and the performance of the current source. The times and parasitics used in the simulation are taken from the respective manufacturer datasheets. Additionally, the voltage divider and the current sensor have been simulated as first order low pass filters, with the bandwidth listed in Table III. The analog to digital interface has been modeled as a conventional quantizer with a resolution of 12 bits and a sampling frequency of 2MHz. Moreover, the SiC MOSFETs, are modeled with an equivalent resistance $R_{\text{ds,on}}$ and the IGBTs with a voltage source $V_{\text{ce,on}}$ in series to a resistor $R_{\text{ce,on}}$. The simulation model is running with a frequency of 100MHz, which is representing the maximum resolution of the FPGA clock of the control unit.

A. Resistive-Inductive Loads

Fig. 12 shows an arbitrary current waveform for a 2Ω-10μH load. Initially, a ramp reference current with a gradient of $1\text{A}/\mu\text{s}$ is imposed and the PI controller is enabled for the duration of this transient since there is no need for high dynamic performance. The module currents during these transients are interleaved, as shown in Fig. 12b, and the load current ripple remains low due to the phase-shifting controller described in Fig. 8. As can be seen in the detailed transient on Fig. 12a), despite the level change of the M3TC that causes the voltage V_{c} to collapse, the converter currents are only slightly disturbed due to the feed-forward of the voltage $V_{\text{precontrol}}$, shown in Fig. 7.

Fig. 12c) shows the output voltage of the M3TC V_{M3TC} and the corresponding converter output voltage V_{c}. The control of the M3TC follows the state machine described in Fig. 9, as its output voltage is changing with a step of $0.5V_{\text{st}}$. It is worth noting that the droop is compensated by a respective increase of the voltage V_{c}, when the capacitors of the M3TC are discharging, as highlighted in Fig. 12c).

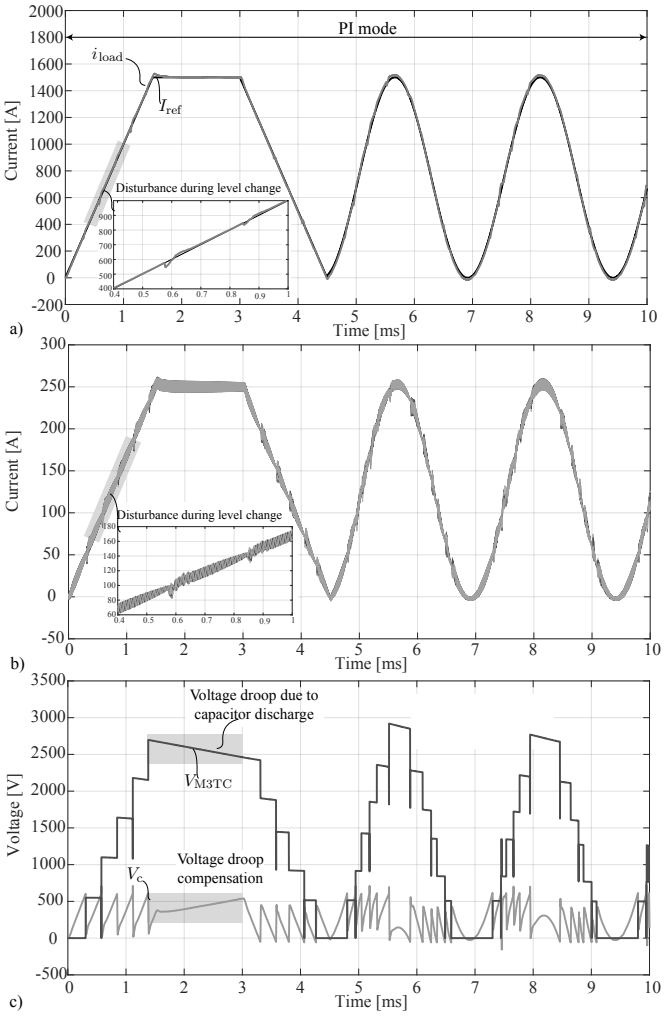

Fig. 12: Arbitrary current waveform generation driving a 2Ω-10μH load. a) Reference current (black) and load current waveform (grey). The PI controller is used in transients (slow ramp ($1\text{A}/\mu\text{s}$ and 200Hz sinusoidal wave), b) Individual module currents (interleaved). The disturbance caused by the level change is attenuated due to the pre-control voltage command described in Fig. 7, c)M3TC voltage V_{M3TC} and converter output voltage V_{c}.

B. Inductive Loads

In Fig. 13 the ability of the current source to drive highly inductive loads with a high current gradient (i.e. septum magnets) is demonstrated. As soon as the pulse reference is given, the M3TC state machine jumps to V_{preset}, which is in this case 9.35kV, the maximum output voltage of the M3TC, as highlighted in Fig. 9. At the same time, the current-shaping converter switches to hysteretic mode in order to generate the maximum possible di/dt. As shown in Fig. 13a) once the current is approximately settled, the M3TC stages are turned

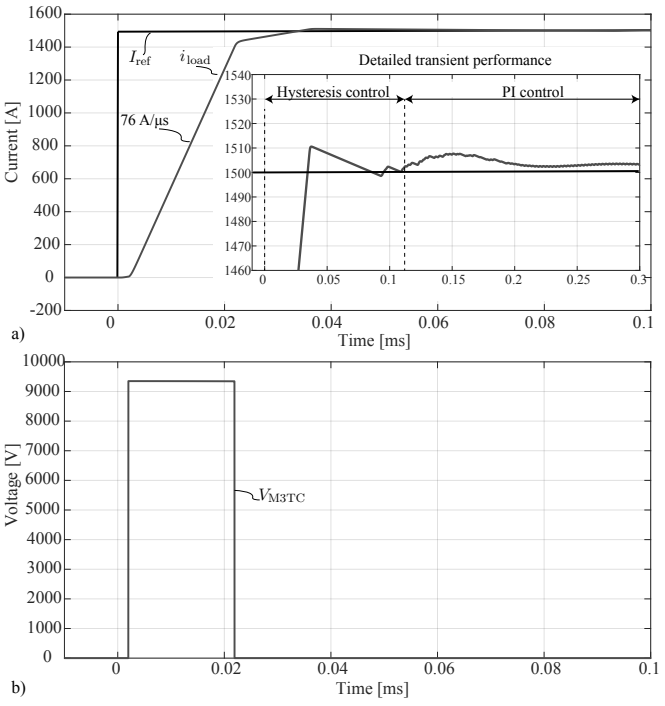

Fig. 13: Transient response of the current source driving an inductive load 20mΩ-100μH. a) Reference current (black) and load current waveform (grey). The hysteresis controller is used in transients and along with the M3TC voltage generates a current gradient of $76\text{A}/\mu\text{s}$ on the load, b) M3TC voltage V_{M3TC}. When the reference change takes place, the M3TC state machine jumps to V_{preset} (here 9.35kV).

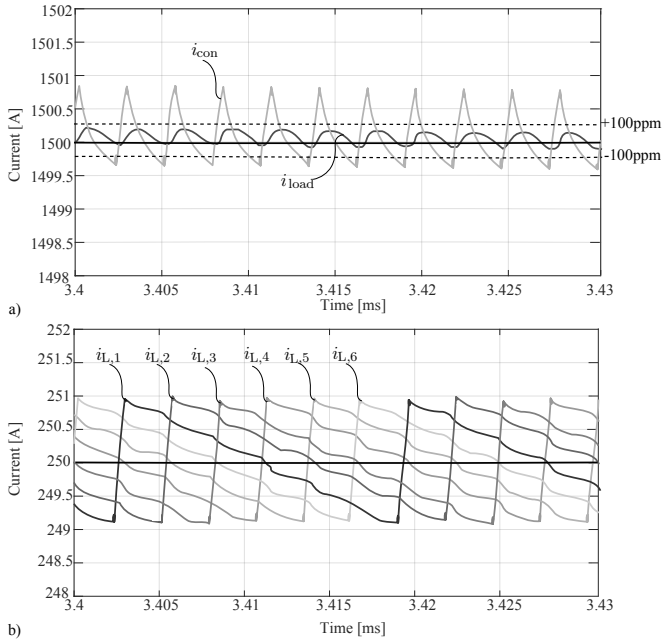

Fig. 14: Steady state performance of the current source driving an inductive load 20mΩ-100μH. a) Reference current (black), load current (dark grey) and converter current (light grey). b) Individual module currents (interleaved) as seen by the control unit. The distortion is a result of the common coupling between the different phases and the effect of the finite current sensor bandwidth and finite ADC precision.

off and the current gradient is slowed down in order to avoid a high overshoot in the current. The transient performance graph of Fig. 13a) shows the overshoot of the current, which is less than 1%. During the transient, the individual module currents of the current-shaping converter are not interleaved and therefore the ripple is higher. In fact the ripple in the hysteretic cycles is caused due to the non-optimal interleaving. More details about the performance of the advanced hybrid control can be found in [21]. Nevertheless, as soon as the reference has settled, the controller returns to PI control mode and the phase-shifting controller returns the module currents to their optimal positions as shown in Fig. 8.

Additionally, Fig. 14, illustrates the steady state performance of the current source, when driving a highly inductive load. On Fig. 14b) it can be seen that in steady state, the module currents are fully interleaved, resulting in a converter current i_{con}, with minimum ripple and high effective switching frequency (six times higher than the module switching frequency). The additional filter stage at the output of the current source, shown in Fig. 1, further attenuates the converter current ripple. The peak to peak ripple of load current i_{load} is in this case smaller than 100ppm. It should be highlighted, that further oscillations are caused due to the action of the PI controller and the non-idealities of the control system (e.g. quantization errors, filter delays). However, as illustrated in Fig. 14, the load current remains well within the ±100ppm bands.

C. Fluctuating Dynamic Loads

Fig. 15 shows the ability of the current source to drive highly fluctuating loads such as the plasma in an operating

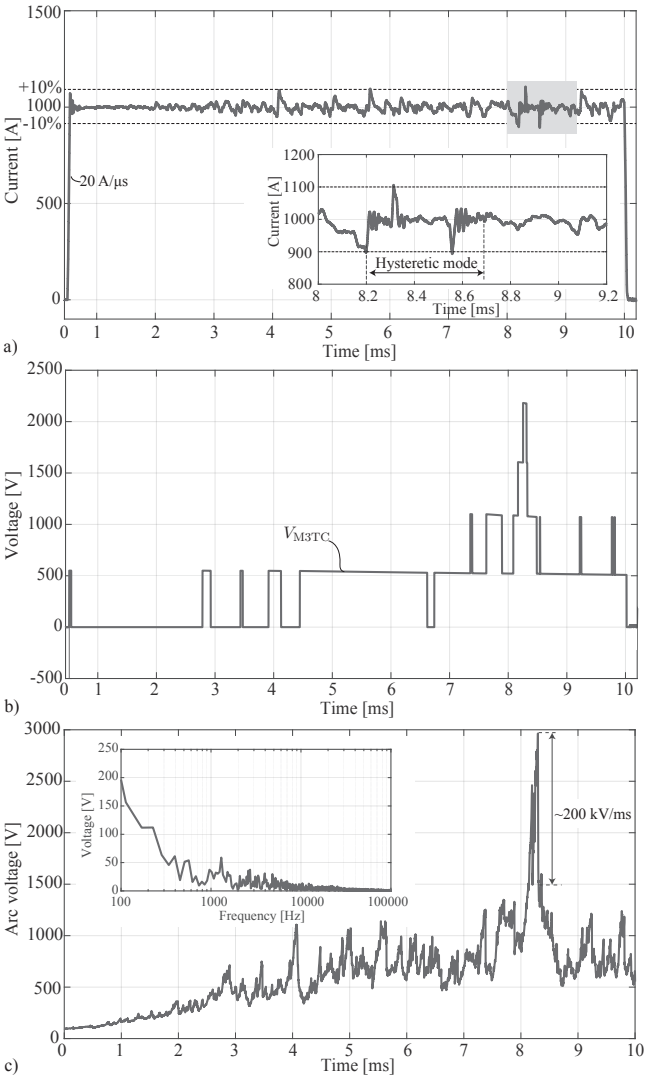

Fig. 15: Simulation results for a DC arc implemented as a fluctuating resistance value: a) Total output current waveform. The output current remains within ±10% of its target value. b) M3TC voltage V_{M3TC}. c) Simulated DC-arc voltage (measurement conducted at the High Voltage Laboratory at ETH Zurich [17]).

HVDC circuit breaker. The load voltage as a function of time is depicted in Fig. 15c) and is deduced from measurements of a DC-arc performed at the High Voltage Laboratory at ETH Zurich [17]. In this case, a reference pulsed current of 1kA is given and the control system generates a current gradient of approximately 20A/μs by using the hysteretic mode. During flat-top, the chaotic behavior of the load causes the voltage of the load to oscillate resulting in oscillations of the output current and a high output current ripple. However, as highlighted in Fig. 15a), the current remains within ±10% of its reference value. It is also evident that, as soon as the output current exceeds the threshold value, the hysteretic mode is enabled and the limits of the hysteretic band act as an over-current protection.

In [11], the need for arbitrary current waveforms including staircase waveforms in order to study the step response properties of the DC-arc, has been noted. Likewise, Fig. 16 shows the performance of the current source while generating

a staircase current waveform in a highly fluctuating load. The load in this case is simulated as a variable voltage source based on arc measurements performed at the High Voltage Laboratory at ETH Zurich. The simulated voltage waveform as a function of time can be seen in Fig. 16c). The high frequency, high amplitude fluctuations result again in a high current ripple. However, the combination of the robust design, with high module inductances and near optimal control results in a current that remains within the specified $\pm 10\%$ limits during flat-top operation and does not result in over-currents that could potentially harm the converter system and trigger the protection systems. At the same time, the needed dynamic performance is met as shown in the zoomed version of the transient in Fig. 16a).

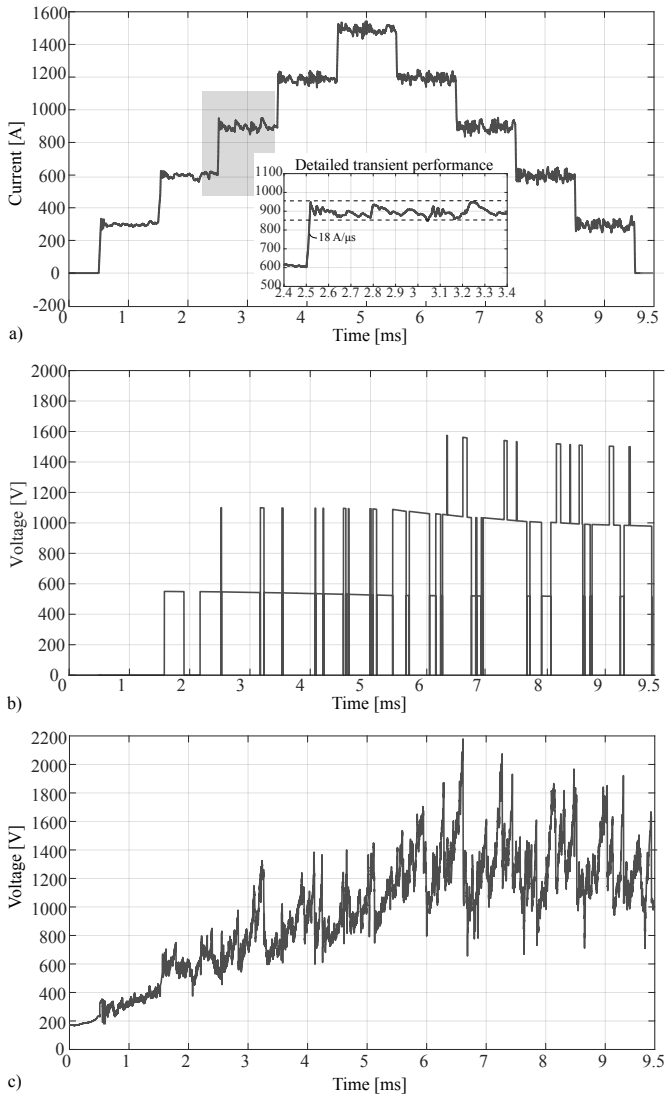

Fig. 16: Simulation results for a DC arc implemented as a fluctuating variable voltage source. The need for staircase current waveforms is explained in [11]: a) Staircase output current waveform. Fast current pulses are generated while the fluctuations of the output voltage cause a relatively high current ripple. b) M3TC voltage V_{M3TC}. c) Simulated DC-arc voltage (measurement conducted at the High Voltage Laboratory at ETH Zurich [17]).

VI. Conclusion

In this paper, a flexible, highly dynamic and ultra-low ripple arbitrary current source is presented. The output current of the source can be increased by increasing the number of stacks up to 30kA and its output voltage can be increased by increasing the number of M3TC stages up to 10kV. The high modularity of the topology makes it an attractive candidate in a wide range of applications including driving HVDC circuit breakers or inductive loads in accelerators and fusion reactors. Moreover, the combination of an analytical design procedure and a near-optimal control have enabled the use of the full potential of the topology.

Detailed simulation results have shown that the current source is able to fulfill the high current gradient requirements during transient operation, the low-ripple and high precision requirements during steady state and the stability requirements during abrupt load changes. The simulations have shown the ability of the current source under different operating scenarios, with several loads using realistic control parameters, including component non-idealities and parasitic components. The results have verified that the current source is able to drive highly fluctuating loads (e.g. DC-arcs) while providing the necessary high dynamic.

Finally, the hardware prototype of the designed system is currently under development at the Laboratory for High Power Electronics, ETH Zurich and experimental results are expected to be published in upcoming publications.

Acknowledgment

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