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Analytical Switching Loss Modelling based on Datasheet Parameters for MOSFETs in a Half-Bridge

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Analytical MOSFET Switching Loss Modeling for a Half-Bridge Configuration based on Datasheet Parameters

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Abstract

Modern wide-bandgap devices, such as SiC or GaN based devices, feature significantly reduced switching losses and the question arises if soft-switching operating modes are still beneficial. For most semiconductor devices only limited information is available to estimate the switching losses. Especially if a wide operating range is desired, excessive measurements have to be performed to determine the switching losses for arbitrary operating points. Therefore, in this paper a fast calculation method to determine the switching losses based on the charge equivalent approximation of the MOSFET capacitances, relying only on datasheet parameters, is presented. In addition, the turn-off losses at high switching currents are investigated and an analytical expression to estimate the maximum current range for which the MOSFET can be turned-off with negligible switching losses is proposed.

Index Terms

Power MOSFET, switching losses, half-bridge

I. INTRODUCTION

Despite the continuously improving semiconductor performance, the switching and conduction losses of the semiconductors are typically still the largest loss contributors.

Especially in case a high switching frequency is required, the switching losses have not only a significant impact on the overall losses but also on the required volume due to their impact

on the cooling system. Thus, an accurate calculation and modelling of the switching losses is one key to optimally design converter systems.

With the advance of new wide bandgap devices, which have relatively low switching losses, also the question arises if soft-switching operating modes (e.g. triangular current mode [1]) are still beneficial at high switching frequencies. This is especially relevant for unipolar devices as for example MOSFETs, which this paper focuses on.

For such designs the conduction losses can be accurately determined based on the temperature dependent on-state resistance provided in datasheets and the device current. However, the switching losses often can be only determined accurately by measurements [2]–[4].

To avoid cumbersome measurement series, analytical approaches based on linearized MOSFET models are applied as for example described in [5]. To have a better understanding of the MOSFET switching transients and the effect of the parasitics several experimental studies were conducted in the past [6]. In [7]–[13] the analytical models are extended by the parasitic elements of the commutation path to determine the characteristic current and voltage waveforms of the MOSFET device during the switching transitions. These models were further improved by taking the diversion process of the MOSFET internal current during the switching process into account (as e.g. proposed in [14]). There a current through the MOSFET channel (i_{ch}) and one to recharge the parasitic capacitances (I_{oss}) are distinguished, where i_{ch} is considered to be the origin of the switching losses.

However, the presented models often have a high complexity and rely on device parameters, which have to be measured and are not or only limited available in datasheets [15]–[17]. Thus, in this paper a model is proposed, which is based only on datasheet parameters and enables a fast and precise estimation of the switching losses in a half-bridge configuration for example within a system optimization procedure.

The model uses the charge equivalent representation of the parasitic MOSFET capacitances. This on the one hand allows the accurate determination of the voltage fall and rise times, on the other hand, it is shown that in the considered half-bridge configuration the charge is directly connected to the energy stored in these capacitances, and thus also enables a precise estimation of the device internal loss energies.

Furthermore, the proposed model includes the parasitic source inductance and estimates the diode reverse recovery based on a simplified power diode model presented in [18]. In addition, a closed analytical expression to determine the maximum current for which the semiconductor

can be turned-off with negligible losses (soft-switching) is derived.

Summarizing, the key adaptations compared to the past work within the proposed method are:

- The parasitic capacitances are approximated by their charge equivalent capacitances to simplify the device internal recharging process.
- The current dependency of the transconductance is taken into account and used in an iterative process to determine the Miller plateau.
- The reverse recovery behaviour is modeled with a simplified power diode model [18].
- A expression to determine the ideal soft-switching operating area with minimal switching losses is derived.
- The model offers a low complexity and is based on only datasheet parameters.

In the following, first the switching transients during turn-off and turn-on are step-wise analysed in section II. This includes the derivation of the underlaying equations for the calculation routine. A summary of the equations used in the optimization routine (flowchart in Fig. 6) as well as the parameter extraction is described and demonstrated for an example MOSFET device in section III. The validation of the model by electrical measurements is presented in section IV. Moreover, the effect of the parasitic source inductance and the temperature are briefly discussed.

II. MODELING OF THE SWITCHING LOSSES

The switching losses in a half-bridge configuration strongly depend on the applied modulation scheme. Basically, two possible switching scenarios can be distinguished.

First, the conducting device is turned off and the current is commutating to the body diode of the opposite device in the half-bridge which, after its body diode is conducting, can be turned on under zero voltage conditions (ZVS).

Second, the semiconductor device is turned off and the current is commutating to its antiparallel body diode (what is assumed to be lossless). After a defined interlocking time, guaranteeing that the body diode is conducting the full current and the device is turned off, the opposite semiconductor device in the half-bridge is turned on resulting in a hard commutation of the body diode (hard turn-on).

For both scenarios, the linearized MOSFET model depicted in Fig. 1 is considered. This model includes the parasitic capacitances of the device (C_{ds}, C_{gd}, C_{gs}) the gate resistor (R_g, including internal and external gate resistors) and the parasitic inductances in the commutation loops(L_s, L_d).
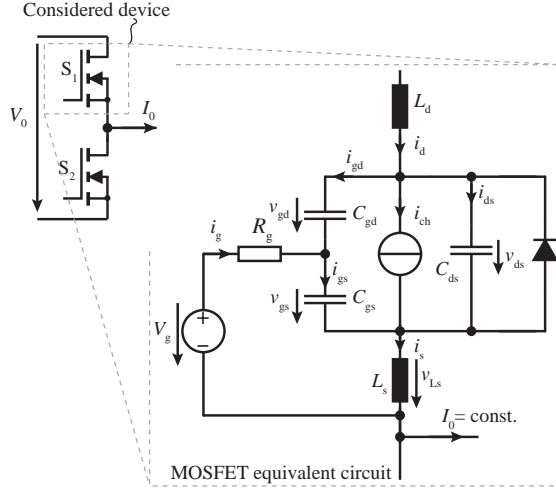
Fig. 1. Half-bridge switching cell and circuit equivalent of a MOSFET during the switching process.

During the switching transition, the MOSFET device is operated in saturation. In saturation the MOSFET channel is modelled as controlled current source i_{ch} , which is linked by the transconductance g_m to the gate source voltage v_{gs} by

$$i_{ch} = g_m(i_{ch})(v_{gs} - V_{th}). \tag{1}$$

The transconductance is a function of the current through the MOSFET channel i_{ch} [19], which can be expressed as

$$g_m(i_{ch}) = \sqrt[x]{\frac{k_1 i_{ch}^x}{i_{ch} - k_2}}, \tag{2}$$

The constants x, k_1 and k_2, the threshold voltage V_{th}, and the reverse recovery behaviour of the body diode, are extracted from the corresponding datasheet as is discussed in section III-A.

With the assumption that the parasitic MOSFET capacitances are only lossless energy buffers, the losses in the device for both scenarios are mainly determined by the current through the MOSFET channel i_{ch} and the drain source voltage v_{ds} during the switching process (duration t_{sw} e.g. given in Fig. 2) [14].

$$E_{sw} = \int_{t_{sw}} i_{ch} v_{ds} dt \tag{3}$$

For the sake of simplicity, the recharging process of the parasitic device-internal capacitances is assumed to be lossless. The current for charging the parasitic capacitances is denoted as $I_{oss} = i_{gd} + i_{ds}$ in the following.

Furthermore, it is assumed that during the complete switching transition the output current I_0 is approximately constant and the gate voltage V_g is ideally set with negligible rise and fall times.

A. Turn-Off

Turning a MOSFET off under ZVS conditions is often assumed to result in negligible losses. However, with increasing current amplitudes this losses become significant and must be included in the loss calculation. In the following a step-wise analysis of the turn-off process is presented to explain the cause of these losses.

In Fig. 2 the characteristic linearized waveforms for turning off MOSFET S_1 are depicted. There, three intervals are distinguished. The losses can be estimated based on i_{ch}, v_{ds} and the time intervals t_{rv} and t_{fi}.

a) ***Interval 0a:*** At $t = T_{off}$ the gate voltage of S_1 is reduced to $V_g \leq 0$. Accordingly, a negative voltage is applied across the gate resistor R_g and the gate source voltage (v_{gs}) decreases to the Miller voltage V_{mil} (saturation region). This process is assumed to be lossless, since v_{ds} and the drain current i_d are approximately constant.

b) ***Interval 1a:*** During interval 1a the drain source voltage v_{ds} is rising to V_0, the parasitic capacitance of S_1 ($C_{oss} = C_{gd} + C_{ds}$) is charged, and simultaneously the capacitance of S_2 is discharged. Since the voltages of these capacitances are clamped to the applied DC-voltage, their dv/dt have the same absolute value. Therefore, the nonlinear capacitances can be considered as parallel connected ($C_{par} = C_{oss,1} + C_{oss,2}$) during the voltage transition as shown in Fig. 3. C_{par} is symmetrical with respect to v_{ds}. The charge, respectively the energy required to recharge the parasitic capacitances C_{par} is

$$E_{par}(V_0) = \int_0^{V_0} v \cdot C_{par}(v) dv = Q_{oss} V_0, \tag{4}$$

whereas Q_{oss} is the voltage dependent charge stored in C_{oss} at the voltage $v_{ds} = V_0$. This circumstance allows to model the parasitic capacitances of the MOSFET by a single charge equivalent capacitance value.

Equation (4) linking the stored charge and the energy content is only valid since C_{par} for two identical devices in the half-bridge is symmetrical with respect to v_{ds}. The effective stored energy in S_1 is $E_{oss,1} < 1/2 Q_{oss} V_0 = 1/2 E_{par}$, and has to be determined with respect to the
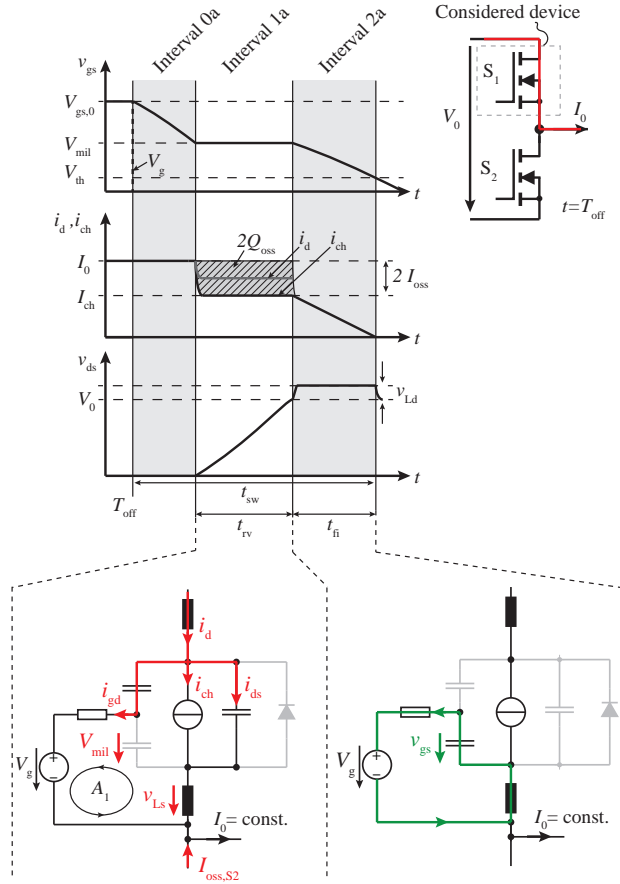
Fig. 2. Linearized MOSFET characteristics of the gate source voltage v_{gs}, the drain-source voltage v_{ds}, and the channel current i_{ch} of the MOSFET S_1 during turning the device off.

nonlinear characteristic of $C_{oss,1}$ [1]. As indicated in Fig. 2 and Fig. 3, i_{ch} is reduced by two times the current required to recharge the parasitic capacitances $I_{oss} = i_{ds} + i_{gd} = const$ during interval 1.

To determine I_{oss}, first the basic equations describing the circuit during that interval have to be considered:

- I_{oss} is linked to the gate drain current, i_{gd}, by the Kirchhoff's law for loop A_1 in Fig. 2

$$-i_{gd} = i_g = -I_{oss} \left(\frac{C_{gd}}{C_{gd} + C_{ds}} \right) \tag{5}$$

$$= \frac{1}{R_g} \left(V_g - V_{mil} - v_{Ls} \right),$$

[1] Effective energy stored in S_1: $E_{oss,1} = \int_0^{V_0} v \cdot C_{oss,1}(v) dv$
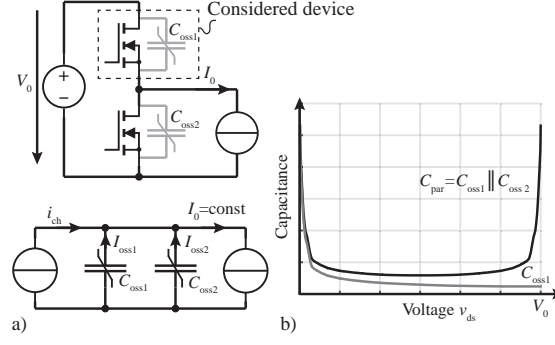
Fig. 3. a) Considered half-bridge topology and the equivalent circuit during the voltage transition. i_{ch} is reduced by $2I_{oss}$ compared to $I_0 = const$. c) Parallel connected nonlinear parasitic capacitances of the two (identical) MOSFET devices.

assuming that $\frac{1}{C_{gd}}i_{gd} = \frac{1}{C_{ds}}i_{ds}$.

- The gate source voltage $v_{gs} = V_{mil}$ is linked to i_{ch} by equation (1)

$$i_{ch} = I_0 - 2I_{oss} = g_m(V_{mil} - V_{th}). \tag{6}$$

- In (6) $v_{gs} = V_{mil}$ and I_{oss} are assumed to be constant. However, the current in the channel and across the parasitic source inductance L_s shows a nonlinear behaviour, due to the capacitive current divider given by S_1 and S_2, such that the voltage drop across L_s additionally has to be taken into account. With increasing voltage across S_1 its parasitic capacitance becomes small and contrariwise the one off S_2 becomes large. Therefore, it is assumed that during interval 1 the current through S_1 decreases from I_0 to I_{ch}. This introduces a negative voltage drop $v_{Ls} < 0$ across the parasitic stray inductance L_s, which counteracts the applied gate voltage V_g. As a consequence, the voltage rise time t_{rv} is increased. The average voltage drop across the parasitic inductance v_{Ls} could be derived by

$$v_{Ls} = \frac{1}{t_{rv}} \int_0^{t_{rv}} L_s \frac{di_s}{dt} dt \tag{7}$$

$$v_{Ls} = \frac{1}{t_{rv}} L_s(i_s(t_{rv}) - i_s(0)) = \frac{1}{t_{rv}} L_s 2 I_{oss} \tag{8}$$

$$|v_{Ls}| = 2L_s \frac{I_{oss}^2}{Q_{oss}} \quad \text{with } t_{rv} = \frac{Q_{oss}}{I_{oss}}. \tag{9}$$

Based on (5), (6) and (9), a quadratic equation for I_{oss}

$$0 = \frac{2L_s}{Q_{oss}R_g} I_{oss}^2 + \left(\frac{2}{g_m R_g} + \frac{C_{gd}}{C_{gd} + C_{ds}}\right) I_{oss} + \frac{1}{R_g}\left(V_g - V_{th} - \frac{I_0}{g_m}\right) \tag{10}$$

results. This equation allows to calculate I_{oss} for an arbitrary operating point.

Determine I_{oss} is an iterative process since the transconductance g_m is depending on i_{ch}. As a consequence I_{oss}, $g_m(I_0 - 2I_{oss})$ and V_{mil} (eq. (6)) have to be determined iteratively. In each iteration these values have to be recalculated until the deviation in I_{oss} is negligible as depicted in the flowchart in Fig. 6.

Once I_{oss} and V_{mil} are calculated, the drain current i_d and the current in the MOSFET channel i_{ch} during this interval can be calculated by

$$i_d = I_0 - I_{oss} \tag{11}$$

$$i_{ch} = I_0 - 2I_{oss}. \tag{12}$$

The voltage rise time is defined by the time required to charge $C_{oss} = C_{gd} + C_{ds}$ and thus can be estimated by

$$t_{rv} = Q_{oss}/I_{oss}. \tag{13}$$

*c) **Ideal Zero Voltage Switching**:* With equation (12) follows that an ideal zero voltage switching with a nearly lossless turn-off (ZVS) can be achieved if $I_0 < 2I_{oss}$, since i_{ch} becomes zero. In that case, the current to charge the parasitic capacitances becomes $I_{oss} = 1/2I_0$ and is not anymore depending on the gate configuration.

At the boundary of the ideal zero voltage switching, $2I_{oss} = I_0$, V_{mil} equals V_{th} and i_{ch} becomes zero. In this case, expression (10) can be simplified and the resulting maximum current for which a lossless turn-off is expected is

$$I_{0,zvs} = \frac{V_0}{2L_s}\left(- R_g C_{gd} + ... \right.$$
$$\left. \sqrt{(R_g C_{gd})^2 - 8(V_g - V_{th})\frac{L_s(C_{gd} + C_{ds})}{V_0}} \right) \tag{14}$$

With increasing gate resistance R_g or source inductance L_s, i_{gd} and accordingly I_{oss} decreases. As a consequence $I_{0,zvs}$ is also at a lower current.

Equation (14) can be used to find the required snubber capacitance (increasing C_{ds}) to mitigate the switching losses during the turn-off at high currents[2] or to check if the assumption of negligible turn-off losses is still valid.

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[2]If a snubber capacitance is employed, a (partial) hard turn-on has to be avoided, since the energy stored in the capacitances can be high and is lost during the switching process (below described in *Scenario 2: Turn-on*).

If I_0 is small, relatively long switching intervals result, since the charging current for C_{oss} becomes small. Turning S_2 on before the recharging process ends results in a partial hard turn-on as described in [20].

When current I_0 exceeds $2I_{oss}$, i_{ch} is increasing, what results in significant switching losses. Furthermore, the remaining current in the channel has to be decreased to zero in interval 2a.

d) Interval 2a: When the voltage across S_1 reaches V_0, the body diode of S_2 starts conducting. The time t_{fi} (Interval 2a in Fig. 2), in which the remaining current I_{ch} commutates to the body diode of S_2, is proportional to the gate source voltage, which decreases from V_{mil} to V_{th}. To find t_{fi}, the loop consisting of C_{gs}, L_s, and R_g is considered, whereas $v_{Ls}(t) = L_s \partial i_s(t)/\partial t \approx L_s \partial (g_m(v_{gs}(t) - V_{th}))/\partial t$. By solving the partial differential equations t_{fi} can be expressed as

$$t_{fi} = -\ln\left(\frac{V_{th} + V_g}{V_{mil} + V_g}\right)(C_{gs}R_g + L_s g_m). \tag{15}$$

Since the current is decreasing, a voltage drop across the parasitic inductance L_d is observed, which results in an increased v_{ds} by

$$V_{Ld} = L_d(I_0 - 2I_{oss})/t_{fi}. \tag{16}$$

Summing up the loss shares of interval 1a and 2a, the total loss energy in S_1 during turn-off is

$$E_{T,off} = \frac{1}{2}t_{rv}V_0(I_0 - 2I_{oss}) + \frac{1}{2}t_{fi}(V_0 + V_{Ld})(I_0 - 2I_{oss}). \tag{17}$$

There, the forward recovery losses of the diode of S_2 are assumed to be negligible. Also the losses due to the recharging process of the parasitic capacitances are neglected. However, [20]–[22] presented energies up to 20% of the stored energy E_{oss} that are potentially lost in SiC devices during this interval. Since these losses can only be experimentally determined they are neglected here.

B. Scenario 2: Turn-On

A similar analysis can be performed when MOSFET S_1 is turned on, while the body diode of S_2 is conducting. The characteristic waveforms are shown in Fig. 4. During the switching process four intervals are distinguished which are analysed in the following. For $t < T_{on}$, MOSFET S_2 is turned off (approximately lossless) and its body diode starts conducting.
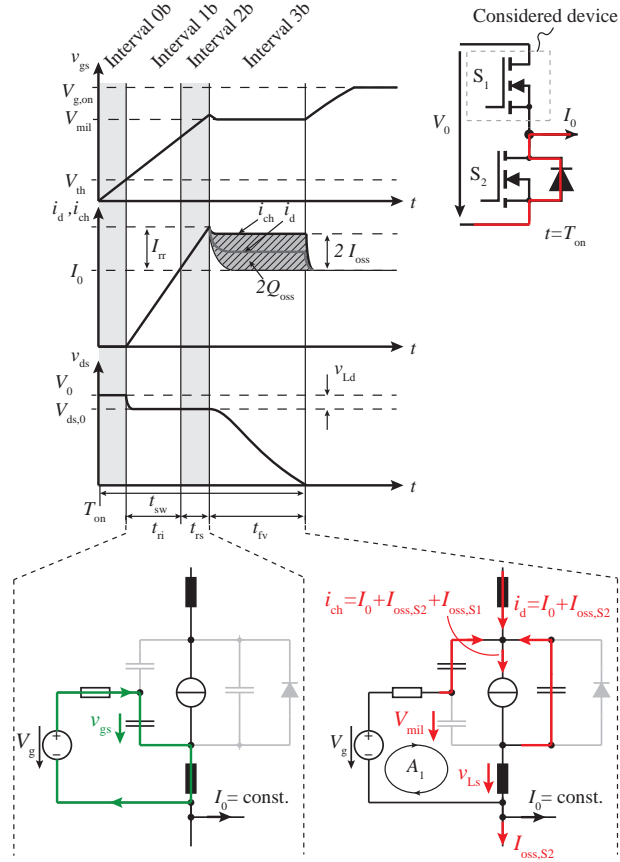
Fig. 4. The linearized MOSFET characteristics of the gate source voltage v_{gs}, the drain-source voltage v_{ds} and the channel current i_{d0} when the MOSFET S_1 is turned on. Below, the applied equivalent circuit to calculate the switching losses is depicted.

a) **Interval 0b**: After the interlocking time, S_1 is turned on at T_{on}, a positive V_g is applied and the gate source voltage v_{gs} rises to V_{th}. During this interval the drain source current is approximately zero. Thus, no impact on the losses in the devices is assumed.

b) **Interval 1b**: As soon as v_{gs} reaches the threshold voltage V_{th} (saturation region), the drain current rises to I_0 proportional to v_{gs} (see Fig. 4 Interval 1b). The current rise time t_{ri} is calculated analogue to the turn-off (see Fig. 4 b loop A_1) by

$$t_{ri} = -\ln\left(1 - \frac{I_0}{g_m(V_g - V_{th})}\right)(C_{gs}R_g + L_s g_m). \tag{18}$$

Due to the rising current, also a voltage across the parasitic inductance $v_{Ld} = L_d I_0 / t_{ri}$ is observed and v_{ds} decreases to $V_{ds,0}$. Contrary to the turn-off discussed above, L_d reduces the switching losses. For the sake of simplicity, here a small L_d is assumed, such that the voltage drop on v_{ds} has no influence on the predetermined voltage dependent charge equivalent capacitances.
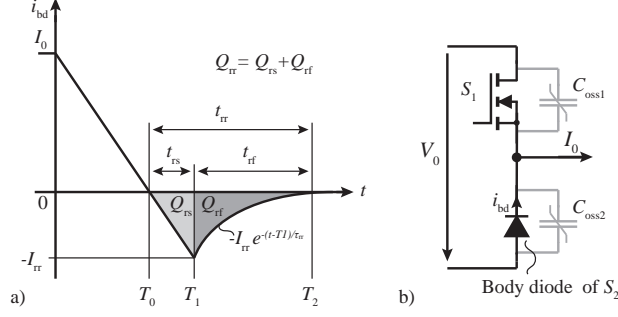
Fig. 5. a) Characteristic current waveform during the reverse recovery effect of the body diode of S_2. b) Equivalent circuit when the body diode of S_2 is conducting. Notice that C_{oss} is connected in parallel to the body diode.

c) *Interval 2b and Diode Reverse Recovery Model*: When i_d reaches I_0, the current increases further (see Fig. 4 Interval 2b) due to the reverse recovery effect of the body diode of S_2.

To estimate the time duration during which the body diode is reverse conducting t_{rs}, a model for a power diode derived in [18], [23]–[25] is applied, which is briefly summarized in the following.

Within this model, the characteristic diode current waveform (see Fig. 5 a)) can be calculated based on three characteristic values of the diode: the drift region transit time T_m, the effective carrier life time τ_c and the time constant τ_{rr} during the recovery phase t_{rf}. The diode current i_{bd} during this interval is

$$i_{bd}(t) = \begin{cases} I_0 - \frac{di_{bd}}{dt}t = \frac{I_0}{t_{ri}}t & t < T_1 \\ -I_{rr}e^{-\frac{t-T_1}{\tau_{rr}}} & t \geq T_1 \end{cases} \tag{19}$$

To determine I_{rr} and Q_{rr} for an arbitrary operating point the analytical equations (20) and (21) describing the lumped charge model of a diode [18] has to be solved.

$$i_{bd}(t) = \frac{q_e - q_m}{T_m} \tag{20}$$

$$q_m(t) = \frac{di_{bd}}{dt}\tau_c \left(T_0 + \tau_c - t - \tau_c e^{-t/\tau_c}\right) \quad t < T_1 \tag{21}$$

There q_e represents the injected minority charge carriers established by the diode current and q_m represents the internal available charge carriers. Charge q_e gets zero at T_1 [18], when the diode becomes reverse blocking. This current is assumed to be linearly decreasing, whereas the slope

is defined by the gate characteristic of MOSFET S_1. Thus, T_1 can be found by (e.g. numerical) solving (21) for T_1

$$q_e(T_1) = 0 = q_m(T_1) + T_m(I_0 - \frac{di_{bd}}{dt} T_1) \text{ with } \frac{di_{bd}}{dt} = \frac{I_0}{t_{ri}} \tag{22}$$

Knowing T_1, the values I_{rr}, Q_{rs} and t_{rs} (see Fig. 5 a) can be determined by

$$t_{rs} = T_1 - T_0 \tag{23}$$

$$I_{rr} = t_{rs} \frac{I_0}{t_{ri}} \tag{24}$$

$$Q_{rs} = \frac{1}{2} t_{rs} I_{rr} \tag{25}$$

Current I_0 is the current in the diode during the conducting state and T_0 is the time when the current through S_2 crosses zero. The above described equations can be used to extract the diode parameters from a datasheet as is demonstrated in section III-A.

For an arbitrary operating point the additional loss energies in MOSFET S_1 due to the reverse recovery effect are E_{rs} for the reverse conducting phase and E_{rf} for the recovery phase. They are determined based on the time integral of the respective current and the voltage.

$$E_{rs} = Q_{rs} V_{ds,0} \tag{26}$$

$$E_{rf} = \int_{T_1}^{T_2} -i_{bd}(t) v_{ds}(t) dt$$

$$= I_{rr} V_{ds,0} \frac{\tau_{rr}}{t_{fv}} \left(t_{fv} - \tau_{rr} + \tau_{rr} e^{-t_{fv}/\tau_{rr}} \right) \tag{27}$$

The loss energy in the body diode of S_2 are similarly calculated by

$$E_{rr,S2} = E_{D,off,S2}$$

$$= I_{rr} V_{ds,0} \frac{\tau_{rr}}{t_{fv}} \left(\tau_{rr} - (\tau_{rr} + t_{fv}) e^{-t_{fv}/\tau_{rr}} \right)$$

$$+ \tau_{rr} I_{rr} V_0 e^{-t_{fv}/\tau_{rr}}. \tag{28}$$

   d) Interval 3b: As soon as the body diode of S_2 blocks, the voltage across S_1 decreases. Analogue equations as for interval 1a of the turn-off of MOSFET S_1 can be applied to determine V_{mil} and I_{oss} (which becomes negative) whereas the underlying quadratic equation is

$$0 = -\frac{2L_s}{Q_{oss} R_g} I_{oss}^2 + \left(\frac{2}{g_m R_g} + \frac{C_{gd}}{C_{gd} + C_{ds}} \right) I_{oss} + \frac{1}{R_g} \left(V_g - V_{th} - \frac{I_0}{g_m} \right) \tag{29}$$

As described above, this is a iterative process where I_{oss}, g_m and V_{mil} have to be adapted in each iteration step. To calculate the drain and the channel current, i_d and i_{ch}, during this interval also

expressions (11) and (12) can be applied. Notice that during this interval the channel current is increased by $2|I_{oss}|$ due to the charging current required to charge C_{oss} of S_2 (assuming $I_0 = const$) and due to the device internal discharging process of S_1.

The resulting fall time of the drain-source voltage of S_1 is approximately

$$t_{fv} = -\frac{Q_{oss}}{I_{oss}} \tag{30}$$

Summarizing, the loss energy when MOSFET S_1 is turned on is

$$E_{T,on} = \frac{1}{2}t_{ri}V_{ds,0}I_0 + \frac{1}{2}t_{fv}(I_0 - 2I_{oss})V_{ds,0}+$$

$$t_{rs}V_{ds,0}I_0 + E_{rf} + E_{rs} \tag{31}$$

III. APPLICATION OF THE SWITCHING LOSS MODEL

In the following, the flowchart in Fig. 6 for applying the model in calculation routine (e.g. in MATLAB) is discussed, where the used equations are indicated. As example the SiC MOSFET C2M0080120D (1200V, 80mΩ, Wolfspeed) is considered, which is operated at $V_0 = 600\,\text{V}$ and I_0 is varied in the range of [0 A...40 A] at a junction temperature of 25 °C.

A. Step 1: Parameter Extraction

The main parameters of the device have to be extracted from the datasheet, what is briefly explained in the following.

1) MOSFET Parameters: To evaluate the switching losses, the MOSFET model in Fig. 1 is used. The parasitic MOSFET capacitances are linearized by their charge equivalent value. From the voltage dependent input, output and reverse transfer capacitance (C_{oss}, C_{iss}, C_{rss}) the charge equivalent capacitances are determined with

$$C_{\nu,q,eq} = \frac{1}{V_0}\int_0^{V_0} C_\nu(v_{ds})dv_{ds} \text{ with } \nu = oss, iss, rss \tag{32}$$

For the considered example device the resulting capacitances are

$$C_{gs} = C_{iss} - C_{rss} = 1080\,\text{pF} \tag{33}$$

$$C_{ds} = C_{oss} - C_{rss} = 130\,\text{pF} \tag{34}$$

$$C_{gd} = C_{rss} = 14.5\,\text{pF} \tag{35}$$

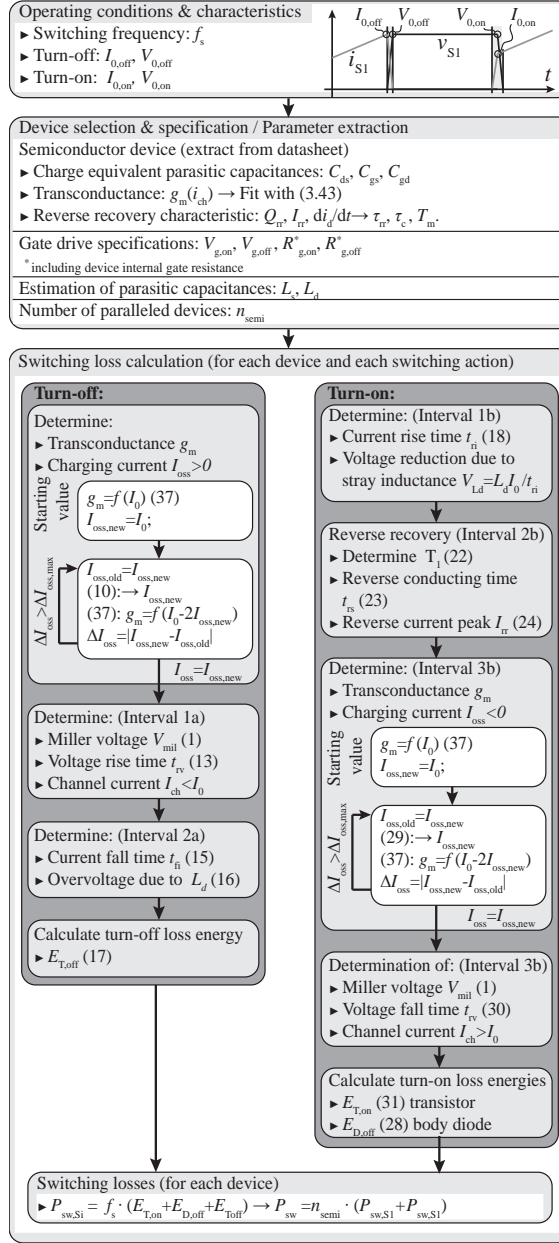and the stored charge Q_{oss} is $86.56\,\text{nC}$.

Fig. 6. Flowchart for calculating the turn-on and turn-off losses of MOSFETs in a half-bridge configuration.

As mentioned above, the transconductance is a function of i_{ch}.

$$i_{ch} = k_1(v_{gs} - V_{th})^x + k_2 \quad \text{with} \tag{36}$$

$$g_m(i_{ch}) = \sqrt[x]{\frac{k_1 i_{ch}^x}{i_{ch} - k_2}}, \tag{37}$$

The resulting constants from the datasheet shown in Fig. 7, are found by a curve fit and for this example $x = 3.80$, $k_1 = 0.1319$, $k_2 = -0.076$ for the corresponding $V_{th} = 4.5\,\text{V}$.
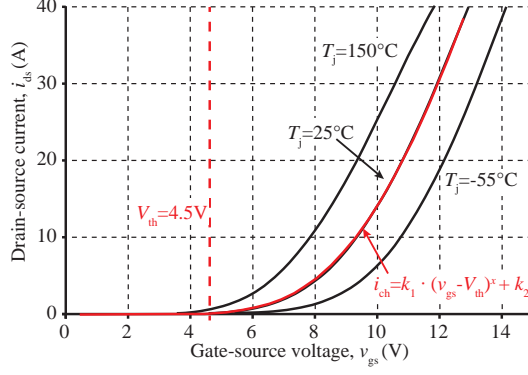
Fig. 7. Current dependency on the gate source voltage given in the datasheet of the C2M0080120D device, which is used to determine x, k_1, k_2 and the corresponding V_{th}.

2) Body Diode Reverse Recovery Parameters: The estimation of the diode reverse recovery losses is rather challenging. Often only a single measurement point is given in the datasheet, which usually does not correspond to the investigated operating conditions. For the considered device the provided values are the reverse recovery charge $Q_{rr} =192\,$nC, the reverse recovery time t_{rr}=32 ns and the reverse recovery peak current $I_{rr} = 10\,$A at a voltage of $V_0 = 800\,$V, a forward current of $I_0 =20\,$A and a current slope of $\frac{di_{bd}}{dt} = -2400\,$A/µs.

Notice that in the applied model, the body diode and the parasitic capacitances are considered separately. Since Q_{rr} often includes both charges, the datasheet value has to be corrected to $Q_{rr}^{\star} = Q_{rr} - Q_{oss} =88\,$nC.

To determine T_m, τ_c and τ_{rr}, which describe the diode reverse recovery behaviour, first Q_{rf} has to be estimated.

$$Q_{rf} = Q_{rr}^{\star} - \frac{I_{rr}^2}{2\,di_{bd}/dt} \tag{38}$$

The time constant τ_{rr} can be determined by integrating i_{bd} for the interval $T_1 < t < T_2$ (see Fig. 5) resulting in:

$$\tau_{rr} = \frac{Q_{rf}}{I_{rr}} \tag{39}$$

The effective carrier life time τ_c can be found by numerically solving [23]

$$I_{rr,dat} = \left.\frac{di_{bd}}{dt}\right|_{dat} \cdot (\tau_c - \tau_{rr}) \left(1 - e^{-T_1/\tau_c}\right). \tag{40}$$

According to [18] the drift region transition time T_m is linked to τ_c and τ_{rr} by

$$\frac{1}{\tau_{rr}} = \frac{1}{\tau_c} - \frac{1}{T_m}. \tag{41}$$

For the considered device, the diode behaviour is characterized by $T_m = 18.6\,\text{ns}$, $\tau_{rr} = 8.6\,\text{ns}$ and $\tau_c = 16\,\text{ns}$.

3) Estimation of the parasitic inductances: The parasitic inductances L_s and L_d are strongly dependent on the design of the PCB and the arrangement of the components as well as the internal bonding of the die. Usually the parasitic inductances introduced by the loops in the commutation path as well as in the connection of the gate drive are minimized to achieve a high performance. Therefore, the considered source inductance values caused by the package (here TO-247) are assumed to be approximately $4\,\text{nH}$ ([6], [26] and [27]).

B. Example Calculation

Based on the extracted parameters, the turn-on and turn-off losses in the half-bridge can be calculated. Additionally the configuration of the gate drive is required, which is here $V_g = -5\,\text{V}/+20\,\text{V}$ and $R_g = R_{g,ext} + R_{g,int} = 2.5\,\Omega + 4.6\,\Omega$.

The characteristic values of the different time intervals are summarized in Table I. The loss energies for the intervals during the switching process are depicted in Fig. 8 for different currents.
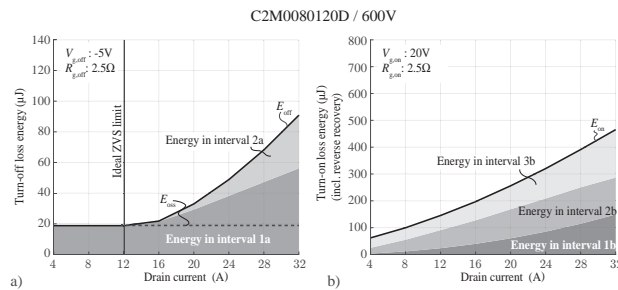

Fig. 8. Distribution of the loss energies on the different intervals during a) the turn-off and b) the turn-on for the C2M0080120D at 600 V.

	Turn-off		Turn-on	
Interval 1a/b	g_m	1.02 S	g_m	3.02 S
	I_{oss}	8.33 A	t_{ri}	10.7 ns
	I_{ch}	3.32 A	V_{Ld}	37.35 V
	V_{mil}	7.46 V		
	t_{rv}	10.5 ns		
Interval 2a/b	t_{fi}	3.5 ns	t_{rs}	4.6 ns
			I_{rr}	8.6 A
Interval 3b	-		g_m	4.1 S
	-		I_{oss}	−6.06 A
	-		I_{ch}	32.16 A
	-		V_{mil}	12.16 V
	-		t_{fv}	14.44 ns
Losses (device internal)	$E_{T,off}$	14.1 μJ	$E_{T,on}$	274 μJ
Stored energy	$E_{oss,S1}$	18.9 μJ	$E_{oss,S1}$	18.9 μJ

IV. MEASUREMENT RESULTS

The theoretical derivations of the previous sections have been experimentally validated. Additionally, the influence of the temperature and the influence of the source inductance are discussed.

A. Measurement Setup

To validate the model, the switching losses of different SiC MOSFETs have been measured with the test setup depicted in Fig. 9. The designed test-circuit consists of a symmetric half-bridge with configurable gate-drive voltages, whereas the device under test (DUT) is the low-side MOSFET. To evaluate the switching losses, a double pulse test has been performed and the drain-source voltage as well as the source current of the DUT have been measured. The drain-source voltage is measured directly at the corresponding MOSFETs pin with a high voltage probe (Lecroy PPE6kV, 6 kV). The drain current is measured at the source pin of the DUT with the high bandwidth rogowski coil presented in [28] in combination with a low voltage probe (Lecroy PP008-1). The DC-link consists of three film capacitors and provide a total

capacitance of 76 μF. In addition, ceramic capacitors close to the half-bridge are insert to reduce the commutation inductance. The 150 μH load inductor is realized with two series connected cable reels. All switching loss energies have been measured with the same laboratory test setup by an integration of i_d and v_{ds} as shown in Fig. 10.

B. Switching Loss Measurements

The loss model was evaluated for the two SiC devices, C2M0080120D (Wolfspeed, see Fig. 11) and the SCH2080KEC (Rohm Fig. 12) for different operating points. For both devices in the half-bridge, the turn-on loss energies are more than four times higher than the turn-off loss energies. The average error $\bar{e}$ with respect to the measurement points is below 10%. However, the model underestimates the switching losses during the turn-off at low currents where the estimation error is above 20%. This mainly results from the non-ideal recharging process of the parasitic capacitances [20]–[22]. In the turn-off measurements it can also been seen that the
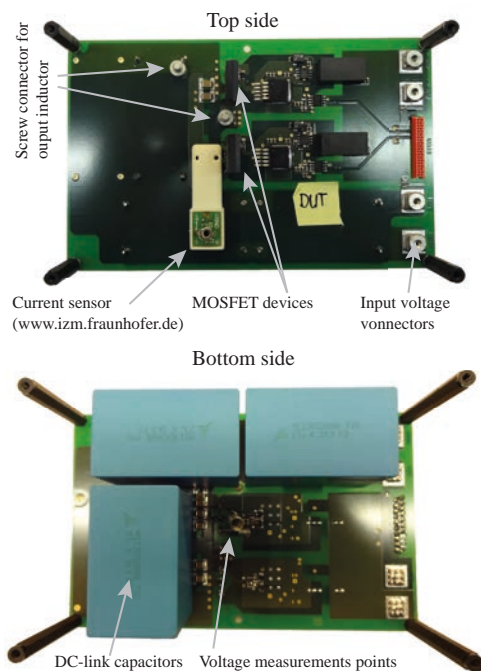

Fig. 9. Test half-bridge for the switching loss measurement consisting of a half-bridge, the gate-drive circuit and the dc-link capacitors. The load inductor is externally connected.
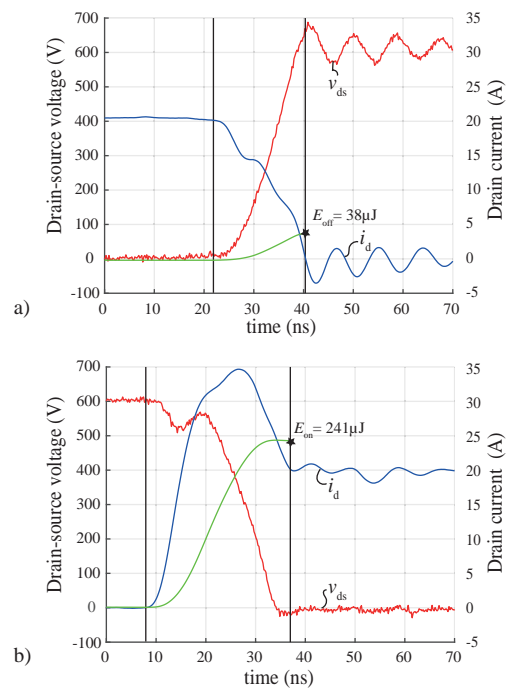

Fig. 10. a) Turn-off and b) turn-on characteristic waveforms of the C2M0080120D. The gate voltages are $V_{g,on}/V_{g,off} =$ 20 V/−5 V and an external gate resistance of 2.5 Ω is applied.

loss energies for high currents is rising less than the calculated loss energies. In the model the remaining current at the beginning of interval 2a (see Fig. 2, section II) is a linearized value. However, the current value at this time instant strongly depends on the exact recharging process of the parasitic capacitances, what is neglected in this simplified approach and needs further investigations.

Furthermore, the temperature dependency of the switching losses for both devices (see Fig. 13) differs a lot. For the C2M0080120D especially the turn-on losses strongly increase, while for the SCH2080KEC the switching losses are nearly temperature independent. The increased losses mainly result from the increased reverse recovery charge, whereas this effect is mitigated for the SCH2080KEC, which includes an additional antiparallel schottky diode. However, the
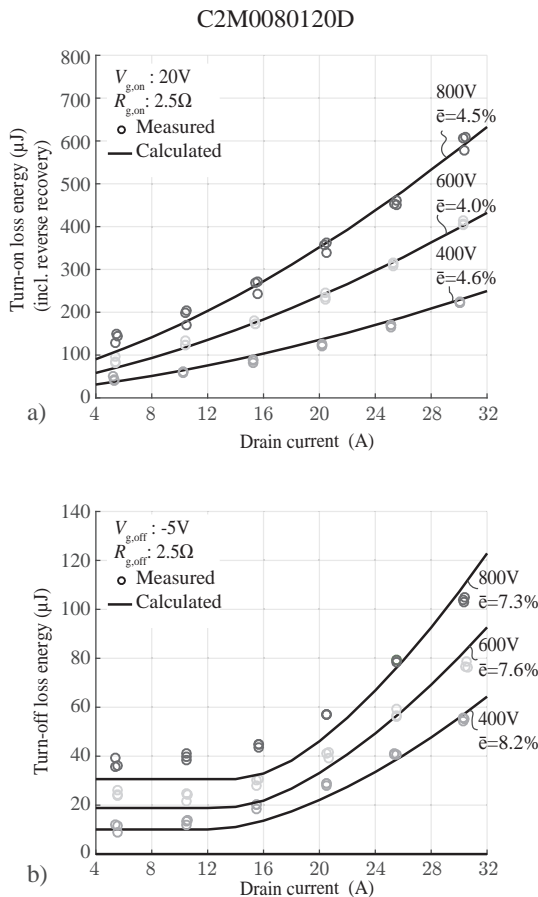

Fig. 11. a) Turn-on and b) turn-off switching loss energies of the C2M0080120D at a device temperature of 25 °C. The estimated L_s is 4 nH. The average error with respect to the measurement points is indicated by $\bar{e}$.
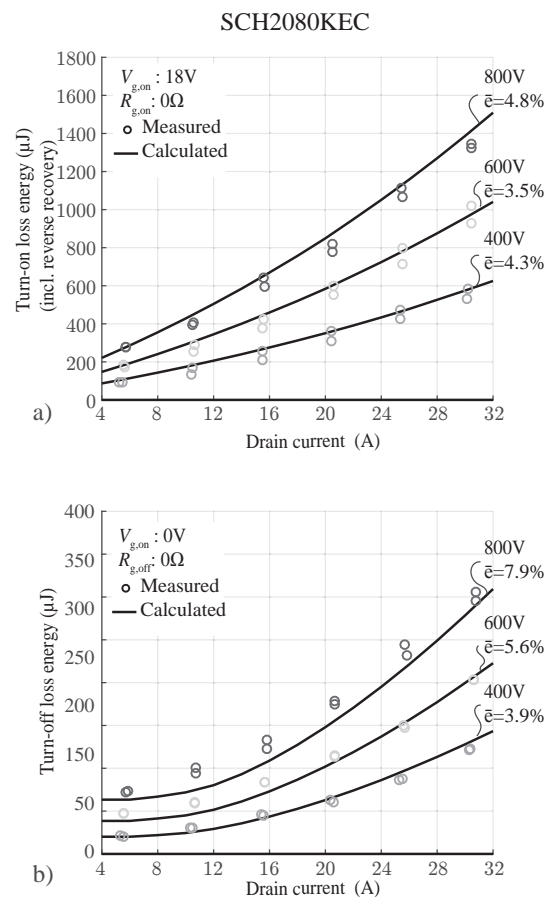
Fig. 12. a) Turn-on and b) turn-off switching loss energies of the SCH2080KEC at a device temperature of 25 °C. The estimated L_s is 4 nH. The average error with respect to the measurement points is indicated by $\bar{e}$.

information to accurately model the temperature dependency is often limited or missing in datasheets, why this effect is not included in the proposed model.

Finally, the value of the source inductance must be defined. In [26] and [27] the value has been estimated to be in the range of 2 nH to 5 nH for the TO-247 housing. As can be seen in Fig. 14, the impact of the source inductance on the switching losses is quite significant since it counteracts the gate-voltage. As a consequence, the commutation times increase and more losses are generated.
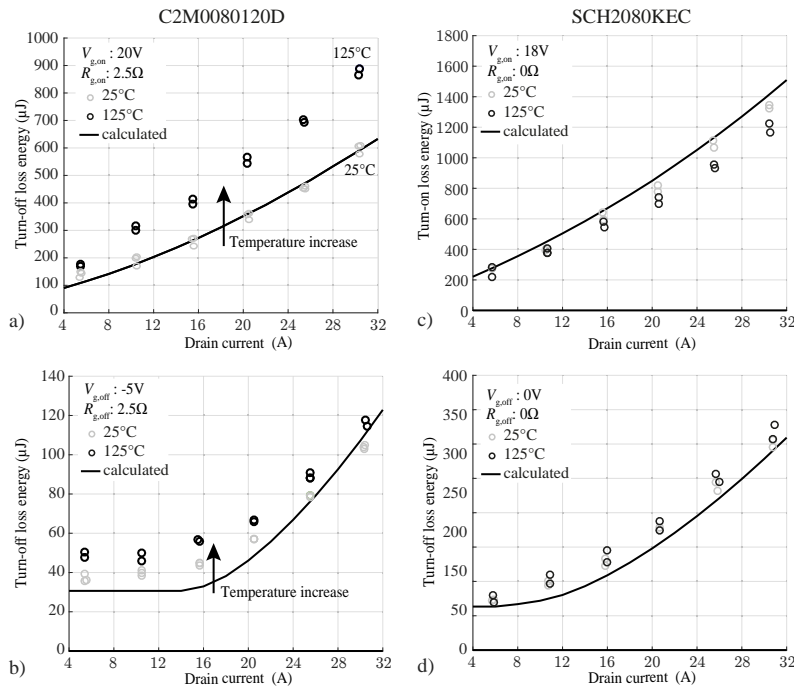

Fig. 13. Temperature dependency of the switching losses at $V_0 = 800\,\text{V}$: C2M0080120D a) turn-on and b) turn-off, SCH2080KEC c) turn-on and d) turn-off.
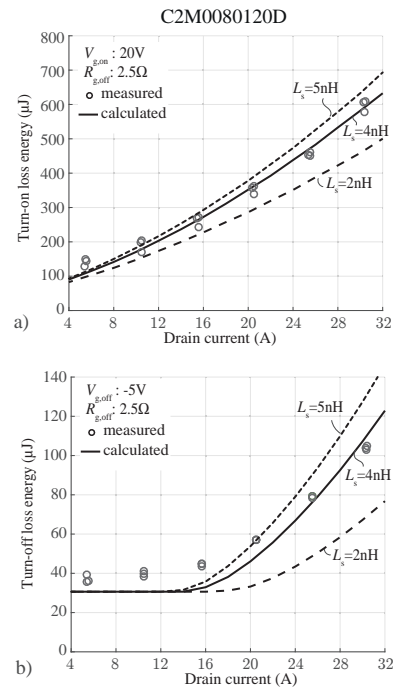
Fig. 14. Influence of the parasitic inductance on the switching losses at $V_0 = 800\,\text{V}$ for the C2M0080120D device during a) the turn-on and b) the turn-off.

V. Conclusion

In this paper, a simple method to estimate the switching losses of MOSFETs in a half-bridge configuration based on datasheet parameters only is presented and validated by measurements. During the switching transient the MOSFET is modelled by its charge equivalent parasitic capacitances. The stored charge and the energy in the parasitic capacitances of the MOSFET in a half-bridge configuration are directly connected. This allows the accurate determination of the voltage fall and rise times and furthermore enables a simple estimation of the device internal loss energies due to the recharging process.

Moreover, the model takes the reverse recovery of the body diode as well as the effect of the source inductance into account. During turn-off, the charge of the parasitic capacitances reduces the MOSFET current/switching loss energies and during turn-on the current in the device and accordingly the loss energy are increased. As a consequence for the considered devices the turn-on loss energies are more than four times higher than the turn-off loss energies.

In this paper also, an analytical expression to determine the ideal ZVS current range, where a nearly lossless turn-off of the MOSFET devices can be achieved, is presented.

Since the model relies on datasheet parameters only, limitations of the model are observed due to the available information about the device as well as the knowledge about the investigated half-bridge layout. This especially includes the temperature dependencies and the diode characteristics.

The MOSFET body diode is assumed to have a similar behaviour as a power diode. However, in datasheets often only a single measurement point is provided to estimate the diode's characteristic parameters and the reverse recovery charge provided in datasheets strongly depends on the applied measurement method [29]. In order to improve the accuracy of the model, further information would be desired to also include the temperature dependency, especially during the reverse recovery of the body diode.

If a large drain inductance (several $10\,\mathrm{nH}$) is present the voltage across the MOSFET devices changes during the current transients such that the stored charge in the parasitic capacitances would have to be adapted. For reasons of simplicity, this is neglected in this paper.

Further investigations are also needed in the second interval of the turn-off, to achieve a higher accuracy in the estimation of the remaining current in the channel, which has to be decreased.

Nevertheless, the model allows to estimate the switching loss energies within a mean error of 10%, and can be easily applied in a calculation routine.

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