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Output Voltage Ripple Analysis for Modular Series Parallel Resonant Converter Systems with Capacitive Output Filter

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Keywords

≪Voltage ripple calculation≫, ≪Resonant converter≫, ≪Fourier coefficients≫.

Abstract

In this paper, an analysis of the output voltage ripple of modular series parallel resonant converter systems with capacitive output filter is presented. An analytical description of the output voltage ripple of output series, output parallel as well as output parallel-output series connections of series parallel resonant converter basic modules is given. The derived equations can be used for investigating the voltage ripple due to component tolerances and non-optimal interleaving angles. The analytical results obtained by simulations and calculations match well with the measurement results. The verification of the determined equations is performed for different switching frequencies over the full range of possible interleaving angles. The measured results also match well for the time dependent waveforms.

1 Introduction

Series parallel resonant converter systems are used in many industrial applications, as e.g. telecom power supplies [1] or high output DC voltage generators [2]. Often only a single series parallel resonant converter basic module (SPRC-Bm) is applied as depicted in Fig. 1 (a) and the output filter C_f is sufficient to keep the output voltage ripple low. However, in high voltage pulsed power applications several modules are required [3]. An example is the european spallation source (ESS) modulator system [4], where eight SPRC-Bms stacks are connected in series at the output in order to generate the required output voltage of $V_{Out} = 115\,kV$ and to keep the output voltage ripple low. Each stack is formed by two SPRC-Bms connected in parallel, to achieve an output power of 2.88 MW. In the considered system, a maximum output voltage ripple of $\Delta v_{Cf} \leq 1\,\%$ of V_{Out} and a maximum energy $E \leq 10\,J$, which is stored in the filter capacitor is allowed. To reduce the ripple voltage, all modules are interleaved. The value of the output capacitor C_f is limited to a maximal value due to the maximum stored energy constraint, resulting in a minimal voltage ripple.

In the literature, the ripple analysis for a single SPRC-Bm is explained in [5] and an estimation is presented in [6], but there is a lack for systems with an arbitrary number of modules and arbitrary output connections. Therefore, a general detailed analysis of the output voltage ripple of SPRC-Bms with arbitrary output connections and interleaved operation is derived in this paper.

In section 2, the ripple derivation of a single SPRC-Bm (Fig. 1 (a)) is given and the formulas for a pure output series (OS) (Fig. 1 (b)), a pure output parallel (OP) (Fig. 1 (c)) and an output parallel-output series (OP-OS) (Fig. 1 (d)) systems are derived. The models are verified by measurement and simulation results in section 3.

2 Output voltage ripple analysis

In this section, the output voltage ripple analysis of a single SPRC-Bm is given. Afterwards, equations for series and parallel output connections of an arbitrary number of SPRC-Bms are derived.

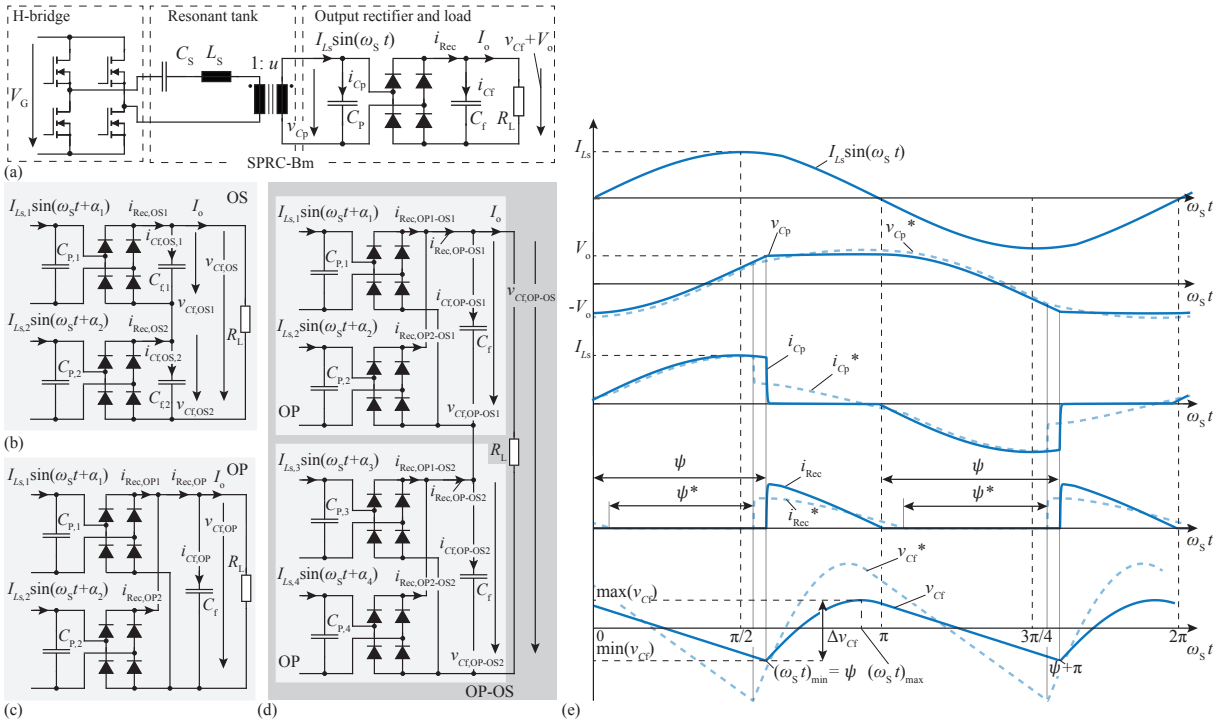

Figure 1: (a) Single SPRC-Bm formed by a H-bridge, a resonant tank and the output rectifier stage with load. The total output voltage is the superposition of the ripple voltage v_{Cf} and the average voltage V_o. Output rectifier stages of (b) an output series connected (OS) system, of (c) an output parallel connected (OP) system and of (d) an output parallel-output series connected (OP-OS) system. The averaged output voltages V_o are not shown in (b) to (d), because only the ripple voltages $v_{Cf,Oxx}$ are in the scope of interest. (e) Simulated typical basic current and voltage output circuit waveforms of a SPRC-Bm (see Fig. 1 (a)). The solid line waveforms are of a SPRC-Bm, where $C_f \gg C_P$ and the dashed line waveforms are if $C_f \approx C_P$. The averaged output voltage V_o is not shown, because just the ripple voltage v_{Cf} is in the scope of interest.

2.1 Output voltage ripple of a single SPRC-Bm

The analysis of the output voltage ripple of a SPRC-Bm is based on the analysis presented in [5]. For the sake of completeness, the main governing equations, which are used for the further analysis in sections 2.2 and 2.3, are shortly repeated. The definition of the used variables and components are given in Fig. 1 (a) and Fig. 1 (e). The output current of the rectifier i_{Rec} is defined by:

$$i_{Rec}(\omega_s t) = \begin{cases} 0 & 0 \le \omega_s t < \psi \\ I_{Ls}\sin(\omega_s t) & \psi \le \omega_s t < \pi \\ 0 & \pi \le \omega_s t < \pi + \psi \\ -I_{Ls}\sin(\omega_s t) & \pi + \psi \le \omega_s t < 2\pi \end{cases} \tag{1}$$

with

$$\psi = \arccos\left(\frac{\pi - 2\omega_s R_L C_P}{\pi + 2\omega_s R_L C_P}\right), \tag{2}$$

where ψ is the non-conduction angle of the rectifier as shown in Fig. 1 (e) and ω_s is the angular switching frequency. The peak secondary transformer current I_{Ls} is calculated based on (3) in [7]

$$I_{Ls} = \frac{2V_o\omega_s C_P}{1 + \cos(\pi - \psi)}, \tag{3}$$

Table 1: Component values of a single SPRC-Bm used for the calculations in Fig. 2 and in Fig. 3.

L_S	C_S	C_P	R_L	V_G	u
(μH)	(nF)	(nF)	(Ω)	(V)	($-$)
4.24	840	4.24	1150	400	20

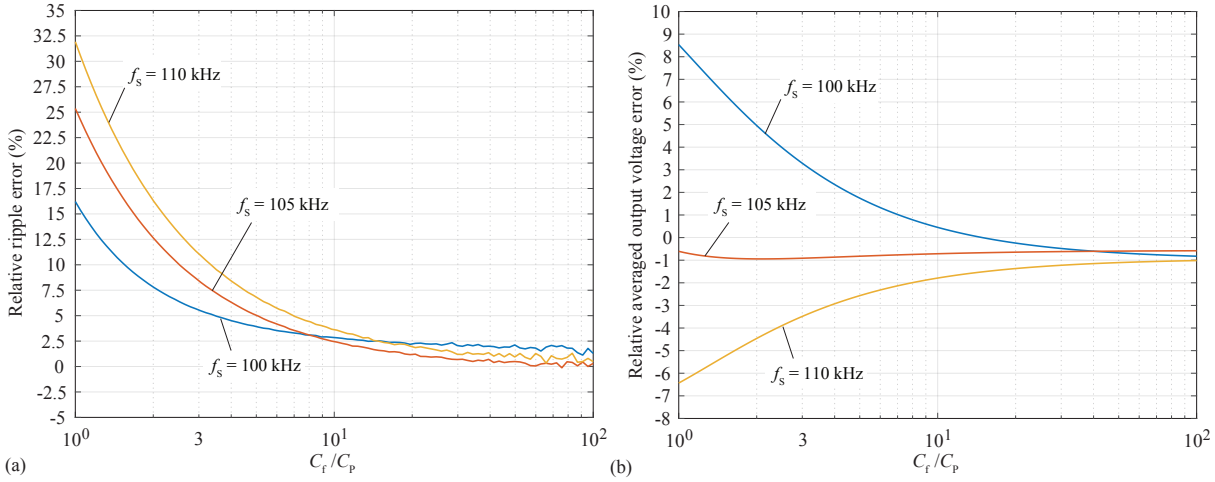

Figure 2: (a) Relative error between the calculated (with (10)) and the simulated output voltage ripple of a single SPRC-Bm for different switching frequencies. (b) Relative error between the calculated and the simulated averaged output voltage V_o of a single SPRC-Bm for different switching frequencies.

and also the average output voltage V_o is taken from [7]. The load current I_o is the average current of the output rectifier current i_{Rec} during a switching period

$$I_o = \frac{1}{\pi}\int_{\psi}^{\pi} i_{Rec}\,\mathrm{d}(\omega_s t) = I_{Ls}(1+\cos(\psi))\frac{1}{\pi}. \tag{4}$$

Applying Kirchhoff's law, the current i_{Cf} of the filter capacitor C_f can be calculated as

$$i_{Cf}(\omega_s t) = i_{Rec}(\omega_s t) - I_o. \tag{5}$$

where the load current I_o is the average current of the output rectifier current i_{Rec} during a switching period. Using (5) and solving the integral results in the filter capacitor voltage v_{Cf}

$$v_{Cf}(\omega_s t) = \frac{1}{\omega_s C_f}\int i_{Cf}(\omega_s t)\,\mathrm{d}(\omega_s t) = \begin{cases} -\dfrac{I_o(\omega_s t)}{C_f\omega_s} + X_1 & 0 \le \omega_s t < \psi \\ -\dfrac{I_o}{C_f\,\omega_s}\left(\dfrac{\pi\cos(\omega_s t)}{1+\cos(\psi)} + (\omega_s t)\right) + X_2 & \psi \le \omega_s t < \pi, \end{cases} \tag{6}$$

where X_1 and X_2 are integration constants. The angle $(\omega_s t)_{max}$ related to the maximum of v_{Cf} is calculated by setting the derivative of the second part of (6) to zero

$$\frac{\mathrm{d}}{\mathrm{d}(\omega_s t)}\left(\frac{-I_o}{C_f\,\omega_s}\left(\frac{\pi\cos(\omega_s t)}{1+\cos(\psi)} + (\omega_s t)\right) + X_2\right) = 0 \tag{7}$$

and solving (7) for $\omega_s t$. To find the maximum, the result has to be shifted by π, what results in

$$(\omega_s t)_{max} = \pi - \arcsin\left(\frac{1+\cos(\psi)}{\pi}\right). \tag{8}$$

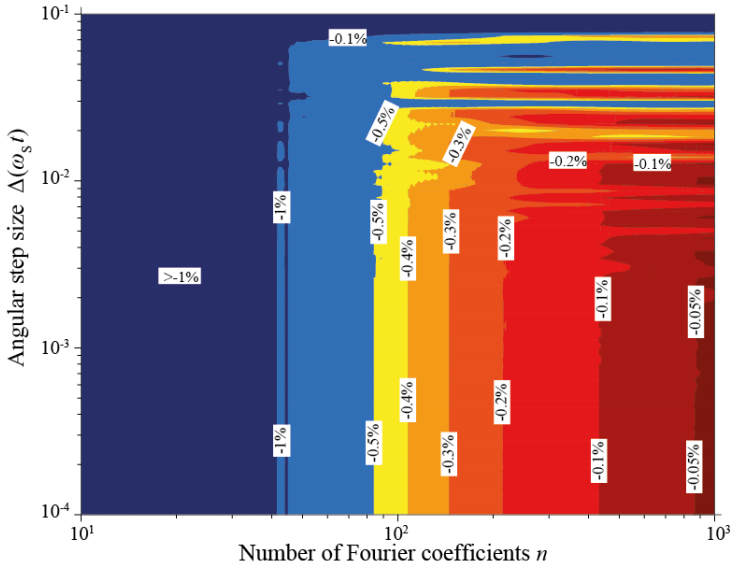

Figure 3: Relative deviation of the fourier series (12) and the exact solution (10) of the output voltage ripple Δv_{Cf} in dependance of the angular step size $\Delta(\omega_s t)$ used in (12) and the number of fourier coefficients n.

The angle related to the minimum of v_{Cf} is

$$(\omega_s t)_{\min} = \psi. \tag{9}$$

Finally, the output voltage ripple Δv_{Cf} is given by

$$\begin{aligned} \Delta v_{Cf} &= v_{Cf}((\omega_s t)_{max}) - v_{Cf}((\omega_s t)_{min}) = \\ &= \frac{I_o}{\omega_s C_f}\left[\frac{\left[\arcsin\left(\frac{1+\cos(\psi)}{\pi}\right)+\psi\right][1+\cos(\psi)]}{(1+\cos(\psi))} + \frac{\sqrt{\pi^2-(1+\cos(\psi))^2}-\pi}{(1+\cos(\psi))}\right]. \end{aligned} \tag{10}$$

Equation (10) is derived based on the assumption that $C_f \gg C_P$, which results in a nearly perfectly clamped parallel capacitor voltage v_{Cp} during the rectifier conduction interval as can be seen in Fig. 1 (e)). If $C_f \approx C_P$, the voltage $v_{Cp}{}^*$ is not strictly constant during the rectifier conduction interval (compare v_{Cp} and $v_{Cp}{}^*$ in Fig. 1 (e)) and the current $I_{Ls}\sin(\omega_s t)$ is divided into $i_{Cp}{}^*$ and $i_{Rec}{}^*$, as can be seen in Fig. 1 (e). This results in a different non-conduction angle ψ^* and leads to a larger error of (10). Figure 2 (a) shows the relative error between the simulated and the calculated output voltage ripple and Fig. 2 (b) shows the relative error between the simulated and the calculated averaged output voltage V_o related to C_f/C_P for different switching frequencies f_s of a single SPRC-Bm. It is clearly shown in Fig. 2 (b) that the variation of the filter capacitor C_f only has a minor effect (approx. $\pm$ 10 % in the worst cases) on the averaged output voltage and can be therefore neglected. The frequency range (100 kHz - 110 kHz) is chosen with respect to the design in [4]. The specifications for the calculations and the simulations, are given in Tab.1. Figure 3 shows the relative deviation between the fourier series (12) and the exact solution (10) of the output voltage ripple Δv_{Cf} in dependance of the angular step size $\Delta(\omega_s t)$ used in (12) and the number of fourier coefficients n. The principle ripple calculation procedure for an OS, an OP and an OP-OS system is depicted in the flow chart of Fig. 4, as a kind of ripple calculation guide. The detailed derivations according to the flow chart are given in the following.

2.2 Output voltage ripple of an OS system

Figure 1 (b) shows the output circuit of an OS system. There, both rectifiers are connected in series. In order to investigate an interleaved operation, (6) has to be developed into its fourier series. The

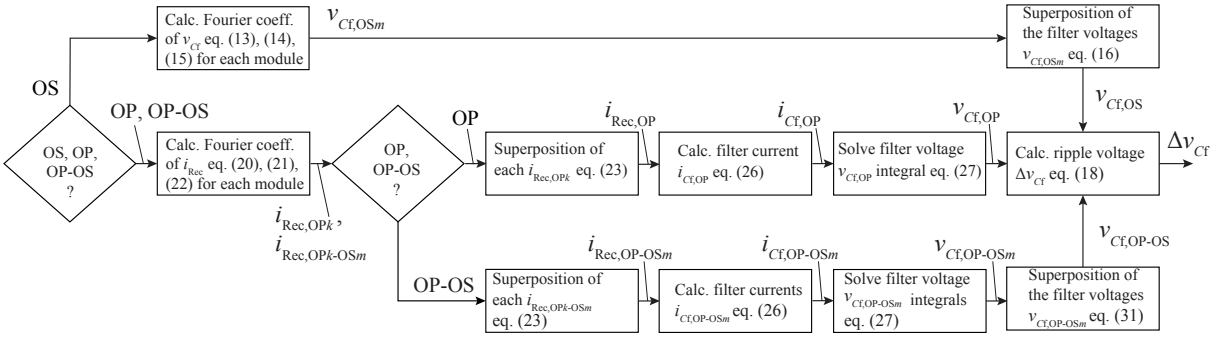

Figure 4: Principle ripple calculation flow chart of the output series (OS), output parallel (OP) and the output parallel-output series (OP-OS) system.

integration constants X_1 and X_2 are calculated by

$$v_{Cf}(\psi) = 0 \rightarrow \begin{cases} X_1 = \dfrac{I_o \psi}{\omega_s C_f} \\ X_2 = \dfrac{I_o}{C_f \omega_s} \left(\dfrac{\pi \cos(\psi)}{1+\cos(\psi)} + \psi \right) \end{cases} \tag{11}$$

The time dependent fourier series of the output voltage ripple $v_{Cf}(\omega_s t)$ is given by

$$v_{Cf}(\omega_s t) = \frac{a_o}{2} + \sum_{n=2}^{\infty} a_n \cos(n\omega_s t) + b_n \sin(n\omega_s t) \tag{12}$$

with its fourier coefficients

$$a_o = \frac{I_o \left[\pi \cos(\psi) - \pi + 2\sin(\psi) + 2\psi\right]}{\omega_s C_f (\cos(\psi)+1)} \tag{13}$$

$$a_n = \frac{I_o \left[1+(-1)^n\right] \left[\frac{\sin(n\psi-\psi)(n+1)+\sin(n\psi+\psi)(1-n)}{2}\right]}{nC_f\omega_s (\cos(\psi)+1)(n^2-1)} \tag{14}$$

$$b_n = -\frac{I_o \left[1+(-1)^n\right] \left[\frac{\cos(n\psi-\psi)(n+1)+\cos(n\psi+\psi)(1-n)}{2}+1\right]}{nC_f\omega_s (\cos(\psi)+1)(n^2-1)}. \tag{15}$$

The total output voltage ripple is determined by the superposition of the output voltages of each SPRC-Bm

$$v_{Cf,OS}(\omega_s t) = \sum_{m=1}^{M} v_{Cf,OSm}(\omega_s t + \alpha_m) \tag{16}$$

with

$$\alpha_m = \kappa_m - \varphi_m \quad \text{and} \quad \kappa_m = \frac{(m-1)\pi}{M}. \tag{17}$$

The angle α_m is the difference between the optimal interleaving angle κ_m of each SPRC-Bm and its input impedance angle φ_m, which is calculated with (35) in [7]. M is the number of SPRC-Bm in series at the output. Computing the maximum and the minimum of the output ripple voltage $v_{Cf,OS}$ results in the output voltage ripple Δv_{Cf}

$$\Delta v_{Cf} = \max(v_{Cf,OS}) - \min(v_{Cf,OS}). \tag{18}$$

2.3 Output voltage ripple of an OP system

Figure 1 (c) shows the output circuit of an OP system. There, both rectifiers are connected in parallel. In order to investigate an interleaved operation, (1) has to be developed into its fourier series. The time dependent fourier series of the output rectifier current i_{Rec} is given by

$$i_{\mathrm{Rec}}(\omega_{\mathrm{s}}t) = \frac{a_{\mathrm{o}}}{2} + \sum_{n=2}^{\infty} a_n \cos(n\omega_{\mathrm{s}}t) + b_n \sin(n\omega_{\mathrm{s}}t), \tag{19}$$

with its fourier coefficients

$$a_{\mathrm{o}} = I_{Ls}\frac{2(\cos(\psi)+1)}{\pi} \tag{20}$$

$$a_n = -\frac{I_{Ls}\left[1+(-1)^n\right]\left[\frac{\cos(n\psi-\psi)(n+1)+\cos(n\psi+\psi)(1-n)}{2}+1\right]}{\pi(n^2-1)} \tag{21}$$

$$b_n = \frac{I_{Ls}\left[1+(-1)^n\right]\left[\frac{-\sin(n\psi-\psi)(n+1)+\sin(n\psi+\psi)(n-1)}{2}\right]}{\pi(n^2-1)}. \tag{22}$$

The total output rectifier current $i_{\mathrm{Rec,OP}}$ is determined by the superposition of the rectifier currents of each SPRC-Bm

$$i_{\mathrm{Rec,OP}}(\omega_{\mathrm{s}}t) = \sum_{k=1}^{K} i_{\mathrm{Rec,OP}k}(\omega_{\mathrm{s}}t + \alpha_k) \tag{23}$$

with

$$\alpha_k = \kappa_k - \varphi_k \quad \text{and} \quad \kappa_k = \frac{(k-1)\pi}{K}. \tag{24}$$

The angle α_k is the difference of the optimal interleaving angle κ_k of each SPRC-Bm and its input impedance angle φ_k. K is the number of SPRC-Bm in parallel at the output. The integral of the load current I_{o}

$$I_{\mathrm{o}} = \frac{1}{\pi}\int_0^{\pi} i_{\mathrm{Rec,OP}}\,\mathrm{d}(\omega_{\mathrm{s}}t) \tag{25}$$

has to be solved numerically and the filter current $i_{Cf,\mathrm{OP}}$ is given by

$$i_{Cf,\mathrm{OP}}(\omega_{\mathrm{s}}t) = i_{\mathrm{Rec,OP}}(\omega_{\mathrm{s}}t) - I_{\mathrm{o}}. \tag{26}$$

The output voltage $v_{Cf,\mathrm{OP}}$ is calculated numerically by

$$v_{Cf,\mathrm{OP}}(\omega_{\mathrm{s}}t) = \frac{1}{\omega_{\mathrm{s}}C_{\mathrm{f}}}\int i_{Cf,\mathrm{OP}}(\omega_{\mathrm{s}}t)\,\mathrm{d}(\omega_{\mathrm{s}}t) + X_3, \tag{27}$$

where the integration constant X_3 is set to zero, because the offset in the output voltage is not in the scope of interest for the ripple calculation. Inserting (27) in (18) results in the total output ripple voltage Δv_{Cf}. The optimal interleaving angle κ, which results in a minimum voltage ripple is exemplary given in Fig. 5 for 2 to 5 OS or OP systems. The component values for the calculations are given in Tab.1 and are the same for all modules. The switching frequency is 104.5 kHz and the filter capacitance C_{f} is 15.49 nF.

2.4 Output voltage ripple of an OP-OS system

Figure 1 (d) shows the rectifier circuit of an OP-OS system, which is a series connection of OP systems. The output voltage for each OP system is calculated using (19) to (27), where (24) is replaced by the following (28), which determines the optimal interleaving angle of each SPRC-Bm and its input impedance

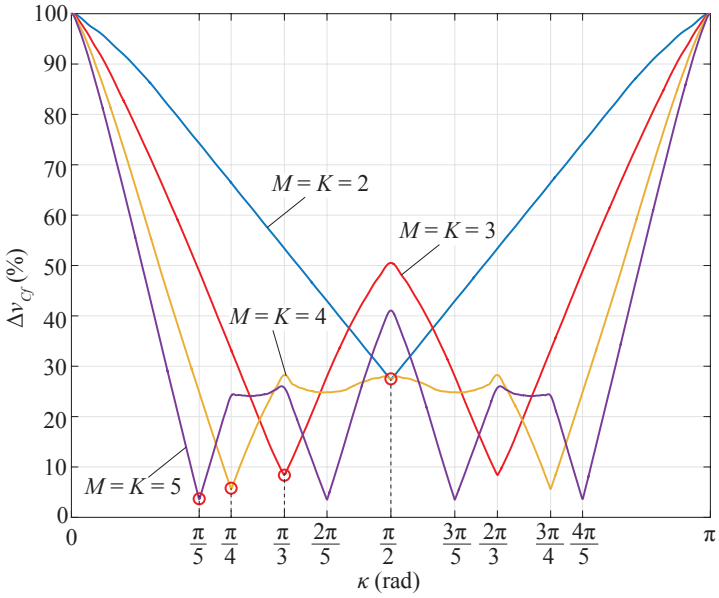

Figure 5: Optimal interleaving angles (red circles) for OP or OS system with two to five SPRC-Bms. The component values are given in Tab.1 and are the same for all modules. The used switching frequency is 104.5 kHz and the filter capacitor C_f is 15.49 nF.

Table 2: Component and input values of the OP prototype system with parallel connected outputs used for the calculation and simulation results in Fig. 7.

C_{f1} (nF)		8.48		f_{s1} (kHz)		104.5	
C_{f2} (nF)		28.48		f_{s2} (kHz)		104	
L_S	C_S	C_P	V_G	u	R_L	n	$\Delta\omega_\mathrm{s}t$
(μH)	(nF)	(nF)	(V)	($-$)	(Ω)	($-$)	(mrad)
4.29	840	4.24	400.3	20	1118	200	0.318

angle $\varphi_{k,m}$. It is assumed that each OP system consists of K SPRC-Bms and M is the number of OP systems in series.

$$\alpha_{k,m} = \kappa_{k,m} - \varphi_{k,m} \tag{28}$$

with

$$\kappa_{k,m} = \frac{(k-1)\pi}{K} + \frac{(m-1)\pi}{MK} \tag{29}$$

and

$$k = [1 \ldots K], \quad m = [1 \ldots M]. \tag{30}$$

The total output voltage $v_{\mathrm{Cf,OP\text{-}OS}}$ is calculated by the superposition of each OP output voltage by

$$v_{\mathrm{Cf,OP\text{-}OS}}(\omega_\mathrm{s}t) = \sum_{m=1}^{M} v_{\mathrm{Cf,OP\text{-}OS}m}(\omega_\mathrm{s}t + \alpha_{k,m}). \tag{31}$$

Again, using (31) in (18) results in the output ripple voltage Δv_{Cf}.

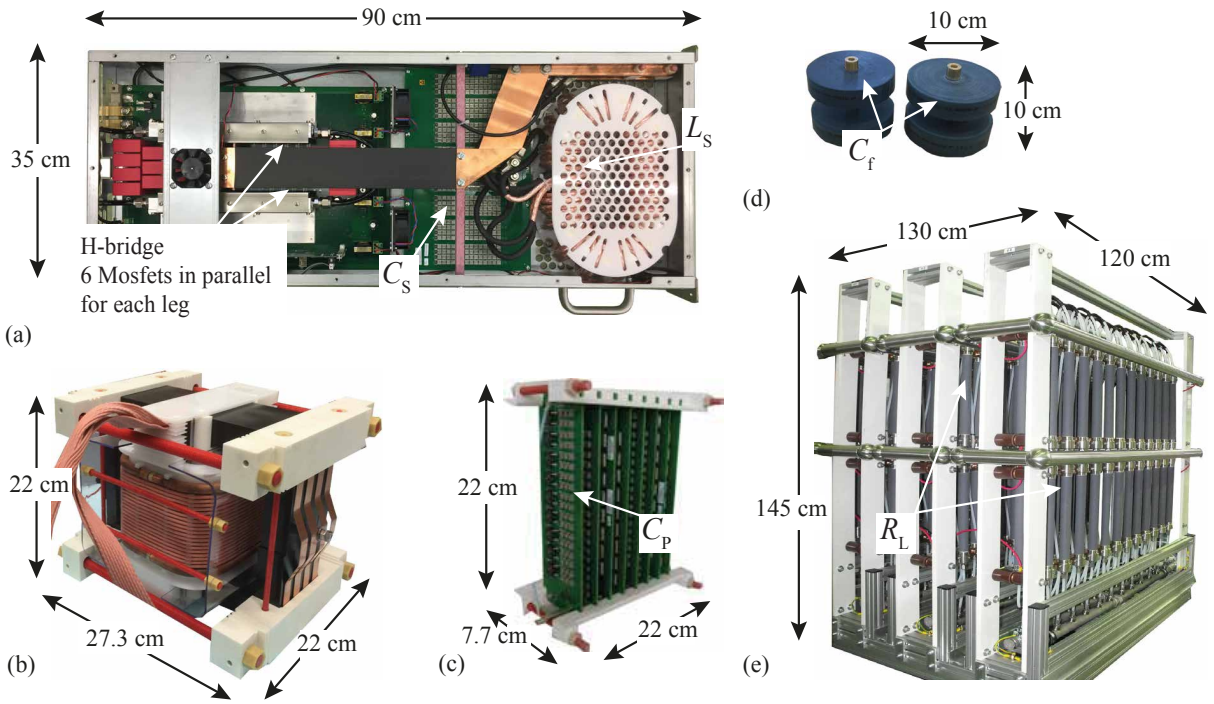

Figure 6: (a) Single SPRC-Bm with H-bridge, series inductor L_S and capacitor C_S. (b) High voltage high frequency transformer. (c) Output rectifier with parallel capacitor C_P, (d) filter capacitors C_f and (e) high voltage load R_L. For the measurements, two SPRC-Bms are connected in parallel at the output according to Fig. 1 (c).

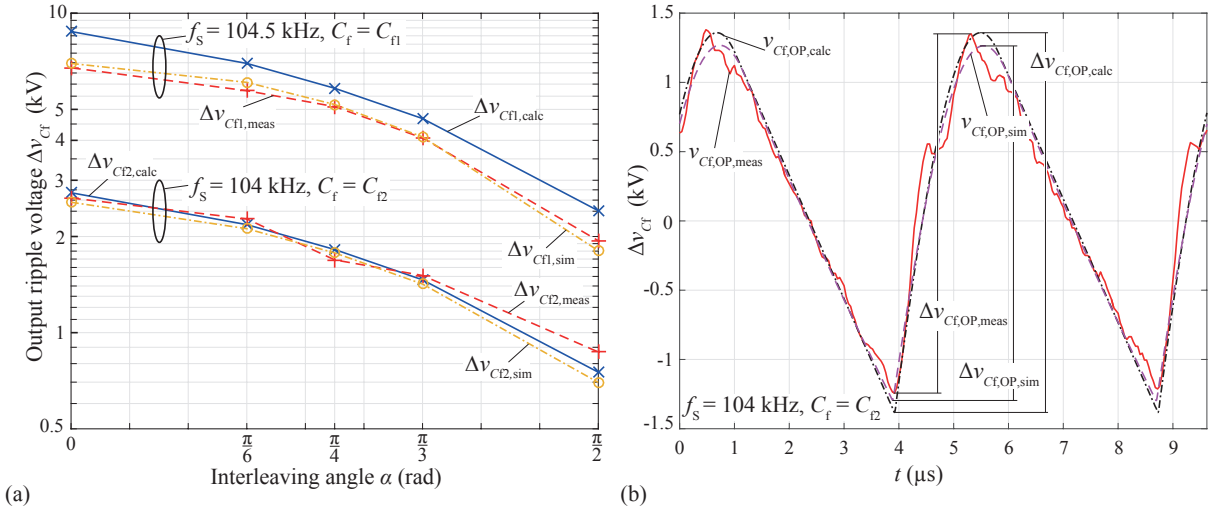

Figure 7: (a) Calculated $\Delta v_{Cfi,calc}$, simulated $\Delta v_{Cfi,sim}$ and measured $\Delta v_{Cfi,meas}$ total output voltage ripple of an OP system with two modules, operated with different angels α. The comparison is given for different output filter capacitors $C_{f1}/2 = C_P$ and $C_{f2}/2 = 3.35 \cdot C_P$ (compare the relative error in Fig. 2 (a)). (b) Calculated $v_{Cf,OP,calc}$, simulated $v_{Cf,OP,sim}$ and measured $v_{Cf,OP,meas}$ output voltage ripple of an output parallel (OP) prototype system with two modules, which is operated non interleaved at a switching frequency f_s of 104 kHz and an output filter capacitor $C_f = C_{f2}$.

3 Simulation and measurement results

In this section, the analysis is verified by comparing measurement and simulation results of an OP prototype system, which consists of two SPRC-Bms. The pictures of a single SPRC-Bm with series inductor L_S and capacitor C_S, of the output rectifier with the parallel capacitor C_P, of the output filter C_f and of the

high voltage load R_L are shown in Fig. 6. The component and input voltage values for both prototype SPRC-Bms, which are used for the ripple simulations and calculations, are given in Tab.2. Figure 7 (a) shows the total output voltage ripple Δv_{Cf} of the OP system, which is operated with different interleaving angles α. The evaluation is given for different filter capacitors and switching frequencies. The calculated total ripple values are in good accordance with the simulated and the measured values. Also, the calculated time dependent waveforms match well with the simulated and the measured waveforms, as could be seen in Fig. 7 (b). There, the OP system is operated in non interleaved mode and with a switching frequency f_s of 104 kHz.

4 Conclusion

In this paper, the ripple model of arbitrary output connections of series parallel resonant converter basic modules (SPRC-Bms) are derived. The analysis is based on the ripple calculations of a single SPRC-Bm and is then extended to either output parallel, output series, or output parallel and series connections of SPRC-Bms. The calculated output voltage ripple is verified by simulations and measurements of an output parallel (OP) prototype system. The analytical results match very well with the simulated and the measured results and also match well to the time dependent waveforms. The derived formulas can be used for ripple investigations caused by component tolerances or by the interleaved operation of the SPRC-Bms in order to determine the minimum required filter capacitor value.

Acknowledgment

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List of symbols

OS	Output series connected
OP	Output parallel connected
OP-OS	Output parallel-output series connected
SPRC-Bm	Series parallel resonance converter basic module
V_G	Input voltage of a SPRC-Bm
V_Out	Output voltage of SPRC-system
V_o	Output voltage of a SPRC-Bm
I_{Ls}	Peak secondary transformer current
I_o	Load current
ψ, ψ^*	Non conduction angle of the rectifier
$\Delta(\omega_\mathrm{s}t)$	Angular step size
$v_{C\mathrm{p}}$,$v_{C\mathrm{p}}{}^*$	Parallel capacitor voltage
v_{Cf}	Ripple voltage
$v_{Cf,\mathrm{OS}}$	Ripple voltage of an OS-system
$v_{Cf,\mathrm{OP}}$	Ripple voltage of an OP-system
$v_{Cf,\mathrm{OP\text{-}OS}}$	Ripple voltage of an OP-OS-system
$v_{Cf,\mathrm{OS}m}$	m-th ripple voltage of an OS-system
$v_{Cf,\mathrm{OP\text{-}OS}m}$	m-th ripple voltage of an OP-OS-system
i_Rec, $i_\mathrm{Rec}{}^*$	Rectifier current
$i_\mathrm{Rec,OP}$	Rectifier current of an OP-system
α	Phase shift angle
α_m	m-th phase shift angle of an OS-system
α_k	k-th phase shift angle of an OP-system
$\alpha_{k,m}$	k-th, m-th phase shift angle of an OP-OS-system
a_o, a_n, b_n	Fourier coefficients
φ	Input impedance angle
φ_m	m-th input impedance angle of an OS-system
φ_k	m-th input impedance angle of an OP-system
$\varphi_{k,m}$	k-th, m-th input impedance angle of an OP-OS-system
C_S	Series capacitor
L_S	Series inductor
C_P	Parallel capacitor
C_f	Output filter capacitor
R_L	Load resistor
u	Transformer ratio
E	Energy stored in the system
ω_s	Angular switching frequency
f_s	Switching frequency
Δv_{Cf}	Maximal voltage ripple
t	Time
$i_{C\mathrm{p}}$, $i_{C\mathrm{p}}{}^*$	Parallel capacitor current
i_{Cf}	Filter capacitor current
$i_{Cf,\mathrm{OS}m}$	m-th filter capacitor current of an OS-system
$i_{Cf,\mathrm{OP}}$	Filter capacitor current of an OP-system
$i_{Cf,\mathrm{OP\text{-}OS}m}$	m-th filter capacitor current of an OP-OS-system
$i_{\mathrm{Rec,OS}m}$	m-th rectifier current of an OS-system
$i_{\mathrm{Rec,OP\text{-}OS}m}$	m-th rectifier current of an OP-OS-system
$i_{\mathrm{Rec,OP}k}$	k-th rectifier current of an OP-system
$i_{\mathrm{Rec,OP}k\text{-}\mathrm{OS}m}$	k-th, m-th rectifier current of an OP-OS-system
κ	Interleaving angle
κ_m	m-th interleaving angle of an OS-system
κ_k	k-th interleaving angle of an OP-system
$\kappa_{k,m}$	k-th, m-th interleaving angle of an OP-OS-system
n	Number of fourier coefficients
K	Number of SPRC-Bms in parallel
M	Number of OP-systems or SPRC-Bms in series
X_1, X_2, X_3	Integration constants

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