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COAXIAL CAPACITIVE VOLTAGE DIVIDER WITH HIGH DIVISION RATIO FOR HIGH VOLTAGE PULSES WITH VERY FAST RISE TIMES

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Abstract

In this paper, a capacitive voltage divider with a high division ratio of >1:1000 based on a high voltage coaxial cable and discrete foil capacitors mounted around the cable is investigated. The divider is designed for high voltage pulses up to 200 kV and has a relatively simple and robust design. For the presented voltage divider a circuit model is presented, which is also validated by measurements using a impedance analyzer and by comparisons with HV standard voltage probes.

I. INTRODUCTION

In many areas efficiency improvements are investigated to minimise global warming effects. This is also true for drilling processes, where novel methods are required for significantly improving efficiency. A promising approach is plasma channel drilling (PCD) ([1], [2]), which is based on electrical discharges through the rock as shown in Fig. 1. The voltage V_1 between the two electrodes must have a high amplitude, in the range of a few 100 kV and requires a very high dv/dt (>1 MV/μs), in order to achieve a discharge through the rock and not the water [1], [3]. With discharges through water the energy consumption rises and therefore reduces drilling efficiency.

For investigating the pulse parameters required for an efficient PCD process, a test setup has been built as shown in Fig. 2. On the left hand side, the high voltage capacitor, providing the energy, is shown. In order to be able to measure the energy, which is transferred to the plasma channel, and analyzing the breakdown conditions, the voltage across the two electrodes needs to be measured accurately. Next to the load a capacitive divider, which is based on the Haefely High Voltage Construction Kit and which consists of two high voltage capacitors, is shown in Fig. 2. The intended application area of the divider are lightning impulses and due to its relatively large capacitance, it influences the measurement result significantly. Additionally, its large dimensions result in a relatively large stray inductance and in a high sensitivity to noise as could be seen in Fig. 3. Since accurate measurements are required for obtaining the energy consumption of the PCD process, a compact and relatively simple coaxial capacitive is presented in the following.

In the considered PCD system, pulses with amplitudes of 200 kV and rise times below 100 ns from 0 V to 200 kV are generated. For measuring these voltages with an oscilloscope a high division ratio of at least 1:1000 is required,

TABLE I: Specifications of the considered pulse voltage measurement system.

Operating voltage V_1	$<$ 200 kV
Division ratio	$>$ 1:1000
Operating frequency	$>$ 1 MHz

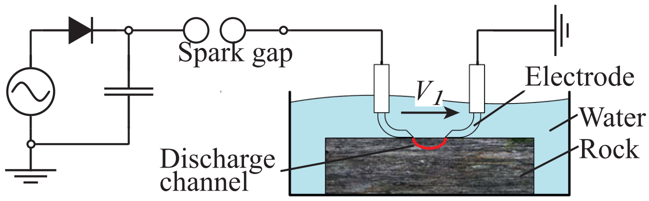

Fig. 1: Principle circuit for the plasma channel drilling (PCD).

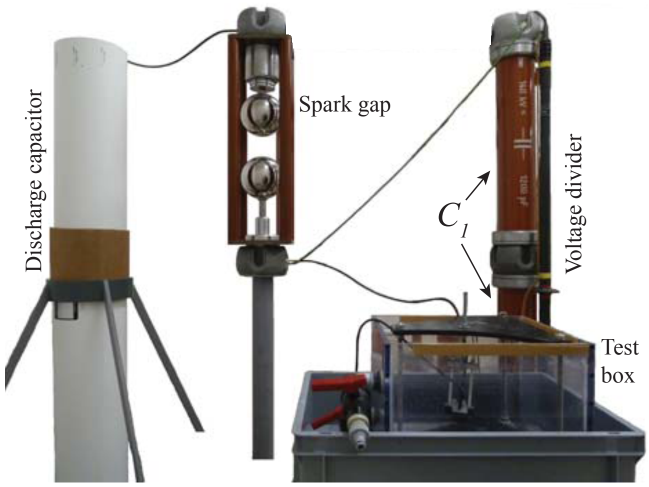

Fig. 2: Photo of the circuit arrangement for PCD (the charging unit is not shown).

so that the specifications given in Table I of the considered divider result. The division ratio of the divider directly depends on the values of the two series connected impedances

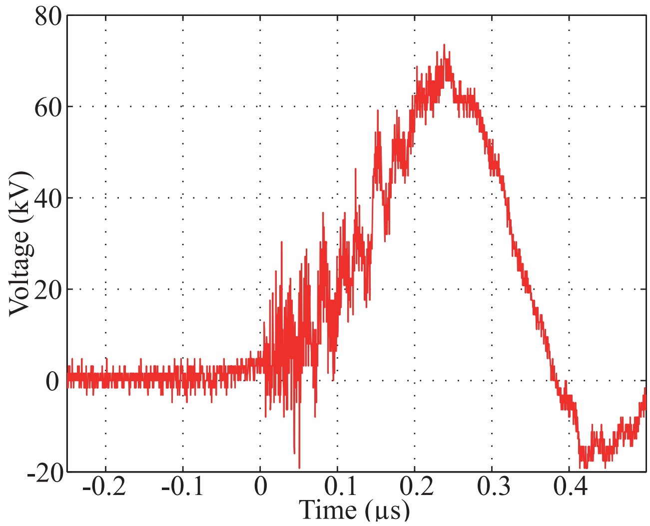

Fig. 3: Voltage measured with the capacitive divider shown in Fig. 2.

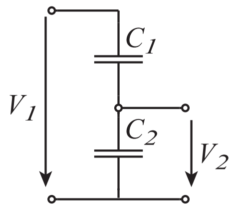

Fig. 4: Basic schematic of the voltage divider.

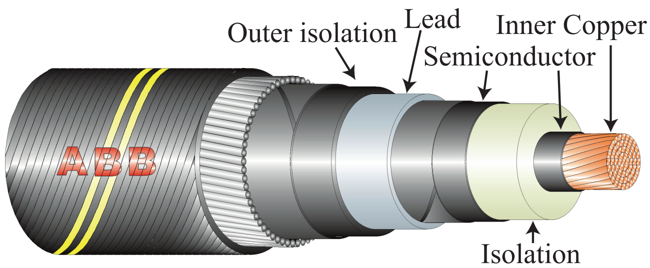

Fig. 5: Illustration of the applied HVDC cable.

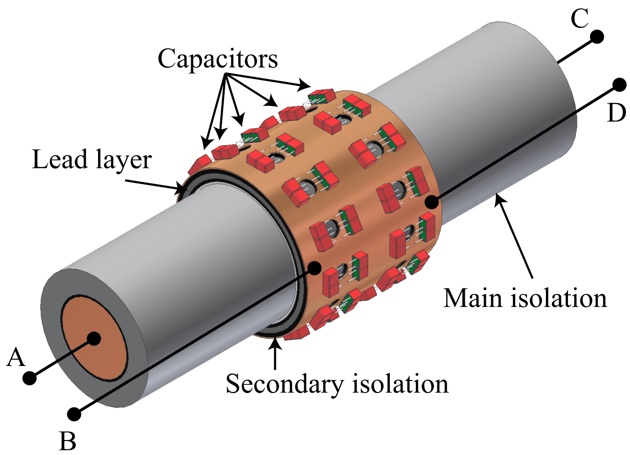

Fig. 6: Sketch of the cable with capacitors.

(Fig. 4) and can be calculated by

$$1 : n = \frac{C_1}{C_1 + C_2} \quad (1)$$

for an ideal capacitive divider, where C_1 is the primary capacitance, C_2 the secondary capacitance and n the division ratio.

For interconnecting the high voltage capacitor, the spark gap and the electrodes, connectors are required. There, coaxial high voltage cables can be used, which inherently provide the high voltage capacitor C_1 (cf. Fig. 4). This avoids the requirement for oil as insulation and results in a compact design. With the compact and optimized design also the parasitics are minimized, accordingly the performance of the voltage divider increases.

In Table II the data of published coaxial voltage dividers is given. All of them utilize self-made capacitors as secondary capacitor C_2. To achieve a high division ratio, a high difference between the value of C_1 and C_2 is needed. The value of C_1 is fixed by the high voltage cable and is usually in the range of few pF. Thus C_2 must be in the range of a few nF, in order to achieve a division ratio in the range of 1:1000 or higher. Such high capacitance values are difficult to achieve reliably with custom made foil capacitors. Therefore, most of the published dividers have a much lower division ratio. Also the maximum allowed voltage of the dividers is lower than the required 200 kV pulse voltage.

The divider with the number 4 in Table II is the only one, which does not use a cylindrical shape for C_2. It is based on a custom made layer of ceramic discs. Ceramic materials are very brittle and to achieve high capacitance very thin layers are required. Therefore, care and special supporting arrangement is required to maintain the capacitor in good shape.

In order to simplify the design and achieve a more robust setup, utilizing small discrete foil capacitors in combination with a high voltage cable is investigated in this paper. With such capacitors a very simple design results and high division ratios are possible. In **section** II first, the mechanical and electrical design of the divider is shown. Thereafter, measurement results are presented in **section** III. There, also the limitations of the presented design are discussed and in **section** IV possibilities to improve the design and performance of the divider are proposed.

TABLE II: Specifications of published coaxial dividers.

No.	Peak voltage	Division ratio	C_2	Reference
1	not specified	≈1:4.84/1:4.64	Self-made	[4]
2	<100 kV	≈1:2778	Self-made	[5]
3	not specified	not specified	Self-made	[6]
4	450 kV	1:3500	Self-made	[7]
5	100 kV	1:110	Self-made	[8]
6	≤20 kV	1:110	Self-made	[9]

II. CONSTRUCTION OF THE DIVIDER

In a first step, the considered divider is based on a 200 kV HVDC submarine cable from ABB [10] (Fig. 5), which acts as C_1. In Fig. 5 all cable layers and in Table III the cable specifications are given. The first three layers were removed completely and for the coaxial part forming C_1, the lead and the outer isolation layer are used as can be seen in Fig. 6 and Fig. 7 showing the final design.

For C_2 different ideas mainly based on self-made capacitors have been proposed (Table II), but in the considered divider discrete foil capacitors distributed uniformly around the divider cable have been utilized.

After removing the outer layers, holes were drilled into the outer isolation layer to provide needed connection points for the discrete foil capacitors. The surface of the outer isolation was covered with copper foil to provide the ground layer.

For reducing the noise influence on the measurement, both capacitors C_1 and C_2 should have a relatively high capacitance value. This, however, increases the impact of the capacitive divider on the circuit due to the relatively large charging current flowing through C_1 and C_2. On the other hand, a very small capacitance value for the two capacitors

TABLE III: Divider dimensions.

Inner conductor diameter	48 mm
Inner diameter of the lead layer	86.6 mm
Outer diameter of the lead layer	92.6 mm
Outer diameter of the outer insulation	97.6 mm
Thickness of the copper foil	0.1 mm
Number of holes	24
Diameter of a hole	10 mm
Length of the coaxial cable (C_1)	100 mm
Total length of active the cable	320 mm

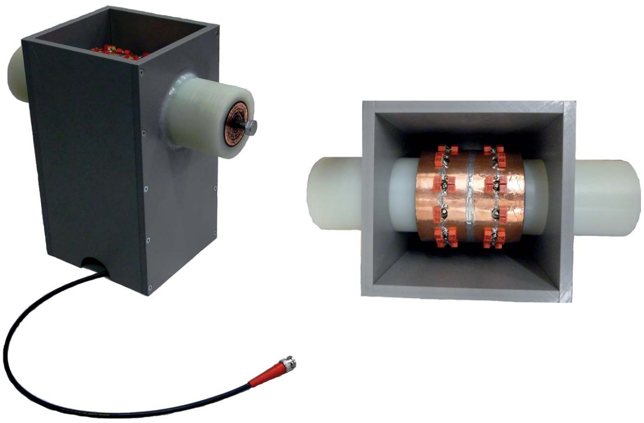

Fig. 7: Final setup of the divider. Left: side view; right: top view of the divider.

increases the impact of parasitic capacitances which might result in worst case in a varying division ratio depending on the measurement setup. Therefore, a compromise must be made, where also the maximum allowed voltage of the oscilloscope has to be respected.

The capacitance of the original HVDC cable was measured to be 307 pF/m and for obtaining a suitable value for C_1, the length of the divider has been set to 10 cm, so that ideally C_1=30.7 pF results. However, due to parasitic capacitances in the area, which is not covered by the lead layer, a value of C_1=44.4 pF results. This could also be seen in the COMSOL Multiphysics simulations, which have been performed for calculating the value of C_1. This results in C_1=37.6 pF. The COMSOL simulations also enable a better insight in the capacitance and inductance distribution of the divider and give indications of possible noise sources due to capacitive couplings to the surrounding. Theoretical calculations with the coaxial arrangement formula can be done as

$$C = \frac{2 \cdot \pi \cdot \varepsilon \cdot \varepsilon_0 \cdot l}{ln(\frac{D}{d})} \tag{2}$$

Where C- capacitance; ε_r- relative permittivity of the material; ε_0=8.85e-12 F/m; l- length of the material; d and D- inner and outer diameter of the material. The computed value $C_1 \approx$30 pF is close to the value of the ideal setup without parasitic capacitances. In section III-A more detailed measurement results for the considered divider are shown.

The voltage division ratio of the considered divider is set to 1:1200, so that with

$$C_2 = (n-1) \cdot C_1 \tag{3}$$

the value of C_2 could be determined tp be C_2=37.53 nF. The capacitance between the ground and the secondary layer (C_2') can be calculated with Eq. 2 which resulted in $C_2' \approx$250 pF. For capacitor C_2, discrete WIMA FKP 2 film capacitors for pulse applications with a maximal operating voltage V=1000 V_{dc} and a capacitance of C_{cap}=470 pF ($\pm 5\%$) are chosen. These are through-hole devices, so that the pins can be directly soldered between the secondary ring and the ground layer. Capacitances C_2 and C_2' are in parallel and by knowing their values, the number of the required capacitors can be calculated according to

$$N = \frac{C_2 - C_2'}{C_{cap}}, \tag{4}$$

which results in 80 capacitors, that are soldered on the cable.

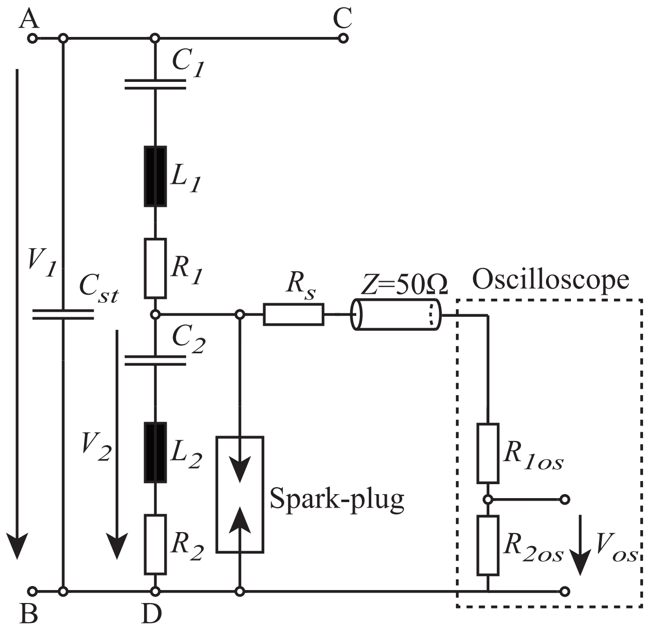

Fig. 8: Equivalent circuit of the divider and the measurement cables between the divider and the oscilloscope.

For interconnecting the divider with the measurement system a PCB with a resistor and a spark plug is soldered on the ground surface. To the PCB a 50 Ω BNC cable is soldered, so that a series resistance with R_s=50 Ω is required for impedance matching (Fig. 8). The added spark plug is used for safety reasons to protect the oscilloscope.

For mechanically supporting the device a plastic box is used as shown in Fig. 7. That provides the required safety distance to ground and helps to mechanically protect the device.

III. RESULTS

For evaluating the performance of the capacitive voltage divider, first measurements of the component impedance and the transfer function have been performed. Secondly, the performance of the divider in the PCD setup has been determined.

A. Impedance measurements

The equivalent circuit parameters of the circuit given in Fig. 8 and in Table IV have been identified based on impedance plots as given in Fig. 10, which have been measured with a Novocontrol Alpha-A impedance analyzer. With the measured circuit parameters the theoretical impedance curves as shown in Fig. 10 and the simulated transfer function of the divider as given in Fig. 11 can be calculated. The theoretical curves and the equivalent circuit enable a better understanding of the physical limits of the divider performance and allow to improve the device.

For determining the values of the capacitances C_1, C_2 and C_{st}, three measurements were conducted as described in Fig. 9. The capacitor C_{st} reflects the parasitic capacitance of the divider between the ground connection and the high voltage signal. There is also some stray capacitance between the signal layer an the high voltage signal, which is neglected as it is relatively small compared to C_2.

For the considered divider, the measurement results are: C_a=44.428 pF, C_b=256.59 pF and C_c=41.008 pF. Based on

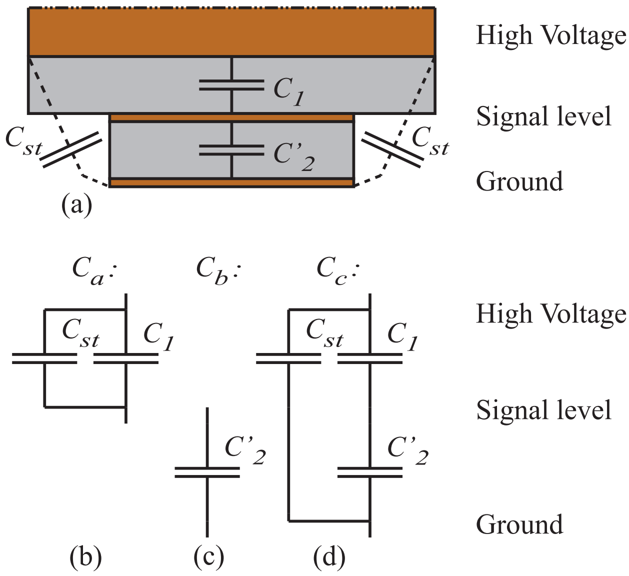

Fig. 9: (a) Capacitances between different layer. (b)-(d) Three measurements performed to get the values of C_a, C_b and C_c.

the equations:

$$C_a = C_1 + C_{st} \tag{5}$$

$$C_b = C'_2 \tag{6}$$

$$C_c = C_{st} + \frac{C_1 * C_2}{C_1 + C_2}, \tag{7}$$

the values for the capacitances can be determined: C_1=31.38 pF, C_{st}=13.05 pF, C'_2=256.59 pF and C_2=37.077 nF (cf. also Table IV). These values are well following expectations and theoretical calculations as described in section II.

In Fig. 11 the measured and simulated transfer functions V_2/V_1 of the divider are plotted. The simulations are performed with models implemented in Ansoft Simplorer. As can be seen, the measured and calculated transfer functions match quite well, except for the damping of the resonance, which is much higher in the measurement. This might be caused by HF resistances not included in the divider model.

Based on the performed measurements and simulations, the division ratio could be identified. With the measured transfer function, a division ratio of 1:1189 results. While from the simulation a division ration of 1:1199 results, which is very close to the measured value. Also the theoretical value 1:1183, which could be determined with equation 1 and the measured values of C_1 and C_2 from Table IV matches the others very well.

Finally, a signal generator was used to generate rectangular pulses in order to compare the divider with the

TABLE IV: Measured equivalent circuit parameters.

High voltage capacitance, C_1	31.38 pF
Low voltage capacitance, C_2	37.077 nF
Stray capacitance, C_s	13.05 pF
Capacitance Signal-to-ground, C'_2	256.59 pF
Parasitic inductance, L_1	500 nH
Parasitic inductance of the capacitors, L_2	450 nH
Series resistance of the measurement cable, R_s	50 Ω
Resistance of high voltage side, R_1	5 Ω
Resistance of low voltage side, R_2	0.01 Ω
Resistance of oscilloscope probe, R_{1os}	9 MΩ
Resistance of oscilloscope, R_{2os}	1 MΩ

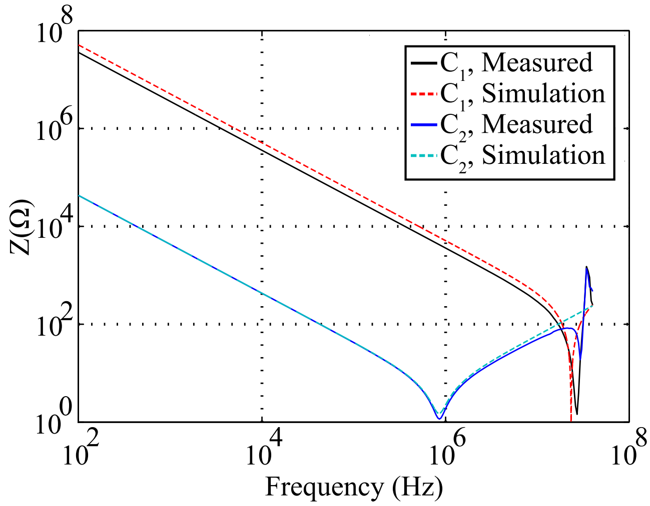

Fig. 10: Measured and calculated impedances of capacitor C_1 and C_2.

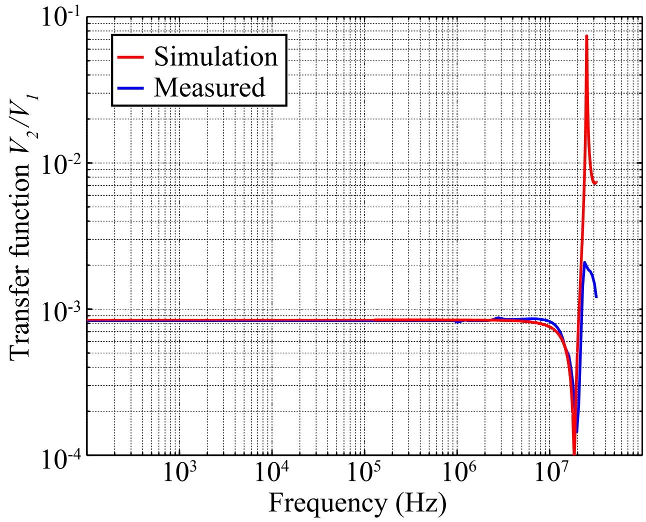

Fig. 11: Measured and calculated transfer functions of the voltage divider.

performance of a 20 kV LeCroy voltage probe. The results are given in Fig. 12 for a 1 MHz. Studying the results shows faster response of the cable divider compared to the the LeCroy 20 kV probe, otherwise the performance is similar. The ringing frequency, that can be seen in Fig. 12, is coherent with resonance frequencies (f_{res}=26 MHz).

B. Performance in the PCD setup

For modelling the complete PCD setup and determine the performance of the divider in the setup, the source impedance Z_{in} and the load impedance Z_{out} as seen by the divider have been measured with the impedance analyser (cf. Fig. 13). The results are given in Fig. 14.

In Fig. 15 one can see the circuit topology around the divider. The source impedance (Z_{in}) includes impedances of the discharge capacitor and connecting cables. The input impedance Z_{in} has a low resonance frequency as the used pulsed capacitor (custom made by Condenser Products, V=250 kV_{dc}, C=10 nF, L_σ=70 nH) has a relatively high capacitance. As can be seen, the load and the input impedance is not matched to the divider impedance, so that the measurement results are affected.

Using the equivalent circuit parameters of the divider together with input and output impedances allows plotting the transfer function that includes all circuit (Fig. 16). Com-

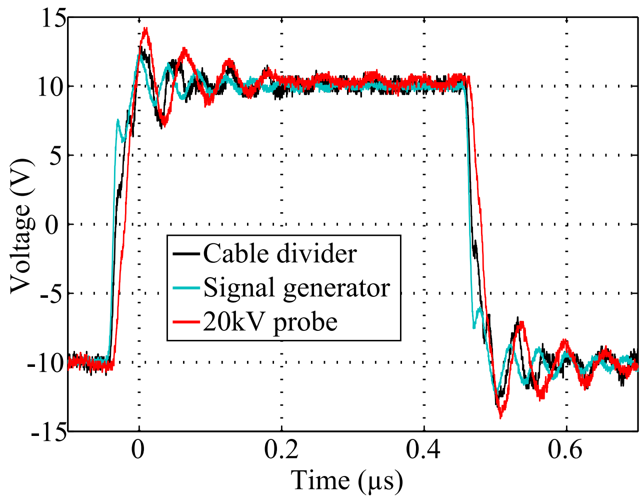

Fig. 12: Measured voltage curves while using a signal generator.

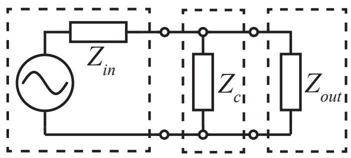

Fig. 13: General circuit scheme.

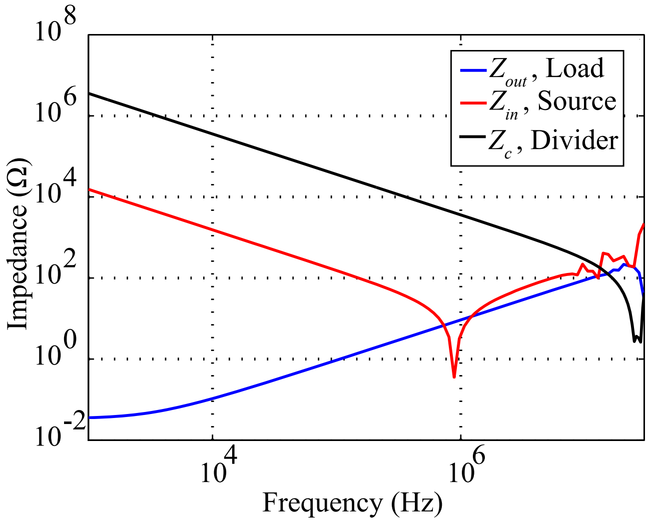

Fig. 14: Impedance curves for the source, the load (assuming a breakdown of the arc) and the divider.

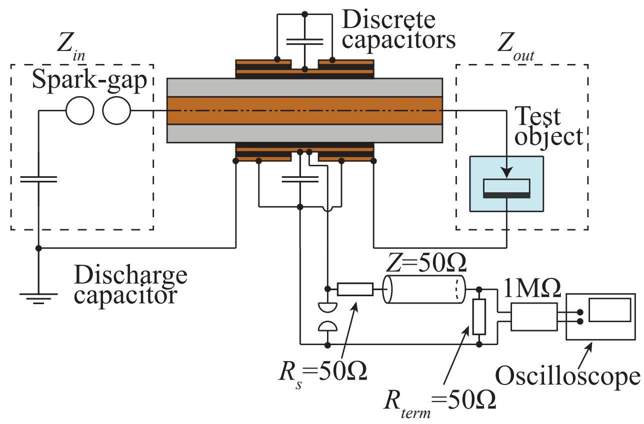

Fig. 15: Schematic of feed-through connection of the divider.

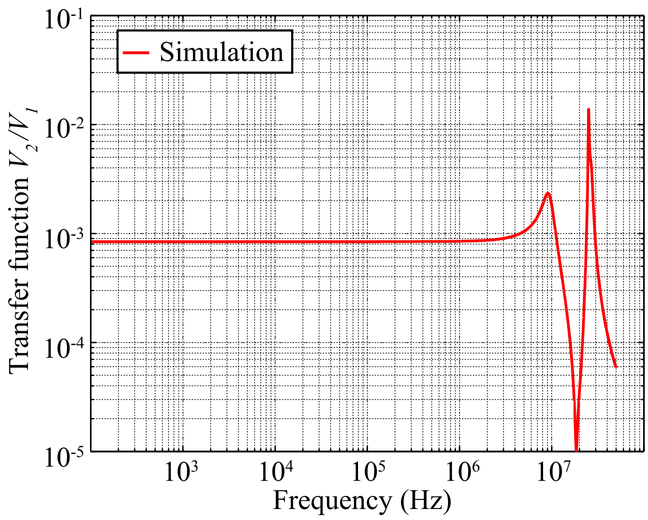

Fig. 16: Calculated transfer functions of the divider including input and output impedance.

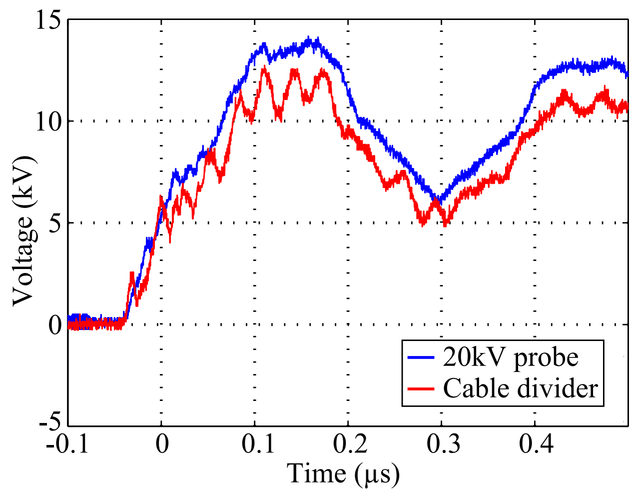

Fig. 17: Measured voltage curves while using medium voltage pulse.

pared to the case where the divider was investigated without PCD setup (Fig. 11) the resonance peak has been shifted to lower frequencies, since with the additional capacitances that have to be considered the resonance frequencies change. That emphasize the fact that for considering performance, all elements have to be involved.

For identifying the voltage divider performance, two comparisons have been performed. First, at relatively low voltages, a standard LeCroy 20 kV voltage probe was used for comparison. The result is given in Fig. 17 and it could be seen, that the coaxial divider matches the results of the LeCroy probe, except for the high frequency ringing, which is caused by the weakly damped oscillations caused by the parasitic elements of the coaxial divider. The reason for low resonance frequency comes from the relatively high C_1 value, caused by the HVDC cable itself. It could be reduced by limiting the length of the coaxial part of the cable, i.e. decrease C_1. Moreover, a major limitation is the inductance introduced by interconnecting the discrete foil capacitors. To improve the performance, concentrated capacitors near the connecting point of the BNC cable can be used. In a further step, a new divider as discussed in section IV is designed to overcome the ringing problem.

In Fig. 18 the measurement results of the coaxial divider are compared with the signal obtained with the divider

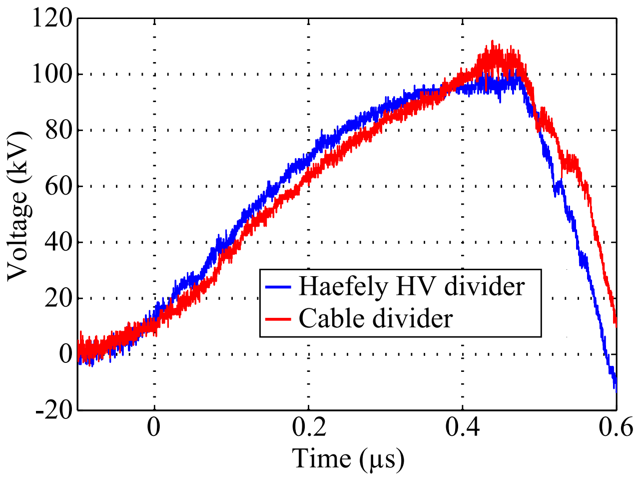

Fig. 18: Measured voltage curves while using high voltage pulse.

shown in Fig. 2. Due to the slower rise time, both dividers show well matching results.

IV. IMPROVEMENTS AND FUTURE STEPS

As discussed in the previous section, the relatively low resonance frequency of the coaxial divider results in oscillations distorting the measurement signal. The performance can be improved by reducing the capacitance value of C_1 and the parasitic inductance of C_2. The latter can be achieved by concentrating capacitors around measuring point.

Therefore, a new design has been developed as shown in Fig. 19. In this setup, the length of the interconnections has been further optimized by using SMD capacitors mounted on a PCB board in vicinity of the BNC connector. Furthermore, a shielding around the setup is used, in order to reduce the measurement noise. The new coaxial divider is based on a HV cable and has the specifications given in Table V.

V. CONCLUSION

In this paper, results for a coaxial capacitive voltage divider with a high division ratio of 1:1200 and a measurement range up to unit[200]kV are presented. The coaxial divider is based on a HVDC cable, which is used for implementing the first capacitor of the divider, and the second capacitor is realised by discrete foil capacitors.

For determining the performance of the coaxial divider and identifying the physical limits, a divider model including all the parasitics has been developed and measurements have been performed for comparing the results with other commercial dividers.

TABLE V: Specifications of the redesigned divider parameters.

Cable diameter	19.3 mm
Voltage withstand	200 kV_{dc}
Cable capacitance	0.1 pF/mm
Length of the coaxial cable (C_1)	20 mm
High voltage capacitance, C_1	2 pF
Low voltage capacitance, C_2	2 nF
Division ratio	1:1200

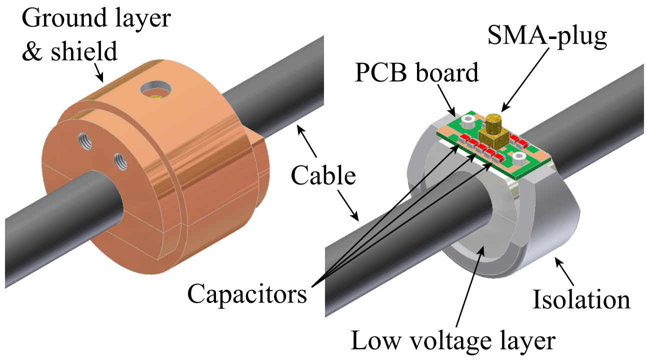

Fig. 19: Sketches of the new divider design. Left: divider with covering shield; right: supporting rings with PCB board and capacitors.

The measured results of the divider match quite well with the predictions. However, the relatively high parasitic inductance of the interconnection of the parallel connected discrete foil capacitors results in a relatively low resonance frequency of the divider and results in some ringing of the measurement signal. Therefore, a new setup is also introduced in the paper.

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