Single Plastic Optical Fiber, Multiple Channel Data Link for Sensing Applications With PCB Implemented Transmitter and Receiver

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Publication date:
2020-03

Permanent link:
https://doi.org/10.3929/ethz-b-000384824

Originally published in:
IEEE Transactions on Circuits and Systems I: Regular Papers 67(3), https://doi.org/10.1109/tcsi.2019.2956592

Single Plastic Optical Fibre, Multiple Channel Data Link for Sensing Applications with PCB Implemented Transmitter and Receiver

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***Abstract*—The limited physical bandwidth of optical data links can be utilised better using pulse amplitude modulation (PAM) schemes. PAM can also be used to implement multiple channels on a single fibre to reduce the fibre count. In this paper, PAM is used with an additional amplitude level transmitting the clock associated with the data. This allows a direct detection of the clock from the signal. Frequent returns to this additional peak level are used to determine the signal strength at the receiver. The paper presents a very compact PCB implemented transmitter achieving a data rate of up to 400 Mbps. Furthermore, three PCB implemented receiver designs that cover different speed (20-400 Mbps) and cost/complexity ranges are presented including measurement results. The proposed solutions are compared to various industry standard solutions in terms of their achievable sampling rate and measurement delay resulting from connected sensors. It is concluded that PAM based data links represent an attractive alternative to the usual time domain multiplexing based 8b/10b encoded no-return-to-zero (NRZ) data links. They lead to an increase of the possible sampling rate (278 %) of the sensor and a decrease of the measurement delay (20 %), while keeping the same signal bandwidth and number of fibres.**

***Index Terms*—Optical fibre communication, Plastic Optical Fibre (POF), Optical modulation, Pulse Amplitude Modulation (PAM), Clock Data Recovery (CDR)**

I. Introduction

PLASTIC optical fibre (POF) based communication systems are widely used to implement isolated low cost communication links. A typical area of application are medium or high voltage power electronic systems, where multiple sensor signals are collected at a central control unit. The sensors are often distributed over a range of different electric potentials such that an isolated communication medium is required. The trend towards modular converter structures results in a need for multiple channels per module/switching cell where there are typically two or more sensors per module (voltage and current). If the sensor values are used for a (closed loop) controller, the real time capability of the transmission is very important. Looking at communication networks such as IP based Ethernet or CAN, a maximum communication delay from the sensor to a central control unit cannot explicitly be guaranteed. Exceptions are e.g. EtherCAT [1], POWERLINK [2] or SyCCo-Bus [3]. However, these require expensive ICs (EtherCAT, POWERLINK) or even an FPGA/ASIC (SyCCo-Bus) plus rather expensive and sensitive single mode fibres, which is not acceptable for simple and low cost sensing applications.

Manuscript received XX YY, ZZZZ; revised XX YY, ZZZZ; accepted XX YY, ZZZZ. This research is part of the activities of the Swiss Centre for Competence in Energy Research on the Future Swiss Electrical Infrastructure (SCCER-FURIES), which is financially supported by the Swiss Innovation Agency (Innosuisse - SCCER program). All authors are with the Laboratory for High Power Electronic Systems (HPE), ETH Zürich, Zürich, Switzerland (e-mail: fuchs@hpe.ee.ethz.ch, jbiela@ethz.ch).

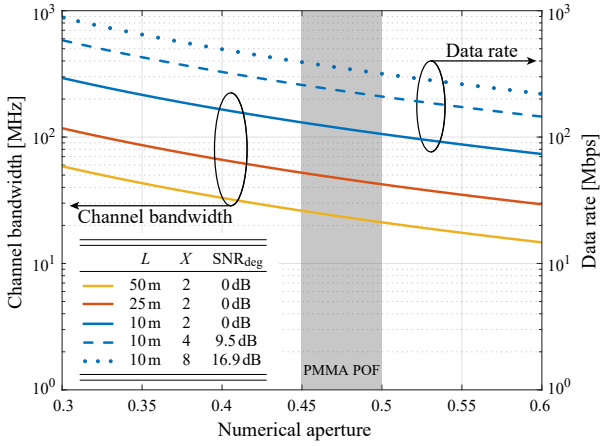

Fig. 1. Physical bandwidth limitations for step-index plastic optical fibres (SI-POF) depending on its numerical aperture [11] and the fibre lengths regarding the data rate for different numbers of amplitude levels X when using pulse amplitude modulation (PAM). The numerical aperture for typical low-cost PMMA-SI-POFs ranges from 0.45 to 0.5.

A solution that suits the cost aspects of sensing applications is presented in [4], where a low cost and low complexity data link is presented. The drawback of this implementation is its very limited data rate. The lower limit of the required data rate in closed loop controlled power electronic systems is typically proportional to their switching frequency, as a new measurement value for all sensed signals is required for each controller update. Therefore, high power density applications such as [5], [6] or high performance (pulse) converters [7] require high speed data links to the used sensors. Often, the more critical issue is the delay introduced by the data transmission. Applications such as [8] may require a relatively low data rate, but also a very low transmission delay, resulting in a high symbol rate of the data link. The same applies for any safety critical sensor.

POFs used for low cost data links are typically multimode fibres made from PMMA (plexiglass) and have a step index (SI) profile. They are simple in handling and mounting [9], [10]. As shown in Fig. 1, the bandwidth and therefore the achievable data rate of such low cost PMMA-SI-POF based

communication links is physically limited by the mode dispersion [11] of the fibre. The so called numerical aperture describes the range of incidence angles possible for a fibre. Different incidence angles result in a broadening of the light pulse while the light is travelling through the fibre. For typical step index PMMA POFs the numerical aperture is in the range of 0.45 to 0.5 resulting in a maximum bandwidth of approx. $150\,\mathrm{MHz}$ / data rate of $150\,\mathrm{MBd}$ for 10 m fibre length [11].
A way to overcome this limit is to use multiple intensity levels to transmit more than one data bit at a time. One can e.g. introduce four intensity levels to encode 2 bit of data (cf. e.g. [12]). This is called 4-PAM (4 level Pulse Amplitude Modulation). Multiple amplitude levels decrease the signal-to-noise ration (SNR) of the transmitted signal compared to only two levels by $20\log(2^2-1)$ for 4-PAM [10]. This means that using PAM results in a trade-off between SNR and data rate. Alternatively, one has to limit the length of the POF, to ensure a minimum optical power output at the receiver side, such that the amplitude of the noise can be kept small in relation to the signal. Sending more than one bit of data at a time can also be used to transmit more than one signal stream at a time and therefore implementing multiple communication channels within a single fibre.
Apart from the (serialised) data, the associated clock must also be transmitted to avoid synchronisation issues at the receiver's side. This can either be done via a dedicated fibre or with the help of clock-data-recovery (CDR) schemes. With CDR the word to be sent is typically encoded such that is has a certain number of level transitions per time. These transitions can be used to run a phase locked loop (PLL) that recovers the clock from the transmitted data. All CDR encoding schemes do not only guarantee level transitions, but also a mean value (DC) free signal. This is important when using signal transformers for galvanically isolated electrical connections, but not necessary with optical transmission systems. Besides the need for an encoding itself, another drawback of CDR schemes is that the encoding generates overhead to the word to be sent as the word is at least a few bits longer after the encoding. This decreases the data rate of the communication system. With e.g. Manchester Encoding [13], each data bit is replaced by two transmitted symbols, such that the effective data rate is reduced by 50%. For the popular 8b/10b encoding scheme (cf. [14]) $8\,\mathrm{bit}$ of (useful) data are substituted by $10\,\mathrm{bit}$ of encoded data, which corresponds to a decrease of the data rate by 20%.
[15] suggests a Manchester Encoding scheme to be used with multilevel PAM. As shown in Fig. 1, this helps to reduce the bandwidth drawback of Manchester Encoding: When using four levels with the proposed encoding, the signal bandwidth is the same as for the equivalent non-encoded two level signal. [16] presents a modulation and encoding scheme that is based on a five level PAM, where additionally to a standard 4-PAM encoding, the second symbol of two equal symbols that occur in a row is replaced by a strobe symbol (the fifth level). Therefore, each transmitted symbol causes a change in the signal, which makes is possible to directly detect the clock. However, with both [15] and [16] there is no guaranteed symbol pattern for any data input that would enable a simple signal strength detection. This means that if neither the signal strength at the receiver nor a reference bit pattern (suggested in [15]) is known to calibrate the level detection circuits of the receiver, complicated adaptive level detection implementations are necessary to demodulate the signal. If an occurrence of the strobe signal from [16] was guaranteed within a defined period, this could serve as a reference for the level detection circuits. However, this would result in a similar scheme as presented later in this paper.

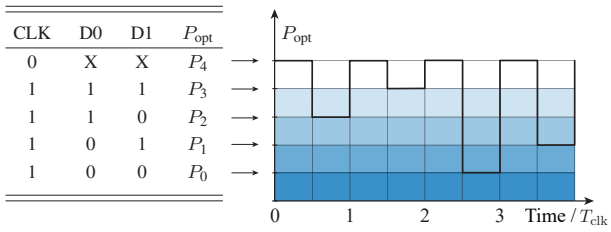

Fig. 2. 5 level Pulse Amplitude Modulation scheme with direct clock detection (5-PAM-DCD) as proposed in [17]. The fifth level is used to frequently output the maximum amplitude to generate the detection thresholds for the other levels and to transmit the clock without the need of en-/decoding as with e.g. 8b/10b encoding.

In [17] CDR is replaced by a dedicated amplitude level for the clock. Here, the highest level is transmitted every clock cycle such that a direct detection of the clock is possible without encoding and decoding the data stream itself. This level is also used to periodically detect the signal amplitude from which the detection levels of the four other amplitude levels can be derived, as will be explained later.
In this paper, the concept from [17] is used to implement short distance (ca. $1-20\,\mathrm{m}$), POF based data transmission systems for different data rates. In detail, the paper contributes the following:

- After a short recapitulation of the Pulse Amplitude Modulation with direct clock detection (PAM-DCD) from [17] the analogue circuity required to implement the PAM-DCD in hardware is shown in section II. Besides this, the bandwidth requirements for the optical transmission are explained.
- The implementation of a very simple and compact five level transmitter, integrating the encoding needed for the modulation proposed in [17] is presented and validated by measurements of the optical output power (section III).
- Three receiver designs for different data rates are proposed in section V.
  1) A low complexity/low number of parts and highly flexible low speed implementation ($20\,\mathrm{Mbps}$).
  2) A medium range implementation ($50\,\mathrm{Mbps}$) resulting in a good cost vs. speed trade-off.
  3) A high performance implementation ($200\,\mathrm{Mbps}$) reaching for the maximum performance of the proposed concept possible with currently available components.

  All designs are based on standard available ICs/parts and implemented on a PCB. Detailed validating measurements and the Bit Error Rate (BER) for all three

design proposals are presented.

- A modulation variant exploiting the channel bandwidth with a few modifications to the PAM-DCD scheme and therefore increasing the possible data rate by a factor of two is shown in section VI. Experimental results for the medium range implementation are presented in order to prove the concept.
- The presented designs are compared to industry standard implementations of unidirectional communication schemes transmitting multiple channels and their clock signal in terms of the transmission delay and possible data rate/throughput defining the possible sampling rate of in a sensing application (section VII). Also the principle proposed in [16] is included.

The findings are concluded in section VIII.

II. Pulse Amplitude Modulation with direct clock detection (PAM-DCD)

The modulation scheme used in this paper was introduced in [17]. It is based on the principle of pulse amplitude modulation, where several digital amplitude levels are used to transmit M (two or more) data bits with a single symbol. For 2 data bits, this can be realised as shown in Fig. 2 when ignoring the CLK column in the table (cf. [12], chp. A.3). As derived e.g. in [12] (chp. A), 2^M-PAM reduces the necessary bandwidth of the signal per transmitted data bit. The data rate is M times higher than with two levels only, while keeping the signal bandwidth constant. Therefore, e.g. 4-PAM requires only half of the bandwidth per data bit compared to a standard no-return-to-zero (NRZ) signal.

In [17] it is proposed, to also transmit the clock of the two symbols by using a dedicated amplitude level which is triggered every cycle, such that the clock can directly be recovered. In the following, this concept is called (2^M+1)-level Pulse Amplitude Modulation (PAM) with direct clock detection (DCD) within this paper. The principle is shown in Fig. 2, for $M = 2$.

The frequent return to the maximum level guarantees a good tracking of the signal peak level which may change over time, due to fibre bending, temperature drifts, wavelength drifts, ageing and other effects that change the damping coefficient of the POF and/or the photo diode characteristics (cf. [11]). This peak detection is necessary to derive the detection levels for the other signal levels such that the signal can be demodulated at the receiver side (cf. Sec. IV).

On the other hand, the return to the peak level in each clock cycle requires a high bandwidth of both transmitter and receiver, as the effective signal bandwidth is twice as high as without the return to the peak level. However, for the implementations presented in this paper with $M = 2$ (5-PAM-DCD), the required bandwidth is the same as for an NRZ signal carrying the same amount of data, but no clock (assuming time domain multiplexing on a single fibre). If information on the clock is added to the NRZ signal by e.g. 8b/10b encoding [14], 5-PAM-DCD requires a lower bandwidth for the same effective data rate. This is shown in greater detail in Sec. VII.

III. Transmitter Circuit Design And Measurement Results

This section describes the circuit design of a two channel/five level transmitter and presents measurement results for the optical output of the photo diode. A principle circuit implementation is shown in Fig. 3. The optical output power levels are realised by discrete LED current levels. A showcase LED - photo diode (PD) combination is shown in Fig. 4.

In the simplest case, the channel impedances Z_0, Z_1 and Z_2 are purely resistive (no peaking capacitor C_p) with $Z_0 = R$ and $Z_1 = Z_2 = 2R$. In this case, the LED current levels are equally spaced. However, due to the non-linearities in the LED - PD combination, the resulting output current of the photo diode I_out, would not be ideally spaced and this would lead to non-optimally spaced voltage amplitudes, as indicated in Fig. 4. Therefore, the sum of the channel resistors R_p and R_s of Fig. 3 needs to be properly adjusted according to the characteristics of the optical transmitter-receiver combination. The quiescent LED current that helps to increase the possible bandwidth [18] also needs to be considered here. A rule of thumb suggests assigning 2/3 of the channel resistance to R_p and 1/3 to R_s [18].

After choosing the values of the resistors, the so called peaking capacitor values C_p need to be selected, in order to form a current peaking stage that enables faster rise/fall times. In general, a higher capacitance leads to faster rise and fall times, due to the higher overshoot of the current. However, a high capacitance value leads also to increased oscillations during the transmission and eventually degrades the signal quality at the receiver's end. In the end, a compromise between fast rise/fall times and signal quality has to be made as shown in the following:

Fig. 5 shows the measured output voltage of the receiver/TIA for two different POF lengths ($1\,\mathrm{m}$ and $10\,\mathrm{m}$) and two different transmission clock frequencies ($50\,\mathrm{MHz}$ and $100\,\mathrm{MHz}$), obtained with the use of the same exemplary peaking capacitor C_p. For $10\,\mathrm{m}$ POF and $100\,\mathrm{MHz}$ (right side of Fig. 5), it results in a satisfactory TIA output voltage waveform. The reduced transmission speed of $50\,\mathrm{MHz}$ for the same length results in a small but acceptable overshoot as shown in the $1\,\mathrm{m}$-$50\,\mathrm{MHz}$ case. The left part of Fig. 5 shows the result for $1\,\mathrm{m}$ POF length. The attenuation of the fibre is obviously lower and the output voltage is significantly higher. For the $200\,\mathrm{Mbps}$ case, the results are satisfactory. However, the need to tune the capacitor value is especially pronounced in the $100\,\mathrm{Mbps}$ case, where a relatively high overshoot of the output voltage occurs. For this case, a smaller capacitance value should be chosen.

Based on performed measurements, the highest value of C_p that does not lead to an unacceptable overshoot at the receiver's end, for a given transmission clock/data rate is chosen. Note that the level spacing when comparing the waveforms in Fig. 5 for the $200\,\mathrm{Mbps}$ cases scale approx. linearly with the POF length. This means that their spacing relatively to the peak voltage is the same. Therefore, the peaking capacitors can be used as a very simple equaliser for a given transmission clock.

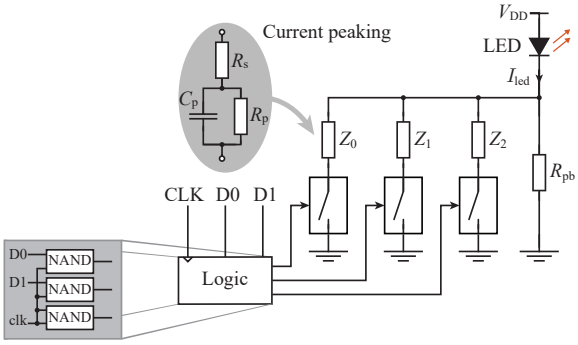

Fig. 3. 5-PAM-DCD transmitter circuit.

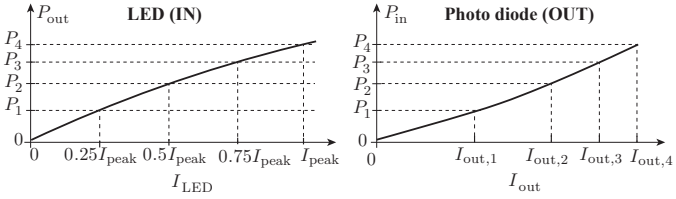

Fig. 4. Showcase combination of LED and photo diode. Bias current is neglected for simplicity.

To decouple the experimental findings of the transmitter and the receiver circuits, an optical probe has been used to measure the optical output power of the transmitter LED. The eye-diagrams for 50 MBd and 100 MBd transmission speed are presented in Fig. 6(b) and (c). The attenuation of a longer POF plus the receiver circuit (photo diode and TIA) will absorb most of the overshoots (cf. Fig. 9). In Fig. 6(a), a picture of the transmitter board is shown. The used LED, ICs, resistor and capacitor values are noted in Tab. I.

IV. Receiver Principle

The receiver for the PAM-DCD principle is shown in Fig. 7. Experimental waveforms are shown in Fig. 8 accordingly. A photo diode (PD) converts the incoming light signal into a current. This current is converted to a voltage signal with a transimpedance amplifier (TIA). Note that the signal amplitude is not necessarily constant over time, as mentioned in Sec. II. The detection threshold levels for the level detection are also derived from the peak detector output. The power levels used for the PAM correspond to a certain percentage of the

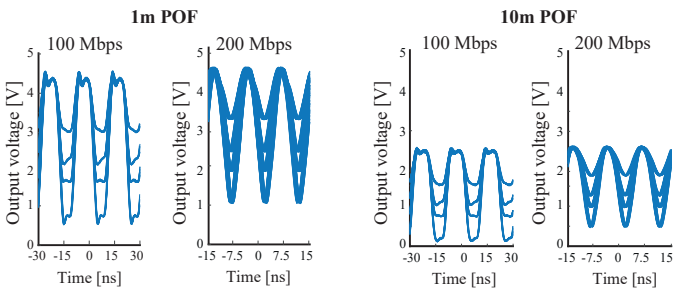

Fig. 5. Experimental eye-diagrams of the TIA output voltage for different fibre lengths and different transmission frequencies, for a given peaking capacitor C_p tuned for the 100 Mbd/200 Mbps transmission speed.

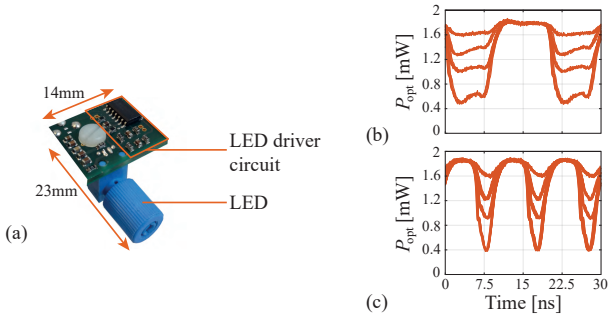

Fig. 6. (a) Picture of transmitter PCB including dimensions. Eye-diagrams from measurements of the LED optical output after 1 m POF at a transmission speed of (b) 50 MBd/100 Mbps and (c) 100 MBd/200 Mbps, Parts and values are given in Tab. I.

TABLE I
Transmitter Parts and Data (Fig. 3)

Part		Value/Part Number
LED		IF-E99B
Z_0	R_s	82 Ω
	R_p	165 Ω
	C_p	15 pF ($f_{TX} > 50$ MHz) 6.8 pF ($f_{TX} \leq 50$ MHz)
Z_1	R_s	166 Ω
	R_p	333 Ω
	C_p	15 pF ($f_{TX} > 50$ MHz) 6.8 pF ($f_{TX} \leq 50$ MHz)

Part		Value/Part Number
Switches & NAND		Avago SN75451BD [18]
$Z2$	R_s	168 Ω
	R_p	336 Ω
	C_p	15 pF ($f_{TX} > 50$ MHz) 6.8 pF ($f_{TX} \leq 50$ MHz)
R_{pb}		137 Ω
V_{DD}		5 V

peak power level (Fig. 2) and therefore also to the peak TIA output voltage as was shown in the previous section. In this paper, two peak and level detection hardware implementation variants are used.

1) The TIA output voltage is directly sampled by an analogue to digital converter (ADC, Fig. 12). The peak detection, the level detection and the signal reconstruction is digitally implemented in a CPLD or a DSP. This variant is used for the 'Low Complexity Realisation' introduced in Sec. V-A.
2) The output voltage of an analogue peak detector serves as a reference for a set of comparators that detect if the TIA output voltage is below this reference as shown in Fig. 12(b). The original digital signal can be reconstructed with some simple logic from the outputs of the comparators. This variant is used for the 'Medium Range' (Sec. V-B) and the 'High Speed Realisation' (Sec. V-C) in this paper.

The clock recovery is performed by comparing a certain percentage of the peak detector output to the TIA output. If the TIA output is higher, this denotes a rising edge of the clock. The output of the level detection must be sampled with some delay to the detected clock edge (sample trigger signal in Fig. 8). After correctly detecting the signal level, the truth table given in Fig. 2 can be used to reconstruct the original data signals. This is done by the 'Logic' block in Fig. 7. The output of this block is identical with the serial data provided to the transmitter and can be deserialised by any shift register.

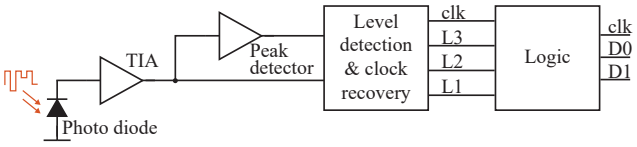

Fig. 7. Principle PAM-DCD receiver parts.

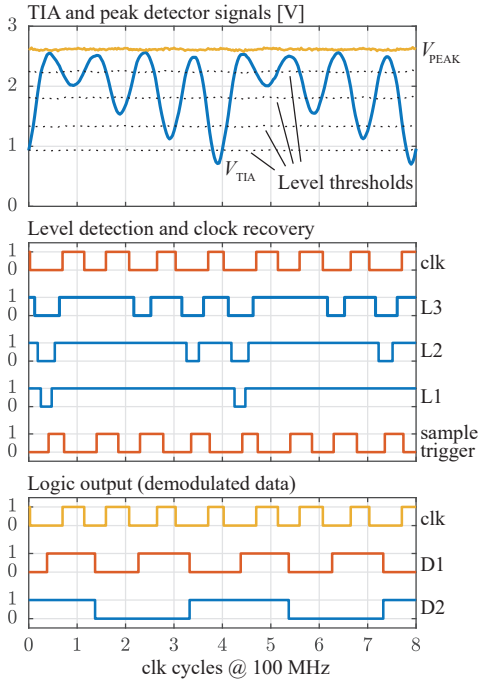

Fig. 8. Measurement results for the 'High Speed Realisation' presented in Sec. V-C. with 10 m POF. Note that there is a delay (4 ns or approx. half a clk cycle) between the actual events (e.g. V_{TIA} higher than threshold) and the according comparator outputs due to the rise time of the comparator outputs.

V. Receiver Circuit Design And Measurement Results

In this section, three circuit designs, PCB realisations and measurement results are presented. The design procedure for the two slower realisations (Sec. V-A and V-B) is not based on a specific data-rate requirement. It rather follows a cost orientated approach: First, the general layout as well as the parts that mainly contribute to the system cost (Operational Amplifiers, Comparators/ADC) are selected. The rest of the circuity (mainly passives) is designed to achieve the highest possible bandwidth with the given topology and parts. For the high speed realisation (V-C), a design procedure based on a topology and a bandwidth criterion is presented.

A. Low Complexity Realisation (20 Mbps)

This realisation features a low number of parts and high flexibility concerning the number of detectable levels. To account for a low component cost its transmission speed is limited to approx. 10 MBd symbol rate. It consists of the TIA circuit shown in Fig. 9(a) and an ADC with e.g. a CPLD (Fig. 12(a)) to digitally implement the peak-/level-detection, the clock recovery and the decoding.

An active TIA (Fig. 9(a)) is used to decouple the signal swing from the relatively large photo diode capacitance in order to achieve a high-speed current to voltage conversion. In this realisation, the OP-Amp is selected based on cost criteria and the peripheral components are chosen to optimize the performance. The shown TIA has a second order response behaviour. Its gain is set by the feedback resistance $R_{f,1}$ (cf. [19], chp. 2). The value of $R_{f,1}$ is chosen so that OP1 generates the largest possible voltage swing $V_{OP,max}$ for the maximum expected photocurrent $I_{ph,max}$. According to [11], the maximum photocurrent can be estimated with the known optical output power of the transmitter P_{opt}, the minimum used POF length L_{min}, the wavelength-dependant attenuation coefficient α_λ of the POF and the wavelength-dependant responsivity R_λ of the PD such that the feedback resistance is given as

$$R_{f,1} = \frac{V_{OP,max}}{I_{ph,max}} = \frac{V_{OP,max}}{R_\lambda P_{opt} \exp(-\alpha_\lambda L_{min})}. \quad (1)$$

In order to ensure stability, the feedback capacitance $C_{f,1}$ is added to introduce a zero in the feedback factor. This is done to compensate the phase shift of the loop gain caused by the relatively large capacitance of the PD at the input and the dominant pole of OP1. However, this compensation is done at the expense of TIA bandwidth, therefore the dimensioning of $C_{f,1}$ is critical in wideband applications (cf. [19]–[21]). According to [19] chp. 3, the zero should be placed at the intersection point of the open loop gain of OP1 with the inverse feedback factor for optimal phase compensation. This yields to

$$C_{f.1} = \frac{1}{4\pi R_{f.1} f_{gbw}} \left(1 + \sqrt{1 + 8\pi R_{f.1} C_{in} f_{gbw}}\right), \quad (2)$$

with the gain-bandwidth product f_{gbw} of OP1 and the effective capacitance C_{in} at the input of OP1. C_{in} is mainly determined by the PD junction capacitance C_d but also the parasitic capacitance from the PCB tracks as well as the input capacitance of OP1 should be considered. Any capacitance at the output of OP1, e.g. from the input stage of a following Op-Amp, generates an additional pole with the output resistance of the OP1 (cf. [22]). A small resistor R_{iso} is placed close to the output of OP1 to isolate capacitive loads from the feedback loop. However, there is still some parasitic capacitance from the pad and the PCB tracks of the feedback connection directly at the output which cannot be isolated. To maintain stability, the zero in the feedback factor has to be placed at a lower frequency which requires a larger $C_{f,1}$. Therefore, (2) can be seen as a theoretical lower limit. The circuit can be optimised empirically by using a $C_{f,1}$ twice as large as obtained by (2). Subsequently, the value can be decreased until the circuit becomes unstable or a large overshoot is present on the output signal.

At high frequencies, the open-loop gain of OP1 declines and the voltage at the photo diode's cathode is not kept constant any more. Thus, C_d starts to draw some photocurrent. To avoid this, a JFET (T1) in source follower/common-drain configuration is used to realise a unity gain feedback loop

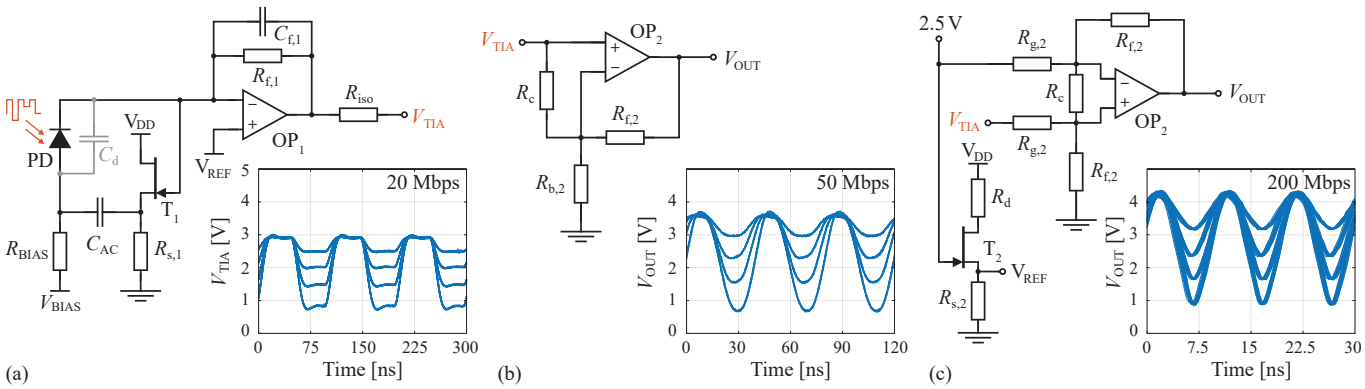

Fig. 9. TIA circuits and measurement results (eye diagrams) for the different receiver variants using the proposed transmitter and a 1 m POF. (a) Low Complexity, (b) Medium Range, (c) High Speed Realisation. The circuit shown in the very left (a) is used to generate V_{TIA} in (b) and (c). Parts and values are given in Tab. II.

(cf. [23], chp. 8.11), such that the changing voltage potential at the photo diode's cathode is also transferred to the anode (bootstrapping). This increases the possible bandwidth of the TIA while the noise is decreased, as the effective input capacitance of OP1 is reduced (C_{d} is greatly reduced, OP1 sees mainly the gate-drain capacitance of T1 (better C_{rss}, cf. [24], chp. 6.3). If bootstrapping is used, the decrease in capacitance should be taken into account in (2). To maximise the benefit from the bootstrapping circuit, a JFET with a particularly low noise figure and a low gate-drain capacitance should be chosen. The AC coupling to the photo diode's anode (with C_{AC} in Fig. 9(a)) allows the photo diode to be pre biased independently of the bootstrapping circuit. The chosen value for C_{AC} is not critical, however the series resonance frequency of the selected capacitor should be bigger than the used transmission clock frequency. The source resistance $R_{\mathrm{s,1}}$ is chosen such that the maximum rated drain-source current of T1 is not exceeded.

Finally, the resulting bandwidth of the TIA can be estimated with (cf. [19], chp. 3)

$$f_{\mathrm{3dB}} = \sqrt{\frac{f_{\mathrm{gbw}}}{2\pi R_{\mathrm{f,1}}(C_{\mathrm{f,1}} + C_{\mathrm{in}})}} \quad . \tag{3}$$

The measured eye-diagram of the TIA for a data rate of 20 Mbps is shown in Fig. 9(a). The exact part specifications are given in Tab. II.

The ADC used to digitize the TIA voltage must have a sufficiently high sampling rate. In order to sample the correct peak value as well as signal level, the ADC sampling interval T_{ADC} needs to satisfy the condition

$$T_{\mathrm{ADC}} < \frac{T_{\mathrm{TX}}}{2} - t_{\mathrm{r}} \quad , \tag{4}$$

with the transmission clock interval T_{TX} and the TIA rise time t_{r}. This relationship is illustrated in Fig. 11. According to [25], the rise time of a signal can be calculated using (3) as $t_{\mathrm{r}} = {}^{0.35}/_{f_{\mathrm{3dB}}}$. This realisation uses a digital peak detector which is implemented in the CPLD/FPGA. It stores the largest value of the ADC output in a register and updates it whenever a new maximum value is detected. In order to react on changes in the signal strength caused by e.g. bending of the POF, the stored peak value is decremented at each system clock cycle. Furthermore, a trigger signal is generated whenever the stored peak value is updated. This signal is delayed and used to synchronise the level detection stage due to the asynchronous transmission clock. The thresholds for the level detection are derived dynamically from the peak value.

TABLE II
TIA PARTS AND DATA (FIG. 9)

	Low compl. (a)	Med. range (a+b)	High Speed (a+c)
PD		SFH250V	
V_{BIAS}	−12 V	−12 V	−25 V
R_{BIAS}	10 Ω	10 Ω	47 Ω
V_{REF}	100 mV	100 mV	2.3 V
V_{DD}	3.3 V	6 V	5 V
$R_{\mathrm{s,1}}$	100 Ω	470 Ω	1 kΩ
C_{AC}		100 nF	
T1/T2		CPH3910	
OP_1	LT6200-10	LT6200-10	OPA858
$R_{\mathrm{f,a}}$	5.6 kΩ	1.5 kΩ	2.7 kΩ
$C_{\mathrm{f,a}}$	1.5 pF	3.3 pF	0.5 pF
R_{iso}	10 Ω	10 Ω	
OP_2		LT6200-10	LT6268-10
$R_{\mathrm{g,2}}$			100 Ω
$R_{\mathrm{f,2}}$		360 Ω	340 Ω
$R_{\mathrm{b,2}}$		120 Ω or 60 Ω	
R_{c}		91 Ω	50 Ω
R_{d}			620 kΩ
$R_{\mathrm{s,2}}$			560 kΩ

A picture of the PCB is shown in Fig. 10(a). The PCB footprint and the component count are very small compared to the other realisations. There were no bit errors found after running the system for 16 hours with a 10 m POF. This corresponds to a Bit Error Rate (BER) of less than $8.68{\cdot}10^{-13}$. With the ADC, many more than the proposed 5 levels can be distinguished if the fibre is not too long. Thus, for short POFs, very high data rates could be realised with this receiver implementation even though the symbol rate is not increased. The CPLD that has been used to implement the digital peak

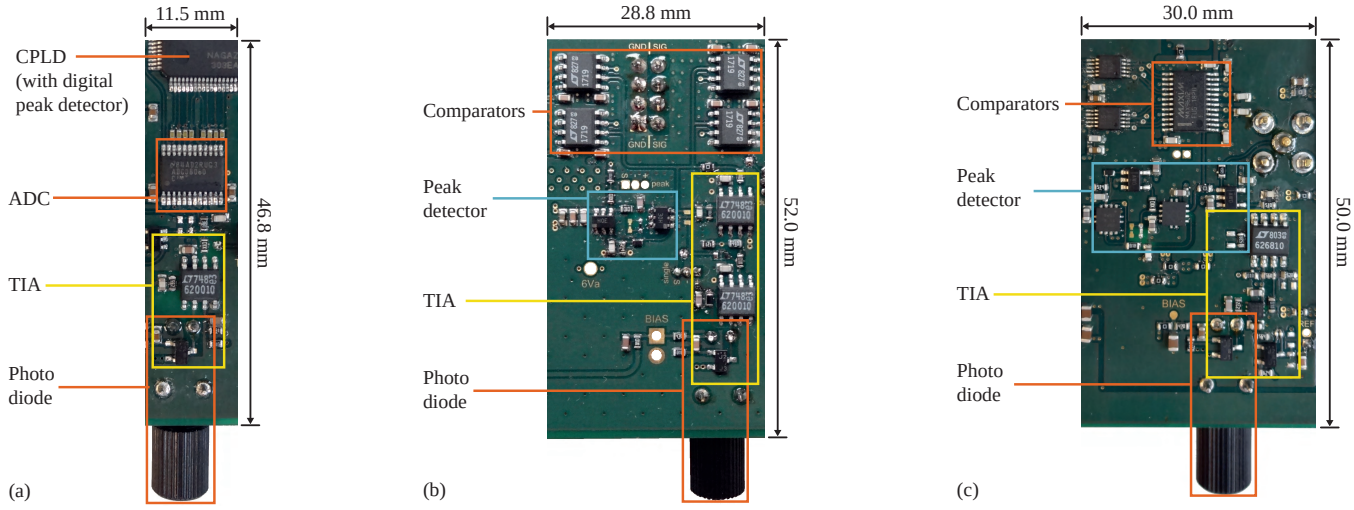

Fig. 10. Pictures of the three presented receiver PCBs. (a) Low complexity, (b) Medium range and (c) High speed realisation.

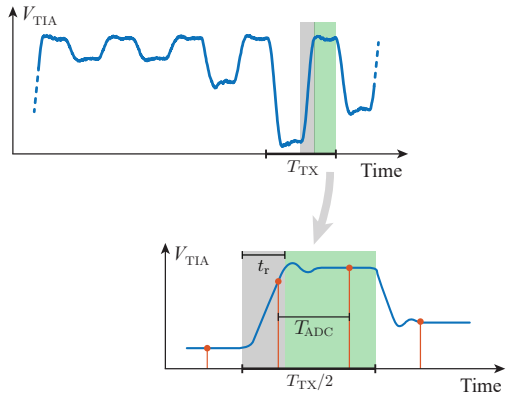

Fig. 11. Required ADC sampling rate to correctly acquire the level of the TIA output signal.

and level detection (Intel MAX 10M02SCE144) can be used for at least 4 more receivers on the same PCB.

B. Medium Range Realisation (50 Mbps)

The realisation presented in the following uses a two stage concept with the previously presented TIA connected to a voltage amplifier. The peak- and level-detection are implemented with analogue circuits. It achieves a symbol rate of 25 MBd. The voltage amplifier is shown in Fig. 9(b). It is directly connected to the output of the first stage as denoted by V_{TIA} in the figure.

The second amplifier stage makes it possible to distribute the necessary gain on the two stages. Therefore, looking at (3), the feedback resistance $R_{\mathrm{f,1}}$ in the first stage can be chosen lower, while the feedback capacitance $C_{\mathrm{f,1}}$ can be increased without losing bandwidth (cf. also [21]). This simplifies the PCB design, because parasitic capacitance values can be higher without becoming dominant and the exact knowledge of e.g. C_{d} is not required any more. The resistor values of $R_{\mathrm{f,2}}$ and $R_{\mathrm{b,2}}$ are chosen such that the lower amplification of the TIA is compensated by the gain of the second stage $A_{\mathrm{v,2}} = {}^{R_{\mathrm{f,2}}}/_{R_{\mathrm{b,2}}} + 1$. Note that decompensated Op-Amps are used in this implementation. Due to the limited output swing, OP2 is operated below its minimal required gain A_{min} which leads to instability. However, it is possible to regain stability without changing $A_{\mathrm{v,2}}$ by introducing a resistance $R_{\mathrm{c,2}}$ between the input ports of OP2 [26]. The circuit is stable if the condition

$$A_{\mathrm{min}} \leq 1 + \frac{R_{\mathrm{f,2}}}{R_{\mathrm{b,2}}} + \frac{R_{\mathrm{f,2}}}{R_{\mathrm{c,2}}}\,, \tag{5}$$

is fulfilled.

Usually, the bandwidth of the two stage topology is limited by the first stage due to the relatively large capacitance at the input. Moving more and more gain to the second stage seems to be the logical conclusion to achieve a higher bandwidth. However, the minimal required gain of the used decompensated Op-Amp puts also a restriction on the choice of the TIA feedback capacitance. As shown in [27], at high frequencies the closed loop gain of the TIA is purely determined by the capacitances and still needs to be bigger than A_{min} according to

$$A_{\mathrm{min}} \leq 1 + \frac{C_{\mathrm{in}}}{C_{\mathrm{f,1}}}\,. \tag{6}$$

From this equation an upper limit for $C_{\mathrm{f,1}}$ can be derived. Consequently, the maximum possible value for $C_{\mathrm{f,1}}$ also defines the minimum required $R_{\mathrm{f,1}}$ as shown by (2). Therefore, the first stage cannot be operated at an arbitrary low gain to increase the bandwidth. From a noise perspective, it is also beneficial to operate the first stage at higher gain [28].

The part specifications are summarised in Tab. II. An eye-diagram of the TIA plus the voltage amplifier for a data rate of 50 Mbps is shown in Fig. 9(b). The maximum achievable bandwidth is limited by saturation effects of OP1 because the signal is close to the lower rail. The transient response can be improved by increasing V_{REF}. However, this generates a DC offset which is amplified by the second stage and limits the signal swing at the output. Therefore, a rather small V_{REF} is chosen. Another approach is to use a bipolar supply for the

TABLE III
LEVEL DETECTION PARTS AND DATA (FIG. 12)

	Medium Range	High Speed		Medium Range	High Speed
CP1	LT1719	MAX9602	R_2	$1010\,\Omega$	$457\,\Omega$
R_0	$830\,\Omega$	$360\,\Omega$	R_3	$960\,\Omega$	$385\,\Omega$
R_1	$855\,\Omega$	$417\,\Omega$	R_4	$2075\,\Omega$	$900\,\Omega$

Op-Amps but this is not used in this realisation due to the cost oriented design.

For the level detection circuit (Fig. 12(b)), an analogue **peak detector** is required. Its design is described in the following: The circuit is given in Fig. 13, where the basic principle is proposed in [23] (chp. 4.5.1). In the concept shown in this paper, a 'bleeding resistor' R_b is added to react on temporary changes of the signal peak value due to temperature drifts or mechanical movement/bending of the POF. The capacitor C_s is discharged with the time constant $R_\mathrm{b}C_\mathrm{s}$. The time constant should be chosen much larger than the symbol period to prevent a substantial discharge between two consecutive symbols which would result in an incorrect reference voltage. In general, a trade-off between fast adoption to new (lower) signal amplitudes and precision has to be found. For both D1 and D2 high-speed Schottky diodes with a low forward voltage drop should be used. D2 prevents OP1 to saturate at the negative rail if the input voltage V_TIA is lower than V_PEAK. Even though, the output signal of the peak detector is most likely a DC voltage, both Op-Amps OP1 and OP2 require a high slew rate/bandwidth to react on the fast changing input signal. OP1 should have a low input capacitance and the capability of driving large capacitors. The additional external capacitance C_a provides the possibility to vary the overshoot of OP1 in order to tune the peak detector for very different POF lengths. OP2 should have a low input bias current I_ib, to meet the requirements for the lowest detectable peak voltage given by $R_\mathrm{b}I_\mathrm{ib}$. The exact parameters for the peak detector are summarised in Table IV. The current buffer (CB) is only used with the high-speed realisation.

The rest of the **level detection** (Fig. 12(b)) consists of a voltage divider with four outputs to generate the reference voltages for the comparators. The individual resistor values are derived from the level spacing generated by the transmitter (cf. Sec. III). The parts used in this paper are given in Tab. III.

A picture of the PCB of the medium range realisation is shown in Fig. 10(b). Due to the second amplifier stage, the analogue peak detector and the discrete comparators, the PCB footprint is significantly larger than for the low complexity realisation. The achievable data rate is however more than sufficient for most sensing applications. The Bit Error Rate (BER) was found to be $3.086 \cdot 10^{-13}$ after 18 hours with a $10\,\mathrm{m}$ POF. This corresponds to a single bit error over the testing time.

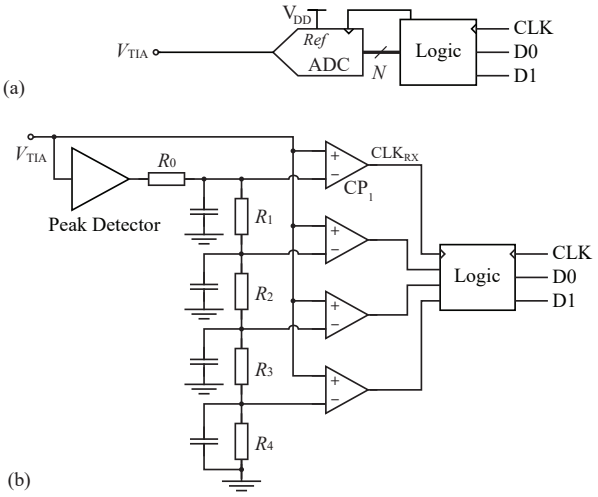

Fig. 12. Level detection circuits. (a) ADC based realisation for the low speed implementation. (b) Comparator based realisation for the medium and high speed implementation. Parts and values are given in Tab. III.

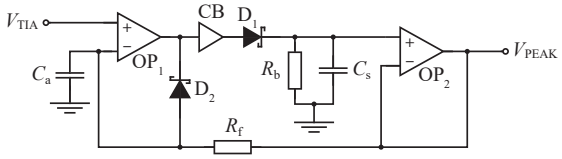

Fig. 13. Peak detector circuit. Parts and values are given in Tab. IV.

C. High Speed Realisation (200 Mbps)

This design is proposed to determine the limits of the implementation using industry standard components only. In the following, a design procedure is given for the receiver design starting from a data rate/bandwidth requirement. The high-speed realisation is designed to support a data rate of $200\,\mathrm{Mbps}$ which translates to a required bandwidth of $100\,\mathrm{MHz}$.

First, a suitable Op-Amp OP1 for the TIA should be selected. According to (3) it should feature a low input capacitance and a high gain-bandwidth product. With the input capacitance of the Op-Amp, the total capacitance at the inverting input can be estimated. This capacitance also includes the parasitic capacitance of the PCB layout. A lower bound for $R_{\mathrm{f},1}$ can be derived from (6) as shown in the medium range realisation. An upper bound for $R_{\mathrm{f},1}$ is determined by substituting $C_{\mathrm{f},1}$ in (3) with (2) and solving for $R_{\mathrm{f},1}$ with the required bandwidth. This results in a range for the TIA gain in which the circuit is stable. A value close to the lower limit of this range should be chosen to include some margin for the bandwidth. The remaining

TABLE IV
PEAK DETECTION PARTS AND DATA (FIG. 13)

	Medium Range	High Speed		Medium Range	High Speed
OP	AD8061	OPA659	C_a	1.2 pF	2.2 pF
CB		BUF602	C_s	330 pF	180 pF
D_1	BAS 40-02L E6327		R_b	270 kΩ	510 kΩ
D_2	DB2L33500L1		R_f	100 kΩ	1 kΩ

components of the TIA can be determined as described in the previous realisations.

Just like with the medium range realisation, the TIA is followed by a second voltage amplification stage as shown in Fig. 9(c). Here, a pseudo-differential structure is used: The TIA in the first stage is pre biased with a reference voltage to avoid saturation effects when V_{TIA} comes close to the lower supply voltage of OP1. This pre bias voltage is removed in the second stage. The reference voltage for the second stage is fixed to $2.5\,\mathrm{V}$, while the reference voltage for the first stage (V_{REF} in Fig. 9(a)) is decreased by approx. $200\,\mathrm{mV}$ to reduce the DC offset from the signal caused by the LED pre bias current on the transceiver side. This is achieved with a (low noise) common-drain amplifier. A bypass capacitor is added close to the non-inverting input pin of OP1 which is not shown in Fig. 9. Due to the lower reference voltage of the first stage the gain of the second stage can be increased. It is given by $A_{\mathrm{v},2} = {}^{R_{\mathrm{f},2}}/_{R_{\mathrm{g},2}}$.

A disadvantage of this concept is its comparably high component count and the necessity for low tolerance resistors in the voltage amplifier. The eye-diagram of the TIA plus the voltage amplifier for a data rate of $200\,\mathrm{Mbps}$ is shown in Fig. 9(c). Exact part specifications are given in Table II. The peak detector and the level detection are realized in the same manner as for the medium range realisation with the parts given in Table IV and Table III.

A picture of the hardware implementation is shown in Fig. 10(c). The PCB footprint is not much larger compared to the medium range version. Nevertheless, the component pricing is comparably high and many supply voltages have to be generated, as a result, making the implementation effort much higher than for the medium range version. However, the achievable communication bandwidth is very high.

The Bit Error Rate (BER) was found to be $2.778 \cdot 10^{-12}$ (corresponds to 36 bit errors) after a runtime of 18 hours with a $10\,\mathrm{m}$ POF.

VI. Two Symbol Header (2SH)

As explained in Sec. II, the frequent return to the max. level for clock transmission causes the signal bandwidth to double. Instead of returning to the peak level for every transmitted symbol, the peak level is now only used once every N symbols. Apart from the resulting lower signal bandwidth, this procedure has the second benefit that the peak level can be used to trigger the beginning of a data word. This means it is used as a header.

For short data words (in measurement systems typically 8 to $16\,\mathrm{bit}$) the pauses between the max. level transmissions are still short enough to implement a reliable peak detector/level detection and the frequency of the directly detected clock is still high enough to feed available PLLs. The PLL is used to multiply the detected clock frequency to match with the actual clock frequency of the data (structure shown in Fig. 14(d)). To reduce jitter in the directly detected clock, a second header symbol is introduced ahead of the maximum level symbol to make the waveform of the header independent of previously transmitted data word. Therefore, this technique is called Two Symbol Header (2SH). The resulting effective data rate using the 2SH is

$$DR = \frac{N}{N+2} \cdot \frac{M}{T_{\mathrm{clk}}}, \tag{7}$$

where N is the word length, M is the number of bits per symbol and $1/T_{\mathrm{clk}}$ is the symbol rate.

In Fig. 14(a) and (b) the 2SH scheme is presented graphically in comparison with the frequent return to the max. level from [17]. Fig. 14(c) shows the measurement results for the medium speed receiver presented in Sec. V-B with 8 data symbols, $10\,\mathrm{m}$ POF and $50\,\mathrm{MBd}$ symbol rate. This means an effective data rate of $80\,\mathrm{Mbps}$. The Bit Error Rate (BER) was found to be $5.82 \cdot 10^{-12}$ (corresponds to 44 bit errors) after a runtime of $21\,\mathrm{h}$. The word length is limited by the minimum input frequency of the PLL used for clock multiplying (e.g. $5\,\mathrm{MHz}$ with Altera Cyclone V FPGAs). Many low cost CPLDs feature integrated PLLs (such as e.g. Intel's MAX10) and there

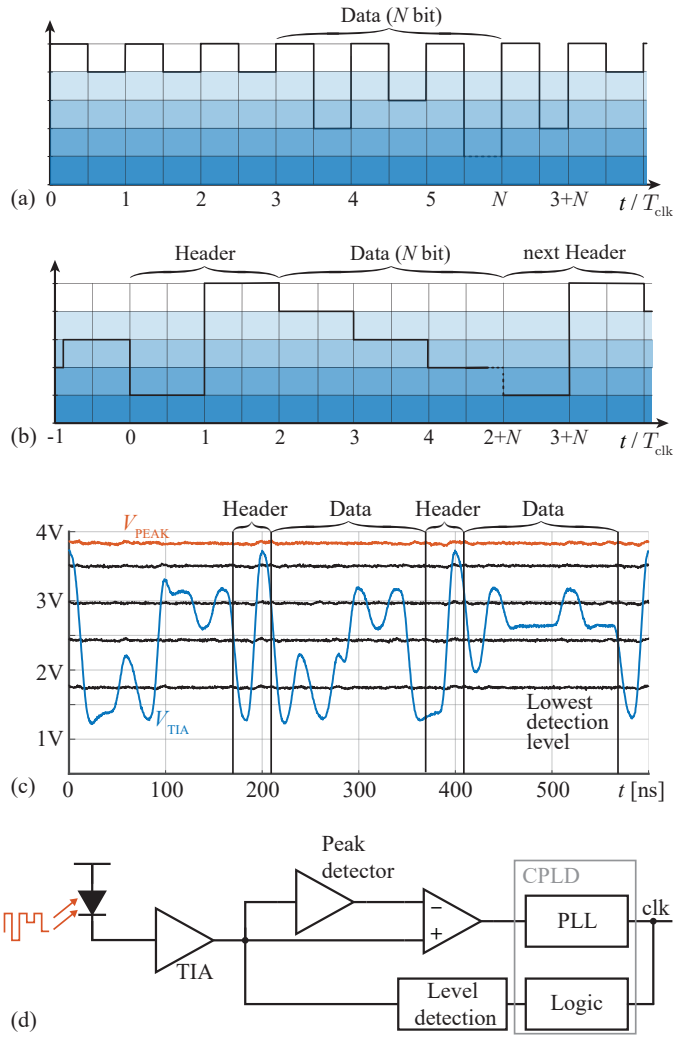

Fig. 14. Two Symbol Header (2SH): Comparison of the modulation proposed in [17] (a) and the Two Symbol Header (2SH) scheme introduced in this paper (b). (c) Experimental waveforms of the TIA output for the medium speed receiver presented in Sec. V-B with 8 data symbols, $10\,\mathrm{m}$ POF and $50\,\mathrm{MBd}$ symbol rate. This is twice the speed achieved without the 2SH. (d) Receiver structure with PLL as a clock multiplier.

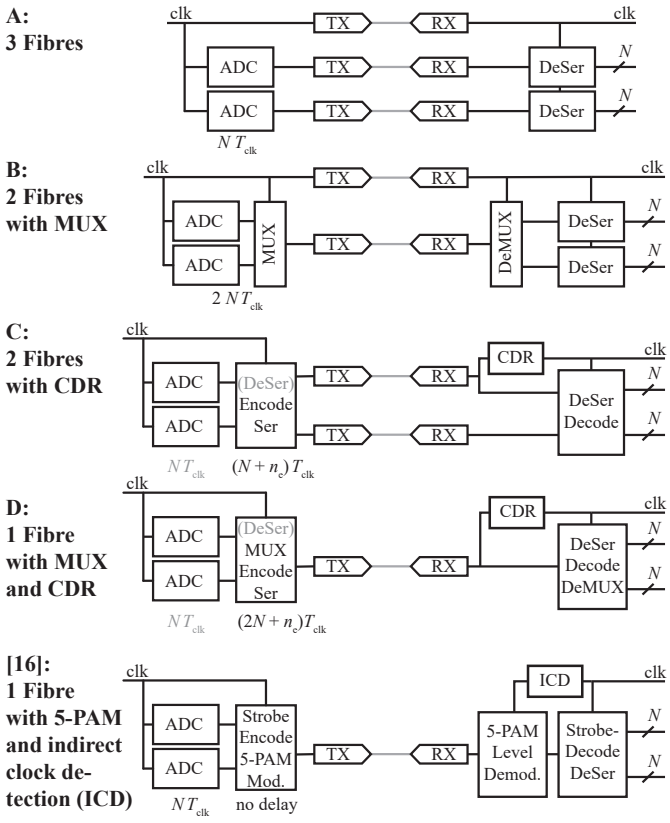

Fig. 15. Different unidirectional communication schemes used for transmitting two data streams and their clock signal captured with two ADCs. With scheme A and B, the ADCs have a serial output. With scheme C and D, it is reasonable to use parallel output ADCs. If this is the case, everything drawn in grey is obsolete. The ADCs have a resolution of N, the data header length is n_h and the clock frequency is $1/T_\mathrm{clk}$. If CDR is present, it is assumed that the word length increases by n_e bits.

are also dedicated clock multiplier ICs available that can cope with much lower input frequencies (e.g. Si5317, 1 MHz).

VII. Comparison with Benchmark Communication Schemes

In this section the complexity and the performance of the proposed communication interfaces is compared to other common unidirectional communication schemes based on the so called binary No Return to Zero (NRZ) principle (cf. [12] chp. 1.2 p. 5) as well as another 5-PAM variant presented in [16]. In the following M is the number of channels, N is the data word length in bit.

A. Circuit Description

The following list describes the communication schemes shown in Fig. 15 one by one.

A) The simplest way of unidirectional communication is to have one dedicated fibre for transmitting the clock and one for each data channel as shown in the upper part of Fig. 15 (scheme A). This simplicity comes at the cost of $M + 1$ fibres, transmitters (LEDs including driver) and receivers (photo diodes including TIA and detection circuit), such that the number of required parts is rather high (cf. Table V). For a single sensor connected with three instead of a single fibre, this might seem negligible, but e.g. in realistic modular power electronic systems, the number of data links can easily reach numbers of 200 and more.

B) A way to reduce the number of required fibres is multiplexing (Fig. 15 scheme B): Here the clock is transmitted just as before while the data is multiplexed on a second fibre.

C) Another way of saving fibres is to use clock data recovery (CDR), such that the clock does not have to be transmitted over a dedicated fibre (cf. e.g. [14]). The drawback of this method is that the data has to be encoded before transmitting it and decoded before it can be used at the receiving side (Fig. 15, scheme C). The length of the encoded signal is longer by n_e bits compared to the original signal, such that the word that has to be transmitted and received increases in length. With CDR, a continuous bit stream has to be sent, no matter if there is data to send or not. Otherwise, the PLL used for the CDR is losing lock. Therefore, a header (K-symbol) of length n_h is needed to identify the beginning of a valid data word. With 8b/10b encoding, the length of this header is fixed to $10\,\mathrm{bit}$ to ensure uniqueness (cf. [14]). When using ADCs with a serial interface, the serial data has to be de-serialised (DeSer), encoded and serialised (Ser) again, which causes a comparably large delay. Both the encoding and decoding require some kind of logic (CPLD/FPGA or dedicated ICs). Assuming that all M data streams are running on the same clock, only one CDR-device is needed. By additionally applying a 2^M-PAM on the encoded data streams, scheme C can be implemented with a single fibre.

D) Combining scheme B and C, one can reduce the number of required fibres to one (Fig. 15 scheme D), as all streams can simply be multiplexed before encoding and demultiplexed after decoding.

[16] The scheme proposed in [16] also requires only a single fibre if utilising $(2^M{+}1)$-PAM. The extra level is used to transmit a strobe symbol that indicates the same symbol in the data as the symbol sent before. As a result, there is never two equal transmitted symbols in a row. Therefore, a change in the symbol is equivalent with the (positive) clock edge and clock detection is possible without adding symbols to the data stream, as done for example with 8b/10b encoding. The scheme was proposed for very short electrical connections, where the signal strength is known a priori and the level detection/demodulation is comparably simple. If using it for a large range of signal strengths, some kind of intensity detection would be necessary for the 5-PAM demodulation.

B. Performance Comparison

Here, the performance (measurement delay and possible measurement sampling rate) of the different schemes are discussed and compared.

The measurement delay is important for the achievable control performance. The longer the measurement delay of a

TABLE V
PERFORMANCE COMPARISON

Scheme	# Fibres	Delay / T_{clk}	Sampling Rate $\cdot T_{\text{clk}}$
A:	$M+1$	N	N^{-1}
B:	2	$M \cdot N$	$(M \cdot N)^{-1}$
C:	M	$2N + n_{\text{e}}$	$(N + n_{\text{e}} + n_{\text{h}})^{-1}$
C (parallel ADC):	M	$N + n_{\text{e}}$	
D:	1	$(1+M)(N+n_{\text{e}})$	$(M(N+n_{\text{e}}) + n_{\text{h}})^{-1}$
D (parallel ADC):	1	$M(N+n_{\text{e}})$	
[16]:	1	N	N^{-1}
PAM-DCD [17]:	1	$2 \cdot N$	$(2N)^{-1}$
PAM-DCD-2SH:	1	N	$(N+2)^{-1}$

controlled variable, the lower the possible control performance in terms of disturbance rejection and (step) response. In the following, the measurement delay is defined as the time that passes from triggering the ADC to sample, to receiving the parallel value at the output of the communication interface. The physical delay of the TX and RX circuits as well as the light travelling through the fibre is neglected.

For all schemes, the (serial output) ADC causes a delay of NT_{clk}, as this is the time it takes to output the serial data stream.

For scheme A, there is only the serialisation delay of the ADC, because the de-serialisation at the receiver can be done 'online' and is therefore delay-free.

For scheme B, multi- and demultiplexing is done such that the data of all M data streams is put in one word. Therefore, to keep the toggling rate of the TX and RX circuits equal to scheme A, the ADC outputs operate M times slower compared to scheme A.

Looking at the transmitter side of scheme C, the serialised data from the ADC has to be de-serialised, encoded and then serialised again. As stated before, the de-serialisation can be done delay-free, but the serialisation of the encoded signal causes an additional delay of $(N + n_{\text{e}}) \cdot T_{\text{clk}}$, where n_{e} is the number of bits required for the encoding.

With scheme D, the statements of scheme B and C can be combined.

Another important performance parameter is the achievable measurement sampling rate, as it determines the maximum bandwidth of the measured signal (Nyquist criterion). The maximum possible measurement sampling rate corresponds to the sample rate of the ADC when the fibre is continuously occupied. Here, the system part dealing with the longest serial word is the limiting factor. For all considered schemes, this is at the de-serialisation of the frame on the receiver side. With all schemes using CDR, one also needs to include the n_{h} header bits in this case.

Table V provides an overview on the performance of the considered schemes, where the index p denotes that a parallel ADC is used. Fig. 16 shows the performance of the different schemes for various toggle rates.

As mentioned in section II, the clock transmission of the $(2^M{+}1)$-PAM-DCD proposed in [17] requires twice the bandwidth of the RX and TX circuits compared to the considered NRZ schemes. Therefore, having the same RX/TX toggle rate compared to the NRZ schemes results in twice the measurement delay and half of the measurement sampling rate as scheme A. Concerning the delay for the transmission of two channels, it is therefore on the same level as scheme B but requires only one fibre as shown in Fig. 16. For more channels ($M > 2$), the delay is lower and the sampling rate higher than with scheme B. Compared to scheme D, which is the only one also using a single fibre, the proposed scheme has less delay and a higher sampling rate even for two channels. This advantage increases with a higher number of channels.

With PAM-DCD using the Two Symbol Header (2SH) modulation introduced in Sec. VI, the necessary bandwidth is reduced by a factor of two for the same data rate as without the 2SH. Combined with the short header, very high sampling rates result, while the delay is equal to the one with scheme A. $(2^M{+}1)$-PAM-DCD with 2SH will always outperform 2^M-PAM with CDR to transmit the clock. Of course this comes at the price of reduced SNR because of the additional amplitude level.

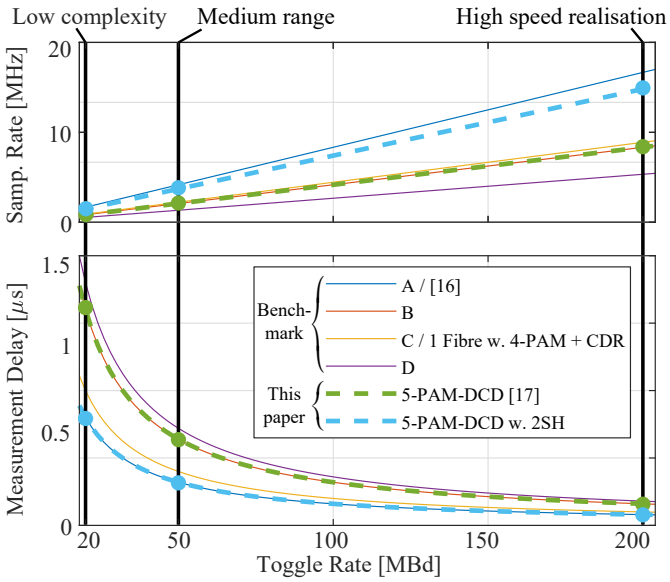

Fig. 16. Performance comparison of the communication schemes from Fig. 15 and the proposed one for different toggle rates of the transmitter/receiver circuits assuming $M = 2$ measurements with $N = 16\,\text{bit}$, $n_{\text{e}} = 4$ bit for the encoding and a $n_{\text{h}} = 10$ bit header for each frame. *Upper plot:* Maximum possible transmittable measurement sampling rate, meaning the sampling frequency of the ADC, where the POF is always occupied with data/header. *Lower plot:* Measurement delay, meaning the time that passes from triggering the ADC to receiving the parallel data.

C. Implementation Comparison

In order to compare the implementation complexity of the considered communication schemes, a PCB implementation of scheme D from Fig. 15 is presented in the following. Both transmitter ans receiver PCB are shown in Fig. 17, where the receiver PCB implements 4 receivers at once. A CPLD is needed at both PCBs for encoding and decoding (3b/4b or similar). The parts used for the shown PCBs are noted in Tab. VI. Integrated optical transmitters and receivers

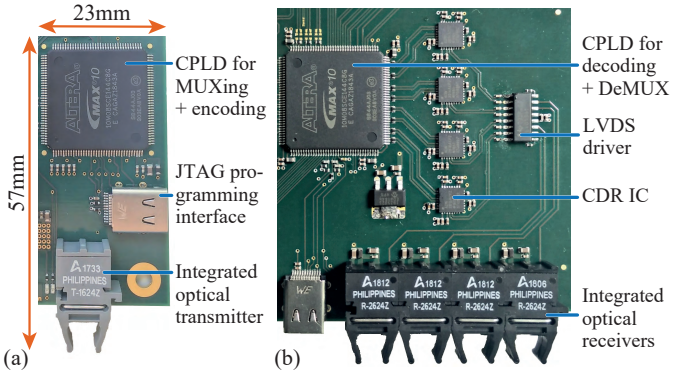

Fig. 17. PCB implementation of the transmitter (a) and receiver (b) to implement scheme D (Fig. 15) with a symbol rate of 50 MBd. The shown receiver PCB implements four receivers and uses dedicated ICs for the CDR. Note that CDR could also be done using the CPLD [29].

have been used. They provide a TTL-logic interface and a maximum baud rate of 50 MBd, such that they match with the middle black line in Fig. 16 (same bandwidth as the medium range receiver presented in Sec. V-B). Of course, the CPLD on the transmitter side can be exchanged with a smaller footprint equivalent (e.g. the 10M02DCV36C8G, 3×3mm). This however would require PCBs compatible with BGA components and together with the JTAG programming interface the PCM implementation size of the transmitter would still be larger than for the transmitter shown in Fig. 6(a). Comparing the PCB implementation area of the two presented designs, the transmitter used to implement scheme D ($1311\,\mathrm{mm}^2$) requires four times more space than the 5-PAM-DCD transmitter ($322\,\mathrm{mm}^2$). The transmitter (not using the 2SH) presented in this paper is capable of 200 Mbps data-rate, resulting in a achievable sample rate (previous subsection) of 14.29 MHz and measurement delay of 60 ns, while the one shown in this subsection achieves only 1.0 MHz (14.3 times lower) and 720 ns (12 times longer) respectively.

Looking at the presented receiver implementations, the low complexity variant (Sec. V-A) using the 2SH, is performing similar to scheme D running at 50 MBd for the given scenario used in the previous subsection: It achieves a maximum sample rate of 1.11 MHz (111 %) and measurement delay of 800 ns (11 % longer). Note that for ADCs with a serial data output, the measurement delay with method D increases to 1040 ns. In this case, the delay with the presented low complexity 5-PAM-DCD-2SH is 23 % lower. An advantage of a communication link based on scheme D is the very simple and compact receiver implementation due to the available integrated optical receivers.

VIII. Conclusion

In this paper, detailed designs of a transmitter and three different receivers based on a five level Pulse Amplitude Modulation (PAM) with Direct Clock Detection (DCD) have been presented. All designs are implemented on a PCB and based on highly available standard components. The DCD enables to recover the clock from the modulated signal without the need for encoding the transmitted data. The frequent return to the signal peak level is used to derive the signal strength and therefore also the detection thresholds for the amplitude levels. The three receiver realisations cover a large range of possible sensing applications with a data rate from 20 to 200 Mbps, where the low speed receiver variant has a low circuit complexity. The presented transmitter implementation including modulation and LED driver is simple and very compact. To overcome the speed limits of PAM-DCD, a modulation method called Two Symbol Header (2SH) is introduced which increases the possible data rate by a factor of two (up to 40 - 400 Mbps, depending on word length). Instead of returning to the peak level that represents the clock of the data stream for each transmitted symbol as proposed in [17], the peak level is now used as a word header.

The performance in the context of a sensing application of both the PAM-DCD with and without 2SH are compared to different unidirectional benchmark communication schemes. It is found that $(2^M{+}1)$-PAM-DCD performs better than the standard 2^M-PAM with 8b/10b encoding. $(2^M{+}1)$-PAM-DCD with 2SH performs almost as good as using $M+1$ dedicated fibres (one for each channel plus the clock) while using only a single fibre. Therefore, it can be used to replace standard PAM and/or binary NRZ based communication schemes featuring a single fibre solution with simple handling and a very low wiring effort as well as a very compact transmitter realisation. In comparison with the modulation scheme described in [16], the signal bandwidth of the (2^M+1)-PAM-DCD without 2SH is twice as high, leading to a much lower data-rate with a comparable transmitter/TIA circuity. However, with the 2SH, the bandwidth requirements of the PAM-DCD decrease a lot, such that the performance is similar or equal with [16]. Nevertheless, [16] does not provide a frequent return to the peak signal amplitude, such that the level detection for demodulating the PAM is more difficult than with PAM-DCD.

TABLE VI
CDR System Parts and Data (Fig. 17 & Fig. 15, Scheme D)

TX	CPLD	MAX 10M02SCE144C8G
	Opt. TX IC	AFBR-2624Z
RX	CPLD	MAX 10M02SCE144C8G
	Opt. RX IC	AFBR-1624Z
	LVDS driver	SN65LVDS391DR
	CDR IC	ADN2816ACPZ

List of Variables

X	Number of amplitude levels
M	Number of data channels
DR	Data rate
N	Number of measurement data bits per channel
n_h	Number of bits for frame header
n_e	Number of bits for encoding
T_clk	(Transmission) clock period

List of Abbreviations

CDR	Clock Data Recovery
PAM	Pulse Amplitude Modulation
PD	Photo Diode
OP	Operational Amplifier / Op-Amp
CB	Current Buffer
NRZ	No Return to Zero modulation
DCD	Direct Clock Detection
2SH	Two Symbol Header

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