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Ultralow-Power Atomic-Scale Tin Transistor with Gate Potential in Millivolt

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After decades of continuous scaling, further advancement of complementary metal-oxide-semiconductor (CMOS) technology across the entire spectrum of computing applications is today limited by power dissipation, which scales with the square of the supply voltage. Here, an atomic-scale tin transistor is demonstrated to perform conductive switching between bistable configurations with on/off potentials ≤2.5 mV in magnitude. In addition to the low operation voltage, the channel length of the transistor is determined experimentally and with density-functional theory to be ≤1 nm because the atoms instead of electrons are information carriers in this device. The conductance at on-states of the bistable configurations varies between 1.2 G_0 to 197 G_0 ($G_0 = 2e^2 h^{-1}$, e stands for the electron charge and h for Planck's constant). Thus, the device can supply driving current from 1 to ≈375 µA in magnitude for logic circuits with the drain-source dc voltage at decades of millivolts. The switching frequency of the atomic-scale tin transistor has reached 2047 Hz. Furthermore, the on/off potentials in millivolts can reduce the energy consumption in the interconnects of integrated circuits at least by ≈400 times. Therefore, the atomic-scale tin transistor has prospects in digital circuits with ultralow-power dissipation and can contribute to the sustainability of modern society.

1. Introduction

Information and communication technology (ICT) has spread into all aspects of social society. Therefore, its energy consumption in devices and services has become of strategic importance and a sustainable issue for modern society.[1] The energetics issue of ICT in the current and future raise a question of the ultimate energy efficiency of digital logic computation based on complementary metal-oxide-semiconductor (CMOS) technology. The advanced CMOS technology now faces a grand power consumption challenge due to a stagnation in the scaling of the supply voltage and the channel length.[2–4] Yet, the lowering of the supply voltage and overall power consumption is precluded by the subthreshold swing of a metal-oxide-semiconductor field-effect transistor (MOSFET) which is found to be at 60 mV dec^{-1} and room temperature.[4–6] These values are defined by the transport mechanism of CMOS devices based on thermionic emission over the barrier with fundamental thermionic limits (so-called Boltzmann tyranny).[6,7] More precisely, the total switching energy of a logic operation can be found as the sum of the dynamic, leakage, and interconnect components versus V_{DD}:

$$E_{total} = E_{dynamic} + E_{leakage} + E_{interconnect} \approx L_d C V_{DD}^2 \left(\alpha + 10^{\frac{-V_{dd}}{S}} \right) + \alpha C_{interconnect} V_{DD}^2 \quad (1)$$

where L_d is the logic depth, C is the switched capacitance, V_{DD} is the supply voltage, α is the logic activity factor (typically ≈0.01), and S is the subthreshold swing.[3,8] Equation (1) indicates that the most effective way to control the power

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density is to scale down the supply voltage. The only way to decisively break the power dissipation bottleneck is to change the operation mechanism of a transistor in ways that facilitate the further reduction of operating voltage.[9] "There is an enormous research space to be explored once you step outside the confines of the established technology," says Thomas Theis.[10] In this spirit, we have introduced atomic-scale metallic transistors operated with a novel fundamental switching paradigm.[11–15]

This paper demonstrates an atomic-scale tin transistor operated with an electrochemical potential applied to a gate. The required switching potential can be as low as 2.5 mV in magnitude, which is much lower than the minimal level on the supply voltage of a CMOS digital logic circuit set by Landauer's limit:[16] $V_{DD} \geq 2(\ln 2)k_B Te^{-1} = 35.8$ mV, where k_B is Boltzmann constant, $T = 300$ K, and e the electron charge,[17,18] and even smaller than the "action potentials" of neuron fire (−20–100 mV) in magnitude.[19]

2. Operation Mechanism of Electrochemically Controlled Atomic-Scale Tin Transistors

Figure 1a shows that the electrochemically controlled single-atom tin transistor is a modified electrolytic cell. Electrical potential energy is converted to chemical potential energy in the electrolytic cell. The electrolytic cell uses an electric current to force a particular chemical reaction, which would otherwise not occur. A standard electrolytic cell consists of two electrodes. One of the two electrodes is the anode, where oxidation takes place. The cathode is the electrode where reduction takes place. In the atomic-scale tin transistor, the gate electrode is taken as one electrode and the combination of source and drain as another. The gate electrode is an electrochemical counter electrode, which can be placed at any location in the electrochemical cell (sometimes decades of millimeters apart). Therefore, no static electric effect is related to the gate in the atomic-scale tin transistor with the operational potential in a few decades or even a few millivolts. We take the terminology of "Gate" from the semiconductor transistor and name our counter electrode "Gate" in our device. The "Gate" in the atomic-scale metallic transistor is not comparable with the gate of a semiconductor transistor. The source electrode is virtually grounded. A negative dc voltage of U_{DS} is applied to the drain electrode.[12,13] When the $U_G > U_{DS}$, the gate electrode is the anode, and the combination of source and drain is the cathode. Some tin atoms on the surface of the gate are oxidized and dissolved as ions into the electrolyte:

$$\mathrm{Sn(solid)} \rightarrow \mathrm{Sn^{2+}(aq.)} + 2e^- \quad (2)$$

At the same time, an equal number of ions are reduced on the surface of the combination of source and drain electrodes:

$$\mathrm{Sn^{2+}(aq.)} + 2e^- \rightarrow \mathrm{Sn(Solid)} \quad (3)$$

Some nano- or microcrystals grow on the surfaces of both source and drain. Two of them are large enough to meet in the gap between the source and drain and form a tin point-contact, as illustrated in Figure 1a. As the $U_G < U_{DS}$, the functions of the gate and the combination of source and drain are reversed. The oxidation reaction takes place on the combination and the reduction on the gate. The tin point-contact is dissolved because of oxidation. When the U_{DS} is fixed, the tin point-contact can be built and dissolved reversibly by letting $U_G > U_{DS}$ or $U_G < U_{DS}$.

On clean gold (or copper) microelectrodes to fabricate an atomic-scale tin transistor, the initial deposition potential should be 30 mV. We applied 30 mV to the gate, deposited electrochemically tin on the source and drain electrodes, and finally formed a point-contact in the gap between the two electrodes on a new sample. After stabilizing the point-contact for some time, many tin micro-and nanocrystals were deposited on the gold (or copper) surfaces of both source and drain electrodes. The deposition potential can be reduced to a few millivolts in the training and operation phases.

3. Results

3.1. Performance of Electrochemically Controlled Atomic-Scale Tin Transistors

The schematic diagram of our experimental setup for the atomic-scale tin transistor is shown in Figure 1a. The atomic-scale tin transistor is in an oxygen-free electrolyte protected with Argon. The electrolyte solution consisted of $SnSO_4$ (10 mM) + H_2SO_4 (40 mM) in bi-distilled water. The model of an atomic configuration at on-state with the conductance of 1.5 G_0 ($G_0 = 2e^2h^{-1}$, e stands for the electron charge and h for Planck's constant) is illustrated with the data calculated with density-functional theory (DFT). The operating mechanism, the experimental setup, and the fabrication of atomic-scale tin transistors are described in more detail in the Experimental Section. Figure 1b shows an SEM image of the two working electrodes (source and drain) in an open window insulated with PMMA 950 photoresist. Figure 1c displays an SEM image to detail the gap between two working electrodes. Figure 1d describes the surface morphology of the two working electrodes after the operation of the atomic-scale tin transistor with an SEM image. For comparison and consistency, the high conductance is indicated in units of the quantum conductance G_0. Following the gate potential via the feedback mechanism,[11] Figure 1e presents a high conductance (0–14 G_0) and current (0– −14 μA) switching. Figure 1f exhibits conductance switching between 0 and 7 G_0 and a current changing between 0 and −7 μA controlled via an A/D card (NI PCI-6221) by a virtual function-generator (NI Labview software package). The conductance and the corresponsive current switching follow the gate potential variation in a delay of 0.1 s.

3.2. Searching for the Smallest Operation Potential Window

In the atomic-scale tin transistor, the potential differences between the gate, source, and drain were determined through U_{DS} applied between the drain and source and the gate potential U_G. The on/off operation ranges of the gate potential are of interest because of an energy-efficient operation. The

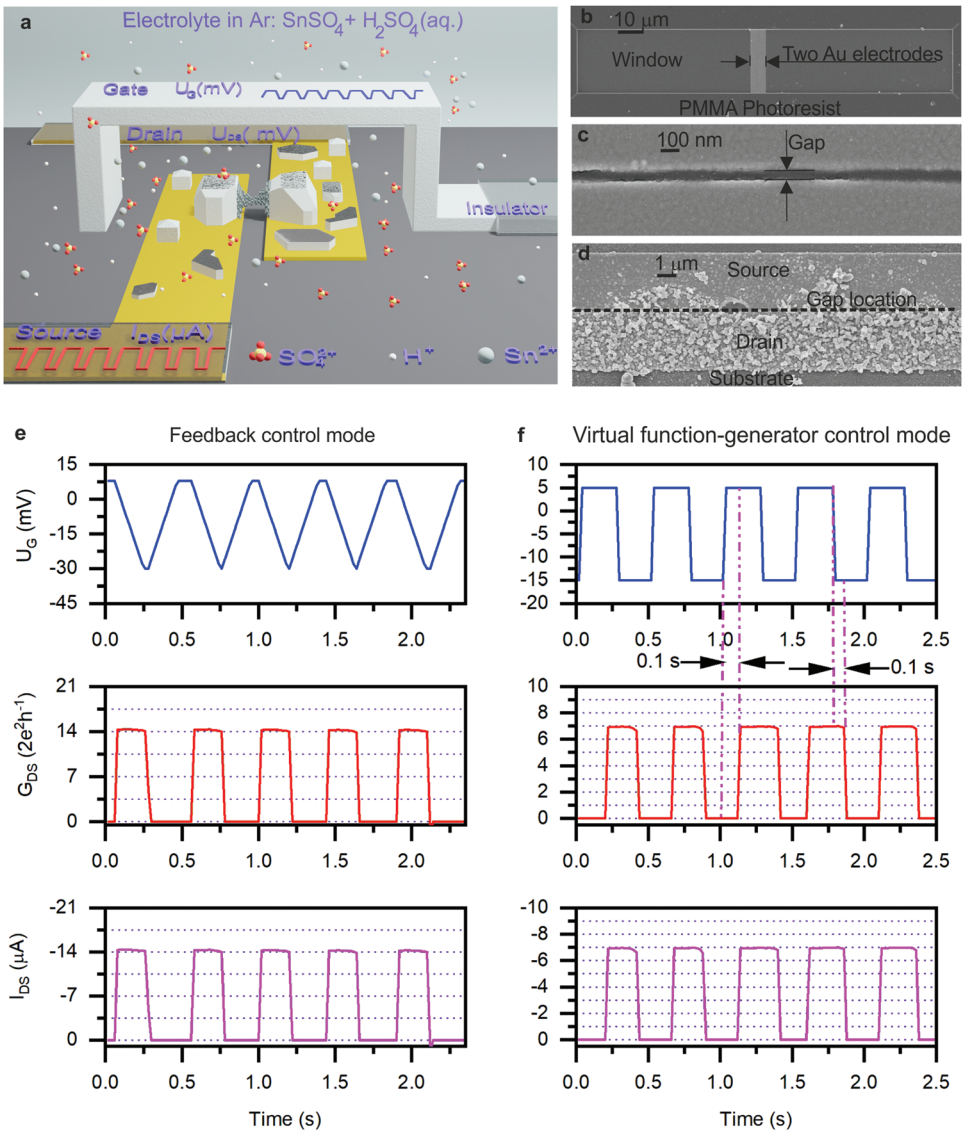

Figure 1. Performance of electrochemically controlled atomic-scale tin transistors. a) Schematic diagram of an atomic-scale tin transistor operated in the argon environment. The electrolyte consisted of $SnSO_4$ (10 mM) + H_2SO_4 (40 mM) in bi-distilled water. The source electrode was virtually grounded via a trans-impedance circuit while a dc U_{DS} was applied to the drain electrode for conductance measurements. The model of an atomic-scale tin point-contact with the conductance of 1.5 G_0 is illustrated with theoretical data. b–d) Three SEM images of the two working electrodes (source and drain) in overview, in detail as prepared and after usage. e) Conductance switching is controlled via the feedback mechanism. The top blue ramping wave between 8 and –30 mV expresses the potential change on the gate, the middle red digital graph presents the conductance variation (0–14 G_0) following the gate potential, and the bottom magenta rectangular curve shows the corresponding current from 0 to –14 μA measured with U_{DS} of –12.9 mV. f) Virtual function-generator-controlled conductance switching between 0 and 7 G_0. The upper blue rectangular wave between 5 and –15 mV illustrates the potential applied to the gate by the virtual function generator. The middle red digital signal exhibits conductance switching between 0 and 7 G_0 succeeding the gate potential with a delay at 0.1 s. Simultaneously, the lower magenta rectangular wave demonstrates the corresponsive current variation in a digital form between 0 and –7 μA when U_{DS} is set at –12.9 mV.

atomic-scale tin transistors are put into operation in four steps, that is, building tin point-contact, training the point-contact, reducing the absolute value of U_{DS}, and decreasing the difference between U_G and U_{DS} from both upper and lower sides of U_{DS}, as described in the Experimental Section. **Figure 2**a–d illustrates 4 bistable switching sequences (0–16 G_0) achieved by setting U_{DS} at a) –12.91, b) –6.48, c) –3.23, and d) –1.62 mV, individually. The corresponding on/off potentials (U_G) were a) 12/–30 mV (ΔU_G = 42 mV), b) 2/–10 mV(ΔU_G = 12 mV), c) 0/–4.5 mV(ΔU_G = 4.5 mV), and d) 0.5/–2.5 mV (ΔU_G = 3 mV). As a general tendency, the switching period increases as the magnitudes of U_{DS} and U_G decrease. The absolute current values were reduced by half, by a quarter, and by one eighth when the magnitude of U_{DS} was decreased from –12.91 mV to –6.48, –3.23, and –1.62 mV, correspondingly. The values of current I_{DS} were a) –16, b) –8, c) –4, and d) –2 μA, respectively. Figure 2e demonstrates a bistable switching sequence (Conductance: 0–24 G_0 and current: 0– –6 μA) achieved by setting U_{DS} at –3.23 mV. In the beginning, the on/off potentials at the gate were –1.5 mV/–4 mV for some periodic switching cycles (ΔU_G = 2.5 mV). Then, an

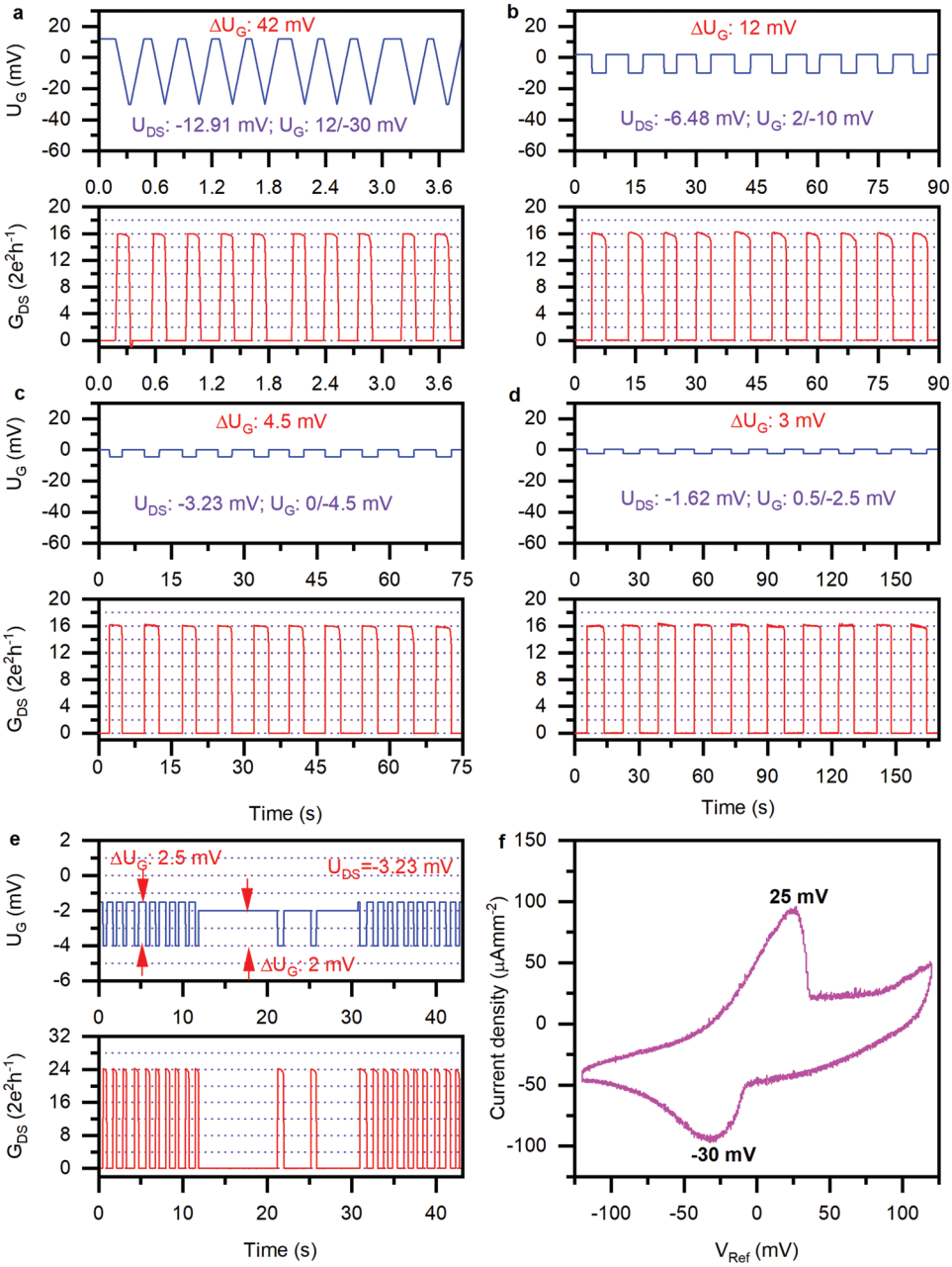

Figure 2. Searching for the smallest operation potential window. The potential differences between the gate, source, and drain were determined through U_{DS} and the gate potential U_G. Four bistable switching sequences (0–16 G_0) were achieved by setting U_{DS} at a) −12.91, b) −6.48, c) −3.23, and d) −1.62 mV, individually. The corresponding on/off potentials (U_G) were 12/−30 (a), 2/−10 (b), 0/−4.5 (c), and 0.5/−2.5 mV (d). The current I_{DS} was measured to be −16 (a), −8 (b), −4 (c), and −2 μA (d), respectively. e) Demonstration of the smallest operating gate potential window of an atomic-scale tin transistor. Graph (e) presents a bistable conductance switching (0–24 G_0) controlled with two different on-gate potentials (U_G). The current (I_{DS}) at the on-state was −6 μA. f) Cyclic voltammogram of tin performed in the electrolyte of $SnSO_4$ (10 mM) + H_2SO_4 (40 mM) in bi-distilled water.

effort was made to find the limit of the potential window. The switching process became slower and irregular when the on-potential was reduced from −1.5 to −2 mV, and the off-potential was kept at −4 mV (ΔU_G = 2 mV). As on/off potentials were set back at −1.5/−4 mV, the switching periodicity recovered at once.

Figure 2f presents a cyclic voltammogram of tin performed in the electrolyte of $SnSO_4$ (10 mM) + H_2SO_4 (40 mM) in bi-distilled water. One piece of gold wire with a diameter of 0.25 mm was used as a working electrode and two pieces of tin wire with a diameter of 0.5 mm as counter and quasi-reference electrodes. The electrochemical potential was scanned reversibly within the ramping range between −120 and 120 mV at a 4 mV s^{-1} in the aqueous electrolyte. The cyclic voltammogram is depicted in the Convention of the International Union of Pure and Applied Chemistry (IUPAC). The formal reduction potential is calculated by $(E_{pc} + E_{pa})/2$. Therefore, the potential is −2.5 mV in this case. The electrochemical potential from the cyclic voltammogram can be translated into the potential applied to the gate

electrode in the atomic-scale tin transistor by just multiplying the value by –1. Therefore, the smallest reduction potential of tin is at ≈2.5 mV, which has been confirmed in Figure 2d, e.

3.3. Demonstration of Bistable Conductance Switching

To verify the variations in possible bistable atomic configurations in atomic-scale tin transistors, we investigated the operation behavior of atomic-scale tin transistors via the feedback mechanism, as aforementioned in Figure 1e. For this test, U_{DS} was set at –12.91 mV. Ten switching sequences with seven cycles are selected as examples and presented in two columns in **Figure 3**. The conductance is plotted on the same scale in each column because of comparison and clear presentation, but the scales are not the same for the two columns. The scales are –0.25–3 (left column), –0.5–7 (right column). Time axes vary to meet the time length of individual switching sequences. In the left column, five graphs demonstrate that the atomic-scale tin transistors can implement operation between an "off-state" and

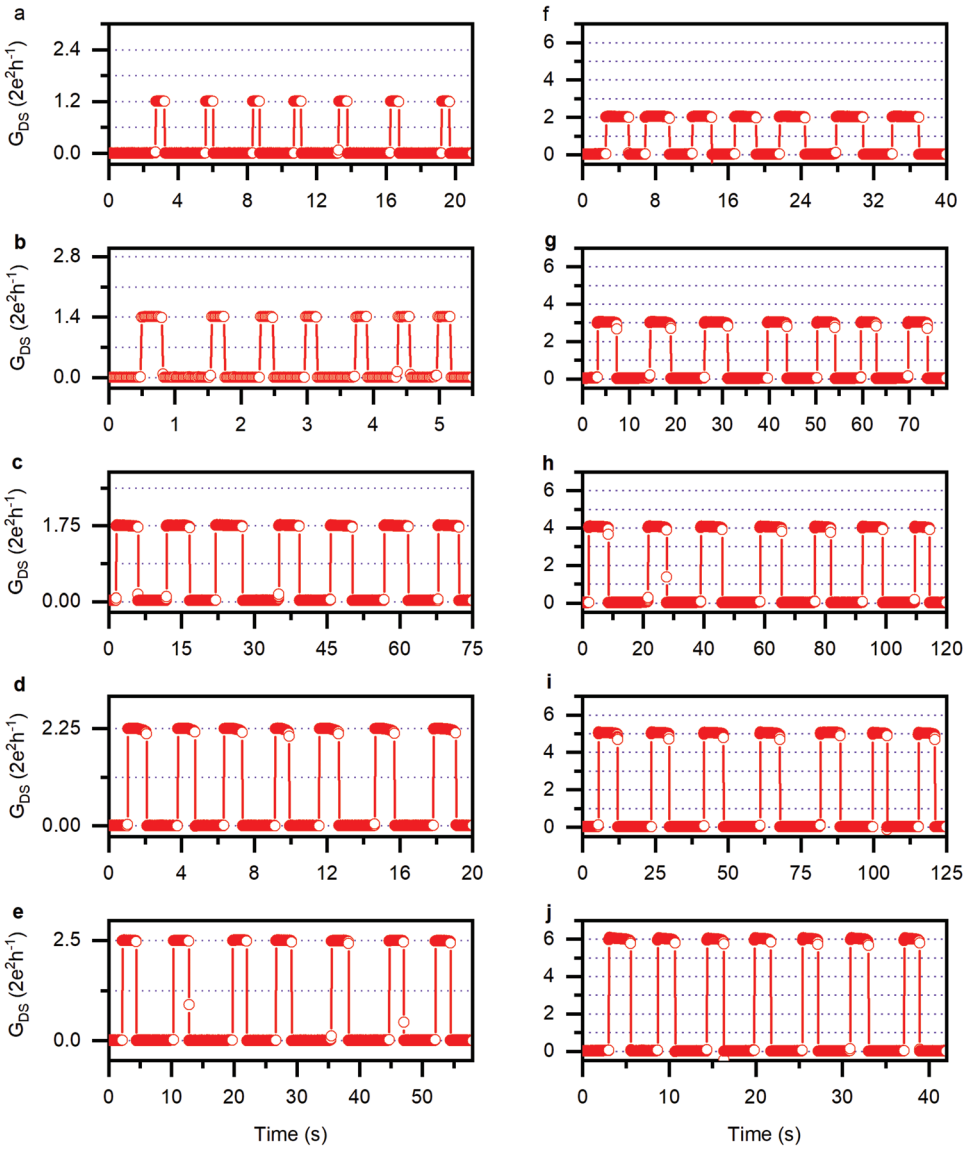

Figure 3. Demonstration of bistable conductive switching between 0 and different non-integer and integer quantum conductance levels. Ten switching sequences with seven cycles are selected as examples and presented in two columns. Via the feedback mechanism, the operation behavior of atomic-scale tin transistors was investigated while U_{DS} was set at –12.9 mV. The axes of conductance in the left column are divided into different units in each panel to plot adapted gridlines as eye guidance at on-states. Gridlines separate the conductance axes at integer quantum conductance levels in the right column. Time axes vary to meet the length of individual switching sequences. In the left column, five graphs demonstrate that the atomic-scale tin transistors can implement operation between an "off-state" and "on-states" with non-integer quantum conductance at a) 1.2 G_0, b) 1.4 G_0, c) 1.75 G_0, d) 2.25 G_0, and e) 2.5 G_0, respectively. In the right column, five digital wave plots illustrate the drain-source conductance switching between the non-conducting "off-state" and the conducting "on-state" with integer quantum conductance at f) 2 G_0, g) 3 G_0, h) 4 G_0, i) 5 G_0, and j) 6 G_0, correspondingly. The plots utilize both lines (as eye guidance) and empty circles (measured points).

"on-states" with non-integer quantum conductance at a) 1.2 G_0, b) 1.4 G_0, c) 1.75 G_0, d) 2.25 G_0, and e) 2.5 G_0, respectively. The deposition/dissolution potentials for each switching sequence were 15/−35 mV (1.2 G_0), 15/−35 mV (1.4 G_0), 8/−24 mV (1.75 G_0), 10/−30 mV (2.25 G_0), and 10/−30 mV (2.5 G_0), correspondingly. A longer sequence of 0–2.25 G_0 quantum conductance switching in 1500 s is illustrated in Figure S2, Supporting Information, indicating the cyclic endurance of single-atom tin transistors. As indicated in the conductance histogram of atomic-scale tin point-contacts, the conductance of single-atom tin point-contacts should be enveloped in the first peak (0–4 G_0) of the tin conductance histogram.[20] In the right column, five digital wave plots illustrate the drain-source conductance switching between the non-conducting "off-state" and the conducting "on-state" with integer quantum conductance at f) 2 G_0, g) 3 G_0, h) 4 G_0, i) 5 G_0, and j) 6 G_0, individually. During the investigation of atomic-scale tin transistors, the quantum conductance periodic switching between 0 and 1 G_0 has not been observed. The on/off potentials for each switching sequence were 8/−24 mV (2 G_0), 8/−24 mV (3 G_0), 8/−24 mV (4 G_0), 8/−24 mV (5 G_0), and 8/−24 mV (6 G_0), correspondingly. In Figure S4, Supporting Information, five graphs in rectangular waveform demonstrate the conductance switching sequences with on-states at a) 8 G_0, b) 9 G_0, c) 10 G_0, d) 11 G_0, and e) 12 G_0, respectively. Since the plots utilize both line and empty circles (measured points), almost only direct transitions of closing edges are observed between these two states. A few intermediate levels are found in the opening edges. This behavior is the same as that observed for the atomic-scale lead (Pb) transistors.[12] Thus, the results indicate that the switching transition of a tin transistor is also due to a reproducible, bistable atomic-scale reconfiguration. The values of on/off switching potentials in each graph are 10/−30 mV (8 G_0), 10/−30 mV (9 G_0), 10/−30 mV (10 G_0), 8/−30 mV (11 G_0), and 8/−30 mV (12 G_0), correspondingly.

The contacts are formed electrochemically in a diluted electrolyte, and they differ from contacts formed in a vacuum by mechanical methods such as the mechanical break junction technique. Electrochemically formed contact is free of the mechanical stress and dislocations, vacancies, and other defects produced due to the deformation process. This method gives the unique opportunity to study the transport properties in a system free from mechanical defects, which is always in equilibrium with the solution by exchange current.[21,22] Silver has the ground state configuration of $[Kr]4d^{10}5s^1$ and only one s-valence electron. Theoretical calculations indicate that the conductance of silver single-atom point contacts changes only a little by tilting and twinning the angles of the two electrode tips with respect to one another. Therefore, the silver single-atom transistor switches between a nonconducting off-state and an on-state only at n G_0 (integer n).[11,14] Tin has the electronic ground-state configuration of $[Kr]4d^{10}5s^25p^2$, two s, and two p electrons on the outside shell. Its atoms exhibit a valence of either two or four. In the bulk crystal, complicated effects of hybridization (sp^3) and considerable spin-orbit interaction make these metals very poor candidates for free-electron approximation.[20] The hybrid orbitals have a specific orientation, and the four lobes are naturally oriented in a tetrahedral fashion like Pb. The Pb electronic ground-state configuration is $[Xe]4f^{14}5d^{10}6s^26p^2$. Since the outermost d electrons are nearly 10 eV below the 6s band and approximately 20 eV below the Fermi level, the 5d levels can be viewed as core levels, and the electronic properties of Pb are dominated by the 6s and 6p bands.[23] The multiplicity of atomic reconfigurations has been observed in an electrochemical Pb single-atom transistor.[12,20,24] With the same mechanism as the Pb single-atom transistors, the single-atom tin transistors exhibit non-integer and integer quantum conductance switching except 1 G_0. The multiplicity of atomic configurations in the atomic-scale tin transistors does not mean that the conductance of the tin point-contacts is not controllable. We can set the conductance of tin point-contacts in the training process.

3.4. Demonstration of Atoms Instead of Electrons as Information Carriers

To confirm the influence of the gate potential (U_G) and drain-source dc voltage (U_{DS}) on the operation behaviors of atomic-scale tin transistors, the switching-on gate potential, the switching-off gate potential, and the drain-source dc voltage were changed in step 2 mV in three experiments, respectively. The experimental results are presented in **Figure 4**a. (via variation of the switching-on gate potential, 0–70 G_0 switching, Figure S5, Supporting Information, in detail), Figure 4b (via variation of the switching-off gate potential, 0–166 G_0 switching, Figure S6, Supporting Information, in detail), and Figure 4c (via variation of U_{DS}, 0–197 G_0 switching, Figure S7, Supporting Information, in detail). Because the atomic-scale tin transistors perform bistable conductance switching, the conductance at on-states in these three figures keeps constant during variation of the gate potentials and the drain-source dc voltage. However, the variation of the gate potential and the drain-source dc voltage influences the switching period. At on-states, the electric current does not depend on the gate potential during bistable conductance switching. Since the atomic-scale tin transistor has metallic point-contact at on-state, its I-V characteristic is Ohmic.[25] The electric current at on-state is linearly proportional to the drain-source dc voltage, as Graph in Color Magenta (Figure 4c) indicates. The current changes (I_{DS}) from −197 to −376 μA when U_{DS} varies from −13 to −25 mV. The constant conductance at on-states in these three experiments demonstrates robust bistable configurations.

For Boolean computation to occur, a physical state variable must be able to reside in two distinguishable states, be controlled between states (write), read, and initialized in a defined state (erase). In addition, information is also required to be transmitted from one physical location to another.[26] For the modern ICT, semiconductor-based electronics, commonly referred to as electron/hole charge-based electronics, can be fundamentally considered a physical state variable that can alter between various states of electron population (charging/discharging of capacitance).[26] Therefore, electrons/holes work as information carriers in semiconductor-based electronics. For example, a collective state switch implements binary operation by reversing a material's order parameter such as ferromagnetism, ferroelectricity, and ferroelasticity as a physical state variable. The information carriers for magnetization,

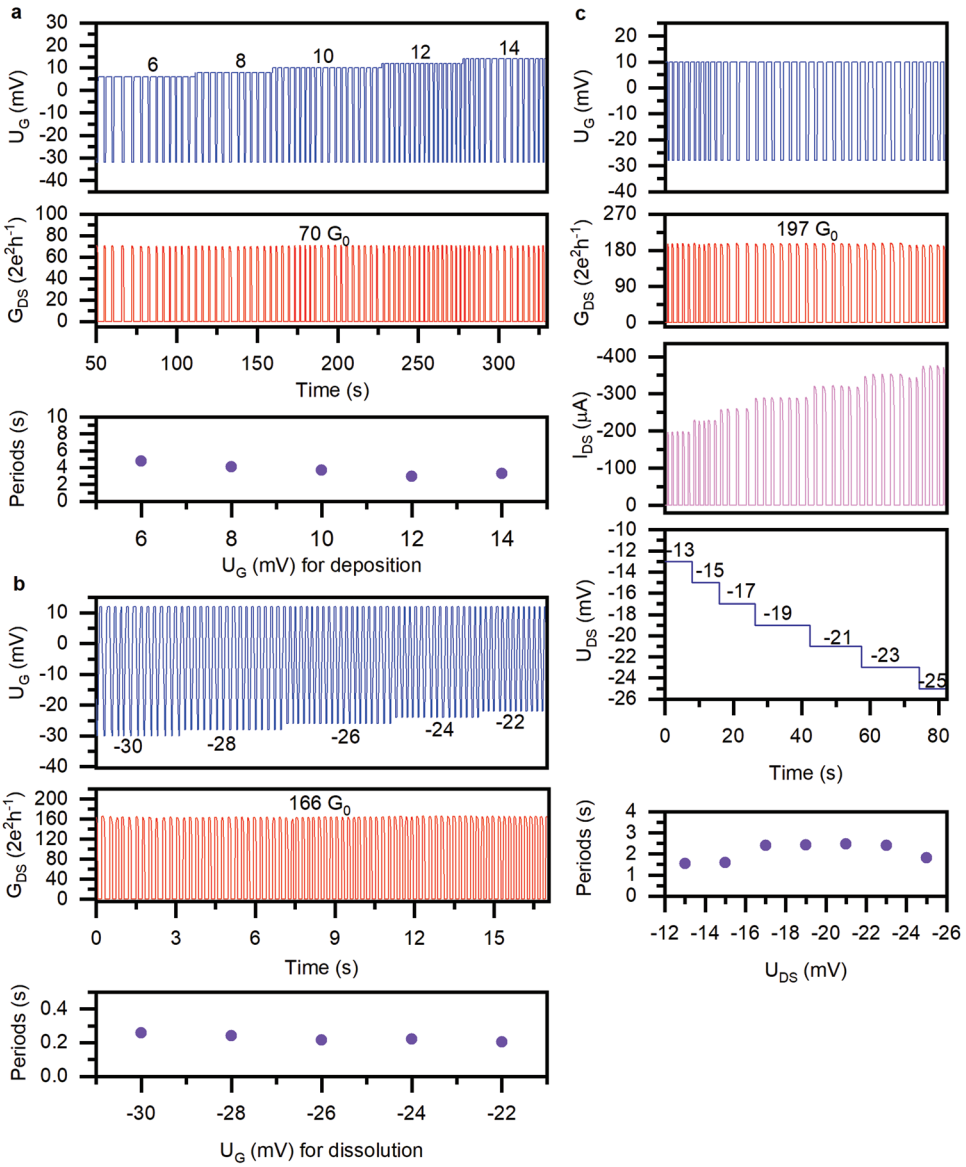

Figure 4. Demonstration of atoms instead of electrons as information carriers with robust bistable configurations in atomic-scale tin transistors. a) Graphs show the influence of the switching-on gate potential (U_G) on the operation behaviors of an atomic-scale tin transistor. The upper blue graph shows the switching-on gate potential increasing from 6 to 14 mV at 2 mV. The middle red graph illustrates the conductance switching between 0 and 70 G_0. The on-state electric current was –70 μA as the U_{DS} was set at –12.9 mV. The lower graph presents the switching periods as solid round violet points versus the switching-on gate potential (U_G). b) Graphs indicate the impact of the switching-off gate potential (U_G) on the operation behaviors of a nano-scale tin transistor. The upper blue graph shows the switching-off gate potential increasing from –30 to –22 mV at the step of 2 mV. The middle red graph illustrates the conductance switching between 0 and 166 G_0. Since the U_{DS} was set at –12.9 mV, the on-state electric current was –166 μA. The lower graph presents the switching periods as solid round violet points versus the gate potential. The switching period decreased gradually when the switching-off gate potential increased from –30 to –22 mV at the step of 2 mV. Finally, (c) graphs present the influence of the drain-source dc voltage (U_{DS}) on the operation behaviors of a nano-scale tin transistor. The upper blue graph shows the gate potential switching between –28 (switching-off) and 10 mV (switching-on). The red graph illustrates the conductance switching between 0 and 197 G_0. The magenta graph presents the switching drain-source current. The black graph displays the stepwise change of U_{DS} from –13 to –25 mV at the step of –2 mV. The violet graph demonstrates the switching period as solid round points versus the drain-source dc voltage.

polarization, and strain are electron spin or magnon, electron, and phonon, respectively.[4,7] By comparison, quantum conductance as one physical state variable represents information in the atomic-scale tin transistor. The quantum conductance as the physical state is determined by the atomic configuration of the atomic-scale tin point-contact. The point-contact can be dissolved and rebuilt by the electrochemical processes indicated in Equations (2) and (3). Therefore, atoms instead of electrons are information carriers in the atomic-scale tin transistors. Both semiconductor-based devices and atomic-scale tin transistors work in the electrical domain.[4,26–28] The electrical current in both devices transmits information from one physical location

to another. The difference between the information carriers related to the physical state variables and electric current carriers in the electronic circuits should be made.

The constraint on the signal voltage swing ($2k_BT\ln2e^{-1}$ = 35.8 mV, e stands for electron charge and T = 300 K) of CMOS (two transistors as one unit, electrons and holes as information carriers) digital logic circuits by Landauer's limit ($k_BT\ln2$).[17] The fundamental minimum binary switching energy dissipated for a single electron in equilibrium with the thermal bath is $k_BT\ln2$ = 17.9 meV at 300 K. We can derive the minimum operating voltage of a single-electron device implementing the binary logic switch to be $k_BT\ln2e^{-1}$ = 17.9 mV.[26,28,29] The switching sequences illustrated in Figure 2b–e show that the magnitude switching on/off potentials are smaller than 17.9 mV. These data can preclude electrons as information carriers in the atomic-scale tin transistors with thermodynamics.

3.5. Increasing the Switching Frequency of an Atomic-Scale Tin Transistor

An atomic-scale tin transistor consisted of two microelectrodes in the separation of 100 nm as the source and drain, a tin wire in diameter of 0.5 mm with high purity as the gate, and the electrolyte of $SnSO_4$ (30 mM) + H_2SO_4 (40 mM) in the cell. The transistor was connected to two computers to determine how fast the transistor with the current configuration could perform conductive switching. As described in detail in the Experimental Section, the first computer-controlled the gate potential with a feedback mechanism and read the voltage from the trans-impedance circuit at the sampling rate of 40 000 samples s^{-1} via an A/D card (NI PCI 6031E) by a program written in C without the data recording function. A fast program developed in NI LabView in the second computer recorded the gate potential and the voltage signal from the trans-impedance circuit at a sampling rate of 500 000 samples s^{-1} at maximum via an A/D card (NI PCI 6120). The gate potential in a rectangular wave and the conductance of the atomic-scale tin transistor converted from the voltage signal are illustrated in the upper graph (blue) and the lower graph (red) in **Figure 5**, respectively. The transistor switched in a bistable configuration between 0 and 13 G_0. The frequency reached 2047 Hz. The on/off gate potentials were 12 and −30 mV, respectively. The conductance at the on-state decreased from 13 G_0 gradually to some level and then jumped into off-state with signal oscillation at the off-state because of the capacitance in the circuit. A section of the switching sequence in 268 ms is illustrated with Graph a in Figure S3, Supporting Information. Graphs b and c are the zoom-in of Graph a in different time scales. This result demonstrates that the conductive switching frequency of the atomic-scale tin transistor can be improved by optimizing the source, drain, and gate configuration and increasing the electrolyte concentration. The atomic-scale transistors are one kind of electrometallization cell with three electrodes, as described in **Section 2**. To estimate their switching time, we can get enlightenment from the experimental results (5 ns)[30] and theoretical simulations (from hundreds of picoseconds to a few nanoseconds)[31] of two-terminal resistive switching in nanoscale electrometallization cells. The experimental and theoretical results

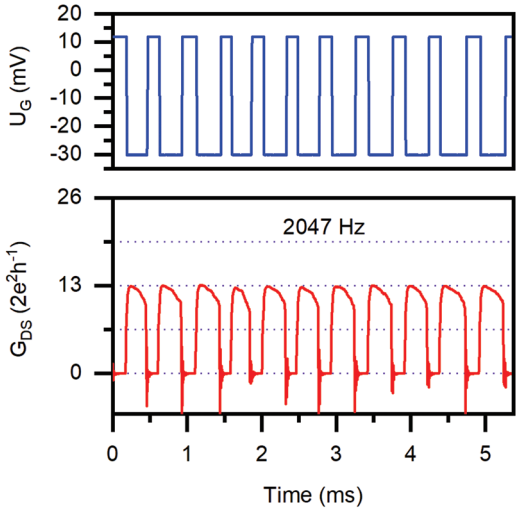

Figure 5. An atomic-scale tin transistor performing conductive switching in kHz. The upper rectangular wave presents the electrochemical potential applied on the gate electrode, while the lower red graph shows the conductive switching signal of the atomic-scale tin transistor.

demonstrate that the building of metallic junctions via solid electrochemical processes in nanoscale electrometallization cells can be finished in nanoseconds. The theoretical simulation indicates that stable switching only occurs when the concentration of Cu in the dielectric is over 12% per SiO_2 formula unit. The copper ions in the SiO_2 matrix are not freely movable without the assistance of an external electrical field. The Sn^{2+} ion concentration in a saturated aqueous solution of $SnSO_4$ can reach a 2.7% molar ratio to water molecules in ambient conditions. The Sn^{2+} ions are freely movable in the aqueous electrolyte. Therefore, there should be an approach to realize the fast switching with the atomic-scale tin transistors in nanoseconds or hundreds of picoseconds. The cycling endurance of two-terminal resistive switching devices has reached 10^{12}[32] or even 10^{15}.[33]

3.6. Analysis of Energy Consumption

To develop the atomic-scale tin transistor as a potential alternative to the CMOS device, we should analyze where this new technological approach can reduce energy consumption: in the switching process or the interconnects. The energy consumption in an atomic-scale tin transistor comes from electrochemically building and dissolving the tin point-contact between the source and drain. These building and dissolving procedures of the point-contact involve the material transfer of tin atoms amid the gate and the gap between the source and drain. The minimal switching energy (E_{SW}) is estimated by the product of the number ($N_{contact}$) of tin atoms building the point-contact, two electrons needed by reducing Sn^{2+} ions, the potential difference between the gate and drain (U_1 (on) or U_2 (off) in volt), and one building and one dissolving procedure in a cycle. Therefore, the energy consumption of an atomic-scale tin transistor in one period is calculated as the sum of the dynamic and leakage parts:

$$E_{\text{total}} \approx E_{\text{dynamic}} + E_{\text{leakage}} = \int_0^T I_G U_G \mathrm{d}t + \int_0^T I_T U_{DS} \mathrm{d}t$$
$$\approx N_{\text{contact}} \cdot 2 \cdot e \cdot U_1 + N_{\text{contact}} \cdot 2 \cdot e \cdot U_2 + \int_0^T I_t U_{DS} \mathrm{d}t \quad (4)$$

where T is the period $T = 1/f$, f the operation frequency, U_{DS} is the dc voltage applied across the drain and source electrodes, I_G is the electrochemical current between gate and drain-source, I_T tunneling current between the drain and source.

The tunneling current at the off-state in the atomic-scale tin transistor is calculated with the formula applied in an electrochemical scanning tunneling microscopy (EC-STM),

$$I_t(d) = AeU_{DS} \exp\left(-4\pi \cdot \frac{\sqrt{2m\varphi}}{h} \cdot d\right) = AeU_{DS} \exp\left(-1.025\sqrt{\varphi} d\right) \quad (5)$$

where A is a constant, e electron charge, φ the tunnel barrier in the electrolyte in volt, U_{DS} the voltage across the drain and source, and d the gap width in Å.[34,35] Considering the electrolyte concentration applied in the experiment, the tunnel barrier φ is set at 1.6 V for further estimation.[35] A tunneling regime with $R_T < 10^7$ Ω was assigned approximately to a substrate-tip separation range < 1 nm in an EC-STM.[36] With Equation (5), it is estimated that when the gap width increases by 5.33 Å, the tunneling current should decrease by 1000 times. The tunneling current at off-state in the atomic-scale tin transistor was measured to be –1.7 nA when U_{DS} was set at –3.23, and the conductance at on-state was measured to be 16 G_0. The gap is estimated to be 0.85 nm.

To estimate the "lower limit" to the number of atoms contributing to the switching, we performed ab initio simulations of Sn filaments, an example of which is illustrated in **Figure 6**a. Several models of tin point-contacts were constructed using DFT. The simulations were performed using the CP2K code,[37] the PBE functional,[38] Goedecker–Teter–Hutter (GTH) pseudopotentials,[39] and a double zeta-valence polarized (DZVP) basis set.[40] The initial structures are prepared by cutting an hourglass-shaped configuration out of bulk Sn. This point-contact is embedded between two Sn electrodes. Subsequently, the electrodes are repeatedly pulled apart and pushed together to optimize the atomic configuration. Detailed information on the simulation is presented in Experimental Section. The distribution of Θ over 26 cones is displayed in Figure 6b, with the mean value of Θ being 32°. With the help of Θ, the volume and the number of atoms of a cone of any cross-section can be calculated. The extrusions all adopt a double conical shape. The apex angle Θ of each cone is extracted from the radius as a function of the cone's height and is shown in Figure 6c. The number of atoms (N_{contact}) in the point-contact in dimensions (length, 0.85 nm; diameter, 0.75 nm) with the conductance of 16 G_0 is theoretically calculated to be 80.

With the N_{contact} and Equation (4), we predict that the minimal switching-on energy is 0.34 eV (13.1 k_BT at 300 K) when U_1 is 2.12 mV (0.5 mV–(–1.62) = 2.12 mV), as shown in Figure 2d. The minimal energy is about 18.9 times larger than the ultimate limit on the minimum energy per switching at $k_BT\ln 2$ (Landauer's limit, approximately 3×10^{-21} J at room temperature). The maximal energy is estimated to be 3.99 eV (154.2 k_BT at 300 K) when the reduction potential (12 mV–(–12.91) = 24.91 mV) is taken from the switching sequence shown in Figure 2a. However, the projected switching energy of a semiconductor transistor at the technology node of "0.7 eq" is 4.99 eV (193 k_BT, T at 300 K) (Table S1, Supporting Information). Thus, if the atomic-scale tin transistors can replace the Si-based CMOS devices in logic circuits, the energy consumption in the interconnects should be dramatically reduced by at least 400 times or at a maximum

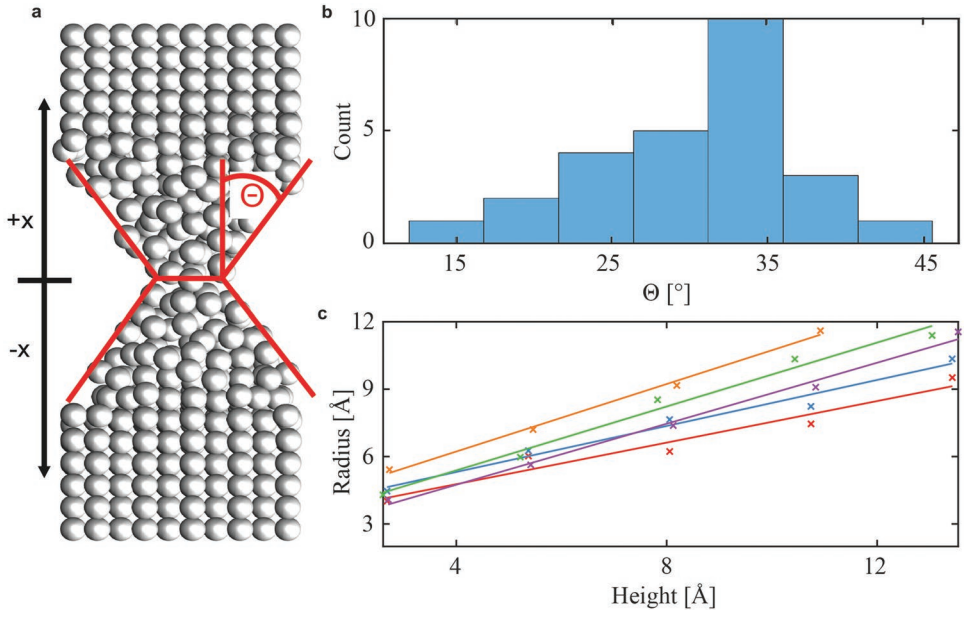

Figure 6. Atomic representation of the tin point-contact with a conductance of 16 G_0. a) The structure consists of an hourglass-shaped filament between two tin bulk electrodes. The red lines highlight the two approximately conical shapes constituting the point contact. b) Distribution of the opening angle Θ. c) "Cone radius versus cone height" for thirteen hourglass filaments with two cones each. The dots refer to the simulated values, while the lines represent the linear fit. The slope of the lines is directly related to the aperture of the cone 2Θ.

of 57 600 times according to the second term in Equation (1). (See Supporting Information).

3.7. Relation between Channel Length and Information Carriers

In the atomic-scale tin transistor, the information carriers are tin atoms. Tin atoms as information carriers are considerably different from electrons or spin due to their natural weight and size. They are physically heavier and more massive. The mass ratio of a tin atom to an electron is 2.18×10^5. The through-barrier-tunneling probability of the information carriers can be estimated using the Wentzel–Kramers–Brillouin (WKB) approximation:[41]

$$p_{\mathrm{WKB}} \approx \exp\left(-\frac{4\pi\sqrt{2m}}{h} \cdot L \cdot \sqrt{E_{\mathrm{b}}} \cdot\right) \tag{6}$$

where m denotes the carrier mass, L the barrier width, and E_{b} the barrier height. Considering both the "classic" over-barrier transition and "quantum" through-barrier tunneling, using atoms as information carriers has apparent advantages for $L < 2.5$ nm.[28] According to the WKB approximation, the tunneling probability of tin atoms through an energy barrier with a height of 1.6 eV and a width of 0.85 nm is exp (–5123.42). For comparison, the tunneling probability of electrons through the same barrier is calculated to be exp (–11.05). Therefore, the tunneling of tin atoms through the gap of 0.85 nm can be ignored. Because of the high conductivity of tin as a metallic material and the low tunneling probability of tin atoms as information carriers, we can reduce the channel length and diameter to the sub-nanometer scale. It has been confirmed both experimentally and theoretically with the DFT that the conductive channel of the atomic-scale tin transistor has geometrical dimensions: a few Å in diameter and ≤ 1 nm in length. In contrast, when the body thickness of silicon is below 5 nm, the mobility (μ) theoretically scales with the sixth power of t_{b} ($\mu \propto t_{\mathrm{b}}^6$) owing to thickness ($t_{\mathrm{b}}$) -fluctuation-induced scattering.[42] The feature poses a critical limit to the continued silicon transistor scaling. The projected channel parameters of a semiconductor transistor at the technology node of "0.7 eq" are 12 nm in length, 10 nm in width, and 5 nm in thickness (See Table S1, Supporting Information).

Unlike the CMOS devices, the bit value is presented by the conductance of the point-contact in the atomic-scale tin transistor. However, in this case, information is easy to be transferred back to electrical current in the electrical domain (quantum resistance to current in microampere), where nearly all of the information processing takes place today. Therefore, the atomic-scale tin transistor fulfills the requirements pointed out by Galatsi et al. on an electronic device as an alternative to the CMOS device.[26] The conductance of the tin point-contact as a physical state variable can reside in two distinguishable on/off states, can be controlled between the on/off states (write) by the gate potential, read by an electrical current through the tin point-contact, transmitted from one physical location to another via the electrical current, and initialized in a defined state (erase) just by setting the gate potential. It has been demonstrated that the conductance of the tin point-contact as a state variable can compete with the thermal noise bath at room temperature. Furthermore, the inner resistance of metallic atomic-scale transistors is ≤ 12.9 kΩ,[12,14] much less than that of molecular electronic devices (in decades MΩ).[43]

3.8. Discussion about Compatibility with CMOS Manufacturing and Design Practices

The footprint of the atomic-scale tin transistors can be reduced by encapsulating a small volume of oxygen-free electrolyte into a cubic nanometer space via nanofluidic[44] and microfluidic techniques.[45] Such an encapsulation makes integrating a vast number of tin transistors into a circuit possible. For example, the devices displayed in Figure S1(a), Supporting Information, can be converted into encapsulated cells by putting a cover layer on the top. A self-sacrification technique can fabricate the channel under the cover. The channel height is only a few decades of nanometers. The channel is closed by electrochemical deposition of tin on both ends of electrodes, and a micrometer-scale cell is produced in the channel limited by a gate electrode and one working electrode.

The conductance variability of the atomic-scale tin transistors at on-state from device to device can be overcome by the preselectable technique,[21] and the current compliance approach is successful in controlling resistive random access memory (RRAM) in the contact-forming phase.[46] The whole resistance of the atomic-scale tin transistors consists of $R_{\mathrm{Interconnect}} + R_{\mathrm{lead\ electrodes}} + R_{\mathrm{Point\text{-}contact}}$. Advanced nanofabrication techniques make it easy to control $R_{\mathrm{Interconnect}} + R_{\mathrm{lead\ electrodes}}$. As demonstrated in Figure 4b, c, the conductance of the tin point-contact has reached hundreds of G_0. Therefore, even $R_{\mathrm{Point\text{-}contact}}$ varies in some range, the variation of the whole resistance can be controlled in some small percentage. To be honest, we think that the switching rate and lifetime are two grant challenges for the fabrication of integrated circuits (ICs) with atomic-scale metallic transistors. Short retrospect of the evolution of MOSFET from conception to very large scale integration (VLSI) may encourage us to face and deal with these grand challenges.[47] Since D. Kahng and M. M. Atalla of Bell Telephone Laboratories reported the first demonstration of a Si-SiO_2 MOSFET in 1960,[48] many innovations and the countless number of perhaps small but indispensable contributions were made to improve the manufacturing techniques of MOSFET by many unsung heroes.[49] Especially the invention and demonstration of the self-aligned planar gate silicon MOSFETs in the late 1960s eliminated the barrier of the conductance variability from device to device in MOSFET and laid the foundation of the semiconductor IC industry.[50] Our research in atomic-scale tin transistors is involved in electronics, electron transport in metallic point-contact, electrochemistry, surface science, micro-and nanofabrication, micro-and nanofluid (in future), and liquid encapsulation (in future). Multidisciplinary efforts should be made to overcome the challenges in conductance variability, switching rate, lifetime, and miniaturization before this novel fundamental switching paradigm can be put forward for application. Our invention has proposed a novel approach to overwhelm the grand challenge of power dissipation in modern digital logic circuits. Therefore, the distinguishing features of the atomic-scale tin transistors and grand challenges in the integration indicate an enormous research space to be explored in investigating atomic-scale metallic transistors as an

alternative to the CMOS devices once we step outside the confines of the established technology for digital logic electronics.

4. Conclusions

In addition to C,[51] Si,[52] Ge,[53] and Pb,[12] Sn is the last one in the fourth main group in the periodic table of elements exploited by us as a working material for transistors. The atomic-scale tin transistor has specifications of low on/off potentials (so low as ≤ 2.5 mV in magnitude), short channel length (≤1 nm), high drain-source current (so high as −375 μA in magnitude), and low dynamic energy (≈154.2 k_BT, 3.99 eV). Furthermore, the on/off potentials are much lower than the constraint on the signal voltage swing (35.8 mV) of CMOS digital logic circuits by Landauer's limit and even smaller than the "action potentials" of neuron fire (−20–100 mV) in magnitude. The low on/off potentials in the atomic-scale tin transistor can reduce the energy consumption in the interconnects of ICs at least ≈400 times by comparison with the digital logic circuits based on the CMOS technology. The conductance at on-states of the bistable configurations has been demonstrated to vary between 1.2 G_0 to 197 G_0. The drain-source current (I_{DS}) at the on-state (197 G_0) reaches −375 μA when the drain-source voltage (U_{DS}) is set at −25 mV. In the atomic-scale tin transistor, tin atoms as information carriers are considerably different from electrons or spins due to their natural weight and size. According to the WKB approximation, the natural weight of tin atoms makes the channel length less than 1 nm. Furthermore, the metallic property of the tin point-contact in the atomic-scale tin transistor ensures high electrical current transport. The low on/off potentials of the transistor depends on the electrochemical characterization of metallic tin. Unlike the CMOS devices, the bit value is presented by the conductance of the atomic-scale tin point-contact in the transistor. Therefore, its information carriers are atoms instead of electrons. On the other hand, the switching frequency of the atomic-scale tin transistor has reached 2047 Hz. There is space to enhance the switching frequency of the atomic-scale tin transistor by optimizing the source, drain, and gate configuration and increasing the electrolyte concentration. Thus, the ultralow-power atomic-scale tin transistor has the potential to serve as an alternative to CMOS for digital logic circuits.

5. Experimental Section

Using Cyclic Voltammetry to Determine the Formal Reduction Potential: Before starting to investigate tin as a working material for atomic-scale metallic transistors, one piece of gold wire with a diameter of 0.25 mm was taken as a working electrode and two pieces of tin wire with high purity (Puratronic, 99.9985%) in diameter of 0.5 mm as counter and quasi-reference electrodes and performed cyclic voltammetry. Within a sweeping range between −120 and 120 mV, the electrochemical potential was scanned reversibly at a rate of 4 mVs^{-1} in the aqueous electrolyte of $SnSO_4 + H_2SO_4$. The cyclic voltammogram is plotted in Figure 2f in the Convention of the International Union of Pure and Applied Chemistry (IUPAC). From the cyclic voltammogram, the cathodic peak potential (E_{pc}) was at −30 mV, and the anodic peak potential (E_{pa}) was at 25 mV. According to cyclic voltammetry, the formal reduction potential ($E^{0'}$) should be equal to $(E_{pa} + E_{pc})/2$.[54] Therefore, the formal reduction potential was determined with this cyclic voltammogram to be −2.5 mV.

Fabricating and Training Atomic-Scale Tin Transistors: Atomic-scale tin transistors were operated electrochemically in an electrochemical cell protected by an inert gas (Ar) environment. Gold (or copper) microelectrodes on thermal oxide silicon wafers (SiO_2 layer in the thickness of 50 nm) shown in Figure S1, Supporting Information, were fabricated with photolithography or e-beam lithography methods. The gap between two gold (or copper) microelectrodes was 2 μm prepared with photolithography or ≈60–160 nm made with e-beam lithography. Because the electrochemical current was in the range of ≈1 nA, a counter electrode was used as a gate instead of two electrodes (reference and counter electrodes) in this case. The gate electrode was made of a tin wire with high purity (Puratronic, 99.9985%) in diameter of 0.5 mm. The two gold (or copper) microelectrodes with a small gap were used as the source and drain. The source electrode was virtually grounded via a trans-impedance circuit. For conductance measurements, a dc U_{DS} was applied to the drain electrode. Only the potential of the gate to the ground was changed. Therefore, the potential differences between the gate, drain, and source were determined through U_{DS} and the gate potential. To fabricate an initial tin point-contact in the gap between the source and drain, potential was applied at 30 mV to the gate and set U_{DS} at −12.9 mV. While tin islands were deposited on the drain and source electrodes, the conductance between the source and drain was monitored continuously. When two of the tin islands on the source and drain met each other in the gap, an atomic-scale tin point-contact was built. After the first tin point-contact formed between the source and drain, the deposition procedure continued for some time to stabilize the tin point-contact.

After the initial stage, the point-contact was opened just by setting the gate potential in the range between −18 and −30 mV. The freshly opened tin point-contact was closed again by setting the gate potential between 2 and 12 mV. The gate potential was changed at a ramping mode in the deposition/dissolution cycling at the ramping rate of 300 mV s^{-1}. The cyclic deposition/dissolution procedure should train the freshly built atomic-scale tin point-contact with the feedback mechanism, similar to the one previously described for the atomic-scale silver and lead (Pb) transistors.[11,12] After the cyclic training procedure, the atomic-scale tin point-contact formed bistable configurations and can perform bistable conductive switching between the source and drain. The sign and the magnitude of the dc voltage (U_{DS}) applied across the source and drain directly influence the growth of the tin point-contact. The three electrodes (gate, source, and drain) and the tin point-contact in the aqueous electrolyte built an atomic-scale tin transistor. The trained atomic-scale tin transistor can implement conductance switching via the feedback mechanism or a virtual function-generator embedded in the NI Labview software.

Microfabrication with Photolithography and E-Beam Lithography: Two masks with patterns for microelectrodes and windows in the insulating layer were prepared with a direct laser writer (Heidelberg Instruments DWL 66). The microelectrodes covered with a SU-8 film on a silicon wafer with a thin thermally oxidized SiO_2 film (50 nm) were fabricated with the photolithography technique in 7 steps. First, a photoresist (AZ 5214E) was spin-coated on the wafer. Second, the microelectrode pattern was transferred to the spin-coated photoresist with a mask aligner. Third, the photoresist film was developed in a developer (MIF 726). Next, Cr/Au (or Cu) (3 nm/40 nm) films were evaporated with an e-beam evaporator (Lesker PVD75). Fourth, the as-evaporated wafer was lifted in a photoresist remover in an ultrasonic bath. Fifth, the wafer with the microelectrodes was spin-coated again with SU-8 in a thickness of 2 μm. Sixth, the pattern with opening windows was transferred to the spin-coated SU-8 film using the mask aligner. Seventh, the wafer with the SU-8 film was developed by a developer (Microposit EC Solvent) and then backed at 210 °C for 1 h to solidify the SU-8 film. Besides the photolithography technique, microelectrodes with gaps between 60 and 160 nm were fabricated with e-beam lithography in Karlsruhe Nano Micro Facility at Karlsruhe Institute of Technology.

Hardware and Software: Under test, the atomic-scale tin transistor was connected to a computer via a homemade electronic device and an A/D card (NI PCI-6221). A dc voltage (U_{DS}) was applied to the drain electrode for conductance measurement. The source electrode was connected to a trans-impedance circuit in the homemade electronic device. The trans-impedance circuit converted the drain-source electrical current in the microampere range to a voltage signal in volt and virtually grounded the source electrode. The voltage signal was readable as an input by the A/D card. The A/D card gave a voltage signal to the gate electrode via the homemade electronic device. The device reduced the magnitude of this voltage signal by N times and gave the output signal in millivolts. To achieve conductance switching of atomic-scale tin transistors, a NI LabVIEW program was developed to control the electrochemical potential applied to the gate, read the voltage signal from the trans-impedance circuit via the A/D card synchronously at a sampling rate of 50 samples s^{-1}, and record the input and output data. The electrochemical gate potential was set using a feedback mechanism. The measured conductance was compared with a preset value of quantum conductance of the atomic-scale tin transistor or by a virtual function-generator (NI Labview software package). The transistor was connected to two computers to realize the fast conductance switching of an atomic-scale tin transistor. In the first computer, a program developed in C on Linux controlled the gate potential and read the voltage from the trans-impedance circuit at a sampling rate of 40 000 samples s^{-1} at maximum via an A/D card (NI PCI 6031E) without the data recording function. A fast program developed in NI LabView in the second computer recorded the gate potential and the voltage signal from the trans-impedance circuit at a sampling rate of 500 000 samples s^{-1} at maximum via an A/D card (NI PCI 6120).

Ab Initio Modeling of the Tin Point-Contact: Two sets of initial structures were prepared. The first set encompassed five bulk structures of the β-phase. Their cross-sections measure was 2.61×2.67 nm^2, and the length was 8.21 nm. The second set consisted of four bulk structures of α-phase of Sn with a cross-section of 2.46×2.67 nm^2 and a length of 6.14 nm. Because of the large size of these simulation boxes, the k-point sampling was restricted to the Γ-point. In all samples, a gap was created to form two separate electrodes, and an hourglass-shaped filament was inserted. Next, the forces on the atoms were minimized. The electrodes were slowly pulled apart in steps of 0.5 Å until the point-contact breaks and then pushed together to re-form the connection to obtain more realistic extrusion geometries. At each step, a force minimization was performed. This process of breaking and re-forming the point-contact was repeated five times. A final structure is illustrated in Figure 6a of the main text.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

F.X. designed and performed the experiments and wrote the whole manuscript except the theoretical part. F.D. performed the theoretical calculation and wrote the theoretical part. M.L. supervised F.D.'s theoretical research. J.L. was the project director from the Werner Siemens Foundation, who discussed and revised the manuscript. M.L. and T.S. were the project co-directors and joined the discussion of the manuscript. F.X. was the subproject leader of Single-Atom Electronics.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

atom-based electronics, beyond complementary metal-oxide-semiconductors, single-atom transistors, sustainability, ultralow-power dissipation

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