Solid-State Marx Generator vs. Linear Transformer Driver: Comparison of Parasitics and Pulse Waveforms for Nanosecond Pulsers

Solid-State Marx Generator vs. Linear Transformer Driver: Comparison of Parasitics and Pulse Waveforms for Nanosecond Pulsers

Raffael Risch and Juergen Biela
Laboratory for High Power Electronic Systems, ETH Zurich
rischr@ethz.ch
http://www.hpe.ee.ethz.ch

***Abstract*—Wide bandgap devices are increasingly used in novel pulse modulator designs, especially for applications requiring nanosecond pulse widths and a high flat-top stability. For fast pulse generator designs, mainly two topologies have been investigated in recent years: Solid-state Marx generators and linear transformer drivers. In both concepts, the mounting space of the mechanical assembly – mainly determined by the required isolation distances – results in stray inductances and capacitances, which significantly influence the pulse shape of the generator. While various designs and measurements of the two topologies have been presented in literature, a detailed discussion and comparison of the parasitics is missing. This paper presents the calculation and comparison of the parasitics based on analytic equations and 3D FEM simulations. The obtained values are then related to equivalent circuits, which are used for transient simulations of the pulse waveforms.**

***Index Terms*—Solid-state Marx generator (SSMG), linear transformer driver (LTD), nanosecond pulses, parasitic modelling**

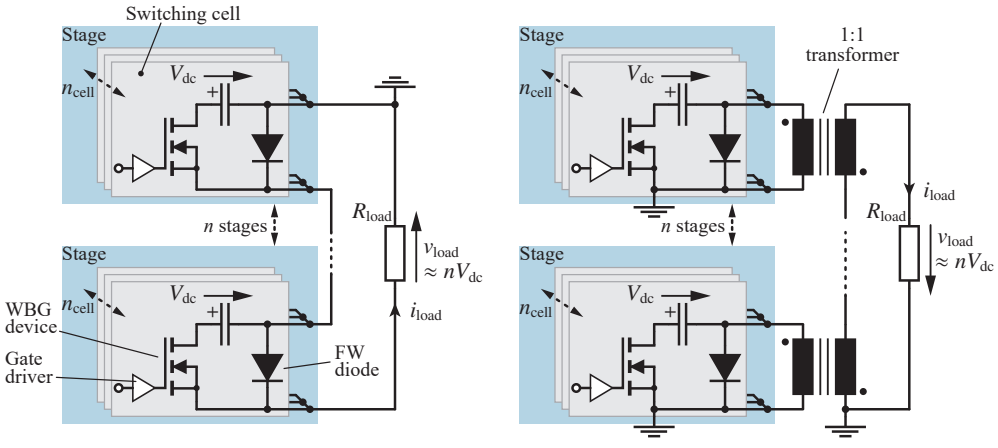
I. Introduction

In the past, pulse modulators have relied on spark-gap devices in combination with pulse-forming lines/networks for generating nanosecond high-voltage pulses [1], [2]. Besides that, solid-state based systems employing opening diodes or avalanche transistors [3], [4] as well as pulse generator designs based on magnetic pulse compression [5] are capable of achieving nanosecond voltage pulses. However, these type of pulse sources have several drawbacks such as limited controllability, short lifetime, and limited availability of system components.

On the other hand, wide bandgap (WBG) semiconductor devices, such as gallium nitride HEMTs or silicon carbide (SiC) MOSFETs, have shown continuous improvement in reliability and performance in recent years [6]. They have been increasingly used in novel medium-voltage converters and fast pulse generators due to their relatively high breakdown voltage and their fast switching speed.

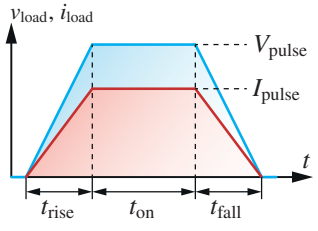
The maximum blocking voltage of commercially available SiC MOSFETs is currently limited to 1.7 kV. Thus, either a series-connection of switches in combination with a high-voltage capacitor bank or a topology with multiple low-voltage switching cells connected in series is required to generate pulse amplitudes of several kilovolts.

Whereas series-connected switches are prone to transient overvoltages due to variations in device characteristics and unsynchronized gate drive voltages [7], topologies based



(a) (b)

	Cell	System
V_{pulse}	800 V	5 kV
I_{pulse}	100 A	100 A
t_{on}	30 ns	30 ns
t_{rise}/t_{fall}	< 5 ns	< 5 ns



(c)

Fig. 1: Investigated topologies for generating unipolar, flat-top pulses for resistive loads: (a) SSMG and (b) LTD. Both topologies consist of n series-connected stages, each having n_{cell} switching cells connected in parallel. (c) Target specifications for the specific designs.

on multiple switching cells are more reliable because the maximum device voltage is clamped/limited by the dc-link capacitors of the switching cells. In addition, the free-wheeling diodes of the switching cells bypass the switch in case of a switch failure, which further increases the reliability of the pulse generator.

For fast pulse applications, mainly two topologies based on switching cells have been investigated: Solid-state Marx generators (SSMG) [8]–[11] and linear transformer drivers (LTD) [12]–[14] (also called inductive voltage adder). Depending on the load conditions and the specific pulse specifications, several variants of the two topologies exist [15], [16]. In this paper, the focus is on the generation of unipolar flat-top pulses for resistive loads, as for example stripline kicker magnets in particle accelerator systems [17]. The investigated topology variants are shown in Fig. 1(a), respectively Fig. 1(b). The target specifications are depicted in Fig. 1(c). The switching cells of the topologies typically consist of a single switch with a dedicated gate drive circuit, free-wheeling diodes, and capacitors as energy storage devices. By choosing sufficiently large capacitance values for the capacitors, the discharge time constant of the capacitors is significantly larger than the pulse width. Accordingly, the capacitors are only slightly discharged during the pulse generation and the capacitor voltages remain approximately constant. As a result, rectangular-shaped voltage pulses can be generated at the output of the generator.

In SSMGs, the capacitors of all n stages are connected in series during the pulse generation, which results in an output voltage $v_{\mathrm{load}} \approx nV_{\mathrm{dc}}$. The electrical potentials of the stages are determined by the series-connection of the capacitors. Accordingly, a transient isolation of the signal control and the power supply of the stages is necessary.

In LTDs on the other hand, each stage forms a primary winding around a magnetic core. A single secondary winding encloses all n cores, whereby the magnetic fluxes in the cores are summed up in the secondary winding. As a result, a voltage $v_{\mathrm{load}} \approx n\mathrm{d}\Phi/\mathrm{d}t = nV_{\mathrm{dc}}$ is induced in the secondary winding, which corresponds to the output voltage of the LTD. In principle, this arrangement can be described by n 1:1 transformers, which have their secondary sides connected in series. On the primary side, all stages can be referenced to the same electrical potential. Therefore, an isolation of the signal control and the power supply is in principle not necessary.

At very fast switching transients, the output voltage pulse shape is greatly influenced by the parasitics of the pulse generator. In this regard, the mechanical assembly of the topologies is a crucial part of the design process, because a significant amount of electromagnetic energy is stored between the conductors of the mechanical assembly. In an ideal case, the pulse distortions can be completely avoided by designing perfectly impedance-matched transmission-lines between the dc-link capacitors and the output of the pulse generator. In addition, package inductances and junction capacitances of the employed components on the stages also influence the pulse performance. Whereas the junction capacitances are primarily determined by the size of the semiconductor chips, and thus by the current rating of the semiconductor devices, the influence of component packages can be minimized by using low-inductive device packages.

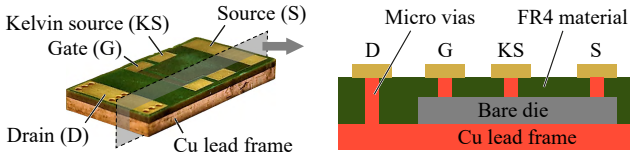


Fig. 2: SiC MOSFET die embedded in a low-inductive PCB-package.

In order to quantify the influence of the parasitics on the pulse shape, parasitic models are required. Models based on transient FEM simulations or transmission line equations [18] usually have a high model complexity and relatively long simulation times. Therefore, this paper describes models for both topologies based on lumped inductances and capacitances. In this way, the model complexity is significantly reduced while still achieving a sufficiently high model accuracy. The parasitics are calculated analytically, which establishes a direct link to the geometry and material parameters. Furthermore, the lumped modelling approach allows to easily combine the parasitics of the mechanical design with circuit-based models of semiconductor devices. This enables a more realistic modelling of the switching transients.

While various designs and measurements of the two topologies have been presented in literature, a detailed discussion and comparison of the parasitics and the switching curves is missing. Therefore, in the second part of this paper, the derived models are used to compare the values of the parasitics and the resulting switching curves of the two topologies. The aim is to identify the topology, with which faster switching transients can be achieved.

Section II describes the coaxial mechanical assembly of the SSMG and the LTD. Thereafter, section III explains the lumped modelling of the mechanical structure of both topologies. Subsequently, section IV describes the modelling of the components on each stage. The design of the systems for the given target specifications is outlined in section V. In section VI, the parasitic values of the designed systems are extracted and the lumped circuit models of the mechanical structures are validated by transient FEM simulations. In addition, the resulting voltage waveforms are discussed.

II. Coaxial Assembly & Parametrization

Both topologies are designed as coaxial mechanical structures, which are schematically illustrated in Fig. 3(a), respectively in Fig. 3(d). The n stages, in the form of printed circuit boards, are stacked on top of each other and are vertically aligned. A centrally placed conductor is electrically connected to the lowest stage and transmits the electromagnetic pulses, generated by the switching cells, to the output at the top end of the assembly. The characteristic impedance of the mechanical assembly can be adjusted by changing the radial dimensions of the geometry. This allows the impedance of the pulse generator to be matched to the load impedance, thus

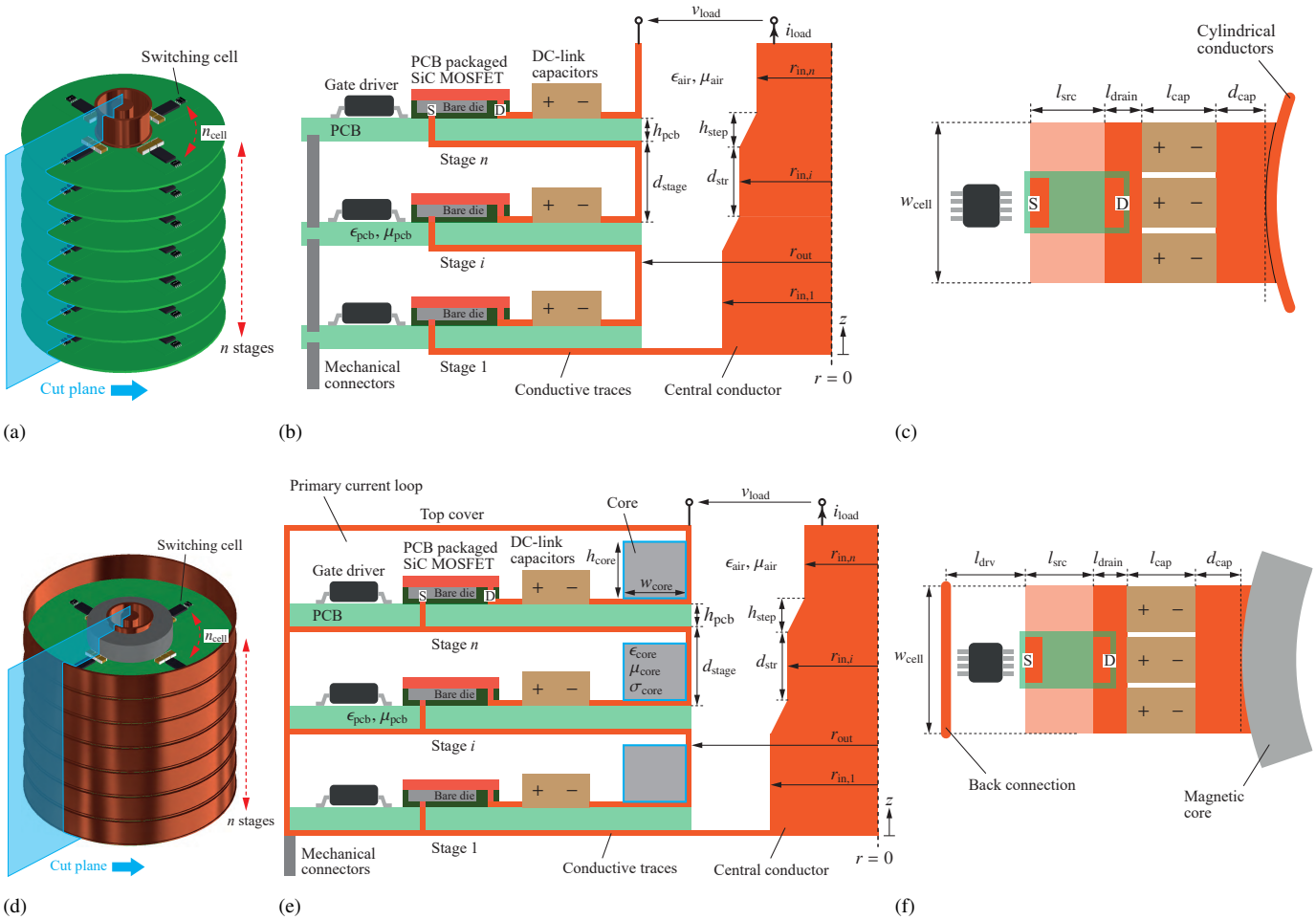


Fig. 3: Mechanical design and parametrization of (a)–(c) SSMG and (d)–(f) LTD. (a),(d) CAD drawing of mechanical design. The top cover of the LTD is removed for better visualization. (b),(e) Parametrization of cross section. (c),(f) Parametrization of switching cell.

minimising pulse reflections and rise times. By designing the central conductor in a stepped (or conical) shape, a linearly increasing impedance profile of the central structure can be achieved. This generally improves the pulse-forming, which results in shorter rise/fall times of the output pulse [19].

On each stage, n_{cell} switching cells are parallel-connected. The number of switching cells depends on the required load current and the current rating of the switches. The switching cells are coaxially arranged around the central conductor. A switching cell consists of a main switch and its gate driver, dc-link capacitors and free-wheeling diodes. Using low-inductive semiconductor packages, realized for example by embedding the power semiconductor die into a printed circuit board as shown in Fig. 2, guarantees a low magnetic coupling between the power and the gate loop, leading to a faster switching of the power devices.

The parameters of the mechanical structure and the switching cell of the SSMG are shown in Fig. 3(b) and Fig. 3(c). The stages are electrically connected to each other by cylindrical conductors at the outer edge of the coaxial structure.

The parameters of the mechanical structure and the switching cell of the LTD are shown in Fig. 3(e) and Fig. 3(f). Due to the mechanical arrangement of the primary windings, the stages can be directly stacked on top of each other. No electrical insulation is required between the primary-sided stages, allowing the LTD to be designed in a relatively compact way.

III. Parasitic Models of Mechanical Structure

The distribution of the electric and magnetic energy within the mechanical structures is modelled by discrete inductances and capacitances. For this, the mechanical structure of both topologies is subdivided into parallel-plate conductors and concentric cylinders, which is shown in Fig. 4 using the example of the SSMG. The parallel-plate conductors model the layout of the switching cells and the concentric cylinders model the connection between the stages. The electromagnetic energy within these sections is then described using ladder networks of inductances and capacitances.

The number of inductances and capacitances in each ladder network depends on the electrical length and the required accuracy for modelling the pulse propagation. In the presented

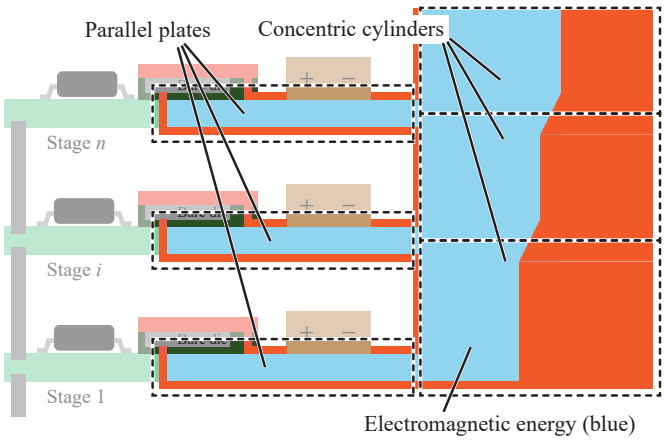


Fig. 4: Geometry of SSMG approximated by parallel-plate conductors and concentric cylinders.

design, the distance between the stages is $d_{\text{stage}} = 20\,\text{mm}$. The space is filled with air, which results in a propagation time of an electromagnetic pulse of approximately 67 ps (propagation velocity in air: $v_{\text{air}} \approx c_{\text{light}}$) for the 20 mm. Analogously, the distance between the dc-link capacitor bank and the central structure is approximately 25 mm, corresponding to a propagation time of 177 ps (propagation velocity in PCB: $v_{\text{pcb}} \approx c_{\text{light}}/\sqrt{\epsilon_{\text{pcb}}}$). Assuming a minimal rise time of the voltage pulses generated by the switching cells of approximately 2 ns, the propagation times are well below 10 % of the rising edge, which is considered to be short enough to accurately model each section by a single pair of inductance and capacitance [20]. This assumption is also validated in section VI.

A. Parasitics of SSMG

In the concentric cylinders, the electromagnetic pulse propagates primarily in the transverse electric magnetic mode, in which the electric and magnetic fields are perpendicular to the z-direction. Hence, per unit length formulas can be used to calculate the total values of the inductances and capacitances.

Assuming a uniform voltage and current distribution along the circumference of the concentric cylinders, (1) and (2) apply for calculating the per unit inductance and capacitance of the straight sections, where the inner radius r_{in} stays constant [21].

$$L'_{\text{str}} = \frac{\mu_{\text{air}}}{2\pi} \ln\left(r_{\text{out}}/r_{\text{in}}\right) \tag{1}$$

$$C'_{\text{str}} = \frac{2\pi\epsilon_{\text{air}}}{\ln\left(r_{\text{out}}/r_{\text{in}}\right)} \tag{2}$$

The stepped sections, in which the inner radius changes linearly, are usually multiple times smaller in height than the straight sections. However, the stepped sections can also be taken into account to further increase the accuracy of the parasitics values. The effective per unit values are calculated by first integrating (1) and (2) along the stepped sections and then dividing the resulting value by the step height h_{step}. This results in equations (3) and (4).

$$L'_{\text{stp}} = \frac{\mu_{\text{air}}}{2\pi} \frac{\ln\left(\frac{r_{\text{out}}}{r_{\text{b}}}\right) r_{\text{b}} - \ln\left(\frac{r_{\text{out}}}{r_{\text{a}}}\right) r_{\text{a}} + r_{\text{b}} - r_{\text{a}}}{r_{\text{b}} - r_{\text{a}}} \tag{3}$$

$$C'_{\text{stp}} = \frac{2\pi\epsilon_{\text{air}} r_{\text{out}} \left[\text{Ei}\left(\ln\left(\frac{r_{\text{out}}}{r_{\text{b}}}\right)\right) - \text{Ei}\left(\ln\left(\frac{r_{\text{out}}}{r_{\text{a}}}\right)\right)\right]}{r_{\text{b}} - r_{\text{a}}} \tag{4}$$

There, r_{a} is the radius at the bottom of the step and r_{b} is the radius at the top of the step. The function "Ei" is the exponential integral function.

Finally, the total inductance and capacitance values of the i-th concentric cylinders are calculated by multiplying the per unit values with the respective heights according to (5) and (6).

$$\begin{aligned} L_i = {} & L'_{\text{str}}(r_{\text{in}} = r_{\text{in},i}) d_{\text{str}} \\ & + L'_{\text{stp}}\left(r_{\text{a}} = \frac{r_{\text{in},i} - r_{\text{in},i-1}}{2}, r_{\text{b}} = r_{\text{in},i}\right) \frac{h_{\text{step}}}{2} \\ & + L'_{\text{stp}}\left(r_{\text{a}} = r_{\text{in},i}, r_{\text{b}} = \frac{r_{\text{in},i+1} - r_{\text{in},i}}{2}\right) \frac{h_{\text{step}}}{2} \end{aligned} \tag{5}$$

$$\begin{aligned} C_i = {} & C'_{\text{str}}(r_{\text{in}} = r_{\text{in},i}) d_{\text{str}} \\ & + C'_{\text{stp}}\left(r_{\text{a}} = \frac{r_{\text{in},i} - r_{\text{in},i-1}}{2}, r_{\text{b}} = r_{\text{in},i}\right) \frac{h_{\text{step}}}{2} \\ & + C'_{\text{stp}}\left(r_{\text{a}} = r_{\text{in},i}, r_{\text{b}} = \frac{r_{\text{in},i+1} - r_{\text{in},i}}{2}\right) \frac{h_{\text{step}}}{2} \end{aligned} \tag{6}$$

As described before, the layout of the switching cells is approximated by parallel rectangular-shaped conductors. The general formula for calculating the loop inductance of a parallel-plate conductor is described in [22]. The respective formula in dependence of the length l of the parallel-plates is given in (7).

For calculating the capacitance of a parallel-plate conductor, the formula described in [23] is applied. The respective formula in dependence of the length l is given in (8).

$$L_{\text{pp}}(l) = \frac{\mu_{\text{pcb}} h_{\text{pcb}} l}{w_{\text{cell}}} \left(\frac{1}{1 + h_{\text{pcb}}/w_{\text{cell}}} + 0.024\right) \tag{7}$$

$$\begin{aligned} C_{\text{pp}}(l) = {} & \frac{\epsilon_{\text{pcb}} w_{\text{cell}} l}{h_{\text{pcb}}} \\ & \cdot \left[1 + \frac{h_{\text{pcb}}}{\pi w_{\text{cell}}} \left(1 + \ln\left(\frac{2\pi w_{\text{cell}}}{h_{\text{pcb}}}\right)\right)\right] \\ & \cdot \left[1 + \frac{h_{\text{pcb}}}{\pi l} \left(1 + \ln\left(\frac{2\pi l}{h_{\text{pcb}}}\right)\right)\right] \end{aligned} \tag{8}$$

Based on the formulas (7) and (8), the parasitics of the switching cell of the SSMG can be calculated based on (9)–(11). The parasitics of the switching cell are described by the loop inductance $L_{\text{p,SSMG}}$ and the two capacitances $C_{\text{n,SSMG}}$ and C_{p}. C_{p} models the space between the drain and source contact of the switch and consequently adds to the value of

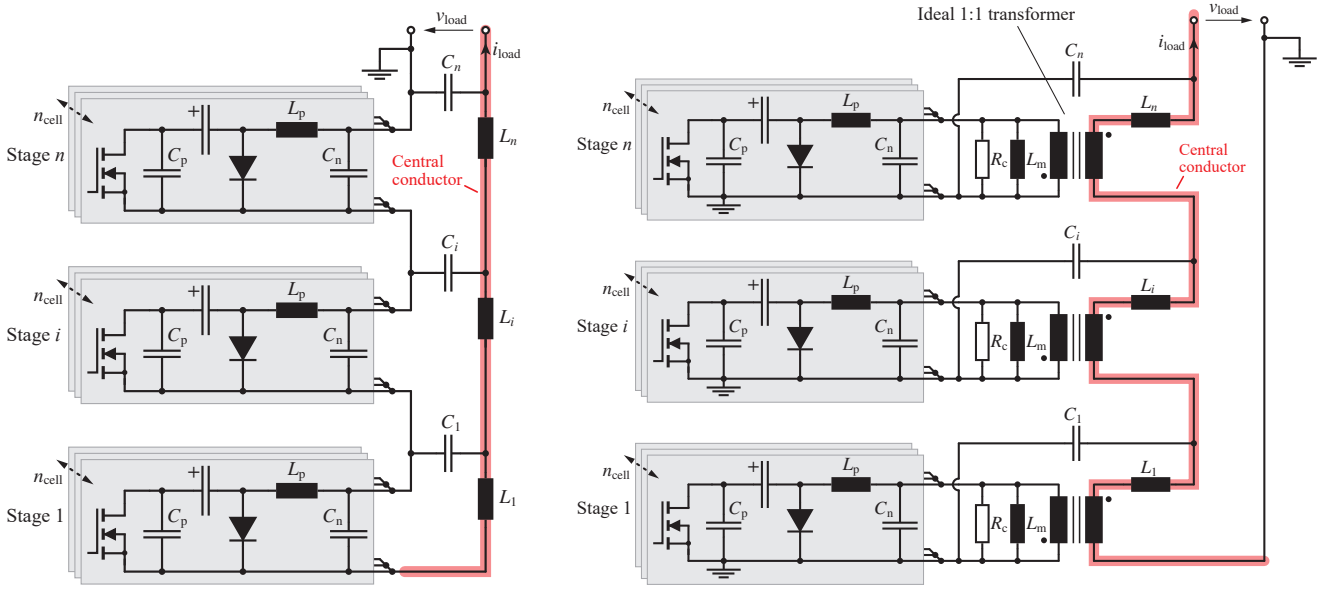


Fig. 5: Circuit models of (a) SSMG and (b) LTD. Each system has n stages in series and n_{cell} parallel-connected switching cells on each stage.

the output capacitance of the switch. C_n models the region between the source contact and the negative potential of the capacitor bank.

$$L_{p,SSMG} = L_{pp}(l = d_{cap} + l_{cap} + l_{drain} + l_{src}) \tag{9}$$

$$C_{n,SSMG} = C_{pp}(l = d_{cap}) \tag{10}$$

$$C_p = C_{pp}(l = l_{drain}) \tag{11}$$

The resulting circuit model, which describes the mechanical structure parasitics of the SSMG, is depicted in Fig. 5(a).

B. Power Flow Description of LTD

The primary and secondary windings of the LTD with the corresponding current paths of i_{prim} and i_{sec} are schematically shown in Fig. 6(a). The secondary winding encloses all primary windings and is electrically connected to the primary windings along the outer part of the housing. Due to this arrangement, the primary currents i_{prim} and the secondary current i_{sec} cancel each other out along the outer part of the housing, except for the magnetising current i_m. The current distribution illustrated in Fig. 6(b) results, in which the magnetizing current i_m flows along the primary windings and the load current $i_{load} = i_{sec}$ flows along the inner part of the structure (main current path).

The resulting behaviour of the LTD no longer represents that of a classical transformer in which the primary and secondary windings are clearly separated from each other. Rather, the magnetic cores are used to increase the inductance of the alternative current path parallel to the main current path and thus minimize the unwanted current flow via this alternative current path. This concept is explained in more detail in [19].

As a result, unlike alternative mechanical designs presented for example in [24], [25], most of the electromagnetic energy is confined within the central coaxial part of the mechanical structure. Thus, the LTD and the SSMG have a similar distribution of the electromagnetic energy.

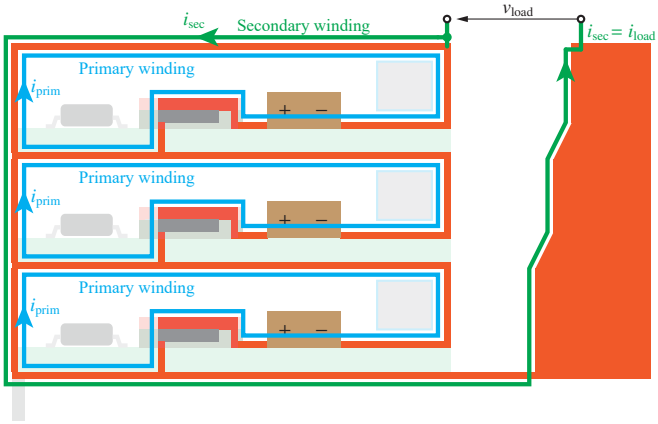
Since the power flow is concentrated in the inner structure, the electrical transmission paths between the dc-link capacitors and the output can be better designed as impedance-matched transmission lines, which improves the pulse-forming.

C. Parasitics of LTD

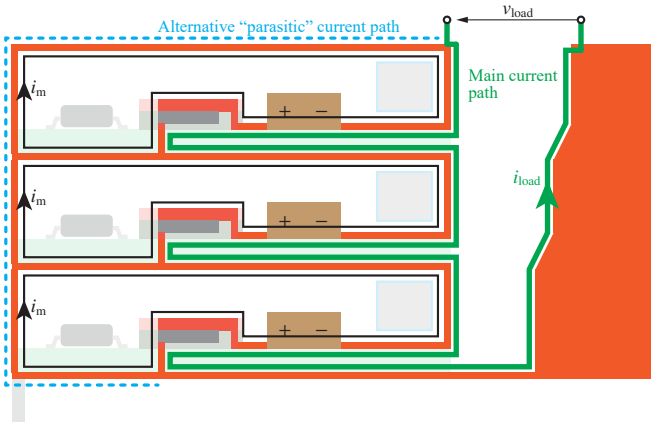
Due to the same load current distribution, the resulting magnetic field within the concentric cylinders is also the same as for the SSMG and consequently, (5) can also be applied to calculate the respective inductance values for the LTD.

Furthermore, each stage of the LTD essentially forms a 1:1 transformer with the section of the central conductor that is directly opposite of the stage at the same height. In general, the electrostatic energy of a two-winding transformer can be modelled based on an equivalent circuit consisting of six capacitances [26], which takes into account the linear distribution of the electric potential along the windings. However, the mechanical arrangement of the primary and the secondary winding of the LTD, allows to simplify the model to a single-capacitance equivalent circuit.

As illustrated in Fig. 7(a), the primary winding and the opposite section of the central conductor are assumed to have a linear distribution of the electric potential. In addition, the potential difference $\Delta\varphi$ along the primary winding and the respective section of the central conductor is the same and corresponds to the dc-link voltage V_{dc}. As a result, the electric



(a)



(b)

Fig. 6: (a) Primary winding currents i_{prim} and secondary winding current i_{sec} of LTD. (b) Resulting current paths. The magnetizing currents i_{m} flows along the primary windings. The load current i_{load} flows along the main current path.

field in the region between is uniform in the azimuthal and the z-direction, and can be modelled by a single equivalent capacitance with the value calculated in (6). These assumptions have been verified by a transient FEM simulation of the electric field in this region, which is shown in Fig. 7(b).

The electric conductor underneath the magnetic core is assumed to be on constant potential yielding a parallel-plate capacitance. The formulas for L_{p} and C_{n} need to be adjusted according to (12) and (13) to take into account the width w_{core} of the magnetic core.

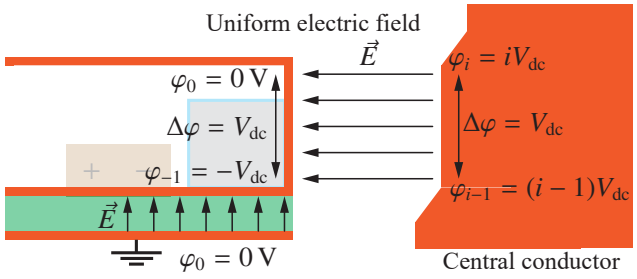
$$L_{\text{p,LTD}} = L_{\text{pp}}(l = d_{\text{cap}} + l_{\text{cap}} + l_{\text{drain}} + l_{\text{src}} + w_{\text{core}}) \quad (12)$$

$$C_{\text{n,LTD}} = C_{\text{pp}}(l = d_{\text{cap}} + w_{\text{core}}) \quad (13)$$

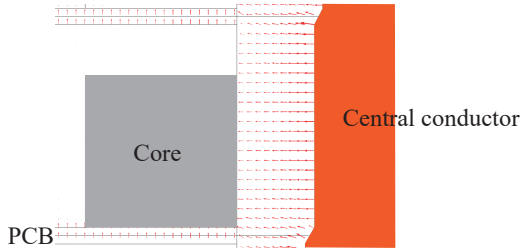
The resulting equivalent circuit of the LTD is depicted in Fig. 5(b).

IV. Parasitic Models of Components

Besides the parasitics resulting from the mechanical structure described in the previous section, the transient switching behaviour of the pulse generator is also influenced by the



(a)



(b)

Fig. 7: (a) Assumption of a uniform electric field between the central conductor and the primary winding due to the same distribution of the electric potential along both conductors. (b) Transient FEM simulation of the electric field of the 5th stage at an output voltage of 5 kV.

package inductances and the junction capacitances of the switching cell components.

The proposed circuit models of the i-th stage of both topologies are depicted in Fig. 8. The parasitics modelled in the previous section are highlighted in blue and the component parasitics in green. The dc-link and auxiliary supply capacitances are modelled by dc voltage sources. The stray inductance of the dc-link capacitors, resulting from the package leads and the internal electrode structure, is modelled by the series inductance L_{esl}. Each stage consist of n_{cell} parallel-connected switching cells.

WBG devices, such as SiC MOSFETs or GaN HEMT, are both unipolar devices and are in theory intrinsically capable of achieving picosecond switching times [27]. However, their device capacitances and internal gate resistance limit the practically achievable switching speed. The respective circuit model is depicted in Fig. 9. The distributed resistance of the gate structure is modelled by $R_{\text{g(int)}}$, the current source i_{ch} models the static behaviour of the drain current and the inductances account for the stray inductances of the package.

The gate driver is typically implemented as a voltage-source driver with buffer capacitors and a half-bridge. The on-state resistance and the finite rise/fall times of the half-bridge increase the charging time of the device's input capacitances and therefore the device's switching speed.

The free-wheeling diode D_{fw} protects the switch from excessive overvoltage stress during turn-off caused by the magnetic energy stored in the commutation inductances and the magnetizing inductance of the LTD. Their voltage-dependent

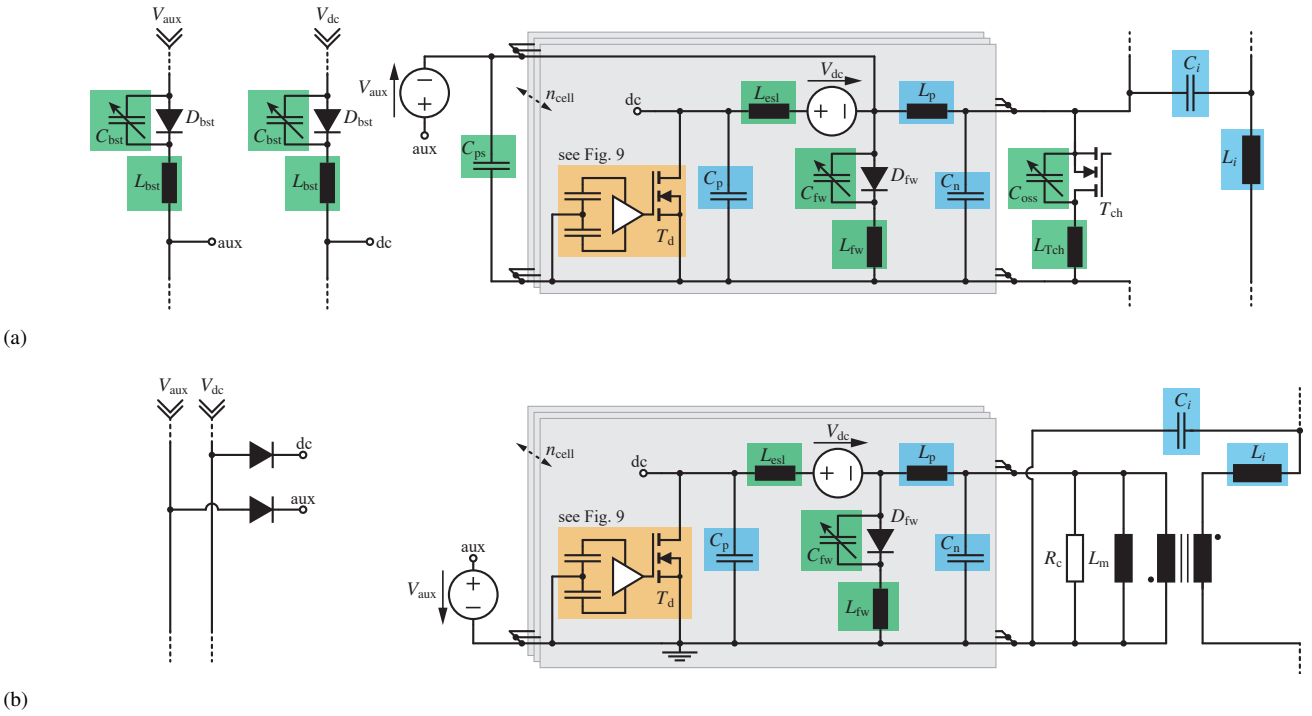


Fig. 8: Circuit models for a single stage of the (a) SSMG, respectively the (b) LTD. Layout parasitics are highlighted in blue, components parasitics in green.

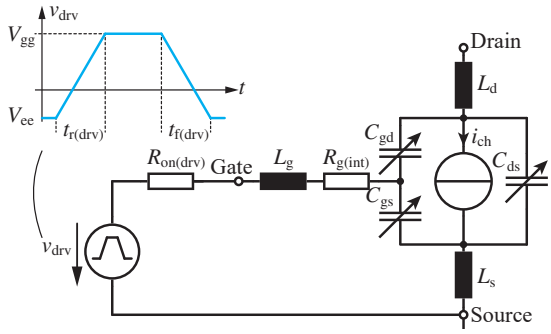


Fig. 9: Circuit model of WBG device based on the inter-terminal capacitances C_{gs}, C_{gd} and C_{ds}.

junction capacitances, which scale with the chip area of the diodes, are also modelled.

The trigger signals for controlling the switches on each stage are isolated by optical fibers, whose isolation capacitances are negligible in relation to the other component parasitics and are therefore neglected.

A. Supply of SSMG

During the pulse generation of the SSMG, the reference potentials of the stages are on elevated electric potentials defined by the series-connection of the dc-link capacitors. Therefore, the charging circuit for the dc-link and the auxiliary capacitors need to be transiently isolated.

A bootstrap charging circuit is used, which consists of two diodes D_{bst}, one for the auxiliary voltage and one for the dc-link voltage, and a charging switch T_{ch}. During the charging cycle, the charging switches T_{ch} are turned on and connect the reference potentials of all stages together. Thereafter, the supply capacitors are charged in parallel through D_{bst}.

The junction capacitances C_{bst} of the bootstrap diodes and the output capacitance C_{oss} of the charging switch add additional parasitic capacitance. However, as opposed to a transformer-based charging circuit, where the primary winding is grounded, the capacitances of the bootstrap diodes are only connected in between stages and not to ground, which significantly reduces the amount of energy that is stored in the parasitic capacitances of the supply during the pulse generation.

Furthermore, the supply of the buffer capacitors for the gate drive circuit of T_d need to be transiently isolated from the source potential of T_d. Isolated dc-dc converters are used to provide the required voltage isolation and the different voltage levels of the buffer capacitors. The isolation capacitance C_{ps}, resulting from the transformer of the dc-dc converter, is included in the model, which is in the range of $C_{ps} = 10\,\text{pF}$ [28].

B. Supply of LTD

In contrast to the SSMG, the stages of the LTD are inductively isolated from each other and the reference potentials of the stages stay on the same potential during the pulse operation. A transient isolation of the supply is not required and the supply capacitors on each stage are charged in parallel. Charging diodes prevent short-circuiting of the dc-link capacitors of parallel-connected switching cells. The

Table I: Geometry and material parameters of the switching cell based on ceramic dc-link capacitors and PCB-package of SiC MOSFET; relevant for calculating L_p, C_p and C_n.

Switching cell dimensions					
h_pcb	1.6 mm	d_cap	5.0 mm	w_cell	12.0 mm
l_src	11.5 mm	l_cap	5.5 mm	l_drain	5.0 mm
PCB material parameters					
ϵ_pcb	$4.5\epsilon_0$	μ_pcb	μ_0		

charging current flows through the dc-link capacitors and back to ground via the free-wheeling diode and the primary winding. Since the charging diodes remain forward biased during the pulse generation, their junction capacitance have no influence on the switching transient.

V. Geometry & Component Design

In the following, example designs for both topologies based on the specifications listed in Fig. 1(c) are presented. These designs have not yet been optimized. Nevertheless, they form the basis for the discussion in section VI.

A. Switching Cell Components

A 1.2 kV/30 A SiC MOSFET is selected as main switch. The SiC MOSFET is embedded in a low-inductive PCB-package, which has dimensions of 14.2 mm×7.5 mm×1.5 mm. Based on the switch's ratings, $n = 7$ stages must be connected in series and $n_\mathrm{cell} = 4$ switching cells in parallel to achieve the specified output voltage and current values. The required dc-link voltage is 720 V and defines the voltage rating for which the other components on the stage have to be designed.

For very short pulse widths, the energy transferred to the load is relatively low. To keep the voltage droop at the load within limits, small capacitance values of the dc-link capacitors are sufficient. For this reason, two 1.0 kV/470 nF multilayer ceramic capacitors in chip packages featuring small equivalent series inductances of $L_\mathrm{esl} = 0.6$ nH are used. The size of the packages is 5.6 mm × 5.0 mm × 4.2 mm.

The dimensions of the switching cell layout is determined by the size of the capacitor bank and the package of the SiC MOSFET. The resulting dimensions are listed in Table I.

The free-wheeling diodes of the SSMG have to absorb the remaining magnetic energy in the stray inductances after the SiC MOSFET turns off. Circuit simulations show that the resulting current peak after turn-off is relatively low (< 2 A). A 1.2 kV/2 A SiC Schottky diode is therefore considered to be sufficient.

On the other hand, the free-wheeling diode of the LTD commutates the whole magnetizing current after turn-off, if no separate reset circuit of the magnetic core is assumed. Based on circuit simulations, a 1.2 kV/5 A SiC Schottky diode is chosen.

Table II: Chosen semiconductor devices for the example designs. The capacitance values are given at the nominal blocking voltage.

SiC MOSFET $T_\mathbf{d}$: Cree CPM3-1200-0075A					
L_d	0.87 nH	C_gs	1388 pF	$R_\mathrm{g(int)}$	9 Ω
L_g	0.90 nH	C_gd	2 pF		
L_s	0.53 nH	C_ds	56 pF		
FW diode of SSMG $D_\mathbf{fw}$: Cree C4D02120E					
L_fw	12 nH	C_fw	8 pF		
FW diode of LTD $D_\mathbf{fw}$: Cree C4D05120E					
L_fw	12 nH	C_fw	20 pF		
Bootstrap diodes $D_\mathbf{bst}$: Cree C4D02120E					
L_bst	12 nH	C_bst	8 pF		
Charging switch $T_\mathbf{ch}$: Cree C3M0350120J					
L_Tch	2 nH	C_oss	20 pF		
Gate driver: IXYS IXD630					
V_gg	18 V	$t_\mathrm{r(drv)}$	10 ns	$R_\mathrm{on(drv)}$	0.6 Ω
V_ee	−5 V	$t_\mathrm{f(drv)}$	10 ns		

B. Supply Components of SSMG

The required current ratings of the bootstrap diodes and the charging switches of the SSMG depend on the pulse repetition frequency. Here, a low repetition rate is assumed, i.e. the focus is on achieving the fastest switching transient for single pulse operation. Accordingly, 1.2 kV/2 A SiC Schottky diodes as bootstrap diodes and 1.2 kV/5 A SiC MOSFETs as charging switches are chosen. The components and their parasitics are listed in Table II.

C. Coaxial Mechanical Structure

The radial dimensions of the central conductor are determined by the electrical isolation and the required system impedance of the generator.

To minimize pulse distortions, the output impedance of the generator must match the characteristic impedance Z_0 of the load. Due to the stepped shape, the different sections of the central conductor have different impedance values $Z_{0,i}$, which can be calculated according to (14).

$$Z_{0,i} = \frac{Z_0}{n-i+1} = \frac{1}{n-i+1}\frac{1}{2\pi}\sqrt{\frac{\mu_\mathrm{air}}{\epsilon_\mathrm{air}}}\ln\left(\frac{r_\mathrm{out}}{r_{\mathrm{in},i}}\right) \tag{14}$$

The electrical field within the coaxial structure is radially directed. The maximum electric field of each section occurs at the surface of the central conductor and is given by (15).

$$E_\mathrm{max} = \frac{V_i}{r_{\mathrm{in},i}\ln(r_\mathrm{out}/r_{\mathrm{in},i})} \tag{15}$$

Thereby, V_i corresponds to the potential difference between the inner and outer conductor of the i-th section.

Table III: Geometry and material parameters of the coaxial structure; relevant for calculating $L_1 \dots L_7$ and $C_1 \dots C_7$.

Coaxial dimensions					
r_{out}	15.0 mm	$r_{\text{in},3}$	10.5 mm	$r_{\text{in},6}$	7.3 mm
$r_{\text{in},1}$	13.3 mm	$r_{\text{in},4}$	9.3 mm	$r_{\text{in},7}$	6.5 mm
$r_{\text{in},2}$	11.8 mm	$r_{\text{in},5}$	8.3 mm		
Vertical dimensions					
d_{stage}	20 mm	d_{str}	d_{stage}	h_{step}	h_{pcb}
Material parameters					
ϵ_{air}	ϵ_0	μ_{air}	μ_0		

The two equations (14) and (15) determine the design space for feasible radii of the central conductor and the outer radius. In addition, the outer radius has to be chosen large enough, such that the n_{cell} switching cells can be placed along the outer circumference of the central structure. The lower boundary is given by (16).

$$r_{\text{out}} \geq \frac{w_{\text{cell}}}{2\sin(\pi/n_{\text{cell}})} \tag{16}$$

In general, the distance between two stages should be kept as short as possible to minimise the overall height of the mechanical structure. This reduces the electrical length and thus helps to avoid problems with pulse distortions due to mismatched impedances. The minimum stage height is limited by the height of the components on the PCBs. In case of the LTD, the magnetic core height must also be taken into account. Depending on the pulse width and the required core cross section, the core can be higher than the other components on the PCBs and therefore determine the necessary distance between the stages. For the given specifications, the core height is smaller than the largest component height. Consequently, the stage height for both topologies is determined by the component heights and is chosen to be $d_{\text{stage}} = 20\,\text{mm}$. The resulting geometrical values are listed in Table III.

D. Magnetic Core

The short voltage pulses that are applied to the magnetic core of the LTD lead to high magnetization rates $\mathrm{d}B/\mathrm{d}t$. As a result of the electrical conductivity of the core, eddy currents are induced, which lead to a decreased magnetizing inductance and increased core losses. Nickel-zinc (NiZn) ferrites are characterised by good high-frequency properties, which is why this material is chosen. The high electrical resistivity of the material is offset by the relatively low saturation flux density and low permeability compared to, for example, nanocrystalline tape wound cores. However at high magnetization rates, nanocrystalline tape wound cores can have the problem that the induced voltage in the individual ribbons exceeds the insulation strength of the ribbons. This can lead to local short circuits, which in turn increases the core losses.

The required core area depends on the allowed magnetic flux swing ΔB of the magnetic material (determined by the saturation and the remanence flux density of the material). In case of ferrites, the core area A_{core} for a unipolar core excitation is calculated according to (17).

$$A_{\text{core}} = \frac{\alpha V_{\text{dc}}\left[t_{\text{on}} + 1/2(t_{\text{rise}} + t_{\text{fall}})\right]}{\Delta B} \tag{17}$$

There, $\alpha = 1.5$ is an additional safety factor to avoid saturation of the core material.

Table IV: Core material parameter of NiZn 4F5.

Core dimensions			
h_{core}	15 mm	w_{core}	15 mm
Core material parameters			
ΔB	150 mT	ϵ_{core}	$5\epsilon_0$
σ_{core}	1 µS/m	μ_{core}	$400\mu_0$
Magnetizing inductance & core resistance			
L_{m}	787 nH	R_{c}	173 Ω

The magnetizing inductance and the core resistance is calculated based on the frequency-dependent complex permeability $\mu = \mu' - \mathrm{j}\mu''$ of the core material. For this, the rising flux transient is converted into an equivalent frequency based on

$$f_{\text{eq}} = \frac{0.35}{t_{\text{on}} + 1/2(t_{\text{rise}} + t_{\text{fall}})} \tag{18}$$

The core inductance and resistance are then calculated according to [29]

$$L_{\text{s}} = \frac{\mu'(f_{\text{eq}})}{2\pi} h_{\text{core}} \ln\left(\frac{r_{\text{out}} + w_{\text{core}}}{r_{\text{out}}}\right) \tag{19}$$

$$R_{\text{s}} = \mu''(f_{\text{eq}}) f_{\text{eq}} h_{\text{core}} \ln\left(\frac{r_{\text{out}} + w_{\text{core}}}{r_{\text{out}}}\right) \tag{20}$$

These values correspond to series parameters and have to be converted to parallel circuit values, resulting in the values for L_{m} and R_{c} listed in Table IV.

VI. Parasitics Calculation & Discussion of Switching Waveforms

In the following, the parasitic inductances and capacitances of the mechanical structure are calculated based on the geometric values in the previous sections and the associated circuit models derived in section III are validated by a comparison with a transient 3D FEM model. Further, the switching transients of both topologies, simulated with the transient circuit models, are discussed.

A. Calculation of Mechanical Structure Parasitics

The parasitics of the mechanical structures are calculated based on (1)–(13). For comparison, the parasitics are also extracted with static FEM simulations, where the inductance and capacitance values are calculated based on the electrostatic and magnetostatic energies. The resulting values are listed in Table V and Table VI.

Table V: Mechanical structure parasitics of SSMG.

Inductances (nH)				**Capacitances (pF)**			
	FEM	Analyt.	Err. (%)		FEM	Analyt.	Err. (%)
L_1	0.58	0.54	6.9	C_1	10.66	10.42	2.3
L_2	1.06	1.03	2.8	C_2	5.27	5.05	4.2
L_3	1.58	1.54	2.5	C_3	3.48	3.37	3.2
L_4	2.09	2.06	1.4	C_4	2.59	2.53	2.3
L_5	2.61	2.57	1.5	C_5	2.06	2.02	1.9
L_6	3.12	3.09	1.0	C_6	1.71	1.68	1.8
L_7	3.48	3.46	0.6	C_7	1.40	1.39	0.7
L_p	3.64	4.10	12.6	C_n	2.27	2.53	11.5
				C_p	6.07	6.90	13.7

Table VI: Mechanical structure parasitics of LTD.

Inductances (nH)				**Capacitances (pF)**			
	FEM	Analyt.	Err. (%)		FEM	Analyt.	Err. (%)
L_1	0.60	0.54	10.0	C_1	10.62	10.42	1.9
L_2	1.09	1.03	5.5	C_2	5.23	5.05	3.4
L_3	1.61	1.54	4.3	C_3	3.45	3.37	2.3
L_4	2.12	2.06	2.8	C_4	2.57	2.53	1.6
L_5	2.63	2.57	2.3	C_5	2.04	2.02	1.0
L_6	3.14	3.09	1.6	C_6	1.70	1.68	1.2
L_7	3.49	3.46	0.9	C_7	1.40	1.39	0.7
L_p	5.53	6.38	15.4	C_n	7.30	8.19	12.2
				C_p	6.07	6.90	13.7

B. Validation of Circuit Models

The circuit models describing the mechanical structure parasitics derived in section III are validated by comparing their output voltage waveforms with the output voltage waveforms of transient 3D FEM models. For this purpose, the mechanical assemblies of both topologies, including the layout of the switching cells, have been modelled in 3D. The FEM model solves the time-dependent partial differential equation given in (21) [30].

$$\Delta \times \mu_r^{-1}(\Delta \times \boldsymbol{A}) + \mu_0 \sigma \frac{\partial \boldsymbol{A}}{\partial t} + \mu_0 \frac{\partial}{\partial t}\left(\epsilon \frac{\partial \boldsymbol{A}}{\partial t}\right) = 0 \qquad (21)$$

This equation is based on the magnetic vector potential formulation of Maxwell's equations, assuming a temporal gauge $\boldsymbol{E} = -\partial \boldsymbol{A}/\partial t$. The material parameters are assumed to be time-independent.

For the considered very short pulse widths, the skin depth is much smaller than the conductor thicknesses and the currents can be approximated by surface currents. Accordingly, the conductors are modelled by electrically conducting boundary layers.

The 3D FEM models are excited by voltage sources that model the series connection of dc-link capacitors and a switch in the switching cells. Lumped input ports are used, which first convert the circuit quantities of the voltage sources into uniform field quantities and then apply these field quantities to the FEM model. The size of the lumped ports is chosen to be the same as the size of the dc-link capacitor banks. By using lumped ports as excitation sources, it is implicitly assumed that the SiC MOSFET is already turned on when the external voltage pulse is applied. Hence, the parasitic capacitance C_p between the drain and source contacts of the SiC MOSFET is already short-circuited and is therefore not taken into account in this validation. The lumped output port is defined at the top of the structure. An infinitely long coaxial cable with a characteristic impedance of $Z_0 = 50\,\Omega$ is connected to this port, which models the cable-connection to an external load.

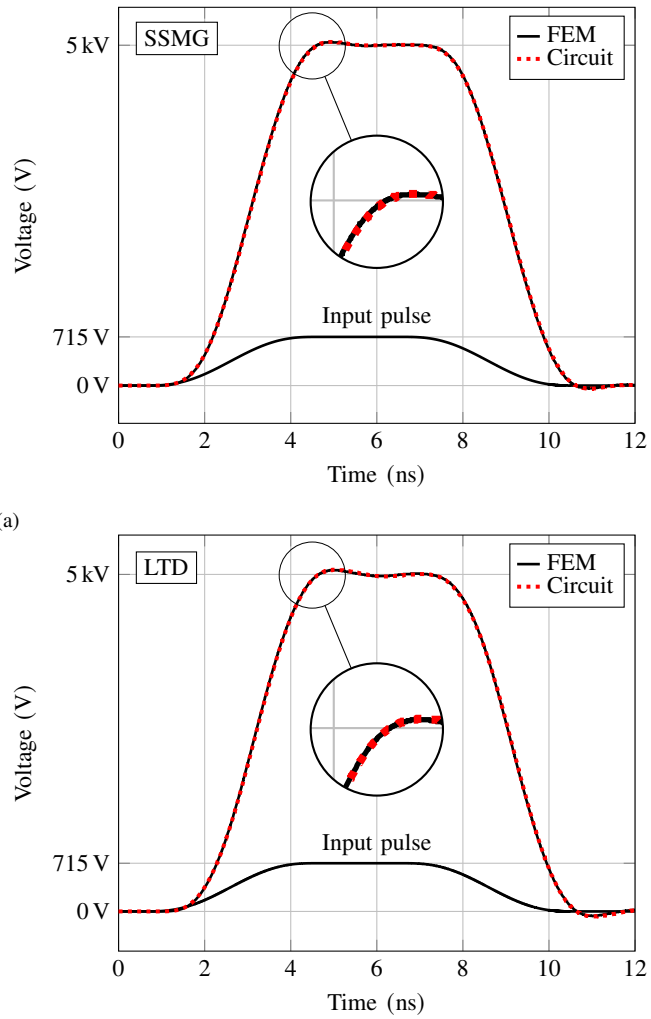


Fig. 10: Validation of circuit models of section III by comparison with transient 3D FEM simulations. The analytically calculated values for the parasitics are used. (a) SSMG, (b) LTD.

For comparing the circuit models with the transient FEM models, the same input voltage pulse with a rise/fall time of 2 ns and a voltage amplitude of 720 V is applied to the models. The analytically calculated values from Table V, respectively Table VI are used in the circuit models. The resulting output waveforms are shown in Fig. 10.

C. Circuit Simulation & Discussion

The discussion of the simulated output voltage waveforms with the transient circuit models of section IV is divided

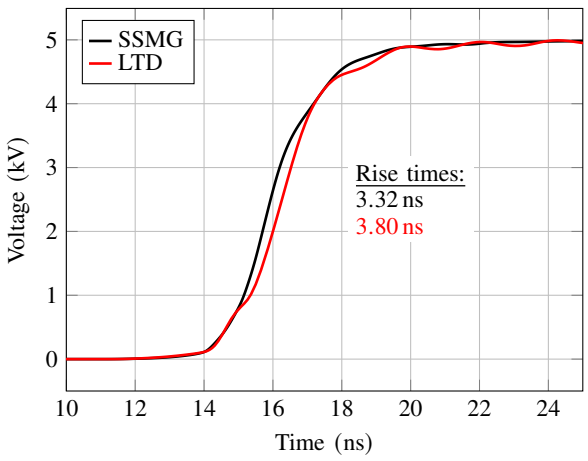


Fig. 11: Circuit simulation of the rising output voltage transients of SSMG and LTD.

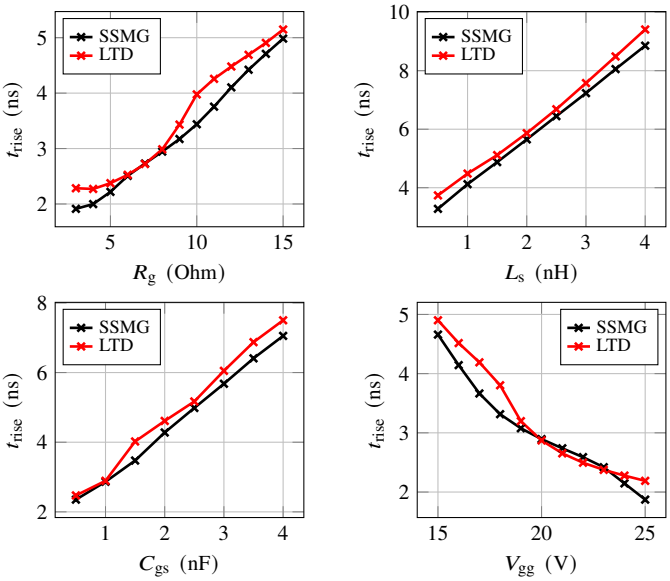


Fig. 12: Sensitivity of t_{rise} to variations in R_g, L_s, C_{gs} and V_{gg}.

between a discussion of the rising transient and the falling transient.

1) Rise Time: The rising transient of the output voltage of both topologies is shown in Fig. 11, showing similar rise times for both topologies.

The output voltage across a resistive load is directly proportional to the load current. The transient load current during turn-on is primarily determined by the MOSFET, which behaves as a current source during this period. The current source behaviour of the MOSFET can be approximately described by $i_{ch} = g_m(v_{gs} - v_{th})$. Thus, the rise time of the load current is primarily influenced by the rise of v_{gs}, i.e. by the charging time of the input capacitance C_{iss} of the MOSFET.

The minimum achievable charging time of C_{iss} is limited by the gate resistance R_g, the source inductance L_s of the package, the value of the input capacitance C_{iss}, and the driving voltage V_{gg}. The sensitivity of the rise time to variations of these parameters is shown in Fig. 12. These parameters are not dependent on the topology. Consequently, both topologies can in general achieve similar rise times.

2) Fall Time: The falling transient of the output voltage of both topologies is shown in Fig. 13. The turn-off transient can be divided into two phases. In the first phase of the turn-off transient, the channel current of the MOSFET goes to zero. This turn-off phase is primarily determined by the same parameters as are dominant during the turn-on transient. Once the channel current is turned off, the resulting circuit represents a passive *RLC* circuit, in which the output voltage fall time is determined by the discharging time of the parasitic capacitances in the circuit. Hence, the parasitic capacitances and the load resistance, i.e. the load current, have a significant influence on the fall time of the output voltage.

In case of the LTD, the magnetizing current helps to discharge the parasitic capacitances and thus can reduce the fall time significantly. This effect is illustrated in Fig. 13, where the circuit has been simulated with a larger magnetizing inductance $L_m = 10\,\mu H$, resulting in a smaller magnetizing

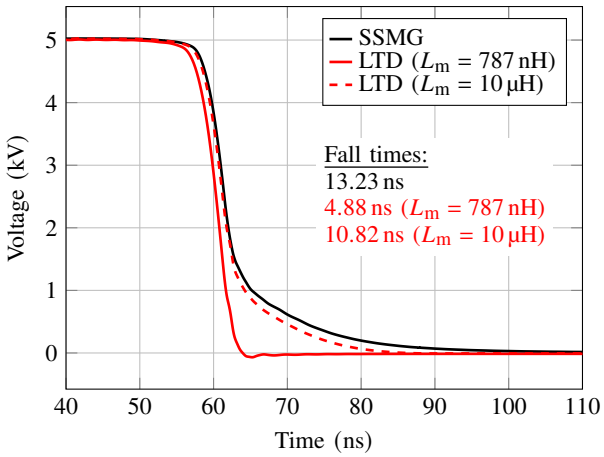


Fig. 13: Circuit simulation of the falling output voltage transients of SSMG and LTD.

current and therefore a larger fall time.

VII. Conclusion

Both topologies, the SSMG and the LTD can be designed in a similar coaxial mechanical assembly. Therefore, the resulting distribution of the electromagnetic energy within the structure is similar and the resulting parasitics of the mechanical structure are comparable for the same geometrical dimensions. This has been analyzed by modelling the stored energy using lumped inductances and capacitances. The values of these lumped parameters are calculated with analytical formulas and are compared with values simulated using FEM, showing in general good agreement. The selected geometry values result in inductance values of less than 7 nH and capacitance values of less than 11 pF. The lumped circuit models have been validated by comparing the circuit-simulated waveforms with

waveforms simulated with transient 3D FEM models of the mechanical structures.

Furthermore, the parasitics originating from the switching cell components and their supply are also modelled. These mainly consist of voltage-dependent junction capacitances of the semiconductor devices and the package inductances. The final discussion indicate that the turn-on times mainly depend on the parasitics of the SiC MOSFET, including its package inductance, and the gate driver. Hence, similar turn-on times below 4 ns can in general be achieved for both topologies.

The turn-off time, on the other hand, is to a large extent determined by the passive discharging time of the parasitic capacitances in the circuit, once the channel current of the SiC MOSFET is completely turned-off. As a result, the turn-off time is significantly longer than the turn-on time. For the SSMG, turn-off times above 13 ns have been simulated. In this regard, a large magnetizing current (small magnetizing inductance) of the LTD can help to reduce the discharging time significantly, resulting in turn-off times below 5 ns.

REFERENCES

[1] T. Huiskamp, E. J. M. van Heesch, and A. J. M. Pemen, "Final Implementation of a Subnanosecond Rise Time, Variable Pulse Duration, Variable Amplitude, Repetitive, High-Voltage Pulse Source," *IEEE Trans. Plasma Sci.*, vol. 43, no. 1, pp. 444–451, Jan. 2015.

[2] L. M. Redondo, A. Kandratsyeu, and M. J. Barnes, "Development of a Solid-State Marx Generator for Thyratron Modulator Replacement," in *Proc. IEEE Eur. Conf. Power Electron. Appl.*, Sep. 2019.

[3] I. V. Grekhov, "Pulse Power Generation in Nano- and Subnanosecond Range by Means of Ionizing Fronts in Semiconductors: The State of the Art and Future Prospects," *IEEE Trans. Plasma Sci.*, vol. 38, no. 5, pp. 1118–1123, May 2010.

[4] T. Heeren, T. Ueno, D. Wang, T. Namihira, S. Katsuki, and H. Akiyama, "Novel Dual Marx Generator for Microplasma Applications," *IEEE Trans. Plasma Sci.*, vol. 33, no. 4, pp. 1205–1209, Aug. 2005.

[5] A. B. J. M. Driessen, F. J. C. M. Beckers, T. Huiskamp, and A. J. M. Pemen, "Design and Implementation of a Compact 20-kHz Nanosecond Magnetic Pulse Compression Generator," *IEEE Trans. Plasma Sci.*, vol. 45, no. 12, pp. 3288–3299, Dec. 2017.

[6] J. O. Gonzalez, R. Wu, S. Jahrdi, and O. Alatise, "Performance and Reliability Review of 650 V and 900 V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7375–7385, Sep. 2020.

[7] C. Yang, Y. Pei, Y. Xu, *et al.*, "A Gate Drive Circuit and Dynamic Voltage Balancing Control Method Suitable for Series-Connected SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6625–6635, Jun. 2020.

[8] L. M. Redondo, J. F. Silva, P. Tavares, and E. Margato, "All Silicon Marx-bank Topology for High-voltage, High-frequency Rectangular Pulses," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2005.

[9] T. Huiskamp and J. J. Van Oorschot, "Fast Pulsed Power Generation With a Solid-State Impedance-Matched Marx Generator: Concept, Design, and First Implementation," *IEEE Trans. Plasma Sci.*, vol. 47, no. 9, pp. 4350–4360, Sep. 2019.

[10] S.-H. Lee, S.-H. Song, and H.-J. Ryoo, "Current-loop Gate Driving Circuit for Solid-state Marx Modulator with Fast-rising Nanosecond Pulses," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8953–8961, Aug. 2021.

[11] J. Ma, L. Yu, W. Sun, S. Dong, L. Gao, and C. Yao, "Investigation and Evaluation of Solid-State Marx Pulse Generator Based on 3-D Busbar," *IEEE Trans. Plasma Sci.*, vol. 49, no. 5, pp. 1597–1604, May 2021.

[12] W. Jiang, "Solid-State LTD Module Using Power MOSFETs," *IEEE Trans. Plasma Sci.*, vol. 38, no. 10, pp. 2730–2733, Oct. 2010.

[13] W. Jiang, H. Sugiyama, and A. Tokuchi, "Pulsed Power Generation by Solid-State LTD," *IEEE Trans. Plasma Sci.*, vol. 42, no. 11, pp. 3603–3608, Nov. 2014.

[14] J. Rao, Y. Zhu, Y. Wang, S. Jiang, and Z. Li, "Study on the Basic Characteristics of Solid-State Linear Transformer Drivers," *IEEE Trans. Plasma Sci.*, vol. 48, no. 9, pp. 3168–3175, Sep. 2020.

[15] Z. Zhong, J. Rao, H. Liu, and L. M. Redondo, "Review on Solid-State-Based Marx Generators," *IEEE Trans. Plasma Sci.*, vol. 49, no. 11, pp. 3625–3643, Nov. 2021.

[16] S. Dong, Y. Wang, J. Ma, *et al.*, "Modular solid-state pulse generator based on multi-turn LTD," *IET Power Electron.*, vol. 13, no. 11, pp. 2342–2349, Aug. 2020.

[17] N. Wang, S. K. Tian, L. Wang, *et al.*, "Impedance optimization and measurements of the injection stripline kicker," *Phys. Rev. Accel. Beams*, vol. 24, no. 3, Mar. 2021.

[18] Y. Hu, F. Sun, J. Zeng, *et al.*, "Circuit Model of Magnetically-Insulated Induction Voltage Adders Based on the Transmission Line Code," *IEEE Trans. Plasma Sci.*, vol. 42, no. 8, pp. 2086–2091, Aug. 2014.

[19] R. D. McBride, W. A. Stygar, M. E. Cuneo, *et al.*, "A Primer on Pulsed Power and Linear Transformer Drivers for High Energy Density Physics Applications," *IEEE Trans. Plasma Sci.*, vol. 46, no. 11, pp. 3928–3967, Nov. 2018.

[20] H. Johnson and M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*. Upper Saddle River, NJ, USA: Prentice Hall, 1993.

[21] D. M. Pozar, *Microwave engineering*, 4th ed. Hoboken, NJ, USA: Wiley & Sons, 2012, p. 53.

[22] A. Letellier, M. R. Dubois, J. P. F. Trovao, and H. Maher, "Calculation of Printed Circuit Board Power-Loop Stray Inductance in GaN or High di/dt Applications," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 612–623, Jan. 2019.

[23] H. B. Palmer, "The capacitance of a parallel-plate capacitor by the Schwartz-Christoffel transformation," *Elect. Eng.*, vol. 56, no. 3, pp. 363–368, Mar. 1937.

[24] J. Holma and M. J. Barnes, "The Prototype Inductive Adder With Droop Compensation for the CLIC Kicker Systems," *IEEE Trans. Plasma Sci.*, vol. 42, no. 10, pp. 2899–2908, Oct. 2014.

[25] D. Woog, M. J. Barnes, A. Ferrero Colomo, J. Holma, and T. Kramer, "First Prototype Inductive Adder for the FCC Injection," in *Proc. IEEE Int. Part. Accel. Conf.*, May 2018.

[26] T. Duerbaum and G. Sauerlaender, "Energy based capacitance model for magnetic devices," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2001.

[27] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*, 2nd ed. Cham, Switzerland: Springer Int. Publishing, 2018, p. 359.

[28] *RA3-242005D 3W Isolated DC/DC converter, Datasheet*, RA3-242005D, Recom Power, Jan. 2022.

[29] R. Hilzinger and W. Rodewald, *Magnetic Materials: Fundamentals, Products, Properties, Applications*. Erlangen, Germany: Publicis Publishing, 2013, p. 117.

[30] *RF Module User's Guide*, version 5.5, COMSOL Multiphysics, Jan. 2022, p. 48.