ETH zürich

ETH Library

Verification and Application of an Analytical Switching Loss Model for a SiC MOSFET and Schottky Diode Half-Bridge

Conference Paper

Author(s):

Hu, Anliang; Biela, Jürgen

Publication date:
2022

Permanent link:
https://doi.org/10.3929/ethz-b-000564428

Rights / license:
In Copyright - Non-Commercial Use Permitted

Originally published in:
https://doi.org/10.23919/ipec-himeji2022-ecce53331.2022.9807184

This page was generated automatically upon download from the ETH Zurich Research Collection.
For more information, please consult the Terms of use.

Verification and Application of an Analytical Switching Loss Model for a SiC MOSFET and Schottky Diode Half-Bridge

Anliang Hu and Jürgen Biela

Laboratory for High Power Electronic Systems (HPE), ETH Zürich, Switzerland

E-mail: hu@hpe.ee.ethz.ch

***Abstract*—This paper investigates the accuracy of a comprehensive analytical switching loss model (*benchmark model*) for a SiC MOSFET and Schottky diode half-bridge over a wide operating range using devices from different manufacturers. The model on average shows an error of 8.63% for turn-on losses and 7.68% for turn-off losses. In addition, the benchmark model is applied to analyze the possible accuracy improvement by using measured device characteristics instead of data sheet information. Furthermore, commonly used assumptions/simplifications in the literature for deriving analytical switching loss models are categorized, and their impact on the accuracy of switching loss models is evaluated based on the benchmark model.**

***Keywords*—SiC MOSFET, Switching losses, Analytical model, Assumption analysis**

I. Introduction

Accurate switching loss models are crucial for optimally designing converter systems, especially when wide band-gap semiconductors are used to achieve a high efficiency and a high power density [1]. The models used in optimization procedures need to be computationally efficient to deliver accurate results within a reasonable time. Therefore, analytical models are usually preferred over physics-based and behavioural models due to their good compromise between accuracy and computational effort [2].

The computational effort of the analytical switching loss models presented in [2]–[12] is simplified by using different assumptions/simplifications, which can be classified into 3 groups based on the analysis given in [3]. The first group approximates the nonlinear device characteristics (e.g. nonlinear capacitances of MOSFETs and Schottky diodes, nonlinear transfer characteristics of MOSFETs). The second group reduces the order of the equivalent RLC circuit, which is solved to calculate the switching losses by a step-by-step switching transient analysis. In order to obtain closed-form analytical equations, the circuit order is mostly limited to two. The third group neglects different parasitic inductances and capacitances from device packages, PCBs, and measurement setups. Until now the analytical switching loss models in the literature have been derived directly based on several of the aforementioned assuptions/simplifications in combination. However, the impact of different assumptions on the accuracy of switching loss models has not been investigated yet.

In order to investigate the impact of different assumptions, [3] proposes a comprehensive and accurate analytical switching loss model for a SiC MOSFET and Schottky diode half-bridge with a wide operating range as a benchmark. The *benchmark model* is based on nonlinear differential circuit equations that are derived including parasitics with few assumptions/simplifications. Fig. 1 depicts the considered equivalent circuit for a hard-switched SiC MOSFET and a SiC Schottky diode half-bridge. In addition, the accuracy improvement by using measured device characteristics instead of data sheet information is investigated in [3], using 3 groups of device parameters including data sheet values (DSV), power device analyzer measurement values (PDAMV), and full measurement values (FMV). Compared to the PDA measurement, the full measurement also includes the dynamic gate-drain capacitance $C_{\mathrm{gd,dy}}$ based on gate charge measurements, the I_{ds}-V_{gs} transfer characteristics during high voltage, high current (HVHI) switching transients, and the measured package parasitic inductances. In [3], it is preliminarily concluded, that the device parameters characterized by static measurements (data sheet information and PDA measurements) are not accurate enough for precisely calculating the switching losses. Instead, $C_{\mathrm{gd,dy}}$ and the I_{ds}-V_{gs} transfer characteristics during HVHI switching transients need to be measured and used. Furthermore, it is also concluded, that group 1 assumptions (approximated nonlinear characteristics) have a larger impact on the switching losses compared to group 2 assumptions (re-

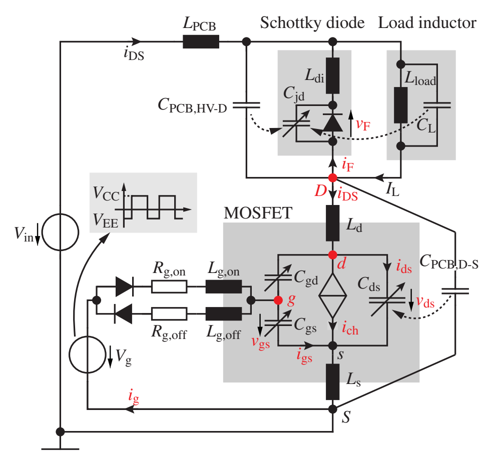

Fig. 1. Hard-switched half-bridge with a SiC MOSFET equivalent circuit, parasitics, a SiC Schottky diode, and an inductive load.

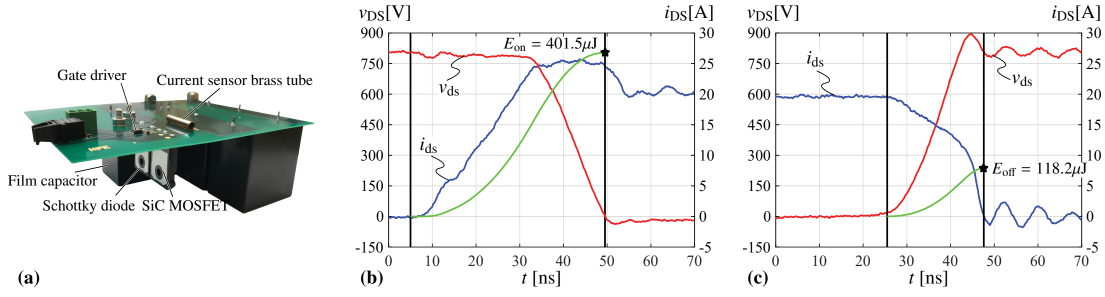

Fig. 2. **(a)** DPT PCB picture. An exemplified measured 800V 20A turn-on **(b)** and turn-off **(c)** waveforms with post-processings.

duced circuit order), where the gate-drain capacitance C_{gd} has the largest influence on the accuracy of switching loss models. However, only one 1.2kV SiC MOSFET is used as device under test (DUT) to verify the model accuracy, and to analyze the aforementioned accuracy improvement and assumption impact problems. Also, only 5 assumptions/simplifications from the first 2 groups are analyzed based on only one operating point at $800\,\text{V}/20\,\text{A}$ for the DUT. In order to draw a more general conclusion, a comprehensive error analysis for more assumptions, operating points, and DUTs is required.

Therefore, this paper comprehensively verifies the accuracy of the benchmark model presented in [3] in a wide operating range for DUTs from different manufacturers under different gate drive circuit conditions. Also, the possible accuracy improvement by using measured device characteristics instead of data sheet information is investigated in detail. In addition, this paper categorizes more assumptions that have been commonly used in the literature and investigates their impact on the accuracy of switching loss models. Finally, guidelines are summarized for selecting different assumptions under different operating conditions to derive simplified and computationally efficient analytical switching loss models.

The paper is organized as follows. Section II verifies the accuracy of the benchmark model and discusses the accuracy improvement by using measured device characteristics instead of data sheet information. In section III, 3 groups of assumptions/simplifications are introduced. Section IV provides insights into the influence of different assumptions on the accuracy of switching loss models with summarized guidelines. Conclusions are drawn in section V.

II. Model Verification

The *benchmark model* proposed in [3] is an accurate analytical switching loss model based on nonlinear differential circuit equations including parasitics. The accuracy results from the fact, that only a few assumptions are used for deriving the equations, and the fact, that device characteristics are measured from the Power Device Analyzer (PDA), impedance analyzer and other measurements. Two most important nonlinear device characteristics, that are measured, are the dynamic gate-drain capacitance $C_{gd,dy}$ based on gate charge measurements and the I_{ds}-V_{gs} transfer characteristics during high voltage, high current (HVHI) switching transients. Measurement procedures for these nonlinear device characteristics are described in [3]. Parasitic inductances from device packages are also measured by an impedance analyzer using the one-port impedance measurement method given in [13]. To comprehensively verify

TABLE I
Switch Diode Pairs with Gate Drive Circuit Conditions

Name	SiC MOSFET	Schottky diode	Gate voltage	External gate resisitor
SDP1	C3M0075120D (Cree, planar gate)	C4D10120H (Cree)	$V_g = [-4, 15]\text{V}$	$R_{g,ext} = 2.7\,\Omega/5\,\Omega/10\,\Omega$
SDP2	SCH2080KEC (ROHM, planar gate)	C4D10120H (Cree)	$V_g = [-3, 20]\text{V}$	$R_{g,ext} = 5\,\Omega/10\,\Omega$
SDP3	SCT3040KLHR (ROHM, Trench gate)	IDWD15G120C5 (Infineon)	$V_g = [0, 18]\text{V}$	$R_{g,ext} = 0\,\Omega/5\,\Omega$
SDP4	SCT50N120 (STMicro, planar gate)	IDWD15G120C5 (Infineon)	$V_g = [-5, 20]\text{V}$	$R_{g,ext} = 2.2\,\Omega/5\,\Omega$

TABLE II
Comparison of Switching Loss Errors (in Percentage)

Test Condition		DSV $\bar{e}_{on}$	DSV $\bar{e}_{off}$	PDAMV $\bar{e}_{on}$	PDAMV $\bar{e}_{off}$	FMV $\bar{e}_{on}$	FMV $\bar{e}_{off}$	Spice $\bar{e}_{on}$	Spice $\bar{e}_{off}$	[4] $\bar{e}_{on}$	[4] $\bar{e}_{off}$
SDP1$_{2.7\Omega}$	$V_{in} = 400\,\text{V}$	15.49	32.63	32.55	44.35	9.61	3.75	13.60	20.07	11.55	34.38
	$V_{in} = 600\,\text{V}$	20.82	33.38	38.81	45.57	8.85	13.64	16.01	25.69	18.34	31.66
	$V_{in} = 800\,\text{V}$	16.43	37.78	26.67	50.43	9.39	13.27	12.90	31.45	17.31	25.51
	average	17.58	34.60	32.67	46.78	9.28	10.22	14.17	25.74	15.74	30.52
SDP1$_{5\Omega}$	$V_{in} = 400\,\text{V}$	10.21	40.19	22.81	49.15	9.90	13.47	13.17	25.38	15.15	18.03
	$V_{in} = 600\,\text{V}$	9.63	44.50	24.46	51.56	9.18	13.88	13.73	29.83	16.78	19.66
	$V_{in} = 800\,\text{V}$	6.47	42.30	23.08	46.14	6.11	10.74	13.79	32.13	17.48	17.10
	average	8.77	42.33	23.45	48.95	8.40	12.70	13.56	29.11	16.47	18.26
SDP1$_{10\Omega}$	$V_{in} = 400\,\text{V}$	29.60	30.57	35.44	38.13	11.52	10.27	27.11	16.99	26.66	40.82
	$V_{in} = 600\,\text{V}$	26.42	32.75	32.05	39.88	10.78	9.43	26.01	24.28	25.77	29.23
	$V_{in} = 800\,\text{V}$	17.78	40.26	23.91	46.73	10.05	9.33	19.31	35.70	18.03	22.28
	average	24.60	34.53	30.46	41.58	10.79	9.68	24.14	25.66	23.49	30.77
SDP2$_{5\Omega}$	$V_{in} = 400\,\text{V}$	40.84	28.78	17.54	19.11	6.39	2.02	26.86	22.33	29.90	23.18
	$V_{in} = 600\,\text{V}$	32.66	23.31	12.77	17.46	4.38	5.44	21.78	19.94	22.51	31.09
	$V_{in} = 800\,\text{V}$	30.63	22.06	12.32	17.31	9.53	7.92	22.28	20.00	22.28	30.19
	average	34.71	24.72	14.21	17.96	6.77	5.12	23.64	20.75	24.90	28.15
SDP2$_{10\Omega}$	$V_{in} = 400\,\text{V}$	24.17	6.19	18.56	9.77	5.59	3.92	19.15	3.34	7.42	71.20
	$V_{in} = 600\,\text{V}$	14.57	1.97	8.09	7.53	2.77	5.72	14.80	2.63	3.48	83.21
	$V_{in} = 800\,\text{V}$	14.37	2.61	8.90	7.31	8.05	8.28	17.96	2.36	5.40	80.06
	average	17.70	3.59	11.85	8.20	5.47	5.98	17.30	2.78	5.43	78.16
SDP3$_{0\Omega}$	$V_{in} = 400\,\text{V}$	111.4	46.38	4.26	22.05	5.85	6.35	32.57	10.35	147.3	134.5
	$V_{in} = 600\,\text{V}$	101.5	52.05	6.14	29.26	11.77	11.85	26.57	10.00	133.0	138.3
	$V_{in} = 800\,\text{V}$	108.2	53.30	15.41	34.32	6.74	11.59	29.13	13.94	138.2	133.9
	average	107.0	50.58	8.60	28.54	8.12	9.93	29.42	11.43	139.5	135.6
SDP3$_{5\Omega}$	$V_{in} = 400\,\text{V}$	85.25	30.40	6.82	13.71	6.62	12.72	37.94	4.65	141.2	104.2
	$V_{in} = 600\,\text{V}$	86.19	32.63	12.61	17.84	8.51	7.84	33.28	5.34	137.4	102.6
	$V_{in} = 800\,\text{V}$	97.52	28.16	23.36	16.46	6.10	4.45	36.69	9.96	146.9	89.82
	average	89.65	30.40	14.26	16.00	7.08	8.33	35.97	6.65	141.8	98.88
SDP4$_{2.2\Omega}$	$V_{in} = 400\,\text{V}$	27.30	28.14	21.13	16.41	13.83	3.08	22.30	20.77	16.38	8.50
	$V_{in} = 600\,\text{V}$	24.14	27.95	22.07	19.13	7.69	5.23	23.21	24.02	7.50	13.76
	$V_{in} = 800\,\text{V}$	27.97	22.64	21.19	14.89	10.60	3.50	28.11	17.73	4.99	9.87
	average	26.47	26.24	21.46	16.81	10.71	3.94	24.54	20.84	9.62	10.71
SDP4$_{5\Omega}$	$V_{in} = 400\,\text{V}$	19.79	30.01	13.15	23.89	14.97	4.75	19.18	19.71	7.99	5.67
	$V_{in} = 600\,\text{V}$	9.68	26.11	9.12	21.44	8.31	2.12	15.43	20.33	13.97	4.44
	$V_{in} = 800\,\text{V}$	2.45	25.10	11.89	22.38	9.86	2.77	11.67	21.38	16.80	7.37
	average	10.64	27.07	11.39	22.57	11.05	3.22	15.43	20.47	12.92	5.82
Total average		**37.46**	**30.45**	**18.71**	**27.49**	**8.63**	**7.68**	22.02	18.16	**43.32**	**48.54**

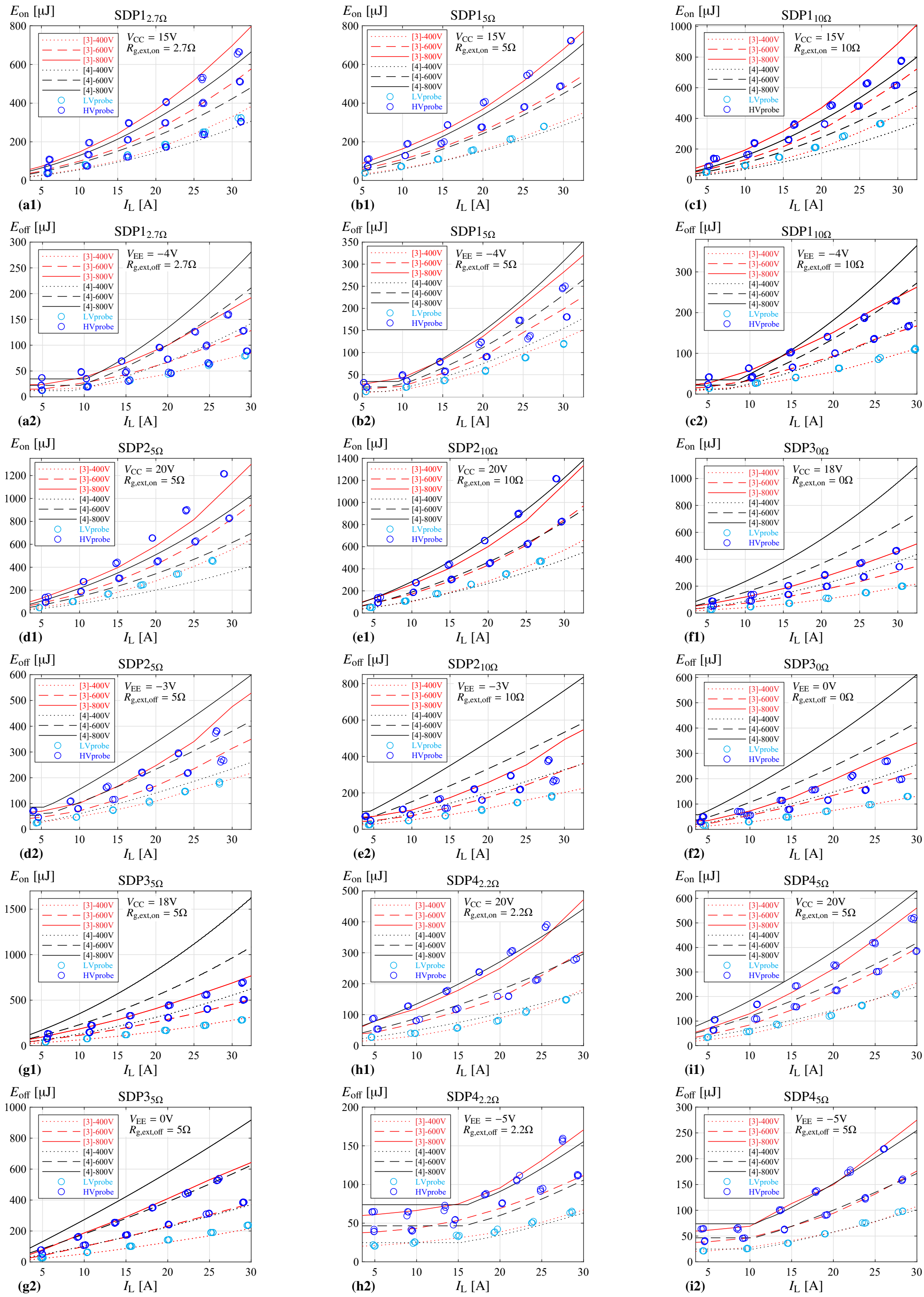

Fig. 3. Switching loss comparison between the benchmark model in [3] (using FMV device characteristics), the re-derived analytical model in [4] (using only DSV), and DPT measurements at different operating points for different SDPs with different gate drive conditions. The de-skew of the voltage and current probe is properly conducted, as supported by the good matching between the LVprobe and HVprobe measurement results for $V_{\text{in}} = 400\,\text{V}$ in **(a1)** and **(a2)**.

the benchmark model, a Double Pulse Test (DPT) setup is designed to measure the drain-source voltage v_{DS} and the drain-source current i_{DS}, as shown in Fig. 2a. The current i_{DS} is measured by a current sensor based on [14], with a $500\,\text{MHz}$ bandwidth and a low insertion inductance ($0.3\,\text{nH}$). The voltage v_{DS} is measured directly at the package pins, using either a low voltage passive probe (Lecroy PP008-1, $400\,\text{V}$, $500\,\text{MHz}$) or a high voltage passive probe (Lecroy PPE6kV, $6\,\text{kV}$, $400\,\text{MHz}$). All switching waveforms are measured with the same laboratory setup and post-processed in the same

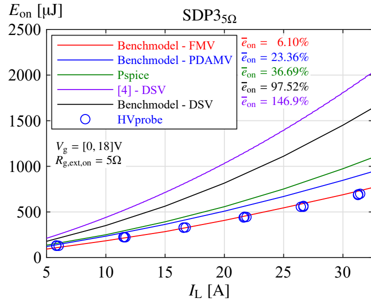

Fig. 4. An exemplified turn-on switching loss comparison ($V_{\text{in}} = 800\,\text{V}$, $\text{SDP3}_{5\Omega}$) between the benchmark model in [3] (using the 3-step: DSV - PDAMV - FMV device parameters), the re-derived analytical model in [4] (using only DSV), Spice simulations and DPT measurements.

manner to calculate the switching losses, with the exemplary $800\,\text{V}/20\,\text{A}$ switching waveforms shown in Fig. 2. For a comprehensive verification, DUTs from different manufacturers with different technologies are selected, which are grouped as 4 Switch Diode Pairs (SDPs) as defined in Tab. I.

Fig. 3 compares the switching loss energies calculated by the benchmark model (based on FMV) and those from the DPT measurements in a wide operating range ($v_{\text{DS}} = [400, 800]\text{V}$, $i_{\text{DS}} = [5, 30]\text{A}$) for different SDPs with different gate drive circuit conditions at room temperature. In addition, the analytical model in [4] is re-derived and implemented to calculate the switching loss energies for the considered Schottky diode and SiC MOSFET half-bridge topology. Tab. II lists the switching loss errors calculated by the benchmark model (based on the 3-step: DSV - PDAMV - FMV device parameters), Spice simulations, and the re-derived analytical model in [4] with respect to the measurement points. For clarity, the $800\,\text{V}$ turn-on switching losses of $\text{SDP3}_{5\Omega}$ are depicted in Fig. 4 to elaborate the error calculation procedure. The mean absolute error is used to evaluate the accuracy, which is defined by

$$\overline{e} = \frac{1}{N}\sum_{n=1}^{N}\left|\frac{E_{\text{n,model/spice}} - E_{\text{n,meas}}}{E_{\text{n,meas}}}\right| \times 100\%. \tag{1}$$

Fig. 3 clearly demonstrates, that the switching losses calculated by the benchmark model match better with measurement results compared to those calculated by the model in [4]. On average, the benchmark model based on the full measurement values has a mean absolute error $\overline{e}_{\text{on}}$=8.63% for turn-on losses and $\overline{e}_{\text{off}}$=7.68% for turn-off losses over a wide operating range, which largely improves the results calculated by the analytical model in [4] with $\overline{e}_{\text{on}}$=43.32% and $\overline{e}_{\text{off}}$=48.54% based only on data sheet information. As can be observed from SDP 2-4 in Tab. II, the accuracy can be already highly improved by using the PDAMV from the individual device characterization instead of the general DSV. However, this is not true for SDP1, which is mainly caused by the smaller internal MOSFET gate resistance $R_{\text{g,int}}$ measured by the PDA compared to the data sheet (C3M0075120D $R_{\text{DSV}} = 9\,\Omega$, $R_{\text{PDAMV}} = 6.5\,\Omega$), since it strongly influences the overlap time between the switching voltage and current. In addition, the switching loss errors of using device characteristics from static measurements (data sheet information, PDA measurements, Spice models from manufacturers) are largely reduced by using those from dynamic measurements (dynamic $C_{\text{gd,dy}}$ based on gate charge measurements and the I_{ds}-V_{gs} transfer characteristics during HVHI switching transients). This results in a reduction from 20-40% to around 8%. Furthermore, not only the nonlinear device characteristics, but also the parasitic inductances from device packages are highly related to the achieved accuracy, which can be observed from SDP3. A bigger common source parasitic inductance from the Spice model compared to the measurement (SCT3040KLHR L_{DSV}=7 nH, L_{FMV}=2.65 nH) results in huge switching loss errors above 50%, even 100%.

As a conclusion, the accuracy of the switching loss model is highly dependent on the adopted device characteristic data. The accuracy increases in general with: DSV $<$ PDAMV $<$ FMV. In addition, based on only DSV without extra device characterization, the benchmark model is more accurate than the model given in [4]. Finally, $R_{\text{g,int}}$ and L_{s} can be relatively easy to measure with an impedance analyzer, which helps to improve the model accuracy compared to using DSV only.

III. Assumptions/Simplifications for Analytical Switching Loss Model Derivation

To study the impact of the assumptions/simplifications on the accuracy of switching loss models, the complete set of nonlinear differential equations (NDE) in [3], which is solved in the time domain to calculate switching losses, is listed below for the equivalent circuit in Fig. 1. The following 9 state variables are used: internal gate-source voltage v_{gs}, gate current i_{g}, MOSFET channel current i_{ch}, internal gate-source current i_{gs}, internal drain-source current i_{ds}, internal drain-source voltage v_{ds}, external drain-source current i_{DS}, Schottky diode forward current i_{F} and Schottky diode forward voltage v_{F}.

$$i_{\text{ch}} = 0 \quad \text{or} \quad i_{\text{ch}} = f_{\text{fit}}(v_{\text{gs}}) \quad \text{or} \quad i_{\text{ch}} = \frac{v_{\text{ds}}}{R_{\text{ds,on}}} \tag{2}$$

$$i_{\text{F}} = g_{\text{fit}}(v_{\text{F}}) \quad \text{or} \quad i_{\text{F}} = C_{\text{jd}}(-v_{\text{F}}) \cdot \frac{\text{d}v_{\text{F}}}{\text{d}t} \tag{3}$$

$$\begin{aligned} V_{\text{CC(EE)}} = {} & R_{\text{g,on(off)}} \cdot i_{\text{g}} + L_{\text{g,on(off)}} \frac{\text{d}i_{\text{g}}}{\text{d}t} + v_{\text{gs}} \\ & + L_{\text{s}} \cdot \left(\frac{\text{d}i_{\text{gs}}}{\text{d}t} + \frac{\text{d}i_{\text{ch}}}{\text{d}t} + \frac{\text{d}i_{\text{ds}}}{\text{d}t}\right) \end{aligned} \tag{4}$$

$$\begin{aligned} V_{\text{in}} = {} & L_{\text{PCB}} \frac{\text{d}i_{\text{DS}}}{\text{d}t} - L_{\text{di}} \frac{\text{d}i_{\text{F}}}{\text{d}t} - v_{\text{F}} + L_{\text{d}} \frac{\text{d}i_{\text{DS}}}{\text{d}t} + v_{\text{ds}} \\ & + L_{\text{s}} \cdot \left(\frac{\text{d}i_{\text{gs}}}{\text{d}t} + \frac{\text{d}i_{\text{ch}}}{\text{d}t} + \frac{\text{d}i_{\text{ds}}}{\text{d}t}\right) \end{aligned} \tag{5}$$

$$i_{\text{g}} = i_{\text{gs}} + C_{\text{gd}}(v_{\text{ds}}) \cdot \left(\frac{\text{d}v_{\text{gs}}}{\text{d}t} - \frac{\text{d}v_{\text{ds}}}{\text{d}t}\right) \tag{6}$$

$$i_{\text{DS}} = C_{\text{gd}}(v_{\text{ds}}) \cdot \left(\frac{\text{d}v_{\text{ds}}}{\text{d}t} - \frac{\text{d}v_{\text{gs}}}{\text{d}t}\right) + i_{\text{ch}} + i_{\text{ds}} \tag{7}$$

$$i_{\text{gs}} = C_{\text{gs}} \frac{\text{d}v_{\text{gs}}}{\text{d}t} \tag{8}$$

$$i_{\text{ds}} = C_{\text{ds}}(v_{\text{ds}}) \cdot \frac{\text{d}v_{\text{ds}}}{\text{d}t} \tag{9}$$

$$I_{\text{L}} = i_{\text{DS}} + i_{\text{F}} \tag{10}$$

TABLE III
ASSUMPTION IMPACT ON THE ORIGINAL BENCHMARK MODEL

	Assumption	Modification	Influenced Interval
Group I	A1.1	replace $C_{gd}(v_{ds})$ in (6), (7) with the fitted data sheet C_{gd}-V_{ds} curve	all
	A1.2	replace $C_{gd}(v_{ds})$ in (6), (7) with a constant charge-equivalent capacitance $C_{gd,Qeq}$ based on data sheet C_{gd}-V_{ds} curve	
	A1.3	replace $C_{gd}(v_{ds})$ in (6), (7) with the two-step piecewise constant capacitance C_{gd} based on data sheet C_{gd}-V_{ds} curve	
	A1.4	replace $C_{gd}(v_{ds})$ in (6), (7) with the fitted PDA measured C_{gd}-V_{ds} curve	
	A2.1	replace $C_{ds}(v_{ds})$ in (9) with the fitted data sheet C_{ds}-V_{ds} curve	all
	A2.2	replace $C_{ds}(v_{ds})$ in (9) with a constant charge-equivalent capacitance $C_{ds,Qeq}$ based on data sheet C_{ds}-V_{ds} curve	
	A3.1	replace $C_{jd}(-v_F)$ in (3) with the two-step piecewise constant capacitance C_{gd} based on data sheet C_{gd}-V_{ds} curve	$I_{on3}, I_{on4}, I_{hoff1},$ $I_{hoff2}, I_{zoff2}, I_{zoff3}$
	A3.2	replace $C_{jd}(-v_F)$ in (3) with a constant charge-equivalent capacitance $C_{jd,Qeq}$ based on data sheet C_{jd}-V_R curve	
	A4.1	replace $f_{fit}(v_{gs})$ in (2) with the fitted data sheet I_{ds}-V_{gs} curve	$I_{on2}, I_{on3},$ $I_{hoff2}, I_{hoff3}, I_{zoff2}$
	A4.2	replace $f_{fit}(v_{gs})$ in (2) with the fitted PDA measured I_{ds}-V_{gs} curve	
	A4.3	replace $f_{fit}(v_{gs})$ in (2) with $g_m(V_{gs} - V_{th})$ using a constant transconductance g_m based on linearized data sheet I_{ds}-V_{gs} curve	
	A4.4	replace $f_{fit}(v_{gs})$ in (2) with the approximated second order equation $\lambda(V_{gs} - V_{th})^2$ based on data sheet I_{ds}-V_{gs} curve	
Group II	A5	change NDE set of interval I_{on1} and I_{hoff1} to: $V_{CC(EE)} = R_{g,on(off)} \cdot i_g + v_{gs}$ $\quad i_g = C_{iss} \cdot dv_{gs}/dt$	I_{on1}, I_{hoff1}
	A6	change (4) to: $V_{CC(EE)} = R_{g,on(off)} \cdot i_g + L_{g,on(off)} \cdot di_g/dt + v_{gs} + L_s \cdot di_{DS}/dt$ change (5) to: $V_{in} = L_{PCB} \cdot di_{DS}/dt - L_{di} \cdot di_F/dt - v_F + L_d \cdot di_{DS}/dt + v_{ds} + L_s \cdot di_{DS}/dt$	all
	A7	change (2) of interval I_{on3} and I_{hoff2} to: $v_{gs} = V_{mil,on(off)} = v_{gs}[t_{2(6)}]$	I_{on3}, I_{hoff2}
	A8	change (3) of interval I_{on1},I_{on2},I_{hoff3},I_{hoff4} to: $v_F = 0$ $\quad$ set $L_{di} = 0$ in (5) change (3) of interval I_{on3},I_{on4},I_{hoff1},I_{hoff2},I_{zoff2},I_{zoff3} to: $i_F = 0$	all
Group III	A9.1	set $L_{g,on(off)} = 0$ in (4)	all
	A9.2	set $L_s = 0$ in (4), (5)	
	A9.3	set $L_{PCB} = 0$ in (5)	
	A9.4	set $L_{g,ext,on(off)} = 0$	
	A9.5	set $C_{PCB,HV\text{-}D} = C_{PCB,D\text{-}S} = C_L = 0$	
	A9.6	set $L_{PCB} = L_{g,ext,on(off)} = C_{PCB,HV\text{-}D} = C_{PCB,D\text{-}S} = C_L = 0$	

Note: Switching interval definition in [3] - Turn-on: I_{on1} turn-on delay + I_{on2} current rise + I_{on3} voltage fall + I_{on4} full gate charging
Hard turn-off: I_{hoff1} turn-off delay + I_{hoff2} voltage rise + I_{hoff3} current fall + I_{hoff4} full gate discharging
ZVS turn-off: I_{zoff2} voltage rise I + I_{zoff3} voltage rise II ($I_{zoff1} = I_{hoff1}$, $I_{zoff4} = I_{hoff4}$)

As mentioned in the introduction, the commonly used assumptions in the literature for deriving analytical switching loss models are categorized into 3 groups as listed below. In a next step, the modifications of the original NDE caused by these assumptions are summarized in Tab. III.

A. Group 1 - Approximated Nonlinear Device Characteristics

A1 MOSFET gate-drain capacitance C_{gd}
- **A1.1** Data sheet C_{gd}-V_{ds} curve [7], [9]
- **A1.2** Constant (charge-equivalent) capacitance $C_{gd,Qeq}$ based on data sheet C_{gd}-V_{ds} curve [4] (multi-step constant in [8])
- **A1.3** Two-step piecewise constant capacitance C_{gd} based on data sheet C_{gd}-V_{ds} curve [5], [6], [10]
- **A1.4** PDA measured C_{gd}-V_{ds} curve

A2 MOSFET drain-source capacitance C_{ds}
- **A2.1** Data sheet C_{ds}-V_{ds} curve [7], [9]
- **A2.2** Constant (charge-equivalent) capacitance $C_{ds,Qeq}$ based on data sheet C_{ds}-V_{ds} curve (multi-step constant in [8])

A3 Schottky diode junction capacitance C_{jd}
- **A3.1** Data sheet C_{jd}-V_R(reverse blocking voltage) curve [7], [9]
- **A3.2** Constant (charge-equivalent) capacitance $C_{jd,Qeq}$ based on data sheet C_{jd}-V_R curve [10] (multi-step constant in [8], constant C_j for the MOSFET body diode in [6])

A4 MOSFET transfer characteristics I_{ds}-V_{gs}
- **A4.1** Data sheet I_{ds}-V_{gs} curve [4]
- **A4.2** PDA measured I_{ds}-V_{gs} curve
- **A4.3** Constant transconductance g_m based on linearized data sheet I_{ds}-V_{gs} curve [5]–[7], [10] (load current I_L dependent in [8]) – $I_{ds} = g_m(V_{gs} - V_{th})$
- **A4.4** Second order $I_{ds} = \lambda(V_{gs} - V_{th})^2$ approximation based on data sheet I_{ds}-V_{gs} curve [9], [15]

B. Group 2 - Reduced Equivalent RLC Circuit Order

A5 Only the step-response of the gate RC circuit (gate resistance R_g and MOSFET input capacitance C_{iss}) is solved instead of the full circuit response during turn-on/turn-off delay intervals [4]–[6], [8], [10].

A6 The voltage drop caused by the gate current i_g on the common source inductance L_s is neglected during current rise/fall intervals [4]–[10].

A7 A constant gate miller voltage is assumed during the voltage rise/fall intervals [4]–[6], [8]–[10].

A8 An ideal Schottky diode is assumed [11] (ideal diode in [5]).

C. Group 3 - Parasitic Inductances and Capacitances

A9 Parasitic inductances and capacitances
- **A9.1** Neglect completely the gate inductance $L_{g,on(off)}$ [4]–[10]
- **A9.2** Neglect the common source inductance L_s [5]
- **A9.3** Neglect the PCB power loop inductance L_{PCB} [5]

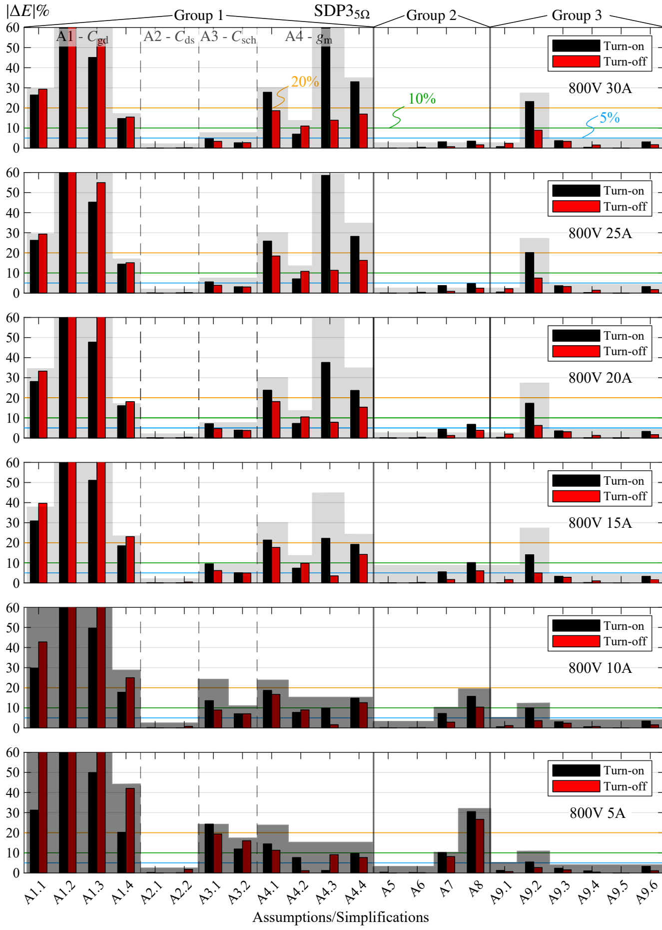

Fig. 5. Turn-on and turn-off switching loss errors for SDP3$_{5\Omega}$ at V_{in} =800 V, I_L =[5,30]A, with assumptions separated into 3 groups. Two different error patterns (light/dark grey) for high/low current regions are highlighted.

A9.4 Neglect the PCB gate loop inductance $L_{PCB,gon(off)}$ [4]–[10]

A9.5 Neglect parasitic capacitances ($C_{PCB,HV\text{-}D}$,$C_{PCB,D\text{-}S}$, C_L) from the PCB and the load inductor [4]–[7], [9]

A9.6 Neglect all external parasitics from the setup (PCB + load inductor) [4], [5]

IV. Impact of Assumptions/Simplifications on Accuracy

The switching loss energies calculated by the benchmark model based on the full measurement values serve as benchmarks. By using different assumptions/simplifications, the NDEs change, as listed in Tab. III, and the resulting switching loss energies are calculated accordingly. The absolute values of the switching energy difference $|\Delta E|$ caused by different assumptions are then divided by the benchmark values, which indicate the impact of different assumptions on the accuracy of switching loss models. A complete group of results with different switching currents from 5 A to 30 A is shown in Fig. 5 for the assumptions mentioned in Section III, with $|\Delta E|\%$ named as *switching loss error* in the following.

Fig. 5 shows, that the switching loss errors caused by different assumptions exhibit a similar pattern in the high current region for I_L=[15, 30] A. However, in the low current region, especially for the ZVS turn-off 5 A operating point, a different pattern appears, which is further validated by Fig. 6 showing two different switching loss error patterns between 30 A and 5 A. After analyzing with different DC link voltages, V_{in} ([400, 800] V) have a negligible influence on the switching loss error pattern. Therefore, the general conclusions below are drawn based on the two different switching loss error patterns at 800 V/30 A and 800 V/5 A, as depicted in Fig. 6. In addition, comparing SDP1$_{10\Omega}$ with SDP1$_{5\Omega}$ or SDP3$_{0\Omega}$ with SDP3$_{5\Omega}$, it can be observed, that R_g has also a negligible influence on the switching loss error pattern.

In Group 1 assumptions, where the nonlinear device characteristics are approximated, the MOSFET C_{gd} (**A1**) has on average the largest impact on the model accuracy, because C_{gd} determines the length of the voltage rise/fall intervals. In general, **A1** assumptions have a larger impact on turn-off than on turn-on, and also a larger impact on hard turn-off than on ZVS turn-off. The impact of **A1** assumptions also varies largely with different DUTs, and none of these assumptions can always lead to the smallest switching loss error compared to the rest of the **A1** assumptions. One possible reason could be, that the C_{gd}-V_{ds} curve is highly nonlinear and the curve fitting is difficult to be accurate. The large error values caused by **A1** assumptions indicate the necessity to use the dynamic $C_{gd,dy}$ [16] based on gate charge measurements [3] in the switching loss model. During gate charge measurements, the current that flows through the channel oxide capacitance $C_{ox,ch}$, which is a part of the gate-drain current i_{gd}, can be captured. On the contrary, this current cannot be captured by the static C_{gd}-V_{ds} curve measurements, because the MOSFET is always in the off-state [16]. However, without extra measurements, **A1.3** (two-step piecewise constant C_{gd}) can be used with typically the best accuracy among **A1** assumptions.

Besides C_{gd}, the MOSFET g_m (**A4**) also has a relatively large impact on the model accuracy in group 1 assumptions, because g_m determines the length of the current rise/fall intervals. In general, **A4** assumptions have a larger impact on turn-on than on turn-off, and also a larger impact on hard turn-off than on ZVS turn-off. Most of the **A4** assumptions lead to $|\Delta E|\%<20\%$, and in the low current region they are typically quite accurate ($|\Delta E|\% < 10\%$). However, for SDP 2-3 **A4.3** (linearized I_{ds}-V_{gs} curve) and **A4.4** (second order approximated I_{ds}-V_{gs} curve) lead to $|\Delta E|\%>20\%$. Therefore, when modeling the switching losses generated in the current rise/fall intervals, the original I_{ds}-V_{gs} curves, either from data sheet (**A4.1**) or PDA measurement (**A4.2**), should be completely included without approximation. In addition, compared to data sheet values, the PDA measured I_{ds}-V_{gs} curve does not further increase much the model accuracy. The impact of g_m on the model accuracy is less than C_{gd}, because the switching losses contributed by the voltage rise/fall intervals dominate the total losses compared to those contributed by the current rise/fall intervals, as validated by Fig. 7. To sum up, **A4.1**

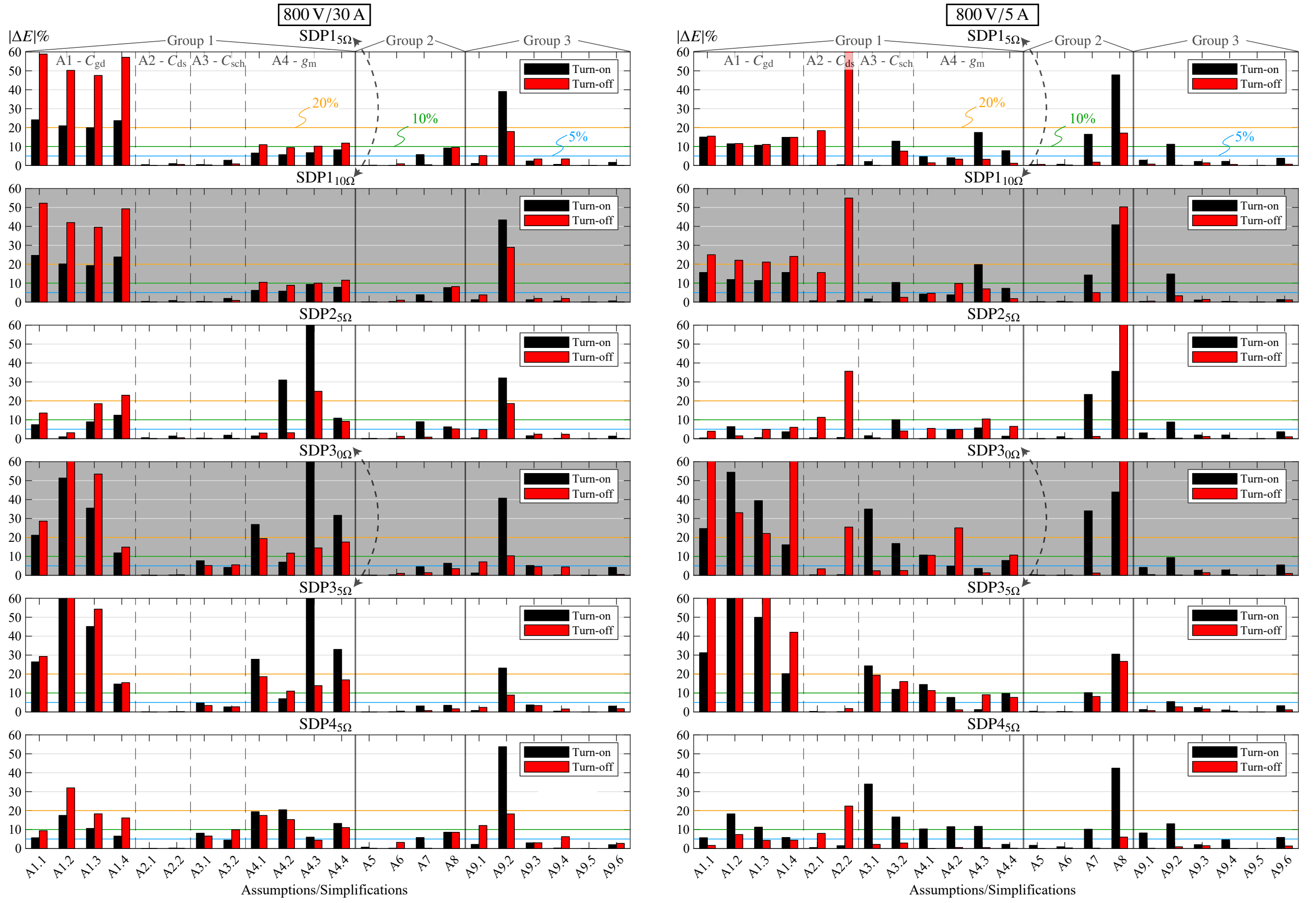

Fig. 6. Turn-on and turn-off switching loss errors for different SDPs with different gate drive circuit conditions at V_{in} =800 V, I_{L} =5/30A. Figures with a grey background are included as control groups to indicate the negligible influence of R_{g} on the switching loss error pattern.

(data sheet I_{ds}-V_{gs} curve) is a relatively accurate assumption to make.

In addition, **A2** (MOSFET C_{ds}) and **A3** (Schottky Diode C_{jd}) assumptions are typically very accurate ($|\Delta E|\% < 5\%$) in the high current region. **A3** assumptions have in general a larger impact on turn-on than on turn-off. However, **A2** assumptions lead to $|\Delta E|\% > 20\%$ for ZVS turn-off in the low current region. It needs to be pointed out, that C_{ds} is usually neglected in the analytical switching loss models from literature, which should be included for ZVS turn-off. Therefore, for an accurate modeling of turn-on and hard turn-off losses, the easier-to-implement **A2.2** (charge-equivalent $C_{\text{ds,Qeq}}$) and **A3.2** (charge-equivalent $C_{\text{jd,Qeq}}$) assumptions can be adopted. However, for ZVS turn-off in the low current region, **A3.2** is still applicable for C_{jd}, but for C_{ds} **A2.2** is not accurate, and with further investigation the two-step piecewise constant C_{ds} assumption should be adopted.

In Group 2 assumptions, where the circuit order is reduced, **A8** (ideal Schottky diode) has the largest impact on the model accuracy and leads to $|\Delta E|\%{>}20\%$. Although Schottky diodes do not have reverse recovery effects, their forward $I_{\text{F}} - V_{\text{F}}$ characteristics and junction capacitances must be included for an accurate switching loss modeling. On the contrary, both **A5** and **A6** are very accurate. **A7** (constant miller voltage) is accurate ($|\Delta E|\%{<}10\%$) in the high current region, but leads to $10\%{<}|\Delta E|\%{<}20\%$ in the low current region. It also has a larger impact on turn-on than on turn-off.

In Group 3 assumptions, where the parasitics are neglected, L_{s} (**A9.2**) has the largest impact on the model accuracy. Instead, all of the remaining parasitic inductances and capacitances can be neglected. However, it needs to be emphasized, that this conclusion is based on the optimally designed PCB with minimal parasitics and the adopted small air-core load inductor (50 µH). If the parasitic capacitance values are not negligibly small compared to the DUT, the parasitic capacitances can be directly added to C_{jd} or C_{ds}, and L_{d} can be easily included in the model, without much more effort.

As a conclusion, in order to derive simplified, computationally efficient yet accurate analytical switching loss models, a guideline is provided in the following.

1) **DSV only**: Without extra measurements, use **A1.3** for C_{gd}. Use **A4.1** (preferred) or **A4.4** for the I_{ds}-V_{gs} transfer characteristics. Use **A3.2** for C_{jd} and use the linearized Schottky diode forward I_{F}-V_{F} curve. Use **A5** and **A6** for model derivation. For turn-on and hard turn-off, use **A2.2** for C_{ds} and **A7** for model derivation. For ZVS turn-off,

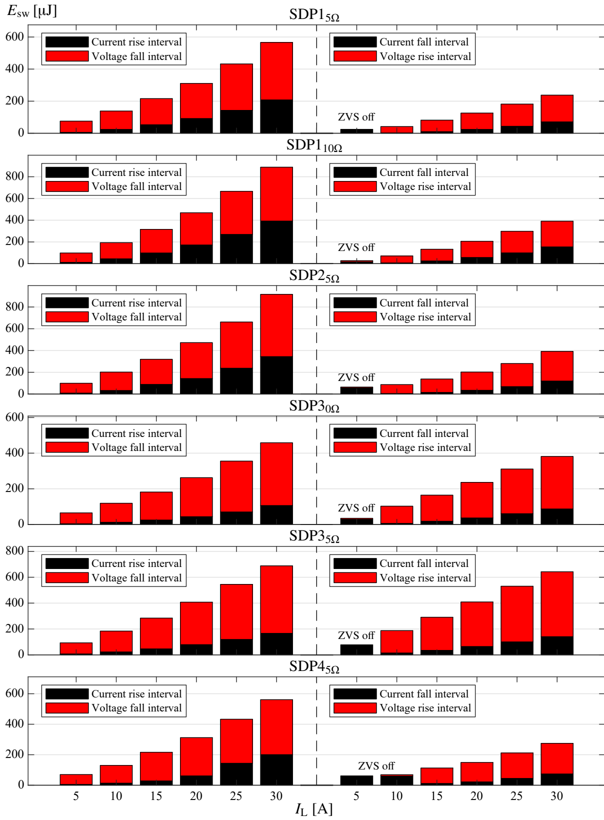

Fig. 7. Turn-on and turn-off switching loss distributions for different SDPs with different gate drive circuit conditions at V_{in} =800 V, I_L =[5,30]A.

C_{ds} must be included (e.g. two-step piecewise constant assumption), and **A7** cannot be used for model derivation. Neglect all parasitics except for L_s, if the PCB is optimally designed. Otherwise, add parasitic capacitances to C_{jd} or C_{ds}, if they are not negligibly small compared to the DUT, and add L_d to the model.

2) **DSV + IA**: If in addition to DSV also simple measurements are performed, use an impedance analyzer to measure the internal MOSFET gate resistance $R_{g,int}$ and L_s, and the model accuracy can be easily improved.
3) **DSV + IA + PDA**: For better model accuracy, characterize the DUT individually with the power device analyzer. Use the device parameters from static measurements, but for C_{gd} use the $C_{gd,dy}$ based on gate charge measurements. Same assumptions (with measured device characteristics) can be adopted as mentioned above.
4) **DSV + IA + PDA + extra**: For even higher accuracy, measure the I_{ds}-V_{gs} transfer characteristics under HVHI switchings and include them into the model.

V. Conclusion

In this paper, the accuracy of the comprehensive switching loss model from [3] for a SiC MOSFET and Schottky diode half-bridge is comprehensively evaluated over a wide operating range using DUTs from different manufacturers with different technologies. On average an error of 8.63% for turn-on losses and 7.68% for turn-off losses results, which is highly improved compared to the analytical model proposed in [4]. In addition, the accuracy of the switching loss model is highly dependent on the adopted device characteristics, and the errors of the switching loss calculation can be largely reduced from around 20-40% to around 8% by using device characteristics from dynamic measurements instead of those from static measurements. Finally, it is concluded, that assumptions for the gate-drain capacitance C_{gd}, the transfer characteristic I_{ds}-V_{gs}, and the common source parasitic inductance L_s have the largest impact on the accuracy of switching loss models. A guideline is also given for selecting different assumptions to derive simplified and computationally efficient analytical switching loss models.

References

[1] J. Biela, J. Kolar, A. Stupar, U. Drofenik, and A. Musing, "Towards Virtual Prototyping and Comprehensive Multi-Objective Optimisation in Power Electronics," in *PCIM Europe*, May 2010.

[2] Yuancheng Ren, Ming Xu, Jinghai Zhou, and F. C. Lee, "Analytical Loss Model of Power MOSFET," *IEEE Trans. on Power Electronics*, vol. 21, no. 2, pp. 310–319, Mar. 2006.

[3] A. Hu and J. Biela, "An Analytical Switching Loss Model for a SiC MOSFET and Schottky Diode Half-Bridge Based on Nonlinear Differential Equations," in *EPE ECCE Europe*, 2021.

[4] D. Christen and J. Biela, "Analytical Switching Loss Modeling Based on Datasheet Parameters for MOSFETs in a Half-Bridge," *IEEE Trans. on Power Electronics*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019.

[5] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd ed. John Wiley and Sons Inc, 2003.

[6] J. Wang, H. S. Chung, and R. T. Li, "Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance," *IEEE Trans. on Power Electronics*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[7] M. R. Ahmed, R. Todd, and A. J. Forsyth, "Predicting SiC MOSFET Behavior Under Hard-Switching, Soft-Switching, and False Turn-On Conditions," *IEEE Trans. on Industrial Electronics*, vol. 64, no. 11, pp. 9001–9011, Nov. 2017.

[8] X. Wang, Z. Zhao, K. Li, Y. Zhu, and K. Chen, "Analytical Methodology for Loss Calculation of SiC MOSFETs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 71–83, Mar. 2019.

[9] S. K. Roy and K. Basu, "Analytical Estimation of Turn on Switching Loss of SiC MOSFET and Schottky Diode Pair From Datasheet Parameters," *IEEE Trans. on Power Electronics*, vol. 34, no. 9, pp. 9118–9130, Sep. 2019.

[10] K. Peng, S. Eskandari, and E. Santi, "Analytical Loss Model for Power Converters with SiC MOSFET and SiC Schottky Diode Pair," in *ECCE*, Sep. 2015, pp. 6153–6160.

[11] X. Li, J. Jiang, A. Q. Huang, S. Guo, X. Deng, B. Zhang, and X. She, "A SiC Power MOSFET Loss Model Suitable for High-Frequency Applications," *IEEE Trans. on Industrial Electronics*, vol. 64, no. 10, pp. 8268–8276, Oct. 2017.

[12] A. Hu and J. Biela, "Evaluation of the I_{max}-f_{sw}-dv/dt Trade-off of High Voltage SiC MOSFETs Based on an Analytical Switching Loss Model," in *EPE ECCE Europe*, 2020.

[13] T. Liu, T. T. Y. Wong, and Z. J. Shen, "A New Characterization Technique for Extracting Parasitic Inductances of SiC Power MOSFETs in Discrete and Module Packages Based on Two-Port S-Parameters Measurement," *IEEE Trans. on Power Electronics*, vol. 33, no. 11, pp. 9819–9833, 2018.

[14] K. Takao and S. Kyogoku, "Ultra Low Inductance Power Module for Fast Switching SiC Power Devices," in *ISPSD*, 2015, pp. 313–316.

[15] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 1st ed. Springer, Boston, MA, 2008.

[16] Z. Dong, X. Wu, H. Xu, N. Ren, and K. Sheng, "Accurate Analytical Switching-On Loss Model of SiC MOSFET Considering Dynamic Transfer Characteristic and Q_{gd}," *IEEE Trans. on Power Electronics*, vol. 35, no. 11, pp. 12 264–12 273, 2020.