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An Analytical Switching Loss Model for a SiC MOSFET and Schottky Diode Half-Bridge Based on Nonlinear Differential Equations

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Keywords
≪Wide bandgap devices≫, ≪Silicon Carbide (SiC)≫, ≪MOSFET≫, ≪Switching losses≫

Abstract
An accurate analytical switching loss model for a SiC MOSFET and Schottky diode half-bridge for a wide operating range is proposed in this paper, which is based on nonlinear differential circuit equations including parasitics. In the model, nonlinear device characteristics are used, including the dynamic gate-drain capacitance and the transfer characteristics measured under real switching conditions. With the proposed model, the accuracy improvement by using measured characteristics instead of device data sheet information is analyzed. In addition, the impact of making different common assumptions/simplifications on the accuracy of switching loss models is evaluated.

1 Introduction
SiC MOSFETs outperform Si power semiconductors in many applications for future energy conversion systems, especially in the medium-voltage-level range, due to the lower conduction and switching losses [1]. As a result, a higher efficiency and a higher power density can be achieved. For optimally designing such systems, an accurate modelling of the switching losses is required [2]. Analytical models are usually preferred over physics-based and behavioural models for converter optimization routines due to their good compromise between accuracy and computational effort, particularly considering the inevitable mass data processing for evaluating different designs over wide operating ranges [3].

Many publications have made endeavors to derive accurate analytical switching loss models for power MOSFETs with clamped inductive loads based on a step-by-step switching transition analysis of their formulated equivalent circuits [2–9]. However, assumptions and simplifications are always made, which inevitably leads to inaccuracies. The assumptions can be classified into two groups. The first group adopts different methods to approximate the MOSFET nonlinear characteristics. Typically, nonlinear MOSFET capacitances are assumed to be constant values (e.g. charge equivalent capacitance [2]), and the transfer characteristic is linearized by a constant transconductance with $i_{ch} = g_m(v_{gs} - v_{gs})$ [3, 4]. The second group simplifies the formulated equivalent circuit equation set to maximally a second order network in order to derive simple closed-form analytical expressions for each time interval of the switching transition. For instance, [3] and [5] solve only the step-response of the gate RC circuit (gate resistance and MOSFET input capacitance) instead of the full circuit response during the turn-on/turn-off delay intervals. In addition, the voltage drop caused by the gate current $i_g$ on the common source inductance $L_s$ is neglected, assuming $i_g$ is much smaller than the drain current $i_d$ during current rise/fall intervals [5–7]. Finally, a constant gate miller voltage is usually assumed during the voltage rise/fall intervals, when $i_g$ is completely used to charge/discharge the MOSFET gate-drain capacitance.

![Fig. 1: Hard-switched half-bridge with a SiC MOSFET equivalent circuit, parasitics, a SiC Schottky diode, and an inductive load.](image-url)
capacitance $C_{gd}$ [2, 5]. Due to these assumptions, the conventional piecewise linear model typically results in roughly 20% turn-on and turn-off loss errors ($\tau_{on}$, $\tau_{off}$) [8]. The switching loss models proposed in [2–9] endeavor to reduce these errors, where an error $\tau_{on}$ of around 5% and an error $\tau_{off}$ of around 10% has been reported in [2] for a SiC MOSFET half-bridge over a wide operating range, only based on data sheet information. However, a possible accuracy improvement by using measured device characteristics instead of data sheet information is not investigated, which is important due to the tolerance between different devices. In [9], $\tau_{on}$ is reduced to roughly 3% by using measured SiC MOSFET characteristic parameters under real switching conditions. However, this small error is only obtained in a relatively small operating range, and the turn-off loss is not modelled. Furthermore, it has not been investigated yet what the impact of different assumptions/simplifications is on the accuracy of switching loss models.

Based on [9], this paper proposes a comprehensive analytical switching loss model, which is valid in a wide operating range, for a SiC MOSFET and Schottky diode half-bridge with all parasitics, in order to improve the accuracy for both turn-on and turn-off. In addition, the accuracy of the proposed model serves as a benchmark to analyze the impact of different assumptions/simplifications on the accuracy of switching loss models. This is crucial for deriving simplified and computationally more efficient models in the future. In a first step, all devices are modelled based on data sheet information. Due to the tolerance between different devices, the data sheet information is generally not very accurate. Therefore, the following nonlinear device characteristics are modelled in this paper based on measurements:

- Nonlinear capacitances $C_{gd}(V_{ds})$, $C_{ds}(V_{ds})$
- Nonlinear junction capacitance $C_{sch}(V_R)$ and forward characteristic $I_F$-$V_F$ for Schottky diodes
- Real SiC MOSFET transfer characteristic $I_{ds}$-$V_{gs}$ during high voltage and high current switching transitions [9, 10]

With these device characteristics, the set of nonlinear differential circuit equations is formulated with as few assumptions as possible, and then solved by numerical solvers like ode [7] to calculate the switching losses. In a second step, the accuracy improvement by using measured characteristics instead of device data sheet information is investigated.

This paper is organized as follows. In section 2, the nonlinear device characteristics are measured and the proposed analytical switching loss model is derived based on a switching transition analysis. Section 3 verifies the accuracy of the proposed model by LTspice simulations and double pulse tests with a detailed analysis. Section 4 provides insights into the influence of different assumptions/simplifications on the accuracy of switching loss models, and the conclusions are drawn in section 5.

2 Proposed Analytical Switching Loss Model

In the following, the proposed analytical switching loss model is derived based on a step-by-step switching transition analysis. The switching losses are then calculated by solving the equation set of the equivalent circuit, which is formulated based on the assumptions given in section 2.1 and the nonlinear device characteristics in section 2.2.

2.1 Assumptions and Simplifications

Fig. 1 depicts the considered equivalent circuit for a hard-switched SiC MOSFET and a SiC Schottky diode half-bridge [11], where all relevant parasitics from the device packages and the PCB layout are included. The model assumptions/simplifications are:

A1) A lumped parasitic inductance $L_{PCB}$ resulting from the PCB traces in the power loop is assumed. Similarly, a lumped turn-on(off) gate loop parasitic inductance $L_{g,on(off)}$ is assumed, including the MOSFET internal gate inductance. The mutual inductive coupling between the power and the gate loop is neglected.

A2) The parasitic PCB capacitance $C_{PCB,HV,D}$ and the parasitic capacitance $C_L$ of the load inductor are connected in parallel to the Schottky diode junction capacitance $C_{sch}$. Similarly, the parasitic PCB capacitance $C_{PCB,D,S}$ is connected in parallel to the MOSFET drain-source capacitance $C_{ds}$.

A3) The resistance of the PCB traces is neglected. A lumped gate resistance $R_{g,on(off)}$ is assumed, which is the sum of the gate driver output resistance, the MOSFET internal gate resistance $R_{g,int}$, and an external gate resistance.
A4) The DC voltage $V_{in}$ and the inductive load current $I_L$ are assumed to be constant during switching transitions. An ideal bipolar gate voltage $V_g$ with negligible rise and fall time is assumed.

A5) A constant temperature is assumed, so that all parameters are temperature invariant during switching transitions. The MOSFET gate-source capacitance $C_{gs}$ is assumed to be constant.

A6) The charge and discharge of the MOSFET intrinsic capacitances are assumed to be lossless. Therefore, the switching losses are determined by the overlap between $i_{ch}$ and $V_{ds}$.

2.2 Nonlinear Device Characteristics and Circuit Description

Based on the aforementioned assumptions, a set of nonlinear differential circuit equations is formulated in the following. To calculate the switching losses accurately, the nonlinearity of the MOSFET and the Schottky diode must be considered. In addition, the device characteristics under real switching conditions must be captured, i.e. at high $V_{DS}$ and high $I_{DS}$ (HVHI) for the MOSFET. In general, the data sheet information is not accurate enough due to the tolerance between different devices, so that a device characterization with a power device analyzer (PDA) is necessary to achieve the best accuracy. The obtained device parameters are then modelled with fitting curves (functions). All devices are modelled based on data sheet information in a first step and based on static power device analyzer measurements in a second step, as well as extra measurements in a final step. The C3M0075120D SiC MOSFET and the C4D10120H Schottky diode are selected as the exemplary devices under test (DUT).

An important parameter for an accurate switching loss model is the nonlinear gate-drain capacitance $C_{gd}$, which is directly related to the voltage rise/fall intervals. Instead of using a static $C_{gd}$ in the $C_{gd}$-$V_{ds}$ curves from data sheet or PDA measurements, [9] introduces a dynamic gate-drain charge $Q_{gd,dy}$ that can be obtained from $V_{gs}$-$Q_g$ gate charge characteristics (Fig. 2a). The gate charge measurement captures the current that flows through the channel oxide capacitance $C_{ox,ch}$. This current is also a part of the gate-drain current $i_{gd}$ but cannot be captured by static $C_{gd}$-$V_{ds}$ curve measurements, during which the MOSFET is always in the off-state. Therefore, the dynamic $Q_{gd,dy}$ is larger than the static $Q_{gd,st}$ that is integrated from $C_{gd}$-$V_{ds}$ curves. As a result, conventional switching loss models based on $C$-$V_{ds}$ curves usually exhibit faster voltage rise/fall intervals than the experiment results [9].

The $V_{gs}$-$Q_g$ characteristics are measured by injecting a constant small gate current (typically in the mA range) until the DUT is fully turned on at a nominal operating point, during which the dynamic turn-on process is close to the real HVHI switching transients. As illustrated in Fig. 2a, line $AB$ corresponds to the current rise interval, and line $BC$ corresponds to the voltage fall interval. Please note that the slope of line $BC$ indicates a rising gate voltage during the voltage fall interval, which is usually assumed to be the constant miller plateau voltage in conventional switching loss models. This rising gate voltage is necessary to avoid that the channel current drops during the voltage fall interval, because the MOSFET $I_{ds}$-$V_{ds}$ curve in the first quadrant has a rising slope in the saturation region, due to the pronounced channel length modulation caused by the short channel lengths in state-of-the-art SiC MOSFETs. The dynamic charge $Q_{gd,dy}$ during the interval $BC$ can be calculated by $Q_{gd,dy} = Q_g - C_{gs} \cdot \Delta V_{gs}$. Fig. 2b shows the measured $Q_{gd,dy}$ for a fixed $I_{ds} = 20$A at different $V_{ds}$ values. The derivative function of the fitted $Q_{gd,dy}$-$V_{ds}$ curve in Fig. 2b is plotted as the red $C_{gd,dy}$-$V_{ds}$ curve in Fig. 2c, which is higher than the static $C_{gd}$-$V_{ds}$ curves as expected.

**Fig. 2:** (a) MOSFET gate charge characteristics, $I_{ds} = 20$A, $V_{ds} = 800$V. (b) Dynamic $Q_{gd,dy}$ from gate charge measurements, $I_{ds} = 20$A. (c) Measured $C$-$V_{ds}$ (solid lines) and their curve fits (dashed lines). Black denotes data sheet information, blue denotes PDA measurements, and red denotes the derived dynamic $C_{gd,dy}$ from (b).
Another important parameter for an accurate switching loss model is the transfer characteristic, which is directly related to the current rise/fall intervals. Instead of using the $I_{ds}-V_{gs}$ curves from data sheet or PDA measurements that are measured under low $V_{ds}$ values (typically tens of volts), the authors of [10] and [12] measure the dynamic transfer characteristics during HVHI switching transients by double pulse tests (DPT). A higher $V_{ds}$ reduces the source-drain potential barrier, which leads to a lower $V_{th}$ and a higher $I_{ds}-V_{gs}$ slope. This drain induced barrier lowering (DIBL) effect is more pronounced in state-of-the-art SiC MOSFETs due to their short channel lengths for reducing $R_{dson}$. Furthermore, the large number of defect states at the SiC/SiO₂ interface in SiC MOSFETs causes an apparent threshold voltage hysteresis (TVH) [10]. Before turn-on, a negative gate voltage leads to a positive charge carrier accumulation in the defect states, which increases the effective turn-on gate voltage and thus reducing $V_{th,on}$. Analogously a larger $V_{th,off}$ is expected for turn-off. Therefore, conventional switching loss models based on $I_{ds}-V_{gs}$ curves from data sheet or PDA measurements are inherently not very accurate.

In order to measure the $I_{ds}-V_{gs}$ curves, a large gate resistor (typically in the kΩ range) is used in the DPT to minimize the influence from parasitic inductances and to capture the transfer characteristics during the slow $dI_{ds}/dt$ intervals with relatively constant $V_{ds}$ values [10, 12]. Fig. 3a and Fig. 3b depict the Table 1: Nonlinear device parameter list of the DUTs based on data sheet, PDA measurement and full measurement. This also includes the fitting functions of the nonlinear characteristics and their fitted coefficients.

<table>
<thead>
<tr>
<th>Parameter (Unit)</th>
<th>Fit function(s)</th>
<th>Data sheet value (DSV)</th>
<th>PDA measurement (PDAVM)</th>
<th>Full measurement value (FMV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{on,on}$ (A)</td>
<td>-</td>
<td>10.548</td>
<td>6.5252</td>
<td>-</td>
</tr>
<tr>
<td>$C_{on}(\mu F)$</td>
<td>-</td>
<td>1450</td>
<td>1200</td>
<td>-</td>
</tr>
<tr>
<td>$C_{off}(\mu F)$</td>
<td>$C_{off} = \frac{C_{D}}{1 + \frac{V_{DD}}{V_{DD}}} + C_{f}$</td>
<td>$C_{off} = 806.8$ ( r = 2.707 ) ( V_{DD} = 21.54 ) $C_{off} = 461.6783$ $C_{f} = 0.7412$ ( r = 0.6948 ) ( V_{DD} = 1.556 ) $V_{DD} = 1.692$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$h_{off}(\mu F)$</td>
<td>$h_{off} = \frac{C_{D}}{1 + \frac{V_{DD}}{V_{DD}}} + C_{f}$</td>
<td>$h_{off} = 741.3981$ ( r = 14.01 ) ( V_{DD} = 21.54 ) $h_{off} = 841.6783$ $C_{f} = 0.7412$ ( r = 0.6948 ) ( V_{DD} = 1.556 ) $V_{DD} = 1.692$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{th}(V)$</td>
<td>-</td>
<td>3.5</td>
<td>3.5</td>
<td>-</td>
</tr>
<tr>
<td>$C_{on}(\mu F)$</td>
<td>$C_{on} = \frac{C_{D}}{1 + \frac{V_{DD}}{V_{DD}}} + C_{f}$</td>
<td>$C_{on} = 406.8$ ( r = 2.707 ) ( V_{DD} = 21.54 ) $C_{on} = 660.6$ $C_{f} = 0.7412$ ( r = 0.6948 ) ( V_{DD} = 1.556 ) $V_{DD} = 1.692$</td>
<td></td>
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</tr>
<tr>
<td>$V_{th}(V)$</td>
<td>-</td>
<td>3.5</td>
<td>3.5</td>
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<td>$h_{off}(\mu F)$</td>
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<td>$h_{off} = 741.3981$ ( r = 14.01 ) ( V_{DD} = 21.54 ) $h_{off} = 841.6783$ $C_{f} = 0.7412$ ( r = 0.6948 ) ( V_{DD} = 1.556 ) $V_{DD} = 1.692$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 3: Comparison of measured MOSFET turn-on (a) and turn-off (b) transfer characteristics with data sheet and PDA measurements, $V_{th} = 4V$, $V_{CC} = 15V$. (c) Schottky diode $I_{F}-V_{F}$ fit. (d) Schottky diode $C_{ch}-V_{F}$ fit.
measured MOSFET turn-on and turn-off transfer characteristics compared to those from data sheet and PDA measurements, where the aforementioned DIBL and TVH effects can be clearly observed. Finally, the nonlinear $I_d-V_F$ curve and junction capacitance $C_{sch}$ of the Schottky diode are characterized in Fig. 3c and Fig. 3d. Table I summarizes the parameters of the DUTs and their fitting functions. Based on these nonlinear device characteristics, the switching losses are determined by solving the equation set (1) - (9) for the electric circuit in Fig. 1.

$$i_{ch} = 0 \text{ (cut-off) or } i_{ch} = f_{fit}(v_{gs}) \text{ (saturation) or } i_{ch} = \frac{v_{ds}}{R_{ds,on}} \text{ (ohmic)} \quad (1)$$

$$i_F = g_{fit}(v_F) \text{ (forward } D_{sch}) \text{ or } i_F = C_{sch} \frac{dv}{dt} \text{ (reverse } C_{sch}) \quad (2)$$

$$V_{CC(EE)} = R_{g,on(off)} \cdot i_g + L_{g,on(off)} \cdot \frac{di}{dt} + v_{gs} + L \cdot \left( \frac{di_{gs}}{dt} + \frac{di_{ch}}{dt} + di_{ds} \right) \quad (3)$$

$$V_{in} = L_{PCB} \frac{di_{DS}}{dt} - L_{sch} \frac{di_{F}}{dt} - v_p + L \frac{di_{DS}}{dt} + v_{ds} + L \left( \frac{di_{gs}}{dt} + \frac{di_{ch}}{dt} + di_{ds} \right) \quad (4)$$

$$i_g = i_{gs} + C_{gd} \cdot \left( \frac{dv_{gs}}{dt} - \frac{dv_{ds}}{dt} \right) \quad (5)$$

$$i_{DS} = C_{gd} \cdot \left( \frac{dv_{gs}}{dt} - \frac{dv_{gs}}{dt} \right) + i_{ch} + i_{ds} \quad (6)$$

$$i_{gs} = C_{gs} \frac{dv_{gs}}{dt} \quad i_{ds} = C_{ds} \frac{dv_{ds}}{dt} \quad i_L = i_{DS} + i_F \quad (7-9)$$

There, the following 9 state variables are selected: internal gate-source voltage $v_{gs}$, gate current $i_g$, MOSFET channel current $i_{ch}$, internal gate-source current $i_{gs}$, internal drain-source current $i_{ds}$, internal drain-source voltage $v_{ds}$, external drain-source current $i_{DS}$, Schottky diode forward current $i_F$ and Schottky diode forward voltage $v_F$. The complete equation set can be written in matrix form:

$$M(t,y)\dot{y} = f(t,y), \quad (10)$$

where $\dot{y} = [v'_{gs}, i'_g, i'_{ch}, i'_{gs}, i'_{ds}, i'_{DS}, i'_F, v'_F]^T$ represents the first derivative of the state variable vector $y$. In order to solve this set of nonlinear differential algebraic equations (NDAE), numerical solvers such as ode15s, ode23t, or ode15i can be used. Fig. 4 depicts the exemplary switching waveforms of the C3M0075120D and C4D10120H half-bridge including turn-on, hard turn-off, and ZVS turn-off transitions [11], obtained by solving this NDAE set including the parasitics listed in Table II in section 3. The complete set of NDAE (10) is included in the appendix.

![Fig. 4: Switching waveforms for a turn-on transition at $V_{in}$ = 800 V, $I_L$ = 20 A in (a), for a hard turn-off transition at $V_{in}$ = 800 V, $I_L$ = 20 A in (b), and for a ZVS turn-off transition at $V_{in}$ = 800 V, $I_L$ = 5 A in (c). Black lines denote the circuit response based on data sheet information and red lines based on the full measurements presented in section 2.2. Detailed switching interval annotations are added only for black lines for clarity.](image-url)
2.3 Turn-on Transition

In the following, the turn-on transition is briefly analyzed based on the step-by-step switching interval analysis in [11]. To solve the system equation set in (10), both the initial and the end states of each interval are required. Obviously, the end state of the previous switching interval is the initial state of the next one. Fig. 4a depicts the exemplary hard turn-off switching waveforms.

Interval \( I_{on1} \) - Turn-on delay \( (t_0 - t_1) \): Before the turn-on delay interval, the MOSFET is in the cut-off region and the Schottky diode \( D_{sch} \) conducts the full load current \( I_L \) with a forward voltage drop \( V_D(I_L) \), so that the initial state vector is: \( y_{1,0} = [V_{EE}, 0, 0, 0, V_{ds}, 0, V_D(I_L)]^T \). At \( t_0 \), the gate voltage jumps up from \( V_{EE} \) to \( V_{CC} \) based on assumption A5, so that the input capacitance \( C_{iss} = C_{gs} + C_{gd} \) is charged. The MOSFET remains in the cut-off region (off-state) until the end state \( V_{gs} = V_{th} \) is reached, and the full load current is still conducted by \( D_{sch} \). No switching losses are generated in this interval.

Interval \( I_{on2} \) - Current rise \( (t_1 - t_2) \): The initial state vector is: \( y_{2,0} = [V_{th}, i_D(t_1), 0, i_{gs}(t_1), i_{ds}(t_1), V_{ds}(t_1), i_{DS}(t_1), i_{FD}(t_1), V_F(t_1)]^T \). At \( t_1 \), the MOSFET channel starts to open and to conduct a rising current. The MOSFET is in the saturation region and the channel current \( i_{ch} \) behaves as a current source controlled by voltage \( V_{gs} \). \( D_{sch} \) is still conducting current in the forward direction until the end state \( i_F = 0 \) is reached, when \( L_{sch} \) is fully commutated from the Schottky diode to the MOSFET.

Interval \( I_{on3} \) - Voltage fall \( (t_2 - t_3) \): The initial state vector is: \( y_{3,0} = [V_{gs}(t_2), i_D(t_2), i_{ch}(t_2), i_{gs}(t_2), i_{ds}(t_2), V_{gs}(t_2), i_{DS}(t_2), V_F(t_2)]^T \). At \( t_2 \), the Schottky diode forward clamping ends, so that the MOSFET output capacitance \( C_{oss} = C_{gs} + C_{gd} \) starts to discharge with decreasing \( V_{ds} \) and the Schottky diode juction capacitance \( C_{sch} \) starts to charge with increasing \( V_F \) in the reverse direction. The MOSFET remains in saturation until the end state \( V_{ds} = V_{gs} - V_{th} \) is reached, when the MOSFET enters the ohmic region.

Interval \( I_{on4} \) - Full gate charging \( (t_3 - t_4) \): The initial state vector is: \( y_{4,0} = [V_{gs}(t_3), i_g(t_3), i_{ch}(t_3), i_{gs}(t_3), i_{ds}(t_3), V_{gs}(t_3) - V_{th}, i_{DS}(t_3), i_{FD}(t_3), V_{F}(t_3)]^T \). At \( t_3 \), the MOSFET enters the ohmic region, while \( C_{sch} \) is charged up to DC-link voltage. As the last interval of the turn-on transition, voltage supply \( V_{CC} \) continues to charge \( C_{iss} \) until the end state \( V_{gs} = V_{CC} \) is reached. No switching losses are generated in this interval.

2.4 Turn-off Transition

In the following, the different types of turn-off transitions are briefly analyzed. Fig. 4b and Fig. 4c depict the exemplary hard turn-off and ZVS turn-off switching waveforms, based on the analysis in [11].

2.4.1 Hard turn-off

Interval \( I_{off1} \) - Turn-off delay \( (t_5 - t_6) \): Before the turn-off delay interval, the MOSFET is in the ohmic region (on-state) and conducts the full load current \( I_L \). At \( V_{ds} = V_{dson} = L_{R_{dson}} \). Capacitance \( C_{sch} \) is charged up to the voltage \( V_F(t_5) = V_{dson} - V_{th} \), so that the initial state vector is: \( y_{5,0} = [V_{CC}, 0, I_L, 0, 0, V_{dson}, I_{ch}, 0, V_F(t_5)]^T \). At \( t_5 \), the gate voltage jumps down from \( V_{CC} \) to \( V_{EE} \) and \( C_{iss} \) is discharged. The MOSFET remains in the ohmic region until the end state \( V_{gs} = V_{ds} + V_{th} \) is reached, when the MOSFET enters the saturation region. No switching losses are generated in this interval.

Interval \( I_{off2} \) - Voltage rise \( (t_6 - t_7) \): The initial state vector is: \( y_{6,0} = [V_{ds}(t_6) + V_{th}, i_g(t_6), i_{ch}(t_6), i_{gs}(t_6), i_{ds}(t_6), V_{ds}(t_6), i_{DS}(t_6), i_{FD}(t_6), V_F(t_6)]^T \). At \( t_6 \), the MOSFET still conducts the full load current \( I_L \) except for the current flowing through \( C_{sch} \), and the Schottky diode cannot conduct any current before the MOSFET \( C_{oss} \) is fully charged and the Schottky diode \( C_{sch} \) is fully discharged. Since \( V_{gs} > V_{th} \) and \( V_{ds} > V_{gs} - V_{th} \), the MOSFET remains in the saturation region. The Schottky diode remains blocked until the end state \( V_F = V_f \) (annotated in Fig. 3c) is reached, when \( D_{sch} \) starts conducting in the forward direction.

Interval \( I_{off3} \) - Current fall \( (t_7 - t_8) \): The initial state vector is: \( y_{7,0} = [V_{gs}(t_7), i_g(t_7), i_{ch}(t_7), i_{gs}(t_7), i_{ds}(t_7), V_{gs}(t_7), i_{DS}(t_7), i_{FD}(t_7), V_F(t_7)]^T \). At \( t_7 \), \( D_{sch} \) starts conducting in the forward direction and the current starts to commutate from the MOSFET to the Schottky diode. The MOSFET remains in the saturation region until the end state \( V_{gs} = V_{th} \) and \( i_{ch} = 0 \) is reached, when \( I_L \) is fully commutated from the MOSFET to the Schottky diode and the MOSFET enters the cut-off region.

Interval \( I_{off4} \) - Full gate discharging \( (t_8 - t_9) \): The initial state vector is: \( y_{8,0} = [V_{th}, i_g(t_8), 0, i_{gs}(t_8), i_{ds}(t_8), V_{gs}(t_8), i_{DS}(t_8), i_{FD}(t_8), V_F(t_8)]^T \). At \( t_8 \), the MOSFET enters the cut-off region, while \( D_{sch} \) conducts the load current. As the last interval of the turn-off transition, voltage supply \( V_{EE} \) continues to discharge \( C_{iss} \) until the end state \( V_{gs} = V_{EE} \) is reached. No switching losses are generated in this interval.
2.4.2 ZVS turn-off

As discussed in [11], the ZVS turn-off occurs when the channel current \(i_{ch}\) falls to zero before the voltage rise interval completes, which leads to almost lossless turn-off switching transitions. Compared to the hard turn-off, only two intervals (named accordingly as interval \(I_{zoff1}\) and \(I_{zoff2}\)) are different.

**Interval \(I_{zoff2}\) - Voltage rise I \((t'_6 - t'_7)\):** The initial state vector is: \(y_{6,0} = [v_{ds}(t'_6), v_{th}(t'_6), i_{ch}(t'_6), i_{gs}(t'_6), i_{ds}(t'_6), v_{ds}(t'_6), i_{DS}(t'_6), i_{F}(t'_6), v_{F}(t'_6)]^T\). At \(t'_6\), \(C_{oss}\) and \(C_{sch}\) start to charge/discharge and \(i_{ch}\) starts to drop. Since \(v_{gs} > v_{th}\) and \(v_{ds} > v_{gs} - V_{th}\), the MOSFET remains in the saturation region until the end state \(v_{gs} = V_{th}\) and \(i_{ch} = 0\) is reached. The Schottky diode remains blocked in this interval.

**Interval \(I_{zoff3}\) - Voltage rise II \((t'_7 - t'_8)\):** The initial state vector is: \(y_{7,0} = [v_{gs}(t'_7), 0, i_{gs}(t'_7), i_{ds}(t'_7), i_{DS}(t'_7), i_{F}(t'_7), v_{F}(t'_7)]^T\). Starting from \(t'_7\), the MOSFET enters and remains in the cut-off region. The load current \(i_L\) is fully used to charge/discharge \(C_{oss}\) and \(C_{sch}\). The Schottky diode remains blocked until the end state \(V_{F} = V_j\) is reached, when \(D_{sch}\) starts conducting in the forward direction. Therefore, the initial state vector for interval \(I_{zoff4}\) is: \(y_{8,0} = [v_{gs}(t'_8), i_{g}(t'_8), 0, i_{gs}(t'_8), i_{ds}(t'_8), v_{ds}(t'_8), i_{DS}(t'_8), i_{F}(t'_8), v_{F}(t'_8), V_j]^T\).

### 3 Simulation and Experiment Verification

To verify the proposed model, switching losses are extracted from LTspice simulations at different operating points using models from the manufacturers. In addition, a DPT setup is designed with minimized parasitics to measure the drain-source voltage \(V_{DS}\) and the drain-source current \(I_{DS}\). As load, a 50 \(\mu\)H air core inductor is used with a low parasitic capacitance. In Table II, the parasitics from the setup and the DUTs are summarized. The source current \(I_{DS}\) is measured by a current sensor based on [13] with a 500MHz bandwidth and a low insertion inductance (0.3nH). Voltage \(V_{DS}\) is measured directly at the package pins, using both a low voltage passive probe (Lecroy PP008-1, 400V, 500MHz) and a high voltage passive probe (Lecroy PPE6kV, 6kV, 400MHz). All switching waveforms are measured with the same laboratory setup and post-processed in the same manner to calculate the switching losses, with the exemplary 800V 20A switching waveforms shown in Fig. 5. Fig. 6 compares the switching loss energies calculated by the proposed analytical model (based on the 3-step: DSV - PDAMV - FMV device characterization parameters in Table I) and those resulting from the DPT measurements in a wide operating range \((V_{DS} = [400, 800])V, I_{DS} = [5, 30])A\) at room temperature. For comparison, the analytical model in [2] is re-derived and implemented to calculate the switching loss energies for the considered Schottky diode and SiC MOSFET half-bridge. The gate circuit parameters are fixed at \(V_{EE} = -4V, V_{CCC} = 15V, R_{g,ext,on/off} = 5\Omega\). Note that the switching losses calculated by the analytical model are based on the drain-source voltage \(V_{DS}\) across the package pins (different from the state variable \(v_{ds}\) in (10) and Fig. 4) and based on the \(I_{DS}\).

Efforts are made to minimize the potential errors resulted from the DPT according to [14]. The desek of the voltage and current probes is properly conducted, which is supported by the good matching (\(E_{on}\) discrepancy \(\xi = 6\%\), \(E_{off}\) discrepancy \(\xi = 1.8\%\)) between the LVprobe and HVprobe measurement.

---

**Table II: Parasitics from DUTs and the measurement setup.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Name</th>
<th>Value</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>L_{PCB}</td>
<td>Power loop PCB parasitic inductance</td>
<td>8.30nH</td>
<td>FEM (DC)</td>
</tr>
<tr>
<td>L_{PCB,g}</td>
<td>Gate-on loop PCB parasitic inductance</td>
<td>10.62nH</td>
<td>FEM (DC)</td>
</tr>
<tr>
<td>L_{PCB,f}</td>
<td>Gate-off loop PCB parasitic inductance</td>
<td>10.52nH</td>
<td>FEM (DC)</td>
</tr>
<tr>
<td>L_{GXM}</td>
<td>MOSFET internal gate inductance</td>
<td>10.45nH</td>
<td>Cree model</td>
</tr>
<tr>
<td>L_{DS}</td>
<td>MOSFET drain inductance</td>
<td>4.37nH</td>
<td>Cree model</td>
</tr>
<tr>
<td>L_{SS}</td>
<td>MOSFET source inductance</td>
<td>5.29nH</td>
<td>Cree model</td>
</tr>
<tr>
<td>L_{S,D}</td>
<td>Schottky diode anode and cathode inductance</td>
<td>13.4nH</td>
<td>Cree model</td>
</tr>
<tr>
<td>C_{PCB,R,V}</td>
<td>PCB high side parasitic capacitance</td>
<td>23.66pF</td>
<td>FEM</td>
</tr>
<tr>
<td>C_{PCB,D,S}</td>
<td>PCB low side parasitic capacitance</td>
<td>12.46pF</td>
<td>FEM</td>
</tr>
<tr>
<td>C_{L}</td>
<td>Load inductor parasitic capacitance</td>
<td>13.74pF</td>
<td>Impedance analyzer</td>
</tr>
</tbody>
</table>

**Fig. 5:** (a) DPT PCB picture. Measured 800V 20A turn-on (b) and turn-off (c) waveforms with post-processings.
results (cyan and blue circles) in Fig. 6a and Fig. 6d. In addition, the end point of the switching energy integration interval is always selected at the zero crossing points of measured voltage/current waveforms, excluding the remaining oscillation periods, as shown in Fig. 5. The same applies to the switching loss energies calculated with the analytical model and the LTspice simulations. The mean absolute error is used to evaluate the accuracy, which is defined by

\[
\tau = \frac{1}{N} \sum_{n=1}^{N} \frac{|E_{n,\text{ana/spice}} - E_{n,\text{meas}}|}{E_{n,\text{meas}}}
\]

(11)

Fig. 6 clearly shows the accuracy improvement of using the FMV compared to using the DSV and the PDAMV in Table I, especially for turn-off losses. However, the model based on the PDAMV is not reducing the switching loss error for neither turn-on nor turn-off, compared to the model based on the DSV. This is mainly caused by the smaller MOSFET gate internal resistance \( R_{g,int} \) measured by the PDA, since it strongly influences the overlap time between the switching voltage and current. As a result, the model based on the PDAMV always leads to lower switching losses compared to the model based on the DSV. In addition, the model based on static measurements (DSV and PDAMV) always leads to lower hard switching losses compared to the model based on dynamic measurements (FMV). This is mainly caused by the larger dynamic \( C_{gd,dv} \) compared to the \( C_{gd} \) from static \( C_{gd} \)-\( V_{ds} \) curves (Fig. 2c). Although the transfer characteristics obtained from the FMV exhibit higher transconductances than the static \( I_{dss} - V_{ds} \) curves (Fig. 3a, Fig. 3b), which result in shorter current rise/fall intervals (\( \tau_{\text{FMV}} < \tau_{\text{DSV}} \) in Fig. 4b), the longer voltage rise/fall intervals (\( \tau_{\text{FMV}} > \tau_{\text{DSV}} \) in Fig. 4b) contribute more and dominate the switching losses due to the much larger dynamic \( C_{gd,dy} \). This also explains the larger accuracy improvement for turn-off losses than for turn-on losses when using the FMV, because \( C_{gd} \) has a larger impact on turn-off switching than on turn-on switching. Note that for the ZVS turn-off scenario this \( C_{gd} \) influence is not very obvious.

On average, the proposed analytical model based on the full parameter measurements has a mean absolute error \( \tau_{\text{on}} = 8.4\% \) for turn-on losses and \( \tau_{\text{off}} = 12.7\% \) for turn-off losses over a wide operating range. This is better than the result calculated by the analytical model in [2] with \( \tau_{\text{on}} = 16.47\% \) and \( \tau_{\text{off}} = 18.26\% \) based only on data sheet information, which is adapted to the SiC MOSFET and Schottky diode half-bridge topology. In general, Fig. 6 indicates that turn-off losses are slightly over-estimated and turn-on losses are slightly under-estimated by the proposed model, which are both quite sensitive to the parasitic capacitance values in Table II. The common-mode noise caused by ground capacitances from

![Fig. 6: Switching losses comparison between the proposed analytical model (using the 3-step: DSV - PDAMV - FMV device characterization parameters in Table I), the re-derived analytical model in [2] (using only DSV), LTspice simulations and DPT measurements at different operating points.](image)
the experimental setup is difficult to model and not included in the calculation, which is one likely reason for the error. Furthermore, the parasitic inductance values are not very accurate, because they are assumed to be constant values (given either directly by manufacturer models or by FEM simulations), and only DC FEM simulation results are used. Nevertheless, good accuracies have been achieved over a wide operating range. In addition, the impact of different assumptions/simplifications on the accuracy of switching loss models can be evaluated with the proposed model, as discussed in the following.

4 Impact of Assumptions/Simplifications on Accuracy

With the proposed model, the impact of different assumptions/simplifications on the accuracy of switching loss models can be evaluated. The commonly used assumptions mentioned in section 1 are:

B1) Constant (charge-equivalent) capacitance $C_{gd,\text{Qeq}}$ based on data sheet $C-V_{ds}$ curves (group 1)
B2) Constant transconductance $g_m$ based on linearized data sheet $I_{ds}-V_{gs}$ curves (group 1)
B3) Only the step-response of the gate RC circuit (gate resistance $R_g$ and MOSFET input capacitance $C_{iss}$) is solved instead of the full circuit response during turn-on/turn-off delay intervals (group 2)
B4) The voltage drop caused by the gate current $i_g$ on the common source inductance $L_s$ is neglected during current rise/fall intervals (group 2)
B5) A constant gate miller voltage is assumed during the voltage rise/fall intervals (group 2)

The switching loss energies calculated by the proposed model based on the full parameter measurements serve as benchmarks. By considering different assumptions, the set of NADE in (10) changes and the resulting switching loss energies are calculated accordingly. The absolute values of the switching energy differences $|\Delta E|$ caused by the different assumptions are then divided by the benchmark values, which indicate the impact of different assumptions/simplifications on the accuracy of switching loss models. Results are shown in Fig. 7, with $|\Delta E|\%$ named as the switching loss error in the following.

In general, group 1 assumptions (approximated nonlinear characteristics) have a larger impact on the switching loss error compared to group 2 assumptions (simplified circuit equations), which indicates the necessity to use accurate device parameters since they have more influence on the switching loss error. In group 1, $C_{gd}$ has more influence than $g_m$ on the switching loss error, especially on the turn-off loss error. The commonly adopted B2 assumption is very reasonable to be used for turn-on ($|\Delta E_{\text{on}}| = 1\%$). Assumption B1 is relatively reasonable for turn-on and assumption B2 is relatively reasonable for turn-off, both of which result in around 10% switching loss error. As a conclusion, both the dynamic $C_{gd,dy}$ based on gate charge measurements and the real $I_{ds}-V_{gs}$ characteristics under HVHI switchings are crucial for an accurate switching loss model.

On the other hand, group 2 assumptions all lead to relatively small errors. Since assumption B3 only influences the turn-on/turn-off delay intervals, the model accuracy is barely reduced. In addition, the low errors $|\Delta E| < 2\%$ using assumption B4 indicates a negligible voltage drop contribution from $i_g$ on $L_s$ during current rise/fall intervals, especially for turn-on. Although the DUT exhibits a quite significant slope in the gate charge characteristic in Fig. 2a, assumption B5 only leads to a relatively reasonable switching loss error $|\Delta E_{\text{on}}| = 10\%$, $|\Delta E_{\text{off}}| = 4\%$. Note that the aforementioned analysis is based on the operating point at $V_{in} = 800\text{ V}$, $I_L = 20\text{ A}$, which is close to the nominal operating point of the considered SiC MOSFET and Schottky diode half-bridge.

5 Conclusion

In this paper, an analytical switching loss model for a SiC MOSFET and Schottky diode half-bridge is proposed, which is based on nonlinear differential circuit equations including parasitics. In the model, only a constant temperature, a constant $C_{gs}$, a constant DC-link voltage and load current, and $|\Delta E|\%$ is the switching loss error in the following.

![Fig. 7: Turn-on and turn-off loss energy differences (percentage) caused by different assumptions at $V_{in} = 800\text{ V}$, $I_L = 20\text{ A}$.

**Assumptions**

<table>
<thead>
<tr>
<th>Assumptions</th>
<th>Turn-on</th>
<th>Turn-off</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>50%</td>
<td>50%</td>
</tr>
<tr>
<td>B2</td>
<td>40%</td>
<td>40%</td>
</tr>
<tr>
<td>B3</td>
<td>30%</td>
<td>30%</td>
</tr>
<tr>
<td>B4</td>
<td>20%</td>
<td>20%</td>
</tr>
<tr>
<td>B5</td>
<td>10%</td>
<td>10%</td>
</tr>
</tbody>
</table>
an ideal gate voltage are assumed, neglecting the mutual inductive coupling between the power loop and the gate loop. The proposed model estimates the switching loss energies with a mean turn-on loss error of 8.4% and a mean turn-off loss error of 12.7% over a wide operating range, which is better than the model proposed in [2].

In addition, the accuracy improvement by using measured characteristics instead of device data sheet information is investigated in the paper. The device parameters characterized by static measurements, including data sheet information and PDA measurements, are not accurate enough for determining the switching losses accurately and lead to errors above 10% for turn-on losses and errors above 40% for turn-off losses. On the contrary, the dynamic gate-drain capacitance $C_{gd,dy}$ based on gate charge measurements and the $I_{ds}-V_{gs}$ transfer characteristics under high voltage high current switchings lead to errors below 10% for turn-on losses and errors below 14% for turn-off losses.

Finally, the proposed model is used to analyze the impact of different assumptions/simplifications on the accuracy of switching loss models. In general, group 1 assumptions (approximated nonlinear characteristics) have a larger impact on the switching losses compared to group 2 assumptions (simplified circuit equations), where the gate-drain capacitance $C_{gd}$ has the largest influence on the accuracy of switching loss models. The commonly used constant charge-equivalent capacitance assumption is reasonable to below 10% for turn-on losses and errors below 14% for turn-off losses. The complete set of nonlinear differential algebraic equations (NDAE) in (10) is written in matrix form for hard turn-off.

$$I_{on1}, I_{on2}, I_{off1}, I_{off2}$$

$$I_{off3}, I_{off4}$$

$$I_{on3}, I_{on4}$$

Parameters, variables, and fitting functions can be found in Fig. 1, Table I and Table II. (L_{PD} = L_{PCB} + L_d)
References


