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Bidirectional Phase-Modular 3-Φ Buck-Boost Converter Systems

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DAVID MENZI

MSc ETH
born on 26.07.1992
citizen of Burgdorf, Switzerland

accepted on the recommendation of

Prof. Dr. Johann W. Kolar, examiner
Prof. Dr. Juan Rivas-Davila, co-examiner

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ETH Zurich
Power Electronic Systems Laboratory
Physikstrasse 3 | ETL H23
8092 Zurich | Switzerland

http://www.pes.ee.ethz.ch

Il est bien facile, & mesme necessaire de voir plus loin que nos devanciers, lors que nous sommes montez sur leur espaules.
– Marin Mersenne

Es ist einfach, & sogar nötig weiter zu sehen als unsere Vorgänger, denn wir sind auf ihre Schultern gestiegen.
– Marin Mersenne

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According to the Swiss writer and stoic Rolf Dobelli most of a person's achievements are not due to innate qualifiers but mostly the result of one's environment and luck. Luck I had plenty and after four years of Ph.D., I would like to thank first and foremost my family, my parents Ueli and Susan and my brother Simon, for their support and unconditional love throughout my entire life. Almost ten years ago, by another lucky coincidence, I met my amazing wife Vera: My life could not even be half as happy without you.

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Abstract

The energy transition from a fossil fuel based towards a carbon dioxide free society is one of the crucial challenges of modern time.

Power electronics, and specifically (bidirectional) three-phase converters are an enabling technology for a wide range of renewable energy applications: They are key components of both electric vehicle drivetrains and the corresponding battery chargers, and for interfacing solar or wind power plants to the grid. Further, they enable substantial efficiency gains in industrial drives and future server power supplies, hence motivating research in this field.

Phase-modular three-phase buck-boost converters further allow to cover wide input and/or output voltage ranges without the need for a subsequent DC/DC converter stage, thereby enabling an integration of functionality and (quasi-)single-stage energy conversion at high efficiency. Therefore, such systems are of great interest for renewable energy powered applications, where often the voltage levels fluctuate in a wide range.

This thesis considers several buck-boost converter module topologies, where a first contribution on a three-phase Twelve-Switch Buck-Boost Y-Inverter (12-YI) is within the field of industrial drive systems and aims at operation with flexible and lightweight unshielded motor and supply cables. No comprehensive filter design guidelines for both conducted and radiated emissions of industrial drives are available in the current literature, and the high-frequency emission profile of the 12-YI was also not investigated so far. Accordingly, this work covers the described gap in literature, and the theoretical findings are experimentally verified using an ultra-compact 11 kW 12-YI prototype system employing 1200 V SiC power semiconductors and a switching frequency of 100 kHz, where measurement results indicate full compliance for operation with unshielded DC supply and AC motor cables according to the IEC 61800-3.

The module structure of the Six-Switch Buck-Boost Y-Inverter (6-YI), a second system analyzed in this thesis is attractive due to its simplicity and low number of components, and is hence considered in the context of an auxiliary drive system. The low complexity of the 6-YI comes at the cost of high component stresses and the 6-YI therefore is inherently limited to low efficiency and power density performance metrics. This work studies advanced modulation techniques enabling component stress reduction, thereby improving the loss performance substantially. The theoretical considerations are validated on a 1 kW hardware prototype employing 600 V GaN power semiconductors and a switching frequency of 300 kHz, where loss reductions of up to 31 % (relative to conventional modulation) at nominal power operation are demonstrated,

such that the 6-YI complies with an auxiliary motor drive efficiency target of 95 %.

A further contribution investigates the new module structure of a Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (RPI-12-YI). The buck-boost inductors of three-phase phase-modular buck-boost inverter systems are typically arranged in the main and/or forward current paths and therefore subject to large current stresses. This has a direct impact on the component losses and volume, and the buck-boost inductors therefore cover a substantial fraction of the overall converter volume and limit the maximally achievable converter power density. The presence of an inductive three-phase load (e.g., a three-phase motor) allows to locate the buck-boost inductors in the current return path of each RPI-12-YI module, thereby reducing the low-frequency current stresses by up to 90 % (corresponding to an 80 % smaller magnetics volume) compared to a conventional forward-path-inductor 12-YI for a typical operating range. This thesis investigates the basic operating principle, derives the relevant component stress metrics and presents a potential control strategy for this novel topology. Experimental waveforms in buck and boost operation of a 3.3 kW RPI-12-YI prototype system with 1200 V SiC power semiconductors and a switching frequency of 100 kHz verify the practical feasibility of the proposed topology.

The bidirectional module structures considered in this work can also be employed in three-phase Power Factor Correction (PFC) rectifier applications, e.g., a 12-YI can be operated as a Twelve-Switch Buck-Boost Y-Rectifier (12-YR). Accordingly, this thesis contains a contribution on a 12-YR with a wide DC output voltage range (e.g., for an electric vehicle battery charger), which is not yet covered in literature. The basic operating concept of a three-phase 12-YR is outlined and a *dq*-coordinate based 12-YR control structure with low computational burden is proposed. A detailed analysis on worst case component stresses for the considered operating range is conducted, and a filter design for compliance with the CISPR 11 Class A emission limits is presented. Preliminary experimental measurements with an 11 kW 12-YR prototype employing 1200 V SiC power semiconductors and a switching frequency of 100 kHz verify the system startup strategy, as well as operation in both buck and boost condition. The prototype system shows a power density of 12 kW/dm^3 and recorded efficiencies of up to 98.2 %.

Advanced component technologies (e.g., WBG semiconductors or high-energy density ferroelectric Multilayer Ceramic Capacitors (MLCCs)) promise ever more compact and efficient converter realizations. To achieve this, systematic converter designs by means of a comprehensive Pareto optimizations

allow to identify the ideal converter parameters and component selection. In order to facilitate meaningful performance predictions, such optimization structures rely on accurate component loss models. However, in literature no loss model exists for ferroelectric MLCCs under large signal excitation. Accordingly, this thesis further comprises a component level contribution and proposes a new Steinmetz loss model which accurately predicts ferroelectric MLCCs losses under non-sinusoidal and/or DC biased voltage excitations. The method is successfully verified under various operating conditions for a 1 kV X7R MLCC with loss prediction errors under 8 %.

The thesis concludes with a summary of the contributions, as well as an outlook to future research topics and opportunities related to the very generic nature of bidirectional phase-modular three-phase buck-boost converter systems.

Kurzfassung

Die Energiewende, d.h., der Übergang von einer auf fossilen Brennstoffen basierender zu einer CO_2 neutralen Gesellschaft gehört zu den herausragenden Herausforderungen der nächsten Jahrzehnte.

Leistungselektronik im allgemeinen, und besonders bidirektionale dreiphasige DC/AC und AC/DC Wandler repräsentieren eine Schlüsseltechnologie für eine Vielzahl von Anwendungen in Verbindung mit erneuerbarer Energie: Beispiele sind die E-Mobilität (sowohl im Antriebsstrang als auch bei den entsprechenden Batterieladegeräten), oder auch die Erzeugung von erneuerbaren Energien, wo der Leistungsfluss von Solarzellen oder Windrädern in das Landes-Elektrizitätsnetz ermöglicht wird. Zusätzlich ermöglichen solche Konverter substanzielle Effizienzgewinne im Bereich der industriellen Antriebstechnik oder auch in der Energieversorgung moderner Rechenzentren, sodass Forschung in diesem Bereich ein breites Anwendungsfeld erschliesst.

Phasenmodulare Dreiphasen-Hochsetz-Tiefsetz-Konverter beherrschen zusätzlich weite Eingangs- und/oder Ausgangsspannungsbereiche ohne eine ansonsten nötige zusätzliche DC/DC Konverter-Stufe, sodass eine (quasi-) einstufige Energieumwandlung mit hoher Effizienz ermöglicht wird. Daher sind solche Systeme hochinteressant für die Nutzung erneuerbarer Energien, wo oftmals die DC und/oder AC Spannungen in weiten Bereichen variieren.

Diese Dissertation untersucht mehrere Hochsetz-Tiefsetz Modul-Konzepte, wobei ein erster Forschungsbeitrag im Bereich eines Zwölf-Schalter Hochsetz-Tiefsetz Y-Umrichters (12-YI) für industrielle Antriebssysteme liegt, wo die Nutzung flexibler und leichter ungeschirmter Motoren- und Versorgungskabel ermöglicht werden soll. Betrachtungen zur Konverter-Auslegung unter Berücksichtigung von leitungsgebundenen und abgestrahlten elektromagnetischen Störungen sind bisher nicht vollständig in der Literatur vorhanden, und auch die Störaussendungssignatur des 12-YI wurde bisher in der Literatur noch nicht untersucht. Die vorliegende Arbeit schliesst diese Forschungslücke und die theoretischen Überlegungen werden experimentell verifiziert anhand eines extrem kompakten 11 kW 12-YI Prototyps mit 1200 V Siliziumkarbid Halbleitern und einer Pulsfrequenz von 100 kHz. Messungen weisen auf volle Komptabilität für den Betrieb mit ungeschirmtem Motor- und Netzkabel gemäss der Norm IEC 61800-3 hin.

Die Modulstruktur des 6-YI, eines zweiten Systems, welches auf Grund der Einfachheit und geringen Anzahl an Komponenten im Rahmen dieser Dissertation untersucht wird, wird im Kontext eines Hilfsbetriebe-Antriebssystems betrachtet. Die geringe Komplexität des 6-YI hat jedoch eine hohe Komponentenbelastung zur Folge, was zu einer inhärent limitierten Effizienz bzw.

Leistungsdichte führt. Hier werden neuartige Modulationstechniken zur Reduktion der Komponentenbelastung untersucht, welche die Umwandlungsverluste substanziell reduzieren. Die theoretischen Überlegungen werden anhand eines 1 kW 6-YI Prototyps mit 600 V Galliumnitrid Leistungshalbleitern und einer Schaltfrequenz von 300 kHz validiert. Eine Verlustreduktion von bis zu 31 % (gegenüber herkömmlicher Betriebsart) wird demonstriert, womit der 6-YI Prototyp das Effizienzziel für Hilfsbetriebe-Antriebssysteme von 95 % erfüllt.

Ein weiterer Forschungsbeitrag untersucht die Modul-Struktur des 12-YI mit Rück-Strompfad-Induktivität (RPI). Beim herkömmlichen 12-YI liegen die Hochsetz-Tiefsetz-Induktivitäten im Haupt- bzw. Vorwärts-Strompfad und sind daher hohen Strombelastungen ausgesetzt, was direkten Einfluss auf die Komponentenverluste und das Bauvolumen nimmt. Entsprechend beanspruchen die 12-YI Hochsetz-Tiefsetz-Induktivitäten einen substantiellen Anteil des Gesamt-Konvertervolumens und limitieren somit die maximal mögliche Konverter-Leistungsdichte. Das Vorhandensein einer induktiven Dreiphasenlast (z.B. eines Dreiphasenmotors) erlaubt es, die 12-YI Hochsetz-Tiefsetz-Induktivitäten in den Rück-Strompfad zu verschieben. Für einen typischen Betriebsbereich wird damit die niederfrequente Strombelastung um bis zu 90 % im Vergleich zum 12-YI reduziert, was ein um ca. 80 % reduziertes Bauvolumen der Induktivitäten erlaubt. Das Betriebskonzept des RPI-12-YI wird untersucht, relevante Komponentenbelastungskennzahlen werden berechnet und mögliche Regelungskonzepte diskutiert. Die praktische Umsetzung des Konzepts wird mit experimentellen Resultaten des Hochsetz-Tiefsetz-Betriebs eines 3.3 kW RPI-12-YI-Prototyps mit 1200 V Siliziumkarbid Leistungshalbleitern und einer Pulsfrequenz von 100 kHz verifiziert.

Die bidirektionale Modulstrukturen erlauben auch einen Einsatz der Konvertersysteme in Dreiphasen-Gleichrichter-Anwendungen. In der Tat kann ein Zwölf-Schalter Hochsetz-Tiefsetz Y-Umrichter (12-YI) auch direkt als Zwölf-Schalter Hochsetz-Tiefsetz Y-Gleichrichter (12-YR) betrieben werden. Entsprechend beinhaltet diese Arbeit einen Beitrag zu einem 12-YR für Anwendungen mit weitem DC Ausgangsspannungsbereich (z.B. Batterieladegeräte im Bereich der E-Mobilität), eine in der Literatur bisher nicht diskutierte Fragestellung. Das Grundkonzept des 12-YR wird präsentiert und eine auf dq-Koordinaten basierende Netzstromregelstruktur mit niedrigem Bedarf an Rechenleistung eingeführt. Eine detaillierte Analyse der maximalen Komponentenbelastungen für den betrachteten Betriebsbereich wird durchgeführt und ein Netzfilter für Kompatibilität mit der CISPR 11 Class A Störaussendungsnorm wird vorgeschlagen. Experimentelle Ergebnisse eines 11 kW 12-YR

Prototyps mit 1200 V Siliziumkarbid Leistungshalbleitern und einer Pulsfrequenz von 100 kHz bestätigen die vorgeschlagene Strategie zum Hochfahren des Systems sowie den Hochsetz- und Tiefsetz-Betrieb. Das Prototyp-System weist eine Leistungsdichte von 12 kW/dm^3 und eine gemessene Effizienz von bis zu 98.2 % auf.

Fortschrittliche Bauteiltechnologien wie z.B. Halbleiter mit grossem Bandabstand oder ferroelektrische Keramikkondensatoren (MLCCs) mit hoher Energiedichte erlauben die Realisierung von Konverter-Systemen mit nie dagewesener Effizienz und/oder Leistungsdichte. Die weitere Verbesserung derartiger Systeme erfordert einen systematischen Design-Prozess und umfassende Pareto-Optimierungen zur Identifizierung der idealen Konverter-Parameter und -Komponenten. Um vernünftige Voraussagen zum Betriebsverhalten machen zu können, nutzen solche Optimierungsprogramme präzise Komponentenverlustmodelle. In der Literatur existiert jedoch derzeit kein Verlustmodell für ferroelektrische MLCCs mit Grosssignal-Aussteuerung. Daher beinhaltet diese Dissertation einen zusätzlichen Beitrag zur Modellierung von MLCCs. Dazu wird ein neues Steinmetz-Modell vorgestellt, welches präzise die Verluste ferroelektrischer MLCCs für nicht-sinusförmige Spannungen und/oder den Betrieb mit einer DC Offset-Spannung vorhersagt. Diese Methode wird für verschiedene Betriebspunkte für einen 1 kV X7R MLCC erfolgreich verifiziert, wobei der Modell-Fehler auf < 8 % beschränkt bleibt.

Die Dissertation schliesst mit einer Zusammenfassung der Forschungsbeiträge, sowie einem Ausblick auf zukünftige Forschungsthemen und einer Diskussion weiterer Einsatzmöglichkeiten phasenmodularer Dreiphasen-Hochsetz-Tiefsetz-Konverter.

Abbreviations

AMN	Artificial Mains Network
BEV	Battery Electric Vehicle
CM	Common Mode
CMAD	Common Mode Absorption Device
DC CCS	DC Combined Charging System
DF	Dissipation Factor
DM	Differential Mode
DPWM	Discontinuous PWM
DSP	Digital Signal Processor
DUT	Device Under Test
EMI	Electromagnetic Interference
ESR	Effective Series Resistance
EUT	Equipment Under Test
EV	Electric Vehicle
EVTOL	Electric Vertical Takeoff and Landing
FC	Fuel Cell
FCEV	Fuel Cell Electric Vehicle
FPI-12-YI	Forward-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter
GaN	Gallium Nitride
HF	High-Frequency
HPC	High Power Charging
ICE	Internal Combustion Engine
iGSE	improved Generalized Steinmetz Equation
iGSE-C	improved Generalized Steinmetz Equation for Ceramic Capacitors
LF	Low-Frequency
LISN	Line Impedance Stabilization Network
MLCC	Multilayer Ceramic Capacitor
MOSFET	Metal-Oxid-Semiconductor Field-Effect Transistor
OATS	Open-Area Test Site
PCB	Printed Circuit Board
PDU	Power Distribution Unit

PE	Protective Earth
PFC	Power Factor Correction
PHEV	Plug-in Hybrid Electric Vehicle
PLL	Phase-Locked Loop
PV	Photovoltaic
PWM	Pulse-Width Modulation
RCD	Residual-Current Device
RPI-12-YI	Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter
SAC	Semi-Anechoic Chamber
SE	Steinmetz Equation
Si	Silicon
Si IGBT	Silicon Insulated-Gate Bipolar Transistor
SiC	Silicon Carbide
SPG	Steinmetz Premagnetization Graphs
SPWM	Sinusoidal PWM
SRC	Series Resonant Converter
ST	Sawyer-Tower
$\tan\delta$	Loss Tangent
THD	Total Harmonic Distortion
TPWM	Third Harmonic Injection PWM
V2G	Vehicle-to-Grid
VSD	Variable Speed Drive
VTA	Voltage-Time Area
WBG	Wide Band-Gap
6-CSI	Six-Switch Current Source Inverter
6-CSR	Six-Switch Current Source PFC Rectifier
6-VSI	Six-Switch Voltage Source Inverter
6-VSR	Six-Switch Voltage Source PFC Rectifier
6-YI	Six-Switch Buck-Boost Y-Inverter
12-YI	Twelve-Switch Buck-Boost Y-Inverter
12-YR	Twelve-Switch Buck-Boost Y-Rectifier
24-YR	Six-Module 24-Switch Buck-Boost Y-Rectifier

Contents

1 Introduction

The use of the inexhaustible energy sources, i.e., solar, wind and hydro power goes back to the very beginning of civilization [1–3]. However, in the course of the electrification of the modern world a major share of the electricity production was covered by fossil fuels, with only ancillary contributions of hydro power and – to an even smaller extent – wind power [4]. Further, the Silicon (Si) Photovoltaic (PV) cell converting sunlight directly into electricity was only invented in 1954, and found early applications rather in satellites than terrestrial energy generation [5].

The 1970s energy crisis revealed the large dependency of the modern world on fossil fuel based energy, and public awareness on finite global resources was further triggered by the book *Limits to Growth* [6] published in 1972 by the Club of Rome. Although fossil fuels turned out to be more abundant than estimated in the 1970s (e.g., the US coal reserves are estimated to cover today's demand for 484 further years [7]), accumulating evidence and consensus on climate change in the 1990s made clear that a large fraction of today's known fossil fuel reserves must not be exploited in order to limit global warming [8, 9], also leading to the term of the *Carbon Bubble* within the context of fossil energy related investments [10]. Accordingly, global endeavours for a transition from fossil to renewable energy sources were initiated by the United Nations Framework Convention on Climate Change and the Kyoto Protocol in 1992 and 1997, respectively.

Fig. 1.1a depicts the world electric energy generation from 1985 to 2020, where coal fired power plants remain the largest contributor up to date. However, an unprecedented increase in renewable electric energy generation starting around the year 2000 brings renewables today in the close vicinity of coal in the year 2020. Further, the annual increase of renewables in 2020

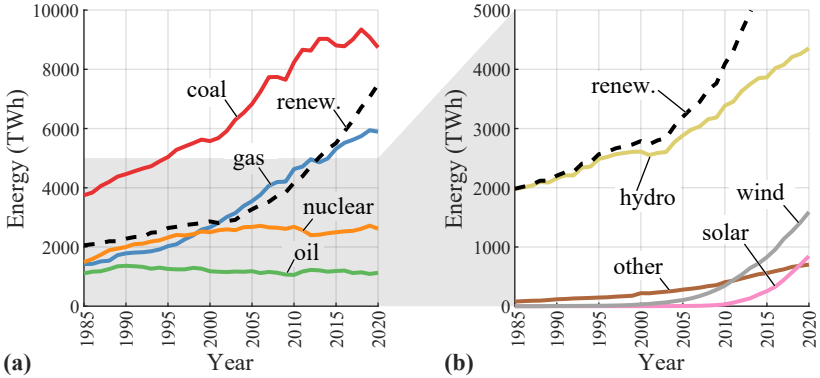

Fig. 1.1: World electric energy generation by category from 1985 to 2020: **(a)** total and **(b)** renewable electric energy generation (data from [11]).

was 7 %, which is 20 % above the respective average annual growth rate of the prior decade [12].

Fig. 1.1b further details the sources of renewable electric energy generation, where hydropower – the only relevant renewable energy contributor up to the year 2000 – maintained an approximately linear growth up to above 4000 TWh by 2020. Wind and solar contribution started with an exponential increase around the year 2000 and 2010, respectively, where fiscal incentives and economies of scale led to a sharp price decay in the past decade of both wind and PV, which today undercut the cost per kWh of a fossil fuel fired power plant [13]. A challenge is posed here by the fact that both PV and wind power plants are subject to large stochastic power generation fluctuations. Accordingly, to assure availability a large energy storage infrastructure (and backup power plants) as well as advanced demand-side management will be required in the electricity grid of the future [14,15]. Given the massive increase in overall electricity demand, a special focus on efficiency improvements will remain crucially important to enable the energy transition. With two thirds of industry's (and approximately 30 % of the global) electric energy consumption used to power electric motors [16], Variable Speed Drives (VSDs) enabling 30 % to 50 % efficiency improvements [17] present a key technology.

With the progressive decarbonisation of the electric energy generation, electrification of transportation – one of the most important energy consumers which is currently predominantly dependent on fossil fuels – is crucial to meet the goal of net zero carbon dioxide emissions by 2050 [20]. This is currently

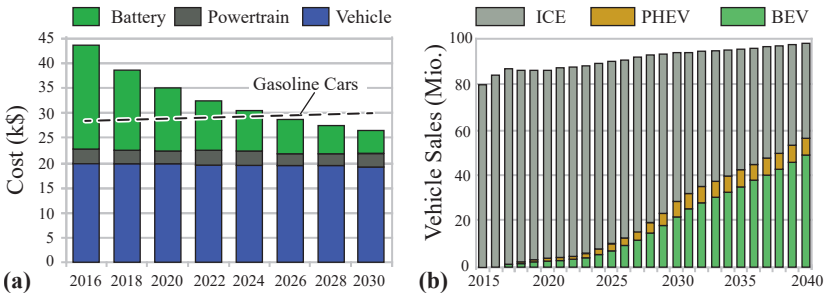

Fig. 1.2: (a) Predicted cost development of the main components of a US medium Battery Electric Vehicle (BEV) (with expected price parity to an Internal Combustion Engine (ICE) car by mid 2020s, data from [18]) and **(b)** past and predicted passenger vehicle sales by category (PHEV is Plug-in Hybrid Electric Vehicle, data from [19]).

addressed by means of a massive rollout of Electric Vehicles (EVs) (i.e., Battery Electric Vehicles (BEVs), Plug-in Hybrid Electric Vehicles (PHEVs) and also Fuel Cell Electric Vehicles (FCEVs) for higher power levels / ranges) [20]: **Fig. 1.2** depicts the projected BEV prices, where a massive decay in battery cost should allow for price parity with an Internal Combustion Engine (ICE) car by the middle of the current decade [18]. Accordingly, BEV (and also PHEV) are expected to reach a global sales share of 57 % by 2040 [19].

Allowing highly efficient electric energy conversion, as well as active control of the instantaneous power flow in a piece of equipment, power electronics will play a major role in the global energy transition [21, 22]. Accordingly, the amount of electric power processed in the USA through some form of power electronics is estimated to reach 80 % of the overall electric power by 2030 [23, 24].

Power electronics three-phase DC/AC converter systems are employed in the previously mentioned application of industrial VSDs, which allow a substantial reduction of energy consumption in comparison to conventional control [16, 17]. Similarly, three-phase DC/AC and AC/DC converters are key components for EV drivetrains and the corresponding charging infrastructure, respectively, and find also application as PV inverters and in wind power plants. Hence, power electronics three-phase DC/AC and AC/DC energy conversion represents a vital technology for a more sustainable society, which is the main motivation for the research conducted in this thesis. Within this field, the emergence of Wide Band-Gap (WBG) power semiconductors [24, 25],

as well as enhanced passive component technologies (e.g., Multilayer Ceramic Capacitors (MLCCs) with rated voltages up to several kV [26], and advanced magnetic materials [27]) triggered a wave of innovations, promising ever more compact (i.e., with reduced resource use) and efficient power conversion [28]. Accordingly, the subsequent section presents an inventory of applications for three-phase DC/AC and AC/DC converters with focus on the input-output voltage range requirements.

1.1 Wide Input-Output Voltage Range Applications of Three-Phase Power Electronic Converters

Pulse-Width Modulation (PWM) three-phase DC/AC and AC/DC converters translate a DC voltage U_{dc} into three-phase AC voltages (with line-to-neutral voltage amplitude $\hat{U}_{\mathrm{ac}}$ and frequency f_{ac}) or vice versa. A characteristic property of many of the above mentioned renewable applications, is the fact that the DC and/or the AC voltage amplitude vary in wide ranges, posing a substantial challenge to the related converter systems. **Fig. 1.3** depicts several examples of such applications, where an exemplary DC voltage range $U_{\mathrm{dc}} \in [U_{\mathrm{dc,min}}, U_{\mathrm{dc,max}}]$ is highlighted on top of the time domain AC voltage waveforms (within one mains period T_{ac}) of the three-phase AC voltages with respect to the negative DC-link rail $u_{\mathrm{an}}, u_{\mathrm{bn}}, u_{\mathrm{cn}}$ (the AC voltage formation is discussed in more detail subsequently in **Sec. 1.3**).

Fig. 1.3a depicts a DC-supplied three-phase VSD inverter of e.g., the drivetrain of a BEV or an FCEV, where the generated AC voltage amplitude $\hat{U}_{\mathrm{ac}}$ and frequency f_{ac} depend on the motor operating point. There, the power flow direction can also reverse in case of regenerative braking, where the released energy can be supplied to other equipment connected to the same DC bus, or stored in the battery. It is important to highlight, that the input voltage U_{dc} provided by the battery depends on the state-of-charge and temperature [29, 30] (in case of an FC U_{dc} heavily depends the power extracted [31, 32]) such that the converter needs to be able to operate from a DC-input voltage varying in a wide range.

Similar input-output voltage requirements can also be found for industrial VSDs inverters allowing compatibility with various DC-bus voltages and/or nominal motor voltages. The voltage range depicted in **Fig. 1.3a** correspond to the voltage ranges considered in **Chapter 2**, i.e., a U_{ac} =230 $\mathrm{V_{rms}}$ three-phase motor powered from a DC input voltage $U_{\mathrm{dc}} \in [400\,\mathrm{V}, 750\,\mathrm{V}]$. It is important

to highlight, that the new WBG power semiconductors with low switching losses and ohmic on-state behaviour allow for evermore efficient and compact realization of VSDs, but at the same time the high dv/dt values pose substantial stresses on the motor (i.e., bearing currents, transient overvoltages and reflected waves on long motor cables) [33, 34], such that future inverter systems ideally feature a full-sinewave output filter [35].

EV battery chargers with rated power > 3 kW are typically supplied from the three-phase AC grid. Hence, the charger system depicted in **Fig. 1.3b** comprises a three-phase Power Factor Correction (PFC) rectifier front-end as well as an isolated DC/DC converter providing galvanic isolation. Ideally the rectifier front-end regulates the DC output voltage, while the isolated DC/DC stage is, e.g., realized as an ultra-efficient Series Resonant Converter (SRC) with fixed input-output voltage ratio [36]. In order to feature compatibility with a large set of nominal battery voltages, a wide range in DC output voltage U_{dc} is required [37–39]. For example the DC Combined Charging System (DC CCS) High Power Charging (HPC) class [38] dictates $U_{\mathrm{dc}} \in [200\,\mathrm{V}, 920\,\mathrm{V}]$. A bidirectional grid interface beneficially allows the inversion of the power flow, hence enabling Vehicle-to-Grid (V2G) operation where EV batteries serve as grid energy storage elements [40]. This is then equivalent to a three-phase PV inverter feeding power into the grid, where the DC input voltage U_{dc} under maximum power point tracking also varies substantially across irradiation and ambient temperature [41–43].

For completeness (and to account for the massive increase in data centers computational power and related energy consumption [44]) **Fig. 1.3c** depicts a server power supply, where a three-phase PFC rectifier interface provides a facility-level DC-bus with $U_{\mathrm{dc}} = 400\,\mathrm{V}$, which is supplied to the server racks via a Power Distribution Unit (PDU). Ideally, such a system features compatibility with both a European $400\,\mathrm{V_{rms}}$ (line-to-line, i.e., $\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V_{pk}}$) and a US $480\,\mathrm{V_{rms}}$ (line-to-line, i.e., $\hat{U}_{\mathrm{ac}} = 390\,\mathrm{V_{pk}}$) three-phase mains (the AC input voltages can further vary within a range of +20 %/-10 % during operation) [45], and hence represents an application with a wide AC input voltage range.

1.2 Categorization of Standard Three-Phase Converter Systems

Bearing in mind the previously discussed application examples with wide input-output voltage ranges, it is important to highlight, that conventional

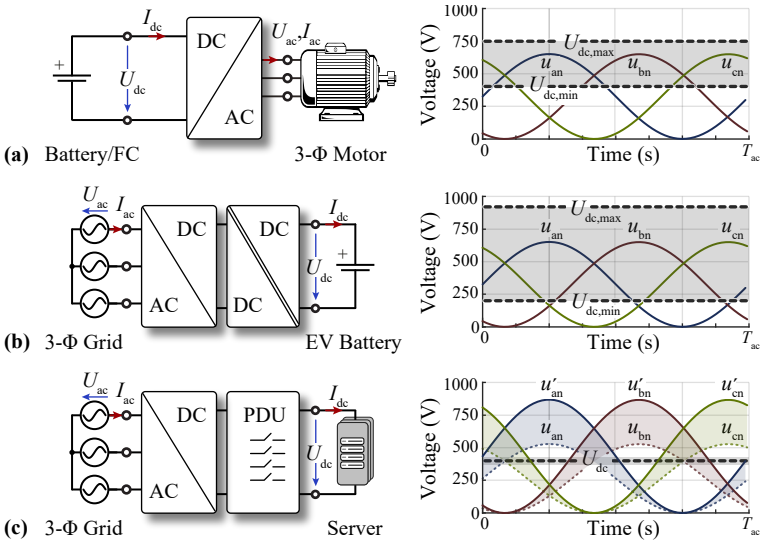

Fig. 1.3: Typical application examples and terminal voltage waveforms for three-phase AC/DC and DC/AC converters with wide operating voltage range requirement: **(a)** DC-supplied Variable Speed Drive (VSD) system powered by e.g., a battery or a Fuel Cell (FC), **(b)** Electric Vehicle (EV) battery charger, **(c)** data center server power supply compatible with both a 480 V_{rms} and 400 V_{rms} (line-to-line) three-phase mains (adapted from [46]).

single-stage three-phase DC/AC and AC/DC converter topologies show a limited voltage range. In fact, according to [47] a three-phase DC/AC converter can be categorized based on the AC line-to-neutral voltage amplitude $\hat{U}_{ac}$ relative to the DC input voltage U_{dc} as either buck-type or boost-type system.

In a three-phase inverter application (cf., **Fig. 1.3a**) the main power flow direction is from the DC side to the AC side and, accordingly, the DC input voltage U_{dc} serves as the base value for the inverter categorization as buck- or boost-type system. In a *buck-type* inverter system (e.g., a standard Six-Switch Voltage Source Inverter (6-VSI) [35]) the three-phase line-to-neutral

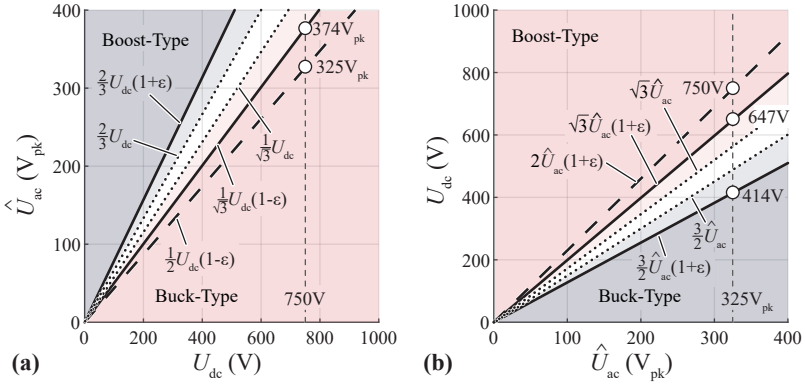

Fig. 1.4: Operating ranges of typical three-phase buck- and boost-type systems in **(a)** inverter and **(b)** PFC rectifier applications considering a current controllability margin of $\varepsilon = 15\,\%$ (adapted from [47]).

AC output voltage amplitude $\hat{U}_{\mathrm{ac}}$ is limited by the DC input voltage U_{dc} as

$$\hat{U}_{\mathrm{ac}} \leq \frac{1}{2} U_{\mathrm{dc}} \cdot (1-\varepsilon) \quad \text{(buck-type inverter)},$$
$$\hat{U}_{\mathrm{ac}} \leq \frac{1}{\sqrt{3}} U_{\mathrm{dc}} \cdot (1-\varepsilon) \quad \text{(buck-type inverter[1])}, \tag{1.1}$$

where ε represents a current controllability margin (e.g., required in case of a load or a reference step, with $\varepsilon = 15\,\%$ as a typical value). Harmonic injection techniques allow to improve the DC-link voltage utilization [48, 49]. For example, a motor drive inverter with a typical DC input voltage of 750 V (and $\varepsilon = 15\,\%$) can supply a three-phase motor with a phase voltage amplitude $\hat{U}_{\mathrm{ac}}$ of up to 325 $\mathrm{V_{pk}}$ and 374 $\mathrm{V_{pk}}$ without and with harmonic injection modulation, respectively, as highlighted in **Fig. 1.4a**.

In contrast, a *boost-type* three-phase inverter system (e.g., a Six-Switch Current Source Inverter (6-CSI) [50–52]) is limited to operation with sufficiently large AC output voltage, i.e., the instantaneous maximum line-to-line voltage strictly above the DC-link voltage U_{dc}, and

$$\hat{U}_{\mathrm{ac}} \geq \frac{2}{3} U_{\mathrm{dc}} \cdot (1+\varepsilon), \quad \text{(boost-type inverter)}. \tag{1.2}$$

It is important to highlight that the definition of buck-type and boost-type inverter systems is based on the main power flow direction, however, the

[1] With harmonic injection modulation.

instantaneous power flow direction might reverse in case of e.g., regenerative braking of a VSD inverter.

In case of a three-phase PFC rectifier (cf., **Fig. 1.3b,c**) the main power flow direction is from the AC side to the DC side and, accordingly, the AC line-to-neutral voltage amplitude $\hat{U}_{ac}$ serves as the base value for the categorization of a rectifier system as buck- or boost-type system:

$$\begin{aligned} U_{dc} &\leq \frac{3}{2}\hat{U}_{ac} \cdot (1-\varepsilon) \quad \text{(buck-type rectifier)}, \\ U_{dc} &\geq 2\hat{U}_{ac} \cdot (1+\varepsilon) \quad \text{(boost-type rectifier)}, \\ U_{dc} &\geq \sqrt{3}\hat{U}_{ac} \cdot (1+\varepsilon) \quad \text{(boost-type rectifier}^2\text{)}. \end{aligned} \tag{1.3}$$

Note, that in a rectifier application the operating ranges of voltage-source converters (e.g., a *boost-type* Six-Switch Voltage Source PFC Rectifier (6-VSR)) and current-source converters (e.g., a *buck-type* Six-Switch Current Source PFC Rectifier (6-CSR)) are reversed compared to an inverter application. Hence, as illustrated in **Fig. 1.4b**, a boost-type PFC rectifier system connected to a mains with $\hat{U}_{ac}$ =325 V_{pk} (i.e., 400 V_{rms} line-to-line voltage) is limited to DC-link voltages above $U_{dc,min}$ =647 V and $U_{dc,min}$ =750 V with and without harmonic injection modulation, respectively. Note that **Fig. 1.4** reveals the existence of an intermediate voltage-band in inverter AC output voltage amplitude $\hat{U}_{ac}$ (and rectifier DC output voltage U_{dc}) which cannot be covered by a standard buck-type or boost-type system [47].

It is important to highlight that the renewable energy applications discussed in **Sec. 1.1** show wide input-output voltage ranges which are overlapping. According to (1.1),(1.2),(1.3) a standard buck-type or boost-type three-phase AC/DC or DC/AC converter system is therefore not sufficient to cover the required operating ranges. Typically, DC/AC converter systems with buck-boost capability are formed by combining a boost-type DC/DC converter (stepping up the DC input voltage to a higher intermediate DC input voltage) with a buck-type three-phase inverter system (e.g., a 6-VSI) stepping down the intermediate DC voltage to sinusoidal three-phase AC output voltages, thereby forming a two-stage converter structure [32,53–55]. Alternatively, the same buck-boost functionality can be also achieved by combining a buck-type DC/DC converter with a boost-type inverter (e.g., a 6-CSI) [56,57]. However, in such cascaded systems, the electric energy is converted twice (i.e., a two-stage energy conversion takes place) limiting the system efficiency [58]. Apart from the conversion losses, the additional DC/DC converter stage also

[2] With harmonic injection modulation.

increases the overall converter bill of material, volume and weight, as well as costs. Last, such a cascaded system is also sub-optimal from a product management perspective as two different subsystems (i.e., a DC/DC and a three-phase DC/AC converter) have to be maintained [41].

The short-comings of such cascaded *two-stage* converter systems of course motivate research in *single-stage* three-phase buck-boost DC/AC and AC/DC converters (i.e., with inherent buck-boost capability and without the need for a preceding DC/DC stage), which can be either realized as impedance-source (e.g., Z-source), or as phase-modular (differential) converters [59]. The impedance network in, e.g., a Z-source three-phase inverter allows shoot-through zero states enabling both buck *and* boost AC output voltages [60]. However, the applicability is limited due to increasing voltage and current stresses in boost operation [61], as well as long commutations paths and potential common-mode related problems.

Accordingly, this thesis focuses on phase-modular (differential) buck-boost three-phase DC/AC and AC/DC converter systems, and the subsequent section discusses the fundamental operating principle of differential converters, as well as possible module structures.

1.3 Phase-Modular Buck-Boost Three-Phase Converter Systems

Fig. 1.5a illustrates the fundamental Differential Mode (DM) and Common Mode (CM) output voltage formation of phase-modular inverter system [56, 62, 63]. Three identical DC/DC converter modules are connected to a common reference potential given by the negative DC-link rail n, while the three-phase load (or source) starpoint N remains without connection. Each module generates a unipolar output voltage with respect to the negative DC-link rail $u_{\mathrm{an}}, u_{\mathrm{bn}}, u_{\mathrm{cn}}$. In the most simple case, each phase-module output voltage comprises a sinusoidally varying voltage component superimposed by a constant offset voltage (assuring unipolar voltages) as shown in **Fig. 1.5a.ii**. This offset voltage is present in each phase-module output voltage and hence represents a CM voltage

$$u_{\mathrm{CM}} = \frac{1}{3}(u_{\mathrm{an}} + u_{\mathrm{bn}} + u_{\mathrm{cn}}), \tag{1.4}$$

which cannot drive any current in the open starpoint N of the three-phase load. Accordingly, bipolar sinusoidal three-phase AC voltages $u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}$ (with

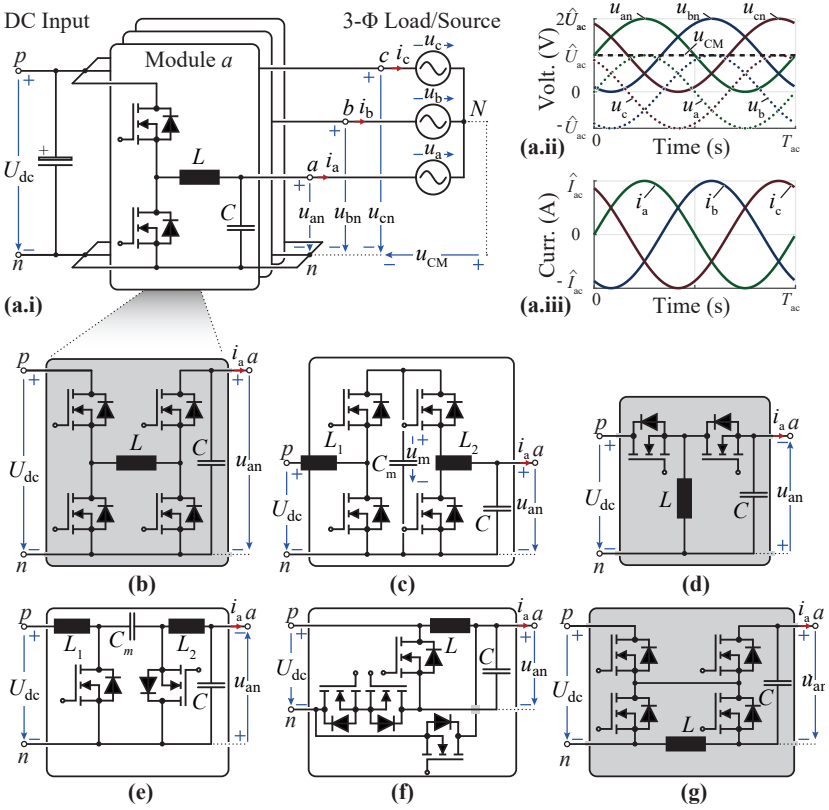

Fig. 1.5: (a) Illustration of the fundamental Differential Mode (DM) and Common Mode (CM) output voltage formation of phase-modular converter systems (**(a.i)** depicts the module structure of a standard buck-type Six-Switch Voltage Source Inverter (6-VSI)). Main power circuit of potential module realizations: **(b)** non-inverting four-switch buck-boost module of a Twelve-Switch Buck-Boost Y-Inverter (12-YI), **(c)** non-inverting four-switch boost-buck module, **(d)** inverting two-switch buck-boost module of a Six-Switch Buck-Boost Y-Inverter (6-YI), **(e)** Ćuk boost-buck converter module, **(f)** Tokusada buck-boost module, and **(g)** non-inverting four-switch return-path-inductor buck-boost module of a Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (RPI-12-YI).

amplitude $\hat{U}_{ac}$) and currents i_a, i_b, i_c (with amplitude $\hat{I}_{ac}$) can be formed [41,58] (cf., **Fig. 1.5a.ii-iii**). In **Fig. 1.5a.ii** the CM voltage is equal to the minimum constant offset voltage $u_{CM} = \hat{U}_{ac}$, which could be further lowered by means of a time varying u_{CM}, i.e., harmonic injection techniques [64].

Fig. 1.5a.i depicts (for completeness) the module structure of a standard buck-type 6-VSI with a sinewave output filter [35], i.e., a buck-type DC/DC converter, which is limited to output voltages u_{an} strictly below the DC input voltage U_{dc}. Then, **Fig. 1.5b-g** show the main power circuit of potential module realizations with buck-boost capability.

Extending the buck converter of **Fig. 1.5a.i** with a boost half-bridge as presented in **Fig. 1.5b**, the basic module of a Twelve-Switch Buck-Boost Y-Inverter (12-YI) is formed, allowing for AC voltage amplitudes both below and above the DC-link voltage [58, 64–67]. Note that advantageously, each converter module can be operated in quasi-single-stage operation [68–70], i.e., based on the instantaneous input-output voltage ratio of the power module, the buck or boost half-bridge is High-Frequency (HF) switched with PWM, thus limiting the switching losses. The 12-YI topology is a core part of this thesis, where no comprehensive analysis on the HF and/or Electromagnetic Interference (EMI) emissions of this topology exists in literature. Accordingly, **Chapter 2** investigates the electromagnetic compatibility of an ultra-compact 12-YI motor drive system for an industrial VSD application with unshielded supply and motor cables. Further, **Chapter 5** discusses the component stresses and control strategy of this topology in rectifier applications, i.e., for a Twelve-Switch Buck-Boost Y-Rectifier (12-YR). Several adoptions of this topology exist in literature, e.g., in [71–73] each module is extended with an additional unfolder full-bridge to mitigate the need for the CM offset in the output voltages, thereby reducing the component voltage stresses at the cost of doubling the number of power semiconductors in each module. Further, in [74] a fourth converter module is added to connect to the neutral conductor in a four-wire mains rectifier application. These approaches are not further investigated in this thesis due to the overall increase in active and/or passive devices and control complexity compared to the 12-YR topology.

By reversing the succession of the buck and the boost half-bridges of the 12-YI module in **Fig. 1.5b**, the non-inverting four-switch boost-buck module in **Fig. 1.5c** results. As for the 12-YI, each module can be operated in a quasi-single-stage fashion. This topology was investigated in [75] but not further pursued within the scope of this thesis, as the large number of magnetic components (which are typically bulky, and demanding in automated

manufacturing and assembly) presents a major limitation of this module structure.

In contrast, the module structure of a Six-Switch Buck-Boost Y-Inverter (6-YI) presented in **Fig. 1.5d** gained significant interest in literature [76, 77, 77–79]. An inverting two-switch buck-boost module generates a strictly negative output voltage. Due to the low number in active and passive components, as well as the simple control structure, the Six-Switch Buck-Boost Y-Inverter (6-YI) is a very promising topology candidate. However, the simplicity of the module structure comes at the cost of elevated component stresses, and **Chapter 3** extends the knowledge base by investigating advanced 6-YI modulation strategies enabling substantial performance improvements.

An inverting two-switch buck-boost module can also be realized as a Ćuk converter (cf., **Fig. 1.5e**) as investigated in [41, 79, 80]. Despite the low number of active devices, this topology, as well as related module structures described in [80] were not further pursued as the magnetic component number is doubled compared to the 6-YI and the 12-YI module. **Fig. 1.5f** presents (for completeness) the buck-boost module structure of a Tokusada converter [81] which was neither further pursued due to the high current stresses and the requirement of switches with bidirectional blocking capability.

Last, **Fig. 1.5g** depicts the non-inverting four-switch return-path-inductor buck-boost module of a Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (RPI-12-YI), which features substantially reduced buck-boost inductor current stresses compared to the conventional (forward-path-inductor) 12-YI module in **Fig. 1.5b**. This very interesting topology is — to the best knowledge of the author — not yet discussed in literature, and is hence the subject of **Chapter 4**.

1.4 List of Publications

Key insights presented in this thesis have been published or will be published in the form of international scientific journal or conference publications, or were presented at workshops. The publications created as part of this thesis, or also in the scope related research projects, are listed below.

1.4.1 Journal Papers

- **D. Menzi**, J. E. Huber, L. Kappeler, G. Zulauf, J. W. Kolar, "New Return-Path-Inductor Buck-Boost Y-Inverter Motor Drive with Reduced Cur-

rent Stresses," *IEEE Transactions on Power Electronics*, Vol. 37, No. 9, pp. 10086-10090, September 2022) DOI: 10.1109/TPEL.2022.3163465.

- **D. Menzi**, S. Chhawchharia, G. Zulauf, D. Bortis, H.-P. Nee, J. W. Kolar, "Comparative Evaluation of Harmonic Injection Techniques for a Phase-Modular Three-Phase Six-Switch Buck-Boost Y-Inverter," *IEEE Transactions on Power Electronics*, Vol.37, No. 3, pp. 2519-2524, March 2022) DOI: 10.1109/TPEL.2021.3115903.

- **D. Menzi**, D. Bortis, J. W. Kolar, "EMI Filter Design for a Three-Phase Buck-Boost Y-Inverter VSD with Unshielded Motor Cables Considering IEC 61800-3 Conducted & Radiated Emission Limits," *IEEE Transactions on Power Electronics*, Vol. 36, No. 11, pp. 12919-12937, November 2021. DOI: 10.1109/TPEL.2021.3075785.

- **D. Menzi**, M. Heller, J. W. Kolar, "iGSE-Cx – A New Normalized Steinmetz Model for Class II Multilayer Ceramic Capacitors, " *IEEE Open Journal of Power Electronics*, Vol. 2, pp. 138-144, February 2021. DOI: 10.1109/OJPEL.2021.3060874.

- **D. Menzi**, D. Bortis, G. Zulauf, M. Heller, J. W. Kolar, Novel iGSE-C Loss Modelling of X7R Ceramic Capacitors," *IEEE Transactions on Power Electronics*, Vol. 35, No. 12, pp. 13367-13383, December 2020. DOI: 10.1109/TPEL.2020.2996010.

Furthermore, the author had the pleasure to contribute to the following journal paper:

- P. Papamanolis, D. Bortis, F. Krismer, **D. Menzi**, J. W. Kolar, "New EV Battery Charger PFC Rectifier Front-End Allowing Full Power Delivery in 3-Phase and 1-Phase Operation," *Electronics*, 10 (17), 2069, August 2021. DOI: 10.3390/electronics10172069.

1.4.2 Conference Papers

- **D. Menzi**, J. W. Kolar J. Azurza, M. Kasper, "New Third-Harmonic Injection Modulation Reducing the DC-Link Energy Buffer Requirement of Phase-Modular Three-Phase Isolated PFC AC/DC Converter Systems," in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Virtual Conference, November 2021. DOI: 10.1109/APEC42165.2021.9487220.

- **D. Menzi**, M. Zhang, J. W. Kolar, J. Everts, "3-Phase Bidirectional Buck-Boost Sinusoidal Input Current Three-Level SiC Y-Rectifier," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Virtual Conference, June 2021. DOI: 10.1109/APEC42165.2021.9487220.

  Outstanding Presentation Award

- **D. Menzi**, J. W. Kolar, J. Everts, "Single-Phase Full-Power Operable Three-Phase Buck-Boost Y-Rectifier Concepts," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Virtual Conference, June 2021. DOI: 10.1109/APEC42165.2021.9487082.

- **D. Menzi**, D. Bortis, J. W. Kolar, "A New Bidirectional Three-Phase Phase-Modular Boost-Buck AC/DC Converter," in *Proc. of the IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Shenzhen, China, November 4-7, 2018. DOI: 10.1109/PEAC.2018.8590670.

  Excellent Paper Award
  Best Presenter at the Session Award

- **D. Menzi**, D. Bortis, J. W. Kolar, "Three-Phase Two-Phase-Clamped Boost-Buck Unity Power Factor Rectifier Employing Novel Variable DC Link Voltage Input Current Control," in *Proc. of the IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Shenzhen, China, November 2018. DOI: 10.1109/PEAC.2018.8590599.

  Best Presenter at the Session Award

Furthermore, the author had the pleasure to contribute to the following conference papers:

- J. W. Kolar, J. Azurza Anderson, S. Miric, M. Haider, M. Guacci, M. Antivachis, G. Zulauf, **D. Menzi**, P. Niklaus, J. Miniböck, P. Papamanolis, G. Rohner, N. Nain, D. Cittanti, D. Bortis, "Application of WBG Power Devices in Future 3-Phase Variable Speed Drive Inverter Systems – How to Handle a Double-Edged Sword," in *Proc. of the IEEE International Electron Devices Meeting (IEDM)*, San Francisco, USA, December 2020. DOI: 10.1109/IEDM13553.2020.9372022.

- M. Antivachis, D. Bortis, **D. Menzi**, J. W. Kolar, "Comparative Evaluation of Y-Inverter against Three-Phase Two-Stage Buck-Boost DC-

AC Converter Systems," in *Proc. of the International Power Electronics Conference (ECCE Asia)*, Niigata, Japan, May 2018. DOI: 10.23919/IPEC.2018.8507664.

1.4.3 Workshops and Seminars

- **D. Menzi**, D. Bortis, J. W. Kolar, "Ultra-compact 12 kW/1200 V SiC Y-Inverter," Presentation at the *33rd ECPE Project Coordination Committee (ECPE PCC) Meeting*, Hamburg, Germany, October 2019.

- **D. Menzi**, D. Bortis, J. W. Kolar, "Y-Inverter for Industry Drives," Dialogue session at the *31st ECPE Project Coordination Committee (ECPE PCC) Meeting*, Kassel, Germany, October 2018.

Furthermore, the author had the pleasure to contribute to the following presentations:

- J. W. Kolar, **D. Menzi**, J. E. Huber, "Conceptualization of the MVDC Power System of Ultra-Deep Sea HyDrones," Keynote Presentation at the *IEEE International Conference on DC Microgrids (ICDCM)*, Virtual Conference, July 2021.

- J. W. Kolar, J. E. Huber, **D. Menzi**, "Three-Phase SiC/GaN Converter Systems – There is No Boogeyman Under the Bed," Tutorial at the Virtual *PowerAmerica Annual Meeting*, Feb 2021.

- D. Bortis, J. W. Kolar, M. Antivachis, J. Azurza, M. Guacci, **D. Menzi**, "Advanced Three-Phase PFC-Rectifiers," Presentation at the *ECPE Cluster-Seminar "Power Factor Correction (PFC) and Active Front-Ends"*, Augsburg, Germany, May 2019.

- J. W. Kolar, M. Antivachis, D. Bortis, **D. Menzi**, J. Miniböck, F. Krismer, D. Rothmund, "Latest Findings in Three-Phase AC/DC Converter Research," Presentation at the *Future Energy Technology Workshop*, Nuremberg, Germany, June 2018.

- J. W. Kolar, M. Antivachis, D. Bortis, **D. Menzi**, J. Miniböck, F. Krismer, "Latest Findings in Three-Phase AC/DC Converter Research," Presentation at the *International Forum on Recent Trends in Power Electronics*, Tokyo, Japan, May 2018.

1.4.4 Patents

- **D. Menzi**, J. W. Kolar, "Flying Capacitor Circuit with Active Capacitor Voltage Control," PCT Patent Application, 2021.
- J. W. Kolar, **D. Menzi**, J. Azurza Anderson , M. Kasper, "Method of Operating a Power Converter Arrangement, Control Circuit and Power Converter Arrangement," European Patent Application, 2021.
- J. W. Kolar, **D. Menzi**, J. Everts, "Modular Reconfigurable Electrical AC/DC Converter," PCT Patent Application, 2020.
- **D. Menzi**, M. Zhang, J. Azurza Anderson, J. W. Kolar, "Multi-Level Bidirectional Electrical AC/DC Converter," PCT Patent Application, 2020.
- D. Bortis, J. W. Kolar, **D. Menzi**, "Vorrichtung und zugehöriges Modulations- und Regelverfahren zur Umsetzung einer in weiten Grenzen variierenden Gleichspannung in eine Mehrphasenwechselspannung mit variabler Frequenz und Amplitude," Swiss Patent Application, 2018.

1.5 Thesis Outline

According to the goals and contributions mentioned above, the content of the thesis is divided into six main Chapters. Chapter interdependencies have been reduced to the strict minimum and each Chapter is written in such a way that it can be read as a standalone text.

- **Chapter 2** focuses on an ultra-compact electromagnetically quiet Twelve-Switch Buck-Boost Y-Inverter (12-YI) motor drive system for applications with long unshielded supply and motor cables. The 12-YI is a very interesting topology for drives, as it allows compatibility with a wide range of DC input voltages and features inherently sinusoidal output voltages with low HF content. In this chapter, the relevant HF emission sources of the 12-YI are discussed. An EMI equivalent circuit for the topology is derived, and filter design guidelines are provided to allow operation with unshielded cables. Experiments are conducted with an 11 kW 12-YI prototype employing 1200 V Silicon Carbide (SiC) power semiconductors with 100 kHz switching frequency. Measurement results indicate compliance with the IEC 61800-3 conducted and radiated emission limits for unscreened power interfaces.

- **Chapter 3** studies harmonic injection modulation techniques for a low-component count Six-Switch Buck-Boost Y-Inverter (6-YI) motor drive system. The simplicity of the 6-YI converter modules comes at the cost of high component stresses, limiting the converter efficiency. Accordingly, advanced modulation strategies, are investigated with respect to the impact on component stresses and conversion efficiency. The expected performance gains with harmonic injection modulation are verified on a 1 kW 6-YI drive prototype employing 600 V Gallium Nitride (GaN) power semiconductors with 300 kHz switching frequency.

- **Chapter 4** provides the basic operating principle, performance metrics and control strategy of a new Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (RPI-12-YI). Phase-modular buck-boost three-phase DC/AC converters typically suffer from large buck-boost inductor current stresses, ultimately limiting the system power density. Accordingly, this Chapter investigates a new converter module structure with reduced inductor current stresses. The RPI-12-YI operating principle in buck and boost regime is verified on a 3.3 kW prototype system employing 1200 V SiC power semiconductors with 100 kHz switching frequency.

- **Chapter 5** focuses on the relevant aspects of a Twelve-Switch Buck-Boost Y-Rectifier (12-YR) with a wide DC output voltage range. Worst case component stresses are derived, and filter design guidelines are provided to limit grid-side HF emissions and allow compliance with the CISPR 11 Class A emission limits. Further, a dq-coordinate-based PFC rectifier control structure with low computational burden is proposed and a startup sequence is discussed. Experiments are conducted on a 11 kW 12-YI prototype employing 1200 V SiC power semiconductors with 100 kHz switching frequency.

- **Chapter 6** summarizes key findings and results of this thesis. Further, an outlook on future research topics, as well as the general applicability of buck-boost converter modules in several application areas is provided.

As mentioned, evermore compact and efficient converter systems highly depend – apart from the selected topology and modulation strategy – on the available component technologies [28]. Further, systematic converter designs and optimization rely on the underlying component performance

and loss models. Accordingly, the Appendix of this thesis further presents a component-level contribution:

- **Appendix A** investigates high-energy density ferroelectric Multilayer Ceramic Capacitors (MLCCs) promising evermore compact converter realizations. The high dielectric constant of such MLCCs comes at the cost of non-constant (voltage and temperature dependent) capacitance values making the modelling of large-signal excitation losses of these devices challenging. No generally applicable model exists up to date and this Appendix addresses this blind spot of literature by proposing a new Steinmetz loss model, which is successfully verified under various operating conditions with a 1 kV X7R MLCC.

2

Electromagnetically Quiet 12-YI Motor Drive

This Chapter summarizes the most relevant findings in the context of designing, building and experimentally analyzing an ultra-compact buck-boost three-phase motor drive system with sinusoidal output voltages also published in:

- D. Menzi, D. Bortis, J. W. Kolar, "EMI Filter Design for a Three-Phase Buck-Boost Y-Inverter VSD with Unshielded Motor Cables Considering IEC 61800-3 Conducted & Radiated Emission Limits," *IEEE Transactions on Power Electronics*, Vol. 36, No. 11, pp. 12919-12937, November 2021. DOI: 10.1109/TPEL.2021.3075785.

Motivation

Allowing for operation with a DC input voltage varying in a wide range, and providing sinusoidal output voltages with low HF content, the Twelve-Switch Buck-Boost Y-Inverter (12-YI) is a very interesting candidate for future Variable Speed Drives (VSDs). Unshielded motor and supply cables are cheaper and more lightweight than their screened counterparts, and also simplify the drive commissioning. However, special care is required to ensure electromagnetic compatibility. Accordingly, this Chapter covers all relevant aspects for the filter design for both conducted and radiated emissions of a 12-YI VSD.

Executive Summary

The standard converter concept employed in variable speed motor drives is the two-level three-phase Si IGBT voltage source inverter with its switch nodes connected to the motor terminals via shielded cables to avoid excessive HF noise emissions. However, high dv/dt pulses of the inverter pose substantial stresses on the motor, which are further intensified by the ever-faster switching speeds of wide band-gap power semiconductors, hence promoting interest in inverters with full-sinewave output filters, which potentially enable the use of inexpensive unshielded motor cables. However, the IEC 61800-3 standard dictates stringent conducted and radiated emission limits on unscreened power interfaces. In this work, a DC input and AC output filter structure allowing operation with unshielded cables is derived for a phase-modular 11 kW Twelve-Switch Buck-Boost Y-Inverter (12-YI) motor drive system employing 1.2 kV SiC MOSFETs with a switching frequency of 100 kHz. First, regulations and measurement techniques for conducted and radiated emissions of motor drives are analyzed. Next, the operating principle of the 12-YI is described and an EMI equivalent circuit is derived, followed by a systematic filter design. Finally, measurements are conducted on an ultra-compact hardware prototype of the converter system with 12 kW/dm^3 (197 W/in^3) power density, where the results indicate full compliance with the IEC 61800-3 conducted and radiated emission limits for operation with unshielded DC supply and motor cables in a residential area.

The basic 12-YI hardware demonstrator was developed within the context of an European Center for Power Electronics (ECPE [82]) Lighthouse Programme on modular and scalable Power Electronics Building Blocks (msPEBB) addressing the challenges of wide band-gap power electronics related to fast switching and highest power density.

2.1 Introduction

Today, more than two thirds of industry's electric energy consumption is used to power electric motors, contributing approximately 30 % to the global energy consumption and further growth is forecasted until 2040 [16]. In many applications, Variable Speed Drives (VSDs) allow a reduction of both the energy consumption and the life cycle cost of the overall drive system and are therefore a key technology towards a more sustainable society [17]. However, it is crucial to manage Electromagnetic Interference (EMI) emissions

of VSDs [83], where the IEC 61800-3 [84] is the relevant standard for industrial VSDs and applies both to AC grid connected and DC supplied systems (cf., **Fig. 2.1**). In industrial applications, there is a clear trend towards DC supply of VSDs [85–87], as e.g., power transfer among several drives is possible without loading the AC grid interface. Further, additional infrastructure such as a super capacitor energy storage can be shared among several VSDs [88], and, accordingly, in the following a DC supplied system is considered for the analysis.

The Pulse-Width Modulation (PWM) two-level three-phase Silicon Insulated-Gate Bipolar Transistor (Si IGBT) Six-Switch Voltage Source Inverter (6-VSI), with the motor cable directly connected to the switch nodes of the inverter bridge-legs, is the predominant topology for DC-fed VSDs in industry. Employing shielded cables, the power converter and the motor can be considered as a single unit located in a shielded enclosure, where motor interface EMI emissions are confined and hence are not relevant from a regulatory perspective. Therefore, the considered standard dictates – when employing shielded cables – only limits for the conducted grid interface emissions from 150 kHz to 30 MHz, as well as for the radiated emissions of the overall system in the range of 30 MHz to 1 GHz as presented in **Fig. 2.1**.

However, shielded cables are substantially more expensive than regular unshielded cables (up to a factor of three [90]) and also heavier (e.g., 152 kg/km for the unshielded 4GE-BC50, and 248 kg/km (+63 %) for the shielded 4GECY-KC50l cable from Belden Inc. (500 V, 20 A)). In case of moving applications (e.g., in robotics) cables are also subject to repetitive bending and flexing stresses, potentially leading to fatigue and fracture of the cable shield [91]. Further, shielded cables are an obstacle towards non-expert installation of drives, as an improper connection of the cable shield to the converter or motor housing is a major source of error during commissioning of VSDs [92]. Accordingly, the use of unshielded cables would be especially interesting. It is important to highlight that the IEC 61800-3 does not necessarily dictate the use of shielded cables, but imposes further conducted emission limits on any power interface (e.g., the motor cable or the DC bus) realized with unshielded cables longer than 2 m for VSDs operating in a residential area (cf., **Fig. 2.1**).

In case of the standard 6-VSI, the pulse-shaped PWM switch-node voltages are directly applied to the motor cable and, accordingly, the use of unshielded cables is discouraged due to excessive conducted and radiated emissions [93]. There, the switched voltages with high dv/dt values further cause High-Frequency (HF) motor losses, and add severe motor stresses (i.e., transient overvoltages and reflected waves on long motor cables [94], as well

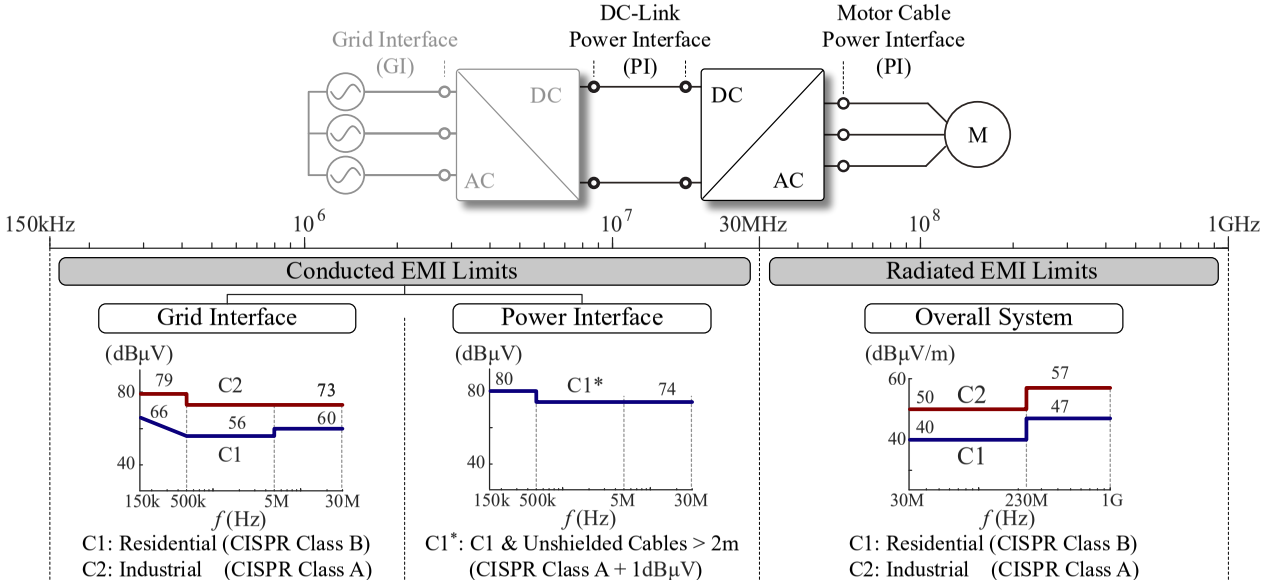

Fig. 2.1: Conducted and radiated EMI emission limits according to the IEC 61800-3 [84] for residential (C1) and industrial (C2) applications. Conducted emission limits apply to the frequency band from 150 kHz to 30 MHz, where the grid interface limits are based on the well known CISPR 11 regulations [89]. When employing long (i.e., ≥ 2 m) unshielded cables in residential applications, emission limits also exist for the respective internal power interfaces (i.e., DC-bus or motor cable). The overall system further needs to comply with radiated emission limits in the range of 30 MHz to 1 GHz, where the stated limit values are valid for a measurement distance of 3 m.

as capacitive bearing currents [95], [33]), ultimately reducing the VSD product lifetime. The emergence of ever-faster switching Wide Band-Gap (WBG) power semiconductor devices further intensifies this problem [96], [97].

Converters with sinusoidal output voltages (e.g., a 6-VSI with a sinewave output filter [35, 98–100] attached to the AC terminals) allow reducing motor stresses by filtering out switching-frequency voltage harmonics, where DC-link referenced filters [101–104] attenuate simultaneously Differential Mode (DM) and Common Mode (CM) HF noise. There, the high switching frequencies of WBG power semiconductors up to 100 kHz allow a very compact realization of the filter and a complete mitigation of audible inverter noise below 20 kHz. Converters employing WBG power semiconductors and full-sinewave filters were demonstrated to *increase* the overall system performance compared to Si IGBT inverters with unfiltered PWM waveforms, as the HF motor losses and the semiconductor switching losses can be significantly reduced [105–107]. Within this context, the recently introduced phase-modular buck-boost Twelve-Switch Buck-Boost Y-Inverter (12-YI) [58, 64, 67] (cf., **Fig. 2.2b**) featuring inherently sinusoidal AC output voltages (similar to a Six-Switch Current Source Inverter (6-CSI)) both above and below the DC-link voltage seems especially attractive, as it allows compatibility with a plurality of nominal DC-bus and/or motor voltages. The 12-YI is therefore considered for the following analysis.

The proliferation of VSDs with sinusoidal output voltages gives rise to the question if – or with what additional amount of filtering effort – such a system could allow operation with long unshielded motor cables. In [90], the impact of several output filter configurations on the conducted EMI emissions up to 30 MHz of a Si IGBT VSD operating with unshielded cables is analyzed, where a DC-link referenced filter structure provided a massive reduction of emission noise level. In [108–110] filter design guidelines are provided, considering the less stringent DO160 power interface limits (compared to the IEC 61800-3 limit values) on the DC side and on the AC side for a standard two-level 6-VSI, where only emissions up to 30 MHz are considered. It was further verified in [111] that radiated emission limits according to the IEC 61800-3 can be met with a sinewave filter for operation with a 5 m and a 75 m long cable. However, so far no comprehensive filter design guidelines for VSD operation with long unshielded cables according to the IEC 61800-3 including radiated and conducted emissions is available.

In this Chapter we use prior art in systematic EMI filter design of three-phase Power Factor Correction (PFC) rectifier systems within the scope of an existing 11 kW 12-YI VSD power stage according to the specifications in

Fig. 2.2a. In a first step, in **Sec. 2.2** the basic operating principle of the 12-YI – a converter with hybrid 6-VSI/6-CSI emission characteristics – is recapitulated and the impact of modulation and operating point on the HF emissions on DC and AC side is discussed. Subsequently, in **Sec. 2.3** measurement techniques for conducted power interface emissions are presented. An EMI equivalent circuit for the 12-YI is derived and filter design guidelines are presented. The radiated emission analysis and the related filter design is then conducted in **Sec. 2.4**, where the resulting electric field strength is estimated based on the converter CM currents. Then, in **Sec. 2.5** the 12-YI prototype with the derived filter structure on DC and AC side is detailed, and experimental verification of the EMI equivalent circuit and the design considerations is presented. Finally, the key findings are summarized in **Sec. 2.6**.

2.2 12-YI Topology

Requirements for future DC-fed VSDs include a wide applicability which means that the inverter needs to be capable of matching the DC supply voltage and the motor voltage for various motor types and supply voltage levels, where sinusoidal output phase voltages allow for low HF motor stresses and losses. Additionally, high efficiency and compactness remain crucial figures of merit, and are especially relevant in mobile applications. In collaboration with the *European Center for Power Electronics* (ECPE [82]), benchmark specifications for an 11 kW VSD were defined for a lighthouse project: A 230 V_{rms} motor (400 V_{rms} line-to-line, nominal stator frequency $f_{ac,nom} = 200$ Hz) is powered from a DC input voltage varying in a wide range of 400 V to 750 V (cf., **Fig. 2.2a**), hence requiring an inverter system with buck-boost functionality.

The recently introduced phase-modular buck-boost 12-YI [58, 64, 67] (the main power circuit is shown in **Fig. 2.2b**) features all above mentioned requirements and hence is selected for the analysis of operation with unshielded cables.

The operating principle of the 12-YI is recapitulated within the following two subsections, where the subsequent EMI filter design is conducted for an existing 12-YI hardware prototype (without explicit EMI filter) capable of covering the operating ranges shown in **Fig. 2.2a** and featuring a power density of 15 kW/dm^3 (246 W/in^3) and a nominal system efficiency of 98.3 %. Employing a switching frequency of $f_s = 100$ kHz, the prototype system comprises a buck-boost inductor of $L = 85$ µH, an effective AC capacitor of $C = 1.3$ µF, and a DC-link capacitor of $C_{dc} = 12$ µF. The employed 12-YI hardware prototype is further detailed in **Sec. 2.5**.

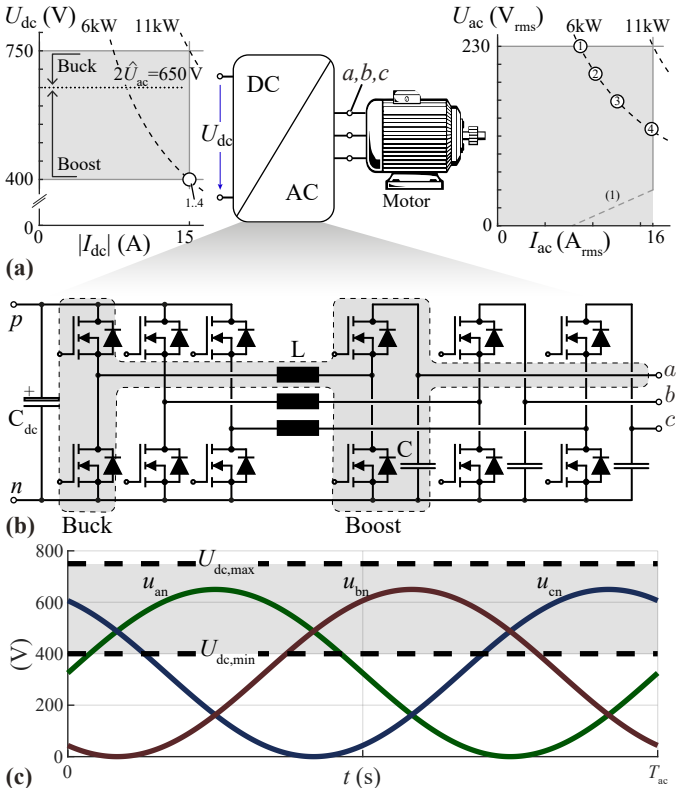

Fig. 2.2: (a) Illustration of the converter DC input and AC output voltage and current range specifications where $U_{dc} = 2\hat{U}_{ac}$=650 V represents the boundary of buck and boost operation. **(b)** Circuit diagram of the Twelve-Switch Buck-Boost Y-Inverter (12-YI) with inherent sinusoidal output voltages; no additional DC/DC converter stage is required for buck-boost capability. **(c)** 12-YI AC output voltages u_{an},u_{bn},u_{cn} with respect to the negative DC-link rail, as well as maximum and minimum DC input voltage U_{dc} of the converter operating range, clearly illustrating the need for buck-boost capability.
(1) Due to the limited semiconductor thermal capacitance the phase current is further restricted for low output frequencies below 50 Hz.

2.2.1 Operating Principle

The three-phase output voltages of the 12-YI with respect to the negative DC-link rail u_{an},u_{bn},u_{cn} are strictly positive and shown in **Fig. 2.2c** for standard modulation with a constant offset voltage. This offset voltage is present in all three output phase voltages and hence represents a CM component $u_{CM} = (u_{an} + u_{bn} + u_{cn})/3$ which does not drive a current in an open star point three-phase motor (cf., **Fig. 2.2a**), and, accordingly, sinusoidal phase currents i_a,i_b,i_c can be realized [58]. Note that the CM offset voltage u_{CM} is only restricted by the requirement of strictly positive output voltages and can be set such that Discontinuous PWM (DPWM) [112] [58] is achieved as shown in **Fig. 2.3b**. There, the phase module with the lowest instantaneous output voltage is not switched during one third of the fundamental period T_{ac}, but remains clamped to the negative DC-link rail, reducing the semiconductor switching losses for unity power factor operation by at least one third. Aiming at ultra-compact and highly efficient operation, the 12-YI hardware prototype employed for the filter design analysis operates with DPWM.

Each of the three 12-YI phase modules consists of a DC/DC buck-boost converter and is controlled independently. Therefore, the modulation is explained here for module *a* only (for more details refer to [58]), which is highlighted for boost and buck operation in **Fig. 2.3a**. The modulation strategy aims at single-stage HF energy conversion in each phase module:

- In boost operation (i.e., when $u_{an} > U_{dc}$, cf., **Fig. 2.3a.i**) the high-side switch of the buck stage is permanently turned on, while the output voltage is controlled by PWM operating the boost stage with a duty cycle d_{Bo}, where the low frequency inductor current $\langle i_L \rangle = i_a/d_{Bo}$ is elevated compared to the phase current (cf., **Fig. 2.3d**).

- In buck operation (i.e., when $u_{an} \leq U_{dc}$, cf., **Fig. 2.3a.ii**), the high-side switch of the boost stage is permanently turned on, and the buck stage is PWM operated with a duty cycle d_{Bu} in order to regulate the output voltage, where the low-frequency inductor current is equal to the sinusoidal phase current $\langle i_L \rangle = i_a$ (cf., **Fig. 2.3d**).

Duty cycles enabling mutually exclusive HF operation of the buck and boost stage can be derived using the instantaneous modulation depth $m(t) = u_{an}(t)/U_{dc}$ (the global modulation index is $M = 2 \cdot \hat{U}_{ac}/U_{dc}$) and are shown in **Fig. 2.3c**:

$$d_{Bu}(t) = \min(1, m(t)), \quad d_{Bo}(t) = \min(1, 1/m(t)) \tag{2.1}$$

The HF peak inductor current ripple $\Delta I_{\mathrm{L,pk}}$ (cf., **Fig. 2.3d**) for buck and boost operation (assuming a negligible switching-frequency voltage ripple of the DC-link voltage and the phase output capacitor voltages) is then defined by

$$\Delta I_{\mathrm{L,pk}} = \begin{cases} \frac{1}{2}\frac{d_{\mathrm{Bu}}(1-d_{\mathrm{Bu}})U_{\mathrm{dc}}}{f_{\mathrm{s}}L} & \text{(Buck)} \\ \frac{1}{2}\frac{d_{\mathrm{Bo}}(1-d_{\mathrm{Bo}})u_{\mathrm{an}}}{f_{\mathrm{s}}L} & \text{(Boost)}\,. \end{cases} \tag{2.2}$$

2.2.2 HF Emissions in the Time Domain

As mentioned, the 12-YI is a hybrid 6-VSI/6-CSI topology. **Fig. 2.3e** shows the equivalent circuit for the HF input and output emissions of the 12-YI phase module a for buck and boost operation. **Fig. 2.3e.i** shows module a in boost operation (i.e., corresponding to a 6-CSI module [51]), where the switched current in the boost stage high-side semiconductor $i_{\mathrm{T,Bo}}$ is flowing towards the output capacitor C and the boost stage switch-node voltage u_{Bo} causes the HF current ripple on the inductor L which is clamped to the positive DC-link rail and $i_{\mathrm{T,Bu}} = i_{\mathrm{L}}$. **Fig. 2.3e.ii** highlights module a in buck operation (i.e., corresponding to a 6-VSI module), where the switched current in the buck stage high-side semiconductor $i_{\mathrm{T,Bu}}$ is flowing from the DC-link, while the buck stage switch-node voltage u_{Bu} causes the HF current ripple on the inductor L which is clamped to the upper terminal of the output capacitor C and $i_{\mathrm{T,Bo}} = i_{\mathrm{L}}$. In **Fig. 2.4a-d**, the calculated peak HF charge variations $Q_{\mathrm{dc,pk}}$ of the DC input capacitor C_{dc} and $Q_{\mathrm{ac,pk}}$ of the 12-YI phase module a AC output capacitor C are shown for the operation with DPWM, $U_{\mathrm{dc}} = 400\,\mathrm{V}$, and the AC operating points ①-④ depicted in **Fig. 2.2a** (i.e., with an output power of 6 kW). The switching frequency and buck-boost inductor value are set according to the prototype specifications (i.e., $f_{\mathrm{s}} = 100\,\mathrm{kHz}$, synchronous PWM carriers for all three phase modules and $L = 85\,\mu\mathrm{H}$). The peak HF voltage ripple on the DC capacitor and the AC capacitor is obtained by dividing $Q_{\mathrm{dc,pk}}$ and $Q_{\mathrm{ac,pk}}$ by the corresponding capacitance C_{dc} and C, respectively.

AC-Side HF Charge Variation

The peak AC charge variation $Q_{\mathrm{ac,pk}}$ depends solely on the operation of the considered phase module (cf., **Fig. 2.3e**). Hence, assuming a purely sinusoidal phase output current without HF content, $\Delta Q_{\mathrm{ac,pk}}$ is given by the integral of

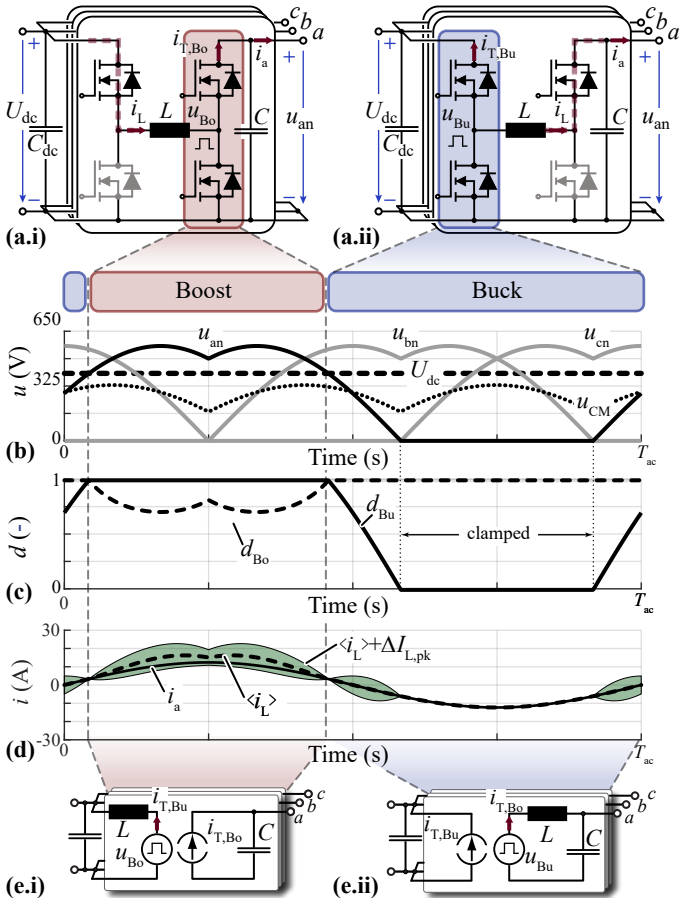

Fig. 2.3: Operation concept of the 12-YI highlighted for phase module a in **(a.i)** boost operation (i.e., when $u_{an} > U_{dc}$) and **(a.ii)** buck operation (i.e., when $u_{an} \leq U_{dc}$). **(b)** DC-link voltage U_{dc} and phase output voltages with respect to the negative DC-link rail u_{an},u_{bn},u_{cn} comprising a time-varying CM offset voltage u_{CM} to enable Discontinuous PWM (DPWM). **(c)** Module a duty cycle of the buck stage d_{Bu} and of the boost stage d_{Bo}. **(d)** Relevant current waveforms of module a including the phase output current i_a, low-frequency inductor current $\langle i_L \rangle$ and inductor current i_L. **(e)** Equivalent circuit for the time domain HF input and output voltage emissions of the 12-YI phase module a depending on the operation mode.

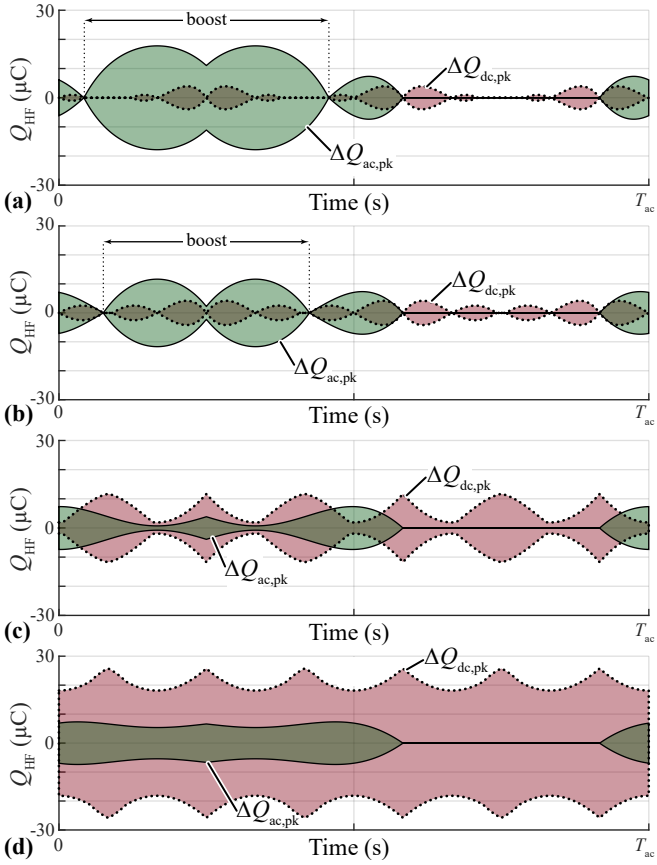

Fig. 2.4: Calculated peak HF charge variations $Q_{dc,pk}$ of the DC input capacitor C_{dc} and $Q_{ac,pk}$ of the AC output capacitor C of phase module a for the 12-YI operating with DPWM and U_{dc} = 400 V, where **(a)-(d)** correspond to the AC operating points ①-④ depicted in **Fig. 2.2a**. The peak HF voltage ripple on DC and AC capacitor is obtained by dividing $Q_{dc,pk}$ and $Q_{ac,pk}$ with its corresponding capacitance C_{dc} and C, respectively. Note that the peak AC charge variation $Q_{ac,pk}$ depends solely on the operation of the considered phase module, whereas the peak DC charge variation $Q_{dc,pk}$ depends on the operation of all three modules (cf., **Fig. 2.3e**).

the HF boost high-side semiconductor current $i_{\mathrm{T,Bo}}$:

$$\Delta Q_{\mathrm{ac,pk}} = \begin{cases} \frac{\Delta I_{\mathrm{L,pk}}}{8 f_s} = \frac{d_{\mathrm{Bu}}(1-d_{\mathrm{Bu}})U_{\mathrm{dc}}}{16 f_s^2 L} \leq 13.8\,\mu\mathrm{C} & \text{(Buck)} \\ \frac{1}{2}\frac{(1-d_{\mathrm{Bo}})i_{\mathrm{a}}}{f_s} \leq 17.6\,\mu\mathrm{C} & \text{(Boost)}\,. \end{cases} \tag{2.3}$$

For buck operation $\Delta Q_{\mathrm{ac,pk}}$ scales with the peak value $\Delta I_{\mathrm{L,pk}}$ of the triangular inductor current ripple and hence is independent of the phase output current. For a given DC-link voltage, the maximum charge variation results for $d_{\mathrm{Bu}} = 0.5$ and is equal to 7.4 µC for $U_{\mathrm{dc}} = U_{\mathrm{dc,min}} = 400\,\mathrm{V}$ in **Fig. 2.4a-d**, where up to 13.8 µC result for $U_{\mathrm{dc}} = U_{\mathrm{dc,max}} = 750\,\mathrm{V}$.

In contrast, for boost operation, $\Delta Q_{\mathrm{ac,pk}}$ results due to the square-wave current $i_{\mathrm{T,bo}}$ (cf., **Fig. 2.3e.i**) and does not depend on the selected inductance value L but scales with the phase current i_{a} (i.e., is load dependent), where the maximum HF charge variation of 17.6 µC results for the maximum boosting effort and nominal power operation at $U_{\mathrm{dc}} = U_{\mathrm{dc,min}} = 400\,\mathrm{V}$ as shown in **Fig. 2.4a**. Note that (2.3) assumes that $\Delta I_{\mathrm{L,pk}}$ does not impact $\Delta Q_{\mathrm{ac,pk}}$ in boost operation (i.e., $\Delta I_{\mathrm{L,pk}} < \hat{I}_{\mathrm{ac}} \cdot (1/d_{\mathrm{Bo}} - 1)$), which holds for the prototype specifications and nominal power operation.

DC-Side HF Charge Variation

In contrast to the AC-side emissions, the peak DC-side charge variation $Q_{\mathrm{dc,pk}}$ depends on the operation of all modules (cf., **Fig. 2.3e**), where the independent phase modules operate with 120° phase-shifted AC output voltages (cf., **Fig. 2.3b**) and hence the three modules may not work in the same mode (i.e., buck or boost operation) at a given point in time.

Since a phase module in buck operation causes a square-wave current $i_{\mathrm{T,Bu}}$, while a module in boost operation causes a continuous current $i_{\mathrm{T,Bu}}$ (with only a HF ripple $\Delta I_{\mathrm{L,pk}}$) flowing from the DC-link, buck operation can be assumed to dominate the worst case DC-side HF peak charge variation (which is consistent with the operating points considered in **Fig. 2.4**). Modeling the 12-YI as a 6-VSI for the DC emissions, $\Delta Q_{\mathrm{dc,pk}}$ can be conservatively approximated with [113]

$$\Delta Q_{\mathrm{dc,pk}} = \frac{1}{8}\frac{\hat{I}_{\mathrm{ac}}}{f_{\mathrm{s}}} \leq 28.3\,\mu\mathrm{C}, \tag{2.4}$$

i.e., by assuming a switching frequency square-wave current with 50 % duty cycle and an amplitude of half the phase current amplitude $0.5 \cdot \hat{I}_{\mathrm{ac}}$, where the maximum charge variation of 28.3 µC results for operation with the maximum AC output current $I_{\mathrm{ac,max}}$ =16.3 $\mathrm{A_{rms}}$ (cf., **Fig. 2.2a**) as displayed in **Fig. 2.4d**.

2.3 Conducted EMI Analysis and Filter Design

In order to allow a systematic EMI filter design, (a) the noise emission measurement method needs to be specified, (b) the EMI noise emission equivalent circuit of the selected power converter topology needs to be derived and (c) the required filter attenuation needs to be determined based on the considered emission limits. Accordingly, possible measurement techniques and a setup to evaluate the power interface emissions are discussed in **Sec. 2.3.1**, in **Sec. 2.3.2** an EMI equivalent circuit for the 12-YI is derived which is used in the filter design procedure in **Sec. 2.3.3** to assess the required DM and CM HF attenuation to comply with the IEC 61800-3 emission limits.

2.3.1 Measurement Method

DC Interface

Limiting the DC power interface emissions of basic drive modules (or the grid interface emissions of complete drive modules, cf., **Fig. 2.1)** is a standard task when designing a VSD and, accordingly, a vast amount of publications on filter design exists for both 6-VSI and 6-CSI drives [51] [114], where the emissions are recorded using a Line Impedance Stabilization Network (LISN) (referred to as Artificial Mains Network (AMN) in the IEC 61800-3). In this work, the DC interface emissions are also evaluated with a LISN serving several purposes: First, the LISN comprises a filter towards the DC source, such that only noise originating from the VSD is recorded. Second, the LISN represents at frequencies larger than 150 kHz and up to 30 MHz an almost constant source impedance of 50 Ω for the attached VSD, and third, the LISN allows to feed the VSD HF emissions into an EMI test receiver.

AC (Output) Interface

Employing predominantly shielded cables, the motor-side EMI emissions of a VSD were of less interest in literature (or only within the scope of HF motor stresses and losses). In case of a standard 6-VSI where the unfiltered PWM pulses are directly applied to the motor cable, the resulting HF emissions are several orders of magnitude larger compared to rectifier applications and hence exceed the operation limits of any three-phase LISN [90]. Hence, the IEC 61800-3 standard suggests the usage of a 1.5 kΩ high-impedance voltage probe. (Alternatively, the effectiveness of the filter structure can be assessed by establishing a coupling between the motor cable and the mains input cable

during the measurement of the grid interface EMI emissions [84].) However, there (in contrast to a measurement with a LISN) no clearly defined and constant (over frequency) load impedance exists on the VSD AC terminals, but the load impedance is highly dependent on the employed motor as well as the cable type, length and arrangement [115]. Further, the DM and CM emissions cannot be separated, complicating the filter debugging process in case the emission limits are not met. Alternatively, in [90] the conducted CM EMI emissions were evaluated separately using a capacitive voltage clamp. DM and CM noise splitting was enabled in [116] using a resistive voltage divider, and in [92] [117] based on four current measurements, where the dependency of the load impedance (and hence the measurement results) on the specific setup remains.

Here, the HF emission target given for the AC power interface for operation with unshielded motor cables lies within the range of grid emission limits and employing a three-phase AC LISN is therefore possible. As the LISN decouples the converter from the motor for the relevant frequencies $> 150\,\text{kHz}$, the emission level can also be evaluated using a resistive three-phase load, greatly simplifying the EMI measurement process. Note that the LISN impedance ($\approx 50\,\Omega$ for $f > 150\,\text{kHz}$) aims at approximating the grid impedance, and is not fully representative for the impedance of a motor [118] [119] [83]. Further, in [120–122] a large dependency of the EMI emissions on the cable and motor impedance was found for inverters without sine-filter. It is important to mention, that first, also the LISN does not fully represent the complex grid impedance [123] and it was found in [124], that the grid impedance in practice may vary in a wide range from $2\,\Omega$ to $450\,\Omega$ within the conducted emission band, where the selected $50\,\Omega$ LISN impedance is a compromise allowing for clear and reproducible measurement results. Second, when applying a sine-filter, the measured emissions are less dependent on the AC load impedance, compared to the case where the PWM pulses are directly applied to the motor cable [95] [51] [113].

Accordingly, for the filter design a HF impedance of $50\,\Omega$ (i.e., the presence of a LISN) is assumed, and in a first step in **Sec. 2.5.1** the experimental emission measurements are conducted employing a LISN and a resistive three-phase load. Then, in a second step in **Sec. 2.5.1** the emissions are evaluated with a high-impedance voltage probe when the converter is driving a motor, where the close matching of the results supports the selected measurement strategy.

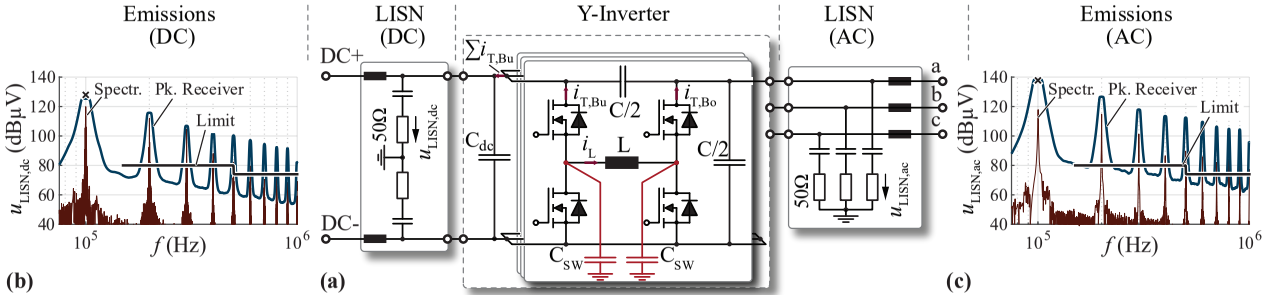

Fig. 2.5: (a) Main power circuit of the 12-YI with a Line Impedance Stabilization Network (LISN) connected on the DC side and on the AC side. The parasitic switch-node capacitances are highlighted in red. The simulated voltage spectrum (red), the resulting peak detector signal (blue), as well as the IEC 61800-3 C1 power interface emission limits (black) on DC side and on the AC side are shown in **(b)** and **(c)**, respectively.

2.3.2 12-YI EMI Equivalent Circuit

The main power circuit of the 12-YI attached to a (simplified) LISN on both input (DC) and output (AC) side is shown in **Fig. 2.5a**. There, the AC output capacitor of each phase module is equally referenced to the positive and negative DC-link rail in order to reduce the capacitance variation of the employed non-linear capacitors (as is discussed in more detail in **Sec. 2.3.3**), and the parasitic switch-node capacitances C_{SW} are highlighted in red. The simulated emission spectrum and the peak detector signal [125] on the DC side and the AC side are also displayed in **Fig. 2.5b** and **Fig. 2.5c**, respectively, for the specifications of the existing 12-YI hardware prototype (i.e., operation with DPWM, $f_{\mathrm{s}} = 100\,\mathrm{kHz}$, $C_{\mathrm{dc}} = 12\,\mu\mathrm{F}$, $L = 85\,\mu\mathrm{H}$ and $C = 1.3\,\mu\mathrm{F}$) and the operating point depicted in **Fig. 2.4a** ($U_{\mathrm{dc}} = 400\,\mathrm{V}$, $U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$ (i.e., modulation index $M = 1.6$) and nominal output power of 6 kW).

The knowledge of the relevant emission mechanisms of the employed power converter topology is crucial for the conducted EMI filter design process, where an abundance of publications on emission mechanisms for three-phase voltage source (i.e., boost-type) PWM rectifiers [126–129] and current source (i.e., buck-type) PWM rectifiers [130–132] exists (note that a bidirectional boost-type PWM rectifier corresponds to a buck-type PWM inverter and vice versa). As discussed in **Sec. 2.2**, the 12-YI is a hybrid 6-VSI (i.e., buck-type) and 6-CSI (i.e., boost-type) inverter topology, where the independent phase modules may work in different modes for a given point in time (cf., **Fig. 2.3**), and so far no EMI equivalent circuit has been presented for the 12-YI in literature. A detailed derivation of the 12-YI EMI equivalent circuit is performed in the following, allowing to quantify the conducted EMI emissions. This information is then used in **Sec. 2.3.3** to determine the required DM and CM filter attenuation for DC and AC side.

As highlighted in **Fig. 2.6**, a single half-bridge of the 12-YI buck stage represents a current source $i_{\mathrm{T,Bu}}$ towards the input terminals DC^{+} and DC^{-}, and a voltage source u_{Bu} towards the switch-node terminal $\mathrm{SW_{Bu}}$ (a half-bridge of the boost stage can be modeled analogously).

Employing this modeling approach to the buck stage and boost stage half-bridges of the main 12-YI power circuit from **Fig. 2.5a**, the equivalent circuit shown in **Fig. 2.7a** results. Further, **Fig. 2.7b** illustrates the power circuit from **Fig. 2.7a** with a separate DM/CM representation of the voltage and current sources: The buck stage voltages u_{Bu} of the modules a, b, c are split into a single CM voltage $u_{\mathrm{CM,Bu}} = 1/3 \sum u_{\mathrm{Bu}}$ and three DM voltages $u_{\mathrm{DM,Bu}}$ (e.g., $u_{\mathrm{DM,Bu,a}} = u_{\mathrm{Bu,a}} - u_{\mathrm{CM,Bu}}$, with $\sum u_{\mathrm{DM,Bu}} = 0$), and the same DM/CM splitting is also performed for the boost stage voltages u_{Bo}. Similarly, each of the boost

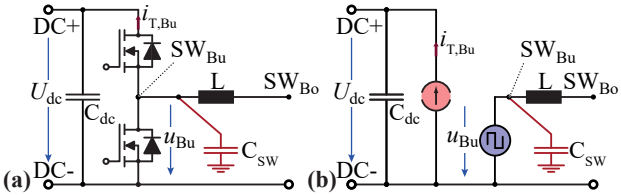

Fig. 2.6: (a) Single 12-YI buck stage half-bridge, and **(b)** voltage and current source based equivalent circuit, where the half-bridge represents a current source ($i_{T,Bu}$) towards the input terminals DC^+ and DC^-, and a voltage source (u_{Bu}) towards the switch-node terminal SW_{Bu} (with a parasitic capacitance C_{SW} to Protective Earth (PE)). This modeling approach is also applicable to the boost stage half-bridges.

stage currents $i_{T,Bo}$ is represented by a CM current $i_{T,Bo,CM} = 1/3 \sum i_{T,Bo}$ and a parallel DM current $i_{T,Bo,DM}$ (e.g., $i_{T,Bo,DM,a} = i_{T,Bo,a} - i_{T,Bo,CM}$, with $\sum i_{DM} = 0$). The DM/CM current splitting is also applied to the buck stage currents, where the buck DM currents cancel out in the DC-link rails and are hence irrelevant for the EMI emission formation. Accordingly, only the buck CM current $\sum i_{T,Bu}$ is shown in the equivalent circuit in **Fig. 2.7b**, which allows now to identify the relevant EMI emission sources and paths.

DC-Side DM Emissions

Fig. 2.8a shows the DM part of the simulated DC-side voltage spectrum presented in **Fig. 2.5b**, and **Fig. 2.8b** illustrates the relevant emission sources and paths. There, the buck CM currents $\sum i_{T,Bu}$ close through the DC-link capacitor and the $DC^{+/-}$ referenced AC-side filter capacitors $3C/2$ (cf., **Fig. 2.7b**). Given the symmetric AC-side filter structure, the two nodes labelled with $(*)$ remain at the same potential, such that no current is flowing through the AC LISN and no DM/CM conversion takes place (the impact of the parasitic capacitances C_{SW} to Protective Earth (PE) is neglected here). Moreover, approximately half the boost CM current $1/2 \sum i_{T,Bo}$ closes through the positive DC-link rail if $C_{dc} >> 3C/2$ (i.e., the voltage drop across C_{dc} can be neglected).

The currents closing through the DC-link capacitor cause a HF voltage variation $u_{C,dc,HF}$ [133], which is also applied to the series connection of the two DC LISN resistors with opposite sign, hence representing a DM emission.

As the 50 Ω LISN resistors are large compared to a capacitor in the µF range for frequencies ≥ 150 kHz, they do not impact the resulting HF voltage variation on DC-link capacitor C_{dc} (the same also holds for the output capacitors C). Further, the impedance of the 250 nF LISN capacitors is < 10% of the

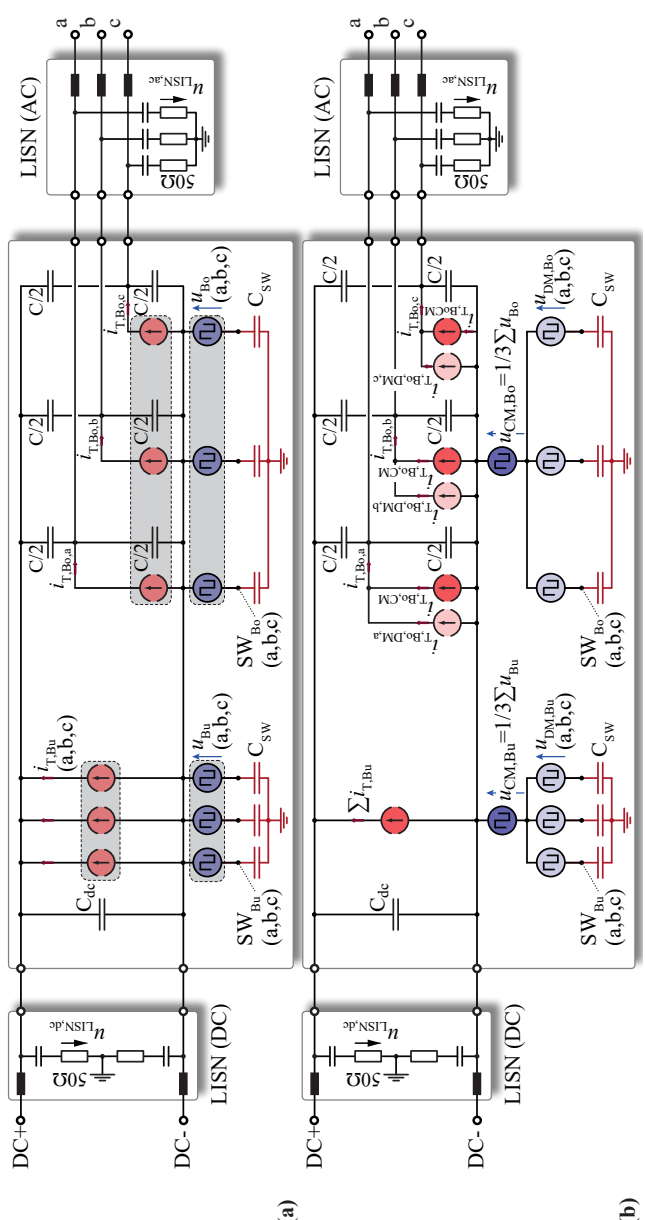

Fig. 2.7: (a) 12-YI main power circuit from **Fig. 2.5a** with the buck stage and boost stage half-bridges modelled according to **Fig. 2.6**. **(b)** 12-YI power circuit with a separate DM/CM representation of the voltage and current sources. Since the buck DM currents cancel out in the DC-link rails only the buck CM current $\sum i_{T,Bu}$ is shown.

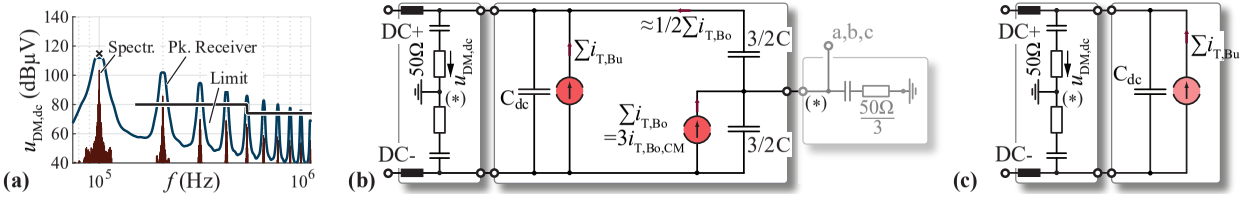

Fig. 2.8: DC-side DM emission equivalent circuit: **(a)** Simulated DM voltage spectrum, **(b)** relevant emission sources and paths, and **(c)** simplified equivalent circuit.

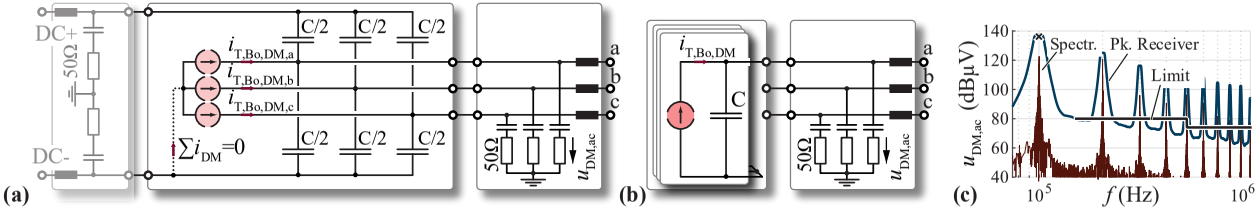

Fig. 2.9: AC-side DM emission equivalent circuit: **(a)** Relevant emission sources and paths, **(b)** simplified equivalent circuit, and **(c)** simulated DM voltage spectrum.

50 Ω LISN resistors for frequencies ≥ 150 kHz and, accordingly, the resulting DM emissions can be approximated with

$$\hat{u}_{\mathrm{DM,dc}} = \frac{1}{2}\hat{u}_{\mathrm{C,dc,HF}}, \tag{2.5}$$

i.e., the DM emissions reduced by 6 dB compared to $\hat{u}_{\mathrm{C,dc,HF}}$.

Fig. 2.8c presents a simplified DC-side DM equivalent circuit where the impact of $1/2 \sum i_{\mathrm{T,Bo}}$ and the path through $3C/2$ on the DC-side DM emissions is neglected. As discussed in **Sec. 2.2.2**, the HF current fed into the positive DC-link rail $i_{\mathrm{T,Bu}}$ is a square-wave current in buck and solely a triangular HF current ripple in boost operation. Accordingly, buck operation is assumed to dominate the DC-side peak voltage ripple. For switching frequencies below the regulated conducted emissions band (i.e., $f_{\mathrm{s}} < 150\,\mathrm{kHz}$), this is further accentuated by the fact that the frequency spectrum of a triangular HF current $i_{\mathrm{T,Bu}}$ in boost operation shows a decay of approximately −40 dB/dec (i.e., with $1/f^2$), whereas the spectrum of the square-wave current $i_{\mathrm{T,Bu}}$ in buck operation decays only with −20 dB/dec (i.e., with $1/f$) [134]. In [134] it is further suggested to conservatively assign the resulting HF peak charge variation $\Delta Q_{\mathrm{dc,pk}}$ according to (2.4) to a single switching-frequency current component in the frequency domain, and assuming a decay of the current spectrum according to the current waveform (i.e., here −20 dB/dec for a square-wave signal). Hence, the DC-side DM emission formation of the 12-YI in the frequency domain can be approximated with

$$\hat{u}_{\mathrm{C,dc,HF}}(nf_{\mathrm{s}}) = \frac{1}{2\pi n f_{\mathrm{s}} C_{\mathrm{dc}}} \frac{2\pi f_{\mathrm{s}} \Delta Q_{\mathrm{dc,pk}}}{n}, \tag{2.6}$$

where $n = 1, 2, 3, \ldots$ represents the switching frequency harmonics at nf_{s}. The estimated peak DM emissions using (2.5) and (2.6) of $\hat{u}_{\mathrm{DM,dc}}(100\,\mathrm{kHz}) = 116\,\mathrm{dB\mu V}$ for the considered operation point are represented by a cross in **Fig. 2.8a** and nicely matches the simulated peak emissions, where $\hat{x}(f)[\mathrm{dB\mu V}] = 20\log_{10}(\frac{\hat{x}(f)}{1\,\mu\mathrm{V}\sqrt{2}})$.

AC-Side (Output) Emissions

As presented in **Fig. 2.7b**, both DM and CM components of the AC-side currents $i_{\mathrm{T,Bo}}$ are relevant for the emission formation. Again, the frequency spectrum of $i_{\mathrm{T,Bo}}$ can be approximated with the peak charge variation $\Delta Q_{\mathrm{ac,pk}}$ (2.3) as

$$\hat{i}_{\mathrm{T,Bo}}(nf_{\mathrm{s}}) = \frac{2\pi f_{\mathrm{s}} \Delta Q_{\mathrm{ac,pk}}}{n^k}, \tag{2.7}$$

where the current spectrum decays with $k = 2$ in buck operation (triangular current, decaying with $-40\,\mathrm{dB/dec}$) and $k = 1$ in boost operation (square-wave current, decaying with $-20\,\mathrm{dB/dec}$) [134]. For the given converter specifications, the maximum $\Delta Q_{\mathrm{ac,pk}}$ occurs in boost operation. Hence the frequency spectrum of the DM and CM currents can be approximated assuming two modules in buck operation and with negligible HF currents (e.g., $\hat{i}_{\mathrm{T,Bo,b}} \approx \hat{i}_{\mathrm{T,Bo,c}} \approx 0$), while the remaining module in boost operation dominates the HF emissions (e.g., $i_{\mathrm{T,Bo,a}} = \hat{i}_{\mathrm{T,Bo}}$), such that

$$\hat{i}_{\mathrm{T,Bo,CM}}(nf_{\mathrm{s}}) = \frac{1}{3}\sum_{a,b,c}\hat{i}_{\mathrm{T,Bo}}(nf_{\mathrm{s}}) \approx \frac{1}{3}\hat{i}_{\mathrm{T,Bo}}(nf_{\mathrm{s}}), \tag{2.8}$$

$$\hat{i}_{\mathrm{T,Bo,DM}}(nf_{\mathrm{s}}) = \hat{i}_{\mathrm{T,Bo}} - \hat{i}_{\mathrm{T,Bo,CM}} \approx \frac{2}{3}\hat{i}_{\mathrm{T,Bo}}(nf_{\mathrm{s}}). \tag{2.9}$$

Hence, the DM and CM currents are reduced by ≈4 dB (i.e., scaled by 2/3) and ≈10 dB (i.e., scaled by 1/3), respectively, compared to $\hat{i}_{\mathrm{T,Bo}}$.

The boost stage DM currents $i_{\mathrm{T,Bo,DM}}$ shown in **Fig. 2.7b** can equally close through $C/2$ via DC^{+} and DC^{-} and thereby cause HF DM voltages on the AC output terminals, as highlighted in **Fig. 2.9a**. Hence, the simplified AC-side DM equivalent circuit in **Fig. 2.9b** comprises per phase module a total capacitance C and (neglecting the impact of the LISN on the HF voltage variation on C) the AC-side DM emissions are defined by

$$\hat{u}_{\mathrm{DM,ac}}(nf_{\mathrm{s}}) = \hat{u}_{\mathrm{C,HF,DM}}(nf_{\mathrm{s}}) = \frac{\hat{i}_{\mathrm{T,Bo,DM}}(nf_{\mathrm{s}})}{2\pi nf_{\mathrm{s}}C}. \tag{2.10}$$

The estimated peak DM emissions $\hat{u}_{\mathrm{DM,ac}}(100\,\mathrm{kHz}) = 136\,\mathrm{dB\mu V}$ for the considered operation point are represented by a cross in **Fig. 2.9c** and nicely match the simulated peak emissions. Note, that for identical parasitic capacitances C_{SW} in all three modules (cf., **Fig. 2.7b**), the buck stage $u_{\mathrm{DM,Bu}}$ and boost stage DM voltages $u_{\mathrm{DM,Bo}}$ cause no current through the DC- and AC-side LISN resistors and are therefore not shown in **Fig. 2.9a** and **Fig. 2.9b**.

Finally, the relevant emission sources and paths for CM emissions is shown in **Fig. 2.10a**. With $C_{\mathrm{dc}} >> 3C/2$, approximately half the boost stage CM current $1/2\sum i_{\mathrm{T,Bo}}$ returns via the positive DC-link rail (cf., **Fig. 2.7b**), and hence the boost CM current path comprises a total capacitance $3C$ (the positive and negative DC-link rails are represented here as a single rail $\mathrm{DC}^{+/-}$). Further, the buck $u_{\mathrm{CM,Bu}}$ and boost stage CM voltage $u_{\mathrm{CM,Bo}}$ connect to PE via $3 \cdot C_{\mathrm{SW}}$.

Here, in a first step, the emissions due to the CM current $\sum i_{\mathrm{T,Bo}}$ are assessed, and the emissions resulting due to the buck stage CM voltage $u_{\mathrm{CM,Bu}}$

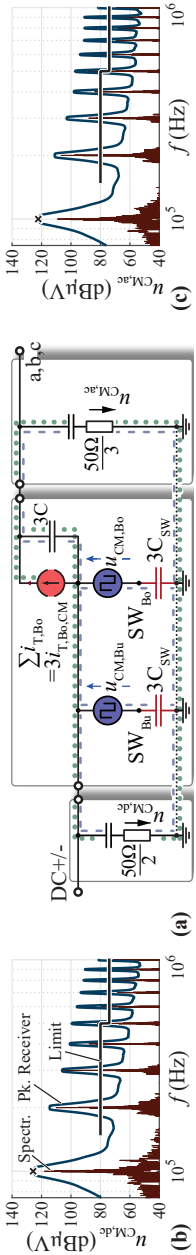

Fig. 2.10: **(a)** CM equivalent circuit of the 12-YI and simulated voltage spectrum on **(b)** DC side and **(c)** AC side.

as well as the boost stage CM voltage $u_{\mathrm{CM,Bo}}$ are discussed in the next subsection. The AC capacitor $3C$ CM HF voltage spectrum $\hat{u}_{\mathrm{C,HF,CM}}$ is defined by $\sum \hat{\underline{i}}_{\mathrm{T,Bo}} = 3\hat{\underline{i}}_{\mathrm{T,Bo,CM}}$ (cf., (2.8))

$$\hat{u}_{\mathrm{C,HF,CM}}(nf_{\mathrm{s}}) = \frac{\sum \hat{\underline{i}}_{\mathrm{T,Bo}}(nf_{\mathrm{s}})}{2\pi nf_{\mathrm{s}}3C} = \frac{\hat{\underline{i}}_{\mathrm{T,Bo,CM}}(nf_{\mathrm{s}})}{2\pi nf_{\mathrm{s}}C}, \tag{2.11}$$

resulting to $\hat{u}_{\mathrm{C,HF,CM}}(100\,\mathrm{kHz}) = 130\,\mathrm{dB\mu V}$ for the considered operation point. This voltage is applied to the series connection of the AC and DC LISN forming a voltage divider (cf., dotted line in **Fig. 2.10a**) with

$$\hat{u}_{\mathrm{CM,dc}}(nf_{\mathrm{s}}) = 0.6 \cdot \hat{u}_{\mathrm{C,HF,CM}}(nf_{\mathrm{s}}) \tag{2.12}$$

$$\hat{u}_{\mathrm{CM,ac}}(nf_{\mathrm{s}}) = 0.4 \cdot \hat{u}_{\mathrm{C,HF,CM}}(nf_{\mathrm{s}}). \tag{2.13}$$

Hence, the recorded LISN CM voltages $\hat{u}_{\mathrm{CM,dc}}$ and $\hat{u}_{\mathrm{CM,ac}}$ are reduced by $\approx$4 dB and $\approx$8 dB, respectively, compared to $\hat{u}_{\mathrm{C,HF,CM}}$ and the expected CM emissions are given by $\hat{u}_{\mathrm{CM,dc}}(100\,\mathrm{kHz}) = 126\,\mathrm{dB\mu V}$ (cf., **Fig. 2.10b**) and $\hat{u}_{\mathrm{CM,ac}}(100\,\mathrm{kHz}) = 123\,\mathrm{dB\mu V}$ (cf., **Fig. 2.10c**), again matching the simulated emissions.

Additional Common Mode Emissions

The 12-YI emission mechanisms discussed so far can be considered modulation imposed, as they can easily be calculated for given converter specifications and operating point using the equations from **Sec. 2.2**. Further, since the impedance of capacitors in the µF range above 100 kHz is much smaller than the 50 Ω LISN resistors, the filter capacitors of the 12-YI depicted in **Fig. 2.5a** are not substantially loaded when attaching a LISN and hence the recorded emission spectrum should not change notably if e.g., the emissions are measured on a resistance higher than 50 Ω or if the measurement is conducted with a high-impedance voltage probe (cf., **Fig. 2.17b**) when the 12-YI is driving a motor.

An additional emission path not yet discussed originates from the parasitic capacitances C_{SW} of the switch nodes of buck and boost stages to PE (cf., **Fig. 2.7b**, **Fig. 2.10a**) existing in a practical converter realization. The total parasitic capacitance $6 \cdot C_{\mathrm{SW}}$ provides a current path for the total HF CM switch-node voltage $1/2(u_{\mathrm{Bu,CM}} + u_{\mathrm{Bo,CM}}) = 1/6 \sum(u_{\mathrm{Bu}} + u_{\mathrm{Bo}})$ to PE (dashed line in **Fig. 2.10a**), where AC and DC LISN form a parallel return path to the DC-link rail $\mathrm{DC}^{+/-}$ (i.e., DC and AC side show the same emission level). As the capacitance C_{SW} is not part of the 12-YI main power circuit, this additional source of emissions is referred to as parasitically imposed.

The CM component of the switch-node voltages in the frequency domain can be approximated conservatively with

$$1/6 \sum (u_{\mathrm{Bu}} + u_{\mathrm{Bo}})(nf_{\mathrm{s}}) \approx \frac{2}{n\pi} \frac{k_{\mathrm{a}}}{6} u_{\mathrm{SW,max}}, \tag{2.14}$$

by assuming a square-wave switched voltage with an amplitude of $1/2 \cdot u_{\mathrm{SW,max}}$ and a duty cycle of 50 %, with $u_{\mathrm{SW,max}} = \max(U_{\mathrm{dc}}, 2\hat{U}_{\mathrm{ac}})$ the maximum switched voltage for a given operation point, and $k_{\mathrm{a}}/6$ as scaling factor representing the number of HF operated half-bridges relative to the total number of six half-bridges (i.e., $k_{\mathrm{a}} = 3$ for PWM and $k_{\mathrm{a}} = 2$ for DPWM). The recorded CM voltage on DC and AC LISN due to the switch-node parasitic capacitance C_{SW} can be approximated with

$$\hat{u}_{\mathrm{CM,par}}(nf_{\mathrm{s}}) \approx \frac{2}{n\pi} \frac{k_{\mathrm{a}}}{6} \frac{u_{\mathrm{SW,max}}}{Z_{6\cdot\mathrm{C,SW}}(nf_{\mathrm{s}})} R_{\mathrm{DC,AC}}, \tag{2.15}$$

where $R_{\mathrm{DC,AC}} = 10\,\Omega$ is the parallel resistance of DC and AC LISN, and $Z_{6\cdot\mathrm{C,SW}}$ the impedance of the total parasitic capacitance $6 \cdot C_{\mathrm{SW}}$. The parasitic switch-node capacitance C_{SW} is typically very small and a value of $C_{\mathrm{SW}} = 20\,\mathrm{pF}$ was measured for the converter prototype with floating heat sinks. Hence, for the considered operating point an emission level of $\hat{u}_{\mathrm{CM,par}}(100\,\mathrm{kHz}) = 99\,\mathrm{dB\mu V}$ results on DC and AC side of the 12-YI, which is more than 20 dB below the modulation imposed CM emissions, thus in this case the impact on the overall CM emissions shown in **Fig. 2.10b** and **Fig. 2.10c** is small.

However, it is important to highlight that $|Z_{6\cdot\mathrm{C,SW}}(100\,\mathrm{kHz})| = 13\,\mathrm{k\Omega} >> R_{\mathrm{DC,AC}}$, and hence $Z_{6\cdot\mathrm{C,SW}}$ dominates the total impedance of the current path represented by the dashed line in **Fig. 2.10a** up to frequencies in the range of 10 MHz. Hence, the parasitically imposed emissions $\hat{u}_{\mathrm{CM,par}}$ according to (2.15) scale approximately linearly with $R_{\mathrm{DC,AC}}$ and are (in contrast to the modulation imposed emissions) not independent of the source and load impedance. Further, $\hat{u}_{\mathrm{CM,par}}$ remains constant over frequency (as long as $|Z_{6\cdot\mathrm{C,SW}}(f)| >> R_{\mathrm{DC,AC}}$) as both the emission source (i.e., the switched CM voltage) and the impedance of the parasitic capacitance decay linearly with frequency, and $\hat{u}_{\mathrm{CM,par}}$ might become relevant for higher frequencies. Last, note that a DC-link referenced filter for combined DM/CM attenuation is not effective for the parasitically imposed emissions, as the filter inductors are bypassed via the filter capacitors providing a low impedance return path to the DC-link rails (cf., **Fig. 2.10a**). Accordingly, (at least) one filter stage on the DC and on the AC side needs to separately attenuate CM and DM noise, where the CM filter comprises Y2 safety capacitors to PE, such that the impact

Tab. 2.1: Worst Case Emissions and required attenuations.

	$\hat{u}(100\,\text{kHz})\,[\text{dB}\mu\text{V}]$	$\hat{u}(200\,\text{kHz})\,[\text{dB}\mu\text{V}]$	$A_{\text{req}}\,[\text{dB}]$
DC_{DM}	121	109	**39**
DC_{CM}	126	114	**44**
AC_{DM}	136	124	**54**
AC_{CM}	123	111	**41**
par_{CM}	102	102	**38**

of the source and load impedance on the recorded emissions on DC and AC side is again minimized.

In summary, the overall expected emission level (given by the sum of the discussed emission mechanisms) of the DC LISN $\hat{u}_{\text{LISN,dc}}(100\,\text{kHz}) = 128\,\text{dB}\mu\text{V}$ and the AC LISN $\hat{u}_{\text{LISN,ac}}(100\,\text{kHz}) = 138\,\text{dB}\mu\text{V}$ is shown in **Fig. 2.5b** and **Fig. 2.5c**, respectively, again closely matching the simulated peak emissions.

2.3.3 EMI Filter Design

As defined, the goal of the filter design is the compliance with the IEC 61800-3 conducted power interface emission limits for residential applications with long unshielded cables (cf., **Fig. 2.1**). Hence, for a DC-fed VSD the emissions on the DC and on the AC side of the 12-YI have to be attenuated below 80 dBµV (i.e., 10 mV) from 150 kHz to 500 kHz, and below 74 dBµV from 500 kHz to 30 MHz.

With the emission mechanisms and equations for a simplified emission estimation derived and verified by means of a circuit simulation in **Sec. 2.3.2**, the goal of this section is to assess the minimum required filter attenuation to comply with the above summarized power interface emission limits and to find a suitable filter structure.

The required attenuation is defined by the design frequency $f_{\text{D}} = n_{\text{D}} f_{\text{s}}$ [134] given by the first regulated switching frequency harmonic

$$n_{\text{D}} = ceil\left(\frac{150\,\text{kHz}}{f_{\text{s}}}\right). \tag{2.16}$$

Here, the design frequency results to $f_{\text{D}} = 200\,\text{kHz}$ (i.e., the second switching frequency harmonic). The filter design target is to attenuate the DM and CM noise below the emission limit of 80 dBµV considering an additional margin of 10 dB (to account for component tolerances) and 6 dB (to account for the

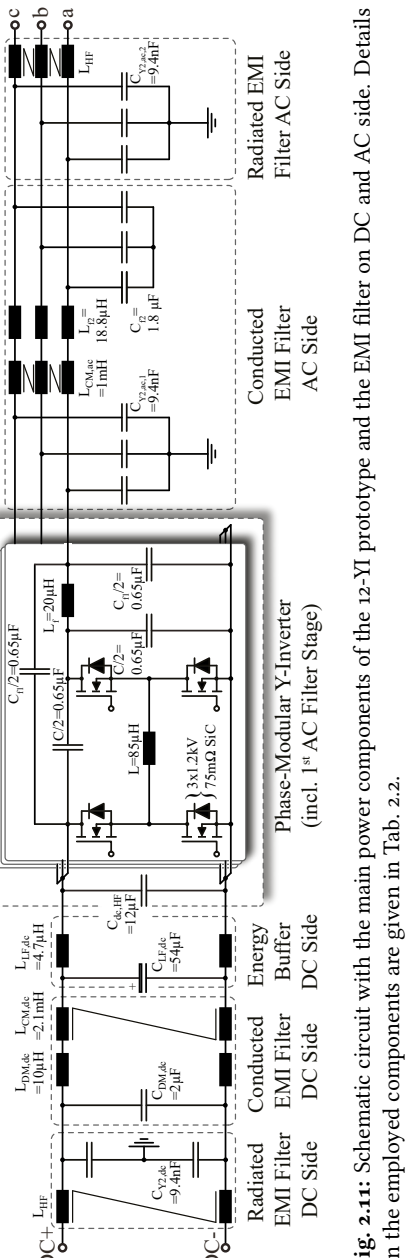

Fig. 2.11: Schematic circuit with the main power components of the 12-YI prototype and the EMI filter on DC and AC side. Details on the employed components are given in Tab. 2.2.

Tab. 2.2: 12-YI VSD Prototype main power components.

Component	Nom. value	Details
Semiconductors	$f_s = 100\,\text{kHz}$	3 x Cree SiC C3M0075120J 75 mΩ 1.2 kV,
AC inductors	$L = 85\,\mu\text{H}$	2 x TDK EELP 43 Ferrite Core (N97), 5.4 mm air gap, 20 turns of 625 x 71 µm litz wire
	$L_{f1} = 20\,\mu\text{H}$	2 x Würth Elektronik WE-HCI 10 µH, 21 A, 3.4 mΩ
	$L_{f2} = 18.8\,\mu\text{H}$	4 x Bourns Inc. SRP1265C-4R7M 4.7 µH, 20 A, 9.5 mΩ
	$L_{CM,ac} = 1\,\text{mH}$	(at 200 kHz) VAC T60006-L2030-W423 (VITROPERM 500 F), 10 turns of 1.4 mm solid wire
DC inductors	$L_{LF,dc} = 4.7\,\mu\text{H}$	1 x Vishay IHLP6767DZER4R7M01 4.7 µH, 27 A, 11.2 mΩ
	$L_{CM,dc} = 2.1\,\text{mH}$	(at 200 kHz) VAC T60006-L2025-W380 (VITROPERM 500 F), 13 turns of 1 mm solid wire
	$L_{DM,dc} = 10\,\mu\text{H}$	1 x Vishay IHLP6767GZER100M01 10 µH, 25 A, 12 mΩ
HF inductors	$L_{HF} = 340\,\text{nH}$	(at 30 MHz) Fair-Rite 1 x 59520208O1, 2 x 5952020601, NiZn (Fair-Rite 52) plug-on core
DC capacitors	$C_{dc,LF} = 48\,\mu\text{F}$	12 x Chemi-Con ALUM 18 µF, 450 V (2 in series)
	$C_{dc,HF} = 12\,\mu\text{F}$	48 x TDK Ceralink 0.25 µF, 900 V
	$C_{DM,dc} = 2\,\mu\text{F}$	8 x TDK Ceralink 0.25 µF, 900 V
AC capacitors	$C = C_{f1} = 1.3\,\mu\text{F}$	6 x Syfer X7R, 0.47 µF, 1 kV referenced evenly to positive and negative DC-link rails (C and C_{f1} represent the min. capacitance values for the considered converter specifications)
	$C_{f2} = 1.8\,\mu\text{F}$	8 x KEMET C0G, 0.22 µF, 500 V
PE capacitors	$C_{Y2} = 9.4\,\text{nF}$	2 x Johanson-Dielectrics Y2 safety certified MLCC, X7R 4.7 nF, 250 V
Controller	-	TMS320C2834X

worst case summation of DM and CM noise) to

$$\hat{u}_{\max}(f_{\mathrm{D}}) = 80\,\mathrm{dB\mu V} - 10\,\mathrm{dB} - 6\,\mathrm{dB} = 64\,\mathrm{dB\mu V}. \tag{2.17}$$

The worst case emission levels on DC and AC side for $f_{\mathrm{s}} = 100\,\mathrm{kHz}$ and $f_{\mathrm{D}} = 200\,\mathrm{kHz}$, as well as the corresponding required filter attenuations A_{req} according to (2.17) are summarized in Tab. 2.1. There, the worst case DC-side DM noise (DC_{DM}) is given for operation with the maximum AC phase current of $I_{\mathrm{ac,max}}$ =16.3 $\mathrm{A_{rms}}$ and unity power factor operation. The remaining modulation imposed worst case emissions on the AC side ($AC_{\mathrm{DM}}, AC_{\mathrm{CM}}$) and on the DC side ($DC_{\mathrm{CM}}$) result for the operating point considered in **Sec. 2.3.2** with maximum boosting effort and nominal output power, while the maximum parasitically imposed emissions (par_{CM}) result for operation with the maximum DC-link voltage $U_{\mathrm{dc}} = U_{\mathrm{dc,max}} = 750\,\mathrm{V}$ (cf., **Fig. 2.2a**).

In the following, a suitable filter structure for DC and AC side of the 12-YI prototype is derived, where the HF attenuation A of an m stage LC-filter can be approximated with [135]

$$A(f) = \frac{1}{(2\pi f)^{2m}} \frac{1}{\prod_{v=1}^{m} C_{\mathrm{f,v}} \prod_{v=1}^{m} L_{\mathrm{f,v}}}, \tag{2.18}$$

where a minimum filter volume results for a realization of the stages with identical component values [136].

AC-Side Filter

Employing ceramic capacitors allows for a highly compact filter realization [137], where the sum of the employed capacitance values located on the AC side of the 12-YI are limited in order to avoid excessive conduction losses due to the capacitive reactive currents. Here, a reactive current limit of 20 % nominal AC output current for operation with 6 kW output power was selected, resulting in

$$\sum C \leq \frac{20\,\% I_{\mathrm{ac,nom}}}{2\pi f_{\mathrm{ac,max}} U_{\mathrm{ac,max}}} \approx 6\,\mu\mathrm{F}. \tag{2.19}$$

To achieve the desired DM attenuation of ≈60 dB (cf., Tab. 2.1) the AC filter is realized as a two-stage LC filter (i.e., with 30 dB attenuation each), where the first stage is DC-link referenced to simultaneously attenuate DM and CM noise (cf., **Fig. 2.11**). There, C_{f1} is realized as the output filter capacitor C of the existing prototype by referencing three 1 kV 0.47 µF X7R capacitors (cf., Tab. 2.2) to the positive and negative DC-link rail, such that the non-linear

capacitance variation over the fundamental period is reduced [138] [104] and a minimum capacitance value of $min(C) = min(C_{f1}) = 1.3\,\mu F$ results. To achieve the desired attenuation of 30 dB per stage $L_{f1} = 20\,\mu H$ is selected according to (2.18). Note that (in contrast to the buck-boost inductor L) the HF losses in subsequent filter inductors are very small, and hence a compact realization with commercial flat-wire inductors is possible.

As discussed in **Sec. 2.3.2**, DM and CM noise are attenuated separately in the second filter stage, where linear 500 V C0G ceramic capacitors are employed for the realization of the DM $C_{f2} = 1.8\,\mu F$, in order to avoid the high capacitance variation and losses resulting when using X7R capacitors in an open star point DM filter [137]. The second filter stage DM inductance is also set to $L_{f2} = 18.8\,\mu H$, where a different commercial inductor is selected to achieve a good form factor (cf., Tab. 2.2).

The second stage CM filter consists of a CM choke and Y2 safety capacitors to PE, where the latter are subject to a ground current limit given by the usage of Residual-Current Devices (RCDs): As the 12-YI prototype employs DPWM, the low-frequency AC terminal CM voltage u_{CM} (cf., **Fig. 2.3b**) is time varying and contains frequency components at multiples of the triple fundamental frequency $3 \cdot f_{ac}$. Neglecting the impedance of the inductive components, u_{CM} is applied to the series connection of the PE capacitances of DC and AC side (cf., **Fig. 2.10a**), causing a low-frequency PE current I_{PE}. Assuming as a worst case a very large PE capacitance of the DC-bus, I_{PE} is only limited by the total AC-side PE capacitance $\sum C_{PE}$, and the (RMS) PE current results equal to

$$\begin{aligned} I_{PE} &= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \left(\frac{\mathrm{d}\, u_{CM}(t)}{\mathrm{d}\, t} \sum C_{PE}\right)^2 \mathrm{d}\, t} \\ &= \sqrt{\frac{1}{2} - \frac{3\sqrt{3}}{8\pi}}\; 2\pi f_{ac} \hat{U}_{ac} \sum C_{PE}\ . \end{aligned} \tag{2.20}$$

The goal is to design the CM filter such that I_{PE} <15 mA_{rms} (i.e., 50 % of a 30 mA_{rms} RCD) for the maximum AC frequency $f_{ac} = f_{ac,max} = 200\,Hz$ and voltage $\hat{U}_{ac} = \hat{U}_{ac,max}$ =325 V_{pk}. Note, that motor and motor cable also contribute to $\sum C_{PE}$, where here a motor PE capacitance up to 10 nF [83], and a motor cable PE capacitance up to 15 nF (corresponding to an unshielded cable with 150 pF/m of 100 m length) is considered for the filter design, and hence according to (2.20) up to 60 nF PE capacitance (i.e., 20 nF per phase module) can be employed.

It is important to mention that the 12-YI prototype employing DPWM may not be attached simultaneously to a LISN on DC and AC side (as illustrated in **Fig. 2.5a**) during the emission evaluation in **Sec. 2.5.1**: A LISN comprises a total PE capacitance in the range of 10 µF (due to the line-side filter), which also contributes to $\sum C_{\mathrm{PE}}$ and causing according to (2.20) massive PE currents > 1 A, leading hence to saturation of the employed CM chokes. Accordingly, in a practical setup the AC LISN is only connected when measuring the AC-side emissions, and the DC LISN only when measuring the DC-side emissions.

This maximum PE capacitance of 20 nF is equally distributed on both sides of the AC-side CM choke $L_{\mathrm{CM,ac}}$ (cf., **Fig. 2.11**): $C_{\mathrm{Y2,ac,1}} = 10\,\mathrm{nF}$ is located in front of the CM choke $L_{\mathrm{CM,ac}}$ to provide a low impedance return path to the DC-link rails for parasitically imposed emissions (cf., **Fig. 2.10a**), and $C_{\mathrm{Y2,ac,2}} = 10\,\mathrm{nF}$ is located after the CM choke $L_{\mathrm{CM,ac}}$ to form an LC filter for modulation imposed CM emissions, where $C_{\mathrm{Y2,ac,2}}$ is also part of the radiated emissions filter discussed in **Sec. 2.4.2**. Note that the low impedance return path for parasitically imposed emissions is typically formed by connecting PE capacitors to the DC-link rails, which were in case of the considered converter prototype not directly accessible due to the integrated DC energy buffer (cf., **Fig. 2.11**). The required filter attenuation of 38 dB (cf., Tab. 2.1) for parasitically imposed CM emissions is achieved according to (2.18) by employing a CM choke with $L_{\mathrm{CM,ac}} = 1\,\mathrm{mH}$, which is realized with a high permeability nanocrystalline magnetic core (cf., Tab. 2.2, note that the core shows a frequency dependent permeability, where $L_{\mathrm{CM,ac}} = 1\,\mathrm{mH}$ results for the design frequency $f_{\mathrm{D}} = 200\,\mathrm{kHz}$).

DC-Side Filter

As mentioned, the converter prototype comprises an electrolytic capacitor energy buffer $C_{\mathrm{LF,dc}} = 54\,\mu\mathrm{F}$ to stabilize the DC-link voltage in case of variations of the current supplied by an upstream converter, where two small inductors $L_{\mathrm{LF,dc}} = 5\,\mu\mathrm{H}$ limit the switching frequency currents in $C_{\mathrm{LF,dc}}$ to avoid excessive capacitor losses (cf., **Fig. 2.11**). Note that according to (2.18), the DM filter formed by $C_{\mathrm{LF,dc}}$ and $2 \cdot L_{\mathrm{LF,dc}}$ provides an attenuation of close to 60 dB, exceeding the DC-side DM filter demand according to Tab. 2.1. However, due to the high series resistance and low self-resonance frequency of electrolytic capacitors, the attenuation provided by the DC energy buffer is not considered in the filter design, and an additional filter stage is added with $2 \cdot L_{\mathrm{DM,dc}} = 10\,\mu\mathrm{H}$ and $C_{\mathrm{DM,dc}} = 2\,\mu\mathrm{F}$, where $C_{\mathrm{DM,dc}}$ is realized with the same CeraLink ceramic capacitors employed in $C_{\mathrm{dc,HF}}$ such that a high self-resonance frequency results. As found in **Sec. 2.5.1**, the electrolytic capacitors

employed in $C_{\mathrm{LF,dc}}$ still provide some attenuation above 150 kHz yielding a very low emission level at the design frequency $f_{\mathrm{D}} = 200\,\mathrm{kHz}$ with a margin above 20 dB, and the HF DC DM filter could eventually employ lower component values.

Finally, the DC-side CM filter consists of a CM choke $L_{\mathrm{CM,dc}} = 2.1\,\mathrm{mH}$ (consisting of a high permeability nanocrystalline magnetic core, cf., Tab. 2.2) forming a second order *CL* filter for parasitically imposed emissions with $C_{\mathrm{Y2,ac,1}}$ and providing a series attenuation with the DC LISN for modulation imposed emissions.

2.4 Radiated EMI Analysis and Filter Design

In contrast to the conducted emission limits applying to each power interface individually, the radiated emission limits concern the overall converter system and have to be complied with for the complete VSD independently of the power interface realization, where employing shielded cables reduces radiated emissions [93]. Again, the measurement method for the experimental verification is discussed in **Sec. 2.4.1** and subsequently the required attenuation and realization of the radiated EMI filter is derived in **Sec. 2.4.2**.

2.4.1 Measurement Method

The test setup for the radiated EMI emission measurement according to IEC 61800-3 is illustrated in **Fig. 2.12a**, where an electromagnetically quiet environment (i.e., an Open-Area Test Site (OATS) or a Semi-Anechoic Chamber (SAC)) is required. The Equipment Under Test (EUT) is located on a wooden table and the cables are HF terminated with a Common Mode Absorption Device (CMAD), such that a reproducible setup with an effective cable length of approximately 1.5 m results and the radiated emissions are then measured with an antenna in 3 m distance.

Since measurements in complying test sites (i.e., OATS or SAC) are time consuming and expensive, a popular pre-compliance method bases on the measurement of the cable HF CM currents (recorded with a clamp-on current probe, cf., **Fig. 2.12a**), which is less susceptible to background EMI noise. It was shown in [140] [141] that radiated emissions due to CM currents can greatly exceed those caused by DM currents, and in [139] the CM currents $i_{\mathrm{CM,rad}}$ **not** returning in the cable are identified as the dominant source of radiation, hence allowing to quantify the radiated emissions based upon a measurement of the conducted CM current $i_{\mathrm{CM,rad}}$ (cf., **Fig. 2.13**). For a given

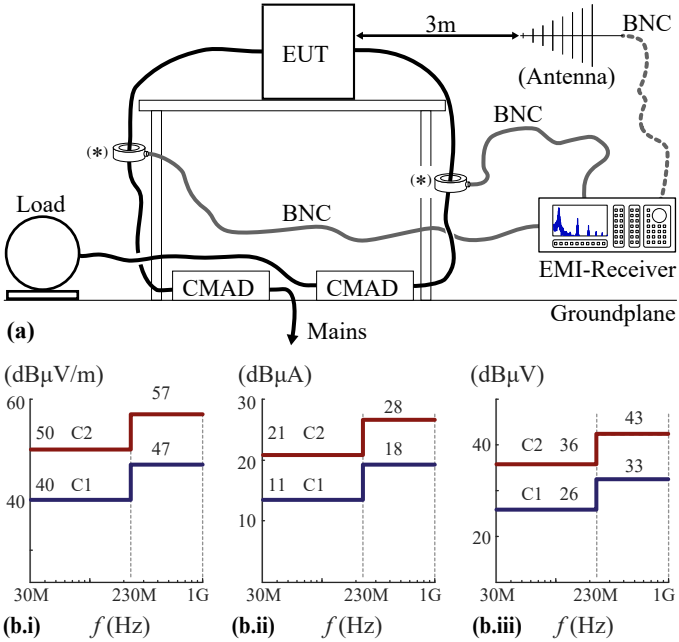

Fig. 2.12: (a) Illustration of the measurement setup for radiated emissions according to IEC 61800-3 [84], where all cables connected to the Equipment Under Test (EUT) are individually HF terminated with a Common Mode Absorption Device (CMAD) and the emission level is sensed with an antenna.
(*) Alternatively, the radiated emissions can be calculated based on a measurement with a high-bandwidth current probe (e.g., F-33-1) [139]. **(b.i)** IEC 61800-3 E-field limits for a measurement distance of 3 m, translated into a **(b.ii)** CM current and **(b.iii)** test receiver voltage reading limit for a current probe with 6.3 Ω transfer impedance.

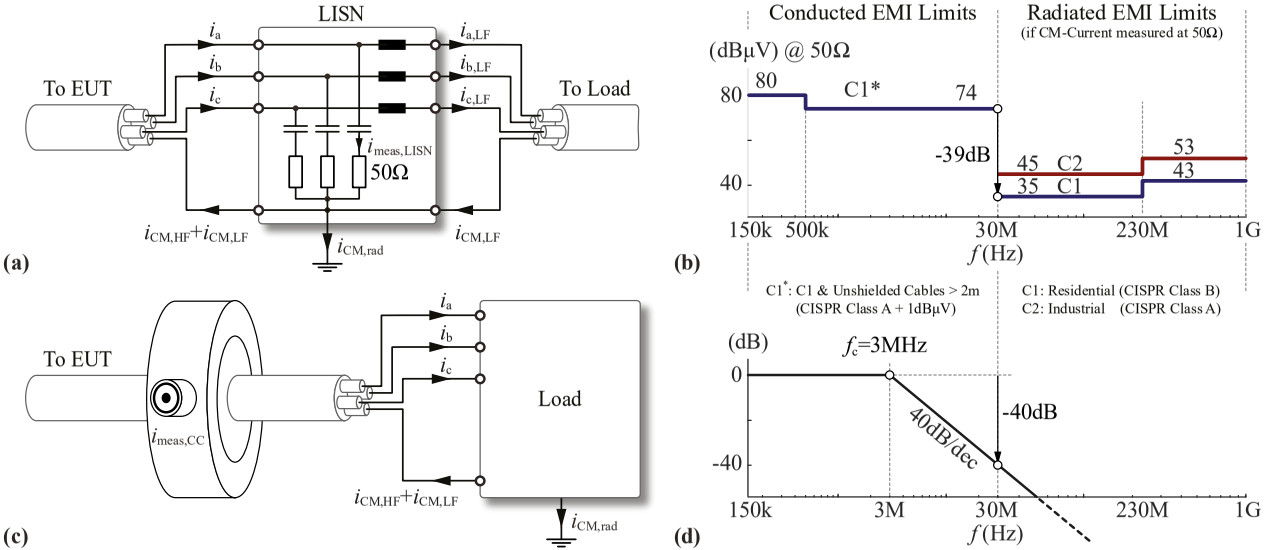

Fig. 2.13: CM-current measurement with **(a)** a LISN (where the phase currents i_a,i_b,i_c are separated into low-frequency $i_{a,LF}$,$i_{b,LF}$,$i_{c,LF}$ and HF $i_{a,HF}$,$i_{b,HF}$,$i_{c,HF}$ currents) and **(c)** a current clamp (where only the CM current $i_{CM,rad}$ **not** returning through the cable is measured). Translating the current limits for radiated emissions from **Fig. 2.12(b.ii)** to a voltage measurement at 50 Ω, the voltage limits above 30 MHz shown in **(b)** result. **(d)** Illustration of the radiated EMI filter design process to compensate for the more stringent CM current limit above 30 MHz according to **(b)**.

frequency f (and hence wavelength $\lambda = c_0/f$, where c_0 is the speed of light in free space) and cable length l_{cable}, the electric field E in function of the CM current $i_{\text{CM,rad}}$ and measured at a distance r can be described as [139]

$$E = \begin{cases} \frac{\mu_0 \cdot f \cdot l_{\text{cable}} \cdot i_{\text{CM,rad}}}{r}, & \frac{\lambda}{4} \leq l_{\text{cable}} \\ \frac{\mu_0 \cdot \frac{c_0}{4} \cdot i_{\text{CM,rad}}}{r}, & \frac{\lambda}{4} > l_{\text{cable}}. \end{cases} \tag{2.21}$$

Accordingly, the IEC 61800-3 E-field limits displayed in **Fig. 2.12b.i**. can be translated with (2.21) into corresponding CM currents **Fig. 2.12b.ii**, yielding a maximum value of 11 dBµA (i.e., 3.5 µA) for residential applications (C1).

Ref. [139] recommends the **Fischer FCC F-33-1** clamp-on current probe with a frequency range up to 250 MHz, which is also employed here for the radiated EMI evaluation. The maximum reading of an EMI test receiver when measuring the CM currents with the **FCC F-33-1** showing a transfer impedance of approximately 6.3 Ω is given in **Fig. 2.12b.iii**, where an emission level up to 26 dBµV (i.e., 20 µV) can be tolerated.

This method was also employed within the field of VSDs in [142], where a successful verification measurement with an antenna in a SAC was conducted. Accordingly, the subsequent filter design process in **Sec. 2.4.2** as well as the experimental verification of the radiated emission level in **Sec. 2.5** bases on the measurement of the CM current $i_{\text{CM,rad}}$.

2.4.2 Radiated EMI Filter Design

According to the IEC 61800-3, the resulting E-field for residential applications has to be attenuated below 40 dBµV/m from 30 MHz to 230 MHz, and 47 dBµV/m from 230 MHz to 1 GHz. Generally, it is hard to assess the filtering demand for radiated emissions, as the main power components experience self-resonance below 30 MHz [143], while the dominant conducted emission mechanisms (cf., **Sec. 2.3.2** greatly decay up to 30 MHz and less deterministic emission phenomena become relevant.

The radiated EMI filter design approach presented here bases on the fact that at the boundary of conducted and radiated EMI emission limits (i.e., at 30 MHz) the emissions are measured with the LISN and the current clamp. **Fig. 2.13a** illustrates the measurement with a LISN (the phase currents i_{a},i_{b},i_{c} are separated into low-frequency $i_{\text{a,LF}}$,$i_{\text{b,LF}}$,$i_{\text{c,LF}}$ and HF currents $i_{\text{a,HF}}$,$i_{\text{b,HF}}$,$i_{\text{c,HF}}$), where the measured HF CM current $i_{\text{meas,LISN}}$ evaluates to

$$\begin{aligned} i_{\text{meas,LISN}} &= (i_{\text{a,HF}} + i_{\text{b,HF}} + i_{\text{c,HF}})/3 \\ &= (i_{\text{CM,rad}} + i_{\text{CM,HF}})/3 \end{aligned} \tag{2.22}$$

and contains both the CM current returning through the cable $i_{\mathrm{CM,HF}}$ as well as $i_{\mathrm{CM,rad}}$. In contrast, **Fig. 2.13c** highlights the measurement with the high-bandwidth current clamp, where the measured HF CM current $i_{\mathrm{meas,CC}}$ is given by

$$\begin{aligned} i_{\mathrm{meas,CC}} &= (i_{\mathrm{a,HF}} + i_{\mathrm{b,HF}} + i_{\mathrm{c,HF}}) - i_{\mathrm{CM,HF}} \\ &= i_{\mathrm{CM,rad}} \quad . \end{aligned} \tag{2.23}$$

Assuming $i_{\mathrm{CM,HF}}$ and $i_{\mathrm{CM,rad}}$ to be in phase, $i_{\mathrm{CM,rad}} \leq 3 \cdot i_{\mathrm{meas,LISN}}$ holds. Considering now conservatively that $i_{\mathrm{meas,LISN}} = i_{\mathrm{CM,rad}}/3$ (i.e., $i_{\mathrm{CM,HF}} = 0\,\mathrm{A}$ and no CM current returning through the cable), the CM current limit of 11 dBµA corresponding to the C1 radiated emission limits displayed in **Fig. 2.12b** translates to 35 dBµV measured at one of the 50 Ω LISN resistors and hence a step of −39 dB compared to the C1 conducted emission limits results at 30 MHz in **Fig. 2.13b**.

Assuming conducted CM emissions equal to the limit value of 74 dBµV at 30 MHz without any dedicated radiated EMI filter measures, an additional second-order filter (i.e., showing a HF attenuation of −40 dB/dec according to (2.18)) with corner frequency $f_{\mathrm{c}} = 3\,\mathrm{MHz}$ as illustrated in **Fig. 2.13d** is required to comply at 30 MHz with the 39 dB lower C1 radiated emission limits.

As mentioned, the radiated emission limits apply above typical self-resonance frequencies of power filter components. Accordingly, dedicated HF filtering components need to be employed, where a proper HF layout of the radiated emission filter is crucial. The selected filter topology is a *CL* filter, where the safety capacitors of the conducted EMI filter $3 \cdot C_{\mathrm{Y2,ac,2}} = 30\,\mathrm{nF}$ (cf., **Sec. 2.3.3**,**Fig. 2.11**) with a low impedance connection to the PE plane in the converter are part of the radiated EMI filter. To avoid capacitive coupling between the CM choke windings, (single-turn) NiZn-Ferrite plug-on cores (Fair-rite 52 material) with a HF attenuation up to 1 GHz are employed. The CM choke consists of one 35 mm core with $AL = 283\,\mathrm{nH}$ and two stacked 21 mm cores with $AL = 151\,\mathrm{nH}$ each, yielding a total inductance of 585 nH (decays to 340 nH at 30 MHz) for the single-turn plug-on choke realization (cf., Tab. 2.2), providing hence the desired filter attenuation at 30 MHz with a margin of 10 dB.

An identical filter realization is employed for the DC side and the AC side of the 12-YI prototype and finally, in **Fig. 2.11**, the schematic circuit and component values of the 12-YI prototype with the conducted and radiated EMI filter stages is shown.

2.5 Experimental EMI Measurements

The 11 kW 12-YI prototype including the first AC output filter stage is shown in **Fig. 2.14a**, where a volume of 740 cm^3 corresponds to a power density of 15 kW/dm^3 (246 W/in^3).

The 12-YI with the designed filter boards attached on the DC and the AC side according to **Fig. 2.11** and ensuring compliance with the IEC 61800-3 C1 conducted and radiated emission limits for operation with long unshielded cables is depicted in **Fig. 2.14b**, where an overall system power density of 12 kW/dm^3 (197 W/in^3) results (DC and AC filter board contribute each a volume of 74 cm^3, hence increasing the total volume by 20 %).

To avoid noise coupling from the converter directly to the cables (i.e., bypassing the converter filters), and to create a reproducible measurement setup, the 12-YI prototype is placed in a metallic EMI enclosure emulating a housing as shown in **Fig. 2.14c**. Note that the enclosure was designed as a general test environment for converters, and for an industrial product a case closely fitting the converter would be preferable to maximize the system power density. Unshielded cables leave the case on both the DC side (three conductor cable for DC^+,DC^- and PE) and the AC side (four conductor cable for *a*,*b*,*c* and PE), whereas the cables inside the housing are shielded to avoid near-field coupling [144]. The casing cooling recesses show a diameter $d = 10\,\text{mm} < \lambda/20$ at 1 GHz such that EMI noise is confined [139].

2.5.1 Conducted EMI Measurements

In the following, emission results recorded for several operating points with the maximum boosting effort (i.e., $U_{dc} = U_{dc,min} = 400\,V$, cf., **Fig. 2.2a**) are presented in order to verify the 12-YI HF emission mechanisms derived in **Sec. 2.3.2** as well as the selected filter structure from **Sec. 2.3.3**. For this reason, the switching frequency emissions at 100 kHz (located below the IEC 61800-3 regulated band for conducted emissions starting at 150 kHz) are also shown, where emissions above the limit value of 80 dBµV result, and a 20 dB attenuator was employed on the input of the test receiver to avoid overloading the intermediate frequency amplifier (cf., [130]).

All EMI measurements are recorded using the R&S ESPI-3 test receiver, where the peak detector (9 kHz receiver bandwidth, 10 ms measurement time and 4 kHz steps) is employed to reduce the measurement time. Note that the IEC 61800-3 limit values depicted in **Fig. 2.1** refer to a measurement with the slow quasi-peak detector, which generally yields readings lower or equal to the peak detector. Hence employing the peak detector is conservative, and also

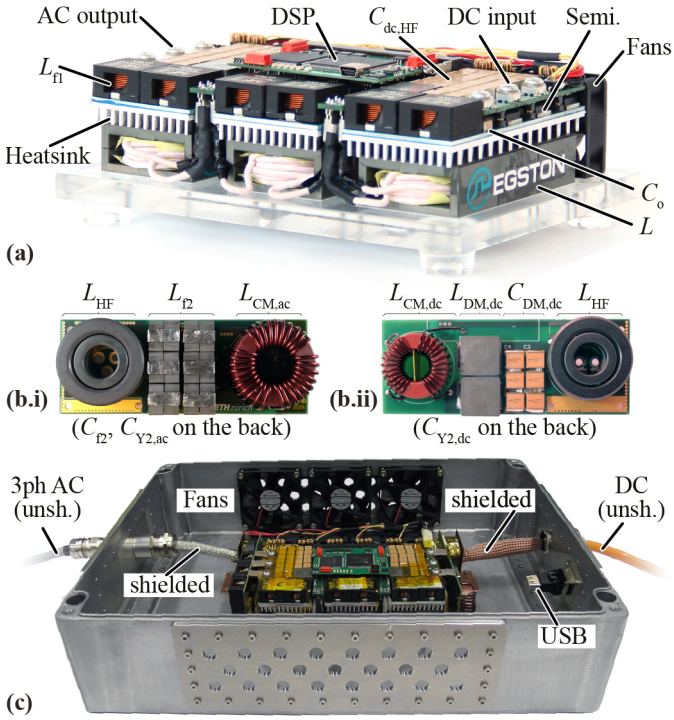

Fig. 2.14: **(a)** 12-YI hardware prototype including the first AC filter stage (160x110x42mm^3 = 6.3x4.3x1.7in^3, ρ = 15 kW/dm^3 = 246 W/in^3) and the additional filter boards for **(b.i)** AC side and **(b.ii)** DC side (110x42x16mm^3 = 4.3x1.7x0.6in^3). Component designators refer to **Fig. 2.11** and **Tab. 2.2**. **(c)** Prototype with the mounted filter boards (ρ = 12 kW/dm^3 = 197 W/in^3) placed in a shielded EMI enclosure to emulate a converter housing. Note that the motor and DC cable inside the enclosure are shielded to avoid coupling of noise from the converter, while the cables leaving the EMI enclosure are unshielded.

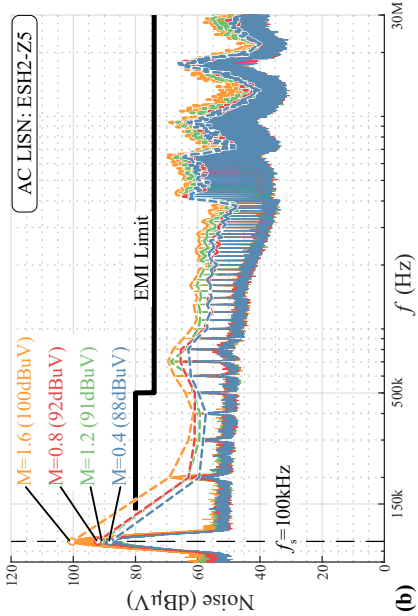

Fig. 2.15: Conducted EMI noise measurement results employing a LISN at **(a)** the DC input side and **(b)** the AC output side of the 12-YI compared against the IEC 61800-3 C1 power interface limits. The converter is operated with DPWM, an input voltage of U_{dc} = 400 V and a constant resistive three-phase load with R = 26 Ω. Several modulation depth values M are employed, where M = 1.6 corresponds to U_{ac} =230 V_{rms} and the nominal power of 6 kW. The thin lines represent the spectrum obtained by the EMI receiver (peak detector, 9 kHz receiver bandwidth, 10 ms measurement time and 4 kHz steps), while the thick dashed lines connecting the respective emission peak values have no regulatory implications but serve to distinguish between the different measurement points more clearly.

indicates compliance for quasi-peak detector measurements. In a first step, the converter is tested extensively with a resistive three-phase load in **Sec. 2.5.1**, where the emissions are recorded using a LISN on the DC input and AC output side for various operating points. There, the impact of output power, modulation index and modulation strategy is assessed. Subsequently, in **Sec. 2.5.1** the converter emissions are evaluated while powering a three-phase induction machine, where a close matching with the results obtained with a LISN is reported. The measured AC emissions presented in the following are recorded for phase *a*, where the remaining two phases show similar emission levels.

Measurements with LISN

A LISN is attached to the converter on the DC side (R&S NNLK8122, single-phase, up to 1 kV) or the AC side (R&S ESH2-Z5, three-phase, up to 250 V_{rms}). As discussed in **Sec. 2.3.1**, when using a LISN on the AC side, the employed load is decoupled from the converter for high frequencies > 150 kHz and hence has negligible impact on the recorded emissions. Accordingly, for the following experiments a resistive three-phase load is employed, greatly simplifying the measurement process.

In **Fig. 2.15**, the impact of the modulation index M on the 12-YI DC-side and AC-side emissions is investigated and compared against the IEC 61800-3 C1 power interface limits. The converter is operated with DPWM, an input voltage of $U_{dc} = 400$ V and a constant resistive three-phase load with $R = 26\,\Omega$. Increasing modulation depth values M (with increasing output power) are employed starting from $M = 0.4$, where $M = 1.6$ corresponds to U_{ac} =230 V_{rms} and the nominal output power of 6 kW. The thin lines in **Fig. 2.15** represent the spectrum obtained by the EMI receiver peak detector, while the thick dashed lines connecting the respective emission peak values (occurring at multiples of the switching frequency) have no regulatory implications but serve to distinguish between the different measurement points more clearly.

As can be noted in **Fig. 2.15a**, the DC-side emissions at the switching frequency increase with increasing modulation index and output power from 81 dBµV at $M = 0.4$ ($P = 0.2$ kW) to 85 dBµV at $M = 0.8$ (P =1.0 kW), which is in accordance with the discussed DC-side EMI emission mechanism in 2.3.2, where the DM emissions scale with the switched phase currents. Accordingly, the DC-side emissions drop to 79 dBµV at $M = 1.2$ ($P = 2.2$ kW), when the phase modules partially are operating in boost operation, and a continuous current is drawn from the DC-link by the boosting module. Then, at $M = 1.6$ ($P = 6$ kW) the emissions increase again with the elevated phase currents and

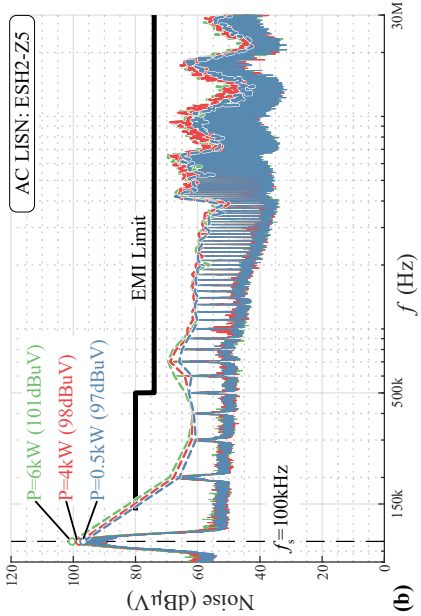

Fig. 2.16: Conducted EMI noise measurement results employing a LISN at **(a)** the DC input side and **(b)** the AC output side of the 12-YI. The converter is operated with DPWM, an input voltage of U_{dc} = 400 V and a constant modulation depth M = 1.6 (U_{ac} =230 V_{rms}), while the resistive three-phase load is gradually decreased down to R = 26 Ω (corresponding to the nominal power of 6 kW).

reach the maximum value of 90 dBµV. It can be noted that for all considered operating points, the second switching frequency harmonic component at $f_D = 2 \cdot f_s = 200$ kHz is clearly below the limit value of 80 dBµV by a margin of more than 20 dB, while the emissions slightly increase again at 300 kHz. This is contradictory to the simulated noise shown in **Fig. 2.5b** which is continuously decreasing with frequency. Both the high margin to the limit value at $f_D = 200$ kHz as well as the noise increase at 300 kHz shown in **Fig. 2.15a** can be explained by the fact that the employed electrolytic capacitors $C_{dc,LF}$ are conservatively considered ineffective at $f_D = 200$ kHz in the filter design process in **Sec. 2.3.3**, which is a too conservative assumption. Then, at 300 kHz the attenuation provided by $C_{dc,LF}$ is reduced (the self-resonance frequency is exceeded), resulting in elevated emissions compared to 200 kHz. Also, although the emissions do not continuously drop with increasing frequency, as in the case of an ideal filter realization without self-resonance of components, the recorded values remain below the respective limit in the complete conducted EMI band up to 30 MHz.

A similar trend can be observed for the AC side in **Fig. 2.15b**, where the switching frequency EMI emissions increase from 88 dBµV at $M = 0.4$, to 92 dBµV at $M = 0.8$, which corresponds to the emission behaviour of a voltage-source inverter with maximum emissions occurring, with $d_{Bu} = 0.5$. When approaching boost operation, the emissions remain constant or even slightly decay and 91 dBµV result at $M = 1.2$ (the employed DPWM operation further reduces the maximum output voltage with respect to the negative DC-link rail $u_{an,max}$ by approximately 15 %, such that a mild boosting effort results for $M = 1.2$). With increasing boosting effort (and output power), the *power dependent* current-source type emissions become the dominant emission mechanism, where up to 100 dBµV result (i.e., an increase of 9 dB or a factor of 3) at the operating point with $M = 1.6$ and nominal power of $P = 6$ kW. As for the DC side, the AC-side results are consistent with the emission model derived in **Sec. 2.3.2**, where the recorded spectrum remains despite the non-ideal filter realization (i.e., employing filter components with self-resonance above a certain frequency) constantly below the relevant limits. Note that the dashed line for $M = 1.6$ crossing the emission limit line between 100 kHz and 200 kHz does not indicate exceeding the emission limits, as this line solely interconnects related emissions peaks for illustration purposes. In fact the emissions at $f_D = 200$ kHz comply with the emission limits with the desired margin of 10 dB.

It is worth mentioning that when operating the converter with sinusoidal PWM instead of DPWM, the boosting effort and, accordingly, also the low-

frequency inductor current $\langle i_L \rangle$ is increased and for the operating point with $M = 1.6$ shown in **Fig. 2.15b** 100 kHz AC-side emissions elevated by 10 dB were recorded.

To isolate the impact of the converter output power on the emissions, **Fig. 2.16** shows emission measurements for a constant modulation depth $M = 1.6$ (corresponding to U_{ac} =230 V_{rms} with $U_{dc} = 400$ V) and a varying resistive AC load. There, a continuous increase in emissions with output power can be observed for the DC side and the AC side. Note that for low power, the power independent voltage source emission mechanism dominates the switching-frequency noise, while the emissions increase by approximately a factor of 1.5 (3.5 dB) when increasing the output power from 4 kW to 6 kW.

Measurements with Motor

With the filter design and EMI equivalent circuit verified using LISNs and a resistive load, the question remains, whether the 12-YI prototype also complies with the emission limits when driving a motor. Accordingly, the converter emissions were measured while driving an induction machine (Bartholdi HAC-145 S 08, 330 V_{rms} (line-to-line), 2 kW, 2880 rpm nominal speed) in no-load condition through an unshielded cable of 5 m length (the motor was not directly grounded, but attached to PE through the cable). The 12-YI is again operated with DPWM and an input voltage of $U_{dc} = 400$ V. Open-loop V/f control is employed, where the nominal motor voltage U_{ac} =191 V_{rms} (line-to-neutral, i.e., $M = 1.35$) corresponds to a stator frequency of 50 Hz. The emissions are measured using a LISN on the DC side, and the Schwarzbeck TK9421 high-impedance voltage probe (attached to the motor terminal a) on the AC side.

The resulting EMI emissions for increasing stator frequency (and motor speed as well as AC voltage) can be observed for the DC side and the AC side in **Fig. 2.17a** and **b**, respectively. The resulting motor phase current for a very low stator frequency $f_{ac} = 5$ Hz is I_{ac} =1.8 A_{rms} (apparent output power $S = 0.1$ kW), then increases and remains constant at I_{ac} =3.0 A_{rms} for $f_{ac} = 25$ Hz ($S = 0.9$ kW) and $f_{ac} = 50$ Hz ($S = 1.7$ kW). Again, the DC-side emissions at the switching frequency depicted in **Fig. 2.17a** increase in buck operation with the increasing phase current from 72 dBµV at $f_{ac} = 5$ Hz, to 81 dBµV at $f_{ac} = 25$ Hz, and then slightly drop to 79 dBµV when reaching boost operation at $f_{ac} = 50$ Hz with $M = 1.35$. Note that the switching-frequency component in **Fig. 2.17a** is reduced compared to the values shown in **Fig. 2.15a**, which is due to the reduced phase currents dominating the EMI emissions around 100 kHz. However, the emissions above 200 kHz are only

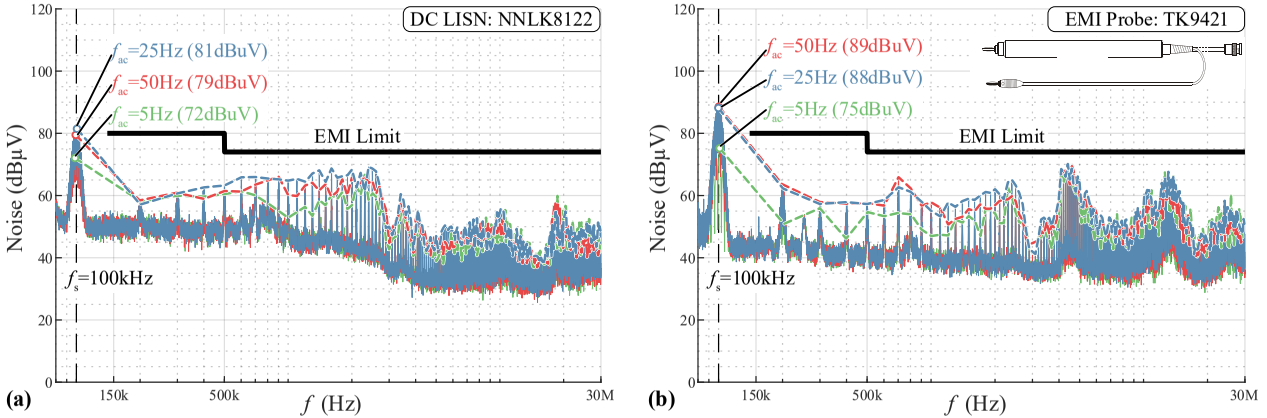

Fig. 2.17: Conducted EMI noise measurement results at **(a)** the DC input side and **(b)** the AC output side of the 12-YI driving an induction machine (Bartholdi HAC-145 S 08, 330 V_{rms} (line-to-line), 2 kW, 2880 rpm nominal speed) in no-load condition. The emissions are measured using a LISN on the DC side, and the Schwarzbeck TK9421 high-impedance voltage probe on the AC side. The converter is operated with DPWM and an input voltage of U_{dc} = 400 V.

mildly power dependent and the DC-side emissions obtained when driving a motor greatly resemble those obtained for a resistive AC load in **Fig. 2.15a**.

The AC-side emissions recorded with the Schwarzbeck TK9421 high-impedance voltage probe are shown in **Fig. 2.17b**, where $f_{ac} = 5\,\text{Hz}$ (i.e., $M = 0.14$) and $f_{ac} = 25\,\text{Hz}$ (i.e., $M = 0.68$) correspond to buck operation and hence voltage-source emission mechanism, where the emissions increase up to a buck duty cycle of $d_{Bu} = 0.5$ and are approximately independent of the output power. Hence the switching-frequency emissions for $f_{ac} = 25\,\text{Hz}$ and $M = 0.68$ of 88 dBµV are close to the emission peaks obtained for operation with a LISN and resistive load depicted in **Fig. 2.15b** with $M = 0.4$ and $M = 0.8$. Due to the low apparent power and phase current, the EMI emissions only increase marginally to 89 dBµV when further increasing the stator frequency to $f_{ac} = 50\,\text{Hz}$ with $M = 1.35$ (i.e., with nominal motor voltage of U_{ac} =191 V_{rms}).

Similar to the DC side, the AC-side switching-frequency noise for operation with a motor shown in **Fig. 2.17b** is reduced compared to **Fig. 2.15b** due to the reduced phase currents and the lower maximum boosting effort (limited by the motor voltage rating), while the emissions above 200 kHz match with good accuracy, hence supporting the selected filter verification process where first in-detail pre-compliance testing is conducted with a LISN and a resistive AC load.

Industrial drives typically contain a user interface / display where speed and/or torque reference can be set. In case of the 12-YI prototype driving the induction motor, the stator frequency reference of the DSP controller was set via communication through a USB cable, where the measurements presented in **Fig. 2.17** were obtained using an optical USB cable. It is important to mention that in the MHz range, auxiliary or communication cables leaving the converter housing may become the predominant source of EMI noise: In case of employing a standard USB cable instead of a fiber-optic USB cable for the operating point with a stator frequency of $f_{ac} = 50\,\text{Hz}$ depicted in **Fig. 2.17a**, DC-side emissions elevated by up to 20 dB could be observed above 10 MHz.

2.5.2 Radiated EMI Measurements

As discussed in **Sec. 2.4.1**, the radiated emissions of the converter prototype are assessed using the **Fischer FCC F-33-1** clamp-on current probe with a frequency range up to 250 MHz, where the ESPI test receiver employs a

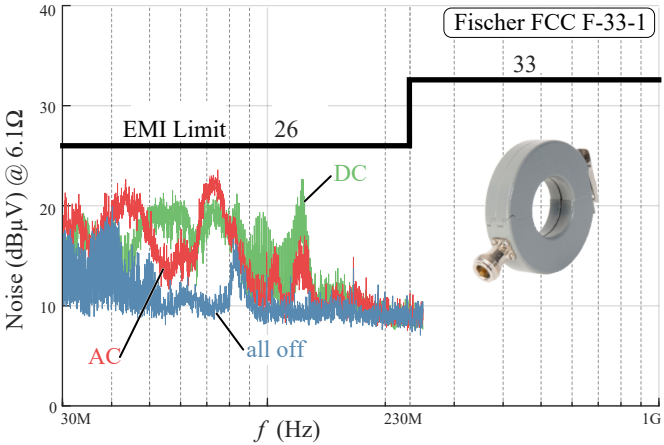

Fig. 2.18: Pre-compliance measurement to assess the radiated EMI emissions: The **Fischer FCC F-33-1** clamp-on current probe with a frequency range up to 250 MHz is employed to measure CM currents not returning through the DC supply or AC motor cable and the limit values corresponding to the IEC 61800-3 C1 radiated emission limits are derived as discussed in **Sec. 2.4.1** (cf., **Fig. 2.12**). Measured currents $i_{\mathrm{CM,rad}}$ (reading in dBµV) are shown for the AC interface when the converter prototype and the DC supply are turned off, as well as for both DC and AC interface at the nominal operating point ($U_{\mathrm{dc}} = 400\,\mathrm{V}$, $U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$, $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$, $P = 6\,\mathrm{kW}$).

receiver bandwith of 120 kHz, and the limit values presented in **Fig. 2.12b.iii** corresponding to the IEC 61800-3 C1 radiated emissions limits are considered.

The test setup is according to **Fig. 2.12a** with CMADs HF terminating the unshielded DC supply and AC motor cable on the floor, such that the measurement can be considered independent of the AC load and the DC source. Accordingly, the experiment is again conducted with a 26 Ω resistive three-phase load.

The resulting HF noise above 30 MHz is shown in **Fig. 2.18**, where a first measurement was conducted on the AC side with the prototype itself and the DC supply turned off. There a substantial noise floor with readings up to 16 dBµV (i.e., only a margin of 10 dB remains to the emission limit value!) results as the unshielded cables act as antenna and pick up e.g., radio broadcast signals.

Operating the converter again with $U_{\mathrm{dc}} = 400\,\mathrm{V}$, $M = 1.6$ ($U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$) and 6 kW output power, the resulting CM currents not returning through

the cables on the unshielded DC and AC interface are measured, where values up to 23 dBµV are recorded. Hence the measurement results imply compliance with the calculated C1 radiated emission limits up to 250 MHz. According to [139], most CM cable radiation occurs below 250 MHz, where above 230 MHz the C1 radiated emission limits are further relaxed by 7 dB. Also, the recorded emissions (up to 23 dBµV) do not peak at the boundary of the current probe frequency range, but decay towards the noise floor when approaching 250 MHz. In summary, the measurement results can be considered as a strong indication towards full compliance with the IEC 61800-3 C1 radiated EMI limits, where only a measurement with an antenna in a certified test site could finally prove full conformity.

We would like to highlight, that at 250 MHz the wavelength is approximately 1.2 m, such that even short cables become efficient antennas [139]. Accordingly, a short disconnected cable for an external auxiliary supply leaving the converter housing caused the recorded emissions to exceed the limit values in an initial measurement.

2.6 Conclusions

Employing unshielded cables in VSD applications allows a more flexible, lightweight and cheaper system realization compared to shielded cables, where the IEC 61800-3 dictates stringent conducted and radiated EMI emission limits on unshielded power interfaces.

Research described in literature so far investigated the impact of several filter structures on the EMI emissions of a VSD, but no comprehensive filter design guidelines including conducted and radiated EMI emissions for operation with unshielded cables are available in publications. In this chapter, we provided an overview on suitable measurement techniques for power interface EMI emissions of DC-fed VSDs, and a complying filter structure for conducted and radiated emissions was derived for an existing 11 kW Twelve-Switch Buck-Boost Y-Inverter (12-YI) motor drive prototype. Within this context, an EMI equivalent circuit was derived and verified for the 12-YI showing hybrid 6-VSI/6-CSI emission characteristics. Experimental measurements support the filter design process and indicate full compliance for operation with unshielded DC and AC cables according to the IEC 61800-3, where the ultra-compact prototype system features a power density of 12 kW/dm^3 (197 W/in^3).

3

Advanced Modulation Techniques for a 6-YI Auxiliary Motor Drive

This Chapter presents an analysis of the impact of harmonic injection on the performance of a low-complexity buck-boost three-phase motor drive system with sinusoidal output voltages also published in:

- D. Menzi, S. Chhawchharia, G. Zulauf, D. Bortis, H.-P. Nee, J. W. Kolar, "Comparative Evaluation of Harmonic Injection Techniques for a Phase-Modular Three-Phase Six-Switch Buck-Boost Y-Inverter," *IEEE Transactions on Power Electronics*, Vol.37, No. 3, pp. 2519-2524, March 2022) DOI: 10.1109/TPEL.2021.3115903.

Motivation

DC-supplied motor drives powered by renewable energy sources are required to cover a wide DC input voltage range. The Six-Switch Buck-Boost Y-Inverter (6-YI) is a low-component count buck-boost converter topology and therefore of particular interest for cost sensitive applications. As the converter efficiency of a 6-YI is inherently limited by the high component stresses, this Chapter investigates potential performance improvements by means of advanced modulation techniques.

Executive Summary

Phase-modular buck-boost DC/AC inverters extend the voltage conversion range of conventional buck-type inverter topologies, and accordingly offer significant advantages for variable-speed motor drives powered from DC sources with wide-voltage-ranges like fuel cells or batteries. In this chapter, two new modulation schemes are applied to the Six-Switch Buck-Boost Y-Inverter (6-YI) topology, with an analysis of the efficiency improvement for the proposed Third Harmonic Injection PWM (TPWM) and Discontinuous PWM (DPWM) schemes relative to conventional Sinusoidal PWM (SPWM). TPWM substantially reduces conduction losses and DPWM extends this gain by eliminating HF switching of each phase for 1/3 of the fundamental period. These gains are validated on a 1 kW hardware demonstrator across a DC input voltage from 80 V to 240 V, with DPWM reducing total converter losses by 31 % over SPWM for a peak efficiency at nominal load of 95.6 % with a power density of 62.3 W/in^3.

3.1 Introduction

The power supply of electric motors from batteries, FCs or renewable sources introduces the requirement of a wide-DC-voltage range during normal operation – for example, the DC output voltage of an FC to drive an electric motor is dependent on the power and may vary by 3x or more across a normal drive cycle [58]. Similarly, the output of a solar cell in a standalone field application under maximum power point tracking will vary substantially across luminescence [41]. Accordingly, the three-phase DC/AC converters needed for these application areas, must provide both buck and boost capabilities simultaneously.

Phase-modular three-phase buck-boost DC/AC converters have, accordingly, gained interest in these critical applications [41, 58, 76–78]. With the buck-boost capability in a single stage, the need for an additional buck or boost DC/DC converter is obviated, and the phase-modular approach realizes a simple control approach (and the potential for fault tolerance in certain applications). The Twelve-Switch Buck-Boost Y-Inverter (12-YI) topology [58] utilizes four switches per phase with dedicated buck and boost half-bridges, and was shown to reach a peak efficiency of 98.3 % with a power density of 108 W/in^3 for a wide-DC-input-voltage application [67]. The disadvantage of a total of 12 switches, however, is clear and a two-switch realization of the buck-boost converter modules, the Six-Switch Buck-Boost Y-Inverter (6-YI) [76–78]

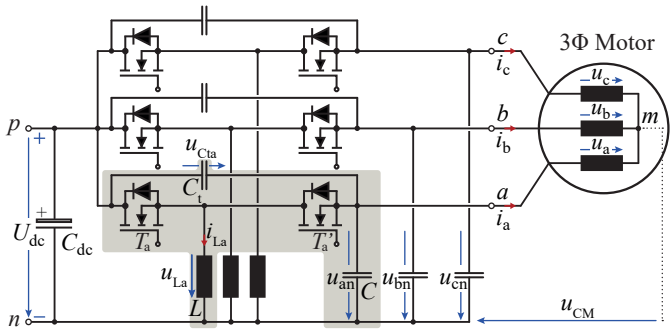

Fig. 3.1: Six-Switch Buck-Boost Y-Inverter (6-YI) to power an electrified auxiliary system (e.g. a pump, fan, or compressor) from a battery or Fuel Cell (FC) power source. Wide DC-input-voltage ranges are a characteristic of these batteries and FCs employed in electric transportation, requiring buck-boost three-phase power conversion. The 6-YI topology results in strictly-negative output capacitor voltages and sinusoidal motor voltages and currents.

Tab. 3.1: 6-YI Specifications.

Parameter	Value
System power P_{nom}	1 kW
DC input voltage U_{dc}	80 V to 240 V
AC pk. voltage $\hat{U}_{ac,nom}$	80 V_{pk}
AC frequency $f_{ac,nom}$	50 Hz
Nominal efficiency η_{nom}	>95 %
Power density ρ	>3 kW/dm^3 (>50 W/in^3)

is an alternative with lower component count and therefore much lower complexity. The main power circuit of the 6-YI is shown in **Fig. 3.1** (module *a* is highlighted in light gray) for an FC-powered motor drive.

The detailed operation principle of the 6-YI was described and verified in [78], where a DC input voltage U_{dc} is converted into strictly-negative output capacitor voltages u_{an},u_{bn},u_{cn} of arbitrary amplitude. Because the offset voltage u_{CM} is present in all three output capacitors, it doesn't result in a current in the open-star-point motor windings and sinusoidal output voltages u_a,u_b,u_c (with amplitude $\hat{U}_{ac}$) and currents i_a,i_b,i_c (with amplitude $\hat{I}_{ac}$) are realized. These continuous AC output voltages reduce the High-Frequency (HF) motor losses [105], a further benefit of the 6-YI topology.

Despite the clear advantages in complexity and reduced component count, though, no performance metrics for the 6-YI exist in literature. Further, although advanced modulation techniques were explored for the 12-YI phase-modular converter in [58] (namely, the conventional Sinusoidal PWM (SPWM), Third Harmonic Injection PWM (TPWM), and Discontinuous PWM (DPWM)), these have not been explored for the 6-YI beyond a cursory mention (without a performance evaluation or hardware validation) in [77]. TPWM is known to increase the utilization of the dc-link voltage in buck-type systems [58], but because the 6-YI is a buck-boost system, the AC output voltage is not constrained by the DC input voltage and TPWM can realize benefits through lowering component voltage and current stresses. Similarly, DPWM is known to decrease switching losses [58] but has not been analyzed for the 6-YI topology.

Our goal here, then, is to analyze and evaluate whether the low-complexity, high-reliability, and low-component 6-YI structure can, with advanced modulation techniques, meet industry-standard requirements for a 1 kW FC-powered auxiliary motor drive with a 1:3 input voltage range of $U_{\mathrm{dc}} = 80\,\mathrm{V}$ to $U_{\mathrm{dc}} = 240\,\mathrm{V}$. With 1 kW motor efficiencies in the 81 %-87 % range [145], the 6-YI efficiency only needs to exceed 95 %, but the power density for these next-generation applications must exceed $50\,\mathrm{W/in^3}$ [146]. Further specifications are detailed in **Tab. 3.1**.

In this chapter, indeed, we demonstrate the important benefits of harmonic injection for the 6-YI, with reductions in semiconductor blocking voltage, semiconductor switching losses, inductor peak and RMS currents, and inductor and semiconductor conduction losses. In **Sec. 3.2**, we summarize the conventional SPWM principle and introduce the two potential harmonic injection techniques, Third Harmonic Injection PWM (TPWM) and Discontinuous PWM (DPWM). The theoretical performance gains of these techniques are verified on a 1 kW hardware demonstrator in **Sec. 3.3**, where we measure up to 2 % efficiency gains (30 % lower losses) with the proposed 6-YI modulation techniques and meet or exceed the auxiliary motor drive specifications. **Sec. 3.4** summarizes the vital improvement in AC/DC power conversion and discusses the tradeoffs between the 6-YI and 12-YI approaches for buck-boost applications.

3.2 6-YI Topology

We briefly detail the fundamentals of 6-YI operation before moving to introduce the proposed harmonic injection techniques. With detailed converter

operation for the 6-YI derived and verified previously [78], we only summarize the basics required to understand the advantages of harmonic injection.

3.2.1 6-YI Fundamentals

With the phase-modular approach of the 6-YI topology, a single phase is sufficient to understand operation, and we use module *a* with references from **Fig. 3.1**.

The blocking voltage for the active semiconductor devices is defined by the commutation capacitor voltage u_{Cta} and depends on the time-varying output capacitor voltage u_{an} as:

$$u_{\mathrm{Cta}}(t) = U_{\mathrm{dc}} - u_{\mathrm{an}}(t) \geq U_{\mathrm{dc}}. \tag{3.1}$$

In the buck-boost topology, the inductor current does not flow continuously towards the output. A balanced voltage-time area for the inductor L yields the duty cycle:

$$d_{\mathrm{a}}(t) = \frac{|u_{\mathrm{an}}(t)|}{U_{\mathrm{dc}} + |u_{\mathrm{an}}(t)|}, \tag{3.2}$$

and, assuming the current into the output filter capacitor C can be neglected in steady-state, the low-frequency inductor current $\langle i_{\mathrm{La}} \rangle$ is defined by the phase output current i_{a} and the duty cycle d_{a} as:

$$\langle i_{\mathrm{La}} \rangle(t) = \frac{-i_{\mathrm{a}}(t)}{1 - d_{\mathrm{a}}(t)}, \quad |\langle i_{\mathrm{La}} \rangle| \geq |i_{\mathrm{a}}(t)|, \tag{3.3}$$

with the HF inductor current ripple $\Delta i_{\mathrm{La,pp}}$:

$$\Delta i_{\mathrm{La,pp}}(t) = \frac{U_{\mathrm{dc}} \cdot d_{\mathrm{a}}(t)}{f_{\mathrm{s}} \cdot L}. \tag{3.4}$$

We see that inductor stress, as expected, increases with increased boosting effort; that is, for a given U_{dc} (and i_{a}), both $|\langle i_{\mathrm{La}} \rangle|$ and $\Delta i_{\mathrm{La,pp}}$ increase monotonically with increasing $|u_{\mathrm{an}}|$ (higher $d_{\mathrm{a}}(t)$).

3.2.2 Harmonic Injection

The proposed harmonic injection for the 6-YI is enabled by the fact that the CM offset voltage u_{CM} remains a degree-of-freedom for the modulation, with only the constraint of the buck-boost topology that the output capacitor voltages u_{an},u_{bn},u_{cn} remain strictly negative. The CM voltage is defined as:

$$u_{\mathrm{CM}}(t) = \frac{1}{3}(u_{\mathrm{an}}(t) + u_{\mathrm{bn}}(t) + u_{\mathrm{cn}}(t)). \tag{3.5}$$

The duty cycle waveform d_{a} is dependent on the output capacitor voltage (see (3.2)), which can be defined in terms of the CM voltage as $u_{\mathrm{an}} = u_{\mathrm{a}} + u_{\mathrm{CM}}$, and the duty cycle therefore depends on the CM voltage. We see, further, that harmonic injection, utilizing a proper $u_{\mathrm{CM}}(t)$, also affects the *(a)* semiconductor blocking voltage u_{Cta}, through (3.1), *(b)* the low-frequency inductor current $\langle i_{\mathrm{La}} \rangle$, through (3.3), and *(c)* the HF inductor current ripple $\Delta i_{\mathrm{La,pp}}$, through (3.4). With switching losses directly determined by blocking voltage, conduction losses (in the semiconductors and inductors) affected by the low-frequency and HF currents, and core losses determined by HF current ripple, we see that intelligent harmonic injection schemes could meaningfully reduce converter losses.

Sinusoidal PWM (SPWM)

The conventional SPWM scheme (employed in [78]) selects a constant offset voltage u_{CM}, with the minimum constant offset limited by the peak output voltage, $\hat{U}_{\mathrm{ac}}$, and selected as this minimum to reduce component stress as:

$$u_{\mathrm{CM,S}} = -\hat{U}_{\mathrm{ac}} \tag{3.6}$$

Note that a margin, of, e.g. 5 % ($u_{\mathrm{CM}} = 1.05 \cdot u_{\mathrm{CM,S}}$) may be included in practical realizations for controllability and to avoid unintended turn-on of semiconductor body diodes. The voltage, duty cycle, and current waveforms for SPWM are given in **Fig. 3.2a**.

Third Harmonic Injection PWM (TPWM)

The TPWM approach of [58] injects a third-harmonic component into u_{CM} to reduce the DC value of u_{CM} relative to SPWM:

$$u_{\mathrm{CM,T}}(t) = -\frac{\sqrt{3}}{2}\hat{U}_{\mathrm{ac}} + \frac{1}{6}\hat{U}_{\mathrm{ac}} \sin\left(3 \cdot (2\pi f_{\mathrm{ac}}) \cdot t\right). \tag{3.7}$$

The voltage, duty cycle, and current waveforms for TPWM are given in **Fig. 3.2b**. With lower output capacitor voltages than under SPWM operation, the semiconductors incur lower switching losses and the inductor current stresses (and losses) are reduced. We note here that a time-varying voltage u_{CM} may cause CM currents in the parasitic capacitance of the motor star-point to ground; these CM currents due to the harmonic injection, however,

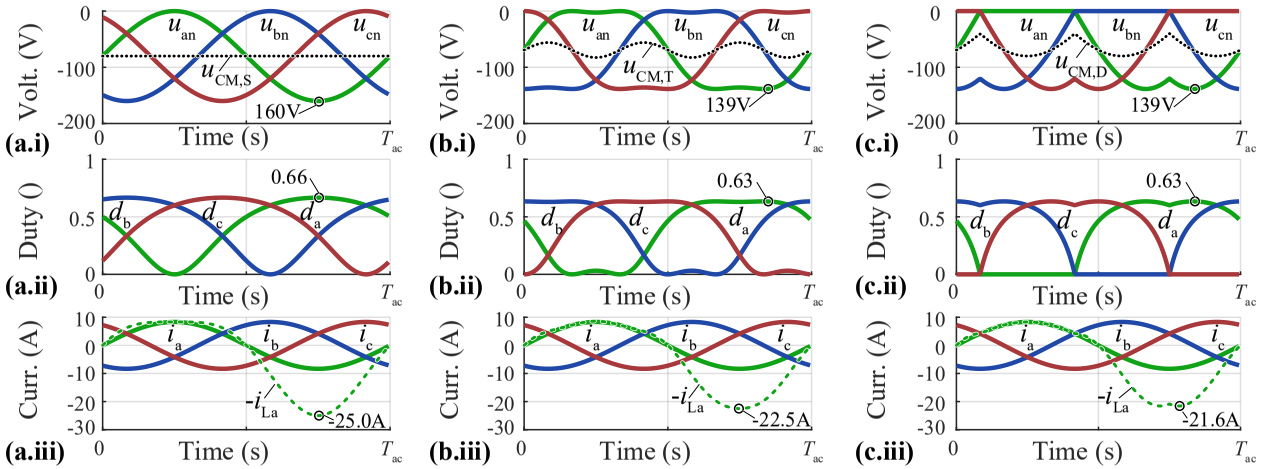

Fig. 3.2: Key converter waveforms for U_{dc} = 80 V and the proposed modulation approaches (**(a)** SPWM, **(b)** TPWM, and **(c)** DPWM), with the output capacitor voltages u_{an},u_{bn},u_{cn} (and the CM voltage u_{CM}), duty cycles d_a,d_b,d_c, and output currents i_a,i_b,i_c (and the negative inductor current $-i_{La}$ of phase *a*) shown. The occurrence of the extreme values of voltage, duty cycle and current of phase *a* within a fundamental period is highlighted with scatter points.

are rather small in amplitude, especially when compared to a standard motor drive system, where a switching-frequency CM voltage drives substantial ground currents [147].

Discontinuous PWM (DPWM)

In DPWM, u_{CM} is selected such that the phase module with the output capacitor voltage closest to zero is not HF switched (i.e., the respective semiconductor T' is permanently turned on) during one-third of the fundamental period [58]. The CM voltage can be defined as:

$$u_{\mathrm{CM,D}}(t) = -\max(u_{\mathrm{a}}(t), u_{\mathrm{b}}(t), u_{\mathrm{c}}(t)). \tag{3.8}$$

The voltage, duty cycle, and current waveforms for DPWM are given in **Fig. 3.2c**, where again the DC component of u_{CM} is reduced compared to SPWM for lower switching losses and inductor currents, but with the added benefit of no HF switching of each phase in one-third of the fundamental period.

3.2.3 Component Stresses

Apart from the selected modulation strategy, the converter component stresses also depend on the voltage step-up ratio, which can be described by the modulation index M as:

$$M = \frac{2\hat{U}_{\mathrm{ac}}}{U_{\mathrm{dc}}}, \tag{3.9}$$

with $M = 1$ corresponding to the maximum output voltage of a standard buck-type inverter with SPWM and $M > 1$, therefore, corresponding to boost operation.

In **Fig. 3.2**, the extreme values of the 6-YI low-frequency waveforms are highlighted, and **Tab. 3.2** provides analytic equations for the operating-point-dependent 6-YI low-frequency component stresses within a fundamental AC period.

The maximum blocking voltage ($u_{\mathrm{Cta,max}} = max(u_{\mathrm{Cta}}(t))$, according to (3.1)) is of particular importance for the selection of the power semiconductors. For all modulation schemes, the worst case value of $u_{\mathrm{Ct,max}}$ results for $U_{\mathrm{dc}} = 240\,\mathrm{V}$ and $M = 2/3$ (i.e., nominal output voltage $\hat{U}_{\mathrm{ac}}$ =80 $\mathrm{V_{pk}}$) and can be reduced from 400 V for SPWM to 379 V for TPWM and DPWM due to the reduced output capacitor voltages. It is important to highlight that the 6-YI semiconductors are exposed to the sum of input *and* output capacitor

Tab. 3.2: 6-YI Analytic low-frequency component stress expressions.

	SPWM	TPWM	DPWM
$u_{\mathrm{Cta,max}}$	$U_{\mathrm{dc}}(M+1)$	$U_{\mathrm{dc}}(1+M\frac{\sqrt{3}}{2})$	$U_{\mathrm{dc}}(1+M\frac{\sqrt{3}}{2})$
$I_{\mathrm{La,rms}}/I_{\mathrm{ac,rms}}$	$\frac{1}{4}\sqrt{7M^2+16M+16}$	$\frac{1}{24}\sqrt{206M^2+288M+576}$	$\frac{1}{8\sqrt{\pi}}\sqrt{(20\pi+3\sqrt{3})M^2+96\sqrt{3}M+64\pi}$
$I_{\mathrm{Ta,rms}}/I_{\mathrm{ac,rms}}$	$\frac{1}{4}\sqrt{M}\sqrt{7M+8}$	$\frac{1}{24}\sqrt{2M}\sqrt{103M+72\sqrt{3}}$	$\frac{1}{8\sqrt{\pi}}\sqrt{M}\sqrt{(20\pi+3\sqrt{3})M+48\sqrt{3}}$
$I_{\mathrm{Ta',rms}}/I_{\mathrm{ac,rms}}$	$\frac{\sqrt{M+2}}{\sqrt{2}}$	$\frac{\sqrt{M\sqrt{3}+4}}{2}$	$\frac{\sqrt{3M\sqrt{3}+4\pi}}{2\sqrt{\pi}}$
$\lvert i_{\mathrm{La}}(t=\frac{3}{4}T_{\mathrm{ac}})\rvert/\hat{I}_{\mathrm{ac}}$	$M+1$	$(\frac{3\sqrt{3}+5}{12})M+1$	$\frac{3}{4}M+1$
$\Delta I_{\mathrm{La,pp,max}}$	$\frac{MU_{\mathrm{dc}}}{(M+1)Lf_{\mathrm{s}}}$	$\frac{\sqrt{3}MU_{\mathrm{dc}}}{(\sqrt{3}M+2)Lf_{\mathrm{s}}}$	$\frac{\sqrt{3}MU_{\mathrm{dc}}}{(\sqrt{3}M+2)Lf_{\mathrm{s}}}$

voltage. In contrast, the 12-YI buck and boost stage semiconductors only block the DC voltage U_{dc} and the output capacitor voltage u_{an}, respectively [67]. Hence, switches with higher voltage rating and worse figure-of-merit [148] are required for the 6-YI, which limits the performance relative to a 12-YI with given DC and AC converter voltage operating ranges.

Tab. 3.2 also highlights the low-frequency RMS current stresses of the inductor and both the high-side T_{a} and low-side semiconductor T_{a}' within a fundamental AC period, all normalized by the AC output current. There, the worst-case stresses result for the maximum step-up ratio with $U_{\mathrm{dc}} = 80\,\mathrm{V}$ and $M = 2$ (i.e., nominal output voltage $\hat{U}_{\mathrm{ac}} = 80\,\mathrm{V_{pk}}$). Harmonic injection reduces the low-frequency inductor RMS current stresses from $12.8\,\mathrm{A_{rms}}$ with SPWM to $12.0\,\mathrm{A_{rms}}$ (−6 %), and $11.8\,\mathrm{A_{rms}}$ (−8 %), corresponding to a conduction loss decrease of −12 % and −16 % for TPWM and DPWM, respectively. The maximum absolute value of the low-frequency inductor current according to (3.3) can be approximated with $max(|i_{\mathrm{La}}(t)|) \approx |i_{\mathrm{La}}(t = \frac{3}{4}T_{\mathrm{ac}})|$, where harmonic injection again reduces this critical metric to the design of the power inductor (to avoid saturation). Overall, the 6-YI is subject to elevated RMS and peak low-frequency current stresses compared to the 12-YI [67] due to the fact that the 6-YI inductor current is strictly larger than the AC output current (cf., (3.3)), even for buck operation with $M \leq 1$.

Lastly, we highlight that the switching-frequency inductor current impacts both the converter conduction stresses and the current-dependent hard- and soft-switching losses in the semiconductors. In **Tab. 3.2**, only the maximum inductor current HF ripple ($\Delta I_{\mathrm{La,pp,max}} = max(\Delta i_{\mathrm{La,pp}}(t))$, according to (3.4)) is provided, as the analytic expressions for the overall HF RMS current stresses are excessively complex. Accordingly, the resulting switched inductor current waveforms were calculated numerically for the converter design and loss distribution calculation presented in **Sec. 3.3**.

3.3 Hardware Validation

3.3.1 Test Setup

To compare the performance of the three modulation strategies, a 1 kW 6-YI hardware demonstrator is constructed (shown in **Fig. 3.3a**). This demonstrator is operated with a switching frequency $f_{\mathrm{s}} = 300\,\mathrm{kHz}$, for small filter components and high power density, into a resistive three-phase load of $R = 9.6\,\Omega$ at $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$ (for unity power factor operation, the typical operating condition for a synchronous permanent magnet machine [67]). A volume

breakdown of the hardware prototype is given in **Fig. 3.3b**, with the power inductors still constituting nearly one quarter of the total volume, even with the high selected switching frequency. Because of the low inductor value needed to achieve high power density, the converter operates in complete or partial soft-switching for a major of the period, and a direct measurement comparison of the proposed modulation techniques is more accurate and direct than a difficult analytical approach to loss estimation.

The output current control implementation deserves a special explanation, as the high switching frequency f_s may result in a high and/or expensive computational burden. Instead of the traditional three cascaded PI controllers *per phase*, a simple control structure is implemented here (summarized visually in **Fig. 3.4**). The current flowing into the output capacitor C is neglected, and the phase current reference i_a^* is directly translated into a corresponding inductor current reference i_{La}^*. A PI controller then tracks this inductor current reference by adjusting the duty cycle d_a^*, which is subsequently processed by a PWM block into the mutually-exclusive switching signals T_a and T_a'. With a single PI controller per phase, this control technique can be implemented with a low-cost DSP instead of an FPGA.

3.3.2 Experimental Waveforms

The measured converter waveforms for the three considered modulation strategies are given in **Fig. 3.5** for a nominal output power of 1 kW and an input voltage of $U_{dc} = 80\,\text{V}$ (and with a 5 % margin on the DC component of the CM voltage in SPWM and TPWM to avoid an unintended polarity reversal). As predicted, the low-frequency inductor current $-\langle i_{La}\rangle$ peak value is reduced by 8 % under TPWM and 14 % under DPWM relative to SPWM, an important result that is highlighted with the dotted line of the maximum magnitude of $-\langle i_{La}\rangle = 24.4\,\text{A}$ under SPWM. DPWM exhibits the lack of HF switching during 1/3 of the fundamental period, as expected. Finally, because of the relatively low inductance value ($L = 9.3\,\mu\text{H}$), the converter is soft-switched during a relatively large portion of the period (anywhere, to first order, with a polarity reversal of i_{La}).

The measured ratio of $i_{La,rms}/I_{ac,rms}$ at $P = 1\,\text{kW}$ for different values of U_{dc} is summarized in **Tab. 3.3**, and reduces from 2.44 (SPWM) to 2.06 (DPWM) at $U_{dc} = 80\,\text{V}$ and from 1.93 (SPWM) to 1.67 (DPWM) at $U_{dc} = 240\,\text{V}$. This underscores that while harmonic injection and DPWM are valuable at any input voltage, the proposed techniques are especially impactful at high step-up ratios (i.e., low dc input voltage). **Tab. 3.3** also provides the measured

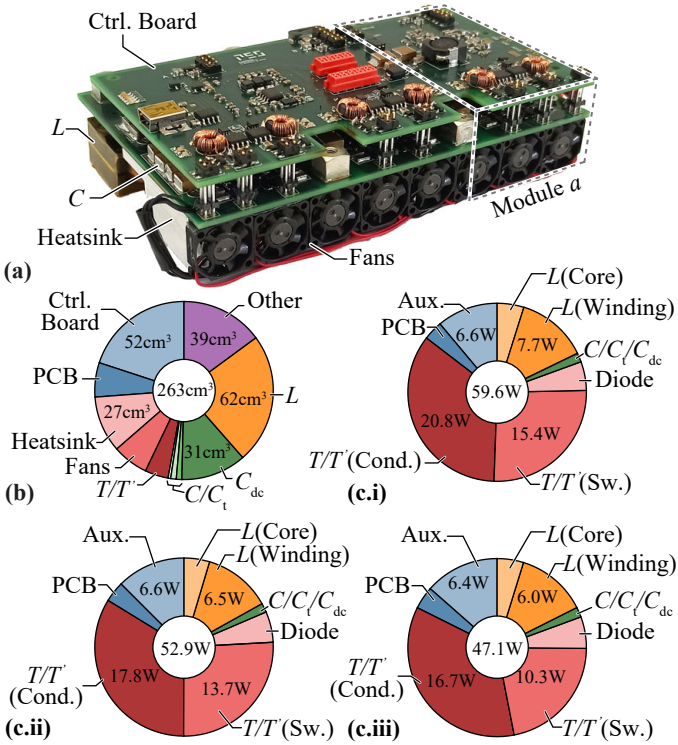

Fig. 3.3: (a) 1 kW 6-YI hardware prototype for an FC-powered auxiliary motor drive with dimensions 120 mm x 80 mm x 27.4 mm for a power density of 62.3 W/in^3. Power semiconductors are 2x IFX GaN IGLD60R070D1 (600 V, 70 mΩ) switched at 300 kHz and controlled by the *TMS320F28335* DSP. Power inductors (L = 9.3 µH) are implemented with a TDK ELP 32 ferrite core (N87) with a 1.0 mm air gap and 8 turns of 420 x 71 µm litz wire. The capacitor values are C = 2 µF and C_t = 2.2 µF. Further prototype specifications are given in **Tab. 3.1**. **(b)** Converter volume distribution, with the control board and power inductors together comprising 43 % of total volume. **(c)** Calculated loss distribution under **(c.i)** SPWM, **(c.ii)** TPWM, and **(c.iii)** DPWM operation for U_{dc} = 80 V and P_{nom} = 1 kW. The losses of the power semiconductors (conduction and switching) dominate the total converter losses (> 57 % of total losses), even with the loss reduction of DPWM.

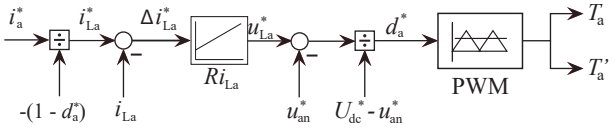

Fig. 3.4: Output current control diagram of the 6-YI module *a*.

Total Harmonic Distortion (THD). The maximum THD values result for the minimum value $U_{dc} = 80\,V$, i.e., for the maximum step-up ratio. This can be explained by the simple control scheme depicted in **Fig. 3.4**, which does not consider the reactive current flow into the output capacitor, C. Further, the THD values are higher for TPWM and DPWM compared to SPWM, which can be explained by the additional frequency components in the output voltage waveforms (cf., **Fig. 3.2**). However, even for DPWM, the maximum THD value remains $< 5\,\%$.

With the expected converter waveforms validated, the input voltage U_{dc} and output power are swept to measure the efficiency improvement of the proposed harmonic injection schemes.

3.3.3 Efficiency Measurements

The converter power losses are measured with a Yokogawa WT1804E power analyzer and reported in **Fig. 3.6** for DC input voltages of 80 V and 240 V. At low-power levels, the losses for SPWM and TPWM are nearly identical, with the advantages of TPWM increasing with higher output powers up to a loss decrease of 13 % for $U_{dc} = 80\,V$. This power-dependent comparison occurs because, although the switched voltage is slightly reduced in TPWM over SPWM, the main improvement is in the smaller conduction losses from reduced low- and HF currents in TPWM.

DPWM reaches the maximum measured efficiency of 95.6 % for $U_{dc} = 240\,V$, with substantial conduction *and* switching loss decreases relative to SPWM and TPWM. A loss breakdown for DPWM operation at $U_{dc} = 80\,V$ is given in **Fig. 3.3c.iii**, where the semiconductor losses comprise nearly 60 % of total converter losses – even with the reductions in both switching and conduction losses of DPWM. The switching loss decrease, in particular, is especially valuable at lower output powers, where DPWM achieves a multi-point efficiency improvement relative to SPWM and TPWM at all input voltages at $P = 100\,W$ (especially pronounced at high U_{dc} operating points, which have the highest switching losses). The loss decrease of DPWM

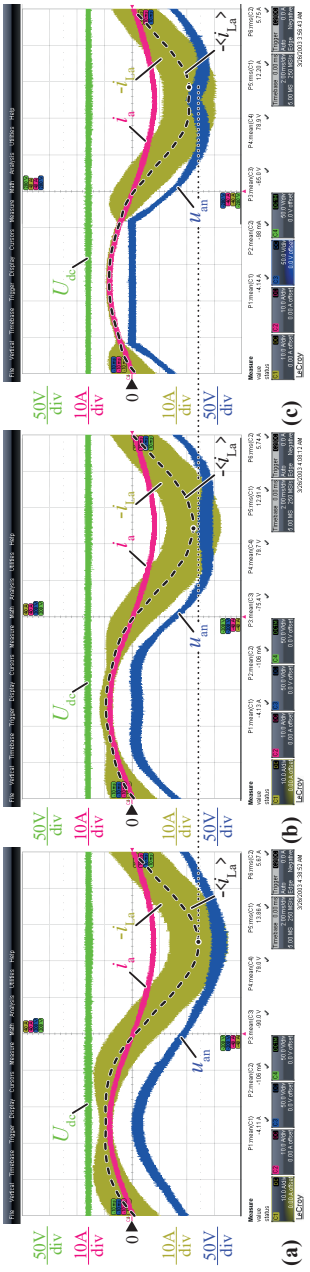

Fig. 3.5: 6-YI experimental voltage (module *a* output capacitor voltage u_{an}) and current (output current i_a and negative inductor current $-i_{La}$) waveforms for modulation with **(a)** SPWM, **(b)** TPWM, **(c)** DPWM at DC input voltage U_{dc}=80 V. The negative low-frequency inductor current $-\langle i_{La} \rangle$ was extracted from the exported oscilloscope waveforms and added manually for illustration purposes, with maximum magnitude values of 24.4 A for SPWM, 22.6 A (-8 %) for TPWM, and 21.0 A (-14 %) for DPWM.

Tab. 3.3: Relative inductor current stress and THD at $P = 1\,\mathrm{kW}$ for different modulation strategies.

U_{dc}	80 V	160 V	240 V
	$I_{\mathrm{La,rms}}/I_{\mathrm{ac,rms}}$ (p.u.)		
SPWM	2.44	1.96	1.93
TPWM	2.24	1.84	1.81
DPWM	2.06	1.70	1.67
Total Harmonic Distortion (THD) (%)			
SPWM	3.3	3.4	1.3
TPWM	2.9	2.8	1.1
DPWM	3.7	4.0	2.7

over SPWM reaches 31 % for $U_{\mathrm{dc}} = 240\,\mathrm{V}$ and $P = 1\,\mathrm{kW}$, with an associated efficiency increase of a full 2 %.

3.4 Conclusions

In this chapter, we propose two harmonic injection schemes for the Six-Switch Buck-Boost Y-Inverter (6-YI), a low complexity phase-modular buck-boost three-phase inverter. These new modulation techniques improve both conduction (through reduced low- and HF currents) and switching (through reduced blocking voltages and, for DPWM, no HF switching of each phase during 1/3 of the fundamental period). The advantages of the novel modulation strategies are validated on a 1 kW hardware prototype that achieves the auxiliary motor drive targets of 95 % efficiency and 50 $\mathrm{W/in^3}$ power density, with the efficiency metric only achievable with the loss reductions of TPWM and DPWM of up to 31 % relative to the conventional SPWM (at nominal power).

With these modulation schemes, the 6-YI topology becomes more attractive in applications requiring buck-boost capabilities, although the consequence of simplicity and a low component count remains: even with the advanced modulation schemes, the 6-YI incurs a simultaneous penalty of a 2× reduction in power density and a 2× increase in losses relative to the Twelve-Switch Buck-Boost Y-Inverter (12-YI) [67]. The selection of topology for a phase-modular, single-stage, buck-boost inverter will, therefore, be de-

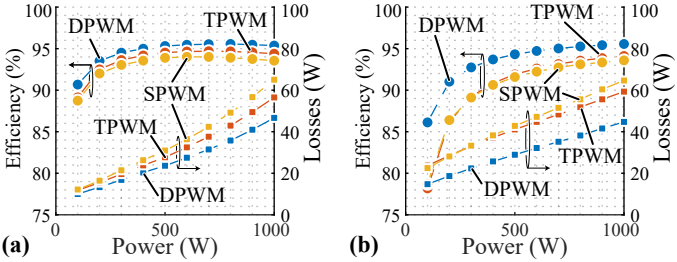

Fig. 3.6: Measured converter efficiency (round scatter symbols) and power losses (square scatter symbols) over output power for **(a)** $U_{dc} = 80\,V$ and **(b)** $U_{dc} = 240\,V$ for the considered modulation techniques. Auxiliary circuits were externally supplied, with measured auxiliary powers of $P_{aux} = 6.6\,W$ for SPWM and TPWM and $P_{aux,D} = 6.4\,W$ for DPWM (due to reduced gate drive power). The auxiliary power consumption is included in the reported efficiencies.

pendent on the particular application weights to complexity, efficiency, size, and cost.

4

Novel Return-Path-Inductor 12-YI Motor Drive

This Chapter presents a new phase-modular buck-boost three-phase inverter structure, allowing for ever more compact converter realizations also published in:

- D. Menzi, J. E. Huber, L. Kappeler, G. Zulauf, J. W. Kolar, "New Return-Path-Inductor Buck-Boost Y-Inverter Motor Drive with Reduced Current Stresses," *IEEE Transactions on Power Electronics*, Vol. 37, No. 9, pp. 10086-10090, September 2022 DOI: 10.1109/TPEL.2022.3163465.

Motivation

Phase-modular buck-boost three-phase DC/AC converter system are extremely versatile as they allow operation with wide (and overlapping) input output-voltage ranges. However, the buck-boost inductors are typically subject to large low-frequency current stresses, thereby limiting the overall converter power density. The topology of the Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (RPI-12-YI) locates the buck-boost inductor in the current return path, thereby reducing the current stresses substantially, hence promises ever more compact converter realizations.

Executive Summary

Variable Speed Drives (VSDs) for electric motors are a foundational component of global electrification, with electric motors consuming 45% of global electricity. Conventional three-phase buck-boost inverter topologies have substantial low-frequency current stresses in the buck-boost inductor, driving size, losses, and cost in VSD systems. In this chapter, we propose a novel circuit topology for phase-modular three-phase buck-boost inverter systems based on the four-switch non-inverting buck-boost concept, which we call the Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (RPI-12-YI). By relocating the buck-boost inductors of the phase modules from the forward current path to the return path, the RPI-12-YI concept reduces the inductor RMS and peak current stresses by up to 90 % compared to a conventional topology, resulting in a potential magnetics volume reduction of 80 %. The RPI-12-YI concept, therefore, supports more compact, efficient realizations of modular buck-boost VSD systems.

4.1 Introduction

Variable Speed Drives (VSDs) for electric motors are a critical element of the infrastructure that supports broad electrification [16, 17], with electric motors and their drives currently accounting for 45 % of the world's total electricity usage [149]. The existing and increasing ubiquity of electric motors demands VSDs that feature a wide operating range and are efficient, cost-effective, power-dense, and tightly integrated.

For VSD applications that require motor drive voltages both above and below the DC-link voltage, the state-of-the-art topology is the Forward-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (FPI-12-YI) [1], which is shown in **Fig. 4.1a** [58, 64, 65, 67, 150]. This inverter structure is phase-modular, features a low number of magnetic components, and has mutually exclusive, i.e., quasi-single-stage buck and/or boost HF conversion in each module. The FPI-12-YI converts a dc input voltage U_{dc} into strictly positive output capacitor voltages u_{an}, u_{bn}, u_{cn} of arbitrary amplitude below and above U_{dc}. An offset voltage u_{CM} is present in all three output capacitor voltages, and therefore does not drive a current into the open-star-point motor windings.

[1] Note that the FPI-12-YI corresponds to the standard 12-YI and is labelled differently in this Chapter to prominently highlight the location of the buck-boost inductor.

Accordingly, sinusoidal motor phase voltages u_a, u_b, u_c (with amplitude $\hat{U}_{ac}$ and low HF content due to the output capacitor of each module) and currents i_a, i_b, i_c (with amplitude $\hat{I}_{ac}$) are applied to the motor.

The primary drawback of the conventional FPI-12-YI topology is that the buck-boost inductor in each stage, L, is subject to high Low-Frequency (LF) current stresses, especially for high modulation indices $M = 2\hat{U}_{ac}/U_{dc}$, where the peak LF current is given by $\hat{I}_L = \hat{I}_{ac} \cdot \max(1, M)$ — an LF current stress that is strictly larger than the motor current (see Fig. 4.3a). This buck-boost inductor, therefore, drives cost, size, losses, and design complexity in such FPI-12-YI VSD systems.

We propose a novel topology to reduce these LF current stresses, drawing inspiration from literature that relocates inductors of a DC/DC buck converter to lower current stress [151]. The proposed Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (RPI-12-YI) concept is shown in **Fig. 4.1b**, where the buck-boost inductor L is relocated to the return path to dramatically lower the LF current stress. The RPI-12-YI concept maintains the critical properties of the FPI-12-YI topology — most notably, phase modularity and buck-boost capabilities — but the peak LF current stresses are now given by $\hat{I}_L = \hat{I}_{ac} \cdot (\max(1, M) - 1)$, a dramatic reduction relative to the FPI-12-YI current stresses (see Fig. 4.3b). The symmetric three-phase load currents i_a,i_b,i_c sum to zero in the motor winding star-point, flowing from one phase to another without introducing any LF inductor currents in buck operation (cf., **Fig. 4.1**) and substantially reducing current stresses in boost operation. While inductor-less buck-boost inverter topologies exist in literature (e.g., [152]), eliminating the buck-boost inductor entirely comes at the cost of an increased number of active components, limited load angle ranges, and the need for three capacitive LF energy storage elements. As a topology candidate, then, the RPI-12-YI is conceptually positioned between an FPI-12-YI, with large magnetics volume and stresses, and these fully inductor-less buck-boost inverters, with the limitations outlined above.

In this chapter, we detail the RPI-12-YI operating principle (**Sec. 4.2**), briefly discuss the control structure (**Sec. 4.3**), and verify the dramatic reduction in inductor current stresses in a hardware demonstrator (**Sec. 4.4**) before concluding the Chapter in **Sec. 4.5**.

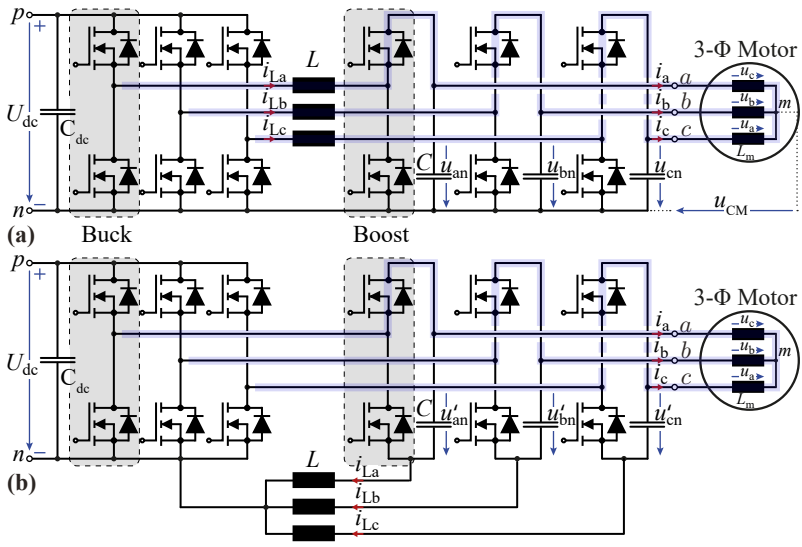

Fig. 4.1: Main power circuit topology of **(a)** standard Forward-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (FPI-12-YI), as well as **(b)** proposed novel Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (RPI-12-YI) Variable Speed Drive (VSD). The motor current paths in buck operation are highlighted in light blue.

4.2 RPI 12-YI Topology

The operating principle of the RPI-12-YI can be characterized by a single module, since each phase is operated independently. The circuit of phase module *a* under RPI-12-YI operation for buck and boost mode are shown in **Fig. 4.2a.i** and **a.ii**, respectively, with the output capacitor voltage waveforms u'_{an}, u'_{bn}, u'_{cn} shown in **Fig. 4.2b** under Sinusoidal PWM (SPWM) operation (that is, with a minimum constant offset voltage $u'_{CM} = \hat{U}_{ac}$).

The operating mode (buck or boost) depends on the instantaneous modulation index, i.e.,

$$\begin{aligned} m(t) &= u'_{an}/U_{dc} = M(1+\sin(\omega t)), \\ M &= 2\hat{U}_{ac}/U_{dc}, \end{aligned} \tag{4.1}$$

where ω denotes the angular frequency of the output voltage.

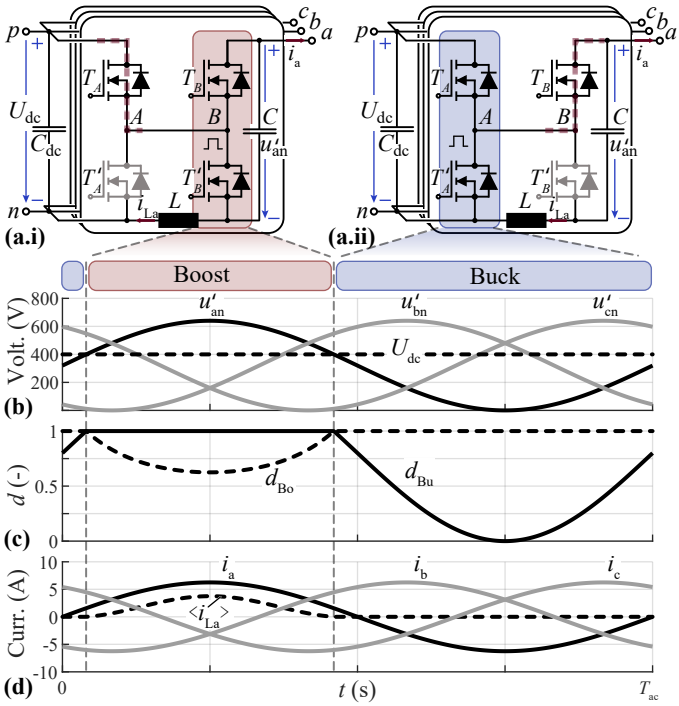

Fig. 4.2: Operating concept of the RPI-12-YI, highlighted for phase module *a*. **(a.i)** boost operation ($u'_{an} > U_{dc}$) and **(a.ii)** buck operation ($u'_{an} \leq U_{dc}$). **(b)** DC input voltage U_{dc} and output capacitor voltage waveforms $u'_{an}, u'_{bn}, u'_{cn}$ for a constant CM offset voltage, i.e., sinusoidally shaped phase-module output voltages. **(c)** Duty cycles of the module *a* buck half-bridge d_{Bu} and of the boost half-bridge d_{Bo}. **(d)** Motor currents i_a, i_b, i_c and LF buck-boost inductor current $\langle i_{La} \rangle$.

For $m(t) > 1$ ($u'_{an} > U_{dc}$), phase module a operates instantaneously in boost mode (**Fig. 4.2a.i**). In this mode, the high-side switch of the buck bridge-leg T_A is on (connecting node A to the positive DC-link rail p) and the boost half-bridge (T_B, T'_B) regulates the output voltage. In this configuration, the inductor remains in the LF path and incurs a LF current component $\langle i_{La} \rangle$ in addition to the HF current ripple.

For $m \leq 1$ ($u'_{an} \leq U_{dc}$), phase module a operates instantaneously in buck mode, as shown in **Fig. 4.2a.ii**. The high-side switch of the boost bridge-leg T_B is kept on, continuously connecting node B to the output terminal a, and the buck half-bridge (T_A, T'_A) is switched to regulate the output voltage. In the RPI-12-YI configuration, the output capacitor C acts as a DC (and LF AC) block, and the inductor does not conduct any LF current. The AC output current is returned via the other two motor phases (cf., **Fig. 4.1**). The RPI-12-YI inductor does still incur an HF Voltage-Time Area (VTA) and therefore an HF current ripple, which can be used to decrease the hard-switching losses of the power semiconductors or even to achieve full soft-switching [153, 154].

The duty cycles for mutually exclusive operation of the buck and boost half-bridges are shown in **Fig. 4.2c**, with identical duty cycles to the FPI-12-YI [58] that are set dependent on the instantaneous modulation index of (4.1) as

$$d_{Bu}(t) = \min(1, m(t)), \tag{4.2}$$

$$d_{Bo}(t) = \min(1, 1/m(t)), \tag{4.3}$$

where d_{Bu} and d_{Bo} denote the duty cycles of the buck and boost half-bridge, respectively.

In both operating modes, the output terminal voltage (relative to the negative DC-link rail u_{an}) is the sum of the continuous output capacitor voltage u'_{an} and the buck-boost inductor voltage u_{La}, which includes an HF voltage component. Therefore, an inductive load (for example, provided by the winding inductance L_m of the electric machine, cf., **Fig. 4.1b**) is required for the RPI-12-YI to operate with a sinusoidal output current. However, with typical motor inductance values L_m in the mH-range (i.e., $L_m >> L$), the resulting HF motor current variation caused by the RPI-12-YI remains small compared to the HF current ripple in the buck-boost inductor L. Also, no LF motor current harmonic distortion occurs. Note that this limitation to inductive loads does not apply to the traditional FPI-12-YI configuration; the FPI-12-YI would allow to impress sinusoidal output currents also into purely ohmic loads.

4.2.1 Magnetics Volume Assessment

The time-varying LF local average (within one switching cycle) inductor current $\langle i_{\mathrm{La}} \rangle$ is found by balancing the output capacitor C charge in periodic steady-state operation, and is dependent on the boost half-bridge duty cycle $d_{\mathrm{Bo}}(t)$:

$$\langle i_{\mathrm{La}} \rangle(t) = \frac{i_{\mathrm{a}}(t)(1 - d_{\mathrm{Bo}}(t))}{d_{\mathrm{Bo}}(t)}. \tag{4.4}$$

The LF inductor current is, therefore, zero in buck operation ($d_{\mathrm{Bo}}(t) = 1$, see in **Fig. 4.2c,d)** and is significantly reduced compared to FPI-12-YI current stresses.

More generally, the LF FPI-12-YI and RPI-12-YI buck-boost inductor current stresses are compared across modulation index M (see (4.1)) in **Fig. 4.3** (normalized against AC output current), where I_{L} and $\hat{I}_{\mathrm{L}}$ represent the (global) RMS and peak value of $\langle i_{\mathrm{La}} \rangle$, respectively, within one fundamental period. The proposed RPI-12-YI approach has a significant reduction in both RMS and peak current stresses in both buck and boost operation across the entire modulation index M. This dramatic reduction occurs because the three-phase motor currents are summing to zero in the motor starpoint, and therefore, in buck operation no LF current returns via the RPI-12-YI inductor ($I_{\mathrm{L}} = 0$ A).

For a given operating point and switching frequency, the HF VTA applied to the buck-boost inductors is identical for FPI-12-YI and RPI-12-YI, and when selecting identical inductance values L, the inductor area product is [155]

$$AP \propto L\hat{I}_{\mathrm{L}}I_{\mathrm{L}}. \tag{4.5}$$

Assuming a maximum $M = 1.6$, this area product is reduced by 90 % for the proposed RPI-12-YI configuration over the conventional FPI-12-YI. With the volume of an inductor scaling approximately with $AP^{\frac{3}{4}}$ [156], this corresponds to a reduction in the inductor volume of ≈80 % compared to the conventional FPI-12-YI.

4.2.2 Converter Loss Considerations

In order to allow a performance estimate for an RPI-12-YI system the main converter loss components are compared qualitatively to an FPI-12-YI in the following:

- **Semiconductors:** Given $L_{\mathrm{m}} >> L$ (i.e., negligible HF motor current variation), the buck and boost semiconductor switched voltages and the conducted HF and LF currents of RPI-12-YI and FPI-12-YI are identical

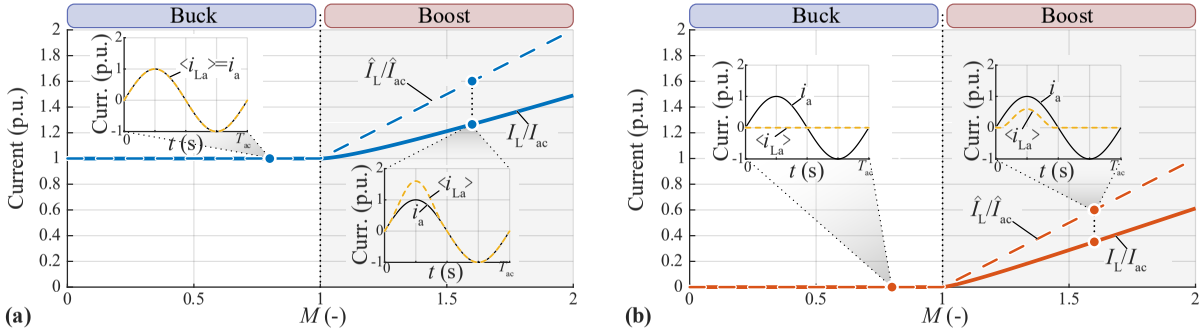

Fig. 4.3: LF RMS and peak current stresses of the buck-boost inductor L under **(a)** conventional FPI-12-YI operation and **(b)** the proposed RPI-12-YI concept. Values are normalized to the RMS and peak AC motor current over the modulation index $M = 2\hat{U}_{ac}/U_{dc}$. LF current waveforms are highlighted for $M = 0.8$ and $M = 1.6$.

for a given operating point. Hence, identical semiconductor switching and conduction losses can be expected.

- **Capacitors:** Both DC-link C_{dc} and AC-side capacitors C (given $L_{\mathrm{m}} >> L$) of RPI-12-YI and FPI-12-YI are subject to identical HF current stresses and accordingly the same capacitor losses.

- **Inductors:** As discussed in **Sec. 4.2.1**, the buck-boost inductors L of RPI-12-YI and FPI-12-YI are subject to the same HF VTA, such that (neglecting the impact of the LF premagnetization) identical HF inductor losses can be expected. In contrast, the LF conduction losses of the RPI-12-YI inductors are substantially reduced compared to the FPI-12-YI.

Based on this component stress assessment, RPI-12-YI efficiency values very similar to the FPI-12-YI can be expected (with reported FPI-12-YI efficiency values $> 98\,\%$ [67, 150]), with the main advantage of the RPI-12-YI magnetics volume reduction.

4.3 Control

While control is not the primary topic of this chapter, we include a brief discussion of a possible control structure for the proposed RPI-12-YI topology for completeness, with a graphical overview shown in **Fig. 4.4**.

The RPI-12-YI topology applies the switched PWM voltages directly to the motor, so a standard motor control algorithm for a buck-type voltage source inverter can be utilized (with the additional buck-boost functionality enabling $m(t) > 1$). Note that this is a major difference from the standard FPI-12-YI, where the motor currents must be controlled by adjusting the output capacitor voltages [58]).

The speed and torque controller—typically in the dq reference frame—seeks to drive the difference between the angular speed reference ω^* and the measured value ω to zero by selecting the appropriate motor phase voltage references u_{a}^*, u_{b}^*, u_{c}^* in order to impress according torque generating currents in the motor stator windings. The desired LF capacitor voltage reference (here, for module a) is calculated by adding the appropriate CM offset voltage value u'_{CM}, and this voltage reference is, in the end, translated into a modulation index m^* (through (4.1)) and duty cycles d_{Bu}^*, d_{Bo}^* (through (4.2)).

The current in the RPI-12-YI inductor L does not necessarily need to be controlled (the LF current $\langle i_{\mathrm{La}} \rangle(t)$ displayed in **Fig. 4.2d** results naturally in

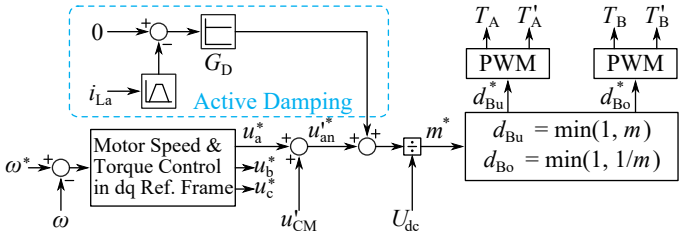

Fig. 4.4: Example RPI-12-YI control concept. The active damping is not strictly required but allows for aggressive motor current control without introducing ringing in the buck-boost inductor currents.

open-loop operation), but ringing may occur if the motor current control is aggressive. To avoid this ringing and support a high-bandwidth control regime, active damping can be introduced, as shown in **Fig. 4.4**, where the HF content of i_{La} (i.e., with reference value equal to zero) is directly regulated through a correction term that is added to the output capacitor voltage reference value. Alternatively, the fully-cascaded control structure proposed in [58] could be used for the RPI-12-YI, with the innermost controller regulating either the buck-boost inductor current or the current between the nodes A and B (see **Fig. 4.2**).

4.4 Experimental Verification

The proposed RPI-12-YI concept is validated with a hardware demonstrator system, built according to the specifications shown in **Tab. 4.1** (component designators refer to **Fig. 4.1b**) and with 1.2 kV SiC MOSFETs as the bridge-leg power semiconductors. An inductive-resistive three-phase load (i.e., operation close to unity power factor as it is typical for permanent magnet synchronous machines [67]) is driven from a DC input voltage of $U_{dc} = 400\,\text{V}$ and the RPI-12-YI inverter is operated with open-loop control.

Fig. 4.5a shows the measured operating waveforms during buck-mode operation at $M = 0.8$, $\hat{I}_{ac} = 5.5\,\text{A}$, and $P = 1.7\,\text{kW}$. The inverter generates a sinusoidal AC output current i_a, and the terminal a output voltage (relative to the negative DC-link rail) u_{an} remains strictly below U_{dc}, as it must under buck operation. The LF output voltage component $\langle u_{an} \rangle \approx u'_{an}$ is extracted from the captured oscilloscope data and added to **Fig. 4.5a** for completeness.

Tab. 4.1: RPI-12-YI prototype specifications.

Parameter	Value
System power P_{nom}	3.3 kW
DC input voltage U_{dc}	400 V
AC pk. voltage $\hat{U}_{\mathrm{ac}}$	160 V_{pk} / 320 V_{pk}
AC frequency f_{ac}	50 Hz
Switching frequency f_{s}	100 kHz
DC-link capacitor C_{dc}	60 µF
Buck-boost inductor L	220 µH
Capacitor C	2.2 µF
Load inductor L_{M}	2.8 mH
Load resistor	25 Ω/50 Ω

Most importantly for the verification of the RPI-12-YI concept, the buck-boost inductor current i_{La} has zero LF component $\langle i_{\mathrm{La}} \rangle = 0$, as expected.

Operation in boost mode is shown in **Fig. 4.5b**, with $M = 1.6$, $\hat{I}_{\mathrm{ac}} = 5.5\,\mathrm{A}$, and $P = 3.3\,\mathrm{kW}$. Here, during the first half of the cycle, the converter operates in a boost mode with u_{an} above U_{dc}, and the buck-boost inductor incurs an LF current $\langle i_{\mathrm{La}} \rangle > 0$ when $m(t) > 1$.

These measured current stresses for the RPI-12-YI buck-boost inductor are compared to the analytical values in **Tab. 4.2**, with the RMS and peak currents normalized to the AC output current. The measured values are close to those predicted by **Fig. 4.3**, with slightly higher measured stresses due to *(a)* a selected offset voltage of $u'_{\mathrm{CM}} = 105\,\% \hat{U}_{\mathrm{ac}}$ for a practical realization and *(b)* non-zero LF capacitive reactive currents from the output capacitors C returning via the buck-boost inductors (see **Fig. 4.2**). Nonetheless, the predicted RPI-12-YI operation matches the measured results closely, validating the dramatic reduction in LF current inductor stress for the proposed RPI-12-YI approach.

4.5 Conclusions

VSDs are a critical component to the widespread electrification of industry, logistics, and mobility. In this chapter, we propose a new topology and oper-

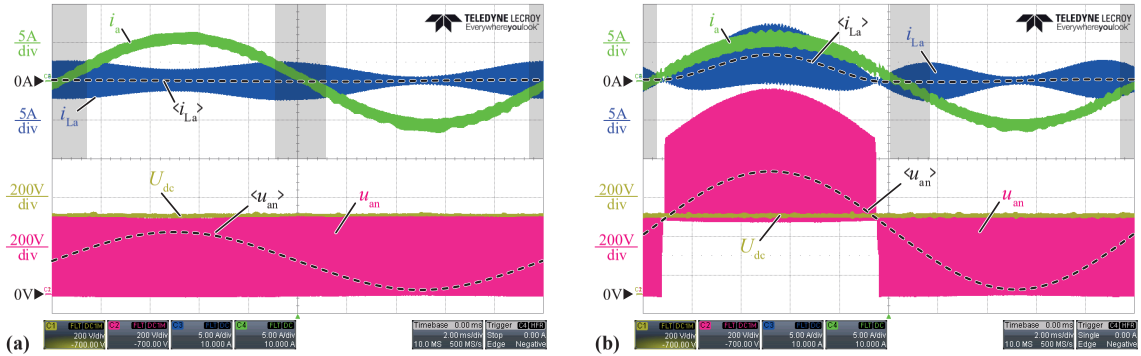

Fig. 4.5: RPI-12-YI experimental waveforms: DC input voltage U_{dc}, module a terminal output voltage with respect to the negative DC-link rail u_{an}, AC output current i_{a}, and buck-boost inductor current i_{La}. Both operating points were recorded with $U_{\mathrm{dc}} = 400\,\mathrm{V}$ and $\hat{I}_{\mathrm{ac}} = 5.5\,\mathrm{A}$, with **(a)** $M = 0.8$ ($P = 1.7\,\mathrm{kW}$) and **(b)** $M = 1.6$ ($P = 3.3\,\mathrm{kW}$). The LF buck-boost inductor current $\langle i_{\mathrm{La}} \rangle$ and output voltage $\langle u_{\mathrm{an}} \rangle = u'_{\mathrm{an}}$ were extracted from the exported oscilloscope waveforms and added on top of the screenshots as dashed lines, for illustration purposes. Regions of the fundamental period where the semiconductor current direction inverts within one switching period (where zero-voltage-switching could be achieved) are highlighted in light grey.

Tab. 4.2: RPI-12-YI LF current stresses.

Op.	Param.	Calc.	Meas.	Error
$M = 0.8$	I_L/I_{ac}	0.0	0.03	-
	$\hat{I}_L/\hat{I}_{ac}$	0.0	0.04	-
$M = 1.6$	I_L/I_{ac}	0.35	0.38	+8.6 %
	$\hat{I}_L/\hat{I}_{ac}$	0.60	0.64	+6.7 %

ating concept to reduce the largest passive component in buck-boost inverter drives, the inductor. The Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (RPI-12-YI) concept moves this buck-boost inductor from the forward path (conventional, or Forward-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (FPI-12-YI)) to the return path, reducing the LF current stresses by up to 90 % considering a typical operating range. We explain the basic operating principles of the RPI-12-YI topology, derive an analytical current stress comparison between the RPI-12-YI topology and the conventional FPI-12-YI approach, and validate the proposed approach with a hardware demonstrator. The measured waveforms demonstrate sinusoidal output currents with the theorized reduction in LF peak and RMS current stresses of up to 90 % over the conventional FPI-12-YI topology.

This RPI-12-YI current stress reduction corresponds to an 80 % smaller magnetics volume, and harmonic injection techniques could further reduce the component stresses [58]. This concept is proposed and demonstrated for VSD systems, but is also applicable to buck-boost rectifier applications (cf., **Fig. 4.6**) that are equally important to our more-electric future.

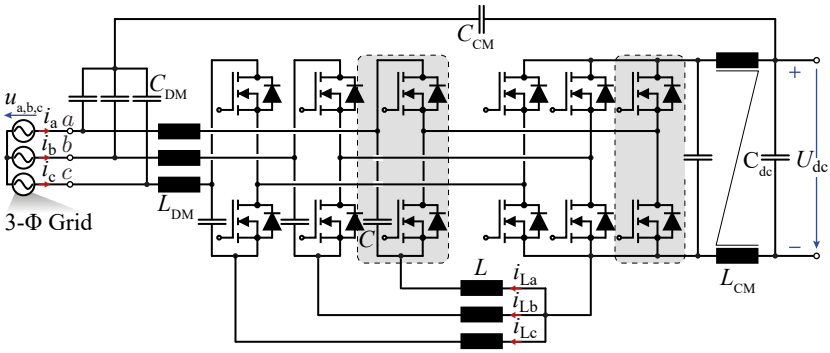

Fig. 4.6: Three-phase PFC rectifier application of the proposed novel Return-Path-Inductor Y-converter, i.e., RPI Y-Rectifier (RPI-YR). The power circuit depicted here includes a CM output filter with internal CM capacitor filter path as described in [126] ensuring a constant ground potential of the DC output voltage, which is crucial for series connected converter stages [157]. It is important to note that the CM inductor can be either located on the DC side (as shown) or on the AC side of the converter switching stage, i.e., connected in series to L_{DM}. A DC-side or AC-side CM inductor is also advantageous for motor drive applications as it largely attenuates conducted CM emissions of unshielded motors cables and motor bearing currents [150].

5

Wide DC Output Voltage Range 12-YR

This Chapter presents the modulation, component stresses, control considerations, as well as preliminary results of the hardware verification of a 12-YR.

Motivation

Single-stage buck-boost Power Factor Correction (PFC) rectifier systems allow to cover a wide DC output voltage range, which is crucial for applications such as Electric Vehicle (EV) battery chargers. This Chapter investigates component stresses, Electromagnetic Interference (EMI) filter design, as well as the modulation scheme, the control concept and the startup sequence of a Twelve-Switch Buck-Boost Y-Rectifier (12-YR).

Executive Summary

An increasing number of applications require three-phase Power Factor Correction (PFC) rectifier systems capable of generating DC output voltages both below and above the mains line-to-line voltage amplitude, i.e., with buck-boost capability. This Chapter investigates a quasi-single-stage Twelve-Switch Buck-Boost Y-Rectifier (12-YR) for operation in a 400 V_{rms} (line-to-line) mains and providing DC output voltages from 200 V to 750 V without the need for a subsequent DC/DC converter. Grid-tied operation of the 12-YR is not yet described in the literature and this Chapter presents a modulation strategy, and proposes a new *dq*-coordinate-based control structure with low computational burden. Further, a comprehensive analysis of the component stresses is conducted and a line-side EMI filter design is presented. Moreover, an experimental analysis is conducted with an existing 11 kW 12-YI power stage and preliminary results verify the converter startup as well as the operation in both buck and boost mode with a peak efficiency of 98.2 %.

5.1 Introduction

An increasing number of applications requires three-phase Power Factor Correction (PFC) rectifier front-ends capable of generating DC output voltages both below and above the mains peak line-to-line voltage, i.e., with buck-boost capability [47]. **Fig. 5.1** presents application examples, as well as the corresponding time domain terminal input voltage waveforms (within one mains period T_{ac}) with the considered DC voltage range $U_{dc} \in [U_{dc,min}, U_{dc,max}]$ highlighted.

Fig. 5.1a shows a Battery Electric Vehicle (BEV) charger with Power Factor Correction (PFC) rectifier front-end connected to a three-phase mains with a peak line-to-neutral voltage of $\hat{U}_{ac}$ =325 V_{pk} (i.e., 400 V_{rms} line-to-line voltage). In order to allow compatibility with various nominal battery voltage levels, a wide DC output voltage range is required [37–39], and **Fig. 5.1a** depicts $U_{dc} \in [200\,V, 750\,V]$, i.e., the voltage range prescribed by the *China Grid 2017 Electric Vehicle Charging Equipment Supplier Qualification Verification Standard* [37].

In order to provide galvanic isolation, the charger further comprises an isolated DC/DC converter stage. Ideally this DC/DC converter is realized as an ultra-efficient series resonant converter [36] (with limited output voltage controllability), and the DC output voltage is controlled solely by the rectifier

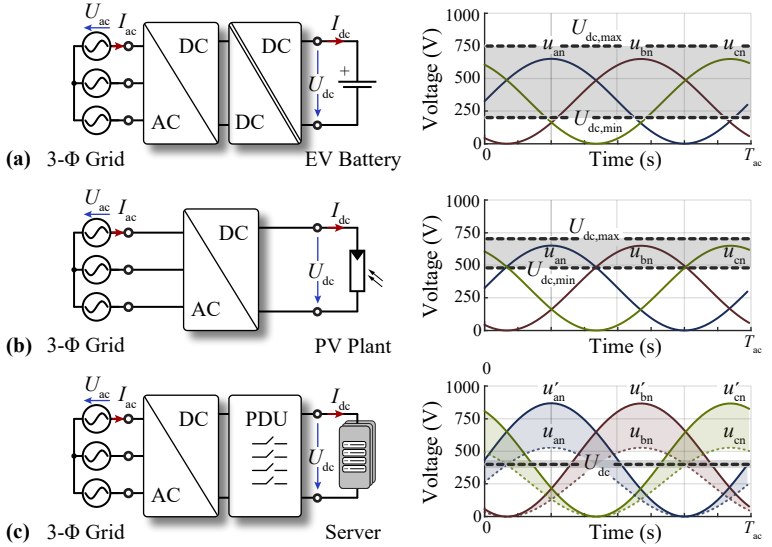

Fig. 5.1: Examples of three-phase Power Factor Correction (PFC) rectifier applications with wide input or output voltage ranges and the corresponding terminal voltage waveforms: **(a)** Electric Vehicle (EV) battery charger, **(b)** Photovoltaic (PV) inverter, and **(c)** server power supply ($U_{\mathrm{dc}} = 400\,\mathrm{V}$) compatible with a $480\,\mathrm{V_{rms}}$ and a $400\,\mathrm{V_{rms}}$ (line-to-line) three-phase mains (adapted from [46]).

front-end. Bidirectional BEV chargers further allow for V2G operation [40], where the power flow reverses and the BEV acts as grid storage element.

This corresponds then to a solar inverter feeding power into the three-phase mains as depicted in **Fig. 5.1b**. In this application, the DC input voltage U_{dc} under PV maximum power point tracking varies based on luminescence and ambient temperature [41–43] and **Fig. 5.1b** highlights $U_{\mathrm{dc}} \in [480\,\mathrm{V}, 700\,\mathrm{V}]$ according to [43].

As a last example, **Fig. 5.1c** depicts a data center power supply compatible with both the European $400\,\mathrm{V_{rms}}$ (line-to-line, i.e., $\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V_{pk}}$) and the US $480\,\mathrm{V_{rms}}$ (line-to-line, i.e., $\hat{U}_{\mathrm{ac}} = 390\,\mathrm{V_{pk}}$) three-phase mains which can further vary in amplitude within +20 %/-10 %. From this wide input voltage range (i.e., $\hat{U}_{\mathrm{ac}} \in [294\,\mathrm{V_{pk}}, 470\,\mathrm{V_{pk}}]$) a three-phase PFC rectifier front-end generates a constant DC-bus voltage $U_{\mathrm{dc}} = 400\,\mathrm{V}$ [45] and supplies the individual server racks via the Power Distribution Unit (PDU).

Phase-modular three-phase buck-boost converter systems [56, 59, 62, 63] allow to cover the input-output voltage ranges of the discussed application examples without the need for an additional DC/DC converter, hence enabling a simple, compact and highly efficient system realization. Within the scope of three-phase buck-boost inverter drive systems, the Twelve-Switch Buck-Boost Y-Inverter (12-YI) gained significant attention in literature [58, 64–67, 150]. Due to the bidirectional nature of the 12-YI, this topology is also applicable in rectifier applications, i.e., can operate as a Twelve-Switch Buck-Boost Y-Rectifier (12-YR) as depicted in **Fig. 5.2a**. Literature discusses several topologies related to the 12-YR, e.g., a 12-YR with additional unfolder bridge-legs [71], a 12-YR with a fourth converter module [74], a multi-level flying capacitor 12-YR [46], and a six-module 12-YR [158] aiming at nominal-power single-phase operation.

However, up to date no comprehensive analysis of a 12-YR including hardware results is available in literature and hence the topic of this chapter. Here the considered application specifications are given by a wide DC voltage range according to [37], i.e., $U_{\mathrm{dc}} \in [200\,\mathrm{V}, 750\,\mathrm{V}]$ covered from a f_{ac} =50 Hz three-phase mains with $\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V_{pk}}$ (i.e., $400\,\mathrm{V_{rms}}$ line-to-line voltage) as presented in **Fig. 5.2a**, where the experimental verification is conducted with an existing 11 kW 12-YI prototype.

This Chapter is organized as follows: **Sec. 5.2.1** summarizes the fundamental operating principle of a 12-YR module, and **Sec. 5.2.2** presents a new *dq*coordinate-based 12-YR control structure. **Sec. 5.2.3** and **Sec. 5.2.4** then discuss the worst-case component current stresses and the High-Frequency (HF) conducted Electromagnetic Interference (EMI) emissions on the grid side, respectively, as well as the implications of the selected DC output voltage and current range. Preliminary experimental results are presented in the subsequent sections, where **Sec. 5.3.1** highlights the relevant considerations for system startup and **Sec. 5.3.2** presents recorded converter waveforms in both buck and boost operation, as well as the corresponding efficiency curves. Finally, **Sec. 5.4** summarizes the findings of this work and presents an outlook on further research to be conducted in relation to the 12-YR.

5.2 12-YR Topology

It is important to highlight, that the fundamental 12-YR operating principle is mostly identical to the 12-YI (where the definition of buck and boost stage is reversed as discussed in **Sec. 1.2**), and summarized here for conciseness. The grid line-to-neutral terminal input voltages $u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}$ (with amplitude

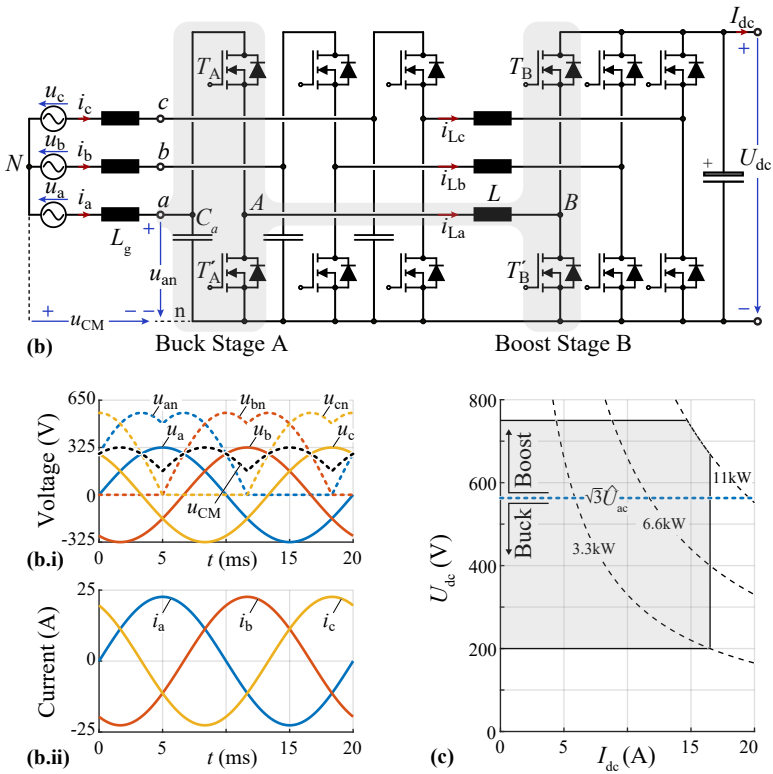

Fig. 5.2: (a) Main power circuit of a Twelve-Switch Buck-Boost Y-Rectifier (12-YR) converting a three-phase voltage (with line-to-neutral voltage amplitude $\hat{U}_{ac}$ =325 V_{pk}) into a DC output voltage which can be set to values both above and below the grid line-to-line voltage amplitude and is defined as $U_{dc} \in [200\,V, 750\,V]$. **(b.i)** AC input terminal voltage waveforms, i.e., the strictly positive input capacitor voltages u_{an}, u_{bn}, u_{cn} (measured against the negative DC-link rail n, i.e., comprising a CM offset u_{CM}), as well as the AC grid voltages u_a, u_b, u_c with respect to the starpoint N, and **(b.i)** sinusoidal AC phase currents i_a, i_b, i_c. **(c)** Considered DC output voltage U_{dc} and current I_{dc} range: The system power is limited for high DC output voltages by a 16 A_{rms} grid current limit corresponding to 11 kW, and for lower DC output voltages the DC output current is further limited to 16.6 A.

$\hat{U}_{ac}$=325 V_{pk}) are highlighted in **Fig. 5.2b.i**. There, the strictly positive input capacitor voltages u_{an}, u_{bn}, u_{cn} are shown in addition and comprise a time-varying CM offset voltage u_{CM} under Discontinuous PWM (DPWM) [58, 112] with

$$u_{CM}(t) = \frac{1}{3}(u_{an} + u_{bn} + u_{cn}) = -min(u_a, u_b, u_c), \tag{5.1}$$

i.e., such that the module input terminal with the instantaneously lowest grid input voltage connects to the negative DC-link rail, As there is no corresponding CM current path, the time varying CM voltage u_{CM} does not drive a current, and accordingly, sinusoidal grid currents in phase with the respective grid voltages can be realized as depicted in **Fig. 5.2b.ii** [56, 62, 63].

Fig. 5.2c presents the considered DC voltage U_{dc} and current I_{dc}: For high DC output voltage values the output power is limited to 11 kW by an AC grid current limit (16 A_{rms} for standard fuses), while for $U_{dc} \leq 665$ V the output power is further limited by a DC current limit $I_{dc} \leq 16.6$ A, such that the nominal power for e.g., U_{dc} =400 V is equal to 6.6 kW. The considered grid line-to-line voltage amplitude (i.e., $\sqrt{3}\hat{U}_{ac}$ =560 V_{pk}) is further highlighted by a dashed line in **Fig. 5.2c** and represents the boundary of buck and boost operation.

5.2.1 Modulation

As the three phase modules operate independently from each other, the modulation strategy is here only explained for the module *a* (highlighted in light grey in **Fig. 5.2a**). **Fig. 5.3** depicts the relevant voltage, current and control signals within one mains period for U_{dc} = 400 V and a three-phase input power P_{ac} = 6.6 kW. Module *a* operates as a quasi-single-stage [68–70] converter, i.e., based on the instantaneous input-output voltage ratio (cf., **Fig. 5.3a**), only the buck or boost half-bridge is HF switched with PWM:

In **buck operation** (i.e., $u_{an} \geq U_{dc}$) the boost high-side transistor T_B is permanently on (thereby connecting the node *B* to the positive DC-link rail). The buck half-bridge steps down the high (instantaneous) input capacitor voltage u_{an}, and $u_A \in [0, u_{an}]$ denotes the buck half-bridge switch-node voltage.

In **boost operation** (i.e., $u_{an} < U_{dc}$) the buck high-side transistor T_A is permanently on (thereby connecting the node *A* to the module input terminal *a*). The boost half-bridge now steps up the low (instantaneous) input capacitor voltage u_{an}, and $u_B \in [0, U_{dc}]$ denotes the boost half-bridge switch-node voltage. Note that with the considered DPWM operation, there is a 120° interval with u_{an} = 0 V where consequently T_A and T'_B are permanently on

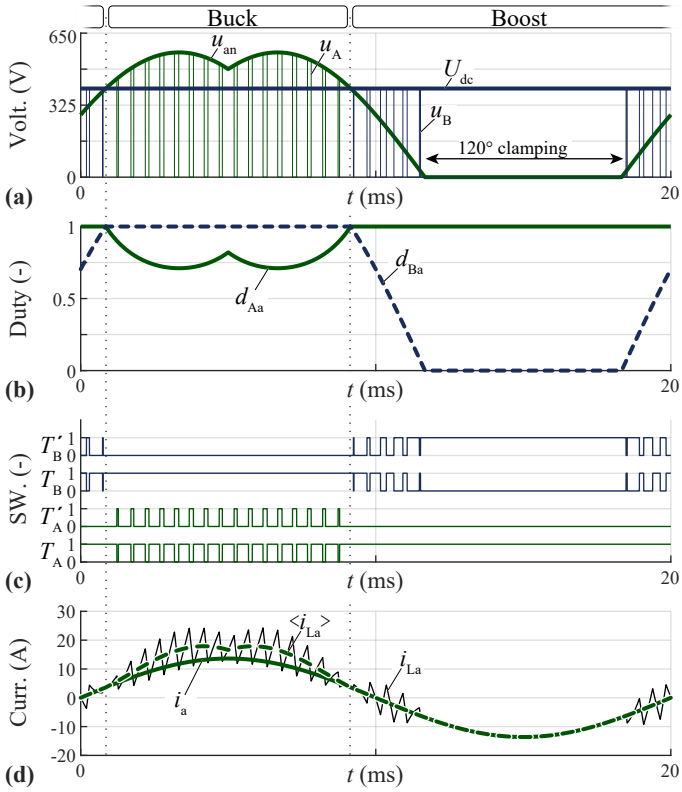

Fig. 5.3: Main Twelve-Switch Buck-Boost Y-Rectifier (12-YR) voltage and current waveforms of module a for $\hat{U}_{ac}$ =325 V_{pk} and U_{dc} = 400 V, i.e., an operating point with both buck *and* boost operation in sections of a mains period: **(a)** input capacitor voltage u_{an} and DC-link voltage U_{dc}, as well as the buck and boost switch-node voltages with respect to the negative DC-link rail u_A and u_B, respectively, **(b)** duty cycles of the buck stage d_{Aa} and the boost stage d_{Ba}, **(c)** corresponding semiconductor PWM switching signals, and **(e)** sinusoidal AC input current i_a, as well as the buck-boost inductor current i_{La} comprising a HF ripple on top of the local average value (within one switching cycle) $\langle i_{La} \rangle$. Note, that an extremely low pulse number has been selected here for illustration purposes.

(thereby connecting the node B to the negative DC-link rail) and therefore the module generates no switching losses during this interval.

The duty cycles of buck and boost half-bridges enabling the quasi-single-stage operation of the module are presented in **Fig. 5.3b** and are defined as

$$\begin{aligned} d_{\mathrm{Aa}}(t) &= \min(1, U_{\mathrm{dc}}/u_{\mathrm{an}}(t)), \\ d_{\mathrm{Ba}}(t) &= \min(1, u_{\mathrm{an}}(t)/U_{\mathrm{dc}}). \end{aligned} \tag{5.2}$$

Fig. 5.3c further depicts the control signals of the individual power semiconductors. **Fig. 5.3d** presents the main module current waveforms, i.e., the grid input current i_{a}, as well as the inductor current i_{La} and its local-average (over one switching period) value $\langle i_{\mathrm{L}} \rangle$ which is elevated in buck operation (compared to i_{a}) and defined by

$$\langle i_{\mathrm{La}} \rangle = i_{\mathrm{a}}/d_{\mathrm{A}}. \tag{5.3}$$

Last, the inductor peak HF current ripple depends on the instantaneous input-output voltage ratio (as well as the buck-boost inductor value L and the switching frequency f_{s}) and is given by

$$\Delta I_{\mathrm{L,pk}} = \begin{cases} \frac{1}{2} \frac{d_{\mathrm{Ba}}(1-d_{\mathrm{Ba}})U_{\mathrm{dc}}}{f_{\mathrm{s}}L} & \text{(Boost)} \\ \frac{1}{2} \frac{d_{\mathrm{Aa}}(1-d_{\mathrm{Aa}})u_{\mathrm{an}}}{f_{\mathrm{s}}L} & \text{(Buck)}\,. \end{cases} \tag{5.4}$$

5.2.2 Control

The grid current control of a 12-YR requires special consideration, especially for high switching frequencies resulting in a limited computation time on a Digital Signal Processor (DSP). In order to avoid many cascaded controller stages, it is proposed in [158] to control the grid currents only indirectly via the buck-boost inductor current. A similar approach is selected here, where the buck-boost inductor currents are further controlled in a dq-coordinate frame [159] to avoid unintended interactions between the phase modules and to assure proper operation under DPWM where always one of the three modules shows no HF switching operation at a given point in time.

The cascaded PFC rectifier control structure in **Fig. 5.4** comprises an outer (slow) DC-link voltage controller, which defines a grid power reference P^*_{ac} based on the difference between the DC-link voltage reference U^*_{dc} and the measured value U_{dc}. Simultaneously, a Phase-Locked Loop (PLL) calculates both the instantaneous grid angle $\varphi = 2\pi f_{\mathrm{ac}} t$, as well as the grid voltage

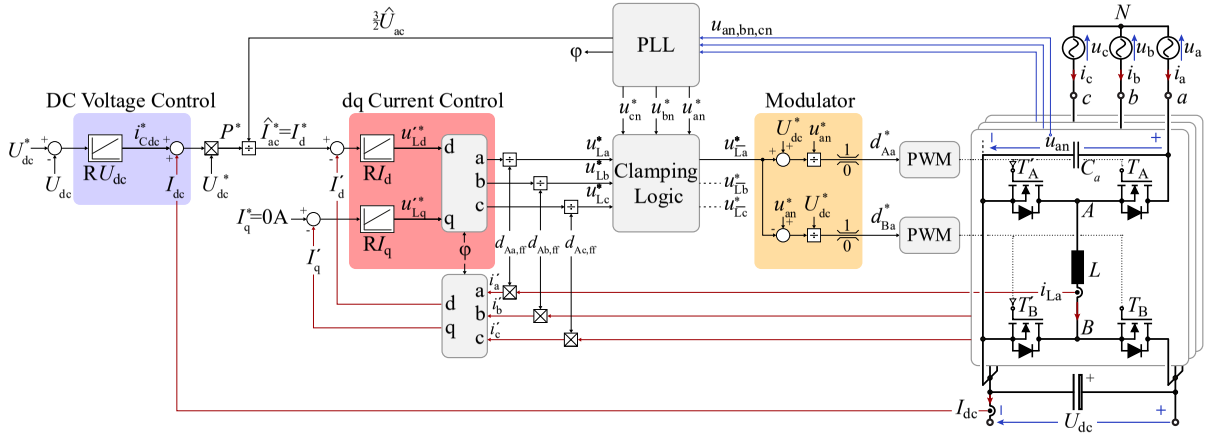

Fig. 5.4: Cascaded 12-YR DC output voltage control scheme for quasi-single-stage PFC operation in buck and boost mode including the relevant control and measurement signals. Note that the feed-forward duty cycles $d_{\mathrm{Aa,ff}}, d_{\mathrm{Ab,ff}}, d_{\mathrm{Ac,ff}}$ are calculated with (5.2) and using the input capacitor voltage waveforms $u^*_{\mathrm{an}}, u^*_{\mathrm{bn}}, u^*_{\mathrm{cn}}$ (from the Phase-Locked Loop (PLL)) as well as the DC-link voltage reference U^*_{dc}.

amplitude $\hat{U}_{\mathrm{ac}}$. The latter can be used to translate P^*_{ac} into a corresponding peak AC current reference $I^*_{\mathrm{ac}} = \frac{P^*_{\mathrm{ac}}}{3/2\hat{U}_{\mathrm{ac}}}$ which (when aiming at unity power factor operation) immediately represents the d-current reference $I^*_{\mathrm{d}} = I^*_{\mathrm{ac}}$ (and $I^*_{\mathrm{q}} = 0$).

Note that the sampled buck-boost inductor currents (i.e., the LF currents $\langle i_{\mathrm{La}}\rangle$, $\langle i_{\mathrm{Lb}}\rangle$, $\langle i_{\mathrm{Lc}}\rangle$) are not purely sinusoidal (cf., **Fig. 5.3d**), and accordingly a transformation from *abc* to *dq* coordinates is not meaningful. It is proposed here to multiply the measured inductor currents with the respective buck stage feed-forward duty cycles $d_{\mathrm{Aa,ff}}, d_{\mathrm{Ab,ff}}, d_{\mathrm{Ac,ff}}$ (calculated from (5.2)), resulting in (ideally) symmetric three-phase currents $i'_{\mathrm{a}}, i'_{\mathrm{b}}, i'_{\mathrm{c}}$, which in turn can be translated into corresponding dq currents $I'_{\mathrm{d}}, I'_{\mathrm{q}}$. In order to avoid unintended noise or ringing in the feed-forward duty cycles $d_{\mathrm{Aa,ff}}, d_{\mathrm{Ab,ff}}, d_{\mathrm{Ac,ff}}$ they are calculated with (5.2) and using the input capacitor voltage waveforms $u^*_{\mathrm{an}}, u^*_{\mathrm{bn}}, u^*_{\mathrm{cn}}$ (from the PLL) as well as the DC-link voltage reference U^*_{dc}.

The dq current controller tracks I'_{d} and I'_{q} and outputs the buck-boost inductor voltage references $u'^*_{\mathrm{Ld}}, u'^*_{\mathrm{Lq}}$ which are then transformed back into *abc* coordinates and scaled by the respective inverse values of $d_{\mathrm{Aa,ff}}, d_{\mathrm{Ab,ff}}, d_{\mathrm{Ac,ff}}$.

Subsequently, the DPWM clamping logic identifies the phase module with the lowest boost stage switch-node reference value i.e.,

$$\langle u^*_{\mathrm{Bx}}\rangle = u^*_{\mathrm{xn}} - u^*_{\mathrm{Lx}}, \quad x \in a, b, c. \tag{5.5}$$

The inductor voltage reference of the phase to be clamped u^*_{Lx} is subtracted from each inductor voltage reference value yielding the final inductor voltage references $u^*_{\mathrm{La}}, u^*_{\mathrm{Lb}}, u^*_{\mathrm{Lc}}$ which are fed into the 12-YR modulator [58] (only shown for module *a*). There, based on the instantaneous input-output voltage ratio and the inductor voltage reference u^*_{La} the duty cycles for mutually exclusive operation of buck and boost stage, i.e., d^*_{Aa} and d^*_{Ba}, are set and switching signals are generated using standard PWM blocks.

5.2.3 Component Stresses

It is interesting to also analyze the LF current stresses of the main 12-YR power components (which take major impact on the component selection [156]), which do not depend on the selected converter design parameters (e.g., inductance value and switching frequency), but are defined solely by the considered operating range and the modulation strategy (i.e., here DPWM).

Fig. 5.5a.i and **a.ii** represent the global RMS I_{L} and peak value $\hat{I}_{\mathrm{L}}$ of the LF buck-boost inductor $\langle i_{\mathrm{La}}\rangle$, respectively, and the red dashed lines represent

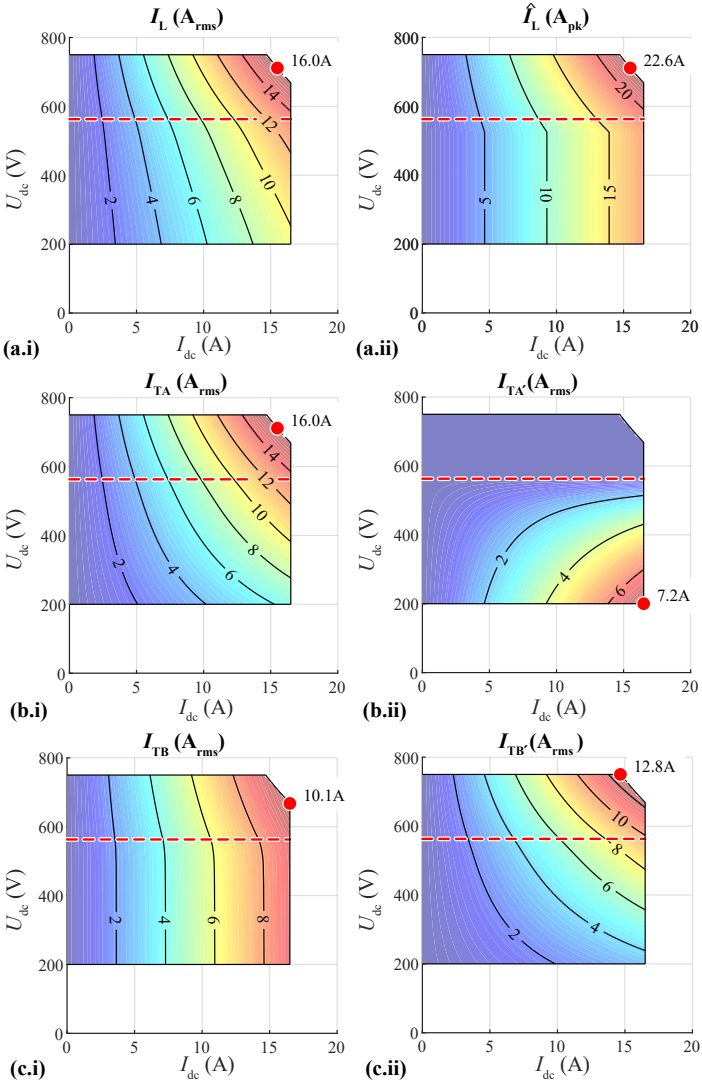

Fig. 5.5: 12-YR main power component current stresses for a three-phase mains with $\hat{U}_{ac}$ =325 V_{pk} (line-to-neutral) and operation with DPWM over DC output current I_{dc} and voltage U_{dc}: **(a.i)** LF RMS and **(a.ii)** LF peak current value of the buck-boost inductor, **(b)** buck stage and **(c)** boost stage semiconductor LF RMS current stresses. The red dashed lines represent the grid peak line-to-line voltage (i.e., 560 V_{pk}) and indicate the limit of buck and boost operation.

the grid peak line-to-line voltage (i.e., 560 V_{pk}) indicating the limits of buck and boost operation. In boost operation I_L and $\hat{I}_L$ are equal to the grid current RMS value (cf., **Fig. 5.3d**), and hence linearly depend on the input power level. In contrast, in buck operation the buck-boost inductor current stresses are elevated compared to the grid current (5.3), and (for a given input power level) increase with increasing step-down effort.

It is important to highlight, that the maximum current stresses of I_L =16 A_{rms} and $\hat{I}_L$ =22.6 A_{pk} occur in boost operation. The considered operating range (with a maximum DC current limiting the input power for $U_{dc} \leq 665$ V) is therefore highly beneficial for a phase-modular 12-YR, as the maximum inductor current stresses are identical to a standard boost-type Six-Switch Voltage Source PFC Rectifier (6-VSR) front-end [47] (which then requires an additional buck DC/DC converter to cover the considered DC output voltage range in **Fig. 5.2c**).

The power semiconductor LF RMS current stresses can be derived from $\langle i_L \rangle$ and the corresponding buck d_A and boost duty cycle d_B waveforms [67] and are depicted in **Fig. 5.5b-c**. Note that the current stresses of high-side and low-side devices are not identical: In the buck stage this is especially accentuated in boost operation, where the high-side semiconductor T_A is permanently on and conducts the grid current (resulting in high current stresses up to I_{TA} =16.0 A_{rms} equal to the grid RMS current limit), while $I_{TA'} = 0$ (the worst case value $I_{TA'}$ =7.2 A_{rms} results then for the maximum step down operating point). It is important to recapitulate, that the buck stage A is not operated with PWM in the boost operating region (and hence does not incur any switching losses), which makes the elevated conduction stresses of T_A tolerable.

In contrast, the worst-case current stresses of the boost stage semiconductors are distributed more evenly across high-side and low-side semiconductors, where the small discrepancy is the result of the selected DPWM operation, causing slightly elevated worst-case conduction stresses in the low-side semiconductor $I_{TB'}$ =12.8 A_{rms} (compared to I_{TB} =10.1 A_{rms}). Again, the stresses I_{TB} and $I_{TB'}$ deviate more clearly for operating points with high step-down effort, where T_B clamps to the positive DC-link rail when the buck stage is operated with PWM.

5.2.4 EMI Filter Design

Grid-connected rectifier systems have to comply with stringent EMI regulations, where the CISPR 11 Class A conducted emission limits from 150 kHz to

30 MHz are considered here. The 12-YR modules show a hybrid voltage-source and current-source EMI behaviour in boost and buck operation, respectively, which hence depends on the instantaneous input-output voltage ratio [150].

According to [46, 150], the HF content $i_{\mathrm{TA,HF}}$ of the buck stage high-side switch current i_{TA} represents the relevant quantity to asses the EMI emissions. This becomes obvious from **Fig. 5.6a** displaying the modular representation of the 12-YR connected to a Line Impedance Stabilization Network (LISN) recording the EMI emissions. Note, that here the input capacitor C_{a} (cf., **Fig. 5.2a**) is not shown, as it can be considered as part of the EMI filter structure. In absence of the EMI filter, $i_{\mathrm{TA,HF}}$ returns via the LISN (and the other two phases), thereby causing a resistive voltage drop u_{LISN} which is regulated by the EMI emission limit.

The HF current $i_{\mathrm{TA,HF}}$ is of triangular shape in boost operation and of approximately rectangular shape (i.e., switched) in buck operation. Accordingly, the maximum HF local RMS current $I_{\mathrm{TA,HF}}$ over one switching period of $i_{\mathrm{TA,HF}}$ for a given operating point with unity power factor operation can be approximated with [46]

$$I_{\mathrm{TA,HF}} = \begin{cases} \frac{1}{\sqrt{3}} \cdot \Delta I_{\mathrm{L,pk}} = \frac{1}{\sqrt{3}} \frac{1}{8} \frac{U_{\mathrm{dc}}}{f_{\mathrm{s}} L} & \text{(Boost)} \\ \hat{I}_{\mathrm{ac}} \sqrt{1/d_{\mathrm{A,min}} - 1} & \text{(Buck)} \end{cases}, \tag{5.6}$$

with L indicating the inductance of the buck-boost inductor, f_{s} the power stage switching frequency, and $d_{\mathrm{A,min}}$ the minimum buck stage duty cycle within one mains period.

Fig. 5.6b presents $I_{\mathrm{TA,HF}}$ over the considered DC output voltage and current range for the power stage specifications of the hardware prototype, i.e., f_{s} =100 kHz and L =85 µH. The red dashed line represents again the boundary of buck and boost operation, where the HF conducted noise emissions in boost mode are solely defined by the maximally occurring inductor current ripple $\Delta I_{\mathrm{L,pk}}$ (5.4) and hence power independent. In contrast, in buck operation the HF emissions scale both with the input current I_{ac} (i.e., linearly with input power) and the step-down ratio.

Note that with f_{s} =100 kHz (<150 kHz), the first (switching frequency) harmonic component $\hat{i}_{\mathrm{TA}}(n = 1)$ of i_{TA} is not of regulatory relevance, such that the required filter attenuation is derived based on the second harmonic component $\hat{i}_{\mathrm{TA}}(n = 2)$ of the design frequency $f_{\mathrm{D}} = 2f_{\mathrm{s}}$ =200 kHz [134]. The spectrum of i_{TA} can be approximated with [46]

$$\hat{i}_{\mathrm{TA}}(n \cdot f_{\mathrm{s}}) = \frac{I_{\mathrm{TA,HF}}}{n^k}, \tag{5.7}$$

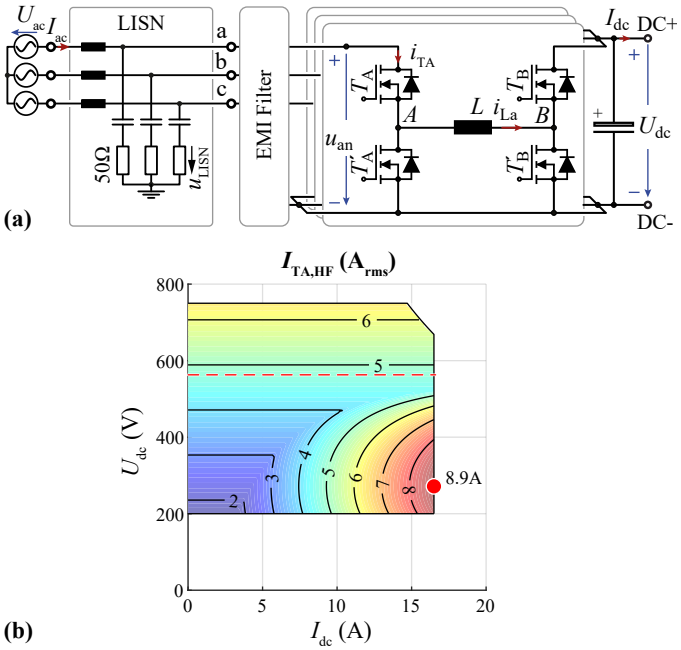

Fig. 5.6: (a) Modular representation of the 12-YR connected to a Line Impedance Stabilization Network (LISN) recording the Electromagnetic Interference (EMI) emissions. Note, that the input capacitor C_a (cf., **Fig. 5.2a**) is not shown here, as it can be considered as part of the EMI filter structure. **(b)** HF RMS current $I_{TA,HF}$ of the buck stage high-side switch T_A according to (5.6) which is the relevant quantity for the EMI filter design. The red dashed line represents the grid peak line-to-line voltage and indicates the limit of buck and boost operation.

where $k = 1$ in buck (rectangular current decaying with $1/f$) and $k = 2$ in boost operation (triangular current decaying with $1/f^2$) [134].

The worst-case emissions result to $I_{\mathrm{TA,HF}}$ =8.9 $\mathrm{A_{rms}}$≈139 dBµA occurring in buck operation (cf., **Fig. 5.6b**). Hence, the maximum emissions at the design frequency result according to (5.7) to $\hat{i}_{\mathrm{TA}}(2 \cdot f_{\mathrm{s}})$ =4.4 $\mathrm{A_{rms}}$≈133 dBµA with $k = 1$. In combination with the 50 Ω (i.e., 34 dBΩ) LISN resistor, this current corresponds to a voltage level of 133 dBµA + 34 dBΩ = 167 dBµV which is substantially above the CISPR 11 Class A conducted emission limits of 79 dBµV at f_{D} =200 kHz. Hence, in order to assure compliance (with an additional margin of 10 dB to account for e.g., component tolerances and saturation [134]), an EMI filter providing an attenuation of

$$A_{\mathrm{EMI}} = (79\,\mathrm{dB\mu V} - 10\,\mathrm{dB}) - (133\,\mathrm{dB\mu A} + 34\,\mathrm{dB\Omega}) = -98\,\mathrm{dB}, \qquad (5.8)$$

is required, corresponding to an attenuation of approximately 5 orders of magnitude.

Fig. 5.7 depicts the main power stage of the 12-YR (based on the existing 12-YI prototype from [150]), as well as the considered EMI filter structure and component values. Details on the component realization are provided in **Tab. 5.1**. The line-side EMI filter is located on two external Printed Circuit Boards (PCBs), such that the 12-YR prototype (including the EMI filter boards) shows a power density of 12 $\mathrm{kW/dm^3}$.

The filter design is conducted according to [150]: Ultra-compact non-linear *X7R* capacitors are employed in the main power stage (equally referenced to the positive and negative DC-link rail to minimize the capacitance variation within one mains period [138]), which attenuate both DM and CM currents. A first filter stage (L_{f1}, C_{f1}) employs *X2* safety rated capacitors referenced to the negative DC-link rail forming a second combined DM and CM filter. The second filter stage is realized as separate DM (L_{f2}, C_{f2} (with *X2* rating)) and CM filter (L_{CM}, C_{CM} (with *Y2* rating)) to also attenuate emissions caused by the switch-node capacitances [150], where the total CM capacitance to PE is limited to 44 nF due to a 3.5 $\mathrm{mA_{rms}}$ ground current limit [136].

5.3 Experimental Verification

This section presents results of first experiments conducted with the 12-YR hardware prototype (details see **Fig. 5.7** and **Tab. 5.1**). The converter is supplied from a three-phase AC source ($\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V}$) and a resistive load is connected on the DC output side.

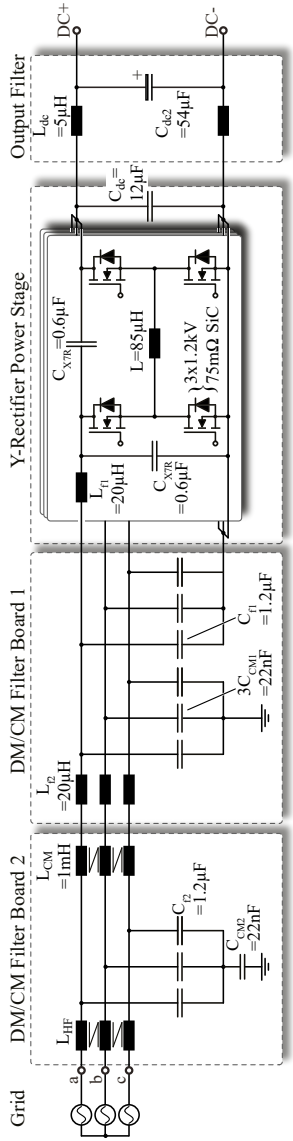

Fig. 5.7: Main power circuit of the 12-YR prototype including the line-side EMI filter.

Tab. 5.1: 12-YR power stage and EMI filter component details (designators refer to **Fig. 5.7**).

Component	Nom. value	Details
Semiconductors	$f_s = 100\,\text{kHz}$	3 x Cree SiC C3M0075120J 75 mΩ 1.2 kV,
Inductors	$L = 85\,\mu\text{H}$	2 x TDK EELP 43 Ferrite Core (N97), 5.4 mm air gap, 20 turns of 625 x 71 µm litz wire
	$L_{\text{fl},2}20\,\mu\text{H}$	2 x Würth WE-HCI 10 µH, 21 A, 3.4 mΩ
	$L_{\text{CM}} = 1\,\text{mH}$	(at 200 kHz) VAC T60006-L2030-W423 (VITROPERM 500 F), 10 turns of 1.4 mm solid wire
	$L_{\text{HF}} = 15\,\mu\text{H}$	(at 200 kHz) VAC T60006-L2030-W514 (VITROPERM 500 F), plug-on core
	$L_{\text{dc}} = 4.7\,\mu\text{H}$	1 x Vishay IHLP6767DZER4R7M01 4.7 µH, 27 A, 11.2 mΩ
Capacitors	$C_{\text{dc}} = 12\,\mu\text{F}$	48 x TDK Ceralink 0.25 µF, 900 V
	$C_{\text{dc2}} = 48\,\mu\text{F}$	12 x Chemi-Con ALUM 18 µF, 450 V (series connection of 2x 6 parallel devices)
	$C_{\text{X7R}} = 1.3\,\mu\text{F}^a$	6 x Syfer X7R, 0.47 µF, 1 kV referenced evenly to positive and negative DC-link rails
	$C_{\text{f2}} = 1.3\,\mu\text{F}$	1x Würth X2 WCAP-FTXX 890334026020CS, 0.68 µF, 310 V
		1x Würth X2 WCAP-FTXX 890334026014, 0.47 µF, 310 V
	$C_{\text{CM1,2}} = 7\,\text{nF}$	1 x Johanson-Dielectrics Y2 safety certified MLCC, X7R 4.7 nF, 250 V
		1 x Johanson-Dielectrics Y2 safety certified MLCC, X7R 2.2 nF, 250 V
Controller	150 MHz	TMS320C2834X

[a] Minimum value for the considered operating range and modulation according to **Fig. 5.2**.

First, **Sec. 5.3.1** discusses the converter behaviour when connecting to the grid and describes the subsequent startup-sequence. Then, **Sec. 5.3.2** presents recorded waveforms in both buck and boost operation, as well as the corresponding efficiency curves.

5.3.1 Startup

The 12-YR is connected to the grid with 250 Ω pre-charge resistors to avoid high current spikes in the input filter capacitors. Note that these resistors are not included in the prototype (originally intended for inverter applications) and hence located externally. **Fig. 5.8a** presents the 12-YR input buck stage when connecting to the grid (with all devices in off state) and **Fig. 5.8b** shows the three input capacitor voltages (which are all at zero voltage initially), as well as the CM voltage recorded during the filter pre-charge process.

It is important to highlight, that the grid impresses the line-to-line voltages (and therefore the input capacitor DM voltages), but not directly the CM voltage. At the same time, the body diodes of the buck stage half-bridge semiconductors T_A and T'_A prevent negative input capacitor voltages. Accordingly, the buck half-bridge diodes of the phase with the instantaneously most negative AC input voltage (i.e., $u_\mathrm{b} < u_\mathrm{a}, u_\mathrm{c}$ in **Fig. 5.8a,b**) clamp the respective input terminal to the negative DC-link rail, thereby defining the CM voltage between the grid starpoint N and the negative DC-link rail n (here $u_\mathrm{CM} = -u_\mathrm{b}$). Hence, an increasing voltage u_CM is established up to the point, where the minimum constant offset voltage $u_\mathrm{CM} = \hat{U}_\mathrm{ac}$ is reached, and no diode conduction takes place any more. As there is no DC CM current path, this offset voltage sustains up to the point, where the CM voltage is controlled actively.

Fig. 5.8c presents the transition to active control with DPWM, which can be initiated after precharge and once the PLL is synchronized to the grid angle φ. Advantageously, active control is started when $u^*_\mathrm{CM} \approx \hat{U}_\mathrm{ac}$ (which occurs every 120° of the mains period) in order to avoid a sudden jump in CM voltage potentially followed by ringing and high current amplitudes. With the DC-link voltage in the close vicinity of zero volts during the startup, the feed-forward term of the buck stage duty cycles d^*_A (5.2) (cf., **Fig. 5.4)** reaches extremely low values during startup, such that the measured inductor currents are multiplied (and divided) by extremely high scaling factors in the controller structure. Hence, to avoid undesired behaviour, the values of d^*_A and $1/d^*_\mathrm{A}$ are limited to 10 and 1/10, respectively.

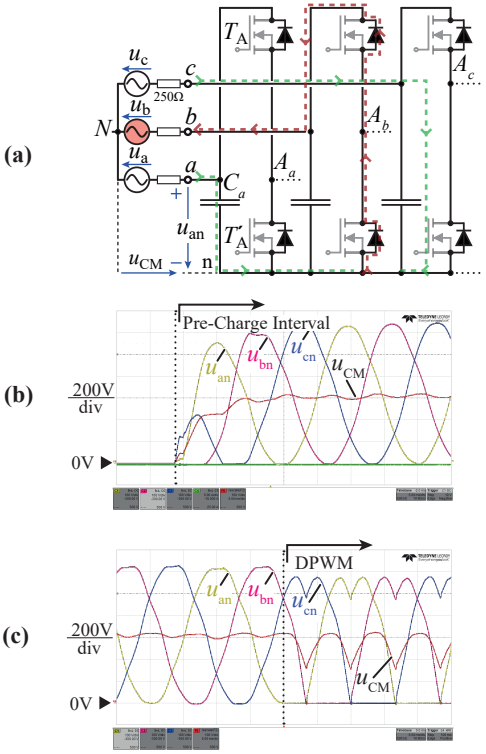

Fig. 5.8: (a) 12-YR input buck stage when connecting to the grid (with all power transistors in off state), and $u_b < u_a, u_c$ such that $u_{CM} = -u_b$. **(b)** Experimental input capacitor voltage waveforms u_{an}, u_{bn}, u_{cn} (as well as the CM voltage component calculated on an oscilloscope math channel) for connection to the three-phase mains (with line-to-neutral voltage $\hat{U}_{ac}$ =325 V_{pk}) with 250 Ω pre-charge resistors to limit the inrush currents, and **(c)** start of the CM control where the phase terminal with the instantaneously lowest input AC voltage is clamped to the negative DC-link rail (i.e., by permanently turning on the respective semiconductors T_A and T'_B, cf., **Fig. 5.3a**).

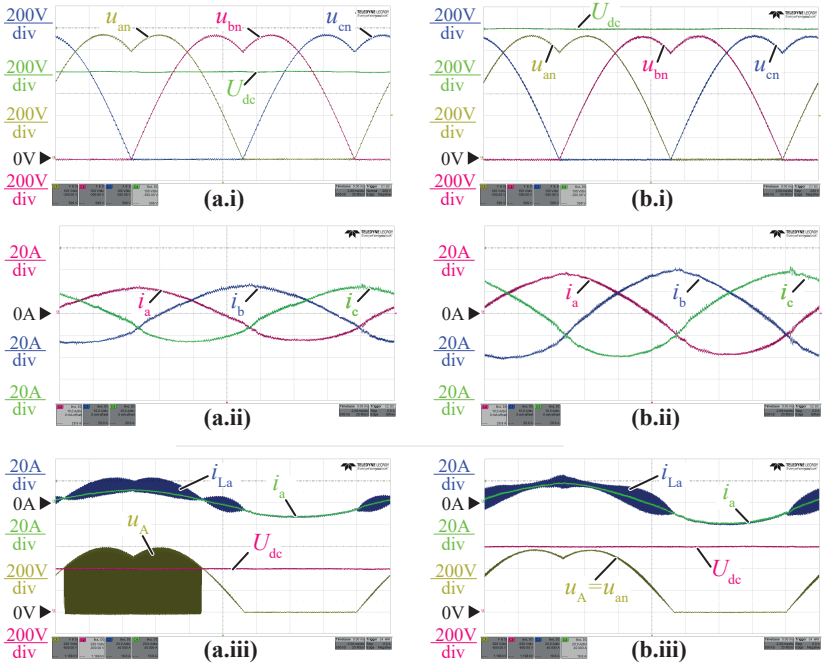

Fig. 5.9: Experimental waveforms recorded for **(a)** buck operation with U_{dc} =400 V and **(b)** boost operation with U_{dc} =600 V with an output power level of 6 kW and 9 kW, respectively. **(x.i)** presents the three input capacitor voltages u_{an}, u_{bn}, u_{cn} as well as the DC-link voltage U_{dc}, **(x.ii)** highlights the sinusoidal input currents i_a,i_b,i_c, and **(x.iii)** shows the module *a* phase current i_a and buck-boost inductor current i_{La}, as well as the DC-link voltage U_{dc} and buck stage switch-node voltage u_A.

5.3.2 Performance

The main 12-YR converter waveforms within one mains period of 20 ms for nominal power operation in a $\hat{U}_{ac}$ =325 V_{pk} three-phase mains with U_{dc} =400 V (i.e., buck operation) and U_{dc} =600 V (i.e., boost operation) are presented in **Figs. 5.9a** and **b**, respectively.

Figs. 5.9a.i and **a.ii** show the terminal voltage waveforms, i.e., the input capacitor voltages u_{an}, u_{bn}, u_{cn} with the characteristic DPWM shape, as well as the DC-link voltage U_{dc}. The three sinusoidal grid input currents are presented in **Figs. 5.9a.ii** and **b.ii** and show a high power factor > 99 % and THD < 5 %.

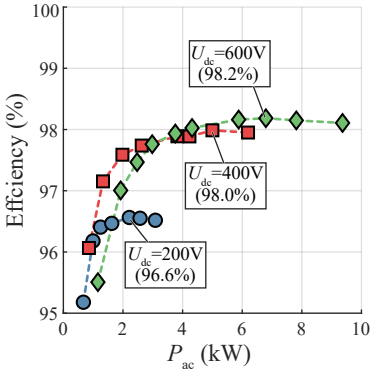

Fig. 5.10: 12-YR prototype efficiency over AC input power P_{ac} for several DC output voltage levels. Auxiliary systems were supplied by a 5 V (2 W for the DSP and sensors / logic devices) and a 12 V (8 W for the fans and the isolated gate drive supplies) DC supply, and the corresponding losses were added manually to calculate the displayed efficiency curves.

However, a small distortion can be identified visually, and could be eventually further reduced by means of a more elaborate dead time compensation.

The main waveforms of module *a* are further highlighted in **Figs. 5.9c.i** and **c.ii**, where in both cases the DPWM operation results in no switching actions (and hence also no inductor current ripple $\Delta I_{L,pk}$) during 1/3 of the mains period. The buck stage switch-node voltage u_A is interesting to observe as it contains switched PWM voltages in buck mode, and is otherwise clamped to the continuous input capacitor potential. It can also be noted, that the inductor current low-frequency value $\langle i_{La} \rangle$ is elevated compared to the input current i_a in buck mode, while the two are (apart from the HF ripple) identical in boost mode.

Last, **Fig. 5.10** presents the efficiency curves over input power recorded with a Yokogawa WT1804E power analyzer. It can be observed, that the lowest nominal efficiency results with U_{dc}=200 V which is due to the low output power level (i.e., auxiliary losses with increased relative impact), as well as the high component stresses in buck operation (cf., **Fig. 5.3d**). The efficiency improves substantially for higher output voltage (and power) levels where a peak efficiency of 98.2 % is reported.

5.4 Conclusions

Due to the bidirectional module structure, a Twelve-Switch Buck-Boost Y-Inverter (12-YI) can also be employed for wide DC output voltage range three-phase PFC rectifier applications, i.e., as a Twelve-Switch Buck-Boost Y-Rectifier (12-YR), which is not yet comprehensively described in literature. This work describes the basic operating principle and a new *dq*-coordinate-based PFC control structure with low computational burden. Further, the main power component stresses and the EMI emission level are analyzed, the implications of the operating range are discussed, and an EMI filter design is presented. Preliminary experimental results with an 11 kW 12-YR prototype verify the converter startup process, as well as operation in buck and boost condition. The prototype system shows a power density of 12 kW/dm^3 and recorded efficiencies of up to 98.2 %.

In the course of further experiments the converter will be tested up to the nominal DC output voltage of 750 V (and maximum output power of 11 kW), the EMI filter design and compliance with the CISPR 11 Class A conducted emission limits will be verified.

6 Conclusions and Outlook

Bidirectional phase-modular three-phase buck-boost converters find application in a wide range of applications: They are key components of both EV drivetrains and the corresponding battery chargers, as well as solar inverters and wind power plants, and enable substantial efficiency gains in industrial drives and future server power supplies. Accordingly, such converter systems represent a vital technology for the global energy transition. In the following section, existing research gaps are recapitulated and the corresponding key contributions of this thesis in the field of bidirectional phase-modular three-phase buck-boost converters are compiled.

6.1 Summary

An ultra-compact Twelve-Switch Buck-Boost Y-Inverter (12-YI) industrial Variable Speed Drive (VSD) with unshielded motor and supply cables is the subject of **Chapter 2**: Unshielded cables are more flexible, lightweight and cheaper compared to their shielded counterparts, but the IEC 61800-3 dictates stringent conducted and radiated Electromagnetic Interference (EMI) emission limits on unshielded power interfaces. This Chapter closes two gaps in the research literature: First, no comprehensive filter design guidelines including conducted and radiated EMI emissions for VSDs with unshielded cables are available in publications. Second, the hybrid voltage- and current-source 12-YI EMI emission mechanisms require special attention and are not yet covered in literature. Accordingly, a 12-YI EMI equivalent circuit is derived, and used to present comprehensive filter design guidelines for both conducted and radiated EMI emissions. Experimental measurements indicate full compliance for operation with unshielded DC and AC cables according

to the IEC 61800-3, where the 11 kW 12-YI prototype system features a power density of 12 kW/dm^3, hence, demonstrating the potential of this topology in future ultra-compact VSDs.

Chapter 3 studies harmonic injection modulation techniques for a low-component count Six-Switch Buck-Boost Y-Inverter (6-YI) auxiliary VSD system. The main drawback of the 6-YI is given by the high component stresses which results in limited converter efficiency and power density performance metrics. Accordingly, this Chapter proposes two harmonic injection schemes for the 6-YI. These new modulation techniques improve both conduction (through reduced low- and high-frequency currents) and switching losses (through reduced blocking voltages and/or reduced number of switching transitions within one fundamental AC period). The advantages of the novel modulation strategies are validated on a 1 kW hardware prototype, where loss reductions of up to 31 % (relative to conventional modulation) at nominal power are demonstrated, such that the 6-YI complies with an auxiliary motor drive efficiency target of 95 % efficiency, although the converter performance remains limited compared to a 12-YI. Therefore, with the efficiency improvements enabled by proposed advanced modulation strategies, the 6-YI remains an interesting topology candidate, where the selection of a suitable module structure for a phase-modular buck-boost inverter system depends on the particular application requirements concerning complexity, efficiency, size, and cost.

In **Chapter 4** a novel topology, denoted Return-Path-Inductor Twelve-Switch Buck-Boost Y-Inverter (RPI-12-YI) is presented. The buck-boost inductors of phase-modular buck-boost three-phase DC/AC converters are subject to large current stresses and therefore cover a substantial fraction of the overall converter volume, which in consequence limits the maximally achievable system power density. Accordingly, this Chapter investigates a new converter module structure, where the buck-boost inductors are shifted into the modules' current return paths, reducing the LF current stresses by up to 90 % (corresponding to an 80 % smaller magnetics volume) compared to a 12-YI for a typical operating range. The basic operating principle, component stress metrics as well as a potential control strategy for the RPI-12-YI are presented. Experimental waveforms in buck and boost operation of a 3.3 kW RPI-12-YI prototype system verify the practical feasibility of the proposed topology.

Given the bidirectional module structure, a 12-YI can also be employed in three-phase rectifier applications, i.e., as a Twelve-Switch Buck-Boost Y-Rectifier (12-YR). Accordingly, **Chapter 5** discusses a 12-YR with a wide

DC output voltage range, which is not yet covered in literature. Worst case component stresses are derived for the considered operating range and filter design guidelines are provided to allow compliance with the CISPR 11 Class A emission limits. Further, a *dq*-coordinate based PFC rectifier control structure with low computational burden is proposed and the startup process is discussed. Experimental measurement with an 11 kW 12-YR prototype verify operation in buck as well as boost condition. The prototype system shows a power density of 12 kW/dm^3 and recorded efficiencies of up to 98.2 %.

Systematic converter designs (i.e., by means of Pareto optimizations) require accurate component loss models, and **Appendix A** accordingly investigates high-energy density ferroelectric Multilayer Ceramic Capacitors (MLCCs) promising evermore compact converter realizations, as no generally applicable loss model for large-signal excitation exists in literature. A new Steinmetz loss model is proposed which accurately predicts MLCCs losses under non-sinusoidal and/ or DC biased voltage excitations. This method is successfully verified under various operating conditions for a 1 kV X7R MLCC with loss prediction errors under 8 %.

6.2 Outlook & Future Research

With the ongoing energy transition, the research on bidirectional phase-modular three-phase buck-boost converters will continue. The generic nature of bidirectional buck-boost converter modules is an important aspect to highlight, which means that the modules can be further applied in a plurality of DC/DC and/or AC/AC applications with wide input-output voltage range requirements:

- *VICOR* lists the non-inverting four-switch buck-boost converter (i.e., the module of a 12-YI) as one of three core topologies for future data center supply systems [160].

- For Electric Vertical Takeoff and Landing (EVTOL) aircraft powered by a battery (for peak and emergency power) and an FC (providing the bulk energy with high gravimetric energy density), the two DC source voltages (each varying in a wide range) need to be interconnected by a buck-boost DC/DC converter [161].

- Similarly, an adapted 12-YI module can be employed in a dual-input (e.g., PV *and* battery supplied) LLC converter [162].

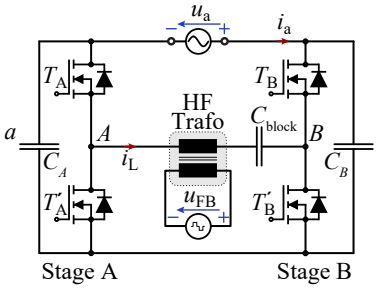

Fig. 6.1: Adaption of a 12-YI phase module to a single-phase isolated AC/AC cycloconverter as proposed in [163].

- As proposed by [163] and highlighted in **Fig. 6.1** a 12-YI module could even be employed (with minor adoptions) as a single-phase quasi-single-stage isolated AC/AC cycloconverter.

- Another field of application could also be fixed-frequency buck-boost three-phase AC/AC conversion [164]. A 12-YR could be modified into a three-phase buck-boost quasi-single-stage AC/AC cycloconverter as highlighted in **Fig. 6.2a**, or could even be used as an isolated AC/AC converter as shown in **Fig. 6.2b**.

Hence, from a product management and/or economic perspective, versatile buck-boost converter modules are extremely interesting, as they can be employed in various application fields. When aiming at further cost reductions, the same 12-YI modules can be employed in applications with and without the need for buck-boost capability, where in case of buck-only applications, the boost half-bridge semiconductors are not assembled (and the boost half-bridge high-side switch is simply replaced with a low-cost short circuit jumper connection). In case of unidirectional power flow one power transistor per half-bridge can be further replaced by a low-cost diode.

Future research aiming at ever higher efficiency and power density values might focus on adapted module structures promising further volume and/or loss reduction, e.g.,

- multi-level (e.g., flying capacitor) bridge-legs [46, 165, 166],

- magnetic coupling of the buck-boost inductors of two or more parallel operated modules [167, 168], and

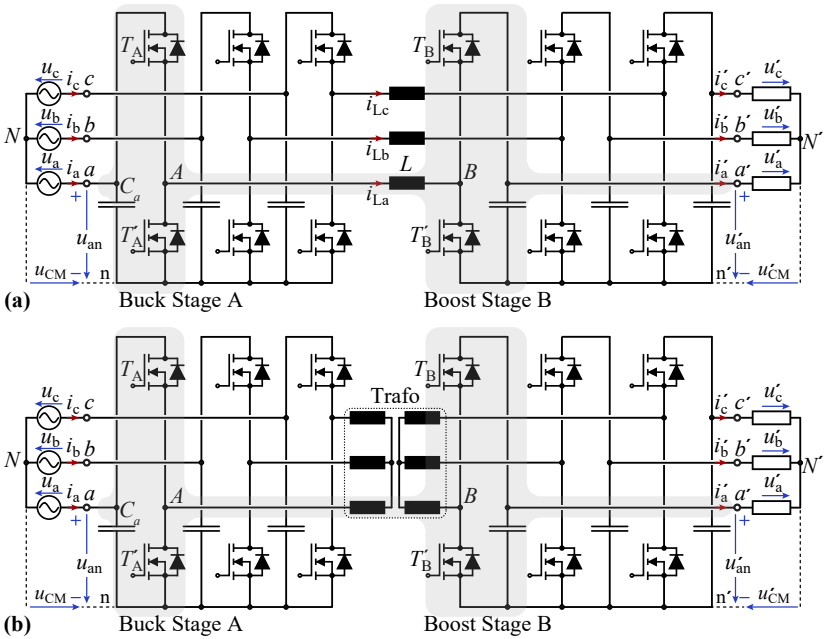

Fig. 6.2: Modification of a 12-YR to a three-phase **(a)** non-isolated and **(b)** isolated 12-YY buck-boost AC/AC cycloconverter (the module of the phase *a* is highlighted in light grey).

- modulation strategies enabling complete soft switching could be considered [169].

Another topic of future research could be an extended converter functionality such as, nominal power operation for single-phase as well as three-phase mains supplies for future EV on-board chargers [158,170]. Within this context, the prototype of a Six-Module 24-Switch Buck-Boost Y-Rectifier (24-YR) [158] – where the number of parallel modules is adapted based on the grid configuration – is currently being commissioned at the Power Electronic Systems Laboratory of ETH Zurich in the course of the continuation of the research described in this thesis.

Appendices

A

Loss Modelling of X7R Ceramic Capacitors under Large-Signal Excitation

This Appendix presents a novel loss model for non-linear ferroelectric multilayer ceramic capacitors under large-signal excitation also published in:

- D. Menzi, D. Bortis, G. Zulauf, M. Heller, J. W. Kolar, Novel iGSE-C Loss Modelling of X7R Ceramic Capacitors," *IEEE Transactions on Power Electronics*, Vol. 35, No. 12, pp. 13367-13383, December 2020. DOI: 10.1109/TPEL.2020.2996010.

Motivation

High-energy density ferroelectrics Multilayer Ceramic Capacitors (MLCCs) allow for ever-more compact converter realizations. This Appendix proposes a new Steinmetz-type loss model valid under large-signal excitation and various operating conditions.

Executive Summary

Due to the large relative permittivity of Class II dielectrics, ceramic capacitors from these materials promise significant volume and weight reductions in inverter and rectifier sinewave filters, and are especially attractive in mobile applications that demand ultra-high power density. While previous literature found large low-frequency losses in these components, no extensible loss model was proposed to accurately characterize these ferroelectric losses. In this work, we take advantage of prior art on ferro*magnetic* components in power electronics to propose a Steinmetz parameter-based loss modelling approach for X7R ceramic capacitors, named the improved Generalized Steinmetz Equation for Ceramic Capacitors, or iGSE-C. This model is verified using the Sawyer-Tower circuit to measure losses in a commercially-available X7R capacitor across excitation magnitude, DC bias, temperature, excitation frequency, and harmonic injection. Losses are shown to scale according to a power law with charge, with the resulting Steinmetz coefficients valid across DC bias and slightly varying as the temperature is increased. The iGSE-C accurately predicts losses for typical non-sinusoidal phase voltage waveforms with an error under 8 %.
Finally, the loss modelling technique is demonstrated for the sinewave output filter of a bridge-leg arrangement with both low- and HF excitations, with total capacitor losses predicted within 12 % accuracy.

A.1 Introduction

In the push towards ultra-compact power converters for emerging applications, including electric vehicles and more-electric aircraft, Electromagnetic Interference (EMI) filter volume and weight represent a key bottleneck to ever-higher volumetric and gravimetric power density. In switched-mode converters, these filters are unavoidable to protect the mains from High-Frequency (HF) conducted emissions and to comply with the relevant harmonic standards, and a path towards both miniaturization and weight reduction is sought.

For the sinewave filters of, e.g., three-phase rectifiers or motor drive systems with low HF stresses (to reduce bearing currents and/or increase feasible cable lengths), a variety of filtering techniques – both Common Mode (CM) and Differential Mode (DM) – are employed to filter switching harmonics while passing the fundamental frequency, as shown in **Fig. A.1**. Due to their low cost and high quality factor [171], film capacitors are predominantly

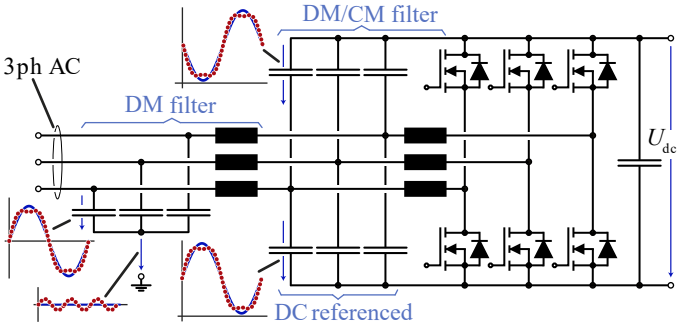

Fig. A.1: Illustration of a common sinewave filter structure for a three-phase inverter or PFC rectifier: open-star-point DM filter and combined DM/CM DC-link referenced filter. The resulting LF voltage waveforms across the filter capacitors for standard sinusoidal PWM operation with constant DC offset (solid line) and with additional 1/6 3rd harmonic injection [48] (dotted line) for maximum utilization of the linear modulation range are shown.

used in these applications, comprising approximately 50 % of the overall filter volume [134].

To reduce the filter volume and weight in applications highly sensitive to power density, Multilayer Ceramic Capacitors (MLCCs) are an attractive replacement for film capacitors [128]. For a 1 kV, 470 nF capacitor, the volume can be reduced by over 75× by moving from an off-the-shelf film capacitor (metallized polypropylene, KEMET PHE844RD6470MR30L2) to an off-the-shelf MLCC (X7R, Knowles Syfer 2220Y1K00474KETWS2), as shown in **Tab. A.1**. With this one-for-one replacement, the capacitor contribution to the filter volume becomes negligible, allowing the inductor size to be increased (reducing losses and improving efficiency) and/or a reduction in overall converter size and weight. As such, MLCCs are the preferred capacitor technology for ultra-compact converters, including those built for the Google Little Box Challenge [166, 172] and/or for any application, where the benefits of compactness outweigh the cost increase of the ceramic replacement (costs given in **Tab. A.1**).

In particular, X7R MLCCs have extremely high capacitance and energy density [171], originating from the large relative permittivity of ferroelectric Class II dielectrics [173]. X7R capacitors have excellent properties in the HF range for filtering switching harmonics, with a constant capacitance value over a wide frequency range, low Effective Series Resistance (ESR), and a

compact geometry that enables a low-inductance realization with a high self-resonant frequency (see the small-signal impedance measurements of the 2220Y1K00474KETWS2 capacitor in **Fig. A.2a-c**). With increasing voltage bias, however, X7R MLCCs exhibit (similar to magnetic components) dielectric saturation [174] and a decrease in capacitance, as measured in **Fig. A.2d**, well-known in the literature (e.g., [175]), and reported in capacitor datasheets.

In the context of line-frequency filtering, the effective capacitance is then highly dependent on the Low-Frequency (LF) voltage waveforms, and therefore on the filter configuration itself. To highlight these voltage waveforms, **Fig. A.1** shows both a combined DM/CM DC-link referenced LC-filter, which was proposed in [104] specifically to reduce the capacitance variation in a line cycle, and a pure DM filter structure. In motor drive applications, alternative modulation schemes employed to expand the modulation range and/or to decrease semiconductor losses [176] introduce additional harmonics (e.g., 3rd harmonic injection [48] or Discontinuous PWM (DPWM) [112]), which further impacts the voltages applied to the filter capacitors. **Fig. A.1** accordingly includes the resulting LF capacitor voltages for both standard sinusoidal modulation and additional 3rd harmonic injection. Lastly, the filter capacitors connected to the DC-link rails in **Fig. A.1** also face the triangular switching-frequency currents of the power inductors, causing a voltage variation and losses on a switching frequency level. Further, HF stresses are possible in alternative topologies such as the three-phase Twelve-Switch Buck-Boost Y-Inverter (12-YI) [58], where the filter capacitors are subject to both LF voltage waveforms with a DC offset and rectangular switching-frequency currents.

Recent work has found an elevated Dissipation Factor (DF) in MLCCs operating at low frequencies that is highly dependent on both DC bias and the large-signal excitation frequency and waveshape [177, 178]. These unexpectedly-high losses – as high as 10 W/cm^3 at 120 Hz [177] – cannot be predicted from the small-signal measurement data provided by manufacturers (in the datasheet or with online tools), and indeed Ref. [179] describes that small-signal measurements are fundamentally insufficient to characterize a ferroelectric capacitor. Within the context of elevated large-signal excitation losses, the compactness of MLCCs becomes a double-edged sword: although the loss contribution of MLCCs in a converter system may still be relatively small, substantial capacitor heating can result, eventually limiting, for example, the maximum fundamental frequency (and hence speed) for a motor drive system. In light of these unmodeled and substantial large-signal losses, we desire a method – extensible across voltage waveshape – to measure, characterize, and predict these losses in MLCCs.

Tab. A.1: Comparison of a film and a ceramic capacitor.

Dielectric	V_n	C_n	Volume	Price
Film (PP)	1 kV	470 nF	9.87 cm^3	1.94 $
Ceramic (X7R)	1 kV	470 nF	0.13 cm^3	6.69 $

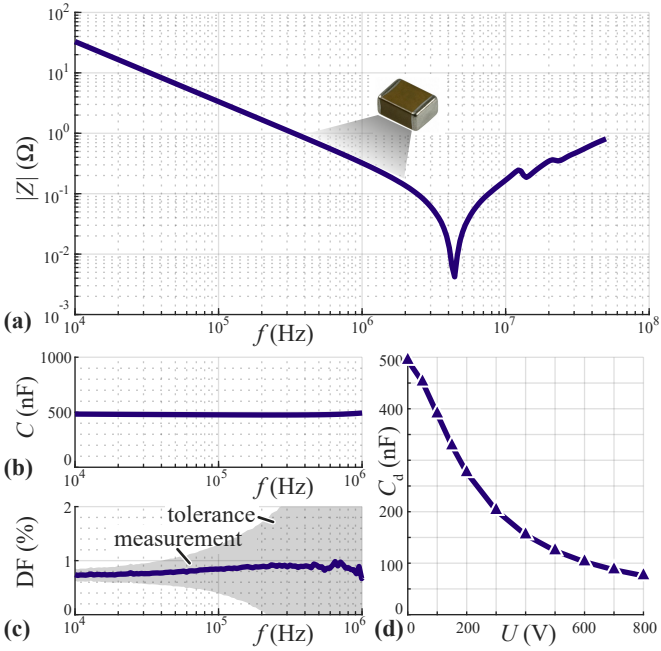

Fig. A.2: Small-signal measurements of **(a)** impedance, **(b)** capacitance, and **(c)** Dissipation Factor (DF) of the 1 kV, 470 nF, X7R Multilayer Ceramic Capacitor (MLCC) under test (Knowles Syfer 2220Y1K00474KETWS2) at room temperature (25 °C) and with 0.5 V_{rms} AC excitation. Self-resonance occurs at 4.4 MHz. The small-signal capacitance dependence on voltage is shown in **(d)**, where an AC excitation of 5 V_{rms} with 100 Hz was applied on top of the reported DC bias voltage U.

For *magnetic* components, which also exhibit loss mechanisms that must be characterized under large-signal conditions, Steinmetz parameters [180] are commonly provided to allow engineers to calculate core losses under a particular operating condition. In contrast, Refs. [177, 178] only provide loss look-up tables for the reported MLCCs under a sinewave excitation at a few frequencies and a multitude of DC bias points, leaving extensibility across DC voltage, AC waveshape, frequency, and part number unanswered. The current state of the art, then, requires additional measurements to design MLCC filters with losses that can be predicted *a priori* (excluding the coincidence when the filter capacitor, frequency, and selected part all exactly align with a reported measurement point).

Given these shortcomings and the attractiveness of MLCCs for converters with high power density, there is a clear need for a loss model for ferroelectric capacitors in power electronics. In the following, we propose a Steinmetz-based loss modelling approach for MLCCs under large-signal excitation, called the improved Generalized Steinmetz Equation for Ceramic Capacitors (iGSE-C), in **Sec. A.2**, which is verified with the measurement technique of **Sec. A.3** on a commercially-available ferroelectric capacitor in **Sec. A.4**. This particular capacitor, or the Device Under Test (DUT), is the 1 kV, 470 nF X7R MLCC of **Tab. A.2**, which was employed in a hardware prototype for an ultra-compact industrial motor drive with large observed LF excitation losses. Low-frequency losses are characterized across excitation magnitude, DC bias, temperature, and 3rd harmonic content. Next, HF losses are added for a complete picture of X7R MLCC losses in switched-mode power converters, which is validated in **Sec. A.5** with straightforward and extensible design guidelines for loss prediction *in situ* based on the iGSE-C. Finally, **Sec. A.6** summarizes the key findings and the proposed iGSE-C model.

A.2 Modelling Approach

For adoption and adaptability, the ferroelectric capacitor loss modelling approach must be extensible across voltage waveshape, excitation magnitude, and DC bias. A Steinmetz-based capacitor loss model is developed analogously to the well-known large-signal approach for ferro*magnetic* components, and we first review the conventional [180] and improved General [181] Steinmetz Equations for inductors to ground the proposed model.

A ferromagnetic hysteresis loop is shown in **Fig. A.3a**, where the magnetic field strength H (or current I) and flux density B (or flux linkage, Ψ, given by the time integral of the excitation voltage U) are linked by the permeability

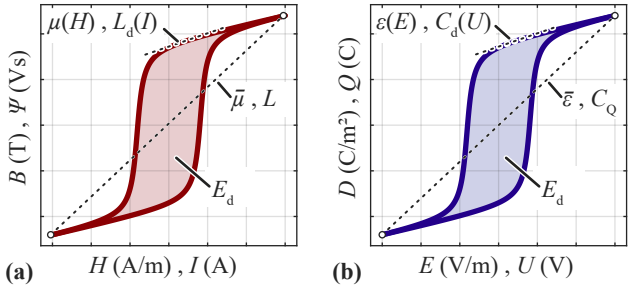

Fig. A.3: Illustration of a **(a)** ferro*magnetic* and **(b)** ferroelectric hysteresis loop, with instantaneous (L_d, C_d) inductances and capacitances highlighted separately from average large-signal values (L, C_Q).

$\mu(H)$ (or differential inductance $L_\mathrm{d}(I)$) as:

$$L_\mathrm{d}(I) = \frac{U}{dI/dt} = \frac{d\Psi}{dI}, \quad \mu(H) = \frac{dB}{dH}. \tag{A.1}$$

For a given hysteresis curve, both the average permeability $\overline{\mu}$ (or large-signal inductance L) and instantaneous permeability $\mu(H)$ can be calculated, and these are shown on **Fig. A.3a** as the appropriate slopes. The enclosed area E_d represents the energy dissipated in a single charge-discharge cycle, where hysteresis, eddy current, and residual losses are the main underlying loss mechanisms [182].

The time-averaged losses P of magnetic materials under a sinusoidal flux excitation depend on both frequency f and the peak magnetic flux density, B_pk, and empirically follow the power law given by the familiar Steinmetz Equation (SE) [180]:

$$P = k \cdot f^{\alpha} \cdot B_\mathrm{pk}^{\beta}, \tag{A.2}$$

where k, α, and β are material-specific constants characterized under large-signal excitation (note that f^{α} was not in the original equation, but was added later and is now standard [181]).

For a non-sinusoidal excitation – the condition in most power converters – a number of loss-modelling methods have been proposed. The improved Generalized Steinmetz Equation (iGSE) [181] is the most established method, and one with parameters directly extractable from the given Steinmetz parameters. The losses are assumed to depend both on the peak-to-peak flux

density ΔB and the flux density change rate dB/dt within a period T, as:

$$P = k_\mathrm{i} \cdot \Delta B^{\beta-\alpha} \cdot \frac{1}{T} \int_0^T \left|\frac{dB}{dt}\right|^\alpha dt, \tag{A.3}$$

with the coefficient k_i derived from the SE parameters as:

$$k_\mathrm{i} = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha 2^{\beta-\alpha} d\theta}. \tag{A.4}$$

If multiple minor hysteresis loops occur within a single period T, (A.3) is summed for each loop j separately to find average core losses as:

$$P_\mathrm{avg} = \sum_j P_j \frac{T_j}{T}. \tag{A.5}$$

With the SE and iGSE well-established for magnetic materials, we seek to develop an analogous loss modelling method for ferroelectric capacitors, including the ceramic components highlighted here. **Fig. A.3b** shows a ferroelectric hysteresis loop, where the electric field strength E (or voltage U) and displacement field D (or charge Q) are linked by the permittivity $\varepsilon(E)$ (or differential capacitance $C_\mathrm{d}(U)$) as:

$$C_\mathrm{d}(U) = \frac{I}{dU/dt} = \frac{dQ}{dU}, \quad \varepsilon(E) = \frac{dD}{dE}. \tag{A.6}$$

For a given hysteresis curve, both the average permittivity $\bar{\varepsilon}$ (or charge-equivalent capacitance C_Q) [183] and instantaneous permittivity $\varepsilon(E)$ can be calculated, and these are shown in **Fig. A.3b** as the appropriate slopes. Again, the area enclosed by the loop E_d represents the energy dissipated in a single charge-discharge cycle. In [184], a summary of capacitor losses mechanisms is provided, where ferroelectric Class II MLCCs hysteresis losses result similar to the hysteresis losses in magnetics [185, 186].

Ref. [187] proposed a Steinmetz power law to model ferroelectric capacitor losses under small-signal excitation with a fit on the peak sinusoidal voltage, $\hat{U}$. The same voltage-based Steinmetz template was used for losses in semiconductor output capacitance in [188, 189], where multiple sets of Steinmetz parameters were required to accurately describe the losses over the excitation voltage range. With the curve of **Fig. A.3b**, however, we see that a power law fit on excitation voltage (or field strength E) cannot hold in a ferroelectric

capacitor due to the charge saturation with increasing voltage magnitude. Steinmetz also worked on dielectric hysteresis and expected, based on theoretical considerations only, the losses to scale with $P = kfD_{\mathrm{pk}}^2$ for a peak charge density excitation D_{pk} [190]. In contrast to magnetic materials, the field quantity D of commercial MLCCs cannot be easily calculated, as the internal structure, and therefore the effective amount of dielectric material and electrode area per device volume, is not known (cf., **Fig. A.4**). However, the charge Q *can* be measured without in-depth knowledge of the exact MLCC realization.

Therefore, and in analogy with the ferromagnetic SE of (A.2), we propose to describe the losses in ferroelectric capacitors with a *peak charge based* (Q_{pk}) SE as:

$$P = k \cdot f^{\alpha} \cdot Q_{\mathrm{pk}}^{\beta}, \tag{A.7}$$

where k, α, and β are to be fitted under large-signal excitation. We note that SE parameters found for one MLCC cannot directly be employed for another product (even when the same dielectric is employed), as the charge density D is not known. However, in future datasheets, device manufacturers could provide the SE parameters of the employed dielectric and the dielectric volume density for each product to support loss calculations.

For non-sinusoidal excitations, an iGSE approach could again be applied, where for a peak-to-peak charge ΔQ the losses can be described:

$$P = k_{\mathrm{i}} \cdot \Delta Q^{\beta-\alpha} \cdot \frac{1}{T} \int_0^T \left|\frac{dQ}{dt}\right|^{\alpha} dt \tag{A.8}$$

and k_{i} is again given by the SE parameters and (A.4), where (A.8) collapses to (A.7) in the case of a sinusoidal excitation. This proposed loss model is named the improved Generalized Steinmetz Equation for Ceramic Capacitors, or the iGSE-C.

A.3 Measurement Method and Setup

With a modelling approach proposed, we turn to characterizing the losses in the selected X7R MLCC of **Tab. A.2**. Firstly, a measurement method must be selected that can evaluate the known loss dependencies outlined in **Sec. A.1** of:

- Large-signal excitation (sinusoidal and non-sinusoidal),
- DC bias,

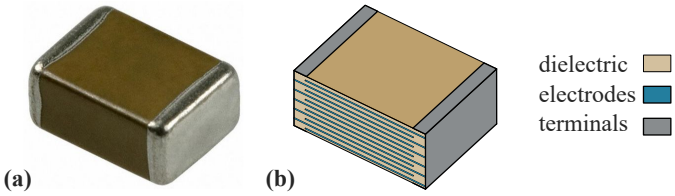

Fig. A.4: (a) Picture of the 1 kV, 470 nF, X7R Multilayer Ceramic Capacitor (MLCC) under test (Knowles Syfer 2220Y1K00474KETWS2) and **(b)** illustration of the internal structure of a MLCC consisting of several electrode and dielectric layers. The resulting capacitance value depends on the employed dielectric and the number, arrangement, and thickness of the electrodes [175]. These parameters are not known for commercial devices.

- Frequency,
- High-frequency currents, and
- Temperature.

Ideally, this measurement method produces rapid measurements that can be applied to transient conditions, can measure losses at constant temperature, is applicable across a wide frequency range, and is valid with non-sinuosoidal waveforms. We briefly survey potential electric and calorimetric methods.

A.3.1 Potential Measurement Techniques

Voltage-Current Electric Measurement

A voltage-current electric measurement that measures instantaneous power with a voltage and current probe is one candidate for loss characterization. This method fulfills the need for fast, quasi-pulse measurements in a time period that avoids a substantial increase of the DUT temperature, and Ref. [177] used a Yokogawa WT3000 power analyzer to measure the losses in two ferroelectric capacitors under 120 Hz large-signal excitation. Ref. [178] used a similar measurement approach to validate a calorimetric measurement and calculate volumetric energy storage at low frequencies.

This direct measurement method introduces a number of challenges, however. For a high-quality factor MLCCs, avoiding a phase error between the voltage and current probes is paramount and, unfortunately, difficult to maintain across excitation frequency and when non-sinusoidal waveforms are

applied. To overcome this problematic calibration step, currents could be measured with a precision shunt and a voltage probe to simplify phase matching. With the current of a capacitor scaling linearly with frequency (for a constant voltage), however, a large number of shunts would be required to achieve a good signal-to-noise ratio for a frequency range of several orders of magnitude.

Sawyer-Tower (ST) Electric Measurement

The Sawyer-Tower (ST) method was introduced in 1930 [191] to evaluate Rochelle salt as a dielectric, and operates by adding a well-characterized, low-loss reference capacitor in series with the DUT to calculate the charge in the DUT. This method has been employed in various power electronics applications, including to characterize capacitors for microprocessor applications [192] and to measure soft-switching losses (up to the MHz frequency range) in silicon superjunction MOSFETs [188], SiC MOSFETs [193], and GaN-on-Si HEMTs [189]. For semiconductor-specific measurements, the ST circuit was improved and simplified in [194].

The ST measurements are conducted with passive voltage probes, and with the voltage ratio between the DUT and the reference capacitor constant over frequency, a single ST setup can be used to cover the whole frequency range of interest.

Calorimetric Measurements

Calorimetric measurement techniques achieve excellent accuracy independent of frequency and the ratio of reactive to active power, and have been used to characterize capacitor losses [178, 195, 196]. Here, three calorimetric measurement types and the respective shortcomings with respect to measuring large-signal excitation MLCC losses are discussed:

- **Steady-State Calorimetric Measurement:** A steady-state calorimetric measurement has the advantage that the fundamentally large ratio of reactive to active power has no impact on the measurement accuracy or precision, and these measurements were conducted with film capacitors for traction applications in [195]. With the strong temperature dependence of X7R MLCCs previously known [177], this technique is not possible here.
- **Indirect Transient Calorimetric Measurement:** An indirect measurement uses the temperature increase of something *other than the*

DUT to estimate the losses in the DUT. These losses are typically recorded under quasi-steady-state conditions. In Ref. [196], the dielectric losses of insulation materials were evaluated by measuring the increase in temperature of a thermally-isolated test chamber (with a calibration resistor in an equal package). In [178], a similar approach was used, with the DUT located in an oil bath and the temperature increase measured. In [197] and [198], Wide Band-Gap (WBG)-semiconductor switching losses were measured with the temperature increase of a brass block after a DC current calibration (the steep $\mathrm{d}v/\mathrm{d}t$-transients jeopardize any electrical measurement). While this measurement technique produces valid, accurate results, it is much slower than the implemented electrically-based technique.

- **Direct Transient Calorimetric Measurement:** In order to rapidly evaluate semiconductor hard and soft switching losses, recently a new method was introduced where the temperature of the semiconductor case is measured directly (again after a DC current calibration step), reducing the measurement time to the range of seconds [199]. The same method was employed in [200] to characterize the losses of magnetic materials under large-signal excitations with frequencies up to 50 MHz. The calibration losses are generated by impressing a DC current upon the magnetic core samples.
  The DC calibration (or any other known loss calibration) is not possible for capacitors, and therefore this method is not directly applicable here. Based on existing capacitor loss data, however, this method can be employed for an *in situ* measurement in a hardware prototype, as discussed in **Sec. A.4.4** and demonstrated in **Sec. A.5.2**.

Selected Measurement Technique

With the ease of calibration, extensibility across waveforms, and transient measurement capability, the ST method is the preferred candidate for this measurement suite, and the circuit operation is covered in detail in the subsequent section.

A.3.2 Sawyer-Tower Measurement

The ST circuit is shown in **Fig. A.5a**, with both the voltage across the linear reference capacitor C_{ref} (u_{ref}) and the excitation voltage u_{ac} measured. Depending on the position of the mechanical switch, either the lossy and

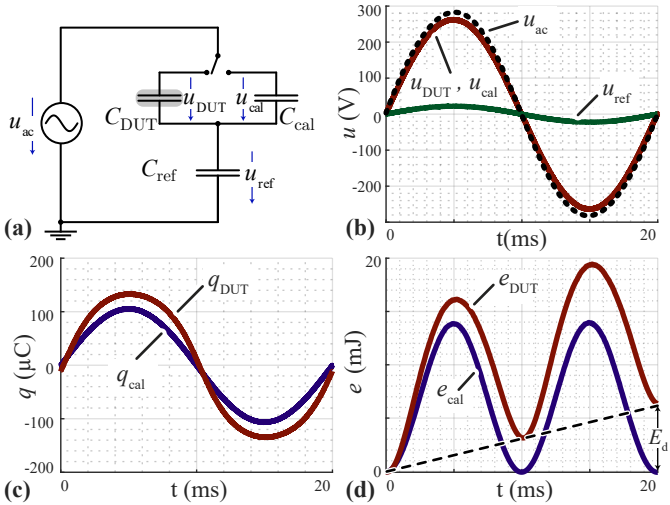

Fig. A.5: (a) Schematic circuit of the employed Sawyer-Tower (ST) measurement setup (either the DUT or a calibration capacitor is connected in series to the reference capacitor) for AC voltage excitation. Resulting time domain waveforms for the ST measurement: **(b)** voltage, **(c)** calculated charge, and **(d)** calculated stored energy. For the lossless calibration capacitor, the stored energy e_{cal} is fully recovered within an AC period, giving identical initial and final energy. For the lossy DUT, however, some portion of the stored energy is dissipated, yielding a final e_{DUT} larger than the initial e_{DUT} (the distance of which is represented by E_{d}).

non-linear DUT or the calibration capacitor C_{cal} is measured, where C_{cal} is ideally linear and lossless and serves to calibrate the ST setup. The component selection for the realization of C_{ref} and C_{cal} is discussed in further detail at the end of this section, where non-ferroelectric C0G capacitors with a 20x to 30x lower Dissipation Factor (DF) than the Class II ferroelectric MLCCs of interest are employed (cf., **Tab. A.2**).

The measured voltage waveforms are shown for operation with both C_{cal} and C_{DUT} in **Fig. A.5b**, and the component values according to **Tab. A.2**. With the charge q (cf., **Fig. A.5c**) in series capacitors equal, we can write (note that the following loss equation is derived for the DUT, but the same equations and procedure apply for the calibration capacitor C_{cal}):

$$u_{\mathrm{DUT}}(t) = u_{\mathrm{ac}}(t) - u_{\mathrm{ref}}(t) \tag{A.9}$$

$$q_{\mathrm{DUT}}(t) = q_{\mathrm{ref}}(t) = u_{\mathrm{ref}}(t) \cdot C_{\mathrm{ref}}. \tag{A.10}$$

With C_{ref} selected as much higher capacitance than C_{DUT} or C_{cal}, only a small fraction of the applied voltage u_{ac} appears across it (cf., **Fig. A.5b**).

Integrating the instantaneous power, the energy stored in the non-linear DUT, e_{d}, can be calculated using measured the DUT voltage u_{DUT} and charge q_{DUT} (derived from u_{ref} with (A.10)) as:

$$e_{\text{DUT}}(t) = \int_0^t u_{\text{DUT}}(\tau) \cdot i_{\text{DUT}}(\tau) d\tau = \int_0^t u_{\text{DUT}}(\tau) \cdot \frac{dq_{\text{DUT}}}{d\tau} d\tau = \int_{q_{\text{DUT}}(0)}^{q_{\text{DUT}}(t)} u_{\text{DUT}} dq_{\text{DUT}}. \quad \text{(A.11)}$$

Note that in practice the time-domain energy waveform $e_{\text{d}}(t)$ highlighted in **Fig. A.5d** is obtained by numerically integrating u_{DUT} across q_{DUT}. For a signal periodic with T (i.e., $u_{\text{DUT}}(0) = u_{\text{DUT}}(T)$ and $q_{\text{DUT}}(0) = q_{\text{DUT}}(T)$) and starting with the global charge minima $q_{\text{DUT}}(0) = q_{\text{min}}$, the dissipated energy E_{d} (i.e., the area enclosed by the U-Q hysteresis loop in **Fig. A.3b**) of one cycle can be calculated, which yields the active power,

$$P = \frac{E_{\text{d}}}{T} = \frac{1}{T}\Bigg(\underbrace{\int_{q_{\text{DUT}}(0)}^{q_{\text{DUT}}(T/2)} u_{\text{DUT}} dq_{\text{DUT}}}_{\text{charge}} + \underbrace{\int_{q_{\text{DUT}}(T/2)}^{q_{\text{DUT}}(T)} u_{\text{DUT}} dq_{\text{DUT}}}_{\text{discharge}} \Bigg), \quad \text{(A.12)}$$

where the charge increment dq is positive and negative in the charge and discharge interval, respectively, such that the respective energy values are effectively subtracted. E_{d} is highlighted in **Fig. A.5d** for the DUT, which stands in contrast to the calibration capacitor (in the same figure) where all of the stored energy is recovered. The Dissipation Factor (DF) is defined by the ratio of dissipated E_{d} and stored E_{stored} energy

$$DF = \frac{E_{\text{d}}}{2\pi \cdot E_{\text{stored}}}, \quad \text{(A.13)}$$

and is a good measure for the loss-rate of non-linear MLCCs. For a linear capacitor (or a non-linear capacitor with small-signal excitation), the DF is identical to the the Loss Tangent ($\tan\delta$) (i.e., the ratio of active and reactive power).

Tab. A.2: Employed components.

Component	Dielectric	Manufacturer	Part Number	V_n	C_n	N(parallel)	C_{tot}	DF
C_{cal}	C0G	TDK	CAA572C0G2J204J640LH	650 V	200 nF	2	400 nF	< 0.02 %
C_{ref}	C0G	TDK	C5750C0G2A154J230KE	100 V	150 nF	32	4.8 µF	< 0.03 %
C_{DUT}	X7R	Knowles Syfer	2220Y1K00474KETWS2	1 kV	470 nF	1	470 nF	> 0.71 %

When C_{cal} is measured, two linear capacitors are excited by the sinusoidal voltage u_{ac}, resulting in the sinusoidal charge waveform q_{cal} of **Fig. A.5c**. The non-linearity of C_{DUT}, however, causes the charge waveform q_{DUT} not to be purely sinusoidal, shown for contrast in **Fig. A.5c**.

The selection of C_{ref} is critical for the accuracy of the ST measurements, and we highlight the key characteristics here. Firstly, C_{ref} takes a certain fraction of the applied AC voltage, which should be kept relatively small, such that the DUT sees the majority of the excitation voltage U_{ac}. This can be achieved with $C_{\text{ref}} >> C_{\text{DUT}}$, where a reasonable choice might be $C_{\text{ref}} \approx 10 \cdot C_{\text{DUT}}$. Secondly, if the DUT and the reference capacitor show the same loss tangent, the two measured voltages (u_{ac} and u_{ref}) will be in phase, resulting in no measured $U - Q$ hysteresis and zero measured losses. The reference capacitor, therefore, must have substantially lower $\tan\delta$ than the DUT. Lastly, the ST is fundamentally reliant on the linearity of C_{ref} to calculate the charge from voltage (see (A.10)), and the reference capacitors should be highly linear, i.e., a ferroelectric Class II capacitor should not be used for C_{ref}.

In light of these requirements, C_{ref} and the calibration capacitors C_{cal} are realized with low-loss, Class I C0G capacitors with extremely stable dielectrics. The key properties are summarized in **Tab. A.2**, with the DF of C_{ref} and C_{cal} at least an order of magnitude below the DUT (which was directly measured under small-signal conditions in **Fig. A.2c**). For the C0G reference and calibration capacitors, the small-signal DF accurately approximates the large-signal DF, and the impact of the small-but-non-zero DF of C_{ref} is neglected in the following loss measurements.

With this simple and extensible technique, losses in ferroelectric capacitors can be characterized across voltage, temperature, waveform shape, DC bias, and frequency, and we move to validate the proposed loss model of **Sec. A.2** with measurements on the selected DUT.

A.4 Experimental Results

A sinusoidal AC excitation is applied to the circuit of **Fig. A.5a** with an AC power source ($U_{\text{ac,max}}$=270 V_{rms}), with the initial calibration measurements shown at 50 Hz for a range of excitation voltages in **Fig. A.6**.

With the calibration C0G capacitor (**Fig. A.6a**), the capacitance is linear for all magnitudes, resulting in a constant C_{Q} across voltage and $C_{\text{Q}} = C_{\text{d}}$. There is no measurable hysteresis between the charging and discharging curves at a given voltage, resulting in negligible losses that are verified with

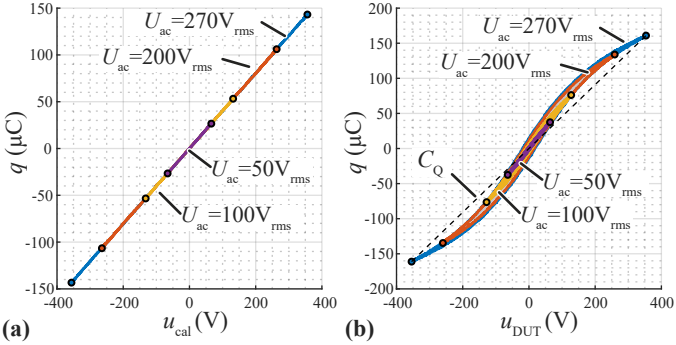

Fig. A.6: $U - Q$ hysteresis recorded at 50 Hz for a range of excitation voltages for **(a)** the calibration capacitor, which shows no hysteresis and has a constant $C_Q = C_d$ at all voltages, and **(b)** the DUT, which exhibits increasing hysteresis and losses with increasing excitation voltage. C_Q highlighted for U_{ac} =270 V_{rms}. Measured $U - Q$ curves are identical at 50 Hz and 100 Hz.

no heating of C_{cal} during the test procedure. This "zero-loss" reading also validates a proper deskew of the voltage probes.

For the same excitation voltages at 50 Hz, **Fig. A.6b** shows the measured ferroelectric $U_{DUT} - Q$ hysteresis curves for the X7R DUT capacitor. At 50 V_{rms}, the capacitor is approximately linear ($C_Q \approx C_d$), but clearly starts saturating for higher excitation amplitude. C_Q changes across applied voltage, and C_d deviates from C_Q at different voltages along the $U_{DUT} - Q$ curve. With an increasing voltage, further, the hysteresis area between the charging and discharging curves expands (especially near the zero-crossing, as we return to later), indicating an increase in losses with excitation voltage.

Even at the line frequency of 50 Hz, these hysteretic losses total as high as 0.5 W per DUT capacitor, and the large-signal DF is nearly an order-of-magnitude higher than the small-signal DF measured in **Fig. A.2c**. These significant losses, validated by [177, 178], justify a deeper investigation of the key loss drivers, and we evaluate the impact of frequency and excitation magnitude based on the proposed SE (**Sec. A.4.1**), harmonic injection based on the proposed iGSE-C (**Sec. A.4.2**), DC bias (**Sec. A.4.3**), temperature (**Sec. A.4.4**), and, finally, the impact of the HF excitations necessarily imposed by the switching frequency current ripple of the inductors connected to the half-bridge switch nodes in **Fig. A.1** (**Sec. A.4.5**).

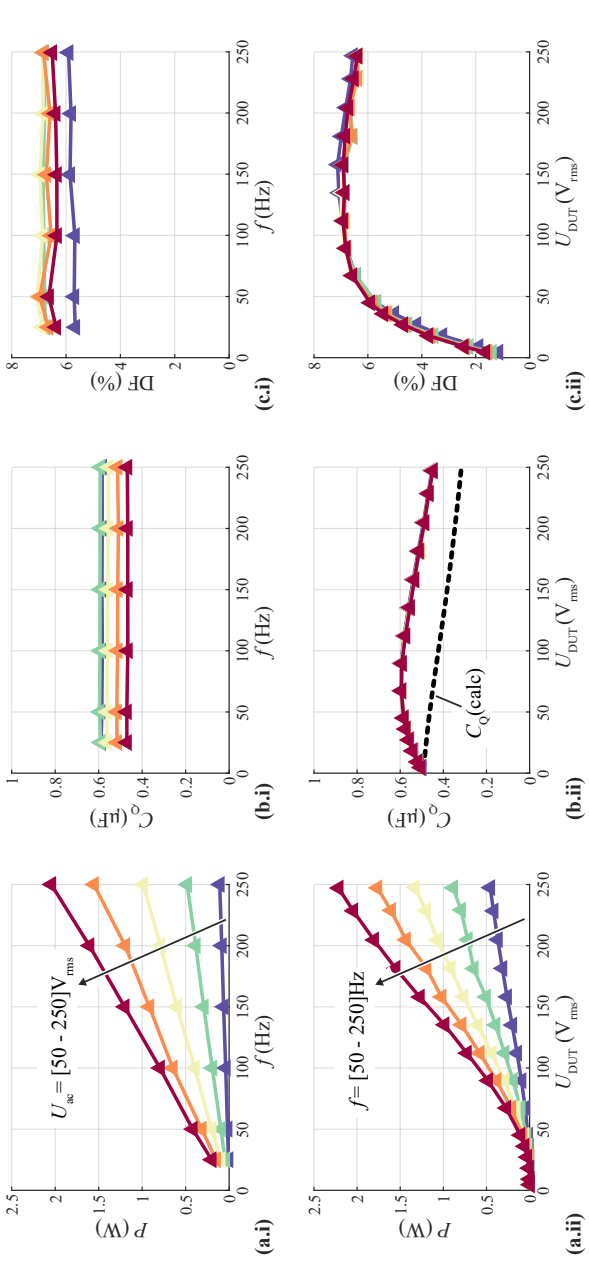

Fig. A.7: Measured losses in the X7R MLCCs DUT using the Sawyer-Tower circuit of **Fig. A.5a** across AC excitation voltage and AC excitation frequency. The DF is nearly an order-of-magnitude larger than expected from the small-signal measurements (**Fig. A.2c**) and capacitance *increases* up to U_{DUT} =100 V_{rms}. Losses linearly increase with frequency equivalent to an SE parameter of $\alpha = 1$. **(a)** Losses P, **(b)** AC charge equivalent capacitance C_{Q} (the expected value C_{Q}(calc) derived from **Fig. A.2d** is represented by the dashed line, and in **(b.ii)** all capacitance curves are overlapping), and **(c)** Dissipation Factor (DF), plotted against **(i)** frequency and **(ii)** DUT voltage rms value.

A.4.1 Impact of AC Excitation Magnitude and Frequency

The impact of LF excitation voltage and frequency are evaluated from, respectively, 50 V_{rms} to 250 V_{rms} and 50 Hz to 250 Hz. These measurements are recorded at room temperature (25 °C) with a measurement time of 1 s to avoid self-heating of C_{DUT} and to isolate any impact of temperature on the losses. The impact of temperature is investigated later in **Sec. A.4.4**, where we find that self-heating of up to 10 °C changes the losses by no more than ≈5 % for the operating points considered here.

The measured losses are shown in **Fig. A.7**. Firstly, we note the measured DF exceeds 7.0 % under certain operating conditions, far above the 0.7 % predicted by the small-signal characterization of **Fig. A.2c** and resulting in losses as large as 2 W. **Fig. A.7a.i-c.i** highlights the impact across frequency, and we find a linear scaling of losses with f, supporting the finding of $\alpha = 1$ from [187] for the SE of (A.7). C_Q and DF do not vary across this frequency range (with the slight measured deviations attributed to measurement error and heating of the DUT). This linear loss-frequency relationship (and the identical $U - Q$ hysteresis curves across frequency) are supported by the stable capacitance value of the DUT across frequency, as observed under both small-signal (**Fig. A.2a-b**) and large-signal (**Fig. A.7b.i**) conditions. Therefore, when increasing the frequency for a given excitation amplitude, the same ferroelectric hysteresis curve (cf., **Fig. A.6**) is traversed more often, dissipating a constant amount of energy per cycle and accordingly resulting in a linearly-increasing power.

Across varying excitation voltage (highlighted in **Fig. A.7a.ii-c.ii**), however, we observe significant deviations from the expected behaviour of the X7R DUT capacitor. At low excitation voltage, the DF approaches the small-signal value (0.7 %), increases up to 7.0 % at 100 V_{rms}, then saturates and even slightly decreases as the magnitude is further increased (**Fig. A.7c.ii**). This voltage-dependent trend follows the other surprising finding that C_Q *increases* up to 100 V_{rms} (**Fig. A.7b.ii**) – for all X7R capacitors, we expect the capacitance to steadily *decrease* with voltage, as shown by the calculated charge-equivalent capacitance derived from the small-signal measurements of **Fig. A.2d** (dotted line in **Fig. A.7b.ii**). The peak capacitance is over 600 nF, more than 20 % greater than the measured value at zero DC bias. This effect of increasing capacitance with AC magnitude is also described in Ref. [175].

The additional capacitance indicates a large-signal polarization mechanism around the voltage zero-crossing that is not captured by measurements with small AC magnitudes. While this phenomenon is investigated more in **Sec. A.4.3**, we note here that the extra capacitance is undesired for filtering.

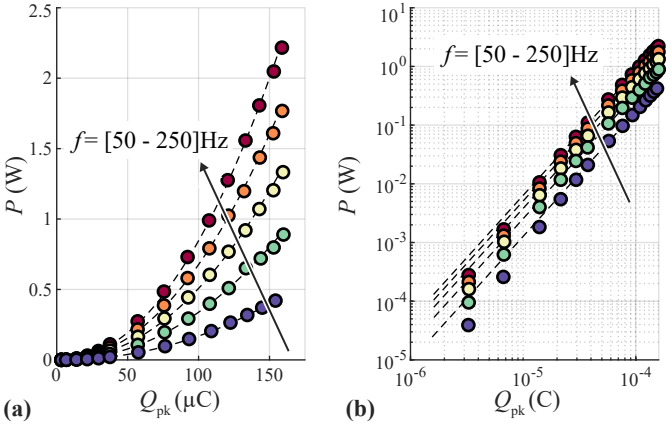

Fig. A.8: Measured losses, from **Fig. A.7**, plotted against measured charge Q_{pk} for AC frequencies from 50 Hz to 250 Hz and AC voltages from 50 $\mathrm{V_{rms}}$ to 250 $\mathrm{V_{rms}}$. Dotted lines are derived Steinmetz parameters ($k = 1.06 \cdot 10^6$, $\alpha = 1$, and $\beta = 2.12$) in (A.7), which show excellent agreement with the measured data. **(a)** Linear representation and **(b)** logarithmic representation.

The fundamental reactive currents in the capacitor are $I_{\mathrm{Q}} = 2\pi f C_{\mathrm{Q}} U_{\mathrm{DUT}}$, so a larger C_{Q} large-signal capacitance maps to increased conduction losses in the inductors and semiconductors of the converter while the capacitance available for switching-frequency filtering remains limited to the appropriate small-signal value of **Fig. A.2d**.

Finally, we return to the proposed charge-based SE modelling to evaluate whether the measured losses are appropriately captured by (A.7). In **Fig. A.8**, the measured losses are scattered against the measured charge excitation amplitude (cf., (A.10))

$$Q_{\mathrm{pk}} = \frac{1}{2}(\max(q_{\mathrm{DUT}}(t)) - \min(q_{\mathrm{DUT}}(t))), \tag{A.14}$$

on both linear (**Fig. A.8a**) and logarithmic (**Fig. A.8b**) scales. Steinmetz parameters are fit from the measured data and plotted using (A.7) as dotted lines on both scales, with selected values of $k = 1.06 \cdot 10^6$, $\alpha = 1$, and $\beta = 2.12$. This fitting matches the measured data extremely well, with discrepancies only at very low excitation magnitudes where the measurement precision is low (losses in the 10 µW range), strongly supporting the proposed charge-based SE modelling approach. We note that a voltage-based power law relationship

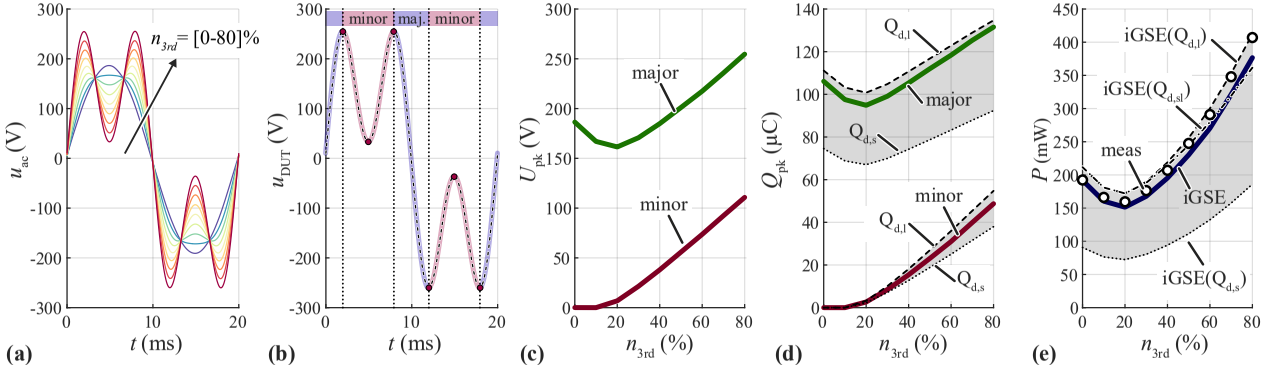

Fig. A.9: Measurements under 3rd harmonic injection conditions to validate the proposed iGSE-C modelling approach for non-sinusoidal voltage waveforms. **(a)** Measured excitation voltage waveforms with the 3rd harmonic injection of variable magnitude (n_{3rd}) superimposed upon the 50 Hz, 150 V_{rms} fundamental voltage excitation. For $n_{3rd} > 20\%$, minor loops result (the splitting of major and minor loops is highlighted for $n_{3rd} = 80\%$ in **(b)**). **(c)** Measured peak voltage amplitude U_{pk} of major and minor loops over n_{3rd}. **(d)** Measured peak charge amplitude Q_{pk} of major and minor loops over n_{3rd}, as well as the calculated charge from the large-signal ($Q_{d,l}$) and small-signal ($Q_{d,s}$) differential capacitance curves of **Fig. A.15**. **(e)** Measured (scatter points) and calculated losses from (A.8) and (A.5) based on the measured charge (iGSE) or based on the calculated charge from the large-signal (iGSE($Q_{d,l}$)) and small-signal (iGSE($Q_{d,s}$)) differential capacitance curves of **Fig. A.15**, or with the hybrid approach using large- and small-signal capacitance (iGSE($Q_{d,sl}$)) for each loop separately (cf., **Sec. A.5.1**). Accuracy between measured and calculated losses is within 7.6 % when using the measured charge.

(proposed in [187] for small-signal excitation) cannot accurately capture the measured losses, as the losses have two distinct scaling regions with voltage (exponential below $50\,V_{rms}$, linear above $50\,V_{rms}$) that are clearly seen in **Fig. A.7a.ii**.

Our characterization of losses across voltage magnitude and frequency confirm the proposed SE fitting, finding a strong dependence of losses on peak charge (more than quadratic, with $\beta = 2.12$) and a large-signal polarization near the zero-crossing that increases both converter conduction losses and the losses in the capacitor itself. With the charge-based SE approach confirmed, we next add superimposed harmonics to evaluate the iGSE-C extension of ferroelectric capacitor losses.

A.4.2 Impact of Harmonic Injection and iGSE Modelling

Generally, the modelling approach must be valid for non-sinusoidal waveforms. For filter capacitors in motor drive inverter or three-phase PFC rectifier applications, in particular, the 3rd harmonic (and its multiples) of the fundamental frequency is often used to extend the modulation range of the PWM scheme [176]. In the proposal of the iGSE loss modelling approach for magnetic materials [181], the method was verified by superimposing a 3rd harmonic component of varying magnitude upon the fundamental frequency excitation. Analogously, the ferroelectric iGSE-C proposed here in (A.8) is tested with the DUT under 3rd harmonic injection.

Methodology

The DUT is excited with a single phase of a pre-existing buck-type three-phase inverter that complies with CISPR 11 Class A, making the HF noise negligible at the DUT and supporting a variable-magnitude 3rd harmonic injection. A fixed fundamental $150\,V_{rms}$, 50 Hz sinusoidal excitation is applied to the DUT and the 3rd harmonic component is gradually increased from 0 % to 80 % of the fundamental amplitude, as shown in **Fig. A.9a**.

With the linear loss dependence on frequency ($\alpha = 1$) found in **Sec. A.4.1**, the integral term in (A.8) simplifies to twice the peak charge excitation magnitude Q_{pk} and the equation collapses to (A.7) for each loop. The losses can be straightforwardly calculated with (A.5) using major and minor loop splitting. In **Fig. A.9b**, an example of this major and minor loop splitting is shown for $n_{3rd} = 80\,\%$, with the peak voltage U_{pk} in each harmonic loop shown across the tested n_{3rd} values in **Fig. A.9c**.

Measurement Results

With the SE parameters defined and the iGSE-C modelling known, the final step in predicting losses under non-sinusoidal excitations is to determine the correct peak stored charge, Q_{pk}, to use in (A.7). **Fig. A.9d** shows three methods of estimating the charge in each loop: the directly-measured charge (solid lines), the charge calculated from the large-signal differential capacitance ($Q_{\mathrm{d,l}}$), and the charge calculated from the small-signal differential capacitance ($Q_{\mathrm{d,s}}$). The large- and small-signal predictions are necessary for extensibility to arbitrary excitation waveforms and voltages, but we see that these two predictions differ widely in charge estimation, and therefore in loss prediction, with the large-signal $Q_{\mathrm{d,l}}$ overestimating stored charge and the small-signal $Q_{\mathrm{d,s}}$ underestimating the measured charge. This discrepancy – and an appropriate technique to estimate charge from an arbitrary voltage waveform – is investigated in depth in **Sec. A.5**.

Fig. A.9e shows the calculated losses under 3$^{\mathrm{rd}}$ harmonic injection conditions with these different charge calculations, with a maximum error of 7.6 % between the measured and calculated losses using the proposed iGSE-C modelling with the measured charge. At low harmonic injection magnitudes, the voltage waveforms consists of a single major loop with decreasing peak amplitude, resulting in a decrease in measured losses. Above 20 % harmonic injection, two identical minor loops start to appear. For $n_{3\mathrm{rd}} > 20\,\%$, the peak charge of the major loop starts to increase again, thereby increasing the measured and predicted losses.

While the agreement between the measured losses and predicted losses constitutes a validation of the proposed iGSE-C loss modelling approach, the estimation of peak charge is again seen to be fundamental to the *a priori* loss prediction in **Fig. A.9e**. This figure highlights the discrepancy in SE loss estimation between using the measured charge (excellent accuracy, denoted as SE), the calculated large-signal differential capacitance $C_{\mathrm{d,l}}$ curve (again fairly accurate, $SE(Q_{\mathrm{d,l}})$), and the calculated small-signal differential capacitance curve $C_{\mathrm{d,s}}$ (significant underestimate of losses, $SE(Q_{\mathrm{d,s}})$). In **Sec. A.5**, we propose a hybrid approach that calculates the large- and small-signal capacitance for each loop separately ($Q_{\mathrm{d,sl}}$) and gives the most accurate and extensible results to estimate peak charge and therefore to predict losses (cf., **Fig. A.9e**).

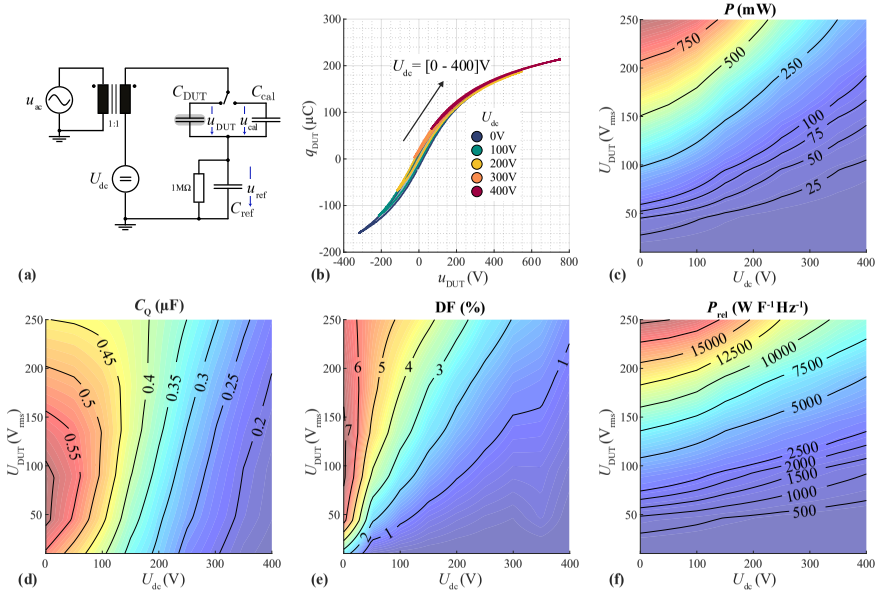

Fig. A.10: Measured losses with varying DC bias and AC excitation voltage in the X7R MLCC under test (frequency fixed at 100 Hz for all measurements). Increasing DC bias decreases the losses in the DUT but simultaneously decreases the effective capacitance. Under the proposed charge-based SE loss model, DC bias has no impact on losses if peak charge is held constant (see **Fig. A.11**). **(a)** Schematic circuit of a Sawyer-Tower measurement setup with AC voltage excitation and DC voltage bias. All measurements are conducted with an AC frequency of 100 Hz. The employed components are given in **Tab. A.2**. **(b)** Measured hysteresis curves for constant AC amplitude of 250 V_{rms} and increasing DC bias from 0 V to 400 V. Due to the parallel resistor of the reference capacitor, only the AC charge can be evaluated. As a function of AC voltage U_{DUT} and DC bias voltage, measured: **(c)** losses P, **(d)** charge-equivalent AC capacitance C_Q, **(e)** Dissipation Factor (DF), and **(f)** losses P_{rel} normalized by measured AC capacitance and frequency, $P_{rel} = P/(C_Q \cdot f)$.

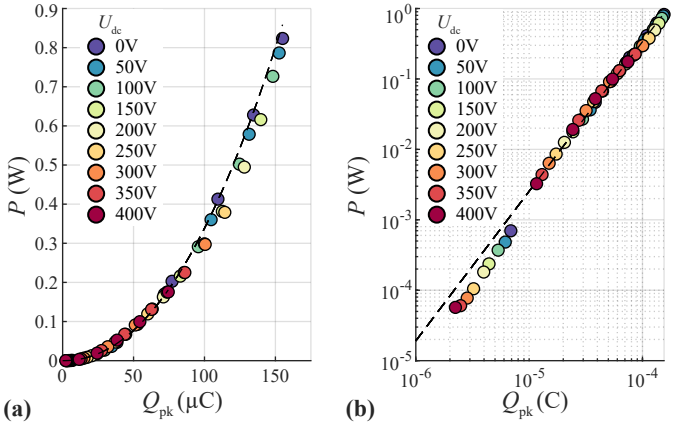

Fig. A.11: Measured losses, from **Fig. A.10c**, plotted against measured charge Q_{pk} for 100 Hz AC frequency, AC voltages from 50 V_{rms} to 250 V_{rms}, and DC bias from 0 V to 400 V. Dotted lines are derived Steinmetz parameters ($k = 1.06 \cdot 10^6$, $\alpha = 1$, and $\beta = 2.12$) in (A.7), which show excellent agreement with the measured data even under DC bias. The same Steinmetz fitting holds under DC bias conditions, indicating that the losses in the DUT are not dependent on DC bias, unlike in magnetic components. **(a)** Linear representation and **(b)** logarithmic representation.

A.4.3 Impact of DC Bias

For magnetic materials, a DC premagnetization has a significant impact on the losses [201] that is not captured by the iGSE. To overcome this shortcoming, Ref. [202] provided Steinmetz Premagnetization Graphss (SPGs) for several magnetic materials to quantify the dependency of the Steinmetz parameters on the premagnetization current bias. Naturally, and especially with the well-known voltage dependence of X7R capacitors (as measured for the DUT in **Fig. A.2d**), the impact of a DC voltage offset on the MLCC losses must be investigated. We find here that the DC bias has no impact on the charge-loss relation found in **Sec. A.4.1**, and that the same SE parameters can be employed to calculate the losses with a DC bias.

Methodology

The Sawyer-Tower circuit of **Fig. A.5a** is modified slightly, as shown in **Fig. A.10a**, to add a variable DC bias to the DUT. The DC bias source U_{dc} is referenced to protective earth with the AC excitation (from the AC power source) applied on top with an insulating transformer. A 1 MΩ resistor is added across the reference capacitor to ensure that the whole DC bias is applied to the DUT (otherwise, the DC voltage sharing is only defined by the capacitor leakage currents and the passive voltage probe resistances, i.e., poorly controlled parameters). As a result, only the AC charge excitation is captured by the Sawyer-Tower measurement, and the DC charge offset is added by integrating the previously-measured (in **Sec. A.4.1**) large-signal differential capacitance to the DC bias voltage. The DC bias is varied from 0 V to 400 V with AC excitations at 100 Hz from 0 to 250 $\mathrm{V_{rms}}$.

Measurement results

Fig. A.10b shows the measured hysteresis curves for a constant AC excitation voltage of 250 $\mathrm{V_{rms}}$ and a DC bias increased in 100 V increments from 0 V to 400 V. With a positive bias, the hysteresis becomes non-symmetric due to the voltage-dependent non-linearity of the capacitor. The peak-to-peak charge excitation shrinks with increasing DC bias, especially when the large-signal polarization around 0 V is avoided, and consequently both the losses and the large-signal capacitance (C_{Q}) decrease.

Fig. A.10c-f show contour maps of measured losses, large-signal capacitance, dissipation factor DF, and normalized losses across varying excitation magnitude (U_{DUT}) and DC bias (U_{dc}). **Fig. A.10c** shows the measured

losses, with the zero DC bias results (along the y-axis) matching the results of **Fig. A.7a.ii** with a maximum of 823 mW. As expected from the curves of **Fig. A.10b**, the hysteresis area and the losses drop with increasing DC bias for a given AC excitation.

The large-signal capacitance also decreases with increasing DC bias, as shown in **Fig. A.10d**. The maximum AC capacitance is shifted towards higher AC amplitudes as the DC bias is increased, with the maximum occurring only when the curve encloses a voltage zero-crossing that results in large-signal polarization (explored in depth in **Sec. A.5**). **Fig. A.10e** shows the dissipation factor DF, which continuously decreases with increasing DC bias (for a given AC excitation magnitude). We find, then, that a DC-referenced filter structure with a DC bias voltage and strictly positive capacitor voltages (cf., **Fig. A.1**) would yield lower overall losses than a filter with zero DC bias, although more parallel capacitors would need to be employed to achieve the same effective capacitance value.

To visualize this tradeoff between losses (improving with DC bias) and capacitance (decreasing with DC bias), **Fig. A.10f** normalizes the losses by AC capacitance and frequency, allowing a direct comparison of filter losses for an effective capacitance requirement. For a given AC excitation amplitude, the losses are either relatively constant across DC bias or decrease slightly at higher excitation amplitudes (where the zero crossing can be avoided with a large DC bias). We return to the Steinmetz fitting to more rigorously assess the effect of DC bias on losses and capacitance.

Steinmetz fitting

The measured losses across DC bias from **Fig. A.10c** are scattered against the Steinmetz excitation parameter of (A.7), Q_{pk} (which is here derived from the charge-equivalent AC capacitance C_{Q} and U_{DUT}) in **Fig. A.10d**, in both linear (**Fig. A.11a**) and logarithmic (**Fig. A.11b**) scales. The scatter color represents the DC offset voltage. The same Steinmetz fitting from **Sec. A.4.1** ($k = 1.06 \cdot 10^6$, $\alpha = 1$, and $\beta = 2.12$) is plotted as a dotted line in each plot.

Fig. A.11 clearly shows that the losses still follow the identical power law fit obtained from the AC-only measurement results, with discrepancies again only evident for loss magnitudes below 1 mW. In contrast to magnetic materials, the DC bias has no impact on MLCC losses *for a given charge excitation amplitude* in the considered frequency range. While the bias has a major impact on the differential capacitance, as shown in **Fig. A.10c**, only the charge magnitude is needed to calculate losses. This greatly simplifies the

loss modelling of MLCCs and again validates the proposed charge-based SE and iGSE-C approaches.

A.4.4 Impact of Temperature

Thus far, short measurement times were used to maintain the DUT near room temperature (25 °C) and measure consistent loss data, but with Ref. [177] showing that the losses of X7R MLCCs are highly temperature dependent, the impact of temperature on the measured and modeled losses needs to be evaluated.

Methodology

To assess the impact of temperature on losses, the DUT capacitor is now allowed to self-heat with a long measurement time. The measurement results from **Sec. A.4.1** revealed losses of 9 mW/Hz or a loss density of 69 mW/Hz/cm^3 at the maximum excitation voltage of 270 V_{rms}, and hence substantial capacitor heating is expected.

Electrical (via the Sawyer-Tower circuit) and thermal measurements (via a high-frame rate thermal camera, the FLIR A655sc) are recorded simultaneously. Voltages are recorded with a large-memory oscilloscope, with memory sufficient to record 28 s of data with losses on an individual cycle basis extractable in post-processing (tests were stopped after 28 s or if the DUT reached 90 °C). To synchronize the electrical and thermal measurements, we assume a small thermal capacitance (C_{th}) of the DUT and align the oscilloscope trigger with the first increase of temperature. Similarly, the turn-off of the electrical source and the peak temperature happen simultaneously (noting that the device does not reach thermal steady-state in any of our test conditions), providing another synchronization verification. The excitation voltage is fixed at 270 V_{rms} and the frequency is varied from 100 Hz to 500 Hz with 100 Hz steps.

To provide a secondary loss verification with temperature, additional short-pulse (no self-heating) measurements (similar to **Sec. A.4.1**) are recorded with the DUT fixed to a heating plate at variable temperature. These losses are recorded at 500 Hz.

Measurement results

The recorded temperature and measured losses across elapsed time are shown in **Fig. A.12a-b**, with the short-duration hot-plate measurements overlaid as scatter points. These short-pulse measurements are close to, but constantly

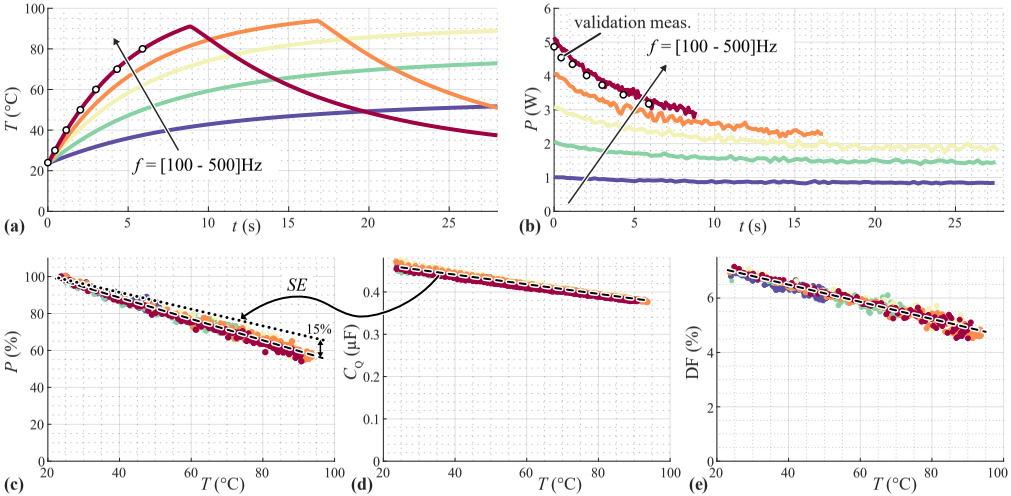

Fig. A.12: Electrically measured losses under transient conditions with varying DUT temperature and excitation frequency from 100 Hz to 500 Hz (excitation magnitude fixed at 270 V_{rms} for all measurements). Scattered circles show measurements without self-heating (a hot-plate was used to control the device temperature and short-pulse measurements, like those reported in **Sec. A.4.1**, were conducted), which match the transient measurements closely and validate the methodology. Losses and effective capacitance decrease with temperature, but losses decrease faster than C_Q and the DF therefore decreases. **(a)** Measured DUT temperature and **(b)** losses over time for a constant AC voltage U_{ac} =270 V_{rms} and increasing frequency f from 100 Hz to 500 Hz. Scatter points show hot-plate measurements to validate the transient method. **(c)** Losses relative to the initial value at room temperature (25 °C), **(d)** measured large-signal capacitance, and **(e)** dissipation factor DF as a function of temperature T. The decrease of charge-equivalent capacitance in **(d)** reduces the SE-predicted losses to those shown by the dotted line in **(c)**, with a maximum overestimation of 15 % over the measured losses at high temperature.

slightly below, the losses measured in the transient measurement, which can be explained by the unavoidable self-heating implicit in the short-duration tests that shifts the real dielectric temperature slightly higher. The losses near $t = 0\,\mathrm{s}$ are close to the measured results and Steinmetz predictions of **Sec. A.4.1**. Overall, these verifications indicate both that the synchronization is accurate and the temperature-dependent losses can be accurately measured under transient conditions.

Measured losses (normalized to the room-temperature value), large-signal capacitance, and dissipation factor DF are plotted with respect to temperature in **Fig. A.12c-e**. We observe that both losses and effective capacitance drop substantially with increasing temperature (also shown in [177]), with losses declining faster than capacitance and dissipation factor DF therefore declining at higher dielectric temperature.

While the charged-based SE parameters for MLCCs do not depend on DC bias, these results indicate that operating temperature is an important factor that must be considered for loss prediction. In **Fig. A.12c**, for example, the dashed line of best fit is plotted to represent the change of losses as $P_{\mathrm{rel}}(T) = 1 - 0.58\,\%/\mathrm{K} \cdot (T - T_0)$ (with $T_0 = 20.28\,^{\circ}\mathrm{C}$). At high temperatures, the room-temperature SE parameters overpredict the measured losses by a maximum of 15 %, as shown with the dotted line in **Fig. A.12c**. This indicates two separate temperature-related effects: firstly, the decrease in charge-equivalent capacitance with increasing temperature (**Fig. A.12d**) results in lower predicted losses based on lower Q_{pk} (the SE line in **Fig. A.12c**), but there appears to be an additional change to the dielectric loss mechanism with temperature that accounts for an additional 15 % of loss reduction. This discrepancy could eventually be obviated by means of an SE coefficient $k(T)$ that scales linearly with temperature, but with a small resulting deviation, this is not further considered.

Transient calorimetric capacitor loss measurement

This work was originally motivated by unexpectedly-high filter capacitor losses in an existing converter prototype. In these existing systems, a Sawyer-Tower circuit cannot be directly employed and the designer may be seeking to select the optimal filter capacitor or quantify the losses. From transient calorimetric techniques (e.g., [199]), we know that the device temperature and device losses are linked by the thermal resistance R_{th} and thermal capacitance C_{th}, and fitting these to the loss measurements of **Fig. A.12** may enable *in situ* calorimetric loss measurements. This transient technique is introduced here and again used for two filter capacitors in **Sec. A.5**.

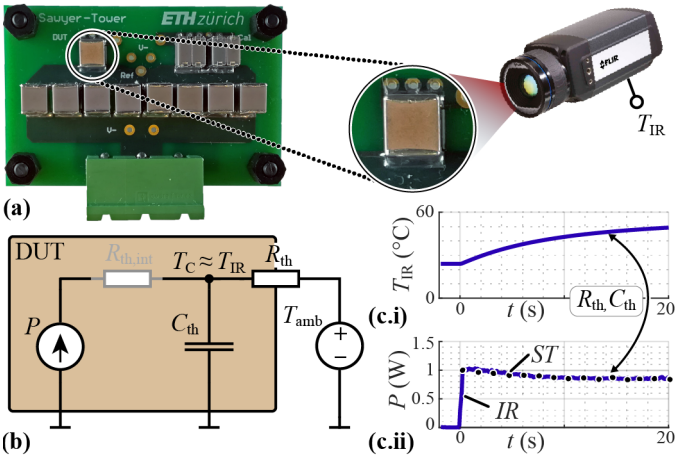

Fig. A.13: Illustration of an *in situ* transient calorimetric capacitor loss measurement approach: **(a)** Sawyer-Tower circuit with highlighted DUT MLCC and FLIR A655sc thermal camera, **(b)** simplified thermal equivalent circuit of the DUT where the internal thermal resistance $R_{th,int}$ is assumed to be negligible, **(c.i)** recorded temperature curve from **Fig. A.12a** ($f = 100\,\text{Hz}$) and **(c.ii)** calculated capacitor losses with $R_{th} = 34.96\,°\text{C/W}$ and $C_{th} = 0.325\,\text{Ws/°C}$.

To perform an *in situ* transient loss measurement (**Fig. A.13a**), the following procedure is followed:

1. The temperature rise of the capacitor $T(t)$ is recorded with a high frame rate thermal camera (if the DUT is not accessible with a thermal camera, a temperature sensor can be used) for an operating point where the losses are known across temperature. Here, we use the 100 Hz excitation of **Fig. A.12a**, but any previously-recorded LF excitation is a good candidate.

2. With the equivalent thermal circuit of **Fig. A.13b**, and assuming $R_{th,int}$ is negligible, the equivalent thermal resistance R_{th} and thermal capacitance C_{th} are extracted from the temperature curve as:

$$P(t) = C_{th} \cdot dT(t)/dt + \frac{T(t) - T_{amb}}{R_{th}}. \tag{A.15}$$

For the measurement results in **Fig. A.12a** and the Sawyer-Tower setup of **Fig. A.13a**, the thermal resistance and capacitance are fitted as $R_{th} =$

34.96 °C/W and $C_{\text{th}} = 0.325\,\text{Ws/°C}$. **Fig. A.13c.i** shows the recorded temperature curve from **Fig. A.12a** for $f = 100\,\text{Hz}$, and in **Fig. A.13c.ii**, we see that the calculated capacitor losses with (A.15) and the measured $T(t)$ are in good agreement with the electrically-measured (using the Sawyer-Tower circuit) losses in **Fig. A.12b**.

Note that both R_{th} and C_{th} are determined by the particular physical environment in which the capacitor is installed, and must be determined on a setup-by-setup basis. We show the application of this transient prediction method in **Sec. A.5**.

A.4.5 HF Excitation

Finally, as a filter component in a switched-mode converter like **Fig. A.1,** the MLCCs will necessarily see switching frequency harmonics. The losses from this HF waveform component must be understood as well, and we seek to characterize the losses in the DUT from 1 kHz to 100 kHz.

Methodology

Measuring these HF losses across the large capacitances studied here introduces additional difficulties and a minor reconsideration and recalibration of the measurement setup (note that prior HF Sawyer-Tower measurements measured capacitances of the, at most, nF order, not the 100 nF order studied here [188, 189]). From **Fig. A.2a**, we see that the DUT impedance is now in the range of Ω, and, according to the DF measurement of **Fig. A.2c**, this places the ESR in the range of 10 mΩ which is of the same order as the contact resistance of the solder joints and connection paths. Further, the current, which increases linearly with frequency, is several orders of magnitude higher than in **Sec. A.4.1**, making the control of the resistive losses critical.

If the reference capacitor and calibration capacitor are considered lossless and $C_{\text{ref}} \approx 10 \cdot C_{\text{cal}}$, as in **Sec. A.4.1**, equal contact resistance for both capacitors causes the apparent loss tangent of the reference capacitor to be ten times larger than that of C_{cal}, giving a *negative* loss reading for the calibration and also deteriorating the measurement with the DUT. Minimizing the return path impedance is therefore crucial and has to be verified with a calibration measurement. For the HF measurements, it is preferred to have similar capacitance magnitudes between C_{ref} and the DUT to overcome this issue and to allow a calibration measurement with close to identical currents as in the DUT evaluation, and C_{cal} is implemented with one 0.2 µF (TDK, CAA572C0G2J204J640LH) and two 0.15 µF (TDK, C5750C0G2A154J230KE)

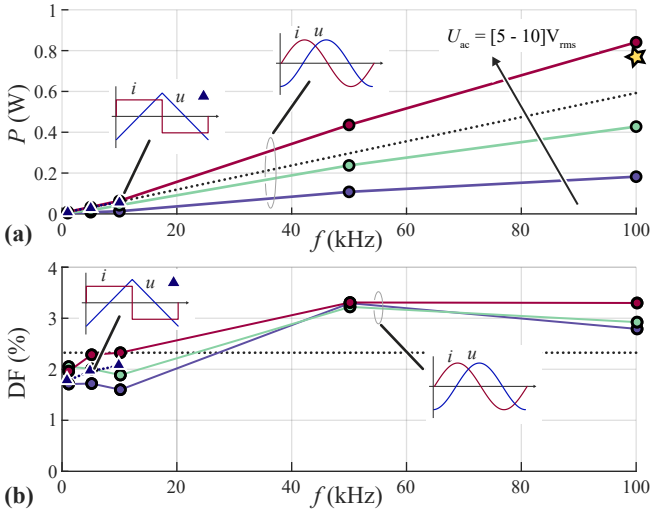

Fig. A.14: Measured losses at HF in the MLCCs DUT from 1 kHz to 100 kHz with excitation voltages of 5, 7.5 and 10 V_{rms}. Losses are identical between triangular (measurement indicated with triangular scatter points) and sinusoidal (indicated with round scatter points) excitations with the same peak voltage, as expected by the SE fitting of $\alpha = 1$. Triangular waveform measurements are limited by the power amplifier bandwidth to 10 kHz. **(a)** Measured losses and **(b)** Dissipation Factor (DF). Star scatter point shows thermally-measured losses using (A.15), which validates the HF Sawyer-Tower measurements.

C0G capacitors, yielding a total capacitance of 500 nF, which is equal to the DUT under small-signal conditions. (Note that one alternative is measuring a capacitor with the same dielectric but less capacitance, which simultaneously increases the impedance and ESR and can be selected to again make the ESR much greater than the contact resistances. This approach was not selected here because the exact realization of the dielectric is not known with commercial devices.)

Excitations of 5, 7.5 and 10 V_{rms} are applied to the DUT, with the magnitude limited by the total losses, which scale with frequency. A sinusoidal excitation is applied with a HF power amplifier up to 100 kHz, and, to validate that $\alpha = 1$ holds at HF, a triangular voltage (rectangular currents) excitation of 10 V_{rms} is also applied. The triangular waveform is limited to 10 kHz by the bandwidth of the HF power amplifier.

Measurement results

Fig. A.14 shows the measured HF losses under the triangular and sinusoidal voltage excitations. The dissipation factor DF for 10 V_{rms} is relatively flat (above 2 %) up to 10 kHz and increases to 3.3 % at 100 kHz for losses of 860 mW. As expected with $\alpha = 1$, the losses for triangular voltages and sinusoidal voltages with the same peak AC voltage are identical, as shown in **Fig. A.14a**. A transient thermal measurement is performed to validate the HF Sawyer-Tower measurements, where using (A.15) and the previously-derived R_{th} and C_{th} values, we find losses of 787 mW at 100 kHz (represented by the star scatter point in **Fig. A.14a**).

These measurements provide a loss estimation for the HF component in the filter capacitors. The measured DF does not change substantially when moving to the kHz range, with a small increase for higher excitation amplitudes. The effect of DC bias on the HF losses was not considered, although recent research indicates a bias dependence for ceramic capacitor losses above 75 kHz [203]. Even under the assumption of constant SE parameters at HF, there is excellent matching between the calculated and calorimetrically-measured losses in a practical application, as we show in the following section. In this section, we combine the HF and LF loss modelling approaches to provide guidelines to estimate MLCC losses in a switched-mode converter application.

A.5 Guidelines for Converter Loss Estimation

We again return to the analogy of ferro*magnetics* to highlight the challenges unique to ferroelectric MLCCs. In a converter like **Fig. A.1**, the inductive components are subject to both LF (typically sinusoidal and near line-frequency) current imposed by the control system and a HF current ripple due to the PWM operation of the power semiconductors. Because these two frequencies are separated by multiple orders of magnitude, the loss contributions are typically considered separately and in most practical applications, the LF core losses are small [204]. The HF magnetic flux is determined easily by integrating the applied voltage-time area, but the losses for a given excitation are DC-bias dependent and Steinmetz Premagnetization Graphss (SPGs) are required to calculate the HF core losses [202]. As gapped inductors are designed with sufficient margin to the saturation flux density of the core (to avoid a sudden roll-off of the inductance value), they feature an almost constant inductance value throughout the eligible current range and hence the premagnetization

can easily be calculated [205]. In summary: with known SE parameters and SPGs, the assessment of core losses is relatively straightforward.

As previously presented, the capacitors of the sinewave filter in the converter of **Fig. A.1** also face a LF voltage excitation and a HF voltage ripple due to the PWM operation of the power semiconductors. To use the presented iGSE-C approach with ferroelectric capacitors, the charge excitation must be known, which for the HF excitation can be obtained directly by integrating the HF inductor current ripple. Assuming the Steinmetz parameters are independent of DC bias (shown in **Sec. A.4.3** for low frequencies up to 250 Hz) for high frequencies as well, the HF losses are straightforward to assess and are relatively minor in sinewave filters with a large fundamental voltage swing and low HF voltage ripple. In contrast to magnetic materials, however, the fundamental frequency losses in the MLCCs are substantial, as shown in this work. For a given voltage, the charge excitation depends on the non-linear relative permittivity (or differential capacitance), and with the SE and iGSE-C modelling dependent on the peak charge stored, the correct estimation of this charge is critical to obtain an accurate loss calculation. According to **Fig. A.2d**, the differential capacitance of the DUT reduces by approximately 70 % for a DC bias of 400 V, and the nominal operating regime includes, essentially, substantial saturation which further complicates the charge estimation. This charge estimation is the focus of the following sub-section.

A.5.1 Evaluation of the Charge Excitation

For a given capacitor voltage excitation $U(t)$, the charge is defined by the differential capacitance C_d as:

$$Q(t) = \int C_\mathrm{d}(U) \cdot \frac{dU(t)}{dt} dt = \int C_\mathrm{d}(U) dU. \tag{A.16}$$

With the highly non-linear C_d found in **Sec. A.4.1**, the small-signal C_d curve in **Fig. A.2d** is only true under small-signal excitation conditions. Otherwise, $C_\mathrm{d}(U)$ must be back-calculated using (A.6) under the large-signal excitations. From **Fig. A.10** and the discussion around those results, we can already see that multiple $C_\mathrm{d}(U)$ functions must exist that depend on the excitation magnitude and the DC bias. The extracted $C_\mathrm{d}(U)$ from the excitations in **Fig. A.10b** are plotted in **Fig. A.15** for U_ac =250 $\mathrm{V_{rms}}$ and DC bias voltages of 0 V, 200 V, and 400 V (in the plot, we exclude regions where dQ/dt or dV/dt are close to zero to avoid poor signal-to-noise ratios).

First, we see a large dependence of differential capacitance both with DC bias U_dc and with the direction of the excitation (charging or discharging) in

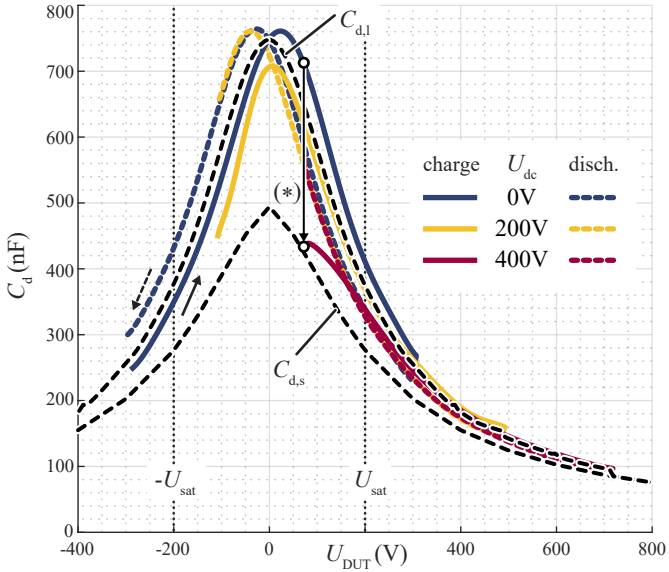

Fig. A.15: Differential capacitance over voltage derived according to (A.6) for the measured hysteresis curves shown in **Fig. A.10b** with 250 V_{rms} AC excitation and increasing DC bias of 0 V, 200 V, and 400 V. The differential capacitance is shown for the charging (solid) and discharging (dotted) portions of the voltage excitation. For a given voltage, C_d depends greatly on the overall hysteresis waveform, including the AC magnitude, DC bias, and direction of the excitation (see $(*)$, which highlights the variability near 0 V). The small-signal $C_{d,s}$ and large-signal $C_{d,l}$ differential capacitance curves can be used to estimate the charge excitation for small or large AC voltage excitations, respectively.

Fig. A.15. The (∗) highlights that the C_d close to the zero-voltage crossing greatly depends on both the DC bias and the overall path of the hysteresis loop. In contrast, if the charging signal exceeds U_sat, the associated discharging C_d is, for the most part, largely independent of DC bias and AC magnitude. (The same holds true if the discharging curve exceeds $-U_\mathrm{sat}$, with identical charging curves.) For the $U_\mathrm{dc} = 400\,\mathrm{V}$ excitation, the capacitor voltage never changes sign, and the large-signal polarization is not fully relaxed when the minimum voltage is approached. The ensuing "non-switching transition" [206] (where the voltage polarity never reverses) results in a low differential capacitance C_d.

The non-linearity of the capacitance around the zero-voltage crossing, then, complicates the prediction of the stored charge for a given voltage waveform, as the integration in (A.16) is not straightforward. For large AC excitation magnitudes, Q can instead be conservatively approximated with the large-signal capacitance as the average of C_d during the rising and falling voltage excitations, as shown in **Fig. A.15** with the $C_\mathrm{d,l}$ dashed line. This curve is a good approximation when the AC swing exceeds $|U_\mathrm{sat}|$ on both the negative and positive voltage swings. $C_\mathrm{d,s}$ remains a valid prediction of charge storage under small-signal excitations.

For an arbitrary waveform, including those with the 3$^\mathrm{rd}$ harmonic injections of **Fig. A.9a**, the charge in a given loop can be calculated with either $C_\mathrm{d,s}$ or $C_\mathrm{d,l}$, which respectively yield the lower and upper bounds on hysteretic losses, as shown in **Fig. A.9d** and **Fig. A.9e**. Neither prediction method of charge from a given voltage waveform, however, is perfect, and there remains the question of exactly what voltage magnitude constitutes a small- or large-signal excitation.

A comparison of the resulting charge approximation error (σ) using $C_\mathrm{d,s}$ and $C_\mathrm{d,l}$ for the measured charge in **Fig. A.10d** is shown in **Fig. A.16**. As expected, the small-signal charge prediction $C_\mathrm{d,s}$ is a good approximation when the AC magnitude is small absolutely or relative to the DC bias (cf., **Fig. A.16a**), while the opposite holds true for the prediction given by $C_\mathrm{d,l}$ (cf., **Fig. A.16b**).

The regions where the small- and large-signal approximation respectively yield the minimal absolute charge error $|\sigma|$ are separated by the red line U_bound in **Fig. A.16**, which can be simplified as (the dashed lined in **Fig. A.16**):

$$U_\mathrm{bound} = 0.60 \cdot U_\mathrm{dc} + 26.35\,\mathrm{V}. \tag{A.17}$$

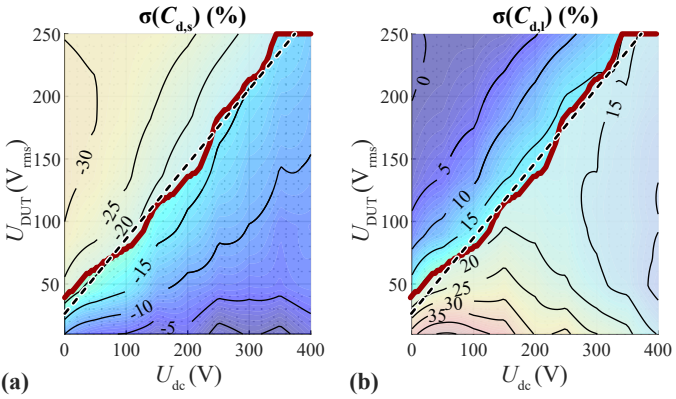

Fig. A.16: Relative error σ of the calculated charge-equivalent capacitance $C_{\mathrm{Q,calc}}$ using (A.16) for sinusoidal AC excitation and DC bias relative to the measured C_{Q} of **Fig. A.10d** with **(a)** the small-signal $C_{\mathrm{d,s}}$ and **(b)** the large-signal differential capacitance $C_{\mathrm{d,l}}$ (cf., **Fig. A.15**) models. The red line indicates the boundary between the regions where the small- and large-signal approximations are respectively preferred to minimize the charge approximation error.

For a minimal charge approximation error at a given DC bias U_{dc}, C_{d} is selected as:

$$C_{\mathrm{d}} = \begin{cases} C_{\mathrm{d,s}}, & U_{\mathrm{DUT,rms}} \leq U_{\mathrm{bound}} \\ C_{\mathrm{d,l}}, & U_{\mathrm{DUT,rms}} > U_{\mathrm{bound}}, \end{cases} \tag{A.18}$$

yielding a maximal charge approximation error of $|\sigma_{\mathrm{max}}| = 20\,\%$ across the full DC bias and AC magnitude sweep. With minor loops for non-sinusoidal excitations, (A.17) should be employed for each loop separately, as shown in **Fig. A.9e**.

This charge estimation approach – necessitated by the non-linear ferroelectric characteristics, and especially by the large-signal polarization near 0 V – could be avoided by designers with two potential alternatives. Once the SE parameters have been derived for a given DUT, the losses can be calculated based solely on a charge measurement (e.g., using a current probe and determining the charge by integration) when the device is excited with the desired fundamental frequency waveform. (Note that this method is difficult to use to *determine* the SE parameters, as discussed in **Sec. A.3**.) Alternatively, manufacturers could provide (in addition to SE parameters) online tools for hysteresis modelling based on their physical knowledge of polarization effects in commercial dielectrics.

A.5.2 Design Example

Finally, we employ the tools and measured losses here to calculate the total losses of MLCCs in a single-phase DC/AC converter with a split 800 V DC-link and a 50 Hz, 250 V_{rms} AC voltage (shown in **Fig. A.17a.i**). The switching frequency is selected at $f_s = 100\,\text{kHz}$ and a two-stage filter (comprised of two identical filter stages, S_1 and S_2, with a crossover frequency $f_c = 10\,\text{kHz}$) provides an attenuation of approximately 80 dB at the switching frequency. Each filter is constructed with an inductor of $L = 85\,\mu\text{H}$ and 6 paralleled DUT capacitors ($C = 2.8\,\mu\text{F}$). A load of 380 Ω is used at the output.

The filter stages have a nearly-identical fundamental-frequency voltage excitation (**Fig. A.17a.ii**), with the fundamental-frequency voltage drop across the inductor of S_1 safely neglected. The peak HF current ripple $\hat{i}_{L,HF}$ of the inductor in S_1 can be calculated from the time varying duty cycle $d(t) = \frac{u_{ac}(t)}{\frac{1}{2}U_{dc}}$ pattern as:

$$\hat{i}_L(t) = \frac{1}{8}\frac{U_{dc}(1-d)(d+1)}{Lf_s}, \tag{A.19}$$

and reaches up to 12 A in this application. In S_2, the HF current ripple is attenuated by an additional 40 dB and is therefore negligible (**Fig. A.17a.iii**), yielding an opportunity to break apart the relative loss contributions from the LF and HF components.

According to (A.18), the LF charge is best calculated using $C_{d,l}$, with $\hat{Q}_{LF} = 159\,\mu\text{C}$ as the result. To validate this prediction, the filter capacitor of S_2 was replaced with the ST setup, where a LF peak excitation of $\hat{Q}_{LF} = 156\,\mu\text{C}$ was directly measured (cf., **Fig. A.17b.i**).

The HF charge excitation in S_1 can be obtained by integrating the HF inductor current of S_1 and dividing the current by the 6 paralleled capacitors, giving a maximum per-device charge of $\hat{Q}_{HF,max} = 2.5\,\mu\text{C}$ (dotted line in cf., **Fig. A.17b.i**). The measured switching-frequency charge ripple amplitude nicely follows this theoretical prediction.

Using the SE parameters from **Sec. A.4.1** ($k = 1.06{\cdot}10^6$, $\alpha = 1$, $\beta = 2.12$), the low- and HF losses for S_1 and S_2 can be calculated from the charge predictions above. In S_1 and S_2, the calculated line-frequency losses are 450 mW, and the time-varying HF losses in S_1 peak at 173 mW with an average value $\bar{P}_{HF}$ of 64 mW (**Fig. A.17b.ii**). The transient calorimetric measurement approach of **Sec. A.4.4** is used to measure the losses (which cannot be accurately measured with the Sawyer-Tower circuit with the low- *and* HF excitations, as discussed in **Sec. A.4.5**).

Fig. A.17c.i shows the temperature rise of the capacitors, which is translated into instantaneous power loss (**Fig. A.17c.ii**) with (A.15) and the thermal equivalent circuit parameters from **Sec. A.4.4**. The measured losses in S_2 are 459 mW, predicted with an error under 2 %. The HF losses are indeed negligible in this stage. For the capacitor of S_1, the measured losses increase by 122 mW over the losses in S_2 due to the HF ripple. While the prediction of $\bar{P}_{\mathrm{HF}}$ is off by approximately a factor of two (64 mW predicted losses), the prediction error of total losses in S_1 is only 12 %, and the HF error can be partially explained by the reported increase of DF by 30 % at HF (**Fig. A.14b**). Non-ideal current sharing among the capacitors is also a potential error source.

Nonetheless, the HF losses of 122 mW are only 20 % of the overall losses, and clearly the LF loss component dominates in MLCCs for the considered sinewave filter with a small HF voltage ripple compared to the fundamental voltage waveform. For motor drives with fundamental frequencies up to 200 Hz to 300 Hz, this ratio may be even more tilted towards the LF losses, The total loss approximation error for S_1 is under 12 %, validating the measurements, the iGSE-C model, and the charge estimation approaches in this work.

A.6 Conclusions

Ferroelectric Class II Multilayer Ceramic Capacitors (MLCCs) promise large volume reductions in inverter and rectifier sinewave filters, and are expected to gain importance in future applications demanding exceptional power density. While prior work has found non-linear and large losses in these components, no extensible loss model is available in the literature that accurately describes these hysteretic losses.

In this work, a Steinmetz-based loss modelling approach – called the improved Generalized Steinmetz Equation for Ceramic Capacitors, or iGSE-C – is proposed and verified for a commercially-available X7R MLCC. We measure the ferroelectric hysteresis losses across AC excitation magnitude, DC bias, frequency, temperature, and harmonic injection using the Sawyer-Tower circuit.

Losses are shown to scale according to a power law with peak charge, with the Steinmetz coefficients constant over DC bias. By analogy with well-developed methods for ferro*magnetic* components in power electronics applications, the iGSE-C accurately predicts losses under non-sinusoidal voltage excitations, as long as the charge is accurately characterized or measured.

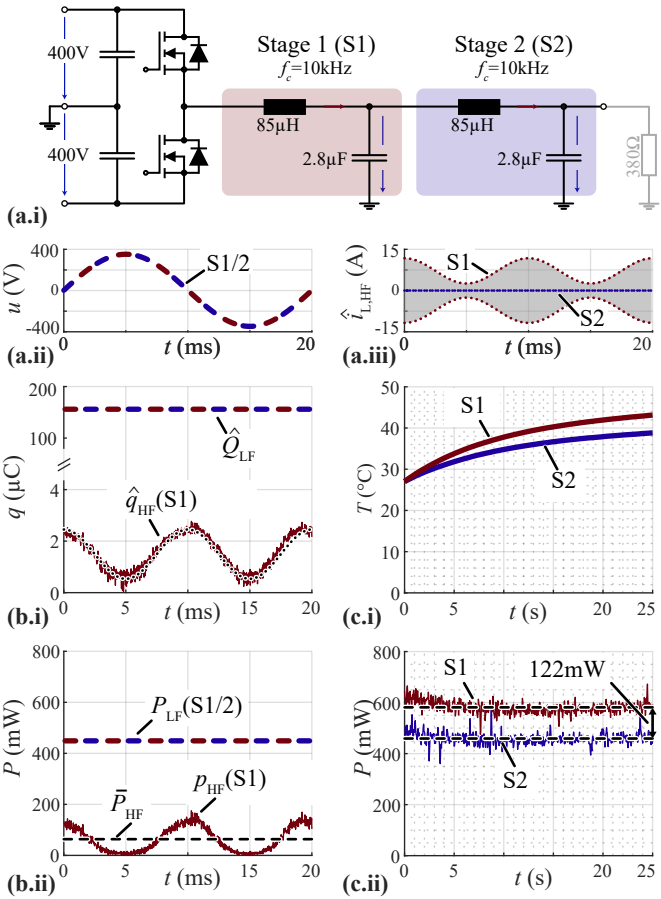

Fig. A.17: (a.i) Example of single-phase DC/AC converter with a split 800 V DC-link and a 50 Hz, 250 V_{rms} AC voltage. The output sinewave filter consists of two identical filter stages, where only the first filter stage S_1 is subject to a substantial HF excitation. Calculated **(a.ii)** LF AC voltage waveforms of the capacitors in S_1 and S_2 and **(a.iii)** calculated HF envelope of the S_1 inductor current. **(b.i)** calculated (dashed line) LF charge excitation of S_1 and S_2 as well as the time-varying HF charge waveforms of S_1 on top of the measured peak charge values. **(b.ii)** Calculated LF and HF capacitor losses using the measured charge excitation and the SE parameters from **Sec. A.4.1**. **(c.i)** Measured capacitor transient temperature curves of S_1 and S_2 during converter operation. **(c.ii)** Calculated capacitor losses (average values represented as dashed lines) from the transient thermal measurements of **(c.i)** with (A.15) and the thermal equivalent circuit parameters from **Sec. A.4.4**.

Finally, a procedure is given and validated for predicting total losses – the sum of LF and HF losses – in a sinewave filter, with the LF losses dominating the total power dissipation in the MLCCs.

Bibliography

[1] E. Delyannis, "Historic background of desalination and renewable energies," *Solar Energy*, vol. 75, no. 5, pp. 357–366, 2003, DOI: 10.1016/j.solener.2003.08.002.

[2] T. S. Reynolds, *Stronger than a hundred men: A history of the vertical water wheel*. JHU Press, 1983, vol. 7, accessed: 23.12.2021. [Online]. Available: https://books.google.so/books?id=aZ0runvrq0AC&lpg=PR6&hl=de&pg=PA128#v=onepage&q&f=false

[3] L. Sun, B. Zhang, T.-Y. Lin, and Z. Zhang, "An investigation and reconstruction of traditional vertical-axle-styled "chinese great windmill" and its square-pallet chain-pump," in *Proc. of the International Symposium on History of Machines and Mechanisms*. Springer, Nov. 2009, pp. 295–308, DOI: 10.1007/978-1-4020-9485-9.

[4] M. Mende, "Energie, Verkehr, Infrastruktur: Frühindustrielle Antriebstechnik - Wind- und Wasserkraft," in *Technik und Wirtschaft*, U. Wengenroth, Ed. Springer Berlin Heidelberg, 1993, pp. 287–539, DOI: 10.1007/978-3-642-95794-9.

[5] J. Perlin, "Silicon solar cell turns 50," *National Renewable Energy Laboratory (NREL) Report No. BR-520-33947*, 2004. [Online]. Available: https://www.osti.gov/biblio/15009471

[6] H. Donella, D. L. Meadows, J. Randers, and W. W. Behrens III, *The limits to growth*. New York: Universe Books, 1972.

[7] "Statistical review of world energy," British Petroleum Company (BP), 2021. [Online]. Available: https://www.bp.com

[8] P. Collier and A. J. Venables, "Closing coal: Economic and moral incentives," *Oxford Review of Economic Policy*, vol. 30, no. 3, pp. 492–512, 2015, DOI: 10.1093/oxrep/gru024.

[9] G. A. Edwards, "Coal and climate change," *Wiley Interdisciplinary Reviews: Climate Change*, vol. 10, no. 5, p. e607, 2019, DOI: 10.1002/wcc.607.

[10] M. D. Delis, K. de Greiff, and S. Ongena, "Being stranded with fossil fuel reserves? Climate policy risk and the pricing of bank loans," *Swiss Finance Institute Research Paper*, no. 18-10, 2019, DOI: 10.2139/ssrn.3125017.

[11] "Our world in data: Energy," Hannah Ritchie and Max Roser, 2020, accessed: 23.12.2021. [Online]. Available: https://ourworldindata.org/energy

[12] "Renewable power," International Energy Agency (IEA), Nov. 2021, accessed: 23.12.2021. [Online]. Available: https://www.iea.org/reports/renewable-power

[13] "Renewable power generation costs," International Renewable Energy Agency (IRENA), Jun. 2021, accessed: 23.12.2021. [Online]. Available: https://www.irena.org/publications/2021/Jun/Renewable-Power-Costs-in-2020

[14] "Optimal flexibility portfolios for a high-RES 2050 scenario: METIS Studies: Study S1," European Commission and Directorate-General for Energy, 2019, DOI: 10.2833/642476.

[15] I. Batarseh and K. Alluhaybi, "Emerging opportunities in distributed power electronics and battery integration: Setting the stage for an energy storage revolution," *IEEE Power Electronics Magazine*, vol. 7, no. 2, pp. 22–32, 2020, DOI: 10.1109/MPEL.2020.2987114.

[16] "World energy outlook 2017," International Energy Agency (IEA), Nov. 2017, accessed: 29.12.2021. [Online]. Available: https://www.iea.org/reports/world-energy-outlook-2017

[17] "Energy efficiency - Motors and drives infographics (3AUA0000182864)," ABB, Dec. 2018, accessed: 23.12.2021. [Online]. Available: https://library.abb.com

[18] N. Soulopoulos, "When will electric vehicles be cheaper than conventional vehicles?" Bloomberg New Energy Finance (NEF), 2017, accessed: 05.01.2022. [Online]. Available: https://about.bnef.com/blog/electric-cars-reach-price-parity-2025/

[19] "Electric vehicle outlook 2019," Bloomberg New Energy Finance (NEF), 2019, accessed: 05.01.2022. [Online]. Available: https://legacy-assets.eenews.net/open_files/assets/2019/05/15/document_ew_02.pdf

[20] "Net zero by 2050 - A roadmap for the global energy sector," International Energy Agency (IEA), May 2021, accessed: 23.12.2021. [Online]. Available: https://www.iea.org/reports/net-zero-by-2050

[21] B. K. Bose, "Global energy scenario and impact of power electronics in 21st century," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2638–2651, 2013, DOI: 10.1109/TIE.2012.2203771.

[22] "Power electronics: Revolutionizing the world's future energy systems," Hitachi ABB Power Grids, Aug. 2021, accessed: 23.12.2021. [Online]. Available: https://library.abb.com

[23] L. Tolbert, T. King, B. Ozpineci, J. Campbell, G. Muralidharan, D. Rizy, A. Sabau, H. Zhang, W. Zhang, Y. Xu *et al.*, "ORNL/TM-2005/230: Power electronics for distributed energy systems and transmission and distribution applications," Oak Ridge National Laboratory, Tech. Rep., 2005, DOI: 10.2172/885985.

[24] I. C. Kizilyalli, E. P. Carlson, D. W. Cunningham, J. S. Manser, Y. A. Xu, and A. Y. Liu, "Wide band-gap semiconductor based power electronics for energy efficiency," USDOE Advanced Research Projects Agency-Energy (ARPA-E), Tech. Rep., 2018, DOI: 10.2172/1464211.

[25] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2014, DOI: 10.1109/TPEL.2013.2268900.

[26] M. Randall, "A brief introduction to high voltage SMT capacitors," Venkel LTD., Tech. Rep. 035002 A4, 2007, accessed: 28.12.2021. [Online]. Available: https://resources.venkel.com/whitepaper-a-brief-introduction-to-high-voltage-ceramic-capacitors/

[27] A. J. Hanson, J. A. Belk, S. Lim, C. R. Sullivan, and D. J. Perreault, "Measurements and performance factor comparisons of magnetic materials at high frequency," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7909–7925, 2016, DOI: 10.1109/TPEL.2015.2514084.

[28] J. W. Kolar and J. E. Huber, "X-technologies driving power electronics 4.0," Keynote presentation at the IEEE Power Electronics and Motion Control Conference (EPE-PEMC), Apr. 2021, accessed: 23.12.2021.

[29] A. Stippich, C. H. van der Broeck, A. Sewergin, A. H. Wienhausen, M. Neubert, P. Schülting, S. Taraborrelli, H. van Hoek, and R. W. De Doncker, "Key components of modular propulsion systems for next generation electric vehicles," *CPSS Transactions on Power Electronics*

and Applications, vol. 2, no. 4, pp. 249–258, 2017, DOI: 10.24295/CPSST-PEA.2017.00023.

[30] G. Pistoia and B. Liaw, *Behaviour of lithium-ion batteries in electric vehicles: Battery health, performance, safety, and cost.* Springer, 2018, DOI: 10.1007/978-3-319-69950-9.

[31] J. Larminie, A. Dicks, and M. S. McDonald, *Fuel cell systems explained.* John Wiley & Sons, 2003, vol. 2, DOI: 10.1002/9781118878330.

[32] M. Mohr, W. T. Franke, B. Wittig, and F. W. Fuchs, "Converter systems for fuel cells in the medium power range — A comparative study," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 6, pp. 2024–2032, 2010, DOI: 10.1109/TIE.2010.2044730.

[33] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Transactions on Industry Applications*, vol. 32, no. 2, pp. 250–259, 1996, DOI: 10.1109/28.491472.

[34] J. W. Kolar, J. Azurza Anderson, S. Mirić, M. Haider, M. Guacci, M. Antivachis, G. Zulauf, D. Menzi, P. S. Niklaus, J. Miniböck, P. Papamanolis, G. Rohner, N. Nain, D. Cittanti, and D. Bortis, "Application of WBG power devices in future 3-Φ variable speed drive inverter systems – "How to handle a double-edged sword"," in *Proc. of the IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, pp. 27.7.1–27.7.4, DOI: 10.1109/IEDM13553.2020.9372022.

[35] J. Guzinski, H. Abu-Rub, and P. Strankowski, *Variable Speed AC Drives with Inverter Output Filters.* Wiley, 2015, DOI: 10.1002/9781118782989.

[36] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kV SiC-based 7 kV/400 V DC transformer for future data centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753–767, 2019, DOI: 10.1109/JESTPE.2018.2886139.

[37] China Grid, "Electric vehicle charging equipment supplier qualification verification standard," 2017.

[38] CHARIN, "DC CCS power classes for conformance tests," *CharIN e.V.*, Jun. 2018, accessed: 29.12.2021. [Online]. Available: https://www.charinev.org/ccs-at-a-glance/ccsspecification

[39] D. Zhang, M. Guacci, M. Haider, D. Bortis, J. W. Kolar, and J. Everts, "Three-phase bidirectional buck-boost current DC-link EV battery charger featuring a wide output voltage range of 200 to 1000V," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Oct. 2020, pp. 4555–4562, DOI: 10.1109/ECCE44975.2020.9235868.

[40] M. Falahi, H.-M. Chou, M. Ehsani, L. Xie, and K. L. Butler-Purry, "Potential power quality benefits of electric vehicles," *IEEE Transactions on Sustainable Energy*, vol. 4, no. 4, pp. 1016–1023, 2013, DOI: 10.1109/TSTE.2013.2263848.

[41] A. Darwish, D. Holliday, S. Ahmed, A. M. Massoud, and B. W. Williams, "A single-stage three-phase inverter based on Cuk converters for PV applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 797–807, 2014, DOI: 10.1109/JESTPE.2014.2313185.

[42] R. Inzunza, R. Okuyama, T. Tanaka, and M. Kinoshita, "Development of a 1500Vdc photovoltaic inverter for utility-scale PV power plants," in *Proc. of the IEEE International Future Energy Electronics Conference (IFEEC)*, Nov. 2015, pp. 1–4, DOI: 10.1109/IFEEC.2015.7361615.

[43] M. Tampubolon, W.-C. Lin, J.-Y. Lin, Y.-C. Hsieh, H.-J. Chiu, K. Yamanaka, and M. Hojo, "A study and implementation of three-level boost converter with MPPT for PV application," in *Proc. of the IEEE International Future Energy Electronics Conference (IFEEC - ECCE Asia)*, Jun. 2017, pp. 1143–1148, DOI: 10.1109/IFEEC.2017.7992202.

[44] "Tracking data centres and data transmission networks 2020," International Energy Agency (IEA), Jun. 2020, accessed: 06.02.2022. [Online]. Available: https://www.iea.org/reports/tracking-data-centres-and-data-transmission-networks-2020

[45] A. Pratt, P. Kumar, and T. V. Aldridge, "Evaluation of 400V DC distribution in telco and data centers to improve energy efficiency," in *Proc. of the International Telecommunications Energy Conference (INTELEC)*, Sep. 2007, pp. 32–39, DOI: 10.1109/INTLEC.2007.4448733.

[46] D. Menzi, M. Zhang, J. W. Kolar, and J. Everts, "3-Φ bidirectional buck-boost sinusoidal input current three-level SiC Y-rectifier," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Jun. 2021, pp. 590–598, DOI: 10.1109/APEC42165.2021.9487220.

[47] J. W. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems—Part I," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 176–198, 2013, DOI: 10.1109/TPEL.2012.2197867.

[48] G. Buja and G. Indri, "Improvement of pulse width modulation techniques," *Archiv für Elektrotechnik*, vol. 57, no. 5, pp. 281–289, Sep. 1975, DOI: 10.1007/BF01476709.

[49] J. A. Houldsworth and D. A. Grant, "The use of harmonic distortion to increase the output voltage of a three-phase PWM inverter," *IEEE Transactions on Industry Applications*, vol. IA-20, no. 5, pp. 1224–1228, 1984, DOI: 10.1109/TIA.1984.4504587.

[50] T. Friedli, S. D. Round, D. Hassler, and J. W. Kolar, "Design and performance of a 200-kHz all-SiC JFET current DC-link back-to-back converter," *IEEE Transactions on Industry Applications*, vol. 45, no. 5, pp. 1868–1878, 2009, DOI: 10.1109/TIA.2009.2027538.

[51] H. Dai, T. M. Jahns, R. A. Torres, D. Han, and B. Sarlioglu, "Comparative evaluation of conducted common-mode EMI in voltage-source and current-source inverters using wide-bandgap switches," in *Proc. of the IEEE Transportation Electrification Conference and Expo (ITEC)*, Jun. 2018, pp. 788–794, DOI: 10.1109/ITEC.2018.8450157.

[52] H. Dai and T. M. Jahns, "Comparative investigation of PWM current-source inverters for future machine drives using high-frequency wide-bandgap power switches," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2018, pp. 2601–2608, DOI: 10.1109/APEC.2018.8341384.

[53] T. Nussbaumer and J. W. Kolar, "Comparison of 3-phase wide output voltage range PWM rectifiers," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3422–3425, 2007, DOI: 10.1109/TIE.2007.896525.

[54] J.-M. Kwon, B.-H. Kwon, and K.-H. Nam, "Three-phase photovoltaic system with three-level boosting MPPT control," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2319–2327, 2008.

[55] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2151–2169, 2013, DOI: 10.1109/TPEL.2012.2212917.

[56] K. D. T. Ngo, "Topology and analysis in PWM inversion, rectification, and cycloconversion," Ph.D. dissertation, California Institute of Technology, 1984, DOI: 10.7907/M91H-FZ91.

[57] M. Guacci, D. Zhang, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, and H. Ishida, "Three-phase two-third-PWM buck-boost current source inverter system employing dual-gate monolithic bidirectional GaN e-FETs," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 4, pp. 339–354, 2019.

[58] M. Antivachis, D. Bortis, L. Schrittwieser, and J. W. Kolar, "Three-phase buck-boost Y-inverter with wide DC input voltage range," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2018, DOI: 10.1109/APEC.2018.8341214.

[59] P. R. Tripathi, P. Thakura, R. K. Keshri, S. Ghosh, and J. M. Guerrero, "25 years of single-stage buck-boost inverters: Development and challenges," *IEEE Industrial Electronics Magazine*, early access, Feb. 2021, DOI: 10.1109/MIE.2021.3050135.

[60] F. Z. Peng, "Z-source inverter," *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504–510, 2003.

[61] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1453–1463, 2007, DOI: 10.1109/TPEL.2007.900505.

[62] F. Barzegar and S. Cuk, "A new switched-mode amplifier produces clean three-phase power," in *Proc. of the International Solid-State Power Conversion Conference*, 1982, p. E3.

[63] C. Cecati, A. Dell'Aquila, and M. Liserre, "A novel three-phase single-stage distributed power inverter," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1226–1233, 2004, DOI: 10.1109/TPEL.2004.835112.

[64] M. Antivachis, D. Bortis, D. Menzi, and J. W. Kolar, "Comparative evaluation of Y-inverter against three-phase two-stage buck-boost DC-AC converter systems," in *Proc. of the IEEE International Power Electronics Conference (IPEC - ECCE Asia)*, May 2018, pp. 181–189, DOI: 10.23919/IPEC.2018.8507664.

[65] S. Nino, "Reversible buck-boost chopper circuit, and inverter circuit with the same," 2005, US Patent 7088595 B2. [Online]. Available: https://patents.google.com/patent/US7088595B2/en

[66] N. Elsayad, A. Berzoy, and O. A. Mohammed, "An integrated PEBB using e-GaN FETs and nanocrystalline inductors for multiple DC-DC, AC-DC and DC-AC applications," in *Proc. of the IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov. 2017, pp. 67–73, DOI: 10.1109/WiPDA.2017.8170524.

[67] M. Antivachis, N. Kleynhans, and J. W. Kolar, "Three-phase sinusoidal output buck-boost GaN Y-inverter for advanced variable speed AC drives," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, Sep. 2020, DOI: 10.1109/JESTPE.2020.3026742.

[68] D. Elizondo and A. Urtasun, "Dual-mode soft-transition control for single-phase grid-connected photovoltaic inverters," in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2018, pp. 1–6, DOI: 10.1109/COMPEL.2018.8459930.

[69] A. A. Khan, H. Cha, H. F. Ahmed, J. Kim, and J. Cho, "A highly reliable and high-efficiency quasi single-stage buck–boost inverter," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4185–4198, 2017, DOI: 10.1109/TPEL.2016.2598251.

[70] W. Wu, J. Ji, and F. Blaabjerg, "Aalborg inverter - A new type of "buck in buck, boost in boost" grid-tied inverter," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 4784–4793, 2015, DOI: 10.1109/TPEL.2014.2363566.

[71] R. Ridley, S. Kern, and B. Fuld, "Analysis and design of a wide input range power factor correction circuit for three-phase applications," in *Proc. of the IEEE Annual Applied Power Electronics Conference and Exposition (APEC)*, Mar. 1993, pp. 299–305, DOI: 10.1109/APEC.1993.290616.

[72] F. Alsokhiry, I. Abdelsalam, G. P. Adam, and Y. Al-Turki, "High-power medium-voltage three-phase AC–DC buck–boost converter for wind energy conversion systems," *Electric Power Systems Research*, vol. 177, p. 106012, 2019, DOI: 10.1016/j.epsr.2019.106012.

[73] D. Tekgun, B. Tekgun, and I. Alan, "A modular three-phase buck-boost motor drive topology," in *Proc. of the IEEE International Conference*

on Electric Power and Energy Conversion Systems (EPECS), 2020, pp. 130–135, DOI: 10.1109/EPECS48981.2020.9304972.

[74] L. Hernandez, "Etude et réalisation d'un convertisseur AC/DC buck boost réversible à haut rendement pour alimentation de secours," Ph.D. dissertation, Institut National Polytechnique de Toulouse, 2017, accessed: 30.12.2021. [Online]. Available: https://oatao.univ-toulouse.fr/20732/

[75] D. Menzi, D. Bortis, and J. W. Kolar, "A new bidirectional three-phase phase-modular boost-buck AC/DC converter," in *Proc. of the IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Nov. 2018, pp. 1–8, DOI: 10.1109/PEAC.2018.8590670.

[76] S.-Y. Kim and K.-H. Nam, "Three phase inverter system utilizing three bi-directional buck-boost converter," in *Proc. of the Conference of the Korean Society for New and Renewable Energy*, 2006, pp. 551–554.

[77] M. S. Diab, A. Elserougi, A. S. Abdel-Khalik, I. F. ElArabawy, A. M. Massoud, and S. Ahmed, "Non-linear sliding-mode control of three-phase buck-boost inverter," in *Proc. of the IEEE International Symposium on Industrial Electronics (ISIE)*, Jun. 2014, pp. 600–605, DOI: 10.1109/ISIE.2014.6864680.

[78] V. Melo, A. Melo, W. Santos, J. Fardin, and L. Encarnação, "Open-loop single-phase space state model and equivalent circuit of a non-conventional three-phase inverter," *Electronics*, vol. 9, no. 5, p. 744, Apr. 2020, DOI: 10.3390/electronics9050744.

[79] X. Li, Z. Yan, Y. Gao, H. Qi *et al.*, "The research of three-phase boost/buck-boost DC-AC inverter," *Energy and Power Engineering*, vol. 5, no. 04, p. 906, 2013, DOI: 10.4236/epe.2013.54B174.

[80] A. Darwish, A. M. Massoud, D. Holliday, S. Ahmed, and B. W. Williams, "Single-stage three-phase differential-mode buck-boost inverters with continuous input current for PV applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8218–8236, 2016, DOI: 10.1109/TPEL.2016.2516255.

[81] Y. Nishida, "A new buck-and-boost DC-DC converter (Tokusada converter)," in *Proc. of the IEEE European Conference on Power Electronics and Applications (EPE)*, Sep. 2003.

[82] "European Center for Power Electronics e.V. (ECPE)," www.ecpe.org, accessed: 23.12.2021.

[83] J. Luszcz, *High Frequency Conducted Emission in AC Motor Drives Fed by Frequency Converters: Sources and Propagation Paths*. Wiley, 2018, DOI: 10.1002/9781119388975te.

[84] *Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods*, IEC Std. 61 800-3, Feb. 2017.

[85] F. J. Ferreira and A. T. de Almeida, "Reducing energy costs in electric-motor-driven systems: Savings through output power reduction and energy regeneration," *IEEE Industry Applications Magazine*, vol. 24, no. 1, pp. 84–97, 2018, DOI: 10.1109/MIAS.2016.2600685.

[86] S. Puls, J. Hegerfeld, J. Austermann, and H. Borcherding, "Transient overvoltage protection solutions for drive inverters operating on an open industrial DC grid," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*, Jul. 2020, pp. 1–8.

[87] D. Meike and I. Rankis, "New type of power converter for common-ground DC bus sharing to increase the energy efficiency in drive systems," in *Proc. of the IEEE International Energy Conference and Exhibition (ENERGYCON)*, Sep. 2012, pp. 225–230.

[88] J. O. Krah, N. Sieweke, C. Klarenbach, M. Hoeltgen, and D. Langhals, "Smart supercapacitor based DC-link extension for drives offers UPS capability and acts as an energy efficient line regeneration replacement," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*, May 2016, pp. 1–8.

[89] *Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement*, IEC Std. 55 011, Feb. 2016.

[90] N. Hanigovszki, J. Landkildehus, G. Spiazzi, and F. Blaabjerg, "An EMC evaluation of the use of unshielded motor cables in AC adjustable speed drive applications," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 273–281, 2006, DOI: 10.1109/TPEL.2005.861182.

[91] "Tech note: Understanding cable stress and failure in high flex applications," W. L. Gore & Associates, Inc., accessed: 23.12.2021. [Online]. Available: https://www.gore.com/resources/tech-note-understanding-cable-stress-and-failure-high-flex-applications

[92] J. Dobusch, D. Kuebrich, T. Duerbaum, and F. Diepold, "Implementation of current based three-phase CM/DM noise separation on the drive side," in *Proc. of the IEEE International Symposium on Electromagnetic Compatibility (EMC EUROPE)*, Aug. 2018, pp. 220–225.

[93] E. J. Bulington, S. Abney, and G. L. Skibinski, "Cable alternatives for PWM AC drive applications," in *Proc. of the IEEE IAS Petroleum and Chemical Technical Conference (PCIC)*, Sep. 1999, pp. 247–259, DOI: 10.1109/PCICON.1999.806443.

[94] L. A. Saunders, G. L. Skibinski, S. T. Evon, and D. L. Kempkes, "Riding the reflected wave - IGBT drive technology demands new motor and cable considerations," in *Proc. of the IEEE IAS Petroleum and Chemical Industry Technical Conference (PCIC)*, Sep. 1996, pp. 75–84, DOI: 10.1109/PCICON.1996.564866.

[95] S. Chen, T. A. Lipo, and D. Fitzgerald, "Modeling of motor bearing currents in PWM inverter drives," *IEEE Transactions on Industry Applications*, vol. 32, no. 6, pp. 1365–1370, 1996, DOI: 10.1109/28.556640.

[96] M. Fuerst and M. Bakran, "An advanced filtering method for partial discharge measurement in the presence of high dv/dt," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*, May 2019, pp. 1–7.

[97] B. Zhang and S. Wang, "A survey of EMI research in power electronics systems with wide-bandgap semiconductor devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 626–643, 2020, DOI: 10.1109/JESTPE.2019.2953730.

[98] P. T. Finlayson, "Output filters for PWM drives with induction motors," *IEEE Industry Applications Magazine*, vol. 4, no. 1, pp. 46–52, 1998, DOI: 10.1109/2943.644886.

[99] J. K. Steinke, "Use of an LC filter to achieve a motor-friendly performance of the PWM voltage source inverter," *IEEE Transactions on Energy Conversion*, vol. 14, no. 3, pp. 649–654, 1999, DOI: 10.1109/60.790930.

[100] N. Hanigovszki, J. Landkildehus, and F. Blaabjerg, "Output filters for AC adjustable speed drives," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2007, pp. 236–242, DOI: 10.1109/APEX.2007.357520.

[101] D. A. Rendusara and P. Enjeti, "New inverter output filter configuration reduces common mode and differential mode dv/dt at the motor terminals in PWM drive systems," in *Proc. of the IEEE Power Electronics Specialists Conference (PESC)*, vol. 2, Jun. 1997, pp. 1269–1275 vol.2, DOI: 10.1109/PESC.1997.616929.

[102] D. A. Rendusara and P. N. Enjeti, "An improved inverter output filter configuration reduces common and differential modes dv/dt at the motor terminals in PWM drive systems," *IEEE Transactions on Power Electronics*, vol. 13, no. 6, pp. 1135–1143, 1998, DOI: 10.1109/63.728340.

[103] H. Akagi and T. Shimizu, "Attenuation of conducted EMI emissions from an inverter-driven motor," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 282–290, 2008, DOI: 10.1109/TPEL.2007.911878.

[104] F. Maislinger, H. Ertl, G. Stojcic, C. Lagler, and F. Holzner, "Design of a 100 kHz wide bandgap inverter for motor applications with active damped sine wave filter," *The Journal of Engineering*, no. 17, pp. 3766–3771, 2019, DOI: 10.1049/joe.2018.8059.

[105] K. Shirabe, M. Swamy, J. K. Kang, M. Hisatsune, Y. Wu, D. Kebort, and J. Honea, "Advantages of high frequency PWM in AC motor drive applications," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Sep. 2012, pp. 2977–2984, DOI: 10.1109/ECCE.2012.6342519.

[106] M. M. Swamy, J. Kang, and K. Shirabe, "Power loss, system efficiency, and leakage current comparison between Si IGBT VFD and SiC FET VFD with various filtering options," *IEEE Transactions on Industry Applications*, vol. 51, no. 5, pp. 3858–3866, 2015, DOI: 10.1109/TIA.2015.2420616.

[107] N. Mukherjee, J. Fuerst, F. Diepold, and F. A. Vega, "900 V GaN-based sine-wave inverters for three-phase industrial applications," in *Proc. of the International Conference on Power Electronics, Machines and Drives (PEMD)*, vol. 2019, no. 17, Apr. 2019, pp. 3754–3759, DOI: 10.1049/joe.2018.8032.

[108] H. Bishnoi, P. Mattavelli, R. P. Burgos, and D. Boroyevich, "EMI filter design of DC-fed motor-drives using behavioral EMI models," in *Proc.*

of the IEEE European Conference on Power Electronics and Applications (EPE - ECCE Europe), Sep. 2015, pp. 1–10, DOI: 10.1109/EPE.2015.7309155.

[109] X. Zhang, D. Boroyevich, P. Mattavelli, J. Xue, and F. Wang, "EMI filter design and optimization for both AC and DC side in a DC-fed motor drive system," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2013, pp. 597–603, DOI: 10.1109/APEC.2013.6520271.

[110] C. Jettanasen and A. Ngaopitakkul, "Minimization of common-mode conducted noise in PWM inverter-fed AC motor drive systems using optimized passive EMI filter," in *Proc. of the International Multi-Conference of Engineers and Computer Scientists (IMECS)*, vol. 2, Mar. 2010, pp. 1249–1252, DOI: 10.1063/1.3510569.

[111] F. Maislinger, H. Ertl, G. Stojcic, and F. Holzner, "Efficiency and motor-performance improvement using WBG-inverters with observer-based actively damped LC-sine wave filters," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*. VDE, May 2019, pp. 1–9.

[112] K. Taniguchi, Y. Ogino, and H. Irie, "PWM technique for power MOSFET inverter," *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 328–334, 1988, DOI: 10.1109/63.17951.

[113] M. Antivachis, P. Niklaus, D. Bortis, and J. W. Kolar, "Input / output EMI filter design for three-phase ultra-high speed motor drive GaN inverter stage," *IEEE CPSS Transactions on Power Electronics and Applications*, vol. 6, no. 1, pp. 74–92, 2021, DOI: 10.24295/CPSSTPEA.2021.00007.

[114] H. Bishnoi, P. Mattavelli, R. Burgos, and D. Boroyevich, "EMI behavioral models of DC-fed three-phase motor drive systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4633–4645, 2014, DOI: 10.1109/TPEL.2013.2284436.

[115] M. Moreau, N. Idir, and P. Le Moigne, "Modeling of conducted EMI in adjustable speed drives," *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 3, pp. 665–672, 2009, DOI: 10.1109/TEMC.2009.2025269.

[116] J. Dobusch, P. Konarski, D. Kuebrich, and T. Duerbaum, "Implementation of voltage based three-phase CM/DM noise separation on the

drive side," in *Proc. of the IEEE European Conference on Power Electronics and Applications (EPE - ECCE Europe)*, Sep. 2018, pp. 1–9.

[117] G. Grandi, D. Casadei, and U. Reggiani, "Common- and differential-mode HF current components in AC motors supplied by voltage source inverters," *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 16–24, 2004, DOI: 10.1109/TPEL.2003.820564.

[118] J. Luszcz, "Motor cable as an origin of supplementary conducted EMI emission of ASD," in *Proc. of the IEEE European Conference on Power Electronics and Applications (EPE - ECCE Europe)*, Sep. 2009, pp. 1–7.

[119] J. Luszcz, "Motor cable effect on the converter fed AC motor common mode current," in *Proc. of the IEEE International Conference-Workshop Compatibility and Power Electronics (CPE)*, Jun. 2011, pp. 445–450, DOI: 10.1109/CPE.2011.5942277.

[120] B. Revol, J. Roudet, J. Schanen, and P. Loizelet, "EMI study of three-phase inverter-fed motor drives," *IEEE Transactions on Industry Applications*, vol. 47, no. 1, pp. 223–231, 2011, DOI: 10.1109/TIA.2010.2091193.

[121] V. D. Santos, N. Roux, B. Revol, B. Sareni, B. Cougo, and J. Carayon, "Unshielded cable modeling for conducted emissions issues in electrical power drive systems," in *Proc. of the IEEE International Symposium on Electromagnetic Compatibility (EMC EUROPE)*, Sep. 2017, pp. 1–6, DOI: 10.1109/EMCEurope.2017.8094736.

[122] B. Cougo, H. H. Sathler, R. Riva, V. D. Santos, N. Roux, and B. Sareni, "Characterization of low-inductance SiC module with integrated capacitors for aircraft applications requiring low losses and low EMI issues," *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 8230–8242, 2021, DOI: 10.1109/TPEL.2020.3014529.

[123] C. M. Lundmark, E. O. A. Larsson, and M. H. J. Bollen, "Unintended consequences of limiting high-frequency emission by small end-user equipment," in *Proc. of the IEEE Power Engineering Society (PES) General Meeting*, vol. 6, Jun. 2006, DOI: 10.1109/PES.2006.1709476.

[124] J. R. Nicholson and J. A. Malack, "RF impedance of power lines and line impedance stabilization networks in conducted interference measurements," *IEEE Transactions on Electromagnetic Compatibility*, vol. EMC-15, no. 2, pp. 84–86, May 1973, DOI: 10.1109/TEMC.1973.303254.

[125] M. L. Heldwein, "EMC filtering of three-phase PWM converters," Ph.D. dissertation, ETH Zurich, 2008.

[126] M. Hartmann, H. Ertl, and J. W. Kolar, "EMI filter design for a 1 MHz , 10 kW three-phase/level PWM rectifier," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1192–1204, 2011, DOI: 10.1109/TPEL.2010.2070520.

[127] R. Zhang, X. Wu, and T. Wang, "Analysis of common mode EMI for three-phase voltage source converters," in *Proc. of the IEEE Power Electronics Specialist Conference (PESC)*, vol. 4, Jun. 2003, pp. 1510–1515, DOI: 10.1109/PESC.2003.1217683.

[128] D. O. Boillat, F. Krismer, and J. W. Kolar, "EMI filter volume minimization of a three-phase, three-level T-type PWM converter system," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2473–2480, 2017, DOI: 10.1109/TPEL.2016.2617085.

[129] A. Mallik, W. Ding, and A. Khaligh, "A comprehensive design approach to an EMI filter for a 6-kW three-phase boost power factor correction rectifier in avionics vehicular systems," *IEEE Transactions on Vehicular Technology*, vol. 66, no. 4, pp. 2942–2951, 2017, DOI: 10.1109/TVT.2016.2590462.

[130] T. Nussbaumer, M. L. Heldwein, and J. W. Kolar, "Differential mode input filter design for a three-phase buck-type PWM rectifier based on modeling of the EMC test receiver," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1649–1661, 2006, DOI: 10.1109/TIE.2006.881988.

[131] M. L. Heldwein, T. Nussbaumer, and J. W. Kolar, "Common mode modelling and filter design for a three-phase buck-type pulse width modulated rectifier system," *IET Power Electronics*, vol. 3, no. 2, pp. 209–218, Mar. 2010, DOI: 10.1049/iet-pel.2008.0342.

[132] K. Basu, A. K. Sahoo, V. Chandrasekaran, and N. Mohan, "Grid-side AC line filter design of a current source rectifier with analytical estimation of input current ripple," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6394–6405, 2014, DOI: 10.1109/TPEL.2014.2305435.

[133] L. Ran, S. Gokani, J. Clare, K. J. Bradley, and C. Christopoulos, "Conducted electromagnetic emissions in induction motor drive systems. I. Time domain analysis and identification of dominant modes," *IEEE*

Transactions on Power Electronics, vol. 13, no. 4, pp. 757–767, 1998, DOI: 10.1109/63.704152.

[134] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a simplified differential-mode EMI filter design," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 3, pp. 1031–1040, 2010, DOI: 10.1109/TIE.2009.2028293.

[135] A. Nagel and R. W. De Doncker, "Systematic design of EMI-filters for power converters," in *Proc. of the IEEE Industry Applications Society (IAS) Annual Meeting*, vol. 4, Oct. 2000, pp. 2523–2525, DOI: 10.1109/IAS.2000.883177.

[136] M. L. Heldwein and J. W. Kolar, "Design of minimum volume EMC input filters for an ultra compact three-phase PWM rectifier," in *Proc. of the Brazilian Power Electronic Conference (COBEP)*, Sep. 2007, pp. 454–461.

[137] D. Menzi, D. Bortis, G. Zulauf, M. Heller, and J. W. Kolar, "Novel iGSE-C loss modeling of X7R ceramic capacitors," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 367–13 383, 2020, DOI: 10.1109/TPEL.2020.2996010.

[138] F. Maislinger, H. Ertl, G. Stojcic, and L. Siplika, "Performance of a two-stage actively damped LC filter for GaN/SiC motor inverters," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (PEMC)*, Aug. 2018, pp. 177–183, DOI: 10.1109/EPEPEMC.2018.8521984.

[139] H. W. Ott, *Electromagnetic Compatibility Engineering*. John Wiley & Sons, 2011, DOI: 10.1002/9780470508510.

[140] C. R. Paul and D. R. Bush, "Radiated emissions from common-mode currents," in *Proc. of the IEEE International Symposium on Electromagnetic Compatibility*, Aug. 1987, pp. 1–7, DOI: 10.1109/ISEMC.1987.7570770.

[141] C. R. Paul, "A comparison of the contributions of common-mode and differential-mode currents in radiated emissions," *IEEE Transactions on Electromagnetic Compatibility*, vol. 31, no. 2, pp. 189–193, 1989, DOI: 10.1109/15.18789.

[142] Z. Vrankovic, G. L. Skibinski, and C. Winterhalter, "Novel double clamp methodology to reduce shielded cable radiated emissions initiated by electronic device switching," in *Proc. of the IEEE Energy Conversion*

Congress and Exposition (ECCE USA), Sep. 2015, pp. 4351–4360, DOI: 10.1109/ECCE.2015.7310275.

[143] S. Wang, F. C. Lee, D. Y. Chen, and W. G. Odendaal, "Effects of parasitic parameters on EMI filter performance," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 869–877, 2004, DOI: 10.1109/TPEL.2004.826527.

[144] R. Wang, H. F. Blanchette, M. Mu, D. Boroyevich, and P. Mattavelli, "Influence of high-frequency near-field coupling between magnetic components on EMI filter design," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4568–4579, 2013, DOI: 10.1109/TPEL.2012.2237414.

[145] A. T. De Almeida, F. J. Ferreira, and J. A. Fong, "Standards for efficiency of electric motors," *IEEE Industry Applications Magazine*, vol. 17, no. 1, pp. 12–19, 2010, DOI: 10.1109/MIAS.2010.939427.

[146] "Detailed inverter specifications, testing procedure, and technical approach and testing application requirements for the Little Box Challenge," Google, 2015, accessed: 29.12.2021. [Online]. Available: https://www.littleboxchallenge.com

[147] "Bearing currents in modern AC drive systems," ABB Drives, 2011, accessed: 29.12.2021. [Online]. Available: https://library.e.abb.com/

[148] J. Azurza Anderson, G. Zulauf, J. W. Kolar, and G. Deboy, "New figure-of-merit combining semiconductor and multi-level converter properties," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322–338, 2020, DOI: 10.1109/OJPEL.2020.3018220.

[149] "Energy-efficiency policy opportunities for electric motor-driven systems," International Energy Agency (IEA), May 2011, DOI: 10.1787/5kgg52gb9gjd-en.

[150] D. Menzi, D. Bortis, and J. W. Kolar, "EMI filter design for a three-phase buck–boost Y-inverter VSD with unshielded motor cables considering IEC 61800-3 conducted and radiated emission limits," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12 919–12 937, 2021, DOI: 10.1109/TPEL.2021.3075785.

[151] A. Abdulslam and P. P. Mercier, "A passive-stacked third-order buck converter with inherent input filtering achieving 0.7W/mm^2 power density and 94% peak efficiency," *IEEE Solid-State Circuits Letters*, vol. 2, no. 11, pp. 240–243, 2019, DOI: 10.1109/LSSC.2019.2935563.

[152] Z. Du, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, "DC–AC cascaded H-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications," *IEEE Transactions on Industry Applications*, vol. 45, no. 3, pp. 963–970, 2009.

[153] M. Pahlevaninezhad, P. Shangzhi, and P. Jain, "Zero voltage switching interleaved boost AC/DC converter," 2015, US Patent Application 20150194909 A1. [Online]. Available: https://patents.google.com/patent/US20150194909A1/en

[154] D. Rothmund, D. Bortis, J. Huber, D. Biadene, and J. W. Kolar, "10kV SiC-based bidirectional soft-switching single-phase AC/DC converter concept for medium-voltage solid-state transformers," in *Proc. of the IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2017, pp. 1–8, DOI: 10.1109/PEDG.2017.7972488.

[155] C. W. T. McLyman, *Magnetic core selection for transformers and inductors: A users's guide to practice and specification.* CRC Press, 1997, DOI: 10.1201/9781315214856.

[156] C. R. Sullivan, B. A. Reese, A. L. F. Stein, and P. A. Kyaw, "On size and magnetics: Why small efficient power inductors are rare," in *Proc. of the IEEE International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, Jun. 2016, pp. 1–23, DOI: 10.1109/3DPEIM.2016.7570571.

[157] J. Wang, Y. Zhang, M. Elshaer, W. Perdikakis, C. Yao, K. Zou, Z. Xu, and C. Chen, "Nonisolated electric vehicle chargers: Their current status and future challenges." *IEEE Electrification Magazine*, vol. 9, no. 2, pp. 23–33, 2021, DOI: 10.1109/MELE.2021.3070935.

[158] D. Menzi, J. W. Kolar, and J. Everts, "Single-phase full-power operable three-phase buck-boost Y-rectifier concepts," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Jun. 2021, pp. 599–606, DOI: 10.1109/APEC42165.2021.9487082.

[159] H. Zhang, H. Zhou, J. Ren, W. Liu, S. Ruan, and Y. Gao, "Three-phase grid-connected photovoltaic system with SVPWM current controller," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (PEMC)*, May 2009, pp. 2161–2164, DOI: 10.1109/IPEMC.2009.5157759.

[160] M. Salato, "VICOR company whitepaper: Datacenter power architecture," *Power Systems Design*, pp. 11–13, 2011. [Online]. Available: https://www.powersystemsdesign.com/articles/datacenter-power-architecture/32/6245

[161] W. Ng and A. Datta, "Hydrogen fuel cells and batteries for electric-vertical takeoff and landing aircraft," *Journal of Aircraft*, vol. 56, no. 5, pp. 1765–1782, 2019, DOI: 10.2514/1.C035218.

[162] S. Milad Tayebi, X. Chen, A. Bhattacharjee, and I. Batarseh, "Design and implementation of a dual-input LLC converter for PV-battery applications," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Sep. 2018, pp. 5934–5940, DOI: 10.1109/ECCE.2018.8557910.

[163] A. Trubitsyn, B. J. Pierquet, A. K. Hayman, G. E. Gamache, C. R. Sullivan, and D. J. Perreault, "High-efficiency inverter for photovoltaic applications," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Sep. 2010, pp. 2803–2810, DOI: 10.1109/ECCE.2010.5618163.

[164] A. A. Khan, H. Cha, and H. F. Ahmed, "A new reliable three-phase buck-boost AC–AC converter," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1000–1010, 2018, DOI: 10.1109/TIE.2017.2733439.

[165] T. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *European Power Electronics Journal (EPE)*, vol. 2, no. 1, pp. 45–50, 1992, DOI: 10.1080/09398368.1992.11463285.

[166] Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kW single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, 2017, DOI: 10.1109/TPEL.2017.2650140.

[167] R. Bosshard, "Multi-objective optimization of inductive power transfer systems for EV charging," Ph.D. dissertation, ETH Zurich, 2016.

[168] H. N. Tran, A. Castellazzi, S. Domae, T. Dong, and T. Nakamura, "Low-voltage-battery powered hybrid-GaN/SiC Y-inverter dual-rotor halbach motor drive for light electric vehicles," in *Proc. of the IEEE International Conference on Electrical Machines and Systems (ICEMS)*, 2021, pp. 699–704, DOI: 10.23919/ICEMS52562.2021.9634427.

[169] S. Waffler, "Hochkompakter DC/DC Wandler für Hybridfahrzeuge," Ph.D. dissertation, ETH Zurich, 2016.

[170] P. Papamanolis, D. Bortis, F. Krismer, D. Menzi, and J. W. Kolar, "New EV battery charger PFC rectifier front-end allowing full power delivery in 3-phase and 1-phase operation," *Electronics*, vol. 10, no. 17, 2021, DOI: 10.3390/electronics10172069.

[171] C. B. Barth, T. Foulkes, I. Moon, Y. Lei, S. Qin, and R. C. N. Pilawa-Podgurski, "Experimental evaluation of capacitors for power buffering in single-phase power converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7887–7899, 2019, DOI: 10.1109/TPEL.2018.2878825.

[172] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta - \rho$-Pareto optimization and comparative evaluation of inverter concepts considered for the Google Little Box Challenge," in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2016, pp. 1–5, DOI: 10.1109/COMPEL.2016.7556767.

[173] M.-J. Pan and C. A. Randall, "A brief introduction to ceramic capacitors," *IEEE Electrical Insulation Magazine*, vol. 26, no. 3, pp. 44–50, 2010, DOI: 10.1109/MEI.2010.5482787.

[174] A. Sheikholeslami and P. Gulak, "A survey of behavioral modeling of ferroelectric capacitors," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 44, no. 4, pp. 917–924, 1997, DOI: 10.1109/58.655207.

[175] I. Novak, K. B. Williams, R. Miller Jason, G. Blando, and N. Shannon, "DC and AC bias dependence of capacitors," in *Proc. of the DesignCon*, Jan. 2011, pp. 1–16.

[176] J. Kolar, H. Ertl, and F. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," *IEEE Transactions on Industry Applications*, vol. 27, no. 6, pp. 1063–1075, 1991, DOI: 10.1109/28.108456.

[177] D. Neumayr, D. Bortis, J. W. Kolar, M. Koini, and J. Konrad, "Comprehensive large-signal performance analysis of ceramic capacitors for power pulsation buffers," in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2016, pp. 1–8, DOI: 10.1109/COMPEL.2016.7556762.

[178] S. Coday, C. B. Barth, and R. C. Pilawa-Podgurski, "Characterization and modeling of ceramic capacitor losses under large signal operating conditions," in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2018, pp. 1–8, DOI: 10.1109/COMPEL.2018.8460142.

[179] L. E. Mosley, "Capacitor impedance needs for future microprocessors," in *Proc. of the ECA Symposium for Passive Components (CARTS)*, Apr. 2006, pp. 193–203.

[180] C. P. Steinmetz, "On the law of hysteresis," *Transactions of the American Institute of Electrical Engineers*, vol. IX, no. 1, pp. 1–64, 1892, DOI: 10.1109/T-AIEE.1892.5570437.

[181] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. of the IEEE Workshop on Computers in Power Electronics (CIPE)*, Jun. 2002, pp. 36–41, DOI: 10.1109/CIPE.2002.1196712.

[182] J. Goodenough, "Summary of losses in magnetic materials," *IEEE Transactions on Magnetics*, vol. 38, no. 5, pp. 3398–3408, 2002, DOI: 10.1109/TMAG.2002.802741.

[183] S. Ben-Yaakov, "Characterization of ferroelectric ceramic capacitors," in *Proc. of the IEEE European Conference on Power Electronics and Applications (EPE - ECCE Europe)*, Sep. 2018, pp. P.1–P.8.

[184] "Tech report: Equivalent series resistance (ESR) of capacitors," QuadTech, 2007, accessed: 23.12.2021. [Online]. Available: http://www.quadtech.com/app-notes.php

[185] J. F. Scott, "Ferroelectrics go bananas," *Journal of Physics: Condensed Matter*, vol. 20, no. 2, pp. 021 001–021 002, 2007, DOI: 10.1088/0953-8984/20/02/021001.

[186] G. Liu, S. Zhang, W. Jiang, and W. Cao, "Losses in ferroelectric materials," *Materials Science and Engineering: R: Reports*, vol. 89, pp. 1–48, 2015, DOI: 10.1016/j.mser.2015.01.002.

[187] S. Ben-Yaakov, "Some observations on loss and hysteresis of ferroelectric-based ceramic capacitors," *IEEE Transactions on*

Power Electronics, vol. 33, no. 11, pp. 9127–9129, 2018, DOI: 10.1109/TPEL.2018.2822771.

[188] J. Fedison and M. Harrison, "C_{oss} hysteresis in advanced super-junction MOSFETs," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 247–252, DOI: 10.1109/APEC.2016.7467880.

[189] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn, and J. Rivas-Davila, "C_{oss} losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 748–10 763, 2018, DOI: 10.1109/TPEL.2018.2800533.

[190] C. P. Steinmetz, *Lectures on Electrical Engineering*. Dover Phoenix Editions, Dover Publications, 2003, vol. 3.

[191] C. B. Sawyer and C. H. Tower, "Rochelle salt as a dielectric," *Physical Review*, vol. 35, pp. 269–273, Feb. 1930, DOI: 10.1103/PhysRev.35.269.

[192] L. E. Mosley and J. S. Schrader, "Hysteresis measurements of multi-layer ceramic capacitors using a Sawyer-Tower circuit," in *Proc. of the ECA Symposium for Passive Components (CARTS)*, Jan. 2007, pp. 285–295.

[193] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas-Davila, "Active power device selection in high-and very-high-frequency power converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6818–6833, 2018, DOI: 10.1109/TPEL.2018.2874420.

[194] M. S. Nikoo, A. Jafari, N. Perera, and E. Matioli, "Measurement of large-signal C_{oss} and C_{oss} losses of transistors based on nonlinear resonance," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2242–2246, 2019, DOI: 10.1109/TPEL.2019.2938922.

[195] J. M. Miller, C. W. Ayers, L. E. Seiber, and D. B. Smith, "Calorimeter evaluation of inverter grade metalized film capacitor ESR," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Sep. 2012, pp. 2157–2163, DOI: 10.1109/ECCE.2012.6342448.

[196] H. H. Race and S. C. Leonard, "Calorimetric measurement of dielectric losses in solids," *Electrical Engineering*, vol. 55, no. 12, pp. 1347–1356, 1936, DOI: 10.1109/EE.1936.6539235.

[197] L. Hoffmann, C. Gautier, S. Lefebvre, and F. Costa, "Optimization of the driver of GaN power transistors through measurement of their thermal behavior," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2359–2366, 2014, DOI: 10.1109/TPEL.2013.2277759.

[198] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10 kV SiC MOSFETs and diodes," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5240–5250, 2018, DOI: 10.1109/TPEL.2017.2729892.

[199] M. Guacci, J. A. Anderson, K. L. Pally, D. Bortis, J. W. Kolar, M. J. Kasper, J. Sanchez, and G. Deboy, "Experimental characterization of silicon and gallium nitride 200 V power semiconductors for modular/multi-level converters using advanced measurement techniques," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2019, DOI: 10.1109/JESTPE.2019.2944268.

[200] P. Papamanolis, T. Guillod, F. Krismer, and J. W. Kolar, "Transient calorimetric measurement of ferrite core losses," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2020, pp. 195–201, DOI: 10.1109/APEC39645.2020.9124132.

[201] A. Brockmeyer, "Experimental evaluation of the influence of DC-premagnetization on the properties of power electronic ferrites," in *Proc. of the IEEE Applied Power Electronics Conference (APEC)*, vol. 1, Mar. 1996, pp. 454–460, DOI: 10.1109/APEC39645.2020.9124132.

[202] J. Mühlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Core losses under the DC bias condition based on Steinmetz parameters," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 953–963, 2012, DOI: 10.1109/TPEL.2011.2160971.

[203] S. Coday and R. C. N. Pilawa-Podgurski, "High accuracy calorimetric measurements and modeling of ceramic capacitor losses under large ripple operation," in *Proc. of the IEEE Applied Power Electronics Conference (APEC)*, Mar. 2020, pp. 188–194, DOI: 10.1109/APEC39645.2020.9124490.

[204] R. M. Burkart, H. Uemura, and J. W. Kolar, "Optimal inductor design for 3-phase voltage-source PWM converters considering different magnetic materials and a wide switching frequency range," in *Proc. of the International Power Electronics Conference (IPEC - ECCE Asia)*, May 2014, pp. 891–898, DOI: 10.1109/IPEC.2014.6869693.

[205] W. G. Hurley and W. H. Wölfle, *Transformers and inductors for power electronics: Theory, design and applications.* John Wiley & Sons, 2013.

[206] J. T. Evans, "Characterizing ferroelectric materials," Tutorial at the IEEE International Symposium on Applications of Ferroelectrics (ISAF), pp. 1–123, Feb. 2010.

Curriculum Vitae

Personal Information

Name	David Menzi
Date of birth	July 26, 1992
Nationality	Swiss
Citizen of	Burgdorf, Switzerland
Contact	menzi@lem.ee.ethz.ch

Education

2022 –	Postdoctoral Researcher, ETH Zurich Power Electronic Systems Laboratory (PES)
2018 – 2022	Doctorate, ETH Zurich Power Electronic Systems Laboratory (PES)
2016 – 2018	Master's Degree (with distinction), ETH Zurich Information Technology and Electrical Engineering *– ETEL Master Award 2018* *– Ernst Blickle Studienpreis 2018*
2016	M.Sc. Studies (Exchange Semester), KTH Stockholm
2012 – 2016	Bachelor's Degree, ETH Zurich Information Technology and Electrical Engineering
2007 – 2011	High School, Burgdorf Physics and Applied Mathematics

Work Experience

2018 – 2022	Research Assistant Power Electronic Systems Laboratory (PES) ETH Zurich
2016 – 2017	Part Time Student Trainee Control Software Development ABB Medium Voltage Drives, Turgi
2015 – 2015	Internship (Four Months) Control Software Development ABB Medium Voltage Drives, Turgi
2013 – 2015	Course Assistant Digital Circuits / Networks and Circuits II ETH Zurich
2011 – 2012	Private First Class / Mandatory Military Service Swiss Armed Forces