A Time-Domain Readout Technique for Neural Interfaces Based on VCO-Timestamping

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Abstract— **CMOS neural interfaces are aimed at studying the electrical activity of neurons and may help to restore lost functions of the nervous system in the future. The central function of most neural interfaces is the detection of extracellular electrical potentials by means of numerous microelectrodes positioned in close vicinity to the neurons. Modern neural interfaces require compact low-power, low-noise readout circuits, capable of recording from thousands of electrodes simultaneously without excessive area consumption and heat dissipation. In this paper, we propose a novel readout technique for neural interfaces. The readout is based on a voltage-controlled oscillator (VCO), the frequency of which is modulated by the input voltage. The novelty of this work lies in the postprocessing of the VCO output, which is based on generating digital timestamps that contain temporal information about the oscillation. This method is potentially advantageous, because it requires mostly digital circuitry, which is more scalable than analog circuitry. Furthermore, most of the digital circuitry required for VCO-timestamping can be shared among several VCOs, rendering the architecture efficient for multi-channel architectures. This paper introduces the VCO-timestamping concept, including theoretical derivations and simulations, and presents measurements of a prototype fabricated in 0.18-μm CMOS technology. The measured input-referred noise in the 300 Hz – 5 kHz band was 5.7 μV$_{rms}$, and the prototype was able to detect pre-recorded extracellular action potentials.**

Index Terms—**ADC, CMOS, microelectrode array, neural interface, time domain, VCO-ADC.**

I. INTRODUCTION

Action potentials (APs) are voltage signals generated by electrogenic cells, such as cardiomyocytes or neurons, and result from transmembrane ionic currents. In the brain, APs are the main feature of neuronal information processing, and their study is key for progress in neuroscience and the development of treatments to restore lost functions. APs can be detected by placing small electrodes close to neurons, since the ionic transmembrane currents cause small electrical-potential variations in the extracellular medium adjacent to the cell membrane. The amplitude of these voltage variations, known as extracellular action potentials (EAPs), is typically smaller than 1 mVpp, with the majority of the signal power contained within the 300 Hz – 5 kHz band [1], [2].

Neural information processing involves a very large number of neurons, while electrophysiology tools have been traditionally limited in the number of electrodes that can be used in parallel. Over the last decades, CMOS technology has gained popularity for the implementation of active neural interfaces, enabling the recording from thousands of electrodes simultaneously [3]–[11]. The number of readout channels is typically limited by either power and heat dissipation, which may lead to tissue damage, or silicon real estate, which leads to increased fabrication costs and bulkier devices.

Analog circuitry typically consumes a significant part of the silicon area and overall power and requires considerable design efforts. Furthermore, designers tend to avoid deep submicron technologies to reduce manufacturing costs, since analog circuitry does not benefit from CMOS technology scaling [12]–[15]. Larger feature sizes also limit the performance of on-chip digital signal processing circuits, which are not efficient in old CMOS nodes, so that signal processing is frequently performed off chip. Voltage-controlled oscillator (VCO)-based analog-to-digital converters (ADCs) have emerged as area- and power-efficient alternatives to other to well-established architectures, such as successive-approximation-register (SAR) ADCs or classical delta-sigma (ΔΣ) modulators [16]–[26]. VCO-ADCs feature different topologies, such as open-loop converters [17], [21], [25], ΔΣ modulators with VCO-based quantizers [19], [20], or ΔΣ modulators with VCO-based integrators [23], [24], [27]. In these implementations, a significant part of the signal path is built by using standard digital cells and minimizing large analog circuits, such as operational amplifiers. Therefore, these "mostly-digital" circuits are particularly suitable for modern CMOS technologies, which are optimized for implementations of compact and efficient digital circuitry.

In this manuscript, we propose a new VCO-ADC topology designed for neural interfaces. The overall idea is the use of one VCO-based input-stage per channel, each of which generates a digital oscillation, modulated in frequency, which can then be processed using digital circuitry. However, instead of building one standalone VCO-ADC per channel frequency, we propose the use of shared digital circuitry to capture the position of VCO edges (referred to as "timestamps" in this work), which contain enough information to reconstruct the oscillation frequency and the input voltage after postprocessing. As illustrated in Figure 1, this readout strategy is aimed at simplifying the on-chip

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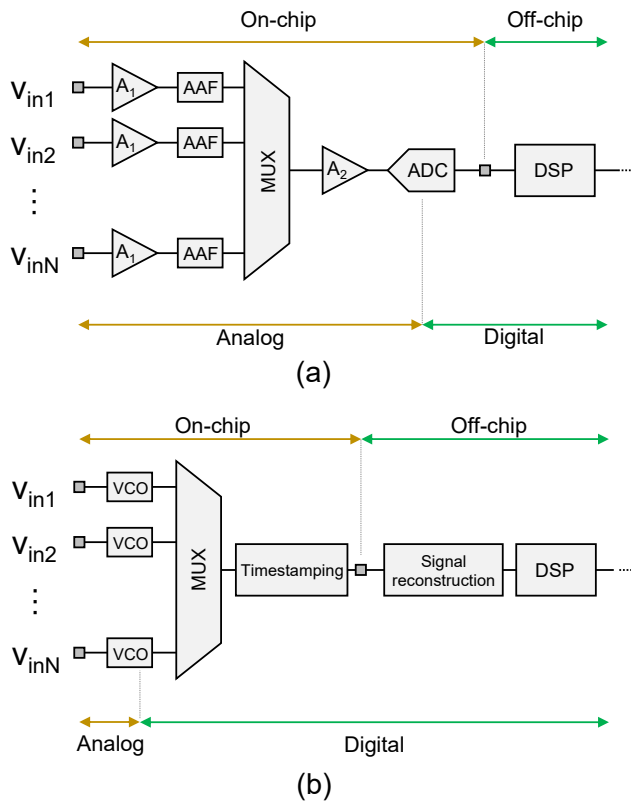
Fig. 1. (a) Simplified block diagram of a generic voltage microsensor array, consisting of a set of preamplifiers (A_1), anti-aliasing filters (AAF), a multiplexer (MUX), shared amplification stages (A_2) and ADCs, and off-chip digital signal processing (DSP) logic. (b) Simplified block diagram of the proposed readout. Each input modulates the oscillation frequency of a VCO, the digital output of which generates a sequence of timestamps on-chip. The input voltage can be inferred from the oscillation frequency, which is estimated off-chip, based on the relative position of the timestamps. The proposed readout is aimed at simplifying on-chip analog circuitry at the costs of more complex off-chip digital processing.

analog circuitry in the system at the costs of adding on-chip and off-chip digital circuitry.

This paper is organized as follows. Section II describes the readout architecture, including the fundamentals of voltage-to-frequency conversion and timestamping. Section III elaborates on how the input signal can be reconstructed from an incomplete collection of timestamps. In Section IV, we evaluate the performance of the system by simulation of a system that has been exposed to different input signals. Section V describes a prototype, manufactured in 0.18-μm CMOS technology, and shows the results of electrical characterization with sinusoids and pre-recorded neuronal signals. Finally, Section VI concludes the paper with a discussion about the potential of the proposed architecture.

II. READOUT ARCHITECTURE

The proposed readout system features three steps: voltage-to-frequency conversion, frequency-to-digital conversion (timestamping), and signal reconstruction. This section focusses on the first two steps, which comprise the on-chip mixed-signal operations required to transform analog input signals into digital 'timestamps'. The algorithms required for the third step, signal reconstruction, are described in Section III.

A. Voltage-to-Frequency Conversion

The instantaneous oscillation frequency of a VCO can be described as

$$f_O(t) = f_{fr} + g(v_{in}(t)) + f_n(t), \qquad (1)$$

where f_{fr} represents the free-running oscillation frequency, $v_{in}(t)$ is the input voltage, $g(\cdot)$ is a function that represents the relation between input voltage and change in oscillation frequency, and $f_n(t)$ is the random frequency fluctuation due to noise (visible as phase noise or jitter). Assuming small input signals, the oscillation frequency can be linearized as

$$f_O(t) = f_{fr} + K_{VCO}(v_{in}(t) + v_{IRN}(t)), \qquad (2)$$

where K_{VCO} represents the gain of the oscillator (in Hz/V), and $v_{IRN}(t)$ describes phase noise as input-referred noise. For simplicity, the oscillator is considered to be linear and noise-free for the rest of the manuscript. Nevertheless, the nonlinearities and phase noise of the VCO are the fundamental limitation in the accuracy of the voltage-to-frequency conversion process. A procedure to estimate the influence of nonlinearities and phase noise in VCOs can be found in [28].

Figure 2 depicts a simplified model of a VCO, including the most relevant signals. Part of these signals can be physically measured in a circuit, such as the input voltage $v_{in}(t)$ and the output oscillation $w(t)$. Other signals are only virtual and cannot be directly observed, such as the oscillation frequency $f_O(t)$, unwrapped phase $\varphi(t)$, or wrapped phase $\varphi_w(t)$. The oscillation frequency (in Hz) follows equation (2), assuming $v_{IRN}(t)=0$. The oscillator phase (in radians) increases unbounded, since it is the integral of the oscillation frequency – always positive – over time. The wrapped phase is the modulo-2π of the unwrapped phase and is, therefore, contained in the interval $[0,2\pi)$. The waveform function $wf(\cdot)$ describes the output voltage as a function of the wrapped phase, which - for a digital oscillation - can be

$$w(t) = wf(\varphi_w(t)) = \begin{cases} 1, & \text{if } \varphi_w(t) < \pi \\ 0, & \text{if } \varphi_w(t) \geq \pi \end{cases}. \qquad (3)$$

The rising edges of $w(t)$ indicate the timepoints at which the unwrapped phase crosses a multiple of 2π. These timepoints can be listed as a discrete sequence $t_r[i]$, so that $\varphi_w(t_r[i])=0$. Although a similar sequence could be built using falling edges, in that $\varphi_w(t_f[i])=\pi$, the rest of the manuscript only considers rising edges for simplicity.

The oscillation period can be calculated as the first difference of $t_r[i]$,
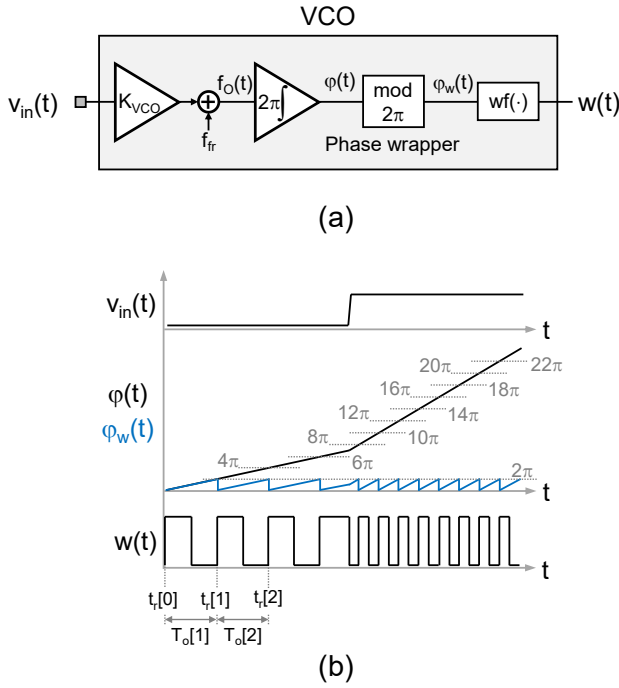
(a)

(b)

Fig. 2. (a) Noise-free linear VCO modeled as a phase integrator. (b) Example of the most relevant signals of the VCO.

$$T_O[i] = t_r[i] - t_r[i-1], \qquad (4)$$

where $T_O[i]$ represents the average value of the instantaneous oscillation period ($T_O(t)$) for $t_r[i-1] \le t \le t_r[i]$:

$$T_O[i] = \frac{1}{t_r[i]-t_r[i-1]} \int_{t_r[i-1]}^{t_r[i]} T_O(t)dt. \ (5)$$

Similar discrete sequences can be defined to describe the oscillation frequency and the input signal and their interdependence:

$$f_O[i] = \frac{1}{t_r[i]-t_r[i-1]} \int_{t_r[i-1]}^{t_r[i]} f_O(t)dt, \qquad (6)$$

$$v_{in}[i] = \frac{1}{t_r[i]-t_r[i-1]} \int_{t_r[i-1]}^{t_r[i]} v_{in}(t)dt, \qquad (7)$$

$$f_O[i] = \frac{1}{T_O[i]} = f_{fr} + K_{VCO}v_{in}[i]. \qquad (8)$$

From equations (4) and (8) we can conclude that the discretized input signal $v_{in}[i]$ can be calculated from sequence $t_r[i]$. Furthermore, as shown in equation (7), the discretized input voltage results from the averaging of $v_{in}(t)$. This averaging is equivalent to a low-pass filter that suppresses signal variations that are faster than the oscillation frequency and inherently acts as an antialiasing filter.

B. Frequency-to-Digital Conversion

The proposed frequency-to-digital conversion scheme is based on timestamping. We assign 'timestamping' to the generation of digital words –'timestamps'– that encode the timepoints at

which oscillation pulses initiate. In its simplest implementation that we call 'continuous timestamping' a 'timestamper' is constantly monitoring the output of the VCO and generates a timestamp at every detected rising edge. The resulting sequence represents $t_r[i]$ which, according to equations (4) and (8), can be used to recover the oscillation period and input signal. However, this approach would require one timestamper per VCO, which would result in relatively high power and area consumption. Therefore, we propose an alternative approach called here 'multiplexed timestamping', for which a single timestamper is shared among several VCOs, following the structure presented in Fig 1(b).

Continuous Timestamping

Figure 3(a) shows the block diagram of the proposed timestamper, which consists of a time reference generator (TRG) and a register. The TRG generates a digital word r(t), the value of which changes in every cycle of the clock clk(t) in a deterministic manner, such as an up-count. The register samples r(t) at every rising edge of the VCO oscillator w(t), generating a digital sequence m[i].

Figure 3(b) shows an example of the relevant signals of the proposed timestamp generator. The output of the up-counter is, neglecting overflow,

$$r(t) = floor(f_{clk}t), \qquad (9)$$

where f_{clk} is the frequency of clk(t), and the floor(·) function returns the greatest integer number, which is less than or equal to its argument. The value of m[i] depends on the timepoint at which the latest rising edge of the oscillation has occurred:

$$m[i] = r(t_r[i]) = floor(f_{clk}t_r[i]). \quad (10)$$

The 'floor' function is equivalent to a quantizer, that can be moddeled as additive quantization error e[i]:

$$m[i] = f_{clk}t_r[i] + e[i]. \quad (11)$$

Note that the oscillation period can be estimated, combining (11) and (4), as follows:

$$\widehat{T_o}[i] = \frac{(m[i]-m[i-1])}{f_{clk}} = T_o[i] + \frac{(e[i]-e[i-1])}{f_{clk}}. \quad (12)$$

where $\widehat{T_o}[i]$ denotes the estimated oscillation period. The difference between the oscillation period and the estimated oscillation period is due to the time quantization error (i.e., due to the limited resolution of the timestamper).

Assuming no correlation between the oscillation w(t) and the reference clock clk(t), quantization error e[i] can be considered random, resulting in white quantization noise bounded to [0,1). From equation (12), we conclude that the time quantization error is high-pass filtered, resulting in first-order noise-shaping. Furthermore, as expected, increasing the frequency of the reference clock mitigates the effect of quantization noise, since higher clock frequencies increase the resolution of the timestamper.
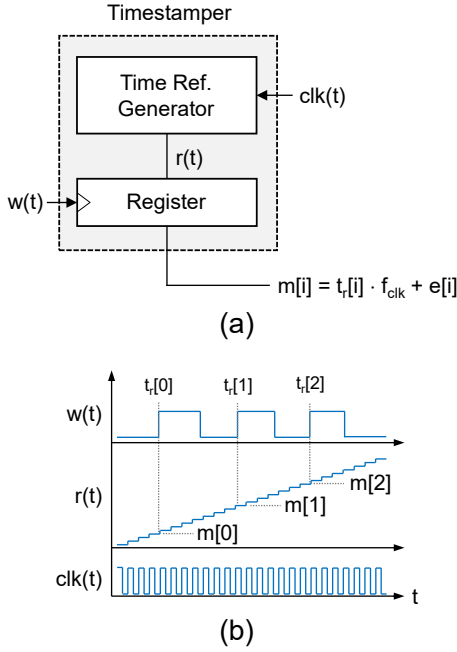
Fig. 3. (a) Block diagram of the proposed timestamper. (b) Example of the most relevant signals of the timestamper.

The estimated input voltage $\widehat{v_{in}}[i]$ can be calculated from the complete sequence of timestamps m[i] by combining equations (12) and (8).

Multiplexed Timestamping

To minimize the area and power consumption per channel, the timestamper can be shared among several VCOs without a significant loss of accuracy. Figure 4(a) depicts the on-chip stage of the system introduced in Figure 1(b), with N VCOs multiplexed to a single timestamper. The sequence generated by the timestamper, $m_{mux}[i]$, contains timestamps triggered by all the VCOs that have been eventually selected by the multiplexer. For simplicity, we consider only the first VCO (VCO$_1$) for the rest of the analysis. We can define $m_{S1}[i]$ as the subset of timestamps contained in $m_{mux}[i]$ triggered by VCO$_1$, while its corresponding selection signal ($\phi_1(t)$) was active. Figure 4(b) shows the most significant signals related to VCO$_1$. As in Section II.A, we can define sequence $t_{r1}[i]$ as the timepoints at which VCO$_1$ rising edges occur. The selected rising edges, $t_{S1}[i]$, are the ones captured by the timestamper and occurred while $\phi_1(t)=1$. The sequence $t_{S1}[i]$ can be defined as

$$t_{S1}[i] = t_r[S_1[i]], \quad (13)$$

where S$_1$[i] is a discrete sequence of integer numbers denoting which rising edges have been selected.

Like in equation (11), the value of timestamps can be described as

$$m_{S1}[i] = f_{clk}t_{S1}[i] + e_{S1}[i], \quad (14)$$

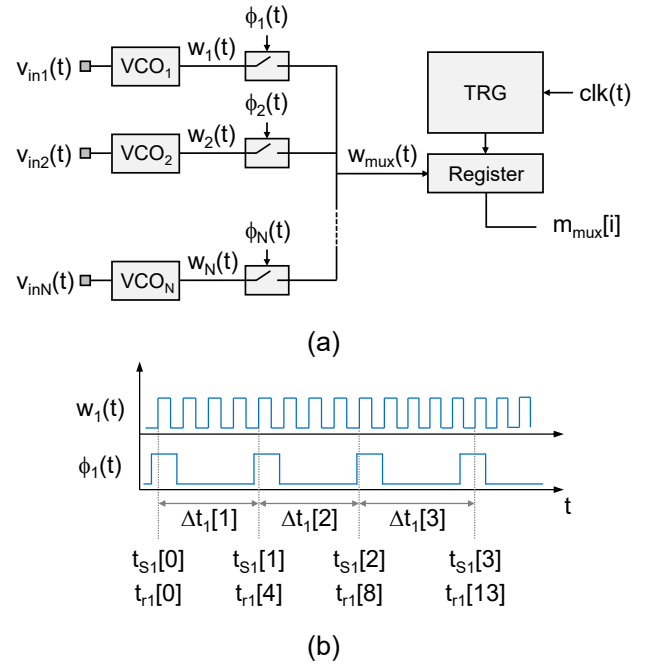and the time elapsed between two consecutive timestamps can

Fig. 4. (a) Block diagram of multiplexed VCOs sharing one timestamper. (b) Example of the subsampling of $t_{r1}[i]$ to generate $t_{S1}[i]$. In this example, the first values of S$_1$[i] were {0,4,8,13}, and the first values of N$_{S1}$[i] were {4,4,5}.

be described as

$$\Delta t_1[i] = t_{S1}[i] - t_{S1}[i-1] = \frac{m_{S1}[i]-m_{S1}[i-1]}{f_{clk}} - \frac{e_{S1}[i]-e_{S1}[i-1]}{f_{clk}}. \quad (15)$$

The average oscillation period between two consecutive timestamps is therefore

$$T_O[i] = \frac{1}{t_{S1}[i]-t_{S1}[i-1]} \int_{t_{S1}[i-1]}^{t_{S1}[i]} T_O(t)dt = \frac{\Delta t_1[i]}{N_{S1}[i]}, \quad (16)$$

where N$_{S1}$[i] represents the number of oscillations that occurred between $t_{S1}[i]$ and $t_{S1}[i-1]$ and can be defined as

$$N_{S1}[i] = S_1[i] - S_1[i-1]. \quad (17)$$

Finally, similarly to equation (12), the oscillation period can be estimated as

$$\widehat{T_{o1}}[i] = \frac{(m_{S1}[i]-m_{S1}[i-1])}{N_{S1}[i] \cdot f_{clk}} = T_{o1}[i] + \frac{(e_{S1}[i]-e_{S1}[i-1])}{N_{S1}[i] \cdot f_{clk}}. \quad (18)$$

Note that, while in equation (12) $\widehat{T_{o1}}[i]$ can be computed directly from the recorded timestamps, equation (18) also requires N$_{S1}$[i], which is a priori unknown. The following section explains how this unknown parameter can be estimated under certain assumptions, which then enables the reconstruction of $\widehat{T_{o1}}[i]$ and $\widehat{v_{in1}}[i]$.

III. SIGNAL RECONSTRUCTION

Consider the sequence $m_{S1}[i]$, a subset of timestamps captured while $\phi_1(t)$ is active. This sequence is the output of the hardware described in Section II and is the only data available off-chip for the reconstruction of the signal $\widehat{v_{in1}}[i]$. For simplicity, we assume for the rest of this section that f_{clk} is large enough, so quantization noise can be neglected and

$$t_{S1}[i] \approx \frac{m_{S1}[i]}{f_{clk}}. (19)$$

The primary challenge of signal reconstruction is to find the number of oscillations that occurred between two consecutive timestamps, $N_{S1}[i]$. From the description given in the previous section, we know that the number of oscillations can be - in theory - any natural number:

$$N_{S1}[i] \in \mathbb{N}. (20)$$

We do not have enough information to find $N_{S1}[i]$ and $v_{in1}[i]$, since there are infinite possible numbers satisfying this condition. However, we can incorporate a-priori knowledge about the hardware and the input signal to facilitate finding the correct number of oscillations.

Figure 5 shows an example of a reconstruction scenario, in which a VCO and a timestamper have been simulated with f_{fr} = 2 MHz, K_{VCO} = 20 MHz/V, v_{in1} = 0, and random $N_{S1}[i] \in [4,6]$. For each sample, we are plotting three possible estimations of the input voltage ($\widehat{v_{in1}}[i]$) for different possible values of $N_{S1}[i]$. It can be observed that, although all the plotted values are feasible from a mathematical point of view, it will be possible to identify the correct values of $\widehat{N_{S1}}[i]$ and $\widehat{v_{in1}}[i]$, if the input signal is known to meet certain conditions.

A. Input signal amplitude minimization

If the input signal is known to be small, signal reconstruction can be based on finding the sequence $N_{S1}[i]$ that results in the smallest possible input signal. Combining equations (8) and (16) we get:

$$v_{in1}[i] = \frac{N_{S1}[i]}{\Delta t_1[i] \cdot K_{VCO}} - \frac{f_{fr}}{K_{VCO}}, (21)$$

$$N_{S1}[i] = \Delta t_1[i] \cdot (f_{fr} + K_{VCO} v_{in1}[i]). (22)$$

If the input voltage is known to be small, we can solve equation (22) for $v_{in1}[i]=0$, and round the result to find an integer sequence $N_{S1}[i]$ that satisfies (20):

$$\widehat{N_{S1}}[i] = round\big(\Delta t_1[i] \cdot f_{fr}\big). (23)$$

This approach is computationally efficient and leads to valid reconstructions, if the input signal is small enough. This method fails, if the input signal is outside the following interval:

$$v_{in1}[i] \in \left(\frac{N_{S1}[i]-0.5}{\Delta t_1[i] \cdot K_{VCO}} - \frac{f_{fr}}{K_{VCO}}, \frac{N_{S1}[i]+0.5}{\Delta t_1[i] \cdot K_{VCO}} - \frac{f_{fr}}{K_{VCO}}\right). (24)$$
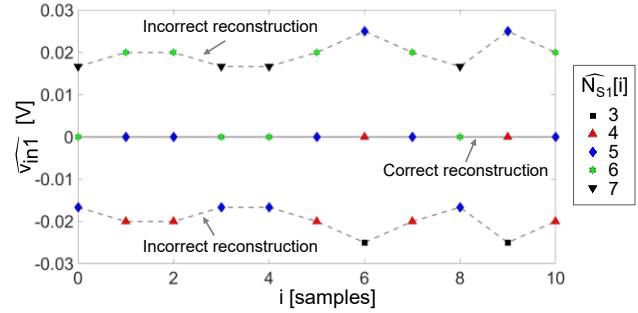

Fig. 5. Example of correct (solid line) and incorrect (dashed lines) reconstructions for f_{fr} = 2 MHz, K_{VCO} = 20 MHz/V, v_{in1} = 0, and random $N_{S1}[i] \in [4,6]$.

Note, that this approach requires accurate a priori knowledge of f_{fr}, since - from the reconstruction standpoint - deviations in the free-running oscillation frequency (Δf_{fr}) are indistinguishable from input offset ($\Delta v_{in} = \Delta f_{fr}/K_{VCO}$). Therefore, according to equation (24), unknown deviations in f_{fr} reduce the valid input range of this reconstruction algorithm.

B. Input signal variation minimization

If the input signal is known to be slow, signal reconstruction can be based on minimizing the total signal variation (TSV), defined here as the sum of the absolute value of the first difference:

$$TSV(x) = \sum_{i=-\infty}^{+\infty} |x[i] - x[i-1]|. (25)$$

As shown in Figure 5, incorrect reconstructions may show larger voltage variations than the correct reconstruction. This assumption is valid for slow or small input signals, for which two consecutive samples are expected to have similar values. The limits of this assumption will be explored in Section IV.

The number of oscillations can be found as a result of the following optimization problem, subject to equations (20), (21) and (25):

$$\widehat{N_{S1}}[i] = arg \min_{N_{S1}[i]} TSV(v_{in1}[i]). (26)$$

This optimization problem can be solved using Viterbi algorithm [29], [30]. Note that, in contrast to the previous reconstruction method, unknown slow deviations of the free-running oscillation frequency do not affect the validity of the reconstruction, since offset does not affect signal variation.

IV. SIMULATION RESULTS

We have evaluated the performance of the proposed readout technique by designing and simulating a VCO-ADC for neural interfaces. Table I summarizes the main parameters of the simulated system.

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TABLE I
SYSTEM PARAMETERS USED IN SIMULATIONS

Circuit	Parameter	Value used
VCO	f_{fr}	2 MHz
	K_{VCO}	20 MHz/V
Multiplexer	$\phi_{S1,T}$	12.2 μs
	$\phi_{S1,W}$	610 ns
Timestamper	f_{clk}	50 MHz / 200 MHz

We have considered the case of 20 VCOs multiplexed to a single timestamper, meaning that the timestamper can only observe each VCO during 5% of the time. The period of ϕ_{S1} ($\phi_{S1,T}$) defines the average sampling frequency of the system. We set the average sampling frequency well above the band of interest (a few kHz for neural signals), in order to limit input signal variations between samples, which facilitates signal reconstruction. With $\phi_{S1,T}$ = 12.2 μs, the average sampling frequency is approximately 82 kHz. The pulse width has been set to $\phi_{S1,W} = \phi_{S1,T}/20$ = 610 ns, so that the same timestamper can monitor 20 VCOs.

The free-running oscillation frequency is chosen in a way that the oscillation period is always shorter than the ϕ_{S1} pulse width, to make sure that there is at least one rising edge (and therefore at least one timestamp) in every ϕ_{S1} window. The sensitivity of the VCO has been chosen to be realistic for a specific VCO topology, as will be shown in Section V.B.

We have first evaluated the accuracy of multiplexed timestamping. The behavioral model of the VCO-ADC described above has been simulated for a sinusoidal input of 100 μV_p at 1 kHz, generating the complete sequence of rising edges ($t_r[i]$). To demonstrate the influence of f_{clk} in the accuracy of the system, we have generated two sequences of selected timestamps ($m_{S1}[i]$) with different clock frequencies, f_{clk} = 50 MHz and f_{clk} = 200 MHz. Selected timestamps have been combined with equations (15), (21) and (23) to estimate the input signal ($\widehat{v_{tn1}}[i]$). Figure 6 shows the spectra of the simulated reconstructed signals, obtained after interpolating and resampling $\widehat{v_{tn1}}[i]$ at 200 kHz. Interpolation and resampling were employed to achieve uniform sampling and facilitate the estimation of the power spectra, since the input signal is non-uniformly sampled at its origin (see equation (7)). The input-referred noise, integrated in the 300 Hz – 5 kHz band, is 3.1 μV_{rms} for f_{clk} = 50 MHz, and 0.96 μV_{rms} for f_{clk} = 200 MHz. As expected, quantization noise is inversely proportional to f_{clk}, since higher clock frequencies result in more accurate timestamps. Nevertheless, even for f_{clk} = 50 MHz, the in-band noise is low enough for action potential detection.

After simulating the accuracy of the timestamper, we have evaluated the performance of the reconstruction algorithms described in Section III. We have simulated the system described in Table I for a collection of 15000 input signals, with different combinations of amplitude and frequency, ranging from 10μV_p to 10mV_p and from 100 Hz to 10 kHz (uniformly distributed at logarithmic scale). White noise (100 nV/√Hz) was added to all input signals to model circuit noise. For each
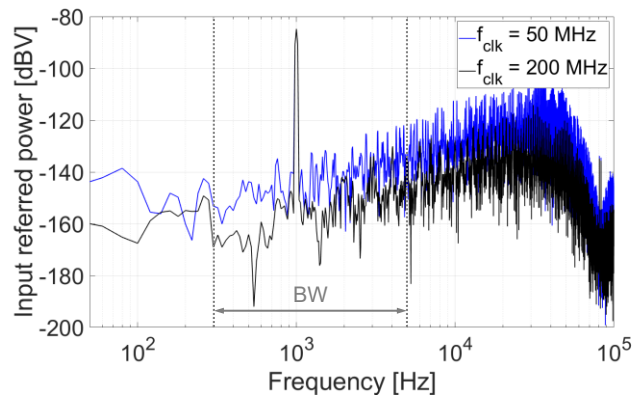

Fig. 6. Simulated spectra of the system described in Table I for an input signal of 100 μV_p at 1 kHz.

simulation of 50 ms, we have computed the selected timestamps ($m_{S1}[i]$) and the ground truth number of oscillations ($N_{S1}[i]$). We have then used the approaches, described in equations (23) and (26), to estimate the number of oscillations ($\widehat{N_{S1}}[i]$). A reconstruction has been considered valid when sequences $\widehat{N_{S1}}[i]$ and $N_{S1}[i]$ were identical for the entire duration of each simulation.

Figure 7 shows a summary of the four sets of simulations, combining the two reconstruction algorithms and the two different clock frequencies. The first approach, described by equation (23), results in valid reconstructions for input signals smaller than approximately 2 mV_p, as expected from equation (24). The performance of the minimization of signal variation described in equation (26) depends on the resolution of the timestamper. For f_{clk} = 200 MHz, this algorithm is consistently able to reconstruct large slow signals and small fast signals, and fails to reconstruct large fast signals. This is expected, since large fast signals feature higher signal variation, and there may be incorrect reconstructions with lower TSV than the correct reconstruction. For f_{clk} = 50 MHz, the reconstruction performance follows a similar trend, but reconstruction is less consistent and fails more frequently. This may be due to the lower accuracy of the timestamper, which increases quantization noise and, therefore, signal variation.

Based on these simulation results, both reconstruction algorithms appear to be suitable for most extracellular neural signals reconstructions, provided that extracellular action potential amplitudes are typically below 1 mVpp, and signal power is mainly contained in the 300 Hz – 5 kHz band. Input amplitude minimization is more robust against high-frequency noise, while input signal variation minimization responds better to large low-frequency signal fluctuations. Nevertheless, these methods still have limitations, and further algorithms need to be developed to achieve more robust signal reconstructions. For example, large abrupt voltage variations —which can be produced during neural stimulation— are likely to be missed by the proposed reconstruction approaches. Changes in system parameters, such as a different oscillation frequencies or multiplexing schemes, may be required to accommodate specific needs of different applications.
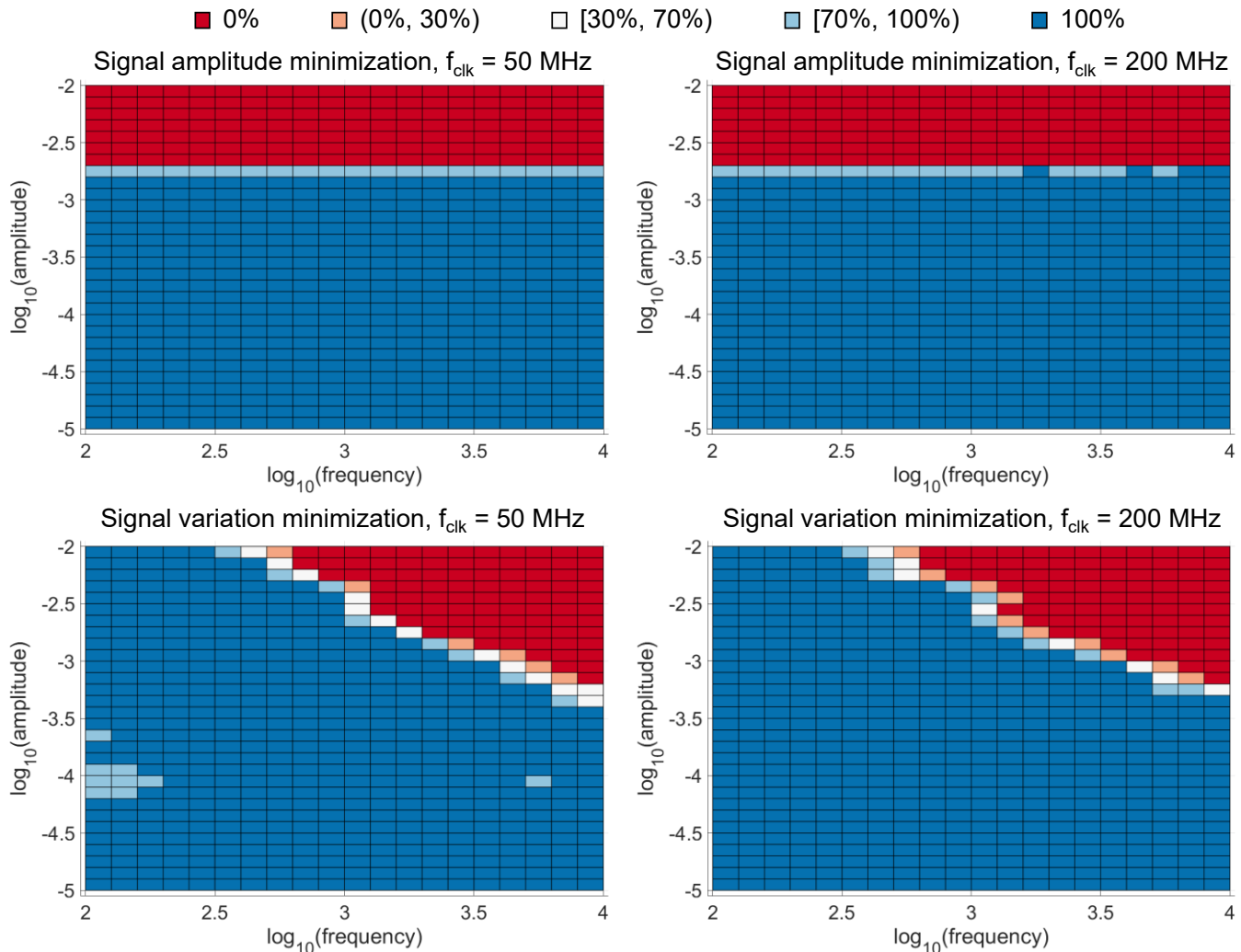
Fig. 7. Simulated performance of the two signal reconstruction algorithms described in Section III: signal amplitude minimization as described in equation (23), and signal variation minimization as in equation (26). Each rectangle represents the percentage of correct reconstructions in 25 simulations. Each simulation lasted for 50 ms, and the input signal was the combination of white noise (100 nV/√Hz) and a sinusoidal signal of varying amplitude and frequency.

V. EXPERIMENTAL VALIDATION

A prototype of the system described in the previous sections has been fabricated in 0.18-μm CMOS technology. This section describes the circuit implementation and the results of the electrical characterization.

A. Prototype description

The main requirements for neural interfaces and microelectrode arrays include sensitivity and low noise (to detect small action potentials), and low real estate and power consumption (to integrate thousands of units in the same substrate) [31]. Therefore, ring oscillators are a good choice due to their simplicity, compact size, and relatively low phase noise. Moreover, although ring oscillators normally feature a nonlinear voltage-to-frequency conversion, distortion is not problematic due to the small amplitude of input signals.

Figure 8(a) shows the schematic of our voltage-to-frequency converter. The input signal v_{in} is first filtered by a passive RC high-pass filter (HPF), based on a 350-fF metal-insulator-metal (MIM) capacitor (C_1) and a pseudoresistor (M_1). The cut-off frequency of this filter is set at approximately 0.1 Hz in order to block low-frequency fluctuations and to minimize the noise contribution of the pseudoresistor in the band of interest. The high-pass filtered voltage drives the gate of a P-type transistor (M_1) which, in combination with a cascode (M_2), acts as a transconductor [32]. The resulting current (i_{CCO}) modulates the frequency of a current-controlled oscillator (CCO). As shown in Figure 8(b), the CCO consists of three CMOS inverters, with three 60-fF MIM capacitors (C_{2-4}) used as load to achieve a lower oscillation frequency. Since the amplitude of the oscillation at v_{osc} is approximately 700 mV$_{pp}$, a level-shifter (M_{4-5}) and a digital buffer is used to obtain a square rail-to-rail oscillation at output w. The size of the relevant transistors is summarized in Table II.

TABLE II
VCO TRANSISTOR SIZE

Transistor	W(μm)/L(μm)	Transistor	W(μm)/L(μm)
M_1	1/0.4	M_4	1/0.2
M_2	30/1.2	M_5	1/0.2
M_3	10/1.2	M_{6-11}	0.8/3

The timestamper is implemented following the structure described in Figure 3(b), with an 8-bit Gray counter acting as TRG, driven at $f_{clk} = 50$ MHz by an external clock. Gray-code has been chosen to avoid potential problems caused by sampling a wrong code during a transition, right after a clock edge. The counter was oversized to prevent overflows at very low oscillation frequencies or very high clock frequencies. The number of bits could be further optimized, based on the maximum number of clock cycles expected between two consecutive sampled VCO rising edges.

Figure 9 shows the micrograph of the prototype, in which the areas containing the relevant building blocks have been highlighted. The estimated real estate and the simulated power consumption of each block are summarized in Table III. The total area and power of our circuits amount to 5550 μm² and 40.05 μW. However, since the timestamper can be shared among several VCOs, the effective area and power per channel depends on the number of multiplexed channels. For example, if we consider 20 VCOs sharing the same timestamper (as simulated in Section IV), area and power consumption per channel would be 1330 μm²/channel and 4.4 μW/channel.

TABLE III
SUMMARY OF AREA AND POWER CONSUMPTION

Block	Circuit	Area (μm²)	Power (μW)
VCO	Transconductor	630	1.2
	CCO + LS	480	1.32
	Total	1110	2.52
Timestamper	Register	840	1.53
	TRG	3600	36
	Total	4440	37.53

*B. Measurement results*

The transconductor was programmed to generate approximately 1 μA, with a transconductance of 20 μA/V. The resulting measured free-running oscillation frequency (f_{fr}) was 1.95 MHz with a sensitivity (K_{VCO}) of 22.0 MHz/V.

Figure 10 shows the spectra of the recorded signals for a 100-μV_p signal applied at 1 kHz. The black spectrum is the result of continuous timestamping, where a complete sequence of timestamps was collected, and the input signal $\widehat{v_{in}}[i]$ was calculated combining equations (8) and (12). The noise in the band of interest (300 Hz – 5 kHz) was 4.5 μV_{rms}, mainly limited by VCO phase noise. The blue spectrum shows the result of multiplexed timestamping, where timestamps were selected according to the multiplexing scheme used in Section IV (see
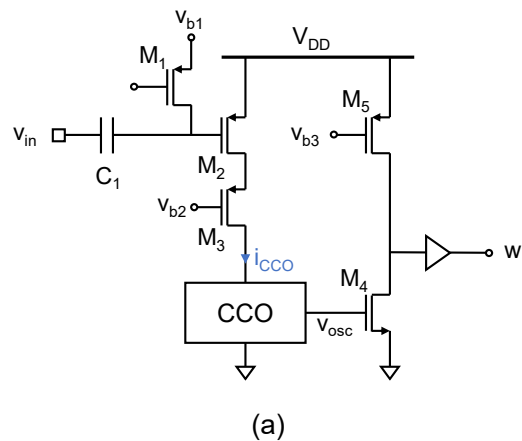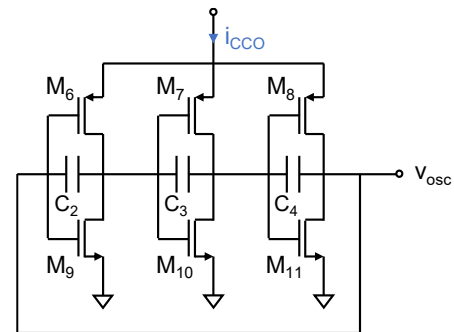
Fig. 8. (a) Schematic of the voltage-to-frequency converter. (b) Schematic of the CCO.
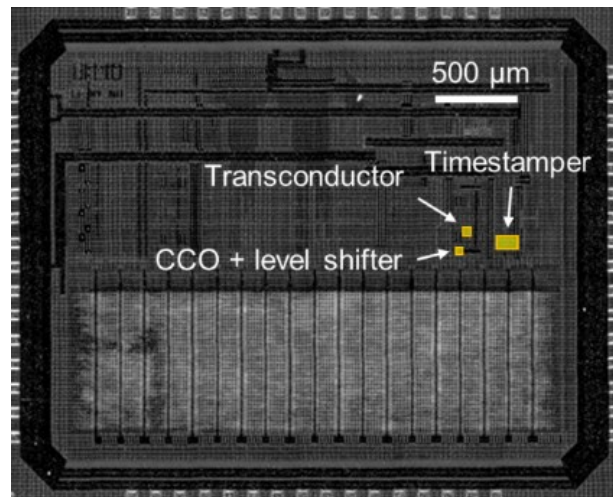
Fig. 9. Micrograph of the prototype fabricated in 0.18 μm CMOS technology, with the location of three relevant circuits highlighted.

Table I), and signal reconstruction was performed using the methods explained in Section III. Both reconstruction algorithms provided identical results. The noise in the band of interest (300 Hz – 5 kHz) was 5.7 μV_{rms}. The contribution of quantization noise due to multiplexing is visible at high frequencies.
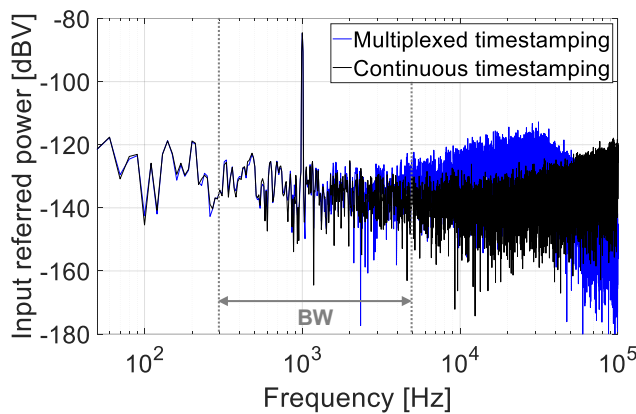
Fig. 10. Spectra of the recorded signals for a sinusoidal input of 100 µV$_p$ at 1 kHz.

As mentioned in section IV, power spectral estimations were preceded by interpolation and resampling at high frequencies to achieve uniform sampling, since the timestamping process results in non-uniform sampling (see equation (7)). The resampling frequencies (20 MHz for continuous timestamping and 200 kHz for multiplexed timestamping) were chosen well above the average sampling frequency for each case (1.95 MHz for continuous timestamping, and 82 kHz for multiplexed timestamping). Note that interpolation and resampling were performed off-chip and only to facilitate spectral estimations, but none of these processes is required for normal operation of the system.

The system has also been tested with a pre-recorded neuronal signal. Figure 11(a) shows the snippet of a signal captured using the CMOS microelectrode array described in [7], from an in-vitro culture of rat primary cortical neurons on day in vitro (DIV) 23. Figure 11(b) shows the snippet of the reconstructed signal after injecting the pre-recorded signal at the input of the system, capturing timestamps and using equations (23) and (25) for reconstruction (both algorithms could be used to successfully reconstruct the signal). Note, that the prototype
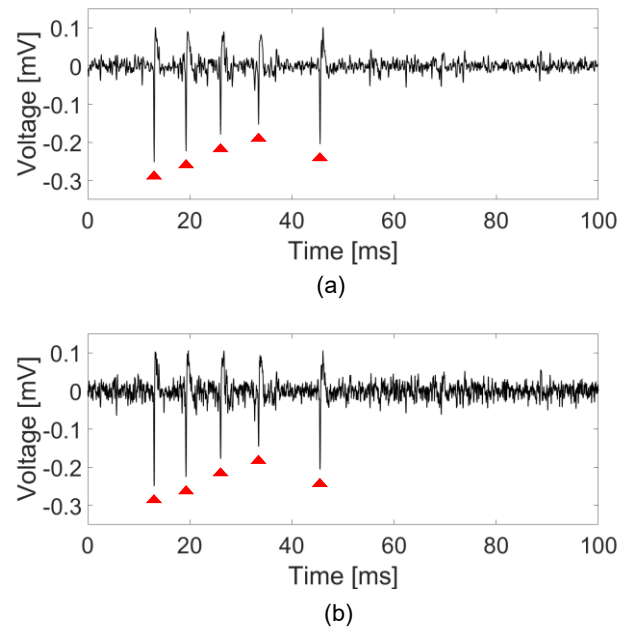

Fig. 11. (a) Snippet of a pre-recorded neural signal captured with the HD-MEA described in [7] in an in-vitro culture of rat primary cortical neurons. (b) Snippet of the reconstructed signal. Red triangles mark significant action potentials with amplitudes larger than 5 times the standard deviation of the signal. Both signals have been band-pass filtered (300 Hz – 5 kHz) before plotting.

could digitize the signal successfully, and all significant APs (marked with red triangles, larger than 5 times the standard deviation of the recording noise) are visible in the reconstructed signal.

VI. CONCLUSION AND OUTLOOK

In this manuscript we have presented a novel readout architecture for neural interfaces. As in other VCO-based systems, VCOs are used to transform analog input signals into

TABLE IV
PERFORMANCE SUMMARY OF A 20-CHANNEL SYSTEM AND COMPARISON WITH STATE OF THE ART

	[7]	[33]	[34]	[10]	[35]	[36]	[32]	**Proposed system**
Year	2017	2018	2018	2020	2021	2021	2021	**2023**
Architecture	SAR	ATC	Δ-ΔΣ	SS	IΔΣ	SAR	VCO-Q	**VCO-TS**
Technology (nm)	180	65	180	90/65	180	180	180	**180**
Sampling frequency (Hz)	20 k	-[d]	25 k	70 k	20 k	11.6 k	1 M	**82 k[e]**
Bandwidth (Hz)	300 – 10 k	11 k	0.5 – 12.7 k	300 – 10 k	300 – 10 k	300 – 5 k	300 – 6 k	**300 – 5 k**
Area/channel (mm²/ch)	0.024[a]	0.006	0.058[c]	0.014[a]	0.0046[c]	0.001[a]	0.0045[b]	**0.0013[b,f]**
Power/channel (µW/ch)	16	1.2	3.05	130	8.59[c]	5.9	3.5[b]	**4.4[b,f]**
Input-referred noise (µV$_{rms}$)	2.4	3.8	3.32	5.5	4.37	10.4	5.0	**5.7[f]**

ATC: Analog-to-Time Converter; SS: Single-slope; IΔΣ: Incremental ΔΣ; VCO-Q: VCO-based quantizer. VCO-TS: VCO-timestamping. [a]Estimated. [b]Excluding biasing. [c]Including on-chip digital filter. [d]Asynchronous output. [e]Average frequency (non-uniformly sampled). [f]Assuming 20:1 multiplexing.

digital oscillations that can be post-processed using digital circuitry. Here, we proposed the generation of timestamps, which contain information about when a VCO has completed one oscillation. This information is enough to reconstruct the oscillation frequency and the input signal off chip. The main advantage of the proposed architecture is that on-chip analog circuitry is minimized, since most of the circuitry required for VCO-timestamping is digital. Furthermore, the proposed architecture is easily scalable to a large number of channels, since the digital timestamper can be multiplexed among several VCOs.

The oscillation frequency of each VCO can be easily calculated when all the timestamps are collected. However, when multiplexing the timestamper, a significant number of timestamps is missed. In this case, signal reconstruction algorithms are required to infer the correct oscillation frequency. In this work, we have proposed two different approaches, both of them based on simple assumptions about the oscillation frequency and the amplitude and bandwidth of the input signal. Both algorithms have been simulated, and have been proven to be feasible solutions for the system evaluated in this manuscript. Nevertheless, other algorithms may be more efficient or robust, or may allow to relax the constraints of the VCO. The use of existing algorithms, developed for other fields that address comparable problems (such as module-ADCs [37] or compressed sensing [38], [39]), could be explored.

A single-channel prototype has been fabricated in 0.18-μm CMOS technology. The readout circuit featured 5.7 μV$_{rms}$ of input referred noise in the 300 Hz – 5 kHz band and could capture pre-recorded neuronal action potentials. The area and power consumption of the single-channel prototype was 5'550 μm^2 and 40.05 μW. The performance of a multi-channel neural interface, implemented using the proposed time-domain readout technique, would strongly depend on parameters not yet explored with this prototype. Multiplexing several VCOs per timestamper would significantly reduce the effective area and power per channel, since, as shown in Table III, the timestamper is the main contributor to area and power consumption. To illustrate the potential of the proposed architecture, we have estimated the performance of a hypothetical 20-channel system combining 20 VCOs and one timestamper. This estimation does not consider two factors: multiplexing circuitry and timestamper optimization. On the one hand, multiplexing would require additional circuitry (mainly switches) that may increase area and power consumption. On the other hand, the timestamper could be further optimized, e.g., by reducing the number of bits, to decrease area and power consumption.

Table IV presents a comparison between state-of-the-art neural readout circuits and the estimated performance of the hypothetical 20-channel system. The proposed system features very low real estate while achieving low power consumption. However, input-referred noise is comparatively high, and very small action potentials (on the order of 10-20 uV) may not be distinguishable from noise. Nevertheless, as shown in section V.B, noise is low enough to capture larger extracellular action potentials.

One potential drawback of the proposed system is the relatively high data rate required to transmit all the timestamps off chip. Assuming an average sampling rate of 82 kSps and each timestamp being 8 bits long, the average data rate is 656 kbps per channel. However, the number of bits in the timestamper could be further optimized, and the sampling rate could be reduced at the cost of making the reconstruction process more challenging. It is worth noting that the proposed technique would benefit from CMOS-technology scaling, as most building blocks are digital circuits that would be more efficient in deep submicron technologies.

The proposed approach may be also suitable for cameras and other sensor arrays in which (i) several channels need to be monitored simultaneously, (ii) a-priori knowledge about the input signal is available, and (iii) advanced digital signal processing is possible.
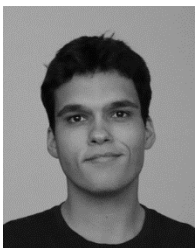
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