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Fast and Accurate Data Sheet based Analytical Turn-on Switching Loss Model for a SiC MOSFET and Schottky Diode Half-Bridge

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***Index Terms*—Wide bandgap devices, SiC MOSFET, Switching losses, Analytical model.**

***Abstract*—This paper proposes a novel data sheet based, fully analytical turn-on switching loss model for a SiC MOSFET and Schottky diode half-bridge including parasitics. The proposed model shows similar accuracy (error around 28%) compared to analytical switching loss models without closed-form analytical equations in the literature, while reducing the computational effort by more than 20 times. In addition, the proposed model shows the best accuracy (error around 12.4%) compared to other fully analytical switching loss models in the literature, which is verified by using measured device characteristics instead of data sheet information. The accuracy of the proposed model is comprehensively verified by double pulse tests using 5 different SiC MOSFET (with different structures) and Schottky diode pairs from different manufacturers.**

I. Introduction

SiC MOSFETs are widely used for building power electronic converters in the medium-voltage-level range due to their superior material properties compared to their Si counterparts [1]. The lower conduction and switching losses of SiC MOSFETs enable a converter design with a higher efficiency and a higher power density. In order to identify an optimal system design, an accurate switching loss model is required [2]. During converter design procedures the switching loss models are typically executed several thousand times [3], which requires computationally efficient models that deliver accurate results within a reasonable amount of time. As a result, analytical models are usually preferred over physics-based and behavioural models for converter optimisation procedures, due to their good compromise between accuracy and computational effort [4], [5].

In the analytical switching loss models, the complete switching transient is usually split into different time intervals. Different equivalent circuits are derived for the time intervals and their responses (voltage and current) are solved accordingly. As analysed in [6], a set of nonlinear differential equations (NDE) has to be solved for determining the voltage and current waveforms, due to the nonlinear device characteristics. In addition, the complexity of the formulated differential equation set is linked to the number of passive (parasitic) components that are included in the equivalent circuit. In order to obtain closed-form analytical solutions to these NDEs, different assumptions must be used, as categorised in [7].

Based on different assumptions/simplifications, many analytical switching loss models have been proposed for power MOSFETs with a clamped inductive load [2], [4], [6], [8]–[20]. In these models, the switching losses are obtained by determining the time integral of the transient power of the device under test ($E_{\mathrm{sw}} = \int_{t_{\mathrm{sw}}} v_{\mathrm{DS}} \cdot i_{\mathrm{DS}} \, \mathrm{d}t$), where t_{sw} is the switching time, v_{DS} is the drain-to-source voltage, and i_{DS} is the drain-to-source current. The analytical models can be categorised into three groups as discussed in the following. The first group of models [8]–[14], called *full-analytical model* (FAM) in this paper, provide completely closed-form analytical equations for $i_{\mathrm{DS}}, v_{\mathrm{DS}}, t_{\mathrm{sw}}$ to calculate the switching losses. The second group of models [4], [15]–[18], called *semi-analytical model* (SAM), only provide closed-form analytical equations for the switching waveforms v_{DS} and i_{DS} but not for t_{sw}. The remaining models, called *num-analytical model* (NAM), either require numerical iterations when calculating the switching losses [2], [19], or require numerical solvers to solve the equations [6], [20]. In order to limit the computational effort (typically less than a few milliseconds per iteration) in converter optimisation procedures, FAMs are preferred.

For the FAMs proposed in [8]–[14], assumptions/simplifications for the waveform shapes or the included parasitic components are made to obtain closed-

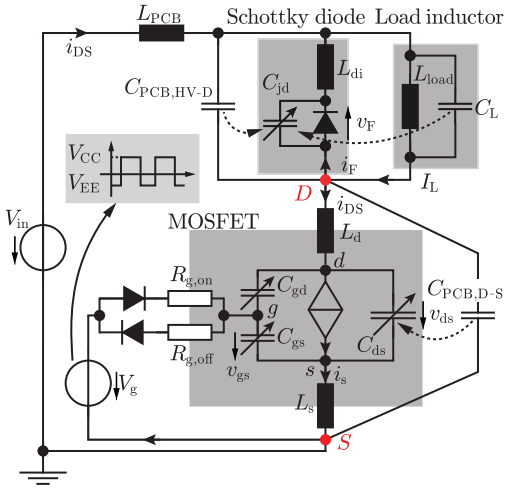

Fig. 1. Hard-switched half-bridge with a SiC MOSFET equivalent circuit, parasitics, a SiC Schottky diode, and an inductive load.

form analytical equations, leading to a limited accuracy. For example, the switching waveforms i_{DS} and v_{DS} are linearised in [8]–[10], [13] based on a constant averaged gate current in each switching interval. In addition, the common source parasitic inductance from the MOSFET package is neglected in [11], [12], causing huge errors. Furthermore, the 5 models presented in [8]–[12] assume a constant gate miller voltage during voltage rise/fall intervals, which is inaccurate, due to the pronounced drain induced barrier lowering effect in state-of-the-art SiC MOSFETs [21]. Although the constant miller voltage assumption is not used in the models [13], [14], they either make direct assumptions on the switching waveform shapes without physical explanations, or directly neglect some terms of the formulated circuit equations based on a pure mathematical analysis.

For the SAMs proposed in [4], [15]–[18], a differential equation for the gate-to-source voltage v_{gs}, which is a second order linear inhomogeneous constant coefficient differential equation (SOLICCDE), has to be solved. The SOLICCDE is obtained based on a piecewise constant assumption of the MOSFET nonlinear capacitances and transconductance. In a next step, i_{DS} and v_{DS} can be derived from the closed-form analytical equation of v_{gs}. However, the switching time t_{sw} cannot be explicitly expressed as a closed-form equation due to the complexity of the general solution of the SOLICCDE, which leads to large computational effort when implementing these models (analysed below in the paper). In addition, although the SOLICCDEs in [4], [15]–[18] are all solved using Laplace transform, only [18] transforms the second derivative term in the time domain correctly into the complex frequency domain without neglecting the first derivative term. As analysed below in this paper, missing the initial condition for the first derivative of v_{gs} could lead to large errors (worst over 30%) to the switching loss calculation.

Due to the limitations of the mentioned models, this paper proposes a novel fast and accurate, purely data sheet based, and fully analytical turn-on switching loss model for a SiC MOSFET and Schottky diode half-bridge including parasitics. The key features of the new model are:

- Model parameters are only based on data sheets.
- It is not assumed that the gate miller voltage is constant during the voltage fall interval.
- Multi-step piecewise constant assumption of the nonlinear MOSFET transconductance and capacitances is used.
- Fully analytical and computationally efficient. Closed-form analytical equations for the switching time, switching waveforms and switching losses are derived as general solutions of the SOLICCDEs, which are solved accurately by including the initial condition for v'_{gs}.
- The model is accurate in a wide operating range for different SiC MOSFETs with different device structures (e.g. trench gate, planar gate).

This paper is organised as follows. In section II, the proposed analytical switching loss model is derived, based on the summarised assumptions and the approximated nonlinear device characteristics. Section III evaluates the proposed model in terms of accuracy (based on Spice simulation and double pulse test) and computational effort, and analyses the impact of the mentioned assumptions in depth. Conclusions are drawn in section IV.

II. Proposed Analytical Turn-on Switching Loss Model

In this section, the proposed fully analytical turn-on switching loss model is derived based on a step-by-step switching transition analysis. The equation set for the equivalent circuit depicted in Fig. 1 is formulated based on the following assumptions/simplifications and the approximated nonlinear device characteristics.

A. Assumptions/Simplifications

- A lumped gate resistance $R_{g,on(off)}$ is assumed, which is the sum of the gate driver output resistance, the MOSFET internal gate resistance $R_{g,int}$, and an external gate resistance $R_{g,ext}$.
- The DC voltage V_{in} and the inductive load current I_L are assumed to be constant during the switching transitions. An ideal bipolar gate voltage V_g with negligible rise and fall time is assumed.

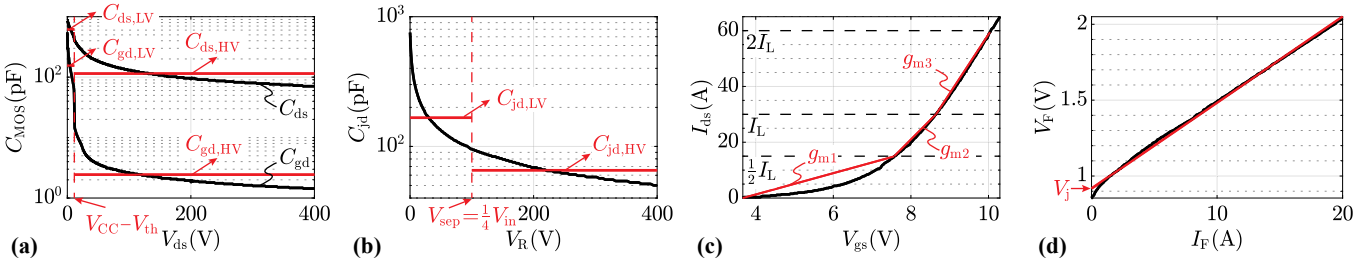

Fig. 2. Approximated nonlinear device characteristics of (a) MOSFET intrinsic capacitances, (b) Schottky diode junction capacitance, (c) MOSFET transfer characteristics, and (d) Schottky diode forward characteristics (for switch diode pair 1 defined in Tab. II).

- A lumped parasitic inductance L_{PCB} from the power loop PCB traces is assumed. The parasitic inductances from device packages (L_{d}, L_{s}, and L_{di}) are also included. The gate loop parasitic inductance and the PCB trace resistance are neglected [7].
- The parasitic PCB capacitance $C_{\mathrm{PCB,HV\text{-}D}}$ and the parasitic capacitance C_{L} of the load inductor are connected in parallel to the Schottky diode junction capacitance C_{jd}, as shown in Fig. 1. The parasitic PCB capacitance $C_{\mathrm{PCB,D\text{-}S}}$ is connected in parallel to the MOSFET drain-to-source capacitance C_{ds}.
- A constant temperature is assumed, so that all parameters are temperature invariant during switching transitions.
- The charge and discharge of the MOSFET intrinsic capacitances are assumed to be lossless. The switching losses are determined by the overlap between i_{DS} and v_{DS}.
- The voltage drop caused by the gate current i_{g} on the common source inductance L_{s} is neglected, i.e. $i_{\mathrm{DS}} = i_{\mathrm{ds}} = i_{\mathrm{s}}$ is assumed.

B. Approximated Nonlinear Device Characteristics

The MOSFET gate-to-source capacitance C_{gs} is assumed to be constant. The nonlinear gate-to-drain capacitance C_{gd} is approximated by the following two discrete values [8], [11], [17]

$$C_{\mathrm{gd}} = \begin{cases} C_{\mathrm{gd,LV}}, & 0 < v_{\mathrm{ds}} \le V_{\mathrm{CC}} - V_{\mathrm{th}} \\ C_{\mathrm{gd,HV}}, & V_{\mathrm{CC}} - V_{\mathrm{th}} < v_{\mathrm{ds}} \le V_{\mathrm{in}}, \end{cases} \tag{1}$$

where $C_{\mathrm{gd,LV}}$ and $C_{\mathrm{gd,HV}}$ are the average values of the nonlinear capacitance within the respective voltage range. The same approximation is used for the MOSFET drain-to-source capacitance C_{ds} and the Schottky diode junction capacitance C_{jd}, as depicted in Fig. 2a and 2b, where the separation voltage is $V_{\mathrm{sep}} = \frac{1}{4}V_{\mathrm{in}}$ for C_{jd}.

In the MOSFET saturation region, a linearised gate-to-source voltage v_{gs} controlled current source i_{ds} model is used with a constant transconductance g_{m}, as in general described by

$$i_{\mathrm{ds}}(t) = g_{\mathrm{m}} \cdot v_{\mathrm{gs}}(t) + h, \tag{2}$$

without separating the channel current from the drain-to-source current. The nonlinear $I_{\mathrm{ds}} - V_{\mathrm{gs}}$ transfer characteristic is separately linearised in three different current regions ($[0, \frac{1}{2}I_{\mathrm{L}}]$, $[\frac{1}{2}I_{\mathrm{L}}, I_{\mathrm{L}}]$, $[I_{\mathrm{L}}, 2I_{\mathrm{L}}]$) with different g_{m} values, as shown in Fig. 2c. Finally, the Schottky diode $I_{\mathrm{F}} - V_{\mathrm{F}}$ forward characteristic is linearised with

$$v_{\mathrm{F}}(t) = k i_{\mathrm{F}}(t) + V_{\mathrm{j}}, \tag{3}$$

as depicted in Fig. 2d.

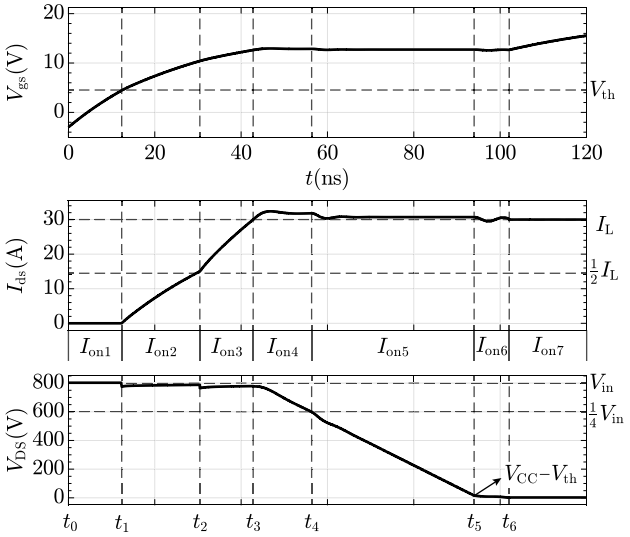

Fig. 3. 800 V/30 A turn-on switching waveforms for SDP2.

C. Turn-on Transition

The turn-on transition is analysed below based on a step-by-step switching interval analysis. To simplify the analytical equations, the device parameters are summarised and listed in Tab. I with different values in different time intervals. In addition, the beginning time of each switching interval is always reset to zero for simplicity. Fig. 3 illustrates a turn-on switching waveform including the following seven time intervals for a switch diode pair (SDP, defined in Tab. II) as an example.

TABLE I
PARAMETERS, VARIABLES, AND EQUATIONS FOR TURN-ON SWITCHING INTERVALS

Interval	V_{gs0}	V'_{gs0}	V_{F0}	g_{m}	h	C_{iss}	C_{gd}	C_{jd}	Δ
I_{on2}	V_{th}	$\frac{V_{\text{CC}}-V_{\text{th}}}{R_{\text{g}}C_{\text{iss}}}$	-	g_{m1}	$-g_{\text{m1}}V_{\text{th}}$	$C_{\text{iss,HV}}$	$C_{\text{gd,HV}}$	-	${T_{\text{n}}}^2-4T_{\text{a}}$
I_{on3}	$v_{\text{gs,on2}}(t_{\text{on2}})$	$v'_{\text{gs,on2}}(t_{\text{on2}})$	-	g_{m2}	$\frac{1}{2}I_{\text{L}}-g_{\text{m2}}V_{\text{gs0}}$			-	
I_{on4}	$v_{\text{gs,on3}}(t_{\text{on3}})$	$v'_{\text{gs,on3}}(t_{\text{on3}})$	$k(I_{\text{L}}-g_{\text{m2}}V_{\text{gs0}}-h)+V_{\text{j}}$	g_{m3}	$I_{\text{L}}-g_{\text{m3}}v_{\text{gs,on3}}(t_{\text{on3}})$			$C_{\text{jd,LV}}$	${T_{\text{b}}}^2-4T_{\text{a}}T_{\text{c}}$
I_{on5}	$v_{\text{gs,on4}}(t_{\text{on4}})$	$v'_{\text{gs,on4}}(t_{\text{on4}})$	$v_{\text{F,on4}}(t_{\text{on4}})$					$C_{\text{jd,HV}}$	
I_{on6}	$v_{\text{gs,on5}}(t_{\text{on5}})$	$v'_{\text{gs,on5}}(t_{\text{on5}})$	$v_{\text{F,on5}}(t_{\text{on4}})$			$C_{\text{iss,LV}}$	$C_{\text{gd,LV}}$		

Note: Fields with "-" are not needed for switching loss calculation. Common variables and equations are listed below.

$V_{\text{g}}=V_{\text{CC}}$, $R_{\text{g}}=R_{\text{g,on}}$, $T_{\text{a}}=R_{\text{g}}C_{\text{gd}}g_{\text{m}}L_{\text{pl}}$, $T_{\text{b}}=R_{\text{g}}C_{\text{iss}}g_{\text{m}}L_{\text{s}}$, $T_{\text{c}}=1+\frac{R_{\text{g}}C_{\text{gd}}g_{\text{m}}}{C_{\text{jd}}}$, $T_{\text{d}}=V_{\text{CC}}+\frac{R_{\text{g}}C_{\text{gd}}(I_{\text{L}}-h)}{C_{\text{jd}}}$,
$T_{\text{e}}=T_{\text{a}}V_{\text{gs0}}$, $T_{\text{f}}=T_{\text{b}}V_{\text{gs0}}+T_{\text{a}}V'_{\text{gs0}}$, $T_{\text{n}}=kg_{\text{m}}R_{\text{g}}C_{\text{gd}}+R_{\text{g}}C_{\text{iss}}+g_{\text{m}}L_{\text{s}}$, $m_0=V_{\text{F0}}+g_{\text{m}}\frac{T_{\text{b}}T_{\text{d}}-T_{\text{c}}T_{\text{f}}}{C_{\text{jd}}T_{\text{c}}^2}$, $\omega=\frac{\sqrt{-\Delta}}{2T_{\text{a}}}$.

$$v'_{\text{gs,u}}(t)=\left\{[2T_{\text{a}}^2T_{\text{d}}-T_{\text{a}}(T_{\text{b}}T_{\text{f}}+2T_{\text{c}}T_{\text{e}})+T_{\text{b}}^2T_{\text{e}}]\cdot\sin\left(\tfrac{\sqrt{-\Delta}}{2T_{\text{a}}}t\right)+\sqrt{-\Delta}\cdot(T_{\text{a}}T_{\text{f}}-T_{\text{b}}T_{\text{e}})\cdot\cos\left(\tfrac{\sqrt{-\Delta}}{2T_{\text{a}}}t\right)\right\}\cdot\tfrac{1}{\sqrt{-\Delta}\cdot T_{\text{a}}^2}\cdot\mathrm{e}^{-\frac{T_{\text{b}}}{2T_{\text{a}}}t}.$$

Interval	d	q	m	n	p
I_{on2}	$-\frac{T_{\text{b}}}{2T_{\text{a}}}$	0	$\frac{V_{\text{CC}}-v_{\text{gs,on2}}(t_{\text{on2}})}{V_{\text{gs0}}-V_{\text{CC}}}$	$\frac{2V'_{\text{gs0}}T_{\text{a}}-V_{\text{CC}}T_{\text{n}}+V_{\text{gs0}}T_{\text{n}}}{\sqrt{\Delta}(V_{\text{CC}}-V_{\text{gs0}})}$	1
I_{on3}			$\frac{V_{\text{CC}}-v_{\text{gs,on3}}(t_{\text{on3}})}{V_{\text{gs0}}-V_{\text{CC}}}$		
I_{on4}	$-\frac{T_{\text{b}}}{2T_{\text{a}}}$	$\frac{T_{\text{c}}(I_{\text{L}}-h)-g_{\text{m}}T_{\text{d}}}{C_{\text{jd}}T_{\text{c}}}$	$m_0+V_{\text{CC}}-V_{\text{th}}$	$\frac{g_{\text{m}}(2T_{\text{a}}T_{\text{c}}T_{\text{d}}+T_{\text{b}}T_{\text{c}}T_{\text{f}}-T_{\text{b}}^2T_{\text{d}}-2T_{\text{c}}^2T_{\text{e}})}{\sqrt{-\Delta}C_{\text{jd}}T_{\text{c}}^2}$	$g_{\text{m}}\frac{T_{\text{c}}T_{\text{f}}-T_{\text{b}}T_{\text{d}}}{C_{\text{jd}}T_{\text{c}}^2}$
I_{on5}			$m_0+V_{\text{in}}-V_{\text{CC}}+V_{\text{th}}$	$\frac{g_{\text{m}}[T_{\text{b}}T_{\text{c}}T_{\text{f}}-T_{\text{b}}^2T_{\text{d}}-2T_{\text{c}}^2(C_{\text{jd}}L_{\text{pl}}T_{\text{d}}+T_{\text{e}})]}{\sqrt{-\Delta}C_{\text{jd}}T_{\text{c}}^2}+$	$\frac{g_{\text{m}}(T_{\text{c}}T_{\text{f}}-T_{\text{b}}T_{\text{d}})}{C_{\text{jd}}T_{\text{c}}^2}-$
I_{on6}			$m_0+V_{\text{in}}-V_{\text{dson}}$	$\frac{g_{\text{m}}L_{\text{pl}}(T_{\text{a}}T_{\text{b}}T_{\text{f}}+2T_{\text{a}}T_{\text{c}}T_{\text{e}}-T_{\text{b}}^2T_{\text{e}})}{\sqrt{-\Delta}T_{\text{a}}^2}+\frac{2g_{\text{m}}T_{\text{a}}T_{\text{d}}}{\sqrt{-\Delta}C_{\text{jd}}T_{\text{c}}}$	$\frac{g_{\text{m}}L_{\text{pl}}(T_{\text{a}}T_{\text{f}}-T_{\text{b}}T_{\text{e}})}{T_{\text{a}}^2}$

1) Interval I_{on1} - Turn-on delay (t_0-t_1): Before the turn-on delay interval, the MOSFET in Fig. 1 is in the cut-off region and the Schottky diode D_{di} conducts the full load current I_{L} with a forward voltage drop $v_{\text{F}}(I_{\text{L}})$. At t_0, the bipolar gate voltage V_{g} changes from V_{EE} to V_{CC} and the MOSFET input capacitance $C_{\text{iss}}=C_{\text{gs}}+C_{\text{gd}}$ is charged. The gate-to-source voltage v_{gs} is given by

$$v_{\text{gs}}(t)=V_{\text{CC}}-(V_{\text{CC}}-V_{\text{EE}})\cdot\mathrm{e}^{-\frac{t}{R_{\text{g}}C_{\text{iss}}}}. \tag{4}$$

The MOSFET remains in the cut-off region (off-state) until the end state $v_{\text{gs}}=V_{\text{th}}$ is reached, and the load current is still fully conducted by D_{di}. No switching losses are generated in this time interval.

2) Interval I_{on2} - Current rise I (t_1-t_2): At t_1, the MOSFET channel starts to open and to conduct an increasing current. The MOSFET operates in the saturation region and the channel behaves as a current source controlled by voltage v_{gs}, as defined in (2). D_{di} is conducting the load current in the forward direction until the end state $i_{\text{ds}}=\frac{1}{2}I_{\text{L}}$ is reached. During this time interval, the circuit equations are expressed as

$$V_{\text{CC}} = R_{\text{g}}i_{\text{g}}(t)+v_{\text{gs}}(t)+L_{\text{s}}\frac{\mathrm{d}i_{\text{ds}}}{\mathrm{d}t} \tag{5}$$

$$i_{\text{g}}(t) = C_{\text{gs}}\frac{\mathrm{d}v_{\text{gs}}}{\mathrm{d}t}+C_{\text{gd}}\frac{\mathrm{d}v_{\text{gd}}}{\mathrm{d}t} \tag{6}$$

$$v_{\text{gs}}(t) = v_{\text{gd}}(t)+v_{\text{ds}}(t) \tag{7}$$

$$V_{\text{in}} = L_{\text{pl}}\frac{\mathrm{d}i_{\text{ds}}}{\mathrm{d}t}+v_{\text{ds}}(t)-v_{\text{F}}(t) \tag{8}$$

$$I_{\text{L}} = i_{\text{ds}}(t)+i_{\text{F}}(t), \tag{9}$$

where the power loop parasitic inductance is $L_{\text{pl}}=L_{\text{d}}+L_{\text{s}}+L_{\text{PCB}}+L_{\text{di}}$. Combining (2)-(3) with (5)-(9), v_{gs} can be expressed by (parameters listed in Tab. I)

$$V_{\text{CC}}=T_{\text{a}}v''_{\text{gs}}+T_{\text{n}}v'_{\text{gs}}+v_{\text{gs}}. \tag{10}$$

This is a SOLICCDE, whose solution exhibits two possible cases, as explained in Appendix V-A. With the initial conditions V_{gs0} and V'_{gs0} from interval I_{on1} at t_1, closed-form analytical equations for v_{gs} are expressed by: ($\alpha_1=V_{\text{CC}}-V_{\text{gs0}}$)

Overdamped case: $\Delta={T_{\text{n}}}^2-4T_{\text{a}}>0$

$$v_{\text{gs,o}}(t)=V_{\text{CC}}-\alpha_1\mathrm{e}^{dt}\cdot[\cosh(\omega t)-n\sinh(\omega t)], \tag{11}$$

Underdamped case: $\Delta={T_{\text{n}}}^2-4T_{\text{a}}<0$

$$v_{\text{gs,u}}(t)=V_{\text{CC}}-\alpha_1\mathrm{e}^{dt}\cdot[\cos(\omega t)-n\sin(\omega t)]. \tag{12}$$

In a next step, $i_{\text{ds}}(t)$ is calculated by (2) and $v_{\text{ds}}(t)$ is calculated by

$$v_{\text{ds}}(t)=V_{\text{in}}+k\,[I_{\text{L}}-i_{\text{ds}}(t)]+V_{\text{j}}-L_{\text{pl}}\frac{\mathrm{d}i_{\text{ds}}}{\mathrm{d}t}. \tag{13}$$

The switching time t_{on2} is calculated by solving $i_{\text{ds}}(t_{\text{on2}})=\frac{1}{2}I_{\text{L}}$. As derived in Appendix V-B1, the closed-form analytical equations for t_{on2} are given by

$$t_{\text{on2,o}} = t_{\text{I,o}} \tag{14}$$

$$t_{\text{on2,u}} = t_{\text{I,u}}. \tag{15}$$

3) Interval I_{on3} - Current rise II (t_2-t_3): Similar to interval I_{on2}, the MOSFET operates in the saturation region. D_{di} is still conducting some current until the end

state $i_{ds} = I_L$ is reached, when I_L is fully commutated from D_{di} to the MOSFET. The same equations for interval I_{on2} can also be applied to this interval with updated parameter values, as given in Tab. I.

4) Interval I_{on4} - Voltage fall I ($t_3 - t_4$): At t_3, the Schottky diode clamping ends, so that the MOSFET output capacitance $C_{oss} = C_{gd} + C_{ds}$ starts to be discharged with decreasing v_{ds} and the Schottky diode juction capacitance C_{jd} starts to be charged with increasing v_F in the reverse direction, until the end state $v_F = -\frac{1}{4}V_{in}$ is reached. During this interval, the circuit equations (5)-(9) remain the same as for interval I_{on2}, but equation (3) is changed to

$$i_F(t) = C_{jd}\frac{\mathrm{d}v_F}{\mathrm{d}t}. \tag{16}$$

Combining (2), (5)-(9), and (16), v_{gs} can be derived by

$$T_a v_{gs}'' + T_b v_{gs}' + T_c v_{gs} = T_d, \tag{17}$$

whose solution is (only the underdamped case is considered in the following sections for simplicity):

Underdamped case: $\Delta = {T_b}^2 - 4T_aT_c < 0$

$$v_{gs,u}(t) = \frac{T_d}{T_c} - \frac{T_aT_d - T_cT_e}{T_aT_c}\mathrm{e}^{dt}\cdot\cos(\omega t) - \frac{2T_aT_cT_f - T_aT_bT_d - T_bT_cT_e}{T_aT_c\sqrt{-\Delta}}\mathrm{e}^{dt}\cdot\sin(\omega t). \tag{18}$$

In a next step, $i_{ds}(t)$ is derived with (2). The diode forward voltage $v_F(t)$ can be calculated by

$$v_F(t) = \frac{1}{C_{jd}}\int [I_L - i_{ds}(t)]\,\mathrm{d}t, \tag{19}$$

which requires the end state $v_F(t_{on3})$ of interval I_{on3} to determine the constant term of the indefinite integral. In the end $v_F(t)$ can be expressed by

$$v_{F,u}(t) = \mathrm{e}^{dt}\cdot[n\sin(\omega t) + p\cos(\omega t)] + qt + m_0. \tag{20}$$

Finally, $v_{ds}(t)$ is calculated by (8). The switching time t_{on4} is calculated by solving $v_F(t_{on4}) = -\frac{1}{4}V_{in}$. As derived in Appendix V-B2, the closed-form analytical equations for t_{on4} are

$$t_{on4,o} = t_{II,o} \tag{21}$$

$$t_{on4,u} = \frac{1}{2}\left(t_{II,u,sol1} + t_{II,u,sol2}\big|_{dt=-1}\right). \tag{22}$$

5) Interval I_{on5} - Voltage fall II ($t_4 - t_5$): Similar to interval I_{on4}, C_{oss} continues to be discharged and C_{jd} continues to be charged in the reverse direction, until the end state $v_{ds} = V_{CC} - V_{th}$ is reached. The same equations for interval I_{on4} can also be applied to this interval with updated parameter values in Tab. I, except for the switching time

$$t_{on5,u} = t_{II,u,sol1}. \tag{23}$$

6) Interval I_{on6} - Voltage fall III ($t_5 - t_6$): Similar to interval I_{on4} and I_{on5}, C_{oss} continues to be discharged and C_{jd} continues to be charged in the reverse direction. The

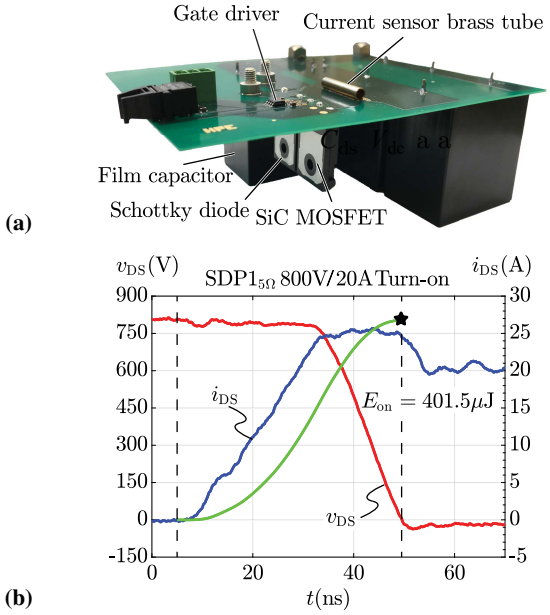

Fig. 4. **(a)** DPT PCB picture. **(b)** Measured 800 V/20 A turn-on switching waveforms for SDP1 with post-processing.

TABLE II
SWITCH DIODE PAIRS WITH GATE DRIVE CIRCUIT CONDITIONS

Name	SiC MOSFET	Schottky diode	V_g(V)	$R_{g,ext}(\Omega)$
SDP1	C3M0075120D (Cree, Planar gate)	C4D10120H (Cree)	$[-4, 15]$	2.7
SDP2	SCH2080KEC* (ROHM, Planar gate)	C4D10120H (Cree)	$[-3, 20]$	10
SDP3	SCT3040KLHR (ROHM, Trench gate)	IDWD15G120C5 (Infineon)	$[0, 18]$	5
SDP4	SCT50N120 (STMicro, Planar gate)	IDWD15G120C5 (Infineon)	$[-5, 20]$	5
SDP5	IMW120R090M1H (Infineon, Trench gate)	IDWD15G120C5 (Infineon)	$[0, 18]$	10

*: Co-packed with SiC SBD

MOSFET remains in the saturation region until the end state $v_{ds} = v_{gs} - V_{th}$ is reached, when the MOSFET enters the ohmic region. Same equations for interval I_{on4} can also be applied to this interval with updated parameter values in Tab. I, except for the switching time

$$t_{on6,u} = \begin{cases} t_{II,u,sol1}, & t_{II,u,sol2}\big|_{dt=-2} \le 0 \\ t_{II,u,sol2}\big|_{dt=-2}, & t_{II,u,sol2}\big|_{dt=-2} > 0. \end{cases} \tag{24}$$

7) Interval I_{on7} - Full gate charging ($t_6 - t_7$): At t_6, the MOSFET enters the ohmic region, while C_{jd} is charged up to the DC-link voltage. As the last switching interval of the turn-on transition, the gate voltage supply V_{CC} continues to charge C_{iss} until the end state $v_{gs} = V_{CC}$ is reached. No switching losses are generated in this interval.

Considering the parasitic inductance from the device package and in order to fairly compare with the measurement results, the turn-on switching loss of each time

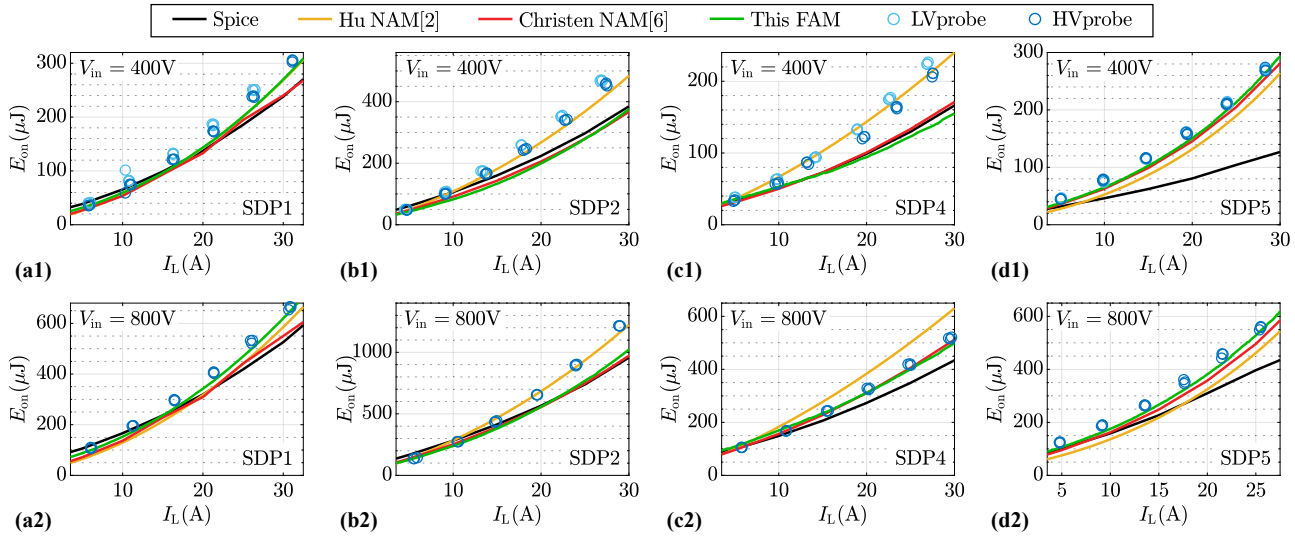

Fig. 5. Switching loss comparison between Spice simulation, the NAM in [6] (using only data sheet information), the re-evaluated NAM in [2], the proposed FAM in this paper, and DPT measurements at different operating points for different SDPs. The de-skew of the voltage and current probe is properly conducted, as supported by the good matching between the LVprobe (Lecroy PP008-1) and HVprobe (Lecroy PPE6kV) measurement results for $V_{\text{in}} = 400\,\text{V}$ in **(a1)**, **(b1)**, **(c1)**, and **(d1)**.

interval is calculated by $E_{\text{on}} = \int_{t_{\text{on}}} v_{\text{DS}} \cdot i_{\text{DS}}\,\text{d}t$, where $v_{\text{DS}} = v_{\text{ds}} + (L_{\text{d}} + L_{\text{s}})\frac{\text{d}i_{\text{ds}}}{\text{d}t}$. As closed-form analytical equations for $v_{\text{DS}}, i_{\text{DS}}, t_{\text{sw}}$ are derived above, equations for E_{on} are not shown in the paper for simplicity.

III. Model Evaluation

A. Accuracy

To verify the proposed model, a Double Pulse Test (DPT) setup is designed to measure the drain-to-source voltage v_{DS} and the drain-to-source current i_{DS}, as shown in Fig. 4a. The current i_{DS} is measured by a current sensor (inductive shunt) based on [22], with a 500 MHz bandwidth and a low insertion inductance (0.3 nH). The voltage v_{DS} is measured directly at the package pins, using either a low voltage passive probe (Lecroy PP008-1/400 V/500 MHz) or a high voltage passive probe (Lecroy PPE6kV/6 kV/400 MHz) depending on the voltage value. For the 400 V switching both voltage probes are used to verify that the de-skew of the voltage and current probe is properly conducted.

For a comprehensive verification, DUTs from different manufacturers with different structures are selected, which are grouped as 5 switch diode pairs (SDPs) as defined in Tab. II. All switching waveforms are measured with the same laboratory setup and post-processed in the same manner to calculate the switching losses. The measured voltage and current are first multiplied with each other to get the transient power, and then the power is integrated over time to obtain the switching loss energy. The end point of the switching energy integration interval is always selected at the zero crossing points of the measured voltage/current waveforms, excluding the remaining oscillation period. As an example, the 800 V/ 20 A switching waveforms and the post-processed turn-on switching loss energy of SDP1 are depicted in Fig. 4b.

Fig. 5 compares the switching loss energies calculated by the proposed FAM and those from the DPT measurements in a wide operating range (v_{DS}=[400, 800]V, i_{DS}=[5, 30]A) for different SDPs at room temperature. In addition, the switching loss energies calculated by Christen's NAM [2], Hu's NAM [6] (based on only data sheet information), and from Spice simulations are also included. Christen's NAM [2] is re-evaluated and implemented for the considered Schottky diode and SiC MOSFET half-bridge topology. Furthermore, Fig. 6 compares the switching loss energies calculated by Peng's FAM [8], Wang's FAM [13], Roy's FAM [14], and the proposed FAM. These 6 models all serve as references for evaluating the accuracy of the proposed FAM. Tab. III lists the switching loss errors calculated by different models and simulations with respect to the DPT measurements. The mean absolute percentage error is used to evaluate the accuracy, which is defined by

$$\bar{e} = \frac{1}{N}\sum_{n=1}^{N}\left|\frac{E_{\text{n,model/spice}} - E_{\text{n,meas}}}{E_{\text{n,meas}}}\right| \times 100\%. \qquad (25)$$

Considering all of the tested SDPs and based on only data sheet information, from Tab. III, the proposed FAM shows similar error values around 27-28% compared to Hu's NAM [6], although more assump-

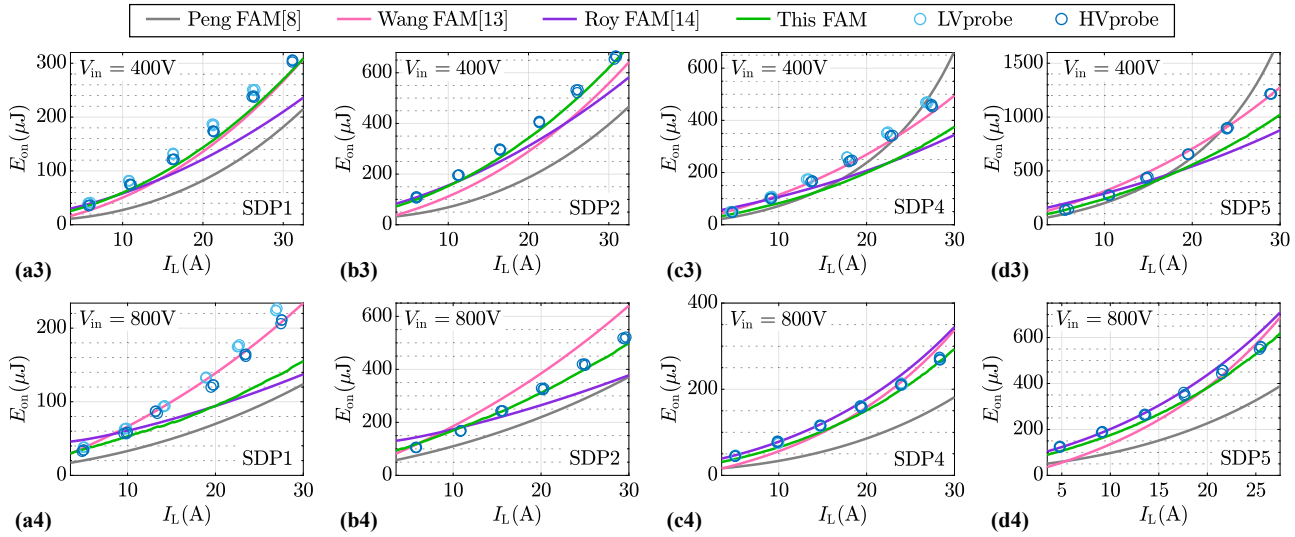

Fig. 6. Switching loss comparison between the FAMs proposed in [8], [13], [14] and this paper, and DPT measurements.

TABLE III
COMPARISON OF SWITCHING LOSS ERRORS (IN PERCENTAGE) AND COMPUTATIONAL EFFORT

	Test condition	Spice	Hu NAM [6]	Christen NAM [2]	Peng FAM [8]	Wang FAM [13]	Roy FAM [14]	This FAM	Roy* FAM [14]	This* FAM
SDP1	V_{in} = 400 V	13.60	15.49	11.55	48.72	16.38	20.50	7.87	20.40	12.71
	V_{in} = 600 V	16.01	20.82	18.34	51.70	25.28	19.15	11.08	18.93	14.88
	V_{in} = 800 V	12.90	16.43	17.31	50.32	25.25	13.96	7.68	13.81	10.88
	average	14.17	17.58	15.74	50.25	22.31	17.87	8.88	17.71	12.82
SDP2	V_{in} = 400 V	17.34	21.61	4.17	24.01	5.76	23.24	25.84	17.47	16.34
	V_{in} = 600 V	14.80	14.57	3.48	21.72	8.78	20.59	16.35	16.79	7.19
	V_{in} = 800 V	17.96	14.37	5.40	17.43	11.31	22.99	13.46	20.45	7.28
	average	16.70	16.85	4.35	21.06	8.62	22.27	18.55	18.24	10.27
SDP3	V_{in} = 400 V	26.60	61.33	111.50	75.07	122.77	45.13	69.67	18.44	20.58
	V_{in} = 600 V	33.28	76.70	126.65	94.14	139.69	51.31	94.16	14.84	11.16
	V_{in} = 800 V	36.69	87.41	135.48	106.07	151.70	52.09	108.75	10.92	29.38
	average	32.19	75.15	124.54	91.76	138.06	49.51	90.86	14.73	20.38
SDP4	V_{in} = 400 V	19.18	19.79	7.98	45.38	6.91	27.25	20.89	17.07	5.74
	V_{in} = 600 V	15.43	9.68	13.97	36.11	13.05	24.67	12.05	23.23	3.61
	V_{in} = 800 V	11.67	2.45	16.80	30.69	18.06	20.57	5.83	22.91	7.80
	average	15.43	10.64	12.92	37.39	12.67	24.16	12.92	21.07	5.72
SDP5	V_{in} = 400 V	46.20	14.16	24.61	50.13	18.46	6.33	10.31	16.91	13.14
	V_{in} = 600 V	43.61	15.07	25.74	48.54	20.51	5.56	9.64	14.17	12.58
	V_{in} = 800 V	23.43	16.13	26.55	47.39	22.79	5.29	9.48	14.68	12.92
	average	37.75	15.12	25.63	48.69	20.59	5.72	9.81	15.26	12.88
	Average error	**23.25%**	**27.07%**	**36.64%**	**49.83%**	**40.45%**	**23.91%**	**28.20%**	**17.40%**	**12.41%**
	w/o SDP3	21.01%	15.05%	14.66%	39.35%	16.05%	17.51%	12.53%	18.07%	10.42%
	$\sim$ Calculation time	$1-10^3$ s	$1-10^3$ s	50 ms	1.5 ms	0.1 ms	0.05 ms	0.85 ms**	-	-

*: Based on the device characteristics measured by a power device analyser (PDA) **: If implemented as a SAM, $\sim$ 20 ms

tions/simplifications (as listed in section II-A) are used when deriving the proposed FAM. The main reason that limits the accuracy of Hu's NAM [6] is the curve fitting of the gate-to-drain capacitance C_{gd} due to its nonlinearity. Based on the similar error values, it can be concluded that the assumptions/simplifications used for the proposed FAM are reasonable and accurate for deriving analytical switching loss models. In addition, the proposed FAM is more accurate than Christen's NAM [2], due to a larger number of piecewise constants for nonlinear characteristics and the modelling of the Schottky diode forward characteristics. Another reason limiting the accuracy of Christen's NAM [2] is that the modelling effort is mainly focused on the nonlinear transfer characteristics instead of the nonlinear capacitances, even during the voltage fall interval when

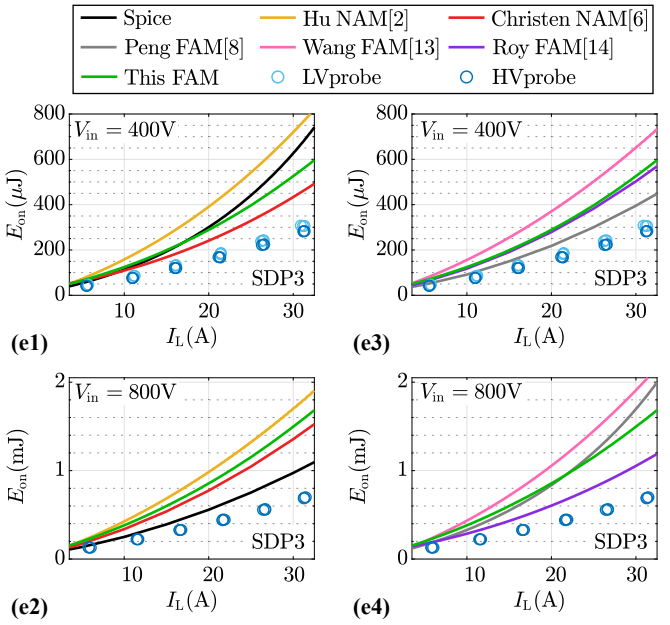

Fig. 7. Switching loss comparison for SDP3.

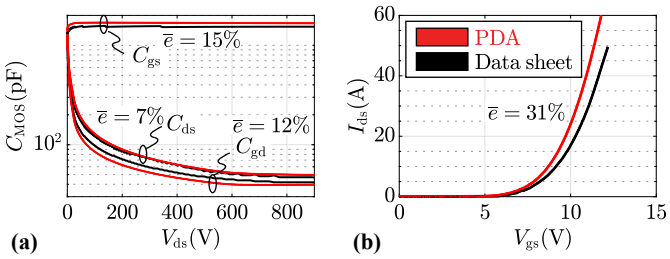

Fig. 8. Comparison of nonlinear characteristics (a) intrinsic capacitances and (b) transfer characteristics for ROHM SCT3040KLHR SiC MOSFET from data sheet and from PDA measurement. The discrepancies $\bar{e}$ are annotated (using measurement as references).

the capacitances are highly nonlinear as a result of the widely varying drain-to-source voltage.

In addition, among all FAMs, the proposed FAM is the second best model in terms of accuracy. It is 10-20% more accurate than Peng's FAM [8] and Wang's FAM [13], and is 4% less accurate than Roy's FAM [14]. Peng's FAM [8] has the lowest accuracy because the switching waveforms are completely linearised based on a constant averaged gate current in each switching interval, and the constant miller voltage assumption is used. The same linearisation is used in [13], but Wang's FAM [13] is a bit more accurate than Peng's FAM [8] due to a larger number of piecewise constants for linearisation, the modelling of the Schottky diode forward characteristics, and the modelling of the oscillating drain-to-source current i_{DS} after the current rise interval. However, Wang's FAM [13] makes direct assumptions on the switching waveform shapes without physical explanations. In addition, it adopts the energy conservation methodology for switching loss derivation, which uses the gate charge Q_g from the data sheet to calculate the gate drive losses. However, Q_g is obtained at one specific operating point, which causes inaccuracy considering the wide operating range and the various gate drive circuit conditions. Therefore, Wang's FAM [13] is less accurate than the proposed FAM. On the other hand, although Roy's FAM [14] directly neglects some terms of the formulated circuit equations based on a pure mathematical analysis, the inclusion of the nonlinear curve fitting into the analytical integration of the switching losses helps to reduce the errors and makes it the most accurate FAM (based on only data sheet information).

Unlike the other 4 SDPs under test, SDP3 shows distinctively large errors above 80%, as listed in Tab III. For SDP3, all models based on data sheet information overestimate the turn-on losses, as depicted in Fig. 7. In order to investigate the reason, a power device analyser (PDA) is used to characterise the ROHM SCT3040KLHR SiC MOSFET, whose nonlinear characteristics are shown in Fig. 8. Note that the measured device characteristics include the nonlinear MOSFET intrinsic capacitances and transfer characteristics, the Schottky diode forward characteristics and nonlinear junction capacitance, the MOSFET internal gate resistance, and all parasitic inductances of the device packages. The device characteristics are measured under the same measurement conditions as specified in the device data sheets. By using the measured device characteristics instead of the data sheet information, the errors above 80% are largely reduced to below 20%, as listed in the last two columns in Tab. III (also investigated in detail in [7]). Therefore, it can be concluded that the large error of SDP3 is caused by the inaccurate data sheet information (caused by device tolerances). Furthermore, the measured device characteristics instead of the data sheet information are applied to Roy's FAM [14] and the proposed FAM, since the error values of these two models are very similar, and the resulting errors are shown in Tab. III. With the measured device parameters, the proposed FAM is the most accurate FAM and is 5% more accurate than Roy's FAM [14].

B. Computational Effort

The execution time of the proposed FAM is approximately 0.85 millisecond when calculating the turn-on losses for one operating point, which is measured on a standard laptop (Windows 10, Intel i7-8665U processor, 16GB RAM, 1/4 cores used), as shown in Tab. III. The *Timeit* function from matlab is used and the execution

time is calculated as the mean value of 1000 runs. Although computationally expensive, all required curve fittings are excluded from the computation time measurement, because the parameters of the fitted curves only need to be calculated once during data pre-processing and are then stored in the device parameter database. Note that it is the relative comparison of execution times that shows the computational performance of different models, as the model implementation and time measurement circumstances are identical. If the closed-form analytical equations for the switching time t_{sw} are not used, as for example in SAMs proposed in [4], [15]–[18], these times need to be solved numerically, so that the execution time is roughly 20 times longer compared to that of the proposed FAM. Although Spice simulations show the best accuracy, the execution time is the longest, varying between seconds and hours depending on the operating point and the complexity of the behavioural model from the manufacturer. All FAMs show similar computational effort within a few milliseconds per operating point.

C. Discussion

Compared to the SAMs proposed in [4], [15]–[18], the key advantage of the proposed FAM is that closed-form analytical equations for the switching time t_{sw} are derived, which largely reduces the computational effort. In addition, the initial condition for the first derivative of v_{gs} is included to accurately solve the SOLICCDEs. Fig. 9 depicts the error values of the switching loss calculation for different time intervals, either including the initial condition for v'_{gs} (black bars) or neglecting it (red bars). The errors are calculated using the proposed FAM with numerically solved t_{sw} as reference values. The black bars verify the accuracy of the approximated closed-form analytical equations for t_{sw}, because compared to the numerical solutions, the total error for the complete turn-on transition is below $\pm 0.5\%$ within a wide operating range. The red bars clearly show that if the initial condition for v'_{gs} is not included, many switching intervals are largely influenced (worst case error above 60%) and the total error for the complete turn-on transition can be up to over 30% (SDP4). Also, it can be observed that large errors of approximately 30% can occur for interval 6 no matter if the initial condition for v'_{gs} is included or not. However, this does not influence significantly the total error for the complete turn-on transition, because the loss contribution of interval 6 is relatively small (always below 0.5%).

Compared to the FAMs presented in [8]–[12], the key advantage of the proposed FAM is that the constant gate miller voltage assumption, which is inaccurate due to the pronounced drain induced barrier lowering effect in state-of-the-art SiC MOSFETs [21], is not used. As shown in Tab. IV, using the constant gate miller voltage assumption increases the switching loss error by 20% compared to not using the assumption. The errors are calculated based on the proposed FAM under the same test conditions as in Tab. III.

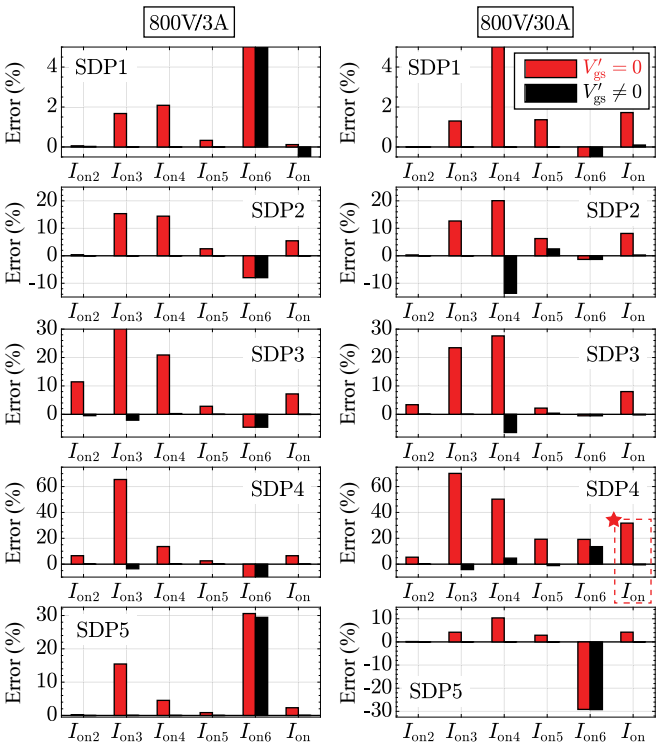

Fig. 9. Switching loss energy error for different turn-on intervals, including or neglecting the initial condition for v'_{gs}.

TABLE IV
COMPARISON OF SWITCHING LOSS ERRORS (IN PERCENTAGE)

Assum.	SDP1	SDP2	SDP3	SDP4	SDP5	**Average**
w/o V_{mil}	8.88	18.55	90.86	12.92	9.81	**28.20%**
w V_{mil}	52.28	29.81	78.51	27.98	50.35	**47.78%**

As analysed in section III-A for SDP3, the inaccurate data sheet information has a strong impact on the accuracy of analytical models. Therefore, the accuracy of any analytical model can only be guaranteed, if both the model and the device characteristics are accurate. In addition, if SDP3 is excluded, the proposed FAM is the most accurate FAM with a 12.53% turn-on loss error, and all of the analytical models have similar switching loss errors around 15% except for Peng's FAM [8]. This suggests that an error around 15% is kind of a limit for an analytical switching loss model based on only data sheet information, if a large number of devices are considered and the models are derived based on the traditional step-by-step switching interval analysis.

IV. Conclusion

In this paper, a novel fast and accurate fully analytical turn-on switching loss model for a SiC MOSFET and Schottky diode half-bridge is proposed, based on only data sheet information. The mean absolute percentage errors are around 28%, as comprehensively verified by measurements in a wide operating range using SiC MOSFETs with different device structures from different manufacturers. The resulting errors are comparable to the error of Hu's NAM [6] based on also only data sheet information. However, the computational effort is largely reduced by at least 1000 times by using the proposed FAM. With the proposed closed-form analytical equations, the computational effort is reduced by 20 times compared to the SAMs proposed in [4], [15]–[18] using similar assumptions/simplifications. Compared to the FAMs proposed in [8], [13], [14], the proposed model is the second most accurate (4% less accurate than Roy's FAM [14]) model based on only data sheet information and is the most accurate (5% more accurate than Roy's FAM [14]) model based on the measured device characteristics. Although the computational effort of the proposed model is slightly higher in comparison to the FAMs proposed in [13], [14], it remains within a few milliseconds per operating point, so that it is suitable for converter design optimisation procedures.

Furthermore, it is shown that neglecting the initial condition for the first derivative of v_{gs} could lead to large errors, when solving the second order differential equation to calculate the switching losses. Also, the commonly used constant gate miller voltage assumption typically leads to large errors. In general, the accuracy of any analytical model can only be guaranteed, if both the model and the device characteristics are accurate. A higher accuracy is achieved (mean absolute percentage error equals to 12.41%) if measured device characteristics are used in the proposed model.

V. Appendix

A. Solution of SOLICCDE

A second order linear inhomogeneous constant coefficient differential equation (SOLICCDE) is defined by

$$v''(t) + bv'(t) + cv(t) = d, \tag{26}$$

where b, c, d are constants. The general solutions for a SOLICCDE exhibit two possible cases depending on the constant values, as described in the following:

Overdamped case: $\Delta = b^2 - 4c > 0$

$$v = \mathrm{e}^{-\frac{b}{2}t} \cdot \left[C_1 \sinh\left(\tfrac{\sqrt{\Delta}}{2}t\right) + C_2 \cosh\left(\tfrac{\sqrt{\Delta}}{2}t\right)\right] + \frac{d}{c} \tag{27}$$

Underdamped case: $\Delta = b^2 - 4c < 0$

$$v = \mathrm{e}^{-\frac{b}{2}t} \cdot \left[C_1 \sin\left(\tfrac{\sqrt{-\Delta}}{2}t\right) + C_2 \cos\left(\tfrac{\sqrt{-\Delta}}{2}t\right)\right] + \frac{d}{c} \tag{28}$$

By using the initial condition of both $v(0)$ and $v'(0)$, the constants C_1 and C_2 can be solved. Comparing (27) with (28), it can be observed that the two cases are highly symmetrical, which can be utilised to reduce the effort for equation derivation.

B. Closed-form Analytical Equations for Switching Time

In general, there are two groups of equations for solving the switching time t_{sw}, separated by which variable triggers the end state of the switching interval. For the seven turn-on intervals, the end state variable of interval I_{on2} and I_{on3} is i_{ds} (linearly correlated to v_{gs} from (2)). In contrast, the end state variable of interval I_{on5} and I_{on6} is v_{ds} (for I_{on4} is v_{F}, which after analysis is proved to exhibit a similar equation pattern as v_{ds}).

1) Group I - v_{gs} Trigger:

Overdamped case:

$$\mathrm{e}^{dt}\left[\cosh(\omega t) - n\sinh(\omega t)\right] + m = 0 \tag{29}$$

Underdamped case:

$$\mathrm{e}^{dt}\left[\cos(\omega t) - n\sin(\omega t)\right] + m = 0 \tag{30}$$

Due to the complexity of these equations, assumptions need to be made to derive closed-form analytical equations for the switching time t.

For overdamped case, the hyperbolic functions are replaced by exponential functions, re-writing (29) as

$$(1-n)\mathrm{e}^{(d+\omega)t} + (1+n)\mathrm{e}^{(d-\omega)t} + 2m = 0. \tag{31}$$

After detailed analysis, the term $\mathrm{e}^{(d-\omega)t}$ can be neglected compared to the term $\mathrm{e}^{(d+\omega)t}$, which can be applied to all switching intervals. Therefore, the closed-form analytical solution is given by

$$t_{\text{I,o}} = \frac{1}{d+\omega} \cdot \ln\left(\frac{2m}{n-1}\right). \tag{32}$$

For underdamped case, $\cos(ot) = 1$ and $\sin(ot) = 0$ are assumed due to the very short switching time. Then the closed-form analytical solution is given by

$$t_{\text{I,u}} = \frac{\ln(-m)}{d}. \tag{33}$$

2) Group II - v_{ds}/v_F Trigger:

Overdamped case:

$$\mathrm{e}^{dt} \cdot \left[n\sinh(\omega t) + p\cosh(\omega t)\right] + qt + m = 0 \tag{34}$$

Underdamped case:

$$\mathrm{e}^{dt} \cdot \left[n\sin(\omega t) + p\cos(\omega t)\right] + qt + m = 0 \tag{35}$$

For overdamped case, the hyperbolic functions are replaced by exponential functions, re-writing (34) as

$$(n+p)\mathrm{e}^{(d+\omega)t} - (n-p)\mathrm{e}^{(d-\omega)t} + 2qt + 2m = 0. \tag{36}$$

After detailed analysis, the term $\mathrm{e}^{(d-\omega)t}$ can be neglected compared to the term $\mathrm{e}^{(d+\omega)t}$, which can be applied to all switching intervals. By using the LambertW function

$W(x)$, which represents the solution y of the equation $y\mathrm{e}^y = x$ for real number x, the closed-form analytical solution is given by

$$t_{\mathrm{II,o}} = \left| \frac{m}{q} + \frac{1}{d+\omega} \cdot W\left[\frac{(d+\omega)(n+p)}{2q} \mathrm{e}^{-\frac{m(d+\omega)}{q}} \right] \right|. \quad (37)$$

For underdamped case, it is more difficult to derive accurate closed-form analytical equations, therefore two strategies are used. The first one assumes $\cos(\omega t) = 1$ and $\sin(\omega t) = 0$ due to the very short switching time of SiC MOSFET, which simplifies (35) as

$$p\mathrm{e}^{dt} + qt + m = 0. \quad (38)$$

Then the closed-form analytical solution is given by

$$t_{\mathrm{II,u,sol1}} = \left| -\frac{m}{q} - \frac{1}{d} \cdot W\left[\frac{dp}{q} \mathrm{e}^{-\frac{md}{q}} \right] \right|. \quad (39)$$

The second one assumes $\cos(\omega t) = 1$ and keeps $\sin(\omega t) = \omega t$. The exponent dt is assumed to be a constant value (-1 or -2). Then the closed-form analytical solution is given by

$$t_{\mathrm{II,u,sol2}}\Big|_{dt=c} = -\frac{m + p \cdot \mathrm{e}^c}{q + no \cdot \mathrm{e}^c}, c = -1 \text{ or } -2. \quad (40)$$

Depending on different switching intervals, either $t_{\mathrm{u,sol1}}$, $t_{\mathrm{u,sol2}}$, or their average is selected for a higher accuracy, as written in Section II-C.

REFERENCES

[1] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si - Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors," *IEEE Trans. on Industrial Electronics*, vol. 58, no. 7, pp. 2872–2882, 2011.

[2] D. Christen and J. Biela, "Analytical Switching Loss Modeling Based on Datasheet Parameters for MOSFETs in a Half-Bridge," *IEEE Trans. on Power Electronics*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019.

[3] J. Biela and J. W. Kolar, "Pareto-Optimal Design and Performance Mapping of Telecom Rectifier Concepts," in *PCIM China*, 2010.

[4] Yuancheng Ren, Ming Xu, Jinghai Zhou, and F. C. Lee, "Analytical Loss Model of Power MOSFET," *IEEE Trans. on Power Electronics*, vol. 21, no. 2, pp. 310–319, Mar. 2006.

[5] J. W. Kolar, J. Biela, and J. Minibock, "Exploring the Pareto Front of Multi-Objective Single-Phase PFC Rectifier Design Optimization - 99.2% efficiency vs. 7kW/dm^3 Power Density," in *PEMC*, 2009.

[6] A. Hu and J. Biela, "An Analytical Switching Loss Model for a SiC MOSFET and Schottky Diode Half-Bridge Based on Nonlinear Differential Equations," in *EPE*, Sep. 2021.

[7] A. Hu and J. Biela, "Verification and Application of an Analytical Switching Loss Model for a SiC MOSFET and Schottky Diode Half-Bridge," in *ECCE Asia*, May 2022.

[8] K. Peng, S. Eskandari, and E. Santi, "Analytical Loss Model for Power Converters with SiC MOSFET and SiC Schottky Diode Pair," in *ECCE*, Sep. 2015.

[9] A. Hu and J. Biela, "Evaluation of the I_{max}-f_{sw}-dv/dt Trade-off of High Voltage SiC MOSFETs Based on an Analytical Switching Loss Model," in *EPE*, Sep. 2020.

[10] C. Qian, Z. Wang, G. Xin, and X. Shi, "Datasheet Driven Switching Loss, Turn-ON/OFF Overvoltage, di/dt, and dv/dt Prediction Method for SiC MOSFET," *IEEE Trans. on Power Electron.*, vol. 37, no. 8, pp. 9551–9570, 2022.

[11] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd ed. John Wiley and Sons Inc, 2003.

[12] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 1st ed. Springer, Boston, MA, 2008.

[13] X. Wang, Z. Zhao, K. Li, Y. Zhu, and K. Chen, "Analytical Methodology for Loss Calculation of SiC MOSFETs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 71–83, Mar. 2019.

[14] S. K. Roy and K. Basu, "Analytical Estimation of Turn on Switching Loss of SiC MOSFET and Schottky Diode Pair From Datasheet Parameters," *IEEE Trans. on Power Electronics*, vol. 34, no. 9, pp. 9118–9130, Sep. 2019.

[15] D. A. Grant and J. Gowar, *Power MOSFETs: Theory and applications*. Wiley, 1989.

[16] M. Rodriguez, A. Rodriguez, P. F. Miaja, D. G. Lamar, and J. S. Zuniga, "An Insight into the Switching Process of Power MOSFETs: An Improved Analytical Losses Model," *IEEE Trans. on Power Electronics*, vol. 25, no. 6, pp. 1626–1640, Jun. 2010.

[17] J. Wang, H. S. Chung, and R. T. Li, "Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance," *IEEE Trans. on Power Electronics*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[18] Z. Dong, X. Wu, H. Xu, N. Ren, and K. Sheng, "Accurate Analytical Switching-On Loss Model of SiC MOSFET Considering Dynamic Transfer Characteristic and Q_{gd}," *IEEE Trans. on Power Electronics*, vol. 35, no. 11, pp. 12 264–12 273, 2020.

[19] M. R. Ahmed, R. Todd, and A. J. Forsyth, "Predicting SiC MOSFET Behavior Under Hard-Switching, Soft-Switching, and False Turn-On Conditions," *IEEE Trans. on Industrial Electronics*, vol. 64, no. 11, pp. 9001–9011, Nov. 2017.

[20] K. Wang, X. Yang, H. Li, H. Ma, X. Zeng, and W. Chen, "An Analytical Switching Process Model of Low-Voltage eGaN HEMTs for Loss Calculation," *IEEE Trans. on Power Electronics*, vol. 31, no. 1, pp. 635–647, 2016.

[21] P. Hofstetter, R. W. Maier, and M. Bakran, "Influence of the Threshold Voltage Hysteresis and the Drain Induced Barrier Lowering on the Dynamic Transfer Characteristic of SiC Power MOSFETs," in *APEC*, 2019.

[22] E. Hoene, A. Ostmann, B. Lai, C. Marczok, A. Müsing, and J. W. Kolar, "Ultra-Low-Inductance Power Module for Fast Switching Semiconductors," in *PCIM Europe*, 2013.