Development, Assembly and Testing of a Power Supply System for a Hyperloop Prototype

Bachelor Thesis

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Development, Assembly and Testing of a Power Supply System for a Hyperloop Prototype

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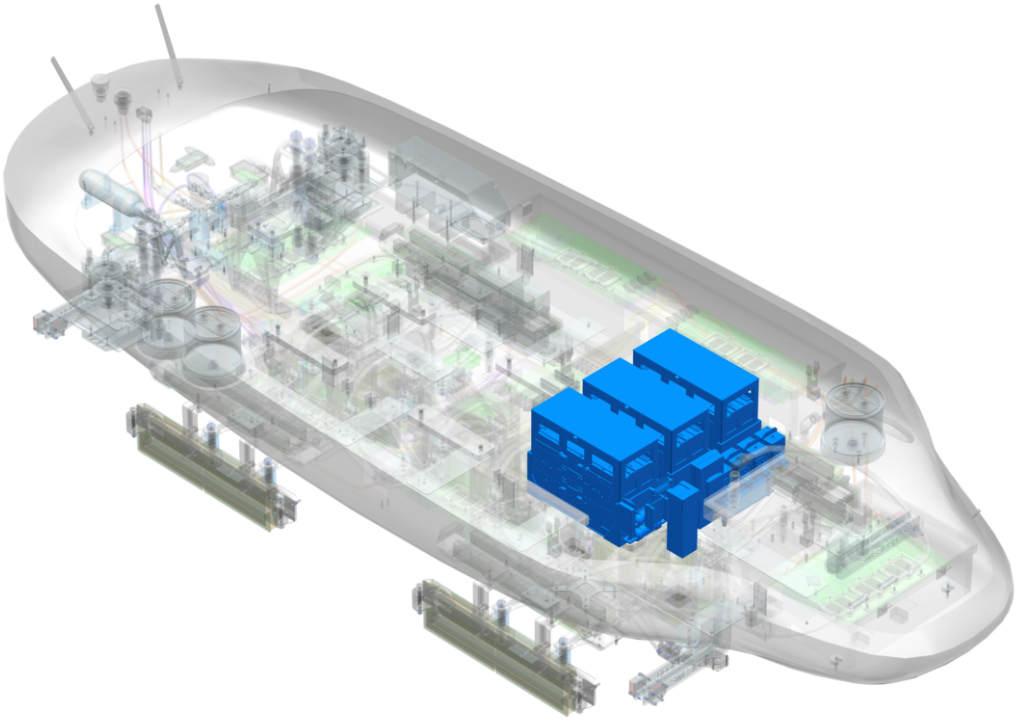
Bachelor's Thesis July 2023



Professor Prof. Dr. Jürgen Biela, jbiela@ethz.ch

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Abstract

This thesis presents the development of an advanced battery system within Swissloop's continuous efforts to advance Hyperloop technology. For the 2023 prototype, several innovations were introduced, including a new Double Sided Reluctance Motor and levitation system. These additions necessitated the creation of a new power supply system capable of meeting their energy requirements. To fulfill these demands, custom-made Lithium Polymer (LiPo) batteries were manufactured, and an improved Battery Management System was designed, assembled, and subjected to thorough testing. The system boasts a high level of autonomy and can be easily detached from the prototype when necessary. It incorporates newly developed software based on FreeRTOS and actively monitors 292 individual sensors to ensure the safety of the battery system.

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List of Acronyms

ADC	Analog to Digital Converter
BMS	Battery Management System
CAD	Computer Aided Design
CAN FD	Control Area Network Flexible Data-Rate
DC	Direct Current
EHW	European Hyperloop Week
EMI	Electromagnetic Interference
FMEA	Failure Mode and Effects Analysis
FPGA	Field Programmable Gate Array
GPPCB	General Purpose Printed Circuit Board
HV	High Voltage
ICU	Inverter Control Unit
IMD	Isolation Monitoring Device
LCU	Levitation Control Unit
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LiPo	Lithium Polymer
LV	Low Voltage
MCU	Microcontroller Unit
PCB	Printed Circuit Board
RMS	Root Mean Square
UART	Universal Asynchronous Receiver Transmitter
VCU	Vehicle Control Unit
VFSM	Virtual Finite State Machine

Chapter 1

Introduction

1.1 Hyperloop

The Hyperloop concept aims to revolutionize transportation by providing fast, comfortable, and environmentally friendly travel. It achieves this through the use of a vacuum tube and electromagnetic suspension and propulsion systems. By minimizing drag, vibrations, and rolling resistance, the Hyperloop enables speeds exceeding 800 km/h, this which has the potential to reduce long rail journeys to just an hour and possibly replace short- to mid-distance air travel.
However, several technical challenges still need to be addressed for Hyperloop technology to become a practical reality. These include the development of reliable and efficient levitation systems, linear electromagnetic motors for propulsion, effective thermal management solutions, and cost-effective infrastructure. To tackle these issues, numerous private organizations, research institutes, and state-sponsored associations are actively working on solutions and advancements in these areas.
Furthermore, student teams participate in international competitions where they construct functional, scaled-down Hyperloop vehicles within a single academic year. These competitions showcase prototypes and the technologies developed by these teams. Since 2019, the European Hyperloop Week (EHW) provides a platform for displaying these prototypes and exchanging knowledge and ideas among participants and enthusiasts.

1.2 Swissloop

Swissloop [1] is a student-led initiative dedicated to advancing Hyperloop technology and its real-world application. The team's primary objective is to contribute to the research and development of this innovative mode of transportation. They achieve this by designing and constructing functional prototypes of transport capsules, known as "pods," which is used to compete in international competitions and participate in conferences.
By participating in these events, Swissloop aims to make contributions to the ongoing progress of Hyperloop technology. Additionally, they seek to gain valuable practical experience in both the technical and operational aspects of the project. This hands-on involvement allows the team members to deepen their understanding of the technology and enhance their skills.
Swissloop has currently 35 active members and designs a new prototype each year. This allows Swissloop to explore new technologies at a rapid pace, while preserving knowledge of past iterations through knowledge transfer from former members.
In 2023, Swissloop is enhancing their award-winning linear switched reluctance motor, which was successfully implemented the previous year. The ambitious objective is to triple its top speed, aiming for 80 km/h. Moreover, Swissloop is introducing an new levitation system, enabling the entire system to remain airborne even during strong accelerations.
To meet the increased power demands of these two systems, a significant redesign of the power supply system becomes imperative. The development of this redesigned battery system is thoroughly described in this thesis.

1.3 Scope

The document begins with a brief overview of the system's requirements and operational environment. It then proceeds to compare the new power supply system's objectives with the previous one's. Next, the system architecture is examined in detail, including the low voltage schematics, code architecture and high voltage topology. The design implementations section discusses the batteries, their integration, and the Master PCB of the Battery Management System (BMS), providing detailed explanations. Additionally, the document discusses the current and voltage measurements of the system during operation. Finally, the practical learnings are summarized, and recommendations are formulated for future work in the conclusion and outlook section.

Chapter 2

Background

This chapter aims to provide information on the motivation behind the project and its realization. It explores the specific environment in which the project is implemented and examines the evolution of the power supply system through previous iterations. Additionally, the chapter outlines the requirements that the final power supply system must meet to fulfill its intended purpose.

2.1 Problem Setting

Two of the main goals of Swissloop this year are complete levitation in all directions and to achieve high speeds of up to 80 km/h. Since there is limited track length of 60 m, high speeds can only be reached with high acceleration.
To reach the first goal, a new Double Sided Linear Switched Reluctance Motor has been designed by Noël Strasser. The motor has a fully prototype-sided active part, which enables the track to be built cost-efficiently from passive material like steel or aluminium. The propulsion system is visible in Figure 2.1.

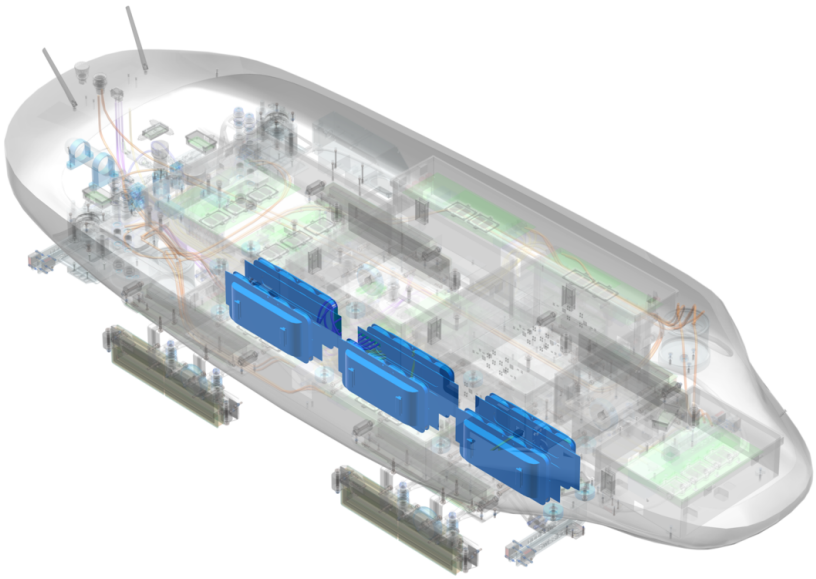

Figure 2.1: Propulsion system overview with motor sets marked in blue. All renderings were created with Siemens NX [2] if not noted otherwise.

To reach the second goal, a Levitation system consisting of four lateral and four vertical guide units has been designed by Yanik Schwab. All Units have integrated electromagnetic coils to allow for variable electromagnetic force, whereby the vertical levitation system also boosts additional permanent magnets to compensate for the constant force of gravity. The levitation system is visible in Figure 2.2.

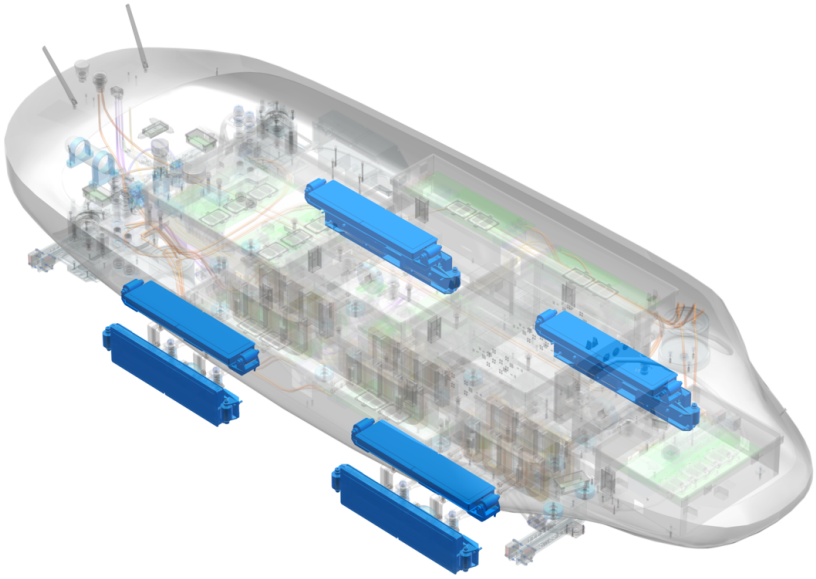

Figure 2.2: Levitation system overview with levitation sets marked in blue

To meet the power requirements of those two systems a powerful energy supply system is needed. The development, assembly and testing of this system is the topic of this thesis. To determine at what current and voltage those systems should operate a few calculation were considered:

2.1.1 Reluctance Force

The acceleration of the Prototype is directly influenced by the reluctance force produced by the Motor. To convert magnetic flux into mechanical power, a reluctance circuit is utilized, comprising an electric coil and a ferromagnetic core. When current flows through the coils, a magnetic field is generated. Due to the higher magnetic permeability of the ferromagnetic core compared to air, the magnetic field is predominantly guided through the core. This allows the reluctance circuit to effectively convert magnetic flux into mechanical power.

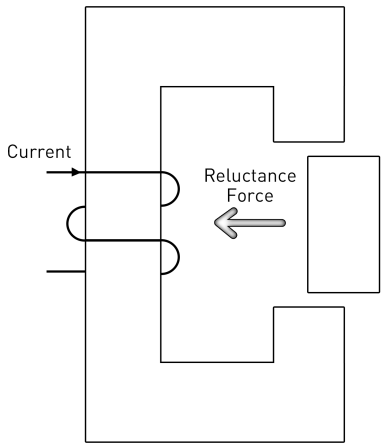

Figure 2.3: Reluctance circuit

The formula for reluctance force is as follows:

$$F_R = -\left(\frac{\partial W_m}{\partial x}\right)_{\Psi=\text{const}} = \left(\frac{\partial W_m}{\partial x}\right)_{\text{I=const}}, \tag{2.1}$$

where W_m represent the magnetic energy, ∂x denotes the position element, and Ψ represents the total flux linkage. By substituting W_m with the formula for the magnetically stored energy in an inductor, namely $W_m = \frac{1}{2}LI^2$, and assuming a constant current, we obtain the following expression:

$$F_R = \frac{1}{2}\frac{\partial L}{\partial x}I^2, \tag{2.2}$$

The magnetic energy is dependent on the square of the current flowing through the inductor and the gradient of the inductance. Consequently, achieving high acceleration necessitates the utilization of high currents. [3]

2.1.2 Rise time

When a direct current (DC) voltage is applied to a coil, a current begins to flow through the circuit, following the time-dependent relationship:

$$U = L\frac{di}{dt}. \tag{2.3}$$

where U represents the voltage, L denotes the inductance, and $\frac{di}{dt}$ indicates the rate of change of current with respect to time. Assuming a constant voltage and inductance, and after integrating the equation, we can rearrange it to obtain the rise time:

$$t_R = L\frac{I}{U}. \tag{2.4}$$

In our specific application, a low rise time is desired due to its benefits for current control in the coils. This characteristic is crucial for ensuring acceleration is maintained even at high speeds. Additionally, low rise time improves the responsiveness of the levitation system, leading to increased stability. Since high current is required for acceleration, it is important to have high voltage to reduce rise time.

2.1.3 Further Requirements of the Power Supply System

Apart from the above discussed advantages of high voltage and currents there are a few more important requirements that were considered in the design of the power supply system.

1. The system needs to comply with every safety rule of the EHW. Furthermore all crucial safety mechanism should be introduced redundantly with hardware as well as software. The result of this thesis is used in a prototype that also uses new inverters. Therefore the system needs to be able to handle a possible catastrophic inverter failure.
2. The system needs to monitor voltage and temperature of each battery cell and be redundantly safe in general
3. The system needs to work completely isolated from all other subsystems and operate safely even if all other systems have failed or malfunction. The system should also be removable from the rest of the prototype. To allow for an easier assembly and disassembly of the batteries.
4. The system should be simple to operate and require minimal maintenance.
5. The system should be as small as possible and weigh less than 30 kg.
6. The system should store at least 1 kWh to allow for a full day of testing the prototype without needing to recharge.

2.2 Choice of Energy Storage

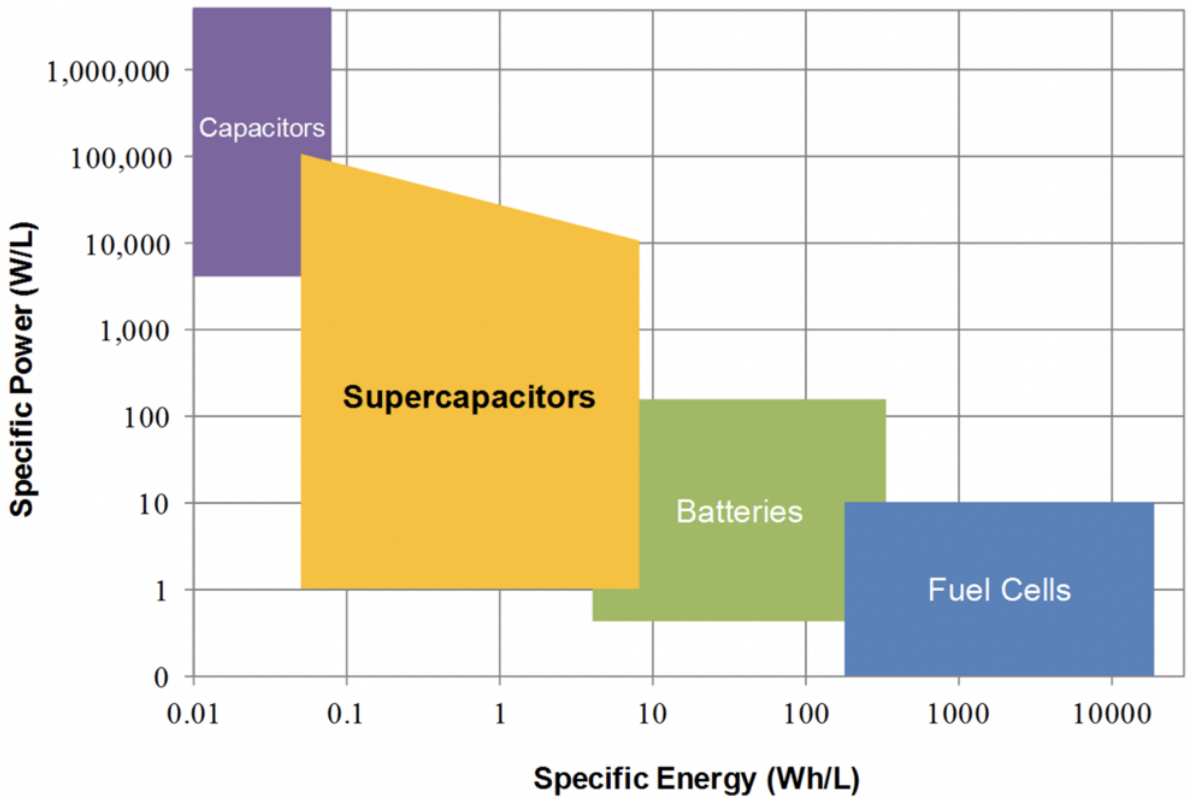

Figure 2.4: Comparison of different energy storage devices [4])(

Several energy storage options were evaluated for the power supply of the prototype. However, due to the limited track lengths expected in the near future for Swissloop prototypes, the primary consideration was not high energy capacity. Hence, everything to the right of batteries in Figure 2.4 can be disregarded. Supercapacitors were found to be intriguing due to their high power density, virtually unlimited cycle life, and rapid charging capabilities. However, it is important to note that one major drawback of supercapacitors is their inability to provide a stable voltage output like batteries. To overcome this, an additional boost converter would be required, which would've exceeded the available resources. Further exploration of their implementation could be undertaken in future research, particularly if there is a greater emphasis on regenerative braking.

Building on knowledge from previous years and considering the advantages of LiPo Batteries such as:

- High Energy Density: LiPo batteries have a high energy density, which means they can store a large amount of energy in a compact size. This makes them well-suited for this applications where space and weight are critical.
- High Discharge Rates: LiPo batteries can provide high discharge rates, allowing for the delivery of high bursts of power when needed. This allows for the necessary high currents requested by the levitation and propulsion systems.
- High Voltage: LiPo batteries have a higher nominal voltage compared to other common rechargeable battery types, such as nickel-cadmium (NiCd) or nickel-metal hydride (NiMH) batteries. This allows the system to reach higher voltage with less cells. [5]

New custom-made LiPo batteries were ordered from Swaytronic [6] to use for energy storage. Section 4.1.1 provides more details about the batteries.

2.3 Outline and Constraints Power Supply 2023

The decision was reached to design one single box containing the entire battery system. It consists of 24 lithium-polymer battery packs and has a maximum voltage of 823 V. The box contains additional electronics, including the BMS, which is responsible for monitoring each individual battery cell, and an IMD to ensure proper isolation of the different potentials. The batteries can provide currents of up to 250 A and power of up to 203kW.

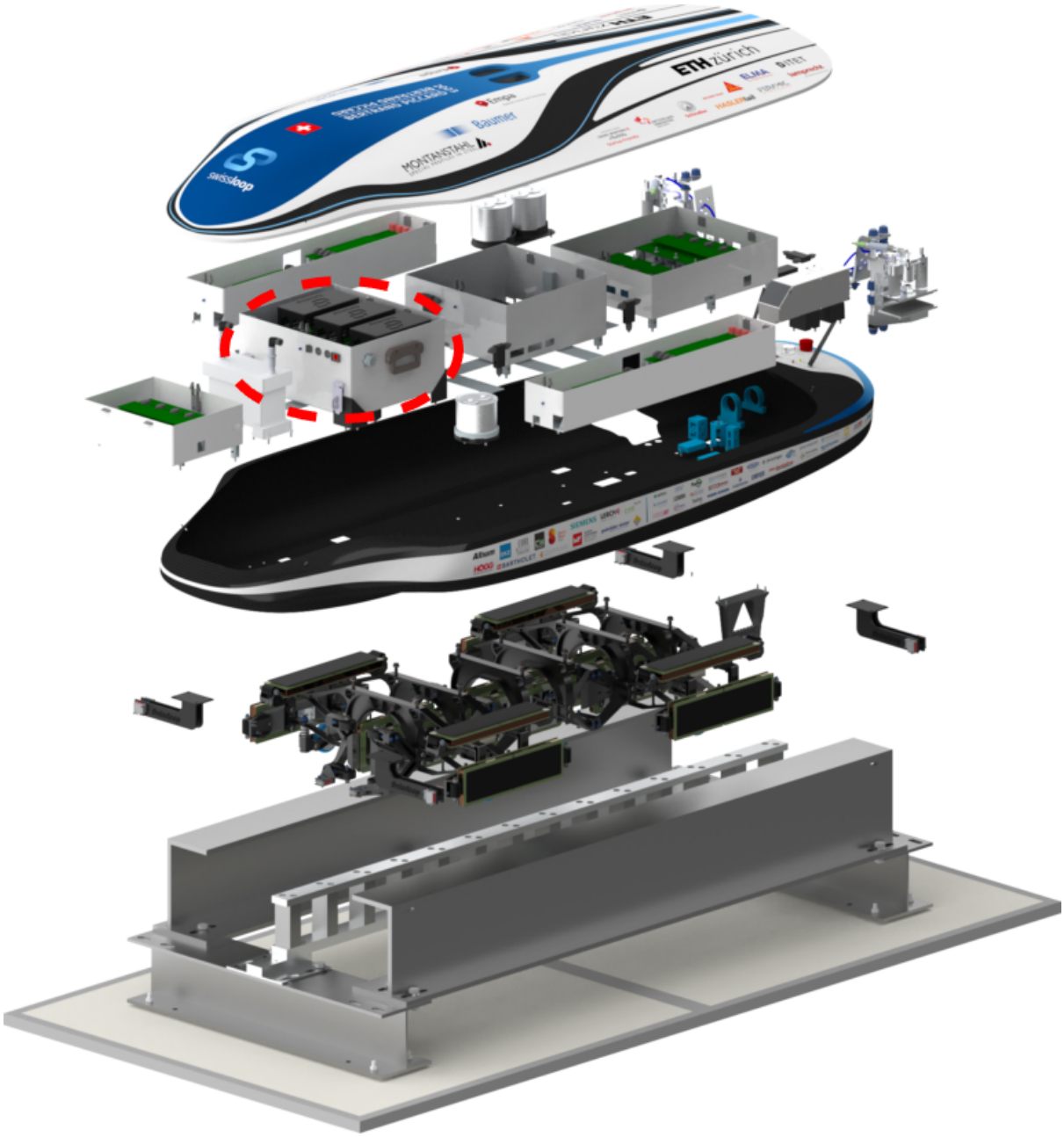

Figure 2.5: Explosion view of the 2023 Swissloop prototype Betrand Piccard[7]

In Figure 2.5 the battery box is the larger box in the middle left with the gray handle and the three black boxes on the inside. In the end, the following constraints were set to the battery box :

Table 2.1: Battery Box Constraints

With	Length	Height	Weight	Volume
400 mm	300 mm	180mm	26 kg	21.6 l

The System has two connections linking it to other subsystems, one is the High Voltage (HV)-connector visible next to the handle in the picture above which is the power output. The second one is a harting connector for Control Area Network Flexible Data-Rate (CAN FD) communication with the VCU.
The next section will compare the new system to the 2022 battery system and cover the major changes and improvements.

2.4 Previous Swissloop Battery Systems

Swissloop has been consistently designing and developing an enhanced Battery Management System (BMS) every year since 2019, incorporating the experience of previous iterations. In 2022, Noah Kim took charge of designing and developing the power supply system, and this section will highlight the enhancements that were made to his design as well as the parts that were reused from his design.[8]

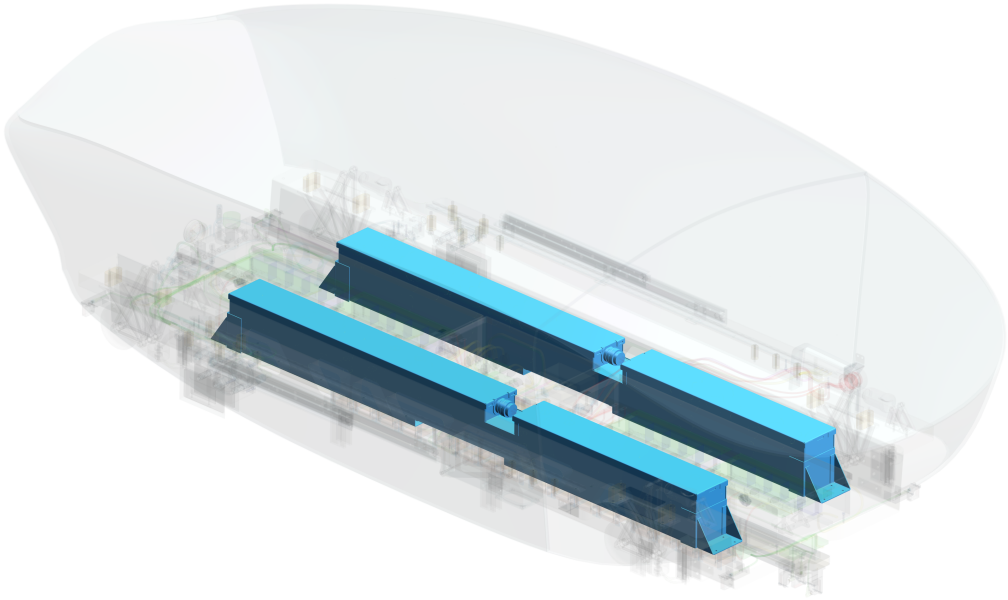

Figure 2.6: Battery System in the 2022 Swissloop prototype Lavina Heisenberg

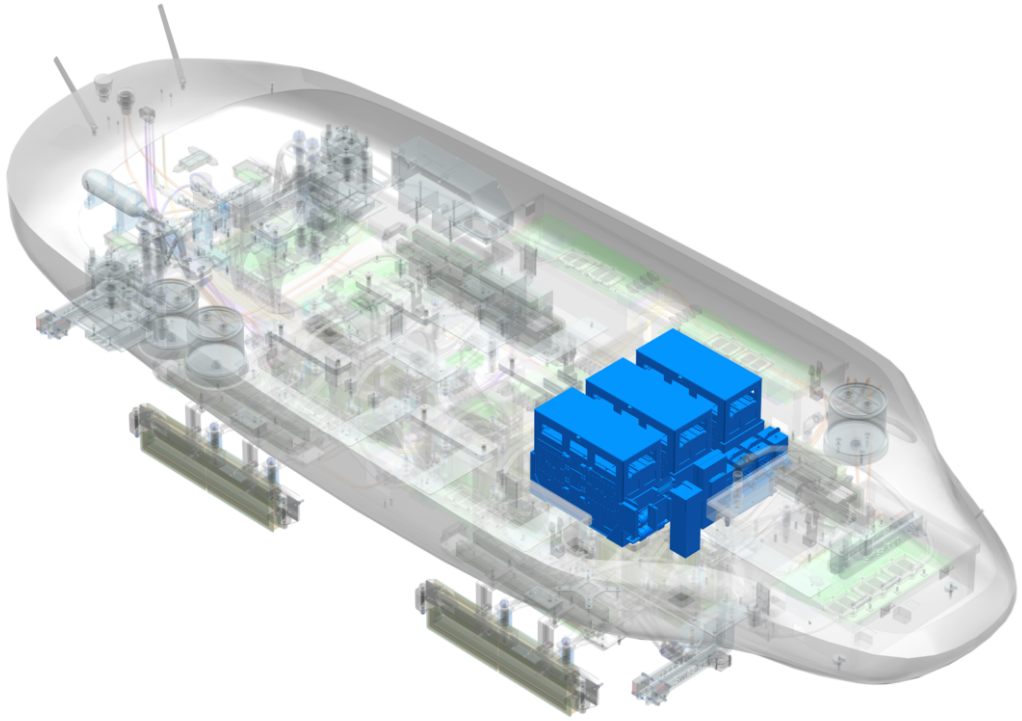

Figure 2.7: Battery System in the 2023 prototype Betrand Piccard

Table 2.2: Comparsion of the Battery System of 2022 and 2023

	Battery System 2022	Battery System 2023	Relative Change
Battery Box(es)	2	1	-50%
Battery Packs in Series	12	24	+100%
Battery Packs in Parallel	2	1	-50%
Nominal Voltage	355V	710V	+100%
Max Voltage	412V	823V	+100%
Max Current	305A	249A	-18%
Max Power	126kW	203kW	+62%
Energy	7'282Wh	2'060Wh	-72%
Weight	64kg	26kg	-59%
Volume	52.3l	21.6l	-59%
Time Precharge	15s	1s	-93%
Time Discharge	>180s	1s	-99%

2.4.1 Major Changes to the previous year

In 2022, several aspects of the Battery system were identified as areas requiring improvement. The following are the significant enhancements addressed during the year, roughly ordered in declining significance:

1. The code from the Battery Management System (BMS) in 2022 was a compilation of many code snippets from different authors and iterations. There were many outdated or faulty functions in the libraries and the code lacked consistency. It struggled with memory management and frequent timeouts. To address those issues, the code was rebuilt and restructured almost entirely on the basis of the Real-Time Operating System FreeRTOS. The advantages of FreeRTOS will be discussed in the Section 3.2.2.

2. The batteries of last year were only able to provide a voltage of 360 V nominal in comparison to the 710 V nominal they can provide this year. This increase was accomplished by maintaining the same number of cells but connecting them all in a series configuration. Unlike the previous year's cells, which were partially connected in parallel. The new cells are more powerful and capable of delivering higher currents. Consequently, the overall maximum current that can be drawn from the batteries remains approximately the same. The Batteries will be covered in more detail in Section 4.1.1

3. The two separate battery boxes visible in Figure 2.6, while being structurally reasonable, were inconvenient in any other way. They could not directly communicate with each other. Instead they each communicated with the Vehicle Control Unit (VCU) independently. This year they were merged into one centralized battery box. There are a lot of justifications for this. This design improvement enables the box to have complete control over all the batteries, rather than just half of them. As a result, there is no longer a need for a separate subsystem to handle communication between two systems. This reduction in subsystems allows for significant hardware simplification since only one battery system is now required. Additionally, with the elimination of the extra system, there is one less component that could potentially experience failure.

4. In the 2022 Version the precharge of the inverter capacitors took about 15s and since there was no discharge resistor for the capacitors it took at least 3 minutes until they discharged over the resistors of the voltage sensors in the inverters. To adress this issue, the resistance of the precharge resistor was quartered and a new discharge circuit was introduced to both pre- and discharge the capacitors in under a second. This enhances both the speed of testing as well as safety. The Pre- and Discharge will be covered in more detail in Section 4.3

5. Experience from the previous year has shown that the batteries were oversized in terms of capacity, hence this year the capacity was reduced by a factor of approximately four subsequently the weight was also reduced by roughly a factor of three.

Structurally the battery box has lost significance since it is a lot lighter and smaller in comparison to other subsystems in 2023.

2.4.2 PCBs that have been adopted from the previous year

In 2022, the Slave BMSs were newly designed and will be utilized again this year. These Slave BMSs units have the responsibility of monitoring 16 cells each, collecting data on their temperatures and voltages, and transmitting this information to the Master BMS.
Furthermore, the Slave BMSs units are capable of performing cell balancing during the charging process or inbetween runs. This allows for equalization of the charge levels among the cells, ensuring optimal performance and longevity of the battery pack.

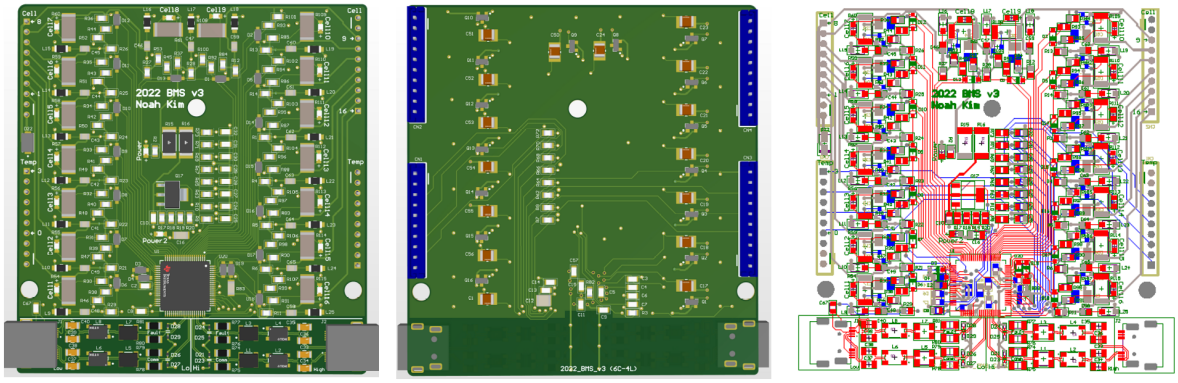

Figure 2.8: Battery Monitoring Board. All renderings of PCB's were created with Altium Designer [9]

Since the board is designed for two battery packs with each eight cells, the same battery pack configuration was requested from our battery manufacturer Swaytronic this year.

Chapter 3

System Architecture

This chapter presents a comprehensive overview of the architecture of the designed system. It delves into the architecture of the entire system, providing detailed insights into the relay gate control, HV topology, and code architecture.

3.1 System Overview

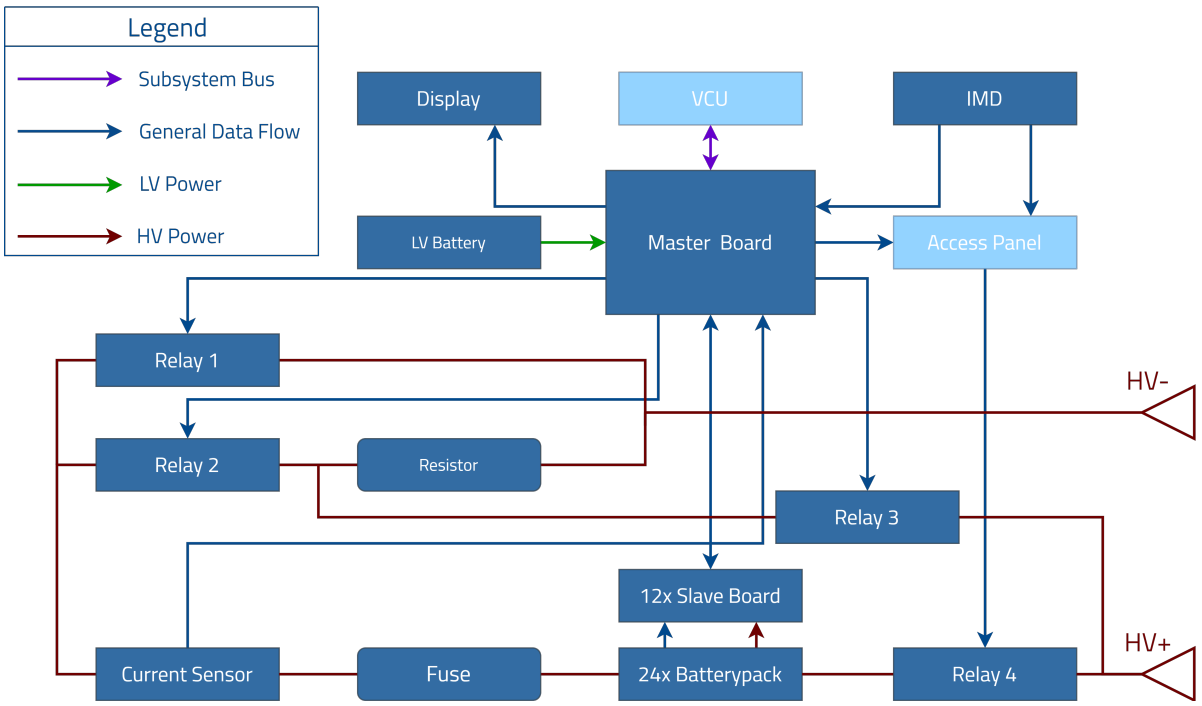

Figure 3.1: System overview of Batteries and Battery Management System (BMS) [10]

At the core of the system is the Master BMS PCB), which serves as the central control unit. Connected to the Master PCB are 12 Slave PCBs, each responsible for monitoring 16 individual cells in two battery packs. Together, the Slave and Master PCBs enable the monitoring of temperature and voltage across all 192 LiPo cells.
In addition to cell monitoring, the Master PCB communicates with the IMD, a safety component that detects faults in electrical isolation. An external display is installed on the battery box, providing direct information on the battery's status. The Master PCB is powered by a separate LV battery to ensure independence from other LV systems.

When connected within the pod, the BMS maintains constant communication with the VCU and sends two signals to LEDs on the back of the prototype. These signals indicate if the IMD has detected a fault and whether HV is enabled.
Figure 3.1 presents an overview of the entire BMS, highlighting the crucial connections. Components inside the battery box are depicted in dark blue, while external parts are represented in light blue. To enhance readability, the LV power connections from the Master Board to the Display and the IMD and the connections of the Master Board and IMD to the HV power lines are omitted. The next section will discuss the architecture of the code in more detail.

3.2 Code Architecture

3.2.1 Virtual Finite State Machine

The BMS operates on the basis of a Virtual Finite State Machine represented in Figure 3.2. All transition between states are automatic or by request of the VCU. Every request is reviewed by the Microcontroller Unit (MCU) and a transition is only accepted if all safety conditions are met. The only exception is the transition to emergency which is always accepted instantly for obvious safety reasons.

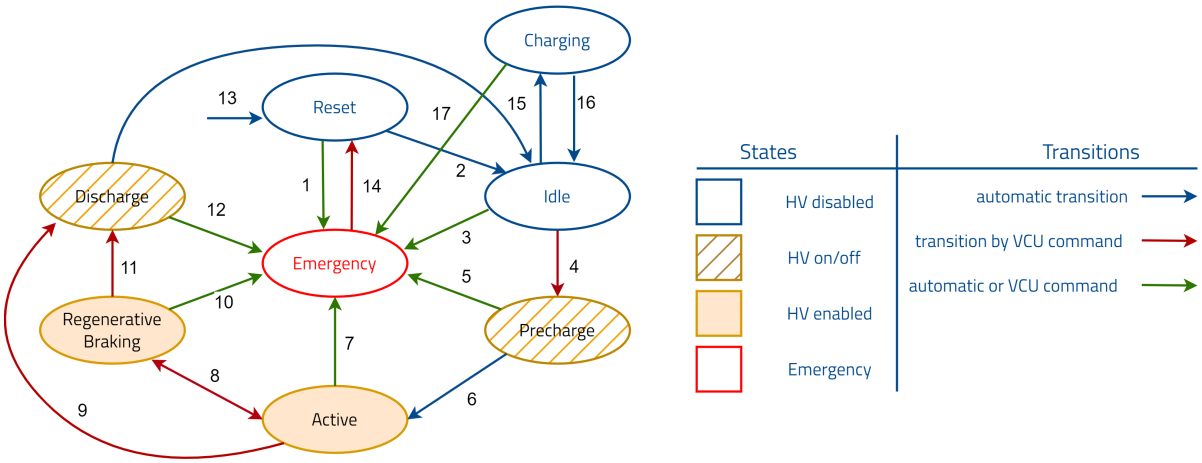

Figure 3.2: State Machine of the BMS

The Virtual Finite State Machine (VFSM) of the BMS has the following states:

- **Reset**: initial state, all peripherals of the MCU are initialised. If possible, communication with VCU is established.
- **Idle**: The BMS is passively balancing the cells and in constant communication with the VCU. High Voltage is disabled.
- **Precharge**: The BMS charges the inverters to prepare for a run. The batteries are connected to the inverters with a small resistance in series. In Figure 3.1 Relay 2 and 4 are closed while Relay 1 and 3 remain open.
- **Active**: Batteries are directly connected to the inverters of levitation and propulsion to provide and absorb power. The BMS is closely monitoring the current and voltage at the batteries. In Figure 3.1 Relay 1 and 4 are closed while Relay 2 and 3 remain open.
- **Regenerative Braking**: This state is similar to the active state. However during the electromagnetic recuperation different voltage and current limits are in place. In Figure 3.1 Relay 1 and 4 are closed while Relay 2 and 3 remain open.
- **Discharge**: The BMS connects a resistor to the inverters, until the inverters are powerless. In Figure 3.1 Relay 3 is closed while Relay 1, 2 and 4 remain open.

- **Emergency**: An error was detected either by the VCU, BMS, Inverter Control Unit (ICU), Levitation Control Unit (LCU) or the operator. The BMS opens all relays except the Relay 3 which is closed in order to discharge the Direct Current (DC)-Link capacitors. The emergency reason is displayed on the Control Panel.

The conditions for the automatic transition between the states are described in the appendix B. In addition to all described transitions it is possible to manually enter the emergency state from any state at any time.
The code always starts in the state reset. From there it either transitions into idle or emergency. A normal circle performed during operation would be: Reset, Idle, Precharge, Active, Discharge, Idle. In Figure 3.3 such a cycle is highlighted. The state regenerative braking could be integrated in the cycle as soon as the safety of regenerative braking is ensured.

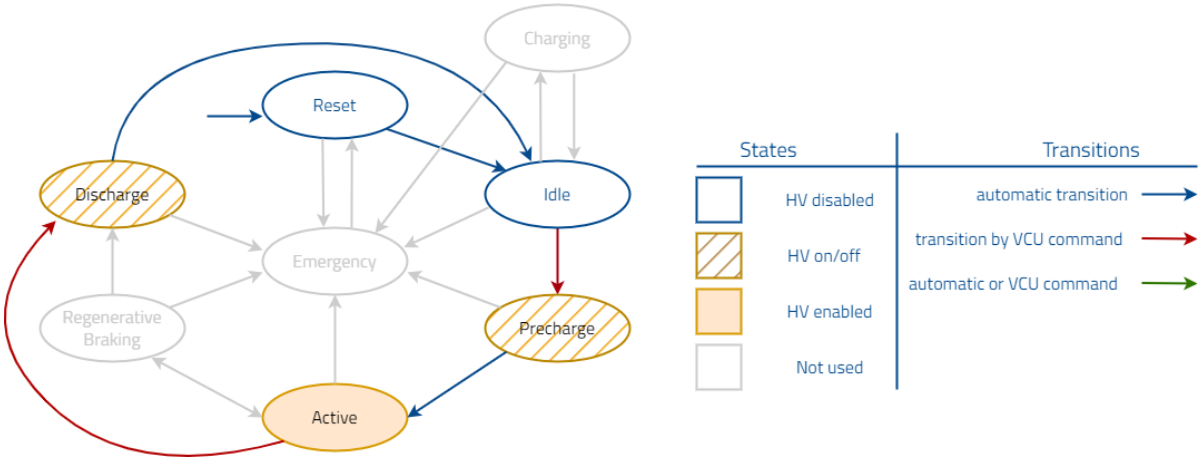

Figure 3.3: Normal State Cycle in Errorless Operation

3.2.2 FreeRTOS

The MCU code works on the basis of FreeRTOS [11][12]. FreeRTOS (Real-Time Operating System) is an open-source, real-time operating system designed for embedded systems and microcontrollers. It provides a small and efficient kernel that enables multitasking and scheduling of tasks with minimal resource requirements.
Key features of FreeRTOS include:

- Task Management: FreeRTOS allows the creation and management of multiple tasks, each with its own priority and execution context. Tasks can be created, suspended, resumed, and deleted, enabling efficient multitasking.
- Scheduling: FreeRTOS provides priority-based preemptive scheduling, allowing tasks with higher priority to preempt lower-priority tasks. This ensures that critical tasks are executed in a timely manner.
- Synchronization and Communication: FreeRTOS offers various synchronization primitives like semaphores, mutexes, and queues for inter-task communication and coordination. These mechanisms facilitate data sharing and synchronization between tasks.
- Memory Management: FreeRTOS provides a flexible memory allocation scheme tailored for embedded systems with limited resources. It offers dynamic memory allocation and deallocation capabilities through its memory management functions.
- Timers: FreeRTOS includes a timer management feature that allows the execution of tasks or callback functions at predetermined intervals. Timers are useful for implementing periodic tasks, scheduling events, or triggering actions based on time.
- Interrupt Handling: FreeRTOS provides interrupt-safe mechanisms for handling hardware interrupts. It allows the execution of interrupt service routines (ISRs) and provides efficient context switching between tasks and interrupts.

3.2.3 Multitasking

The FreeRTOS scheduler orchestrates five tasks within the MCU code of the BMS. Those are in declining priority:

1. Task Safety: This task is responsible for emergency handling and state transitions. It gets called by task default in case of an emergency or if a transition is requested. In the latter it verifies if the state transition is valid and does not pose a safety issue. A transition to emergency is always valid.
2. Task Default: This task is constantly monitoring and processing all sensors and verifies if all values are in order. Additionally it is responsible for the communication with the VCU over CAN FD [13]. It sends sensor data at a low frequency of 5 Hz to the VCU so that it can be seen live on the control panel. If it detects an error it notifies Task Safety
3. Task Display: This task is responsible for the display on the outside of the battery box.
4. Task Logging and Task Logging SD: These Task are responsible to write log data. The code for them are based on a template written by Philip Wiese.

Additionally the main current and voltage sensor are processed using timer interrupts to enable sampling at 5kHz. This is necessary to allow for quick reactions in operation as well as accurate logging of voltage and current patterns. The entire code for the MCU was written in C++ and C. The MCU is in sole control of the whole BMS except the control of the relays which is further discussed in the next section.

3.3 Gate Control and FPGA

Originally the idea was to use a MCU for the whole control, similar to previous years' BMS from Swissloop. However, after reviewing the constructed Failure Mode and Effects Analysis (FMEA), this was deemed unsafe, due to the possibility of a malfunctioning MCU. Therefore an additional FPGA was integrated into the control structure.

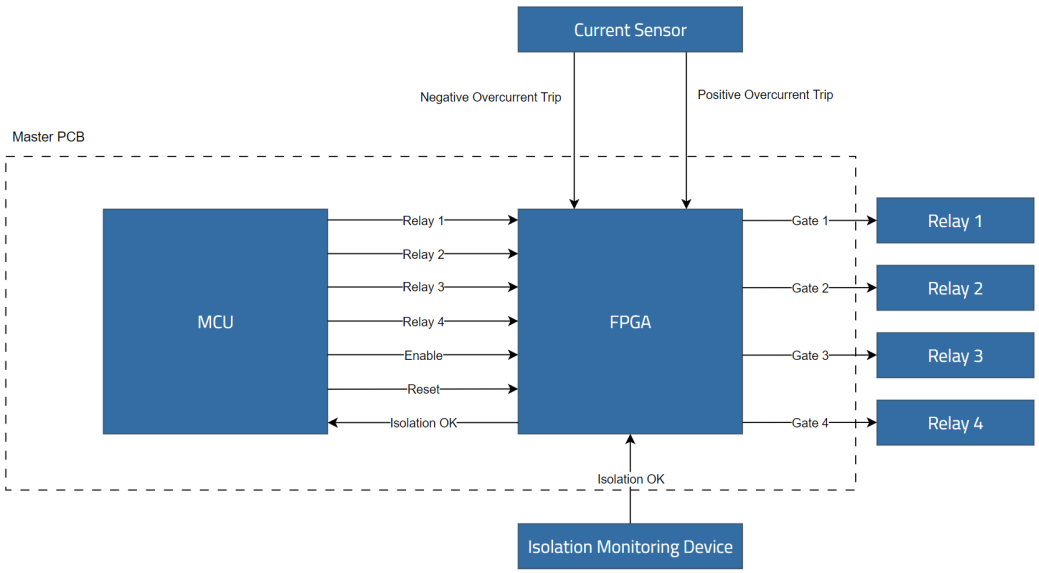

Figure 3.4: FPGA Input and Output Signals

The Master Board consists of two programmable components: the primary controller, known as the MCU, and a FPGA (Field-Programmable Gate Array) positioned between the MCU and the relays as shown in Figure 3.4. The FPGA directly receives OK signals from the IMD and both positive and negative overcurrent trip signals from the current sensor. This arrangement enables the FPGA to initiate

a hardwired relay opening in the event of a current or isolation emergency, ensuring a rapid response, such as in the case of a short circuit.
During operation, the MCU transmits the desired state for each relay to the FPGA, along with a reset and enable signal. The FPGA then evaluates whether the relay states sent by the MCU fall within the four valid combinations discussed in the following section. If the states are deemed valid, they are forwarded to the relays. Conversely, if the states are determined to be invalid, the FPGA opens all relays as a safety measure.
The "all relays open" state is also utilized as the dead time state when transitioning between relay states. This dead time insertion serves to introduce a brief pause or interval between turning off one relay and turning on the next relay. The purpose of this dead time is to prevent any potential overlap or short-circuiting between relay switches, thereby safeguarding the system from damage and undesirable electrical behavior.
The only information propagated from FPGA to MCU is the status of the isolation, since the MCU itself has no direct communication to the IMD.

3.4 High Voltage Topology

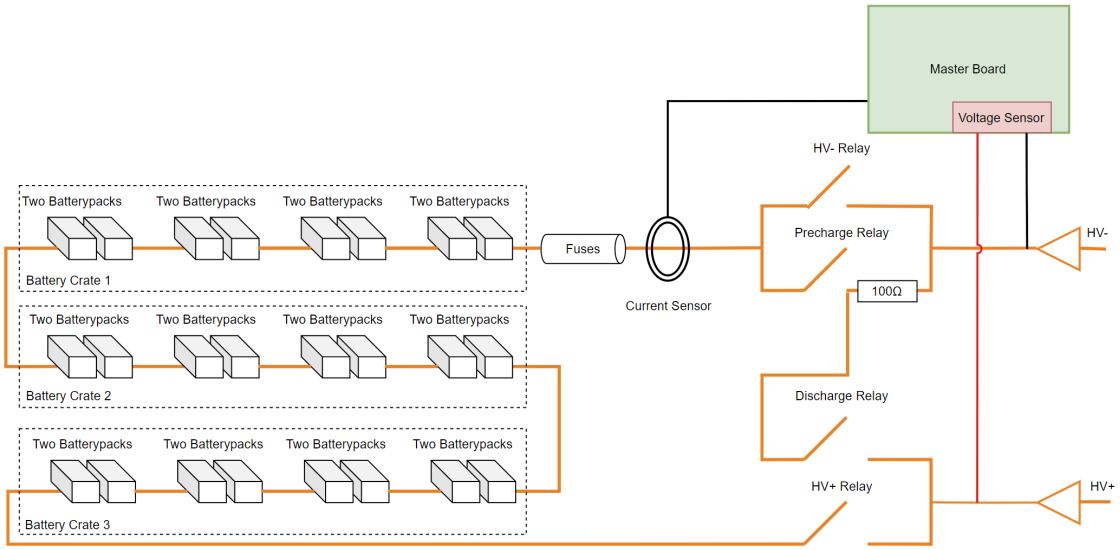

Figure 3.5: High Voltage Topology of the System

The power circuit of the Batteries as seen in Figure 3.5 is controlled using the four relays mentioned in the section above and can be operated in four modes:

1. **Open:** If all relays are open, there is an open circuit between HV- and HV+. The batteries are disconnected from the output. This is also the dead time state used by the FPGA during transitions. The system is not discharging the capacitors of the inverters. The current flow in this state is highlighted orange in Figure 3.6.

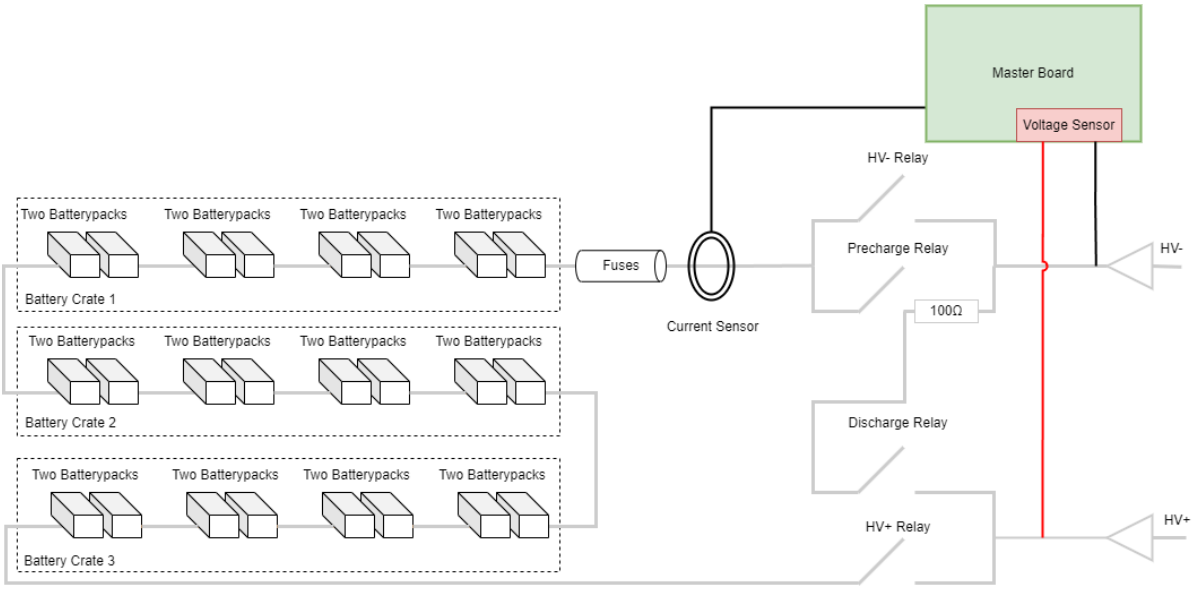

Figure 3.6: Current Flow in the Open Mode

2. **Discharge:** If only the Discharge relay is closed, the batteries are also disconnected from the outside. However there is a resistance of 100 Ohm between HV- and HV+. The system is discharging the capacitors of the inverters. The current flow in this state is highlighted orange in Figure 3.7.

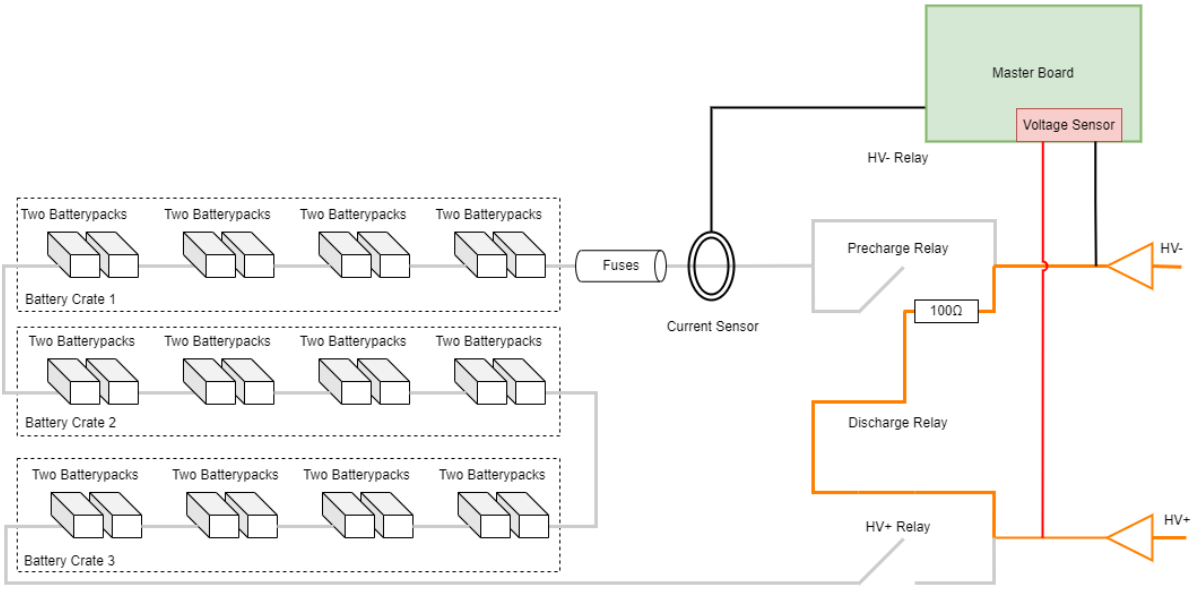

Figure 3.7: Current Flow in the Discharge Mode

3. **Active:** If only relays HV- and HV+ are closed, the batteries are directly connected to HV- and HV+. This is the mode which is used during runs. The current flow in this state is highlighted orange in Figure 3.8.

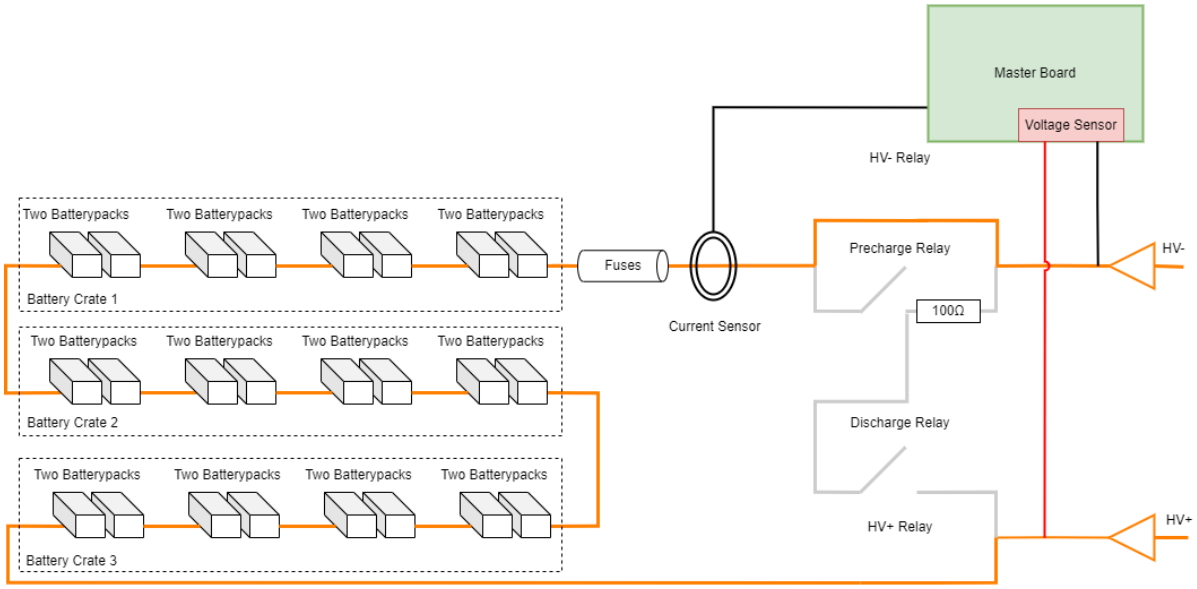

Figure 3.8: Current Flow in the Active Mode

4. **Precharge:** If only relays Precharge and HV+ are closed, the batteries are connected directly to HV+ and with a resistance of 100 ohm in series to HV-. This mode is used to precharge the capacitors of the inverters. The current flow in this state is highlighted orange in Figure 3.9.

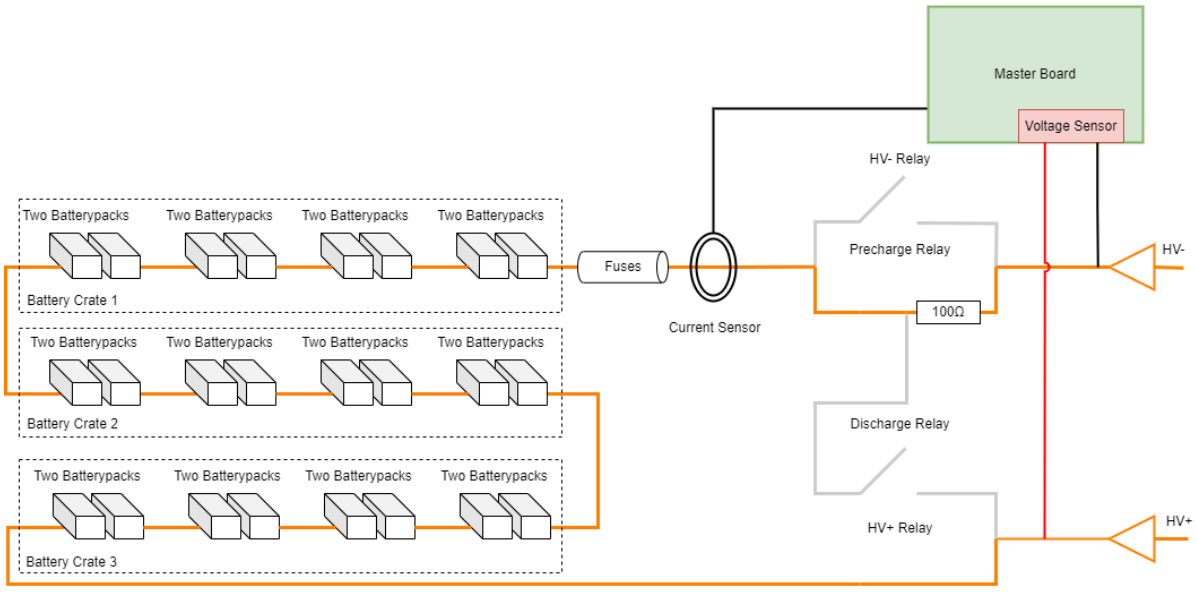

Figure 3.9: Current Flow in the Precharge Mode

All other states are illegal and not allowed by the FPGA. The topology works exactly the same with less batteries. For example, if a lower voltage is desired. The easiest way is to remove a battery crate from the circuit, and replace it with a short.

Chapter 4

Design Implementations and Results

This chapter delves into the details of the batteries, their integration into the system, the implementation of the Master Board of the BMS, and the measurements taken during the operation of the power supply system.

4.1 Electrical and Mechanical Integration

The battery box and battery integration has been designed and implemented in collaboration with Julia Näf, who was responsible for the electrical integration of the 2023 prototype. The content presented in this section primarily represents her contributions and efforts.

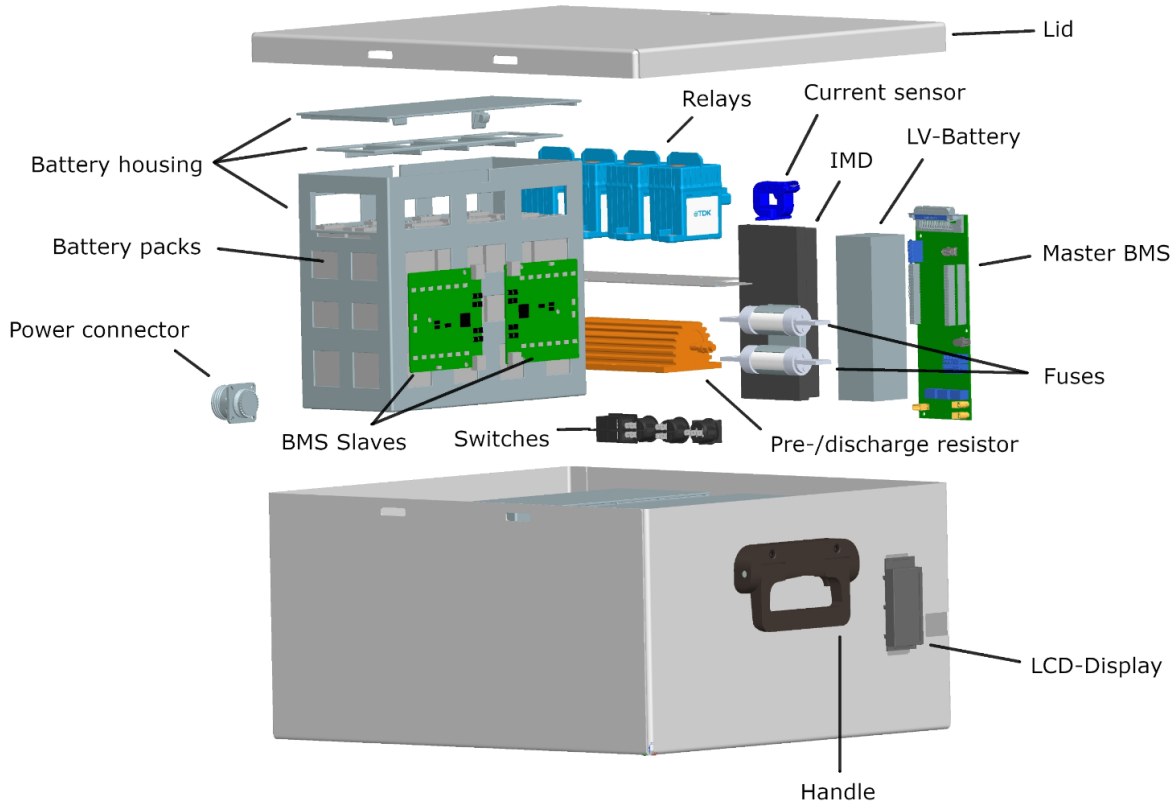

Figure 4.1: Explosion view of the battery box

Figure 4.1 shows a Computer Aided Design (CAD) of the battery box with all its components and one of

three battery crates.
The batteries and electrical components are enclosed in an aluminum box, taking inspiration from the concept of a Faraday cage. This design serves two purposes: shielding the emitted Electromagnetic Interference (EMI) from the batteries and protecting the Master BMSs from external noise. The box is constructed from 1.5mm thick bent aluminum sheet, chosen for its lightweight nature and excellent conductivity. In comparison to boxes made of 1mm thick sheets, the battery box offers enhanced durability and strength.
To ensure safety, the surfaces of the box are powder coated, diminishing the risk of electrical shocks, even in the event of isolation failure. A major challenge was to create a battery box that is easily removable while also being securely held in place during runs. This obstacle was overcome by utilizing security raids and 3D printed case corners, providing a solution to the problem.
Similar to the previous year, the Slave BMS units are interconnected using Harting cables, which feature integrated shielding mesh. In order to minimize EMI within the battery box, the internal arrangement was carefully planned to keep current loops as small as possible. This involved utilizing XT150 connectors for the daisy-chain connection between the battery packs. Additionally, an extra precautionary step was taken by maintaining a minimum distance of 3cm between HV-cables and the Master BMS. These measures collectively contribute to the reduction of EMI and ensure optimal performance within the system.

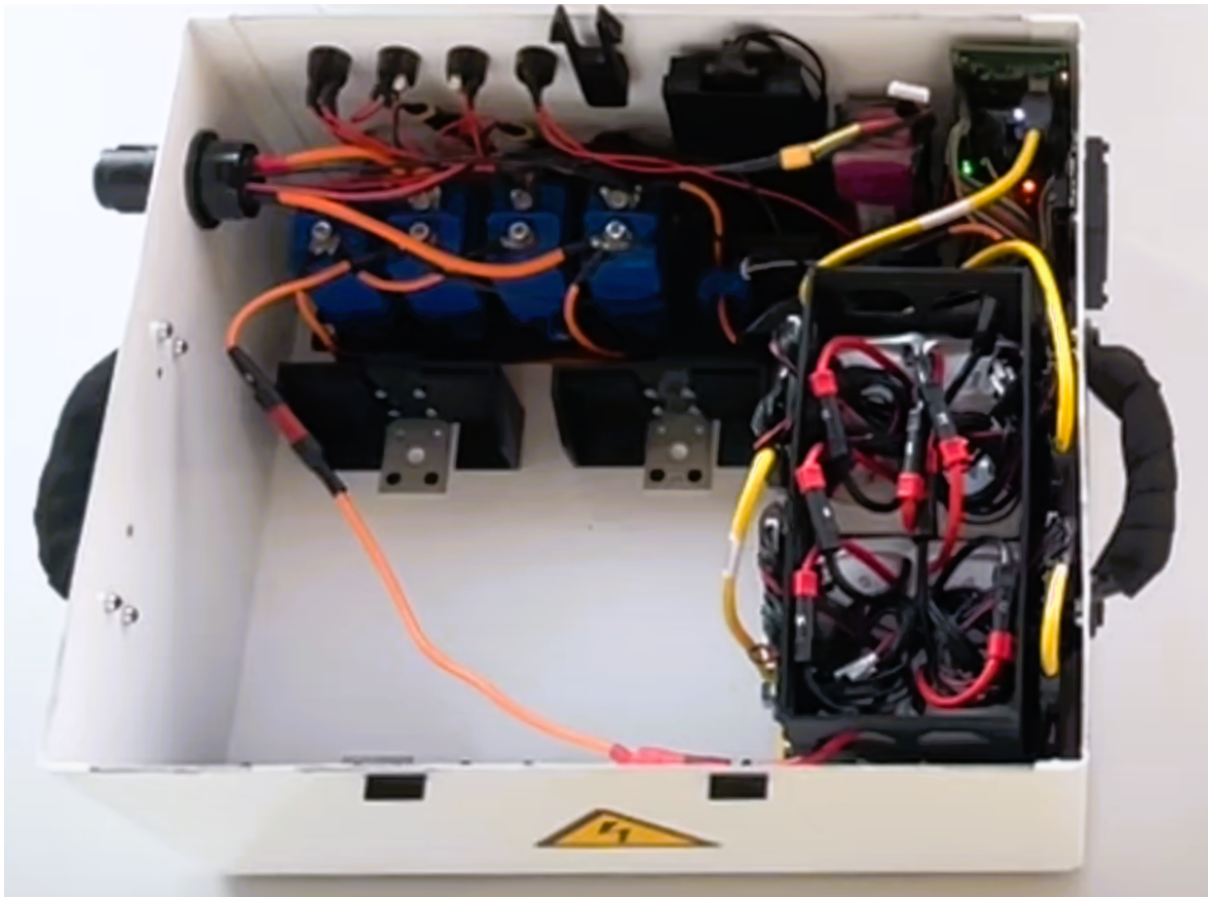

Figure 4.2: Assembled Battery Box

4.1.1 Batteries

After reviewing the previous years batteries the conclusion was reached that significant space, weight and performance improvements could be achieved with new more powerful batteries.

Figure 4.3: LiPo Battery Pack

Swaytronic manufactured a total of 40 custom battery packs for the battery system, each configured as 8s1p (8 cells in series, 1 cell in parallel). These battery packs were specifically requested to include thermistors and balancing cables on each individual cell. To form a battery crate, eight battery packs are connected in series. Depending on the desired voltage, one, two, or three battery crates can be connected in series. The maximum performance can be achieved by utilizing all three crates and subsequently having 24 Battery packs in series. Here are the main specifications of the battery:

Table 4.1: Main Battery Specifications

Nominal voltage	Max. voltage	Max. current	Max. power	Total weight	Total capacity
710 V	823 V	247 A	203 kW	15.6 kg	2060 Wh

As a result of EMI issues in the inverters, the power supply system was never subjected to full testing using more than two battery crates. However, successful testing was carried out for precharges up to 820V and discharges from 820V, with no reported problems or issues encountered during these tests. In table 4.2 additional data about the batteries are provided.

4.1.2 Detailed Battery Specifications

Table 4.2: Detailed Battery Specifications

Battery Type	Swaytronic Ultra LiPo
Packs	24
Packs In Series	24
Packs In Parallel	1
Weight/Pack [kg]	0.65
Total Weight[kg]	15.6
Total Nominal Voltage[V]	710.4
Total Max Discharge Current[A]	246.5
Total Peak Discharge Current[A]	493.0
Total Capacity [Wh]	2060.2
Max total Power [W]	175113.6
Cells per Pack	8
Cells in Series	8
Cells in Parallel	1
Nominal Voltage P [V]	29.6
Max Discharge C Rating	85
Max Discharge Current [A]	246.5
Peak Discharge C Rating	170
Peak Discharge [A]	493.0
Std Charge Current C Rating	3
Std Charge Current	8.7
Max Charge Current C Rating	8
Max Charge Current [A]	23.2
Electric Charge [Ah]	2.9
Capacity/Pack [kW]	85.8
Volume/Pack [ml]	373.6
Volume Total [ml]	8967.2

4.2 Master Board

The initial design of the Master Board's schematics and layout was finalized shortly before the commencement of this thesis. Subsequently, the PCB was soldered, and extensive testing was conducted to verify the functionality of all features. No second version of the PCB had to be designed, as the initial version exhibited only minor flaws that could be addressed and rectified in the first iteration. The PCB was designed using Altium Designer and manufactured by Eurocircuits.

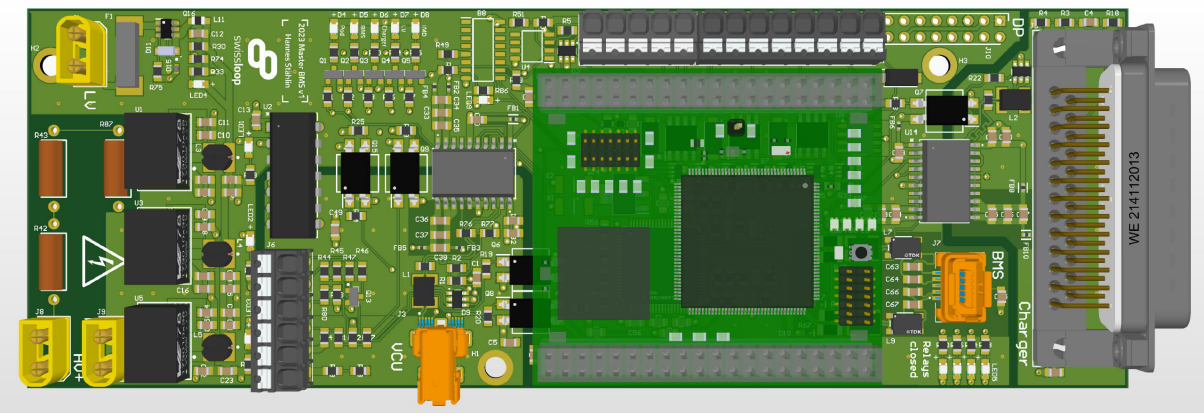

Figure 4.4: The Master Board

The dimensions of the PCB are specified as 165 mm in length, 60 mm in width, and approximately 30 mm in height. The subsequent sections will provide a detailed breakdown of all the functionalities encompassed within the Master PCB.

Figure 4.5: The Master Board being soldered

4.2.1 General Purpose PCB

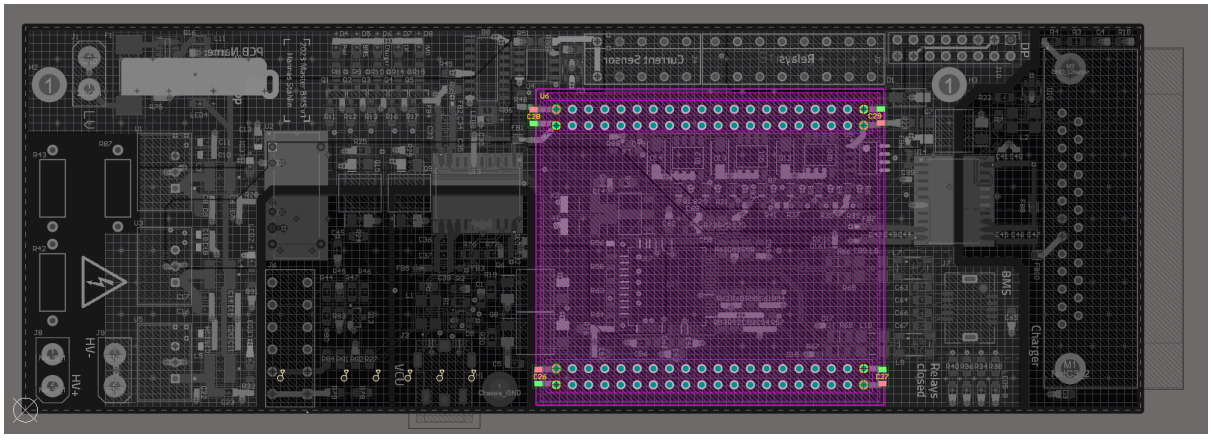

Figure 4.6: GPPCB

Mounted on the Master Board is a GPPCB designed in 2021 by Fabian Sidler. The GPPCB features the STM32H723 MCU [14], the LMXO3LF-4300C FPGA [15] and a slot for a SD Card for data logging.
The embedded software on the master board is executed on the STM32H723 microcontroller, which serves as the primary controller for almost all functionalities of the board. The STM32H723 microcontroller handles various tasks and operations, including but not limited to data monitoring, communication and the state machine of the system.

The FPGA's role in the system is focused on relay gate control, specifically managing the activation and deactivation of the relays based on input signals from the microcontroller.
One critical aspect of the FPGA's functionality is the accurate insertion of dead time between relay activations and deactivations. As mentioned in section 3.4, dead time refers to a brief pause or interval introduced between turning off one relay and turning on the next relay. The purpose of this dead time is to prevent any potential overlap or short-circuiting between relay switches, thereby avoiding system damage and undesirable electrical behavior.
By dividing the responsibilities between MCU and FPGA, the system can leverage the strengths of each component, enabling efficient and reliable control of the master board's functionalities.

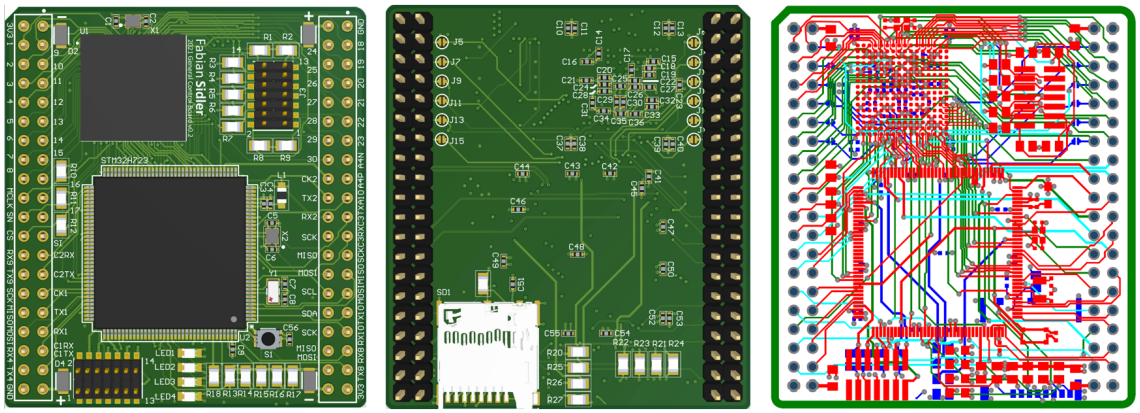

Figure 4.7: Top View, Bottom View and Traces of the GPPCB

4.2.2 Battery Management Chip and Communication to Slave PCB

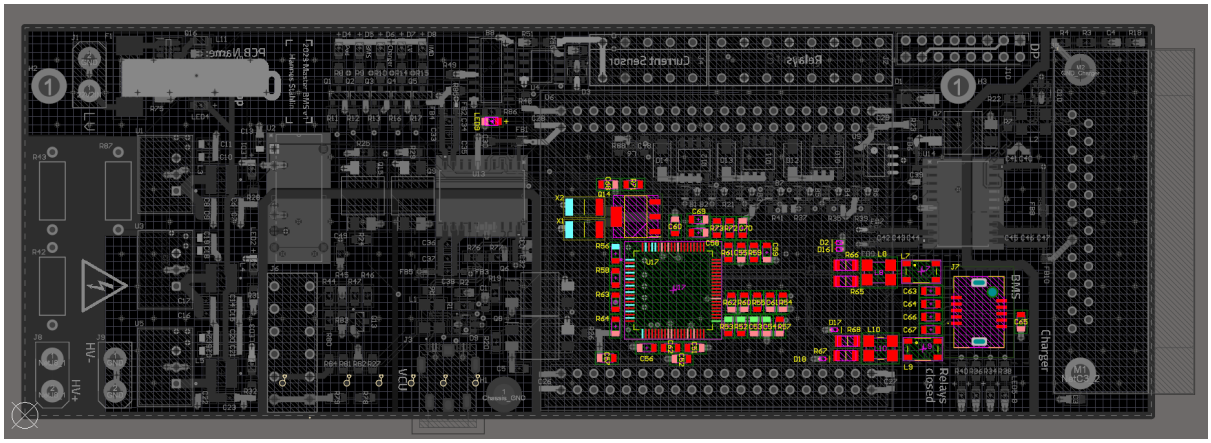

Figure 4.8: Battery Management Chip

The task of cell monitoring and balancing is accomplished through a chain of BQ76PL455APFCT [16] battery management chips from Texas Instruments. The first chip in the chain is positioned on the master board, initiating communication with identical chips on each slave board. This interconnected configuration enables effective monitoring and balancing of the cells within the system. The battery management chip on the master board communicates with the MCU via Universal Asynchronous Receiver Transmitter (UART).

4.2.3 Voltage and Current Sensor

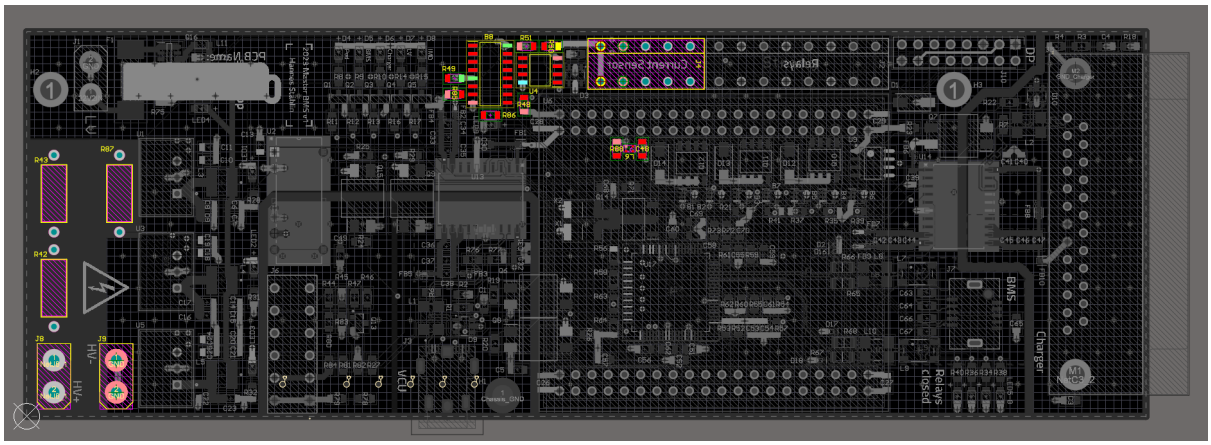

Figure 4.9: Voltage and Current Sensor [17]

On the left side of Figure 4.9, a voltage divider is implemented to measure the voltage using the internal Analog to Digital Converter (ADC) of the MCU. This voltage measurement feature is essential for detecting over- or under-voltage conditions within the system.
In the top middle of the figure, there is a connection to an external current sensor , which enables the measurement of current flowing through the system. Additionally, an overcurrent trip circuit is integrated, utilizing an op-amp as a comparator and a latch to detect negative overcurrent situations. This circuit is designed to quickly identify and respond to instances of excessive current flowing back into the batteries, for example during regenerative braking.
Furthermore, the current sensor incorporates an integrated circuit that specifically detects very high positive overcurrents. This ensures that the system can promptly identify and address potentially dangerous levels of positive current.
Overall, these voltage and current sensing elements play a crucial role in monitoring and safeguarding the system, allowing for early detection of abnormal voltage levels and overcurrent situations. They are both sampled and processed at a frequency of 5 kHz. Measurements of both these sensors are provided in Section 4.4.

4.2.4 Relays

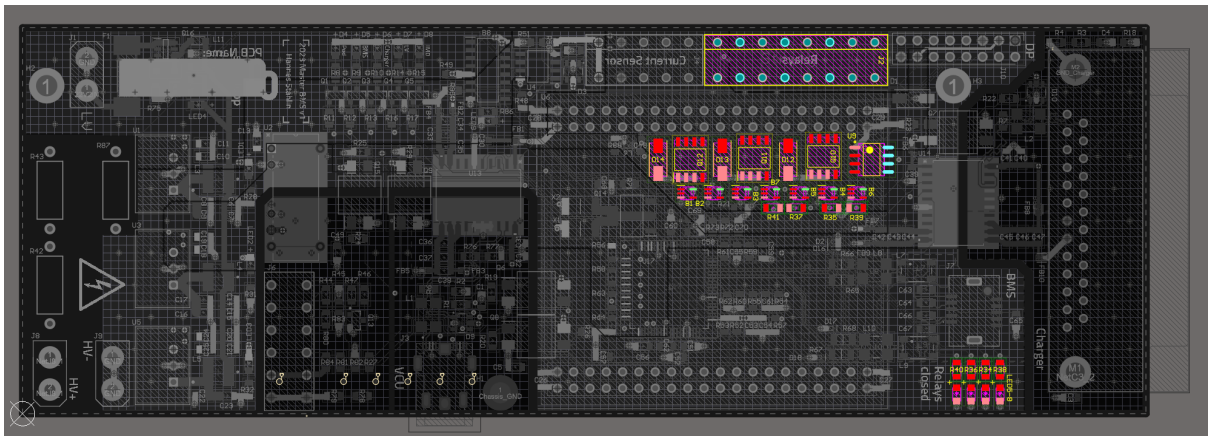

Figure 4.10: Relays [18]

To convert the 3V3 gate signals from the FPGA into 12V gate signals, high and low side switches are employed. These switches serve the purpose of amplifying the voltage level to match the requirements of the gate signals.

Furthermore, LEDs are integrated into the system to provide direct visual feedback on the status of the gate signals. This allows for quick and easy identification of which gate signals are currently active or high. The inclusion of LEDs aids in troubleshooting or monitoring the system.

4.2.5 Isolated communication with VCU and IMD

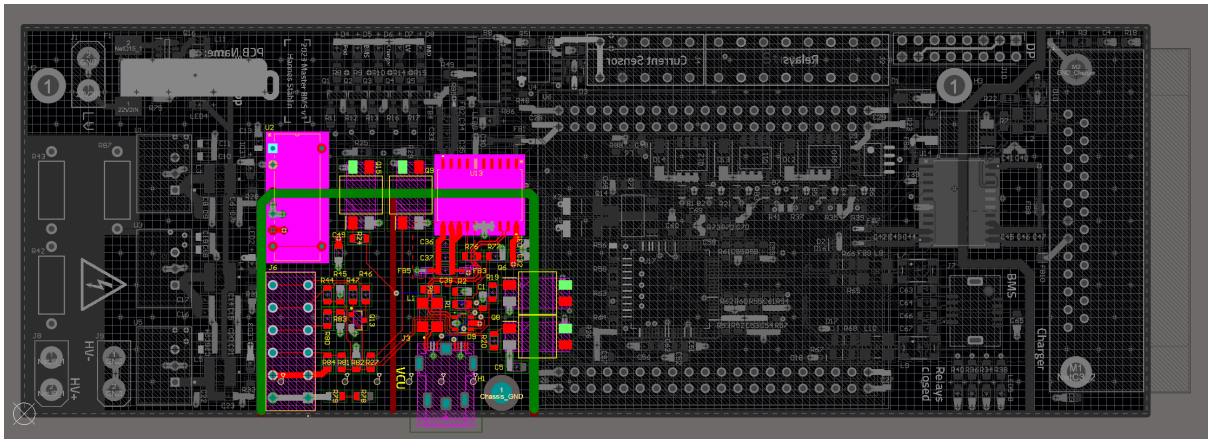

Figure 4.11: VCU and IMD Connection

Due to the direct connection between the BMSs and the negative battery output, the main ground of the Master BMSs aligns with the HV- potential. However, it is undesirable for the entire control system or the IMD to be on HV potential, since this would increase the danger of an isolation fault. To address this issue and ensure the IMD and VCU connection is on the same potential as the VCU, galvanic isolation is implemented. This isolation is crucial for preventing potential damage to be transfered between VCU and BMS, effectively safeguarding both components. In Figure 4.11 the pink component on the left is an isolated 12V DC-DC for the IMD. The pink component on the right is a combined isolated 5V DC-DC and CAN FD transceiver. Furthermore four optocouplers are used to transfer Signals from VCU and IMD.

4.2.6 Communication with Charger

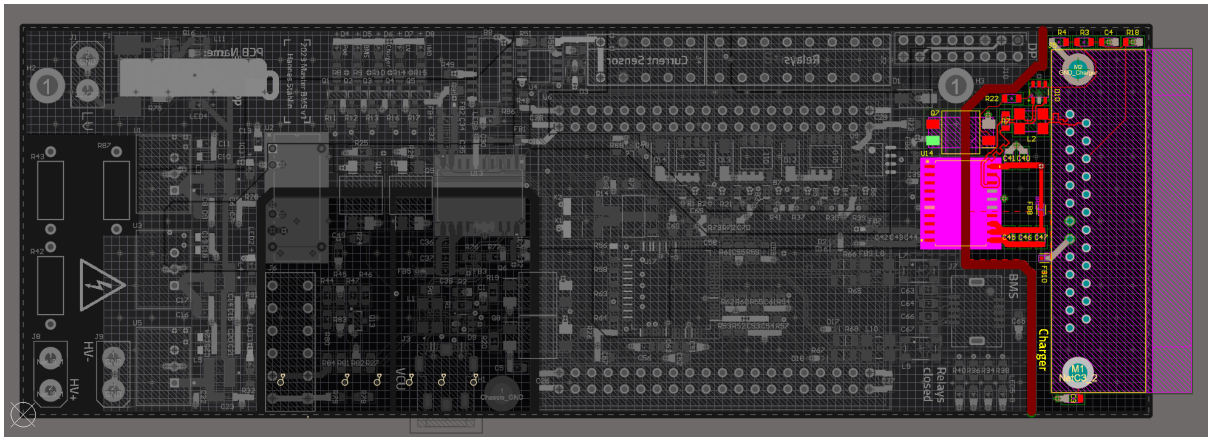

Figure 4.12: Charger Communication

Highlighted on the far right of the PCB is a plug that serves as a potential CAN FDs connection point for a charger. This connection enables communication between the BMSs and the charger. The hardware for this connection is fully functional and ready for use.

However, it is important to note that the charging of the entire battery box was not considered a significant improvement, as the individual battery packs can be charged relatively quickly. As a result, the software implementation of the communication between the BMSs and the charger has not been addressed at this stage. This aspect could be explored in future work, allowing for the integration of charging control into the system.

4.2.7 LED and LCD Display Connection

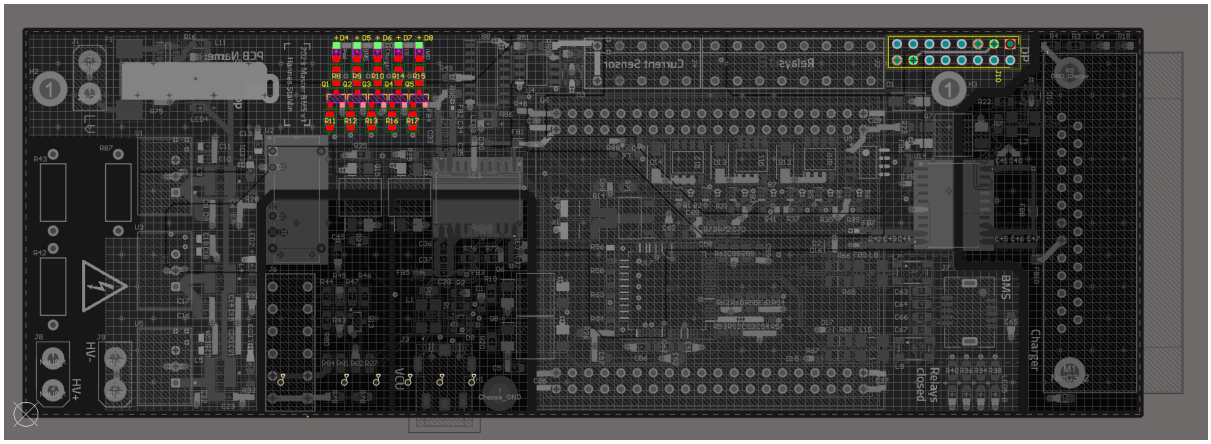

Figure 4.13: LED and LCD Display Connection

To provide real-time feedback on the system and battery condition without the need for an additional system, LEDs on the PCB and an LCD display on the exterior of the box have been incorporated . These visual indicators have proven to be highly useful during testing and debugging processes.
The LCD display is controlled via a parallel bus, as it primarily serves as an informative system. Due to space constraints on the PCB and the focus on functionality over EMI shielding, no efforts were made to shield the display's signals against electromagnetic interference (EMI). Consequently, the display often experiences malfunctions when relays are switching, requiring it to restart itself.
In future work, improvements could be made to address this issue and enhance the reliability of the LCD display. Implementing measures to mitigate EMI interference, such as shielding or signal filtering, could help ensure stable operation even during relay switching events.

4.2.8 Power and Protection

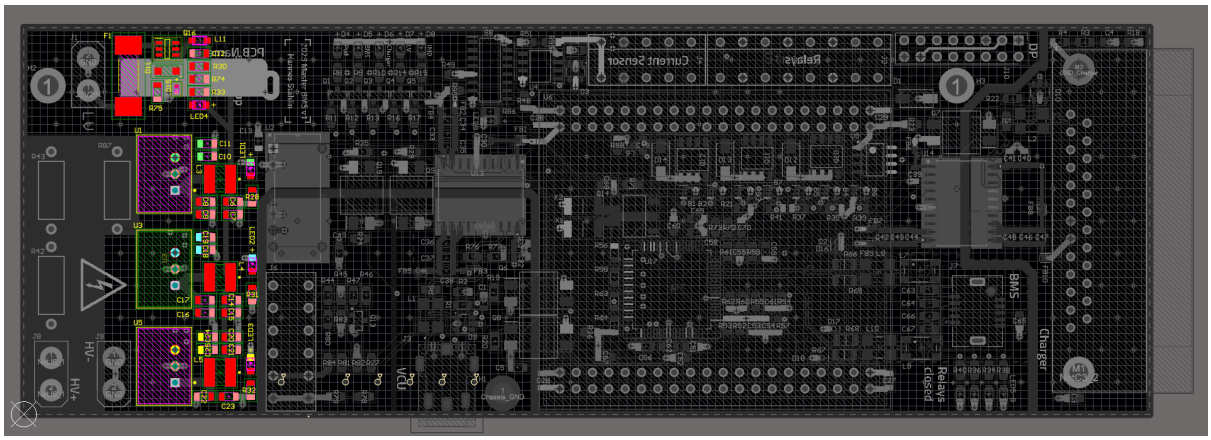

Figure 4.14: Power and Protection

The Master Board is equipped with its own LV (Low Voltage) battery to ensure optimal autonomy. A protection circuit is incorporated at the power input to safeguard against reverse polarity, overvoltage, and overcurrent situations. Three DC-DC converters, represented by different colors (yellow for 5V, green for 3V3, and blue for 12V) in Figure 4.14, are responsible for supplying power to the respective nets on the PCB.

4.3 Pre- and Discharge

To enable high current spikes and effectively store energy from electromagnetic coils while also protecting the batteries, each of the seven inverter boards is equipped with four capacitors. In addition, three central large inverters have been introduced to enhance the overall capacity. When connected in parallel to the batteries, these capacitors provide a combined total capacity of:

$$C_t = 4 \cdot 7 \cdot 30\mu\text{F} + 3 \cdot 420\mu\text{F} = 2.1\text{mF} \tag{4.1}$$

The capacitors serve as energy storage devices and play a crucial role in handling transient power demands and fluctuations in the system. They can rapidly discharge stored energy when high current spikes are required. By acting as a buffer, the capacitors help to stabilize the voltage and supply additional power when needed, reducing voltage drops.
Furthermore, the capacitors contribute to the protection of the batteries. They can absorb and dissipate excess energy generated by the electromagnetic coils, preventing it from reaching and potentially damaging the batteries.
However those capacitors have to be precharged before normal operation. To achieve this, a dedicated circuit has been implemented, which incorporates a 100 Ωresistor to limit the current during precharging. This current-limiting resistor helps regulate the flow of current into the capacitors, preventing the sudden influx that would otherwise blow the fuses.
Figure 4.15 illustrates the measurements of current and voltage during a complete precharge, starting from 0 volts and increasing to 500 volts. The measurements are sampled at a rate of 5 kHz, allowing for detailed monitoring and analysis of the precharge process.The rolling average and Root Mean Square (RMS) shown in the figure below are sampled over a 5 ms interval.

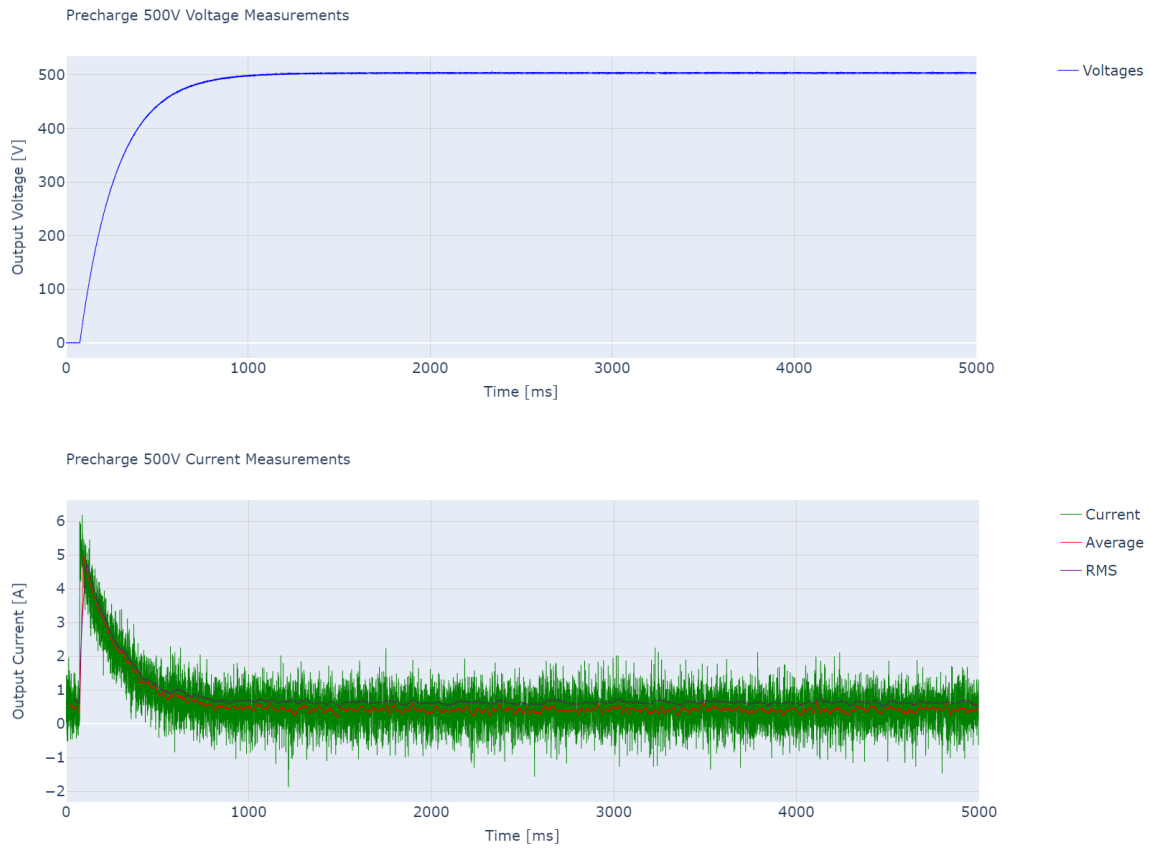

Figure 4.15: Voltage and Current Measurements during Precharge

The precharge process is designed to end once two conditions are met: reaching the desired voltage level and a predefined time duration of 5 seconds. This additional safety measure ensures that the capacitors are adequately precharged before proceeding to normal operation.
Figure 4.15 demonstrates the behavior of the voltage during the precharge process. It shows that the desired voltage level is typically reached in less than a second. The initial 60ms period, during which the voltage remains low, is due to the dead time insertion operation that takes place.
By setting a fixed time duration of 5 seconds for the precharge process, the system allows sufficient time for the capacitors to reach the desired voltage level, even in case of wrong voltage measurements or configurations.
To ensure safe operation and proper handling of the capacitors, a discharge circuit has been implemented in the system. This circuit allows the capacitors to be discharged from the operating voltage back to 0V after a run or in case of emergency. The discharge circuit is also in place when the BMS is in idle to prevent the capacitors from charging themselves in any way.
Figure 4.16 illustrates the measurements of voltage during a complete discharge, starting from 267 volts and decreasing to 0V. The measurements are sampled at a rate of 5 kHz.

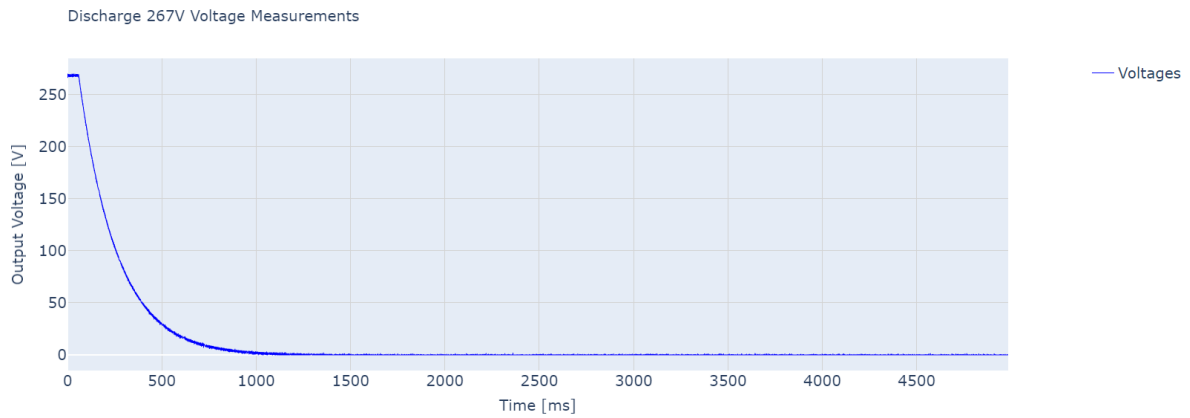

Figure 4.16: Voltage Measurements during Discharge

Similar to the precharge process, the discharge circuit utilizes the same resistor to limit the current during the discharge operation. As a result, the voltage curve exhibits the same pattern to that of the precharge process. There is no current flowing through the current sensor during the discharge process therefore it cannot be monitored. However it can be assumed to be similar to the precharge current.

4.4 Current and Voltage Patterns

There are three operation modes that Swissloop will present at the EHW this year. The current and voltage on the output of the batteries during these three modes will be discussed in the following sections:

4.4.1 Propulsion Run

The propulsion run is where the maximum potential of the propulsion is showcased. The prototype is not airborne during this run, the vertical levitation is only preventing the prototype from getting stuck at the top of the track and the lateral levitation is switched off completely. The inverters allow 120A through the propulsion coils. Two battery crates are used during this type of run, which results in an operating voltage between 538 Volt (full) and 422 Volt (almost empty).

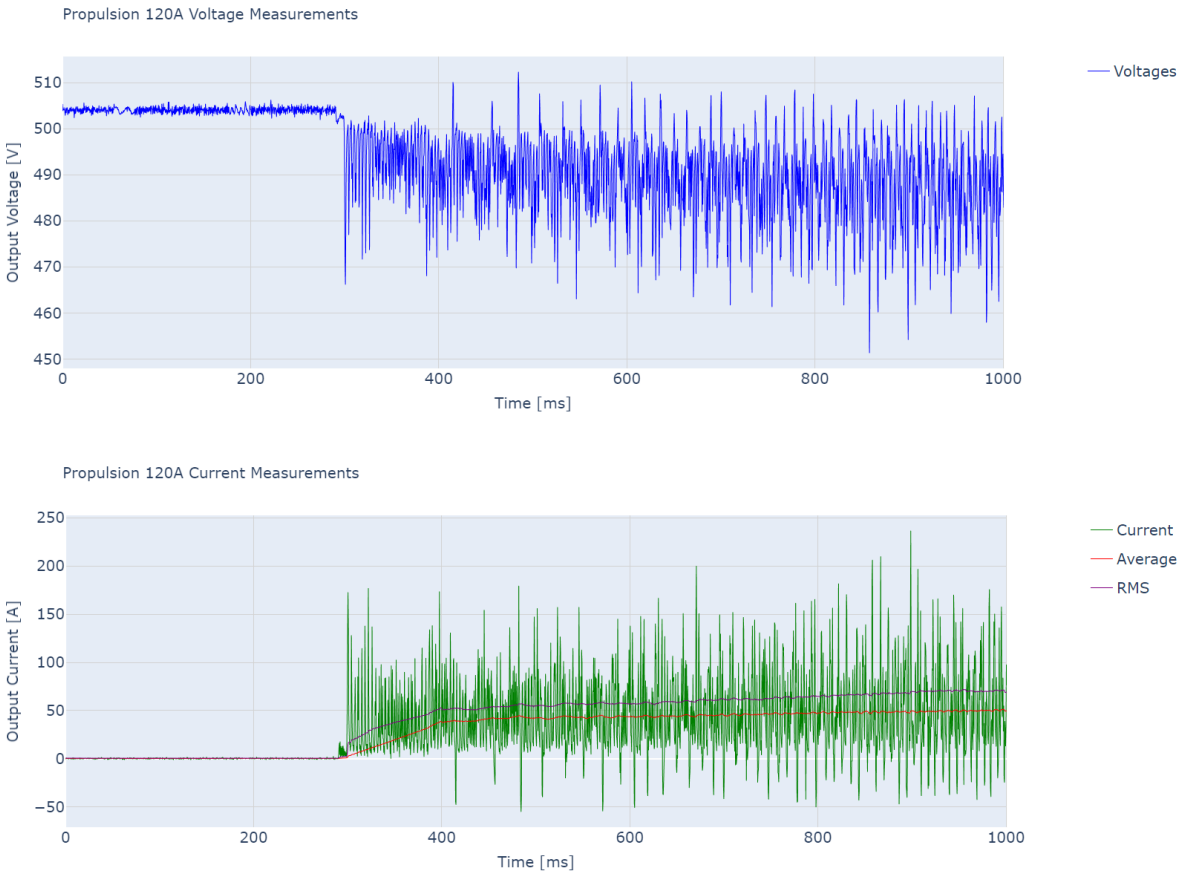

Figure 4.17: Voltage and Current Measurements during a Propulsion Run

In Figure 4.17, voltage and current measurements from the initial second of a propulsion run are displayed, with a sampling rate of 5 kHz. The rolling average and Root Mean Square (RMS) shown in the figure are sampled over a 50 ms interval. While the average current never exceeds 50 A, there are current spikes reaching as high as 240 A and as low as -50 A. These spikes are a result of the switching behavior of the inverters. As one can see, the current spikes align almost perfectly with the inverse spikes in voltage. This correlation is attributed to the fact that when current is drawn, it induces a voltage drop across the batteries due to their internal resistance.
While the batteries can easily handle these spikes this may still warrant additional filtering to mitigate their impact. It is worth noting that the strength of these spikes is partially attributed to the lower operating voltage than initially expected.
With low voltage more current has to be drawn to reach similar power for propulsion and levitation. However, due to excessive electromagnetic interference (EMI) observed in the inverters at higher voltages, reducing the voltage was a necessity to perform reliable runs.

4.4.2 Standstill Levitation

The second operation mode is the standstill levitation. In this operation mode the propulsion is switched of and only levitation is enabled. The rolling average and Root Mean Square (RMS) shown in the figure are sampled over a 50 ms interval.

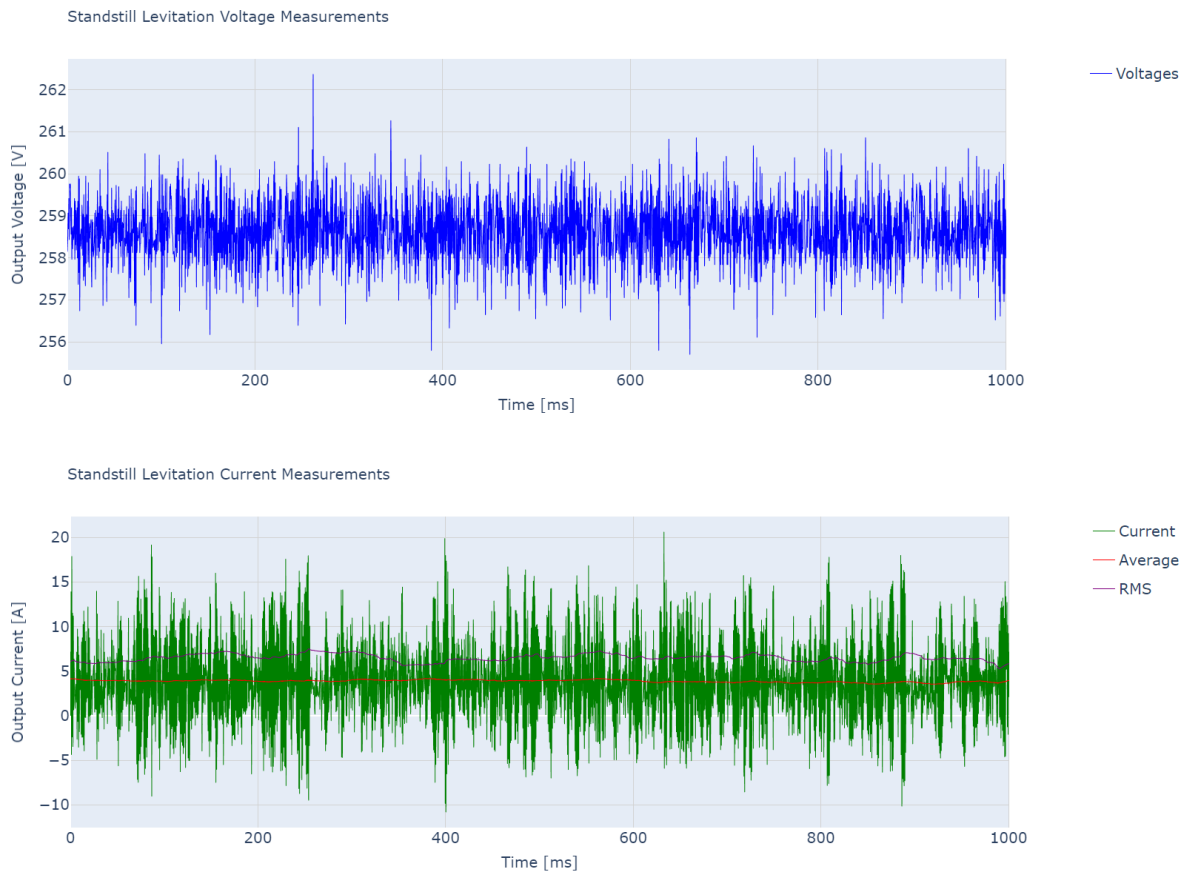

Figure 4.18: Voltage and Current Measurements during Standstill Levitation

Figure 4.18 illustrates one second of standstill levitation, sampled at a rate of 5kHz. The average current drawn from the batteries during this period is approximately 4 A. Consequently, the power consumed by the entire system for levitation is estimated to be around $4A \cdot 259V = 1036W$. With the energy capacity of one battery box, which accounts for a third of the maximum energy of the battery system, the prototype can remain airborne for approximately 40 minutes. With the full 2060Wh capacity, the prototype could stay airborne for up to 2 hours.
An interesting observation is the symmetry of the current spikes, where the energy drawn during levitation is quickly returned back to the batteries. This suggests that the levitation controllers may be overly aggressive and tend to overreact, resulting in rapid fluctuations in energy consumption.

4.4.3 Levitation Run

During the levitation run, the prototype demonstrates its combined levitation and propulsion capabilities. The levitation system is activated, allowing the prototype to hover in all directions. After 5 seconds of levitation, the propulsion system is also enabled to accelerate for five seconds. The inverters allow a current of 120A to flow through the propulsion coils during this time After this period, the propulsion is stopped, allowing the prototype to glide effortlessly for the remainder of the track. One battery crate was used during levitation runs, which results in an operating voltage betweeen 269 Volt (full) and 211 Volt (almost empty).

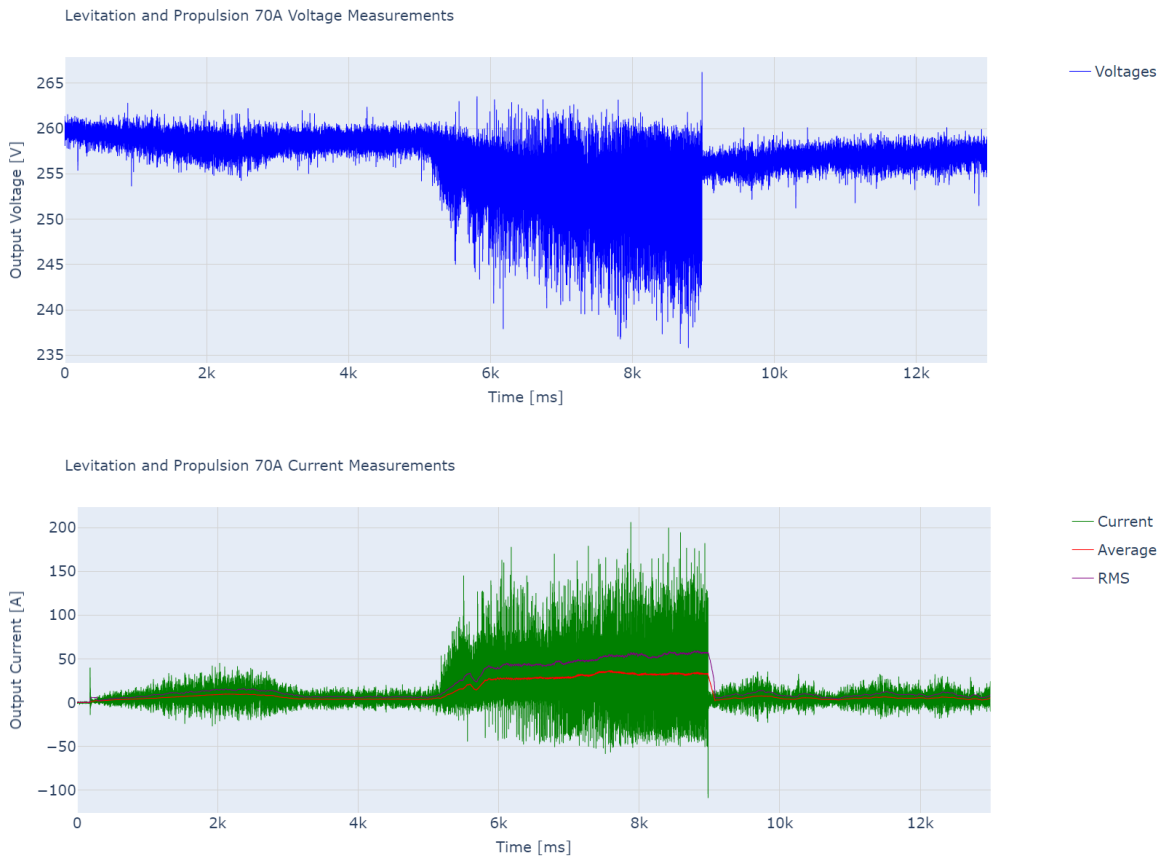

Figure 4.19: Voltage and Current Measurements during a Levitation Run

Figure 4.19 illustrates a 13-second duration of a levitation run. During the initial three seconds, the levitation force raises the prototype to its equilibrium position. Subsequently, there are two seconds of stationary levitation where the prototype necessitates minimal energy. This is succeeded by a distinct propulsion phase, clearly noticeable in the graph, which lasts approximately four seconds. Finally, there is a four-second gliding period. The rolling average and Root Mean Square (RMS) shown in the figure are sampled over a 50 ms interval.
While the levitation alone never induces current spikes higher than 50 A. The levitation in combination with propulsion induces current peaks up to 200 V even with the propulsion inverters reducing the current in the motor to 70 A. One reason for this is once again the very low voltage of only 260 V. To reduce these spikes the voltage would need to be increased. However the levitation experienced issues with higher voltages that could not be addressed in time. Noticeable is a single strong negative current spike as soon as the propulsion is switched off. This is the energy stored in the propulsion coils flowing back into the batteries.

4.5 Battery Cell Monitoring and Balancing

In order to continuously monitor the health of the battery, the voltage of each of the 192 cells and the temperature of every other cell are measured by 12 Slave BMS. These measurements are sampled at a frequency of 10 Hz, allowing for real-time monitoring of the battery's condition. An automatic emergency is called if abnormal values are detected.

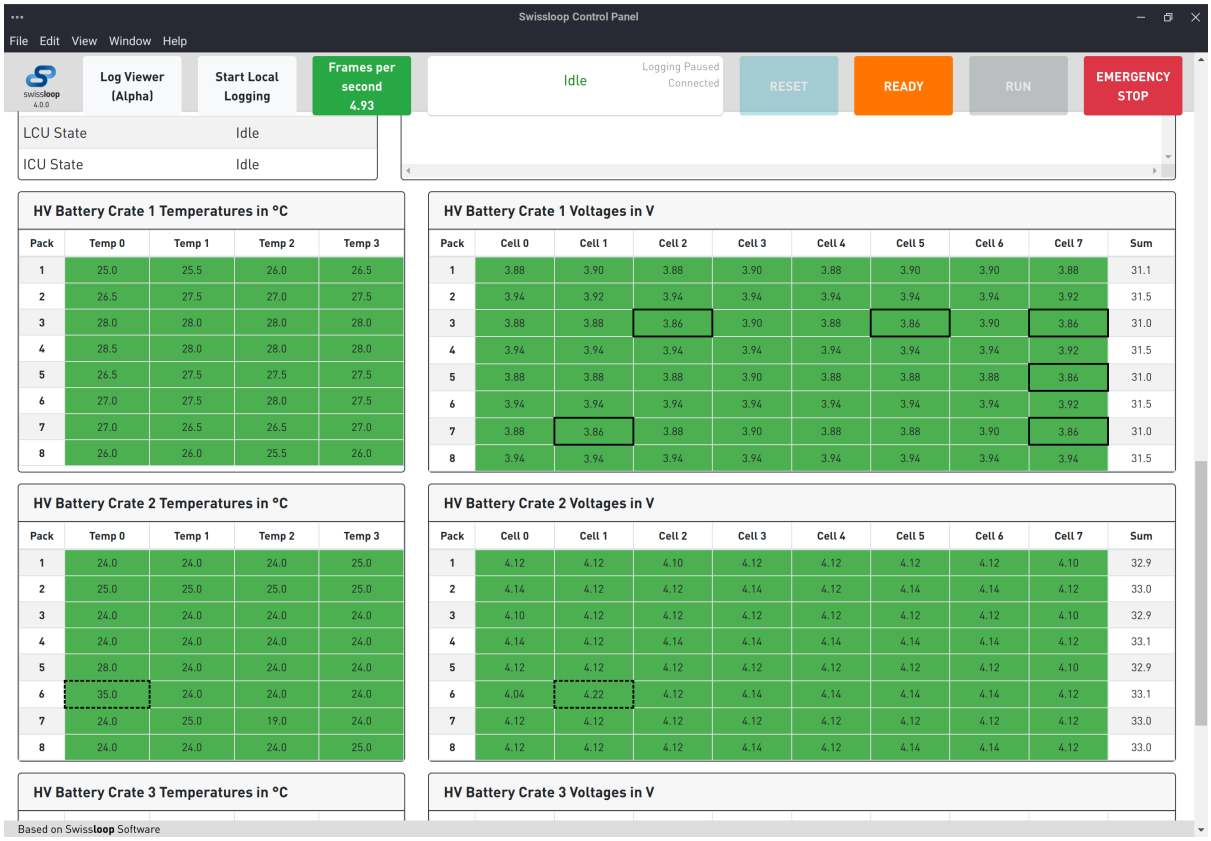

Figure 4.20: Control Panel Overview of Two Battery Crates

The control panel overview of the battery cells in the first and second crates is visible in Figure 4.20. The highlighted information includes the lowest cell voltage values, as well as the highest cell voltage and cell temperature. By analyzing the data, it is evident that the first crate has been discharged more than the second crate. This can be attributed to the fact that the initial tests conducted on that day were exclusively performed with the first crate.
To achieve a balanced state between the two crates, the user has the option to enable balancing with a single button on the control panel. Once activated, the second crate will passively balance itself to match the level of the first crate. Balancing occurs whenever the BMS is in the idle state and is halted as soon as another operation begins. After the operation the BMS will automatically resume balancing until either all cells are balanced, balancing is toggled off or an emergency is triggered.

4.6 Isolation Monitoring Device (IMD)

Figure 4.21: Isolation Monitoring Device (IMD) used in the Prototype [19]

The Isolation Monitoring Device (IMD), is a crucial component in the prototype ensuring electrical safety. Its primary purpose is to monitor the insulation resistance between the high-voltage system and the chassis. The IMD continuously measures the resistance between the the high-voltage potentials and the chassis, detecting any insulation faults or breakdowns that may occur. It helps identify potential electrical faults, such as insulation degradation, moisture ingress, or insulation failure, which could lead to hazardous conditions like electric shock or short circuits. The decision was made to use the IR155-3204 from bender, since they where successfully used in previous years and are developed for electric vehicles. It reports if the isolation resistance falls below 100 kΩ.
The IMD serves two purposes depending on the operating conditions:

1. Standalone Battery Box: When the battery box is used independently without being integrated into the prototype, the IMD monitors the isolation between the high-voltage potentials and the aluminum walls of the box. It continuously measures the insulation resistance and generates an alert if the resistance falls below 100kΩ. This ensures that any potential insulation faults between the high-voltage components and the box walls are detected.

2. Battery Box Integrated into the Prototype: When the battery box is inserted into the prototype and connected to other components, the IMD now monitors the isolation of the entire chassis. It checks the insulation resistance between the various high-voltage potentials and the chassis of the prototype. Again, if the resistance drops below 100kΩ, indicating an insulation fault, the IMD generates an alert.

To provide a visual indication of the insulation status, the isolation monitoring device is connected to an LV located on the access panel at the back of the pod. If the IMD detects an abnormality, such as insulation resistance below the specified threshold, it triggers the LED to illuminate, signaling the presence of

an insulation fault. This allows for easy visual identification of any abnormalities and prompts further investigation or necessary action to rectify the issue promptly, ensuring electrical safety in the prototype.

4.7 Safety and Testing

4.7.1 Safety

In order to evaluate the risks associated with batteries of the given dimension, a FMEA was carried out, leading to the implementation of numerous safety measures. Additionally, the EHW Rules and Regulations incorporates a comprehensive set of rules pertaining to battery handling. This year's power supply strictly adheres to all these rules and, in most cases, surpasses them, ensuring full compliance with safety regulations.

4.7.2 Testing

To ensure that all safety functionalities of the battery system are working properly. They have been all extensively tested. Figure shows the 2023 Testing Plan for the power supply system. Every Test is documented in its own testing document and has been approved by this years engineering lead Tim Aebersold and Focus Coach Luca Rufer. All tests could be conducted successfully and all safety systems were found to operate reliably.

Number	Test	Description	Status	Responsible	Due Date	Video	Comment
1.0	Hardware	Resistor Power Test	100%	Hannes Stählin	14.6	not needed	-The Test how much the temperature of the resistor increases during pre- and discharge
2.0	Hardware/Software	Balancing Demonstration	100%	Hannes Stählin	14.6	not needed	- Demonstrate that BMS can balance individual cells, show results over a longer balancing period
3.0	Hardware/Software	Cell Measurements Test	100%	Hannes Stählin	14.6	not needed	- The BMS can correctly monitor the Voltages and Temperatures of the cells in a pack, show results of significant, meaningful change over time
4.0	Hardware/Software	Emergency Overcurrent	100%	Hannes Stählin	30.5	needed	- Overcurrent is detected through software and hardware and the BMS opens the relays
5.0	Hardware/Software	Emergency Overvoltage	100%	Hannes Stählin	14.6	needed	- Overvoltage is detected and the BMS through software and the BMS opens the relays
6.0	Hardware/Software	Emergency LV-Undervoltage	100%	Hannes Stählin	14.6	needed	- The BMS shuts down and opens the relays, when the voltage of the LV battery drops too low
7.0	Hardware/Software	Emergency Disconnections	100%	Hannes Stählin	30.5	needed	- The BMS shuts down and opens the relays, when disconnecting the LV-Battery, a HV-Battery, the Daisychain or the VCU
8.0	Hardware/Software	Emergency HV-Cell Undervoltage	100%	Hannes Stählin	14.6	needed	- The BMS shuts down and opens the relays, when a HV-Cell drops too low in Voltage
9.0	Hardware	Isolation Test	100%	Hannes Stählin	30.4	not needed	- The Isolations of the Master Board can withstand 1200V

Figure 4.22: Testing Plan for the Power Supply System

The safety concept for the batteries was readily accepted by the EHW safety committee without encountering any issues. [20]

Chapter 5

Conclusion

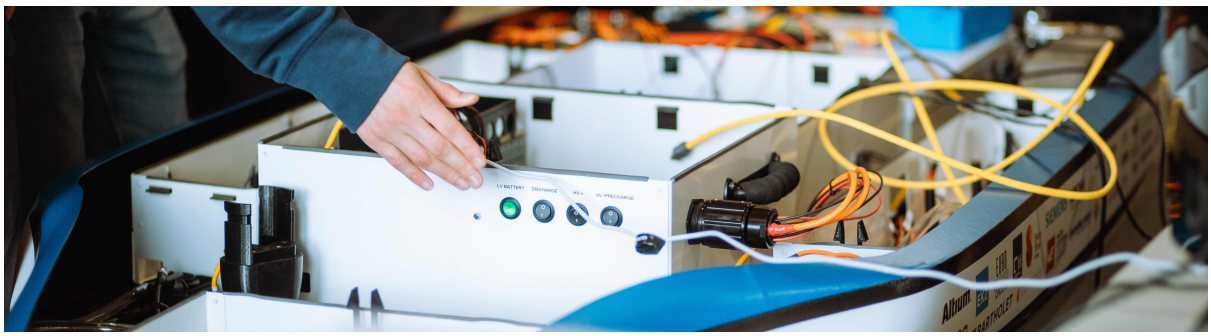

Figure 5.1: Battery box integrated into the prototype

The developed battery system in this project showcases exceptional power capabilities, delivering large amounts of power reliably and safely. By being capable of handling up to 820V, the system has the potential to reach a maximum power output of approximately 203kW. Safety is ensured through the custom BMS equipped with 292 individual sensors and integrated IMD. The BMS can communicate to the VCU via CAN FD, while remaining galvanically isolated from the VCU and other electrical control systems.

The assembly process of the battery is straightforward, facilitated by easily removable crates that can be assembled or disassembled outside the system without space limitations. While electrical integration posed unforeseen challenges, emphasizing simplification in operation and debugging was beneficial. Notably, the inclusion of a display has significantly expedited testing and debugging processes, proving to be an invaluable addition due to its seamless implementation.

A notable feature is the detach ability of the battery box from the prototype, as it can be separated in under 5 seconds. This standalone functionality enables the box to independently monitor and balance the batteries, disconnected from the prototype and other subsystems.

The newly implemented software, built upon FreeRTOS, operates without any issues, providing smooth and error-free functionality. This software framework offers enhanced flexibility and enables faster sampling of critical sensors. In addition, the FPGA-based relay gate control has demonstrated its reliability by consistently performing without any failures.

Chapter 6

Outlook

6.1 European Hyperlook Week

The battery system, which has been developed and tested in this thesis, is scheduled to be showcased and exhibited at the EHW in July 2023. Swissloop aims to secure victories in multiple categories, namely Electrical, Control and Sense, and Full Pod Award, with the power supply system playing a crucial role in all of them.

6.2 Future work and improvements

6.2.1 FPGA Implementation

Throughout the project, it has been evident that utilizing an FPGA to control the gate signals of the relays offers a safer, more space-efficient, and flexible approach. In future iterations of the Master PCB, it is recommended to phase out the legacy logic components and transition to an FPGA-based solution, where all logic functions are consolidated within the FPGA.

6.2.2 Redesigning Slave Boards

Swissloop is currently facing a scarcity of spare BQ Chips, which are no longer in production or supported. These chips play a crucial role in monitoring cell voltages and temperatures on both the Slave and Master PCBs. Given this situation, it may be necessary to consider a redesign of all slave boards, incorporating an updated and enhanced version of the battery monitoring chip as its core.
A redesign presents an excellent opportunity to not only improve the integration and assembly process but also enhance the disassembly of the batteries. An inherent issue with the slave boards used in the past two years is the requirement to disconnect them from the slave boards after testing, as they passively drain energy from the cells they monitor. However, with a few minor modifications, it should be feasible to allow them to remain connected for extended periods, potentially lasting multiple months. This, coupled with the possibility of charging all cells simultaneously, would eliminate the hazardous aspects of battery assembly and disassembly.

6.2.3 Enhanced Electrical Integration

The integration of batteries within the Battery System is of utmost importance. This year, issues with unreliable physical connections were the primary causes of battery problems. To mitigate such issues, it is crucial to ensure that all cables, connectors, and mounting components can withstand the shocks experienced during acceleration and braking. Simplifying the assembly and disassembly processes, including the Master Board if feasible, will enhance system safety and save valuable time. The reliability and ease of operation are critical factors in determining the overall quality of the battery management system.

6.2.4 Individual LV Battery Cell Monitoring

Going forward, it is advisable to monitor individual cells of the LV Battery powering the Master Board rather than relying solely on combined voltage measurements. Establishing a mechanism that can interrupt the power supply in case the voltage of any cell drops below a specified threshold will help prevent undercharging and ensure optimal battery performance.

6.2.5 Inclusion of Acoustic Beeper

To improve the operational awareness of the BMS, it is recommended to incorporate an acoustic beeper. This beeper can alert operators in the event of an isolation fault detected by the IMD or prompt them to replace the LV battery before the BMSs initiates a last-resort power cut-off. Although these errors already raise emergencies in this year's pod, their detection can go unnoticed if there are other errors during comprehensive pod testing. The addition of an acoustic beeper will provide an additional layer of notification to ensure prompt attention to critical issues.

6.2.6 Supercapacitors

Deeper research into super capacitors is something that could be approached especially if very high power burst are requested.

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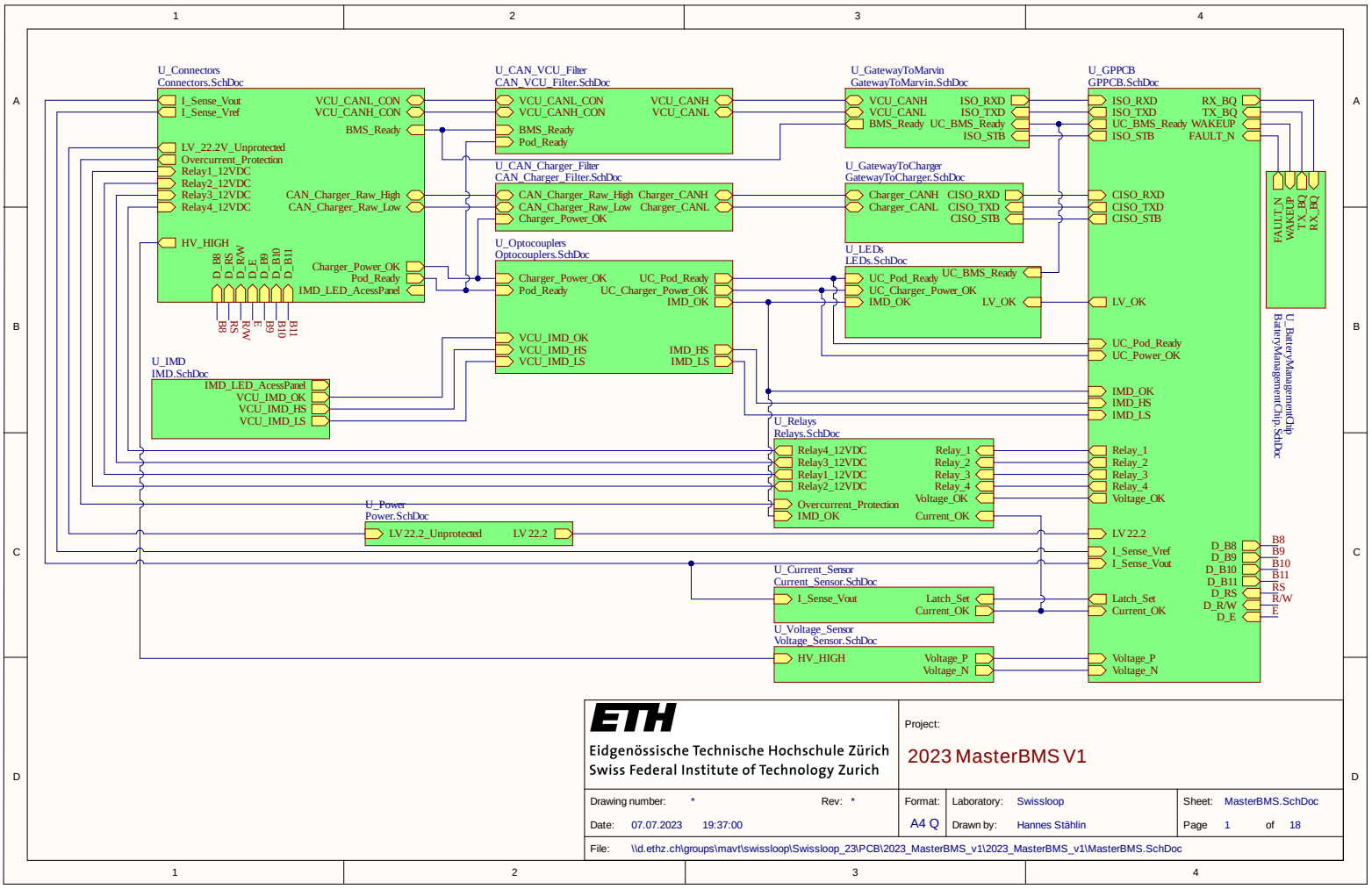
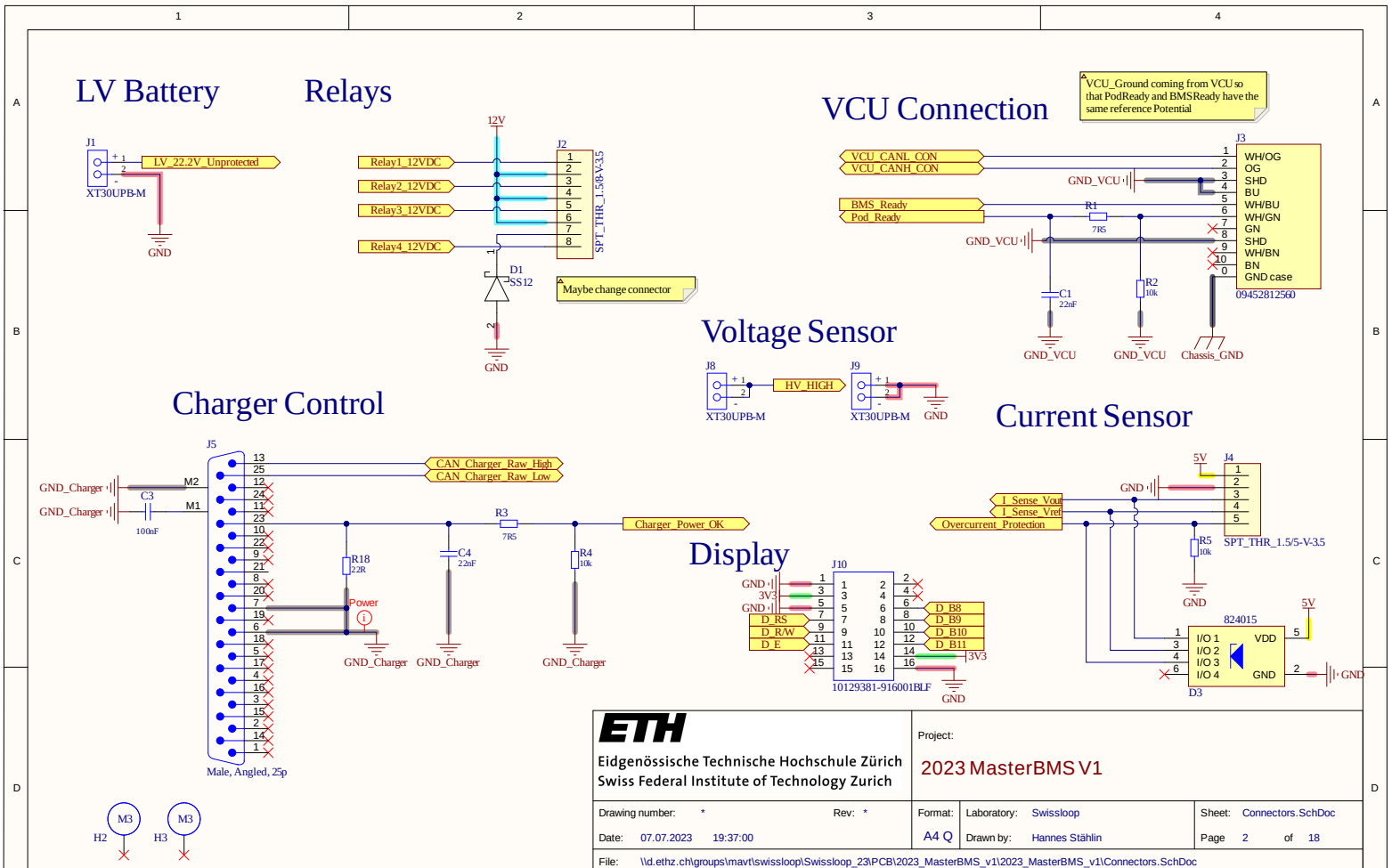
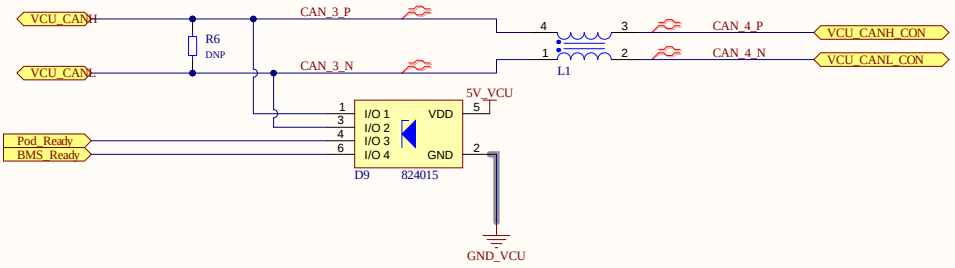
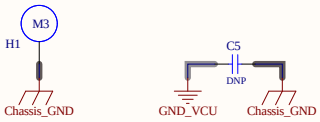
Appendix A

Master PCB Schematics


U_Connectors
Connectors.SchDoc
I_Sense_Vout
I_Sense_Vref
VCU_CANL_CON
VCU_CANH_CON
BMS_Ready
LV_22.2V_Unprotected
Overcurrent_Protection
Relay1_12VDC
Relay2_12VDC
Relay3_12VDC
Relay4_12VDC
CAN_Charger_Raw_High
CAN_Charger_Raw_Low
HV_HIGH
D_B8
D_RS
D_R/W
D_E
D_B9
D_B10
D_B11
Charger_Power_OK
Pod_Ready
IMD_LED_AcessPanel
U_CAN_VCU_Filter
CAN_VCU_Filter.SchDoc
VCU_CANH
U_CAN_Charger_Filter
CAN_Charger_Filter.SchDoc
Charger_CANH
Charger_CANL
U_Optocouplers
Optocouplers.SchDoc
UC_Pod_Ready
UC_Charger_Power_OK
IMD_OK
VCU_IMD_OK
VCU_IMD_HS
VCU_IMD_LS
IMD_HS
IMD_LS
U_IMD
IMD.SchDoc
U_Power
Power.SchDoc
LV 22.2_Unprotected
LV 22.2
U_GatewayToMarvin
GatewayToMarvin.SchDoc
ISO_RXD
ISO_TXD
UC_BMS_Ready
ISO_STB
U_GatewayToCharger
GatewayToCharger.SchDoc
CISO_RXD
CISO_TXD
CISO_STB
U_LEDs
LEDs.SchDoc
LV_OK
U_Relays
Relays.SchDoc
Relay_1
Relay_2
Relay_3
Relay_4
Voltage_OK
Current_OK
U_Current_Sensor
Current_Sensor.SchDoc
Latch_Set
U_Voltage_Sensor
Voltage_Sensor.SchDoc
Voltage_P
Voltage_N
U_GPPCB
GPPCB.SchDoc
RX_BQ
TX_BQ
WAKEUP
FAULT_N
U_BatteryManagementChip
BatteryManagementChip.SchDoc
B8
B9
B10
B11
RS
R/W
E
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project:
2023 MasterBMS V1
Drawing number: *
Rev: *
Format: A4 Q
Laboratory: Swissloop
Drawn by: Hannes Stählin
Sheet: MasterBMS.SchDoc
Page 1 of 18
Date: 07.07.2023 19:37:00
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\MasterBMS.SchDoc

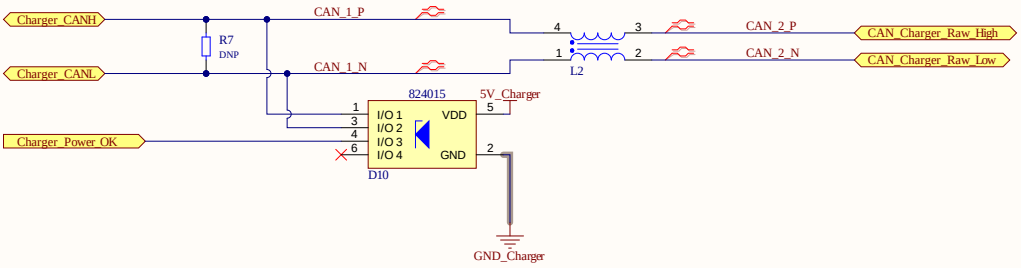

LV Battery
J1
XT30UPB-M
LV_22.2V_Unprotected
GND
Relays
12V
J2
Relay1_12VDC
Relay2_12VDC
Relay3_12VDC
Relay4_12VDC
SPT_THR_1.5/8-V-3.5
D1
SS12
Maybe change connector
VCU Connection
VCU_Ground coming from VCU so that PodReady and BMSReady have the same reference Potential
VCU_CANL_CON
VCU_CANH_CON
BMS_Ready
Pod_Ready
J3
WH/OG
OG
SHD
BU
WH/BU
WH/GN
GN
SHD
WH/BN
BN
GND case
09452812560
GND_VCU
R1
7R5
C1
22nF
R2
10k
Chassis_GND
Voltage Sensor
J8
J9
HV_HIGH
Charger Control
J5
Male, Angled, 25p
CAN_Charger_Raw_High
CAN_Charger_Raw_Low
GND_Charger
M2
M1
C3
100nF
R3
7R5
Charger_Power_OK
R18
22R
Power
C4
22nF
R4
10k
Current Sensor
5V
J4
I_Sense_Vout
I_Sense_Vref
Overcurrent_Protection
SPT_THR_1.5/5-V-3.5
R5
10k
Display
J10
D_B8
D_B9
D_B10
D_B11
3V3
D_RS
D_R/W
D_E
10129381-916001BLF
824015
I/O 1
I/O 2
I/O 3
I/O 4
VDD
D3
H2
H3
M3
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project:
2023 MasterBMS V1
Drawing number: *
Rev: *
Format: A4 Q
Laboratory: Swissloop
Drawn by: Hannes Stählin
Sheet: Connectors.SchDoc
Page 2 of 18
Date: 07.07.2023 19:37:00
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\Connectors.SchDoc



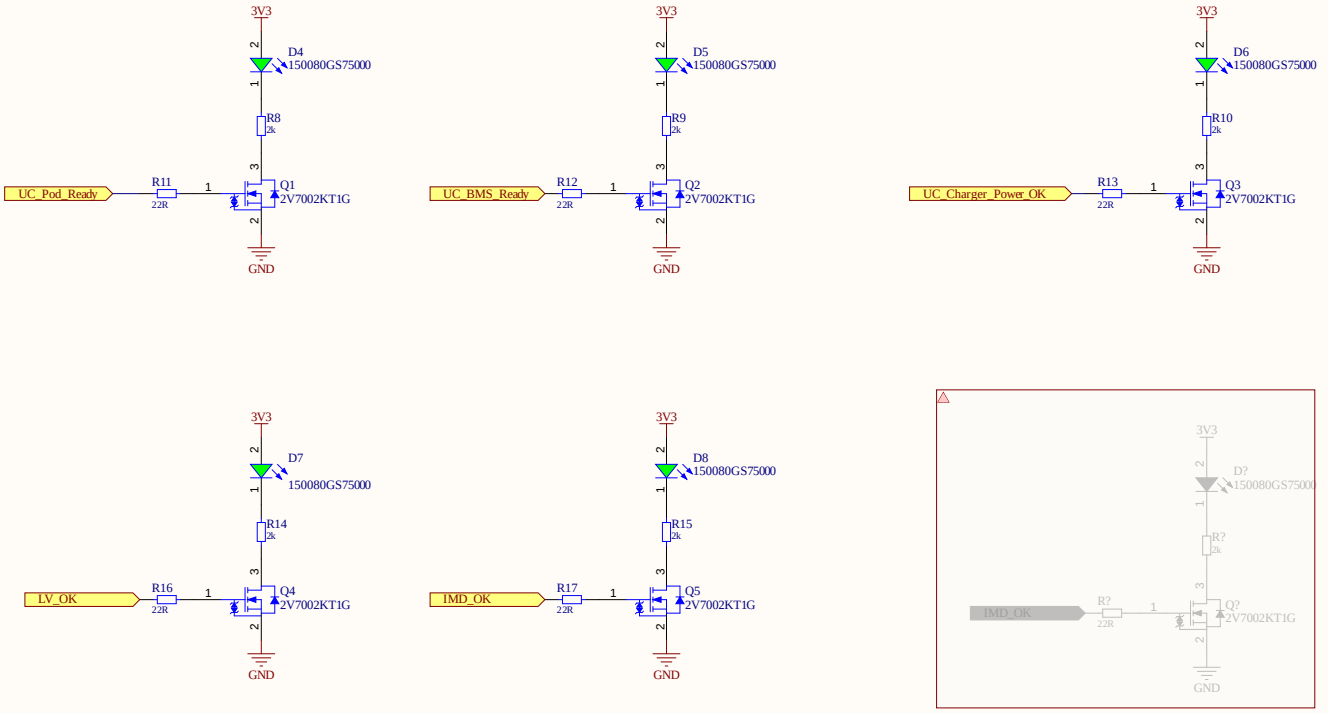


ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: 2023 MasterBMS V1		
Drawing number: * Rev: *	Format: A4 Q	Laboratory: Swissloop	Sheet: CAN_VCU_Filter.SchDoc
Date: 07.07.2023 19:37:00		Drawn by: Hannes Stählin	Page 3 of 18
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\CAN_VCU_Filter.SchDoc			

Neu in 2023:
744235510 CMC für CAN
Wuerth approved!



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: 2023 MasterBMS V1		
Drawing number: * Rev: *	Format: A4 Q	Laboratory: Swissloop	Sheet: CAN_Charger_Filter.SchDoc
Date: 07.07.2023 19:37:00		Drawn by: Hannes Stählin	Page 4 of 18
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\CAN_Charger_Filter.SchDoc			



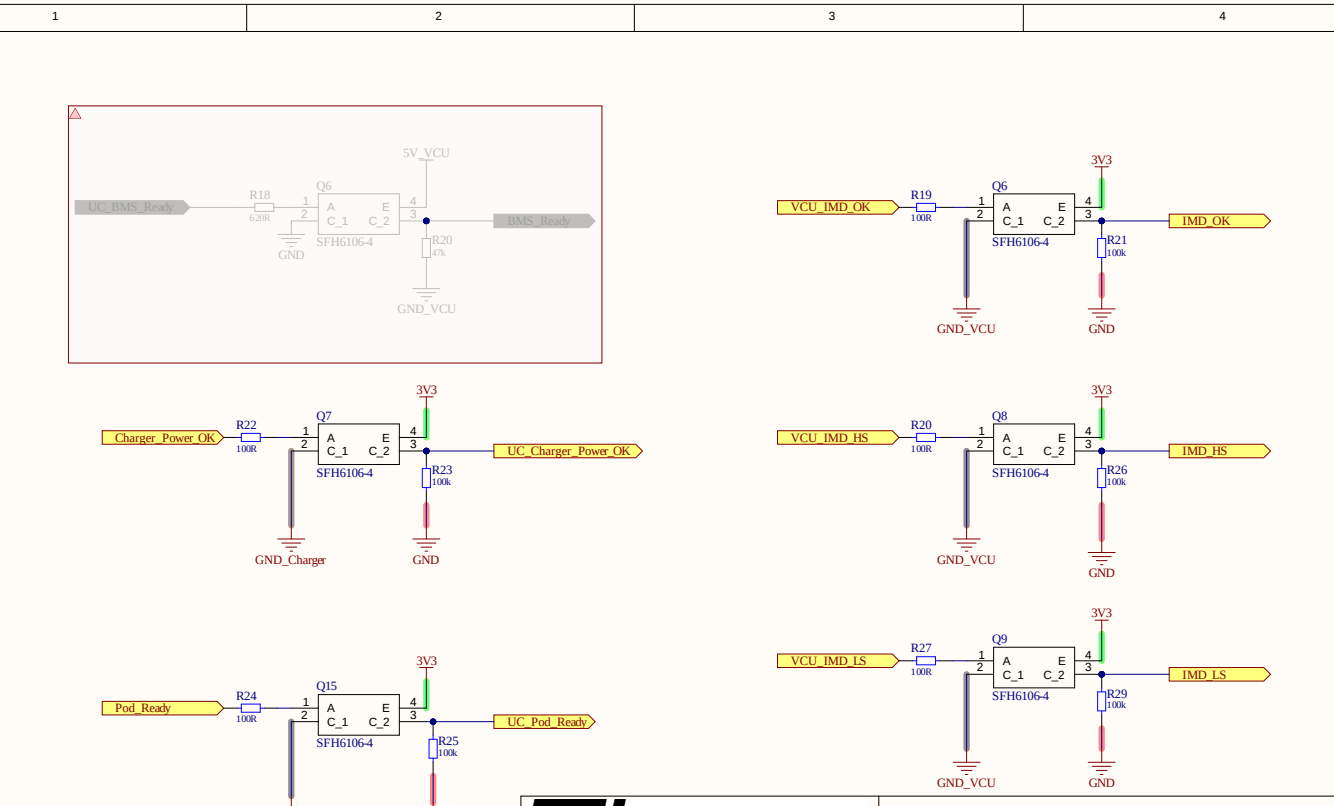
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: 2023 MasterBMS V1

Drawing number: * Rev: *	Format: A4 Q	Laboratory: Swissloop	Sheet: LEDs.SchDoc
Date: 07.07.2023 19:37:00		Drawn by: Hannes Stählin	Page 5 of 18

File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\LEDs.SchDoc

Text

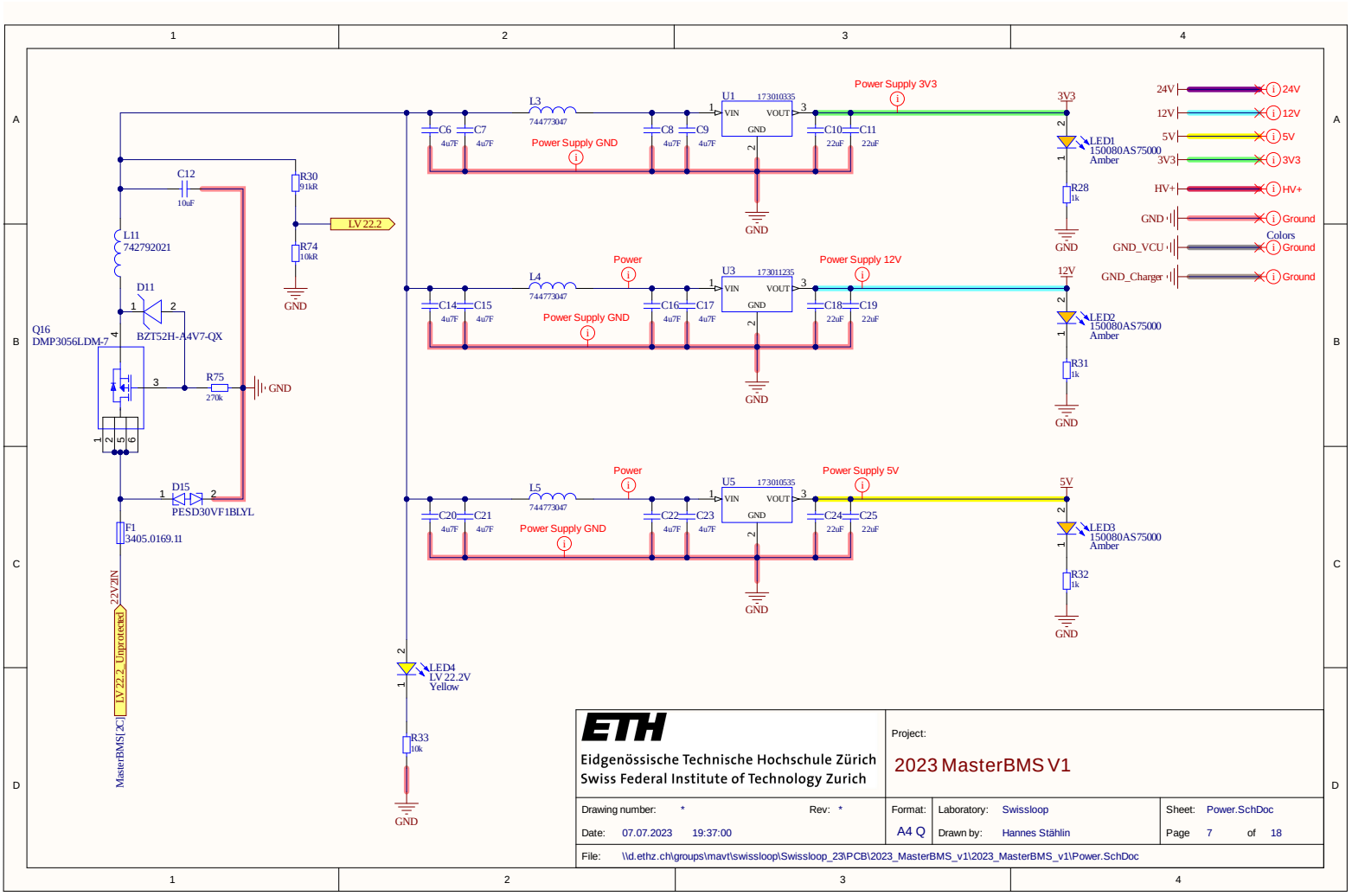


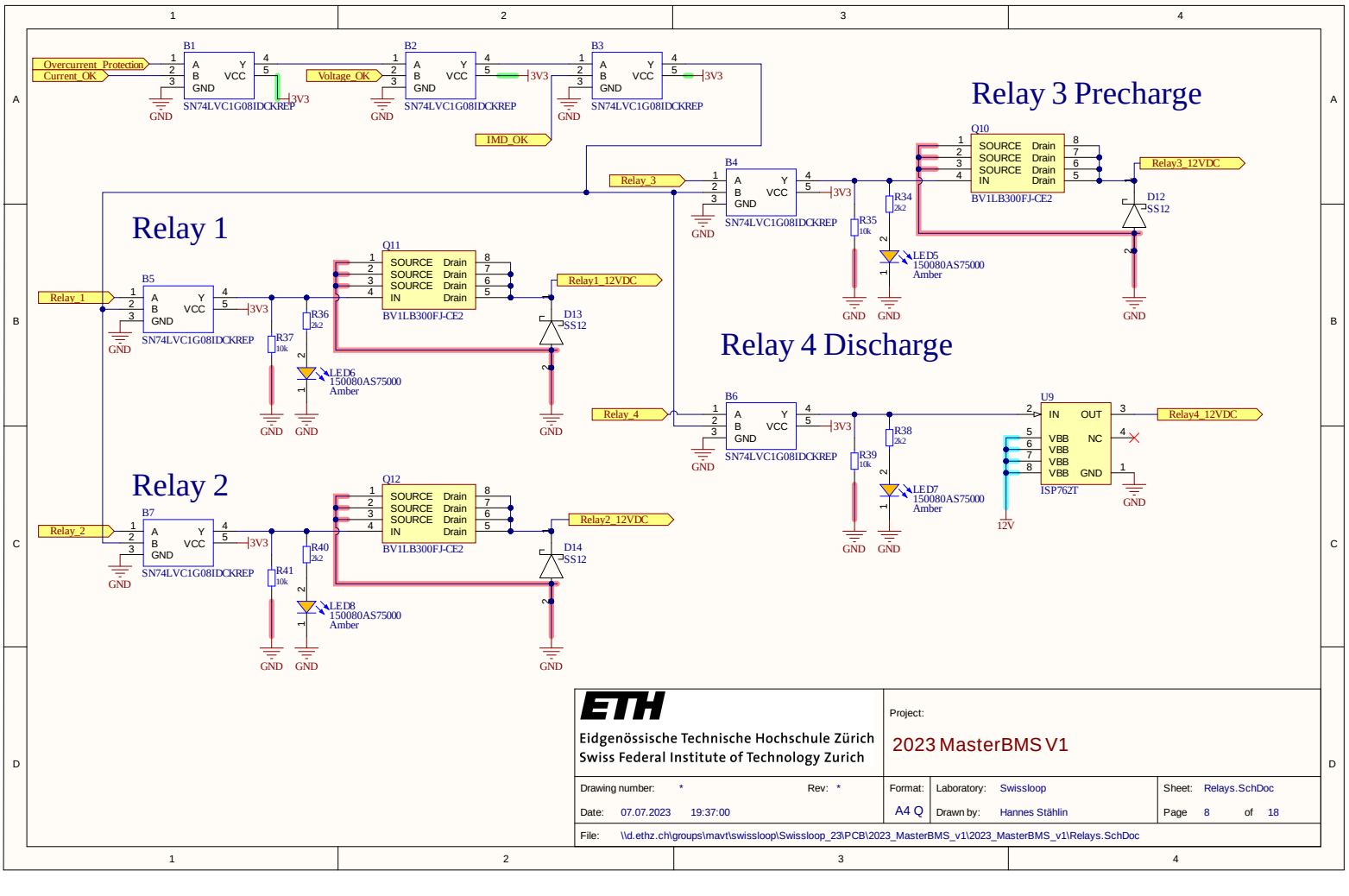
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: 2023 MasterBMS V1

Drawing number: * Rev: *	Format: A4 Q	Laboratory: Swissloop	Sheet: Optocouplers.SchDoc
Date: 07.07.2023 19:37:00		Drawn by: Hannes Stählin	Page 6 of 18

File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\Optocouplers.SchDoc


Power Supply 3V3
Power Supply 12V
Power Supply 5V
Power Supply GND
Power
LV 22.2
LV 22.2_Unprotected
22V2IN
MasterBMS[2C]
24V
12V
5V
3V3
HV+
Ground
GND_VCU
GND_Charger
Colors
LED1 150080AS75000 Amber
LED2 150080AS75000 Amber
LED3 150080AS75000 Amber
LED4 LV 22.2V Yellow
U1 173010335
U3 173011235
U5 173010535
L3 744773047
L4 744773047
L5 744773047
Q16 DMP3056LDM-7
D11 BZT52H-A4V7-QX
D15 PESD30VF1BLYL
F1 3405.0169.11
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project:
2023 MasterBMS V1
Drawing number: *
Rev: *
Format: A4 Q
Laboratory: Swissloop
Drawn by: Hannes Stählin
Sheet: Power.SchDoc
Page 7 of 18
Date: 07.07.2023 19:37:00
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\Power.SchDoc


Relay 1
Relay 2
Relay 3 Precharge
Relay 4 Discharge
Overcurrent_Protection
Current_OK
Voltage_OK
1MD_OK
Relay_1
Relay_2
Relay_3
Relay_4
Relay1_12VDC
Relay2_12VDC
Relay3_12VDC
Relay4_12VDC
SN74LVC1G08IDCKREP
BV1LB300FJ-CE2
ISP762T
LED5 150080AS75000 Amber
LED6 150080AS75000 Amber
LED7 150080AS75000 Amber
LED8 150080AS75000 Amber
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project:
2023 MasterBMS V1
Drawing number: *
Rev: *
Format: A4 Q
Laboratory: Swissloop
Drawn by: Hannes Stählin
Sheet: Relays.SchDoc
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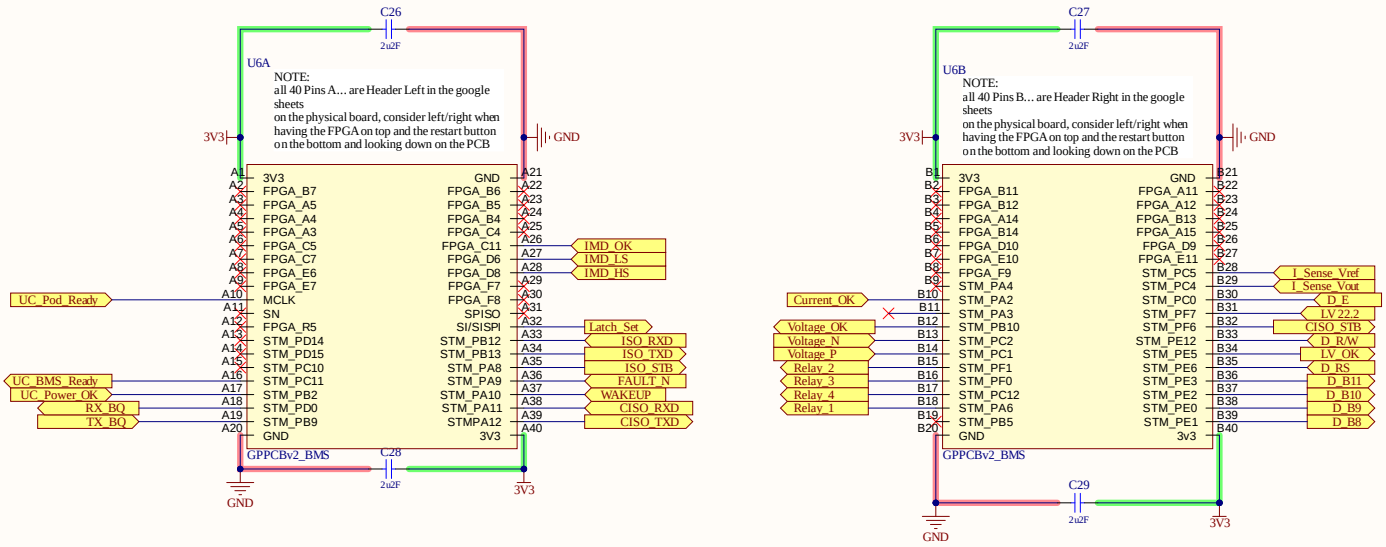
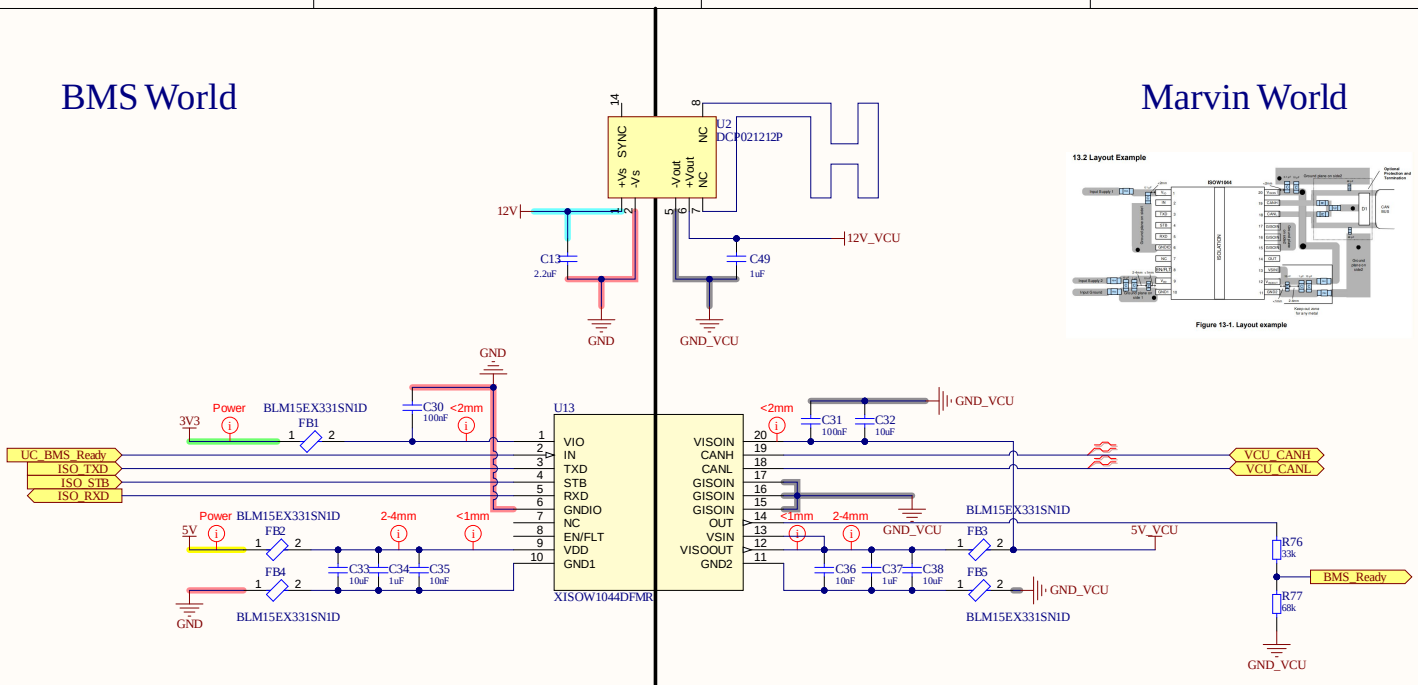
Date: 07.07.2023 19:37:00
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\Relays.SchDoc



ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: 2023 MasterBMS V1

Drawing number: *	Rev: *	Format: A4 Q	Laboratory: Swissloop	Sheet: GPPCB.SchDoc	
Date: 07.07.2023 19:37:00			Drawn by: Hannes Stählin	Page 9 of 18	
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\GPPCB.SchDoc					



To make sure that operation is reliable at all data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible. Power converter input VDD and output VISOOUT supply pins should have high frequency ceramic capacitors 10 nF and bulk capacitors 10 µF atleast close to the pins. Signal path supply pins, VIO and VISOIN, should have 100 nF or higher value ceramic bypass capacitors close to device pins. ISOW10144 can consume typical peak pulse currents of upto 250mA under fully loaded conditions for short durations (10s of µs) from the power source that is powering VDD of ISOW1044. Please make sure the current limit of upstream power device is atleast 300mA typical.

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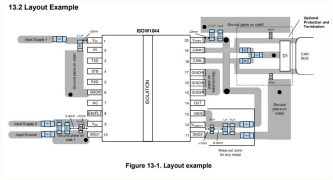
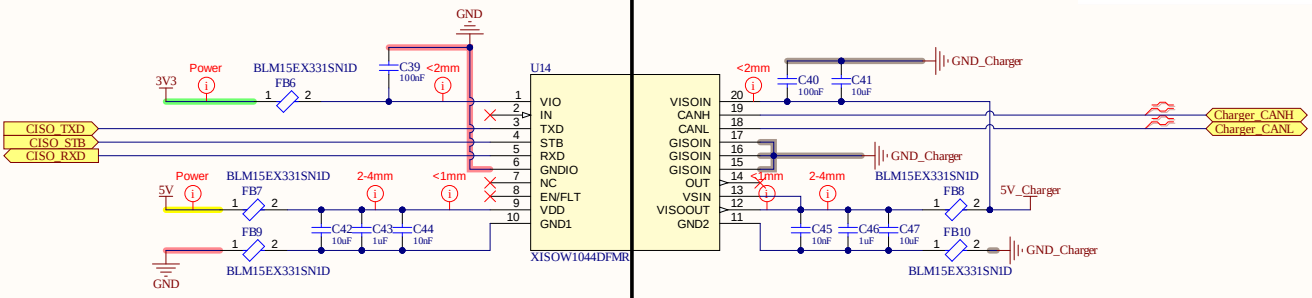
Project: 2023 MasterBMS V1

Drawing number: *	Rev: *	Format: A4 Q	Laboratory: Swissloop	Sheet: GatewayToMarvin.SchDoc	
Date: 07.07.2023 19:37:00			Drawn by: Hannes Stählin	Page 10 of 18	
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\GatewayToMarvin.SchDoc					

BMS World

Charger World





To make sure that operation is reliable at all data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible. Power converter input VDD and output VISOOUT supply pins should have high frequency ceramic capacitors 10 nF and bulk capacitors 10 µF atleast close to the pins. Signal path supply pins, VIO and VISOIN , should have 100 nF or higher value ceramic bypass capacitors close to device pins. ISOW10144 can consume typical peak pulse currents of upto 250mA under fully loaded conditions for short durations (10s of µs) from the power source that is powering VDD of ISOW1044. Please make sure the current
limit of upstream power device is atleast 300mA typical.

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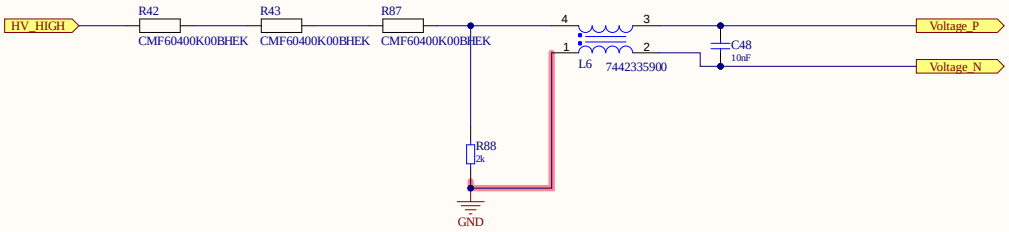
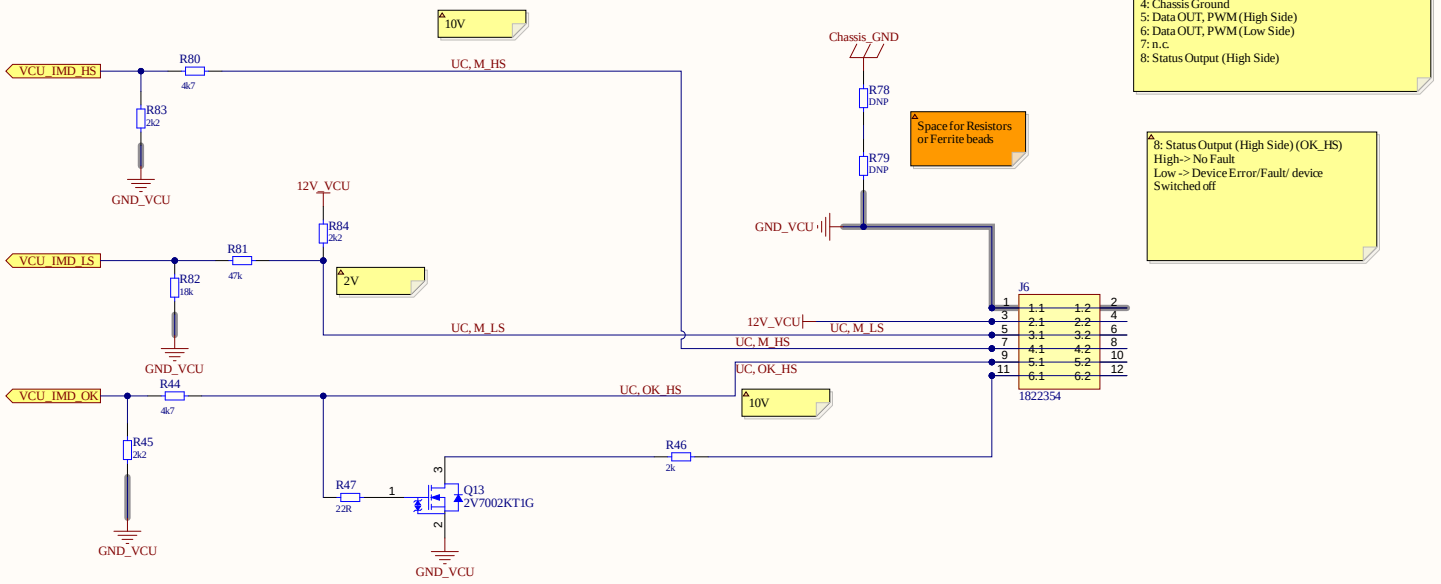
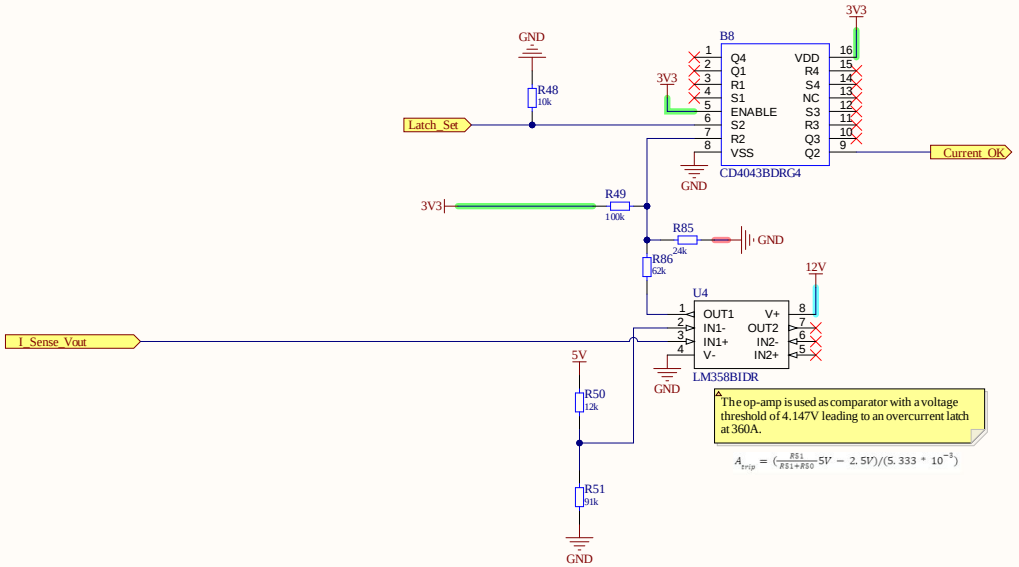
Drawing number: *	Rev: *	Format: A4 Q	Laboratory: Swissloop	Sheet: GatewayToCharger.SchDoc
Date: 07.07.2023 19:37:00			Drawn by: Hannes Stählin	Page 11 of 18
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\GatewayToCharger.SchDoc				



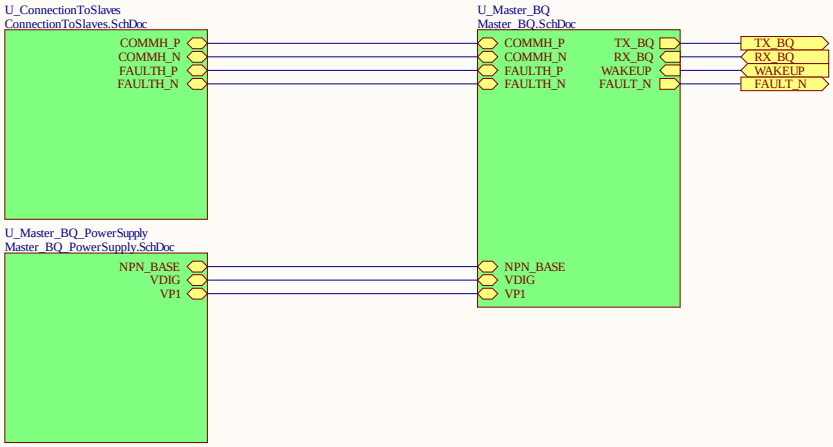
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich			Project: 2023 MasterBMS V1	
Drawing number: *	Rev: *	Format: A4 Q	Laboratory: Swissloop	Sheet: Voltage_Sensor.SchDoc
Date: 07.07.2023 19:37:00			Drawn by: Hannes Stählin	Page 12 of 18
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\Voltage_Sensor.SchDoc				



Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: 2023 MasterBMS V1		
Drawing number: * Rev: *	Format: A4 Q	Laboratory: Swissloop	Sheet: IMD.SchDoc
Date: 07.07.2023 19:37:01		Drawn by: Hannes Stählin	Page 13 of 18
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\IMD.SchDoc			



Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: 2023 MasterBMS V1		
Drawing number: * Rev: *	Format: A4 Q	Laboratory: Swissloop	Sheet: Current_Sensor.SchDoc
Date: 07.07.2023 19:37:01		Drawn by: Hannes Stählin	Page 14 of 18
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\Current_Sensor.SchDoc			



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Project: 2023 MasterBMS V1

Drawing number: *	Rev: *	Format: A4 Q	Laboratory: Swissloop
Date: 07.07.2023 19:37:01			Drawn by: Hannes Stählin
Sheet: BatteryManagementChip.SchDoc			
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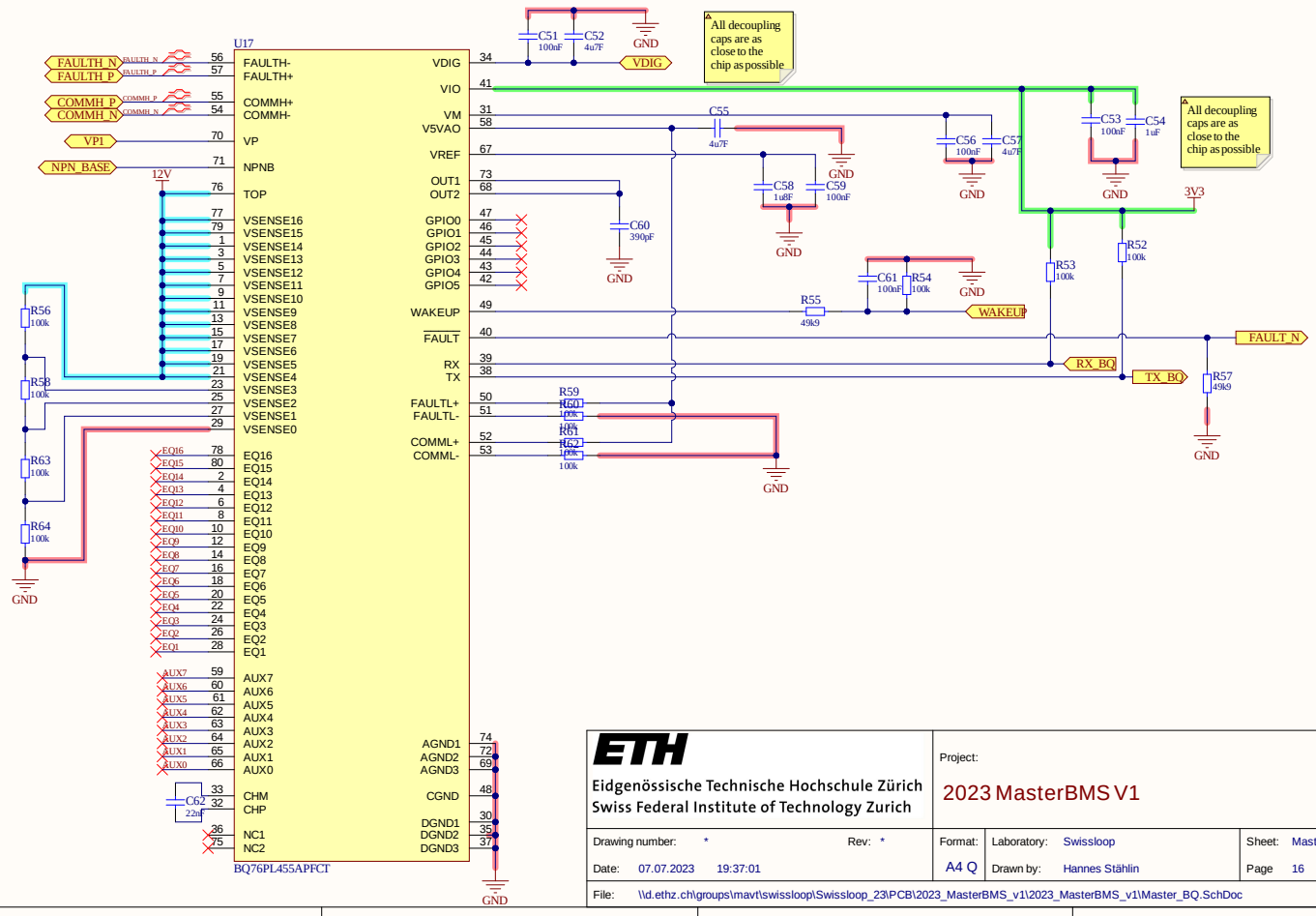
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\BatteryManagementChip.SchDoc



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Project: 2023 MasterBMS V1

Drawing number: *	Rev: *	Format: A4 Q	Laboratory: Swissloop
Date: 07.07.2023 19:37:01			Drawn by: Hannes Stählin
Sheet: Master_BQ.SchDoc			
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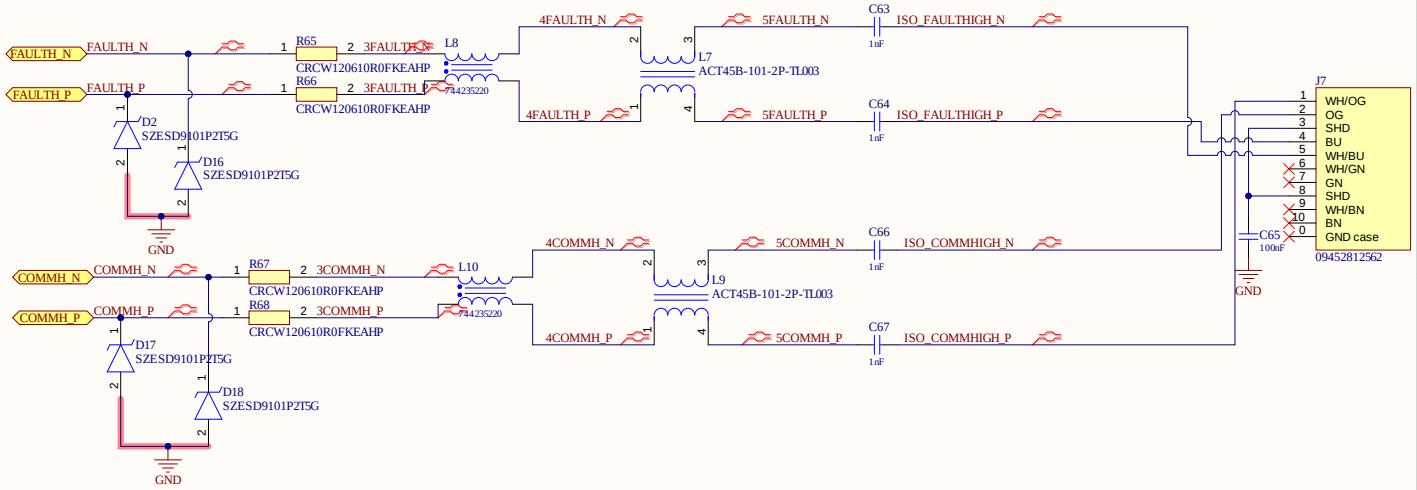
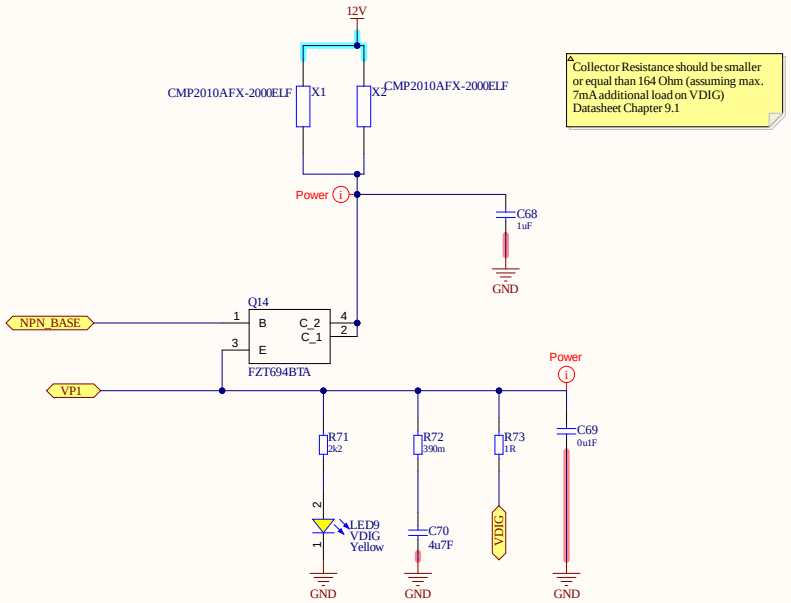
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\Master_BQ.SchDoc



Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: 2023 MasterBMS V1	
Drawing number: * Rev: *	Format: A4 Q	Laboratory: Swissloop Drawn by: Hannes Stählin
Date: 07.07.2023 19:37:01		Sheet: ConnectionToSlaves.SchDoc Page 17 of 18
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\ConnectionToSlaves.SchDoc		



Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: 2023 MasterBMS V1	
Drawing number: * Rev: *	Format: A4 Q	Laboratory: Swissloop Drawn by: Hannes Stählin
Date: 07.07.2023 19:37:01		Sheet: Master_BQ_PowerSupply.SchDoc Page 18 of 18
File: \\d.ethz.ch\groups\mavt\swissloop\Swissloop_23\PCB\2023_MasterBMS_v1\2023_MasterBMS_v1\Master_BQ_PowerSupply.SchDoc		

Appendix B

Automatic State Transitions

The conditions for the automatic transition between the states in the VFSM (Figure 3.2) of the MCU code are listed below:

1: Reset to Emergency Transition if one of the following conditions is met.

(a) For all cells
   i. Cell voltage outside allowed range
   ii. Cell temperature outside allowed range

(b) Isolation Monitoring Device (IMD)
   i. The IMD detects an isolation fault.

(c) Current Sensor
   i. The Current Sensor detects a current.

(d) Voltage Sensor
   i. Voltage outside allowed range.

2: Reset to Idle

(a) All systems completely initialized

3: Idle to Emergency

(a) For all cells
   i. Cell voltage outside allowed range
   ii. Cell temperature outside allowed range

(b) Isolation Monitoring Device (IMD)
   i. The IMD detects an isolation fault.

(c) Current Sensor
   i. The Current Sensor detects a current.

(d) Voltage Sensor
   i. Voltage outside allowed range.

(e) Lost connection to the slave boards.

(f) Propagated emergency from VCU

(g) LV batteries
   i. Battery voltage $<$ 19.2V
   ii. Battery voltage $>$ 30V

(h) VCU is not in reset, idle or stop or start state.

4: Idle to Precharge

(a) VCU is in Ready state.

5: Precharge to Emergency

(a) For all cells
   i. Cell voltage outside allowed range
   ii. Cell temperature outside allowed range

(b) Isolation Monitoring Device (IMD)
   i. The IMD detects an isolation fault.

(c) Current Sensor
   i. Current $>$ 10A.

(d) Voltage Sensor
   i. Voltage outside allowed range.

(e) Lost connection to the slave boards.

(f) Propagated emergency from VCU

(g) LV batteries
   i. Battery voltage $<$ 19.2V
   ii. Battery voltage $>$ 25.2V

(h) VCU is not in ready state.

6: Precharge to Active

(a) Voltage Sensor
   i. Voltage $>$ 620V .

(b) Current Sensor
   i. Current $<$ 5A .

7: Active to Emergency

(a) For all cells
   i. Cell voltage outside allowed range
   ii. Cell temperature outside allowed range

(b) Isolation Monitoring Device (IMD)
    i. The IMD detects an isolation fault.
(c) Current Sensor
    i. Current $>$ 250A.
(d) Voltage Sensor
    i. Voltage $>$ 820V.
(e) Lost connection to the slave boards.
(f) Propagated emergency from VCU
(g) LV batteries
    i. Battery voltage $<$ 19.2V
    ii. Battery voltage $>$ 25.2V
(h) VCU is not in ready, run, braking or stop state.

8: Active to/from Regenerative Braking

(a) Relevant command from VCU

9: Active to Discharge

(a) Relevant command from VCU
(b) Current Sensor
    i. Current $<$ 100A.

10: Regenerative Braking to Emergency

(a) For all cells
    i. Cell voltage outside allowed range
    ii. Cell temperature outside allowed range
(b) Isolation Monitoring Device (IMD)
    i. The IMD detects an isolation fault.
(c) Current Sensor
    i. Current not in the allowed range.
(d) Voltage Sensor
    i. Voltage $>$ 1000V.
(e) Lost connection to the slave boards.
(f) Propagated emergency from VCU
(g) LV batteries
    i. Battery voltage $<$ 19.2V
    ii. Battery voltage $>$ 25.2V
(h) VCU is not in braking or stop state.

11: Regenerative Braking to Discharge

(a) Relevant command from VCU
(b) Current Sensor
    i. Current $<$ 100A.

12: Discharge to Emergency

(a) For allcells
    i. Cell voltage outside allowed range
    ii. Cell temperature outside allowed range
(b) Isolation Monitoring Device (IMD)
    i. The IMD detects an isolation fault.
(c) Current Sensor
    i. Current $>$ 20A
(d) Voltage Sensor
    i. Voltage $>$ 1000V.
(e) Lost connection to the slave boards.
(f) Propagated emergency from VCU
(g) LV batteries
    i. Battery voltage $<$ 19.2V
    ii. Battery voltage $>$ 25.2V
(h) VCU is not in stop state.

13: Discharge to Idle

(a) Voltage Sensor
    i. Voltage $<$ 35V .
(b) Current Sensor
    i. Current $<$ 5A .

14: Emergency to Reset

(a) None (if the error persists, the pod will reenter the emergency state after reset)

15: Idle to Charging

(a) Manual Transition

16: Charging to Idle

(a) Manual Transition

17: Charging to Emergency

(a) For all cells
    i. Cell voltage outside allowed range
    ii. Cell temperature outside allowed range
(b) Isolation Monitoring Device (IMD)
    i. The IMD detects an isolation fault.
(c) Current Sensor
    i. Current $>$ 20A
(d) Voltage Sensor
    i. Voltage $>$ 820V.
(e) Lost connection to the slave boards.
(f) Propagated emergency from VCU
(g) LV batteries
    i. Battery voltage $<$ 19.2V
    ii. Battery voltage $>$ 25.2V

13: Discharge to Idle

(a) Voltage Sensor
    i. Voltage $<$ 35V .
(b) Current Sensor
    i. Current $<$ 5A .

In addition to all described transitions it is possible to manually enter the emergency state from any state at any time.