

Guest Editorial Circuits, Systems, and Algorithms for Beyond 5G and Toward 6G

Other Journal Item**Author(s):**

Zhang, Chuan; Liu, Liang; Studer, Christoph 

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Guest Editorial

Circuits, Systems, and Algorithms for Beyond 5G and Toward 6G

THIS special section of the IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS (OJCS) is dedicated to highlight the state-of-the-art research progress on circuits, systems, and algorithms associated with the design of beyond 5G (B5G) and 6G wireless systems.

In order to meet the requirements raised by emerging applications, such as Industry 4.0, Internet of Things, vehicle-to-everything (V2X), Smart City, Smart Healthcare, Intelligent Logistics, e-learning, new techniques have been identified for B5G and 6G. Research initiatives on circuits, systems, and algorithms are needed for the design, optimization, and implementation of B5G/6G systems. Advances in signal processing solutions, system architectures, and optimized implementations are expected. These new techniques of wireless systems are posing new challenges in an unconventional way, especially from the circuits and systems perspective. It is necessary to help interested researchers to identify the technical challenges, emerging techniques, and recent results related to this area.

This special section is devoted to providing a comprehensive perspective on the state of research on circuits, systems, and algorithms for B5G and 6G through a collection of recent contributions. The selected 5 papers cover both system and module design and implementation for B5G/6G systems.

The first paper is titled “Towards Intelligent Reconfigurable Wireless Physical Layer (PHY),” by Singh *et al.* and proposes the design and implementation of a reconfigurable PHY via a hardware-software co-design approach. Both the ARM processor and FPGA have been employed. Intelligence has been incorporated into the reconfigurability with online machine learning (OML) based decision-making algorithm. Following the first paper, the remaining papers focus on different components of emerging systems, including channelizer, sequence detection, channel estimator, and LDPC decoder.

The second paper is titled “A High-Throughput Oversampled Polyphase Filter Bank Using Vivado HLS and PYNQ on a RFSoc,” by Smith *et al.* and focuses on the design and implementation of a 4 GHz oversampled polyphase channelizer implemented on a Xilinx RFSoc. Compared to the existing FPGA designs incorporating Vivado HLS, the presented design enjoys a larger

input bandwidth (4 GHz) and greater FPGA fabric speed (512 MHz).

The third paper is titled “Massive Machine-Type Communication Pilot-Hopping Sequence Detection Architectures Based on Non-Negative Least Squares for Grant-Free Random Access,” by Sarband *et al.* and proposes two hardware architectures to solve the NNLS problem for the mMTC pilot-hopping sequence detection. Both architectures have been evaluated with a 28 nm FD-SOI standard cell process at 1 V power supply voltage.

The fourth paper is titled “Channel Estimation for Advanced 5G/6G Use Cases on a Vector Digital Signal Processor” by Damjancevic *et al.* and proposes a software implementation process that can dynamically balance latency and throughput. Results have shown that the proposed process can effectively avoid both unnecessary hardware power cost for given use-cases.

The last paper in this group is titled “GPU-Based, LDPC Decoding for 5G and Beyond,” by Tarver *et al.* and demonstrates a high-throughput and low-latency LDPC decoder based on GPUs. Experimental results have shown that this decoder can provide high performance required by 5G and beyond while maintaining the advantages of a software-based decoder.

ACKNOWLEDGMENT

The Guest Editors would like to thank all the authors for contributing technical excellence for this special section. Without their outstanding contribution, we would not be able to keep the high quality for this OJCS special section. We also would like to thank the anonymous reviewers for providing their valuable comments in improving this special section. We are grateful to the Editor-in-Chief (EiC) Dr. Gabriele Manganaro for his consistent guidance, support, and advice. Last but not least, we are grateful to IEEE Publishing Operations personnel for their great efforts and patience in finalizing this special issue. By committing itself to the emerging techniques of circuits and systems for B5G and 6G, we hope this special section will be very interesting for a large portion of related researchers, and inspire further progress in this important research area.

CHUAN ZHANG, *Guest Editor*

Laboratory of Efficient Architectures for
Digital-Communication and Signal-Processing
Southeast University
Nanjing 211189, China
National Mobile Communications Research Laboratory
Southeast University
Nanjing 211189, China
Purple Mountain Laboratories
Nanjing 211189, China

LIANG LIU, *Guest Editor*

Department of Electrical and Information Technology
Lund University
221 00 Lund, Sweden

CHRISTOPH STUDER, *Guest Editor*

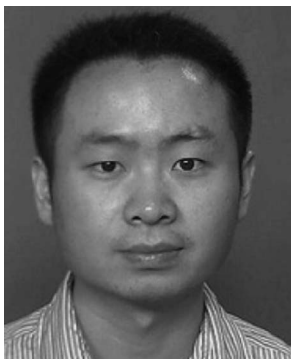
Department of Information Technology and Electrical
Engineering
ETH Zürich
8029 Zürich, Switzerland



CHUAN ZHANG (Senior Member, IEEE) received the B.E. degree in microelectronics and the M.E. degree in very-large-scale integration (VLSI) design from Nanjing University, Nanjing, China, in 2006 and 2009, respectively, and the M.S.E.E. and Ph.D. degrees from the Department of Electrical and Computer Engineering, University of Minnesota, Twin Cities (UMN), USA, in 2012.

He is currently the Excellence Professor and the Purple Mountain Professor with Southeast University. He is also with LEADS, National Mobile Communications Research Laboratory, Quantum Information Center, Southeast University, and Purple Mountain Laboratories, Nanjing. His current research interests include low-power high-speed VLSI design for digital signal processing and digital communication, biochemical computation and neuromorphic engineering, and quantum communication.

Dr. Zhang received the Best Contribution Award of the IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS) in 2018, the Best Paper Award in 2016, the Best (Student) Paper Award of the IEEE International Conference on DSP in 2016, three Best (Student) Paper Awards of the IEEE International Conference on ASIC in 2015, 2017, and 2019, the Best Paper Award Nomination of the IEEE Workshop on Signal Processing Systems in 2015, three Excellent Paper Awards and two Excellent Poster Presentation Awards of the International Collaboration Symposium on Information Production and Systems from 2016 to 2018, the Outstanding Achievement Award of the Intel Collaborative Research Institute in 2018, and the Merit (Student) Paper Award of the IEEE APCCAS in 2008. He also received the Three-Year University-Wide Graduate School Fellowship of UMN and the Doctoral Dissertation Fellowship of UMN. He serves as an Associate Editor for the IEEE TRANSACTIONS ON SIGNAL PROCESSING and IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS. He serves as a Corresponding Guest Editor for the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS twice. He is also the Secretary-Elect of the Circuits and Systems for Communications TC of the IEEE Circuits and Systems Society. He is also a member of the Seasonal School of Signal Processing and Design and Implementation of Signal Processing Systems TC of the IEEE Signal Processing Society, and Circuits and Systems for Communications TC, VLSI Systems and Applications TC, and Digital Signal Processing TC of the IEEE Circuits and Systems Society.



LIANG LIU (Member, IEEE) received the B.S. degree from the Department of Electronics Engineering, Fudan University, Shanghai, China, in 2005, and the Ph.D. degree from the Department of Microelectronics, Fudan University in 2010. In 2010, he was with Rensselaer Polytechnic Institute, USA, as a Visiting Researcher. He joined the Department of Electrical and Information Technology (EIT), Lund University, Lund, Sweden, where he was a Postdoctoral Fellow in 2010. Since 2016, he has been an Associate Professor with the Department of EIT, Lund University. His current research interests include wireless communication system and digital integrated circuits design. He is a Board Member of the IEEE Swedish SSC/CAS Chapter. He is also a member of the Technical Committee of VLSI Systems and Applications and CAS for Communications of the IEEE Circuit and Systems Society.



CHRISTOPH STUDER (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from ETH Zürich, Switzerland, in 2009.

In 2005, he was a Visiting Researcher with the Smart Antennas Research Group, Stanford University. From 2006 to 2009, he was a Research Assistant with the Integrated Systems Laboratory and the Communication Technology Laboratory (CTL), ETH Zürich. From 2009 to 2012, he was a Postdoctoral Researcher with CTL, ETH Zürich and the Digital Signal Processing Group, Rice University. In 2013, he was a Research Scientist with Rice University. From 2014 to 2019, he was an Assistant Professor with Cornell University. From 2019 to 2020, he was an Associate Professor with Cornell University and with Cornell Tech, New York City. Since June 2020, he has been an Associate Professor with the Department of Information Technology and Electrical Engineering, ETH Zürich. Since 2014, he has also been an Adjunct Professor with Rice University. His research interests include the design of very-large-scale integration circuits, as well as wireless communications, signal and image

processing, optimization, and machine learning.

Dr. Studer received the ETH Medals for his M.S. and Ph.D. theses in 2006 and 2009, respectively, the Swiss National Science Foundation Fellowship for Advanced Researchers in 2011, and the U.S. National Science Foundation CAREER Award in 2017. He won a Michael Tien'72 Excellence in Teaching Award from the College of Engineering, Cornell University in 2016. He shared the Swisscom/ICTnet Innovations Award in 2010 and 2013. He was the winner of the Student Paper Contest of the 2007 Asilomar Conference on Signals, Systems, and Computers, received a Best Student Paper Award of the 2008 IEEE International Symposium on Circuits and Systems (ISCAS), and shared the Best Live Demonstration Award at IEEE ISCAS in 2013. He is currently an Associate Editor of the IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS. In 2019, he was the Technical Program Chair of the Asilomar Conference on Signals, Systems, and Computers, and a Technical Program Co-Chair of the IEEE International Workshop on Signal Processing Systems.