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Publication date:
2024-04-16

Permanent link:
https://doi.org/10.3929/ethz-b-000670157

Originally published in:
Journal of Instrumentation 19(4), https://doi.org/10.1088/1748-0221/19/04/C04032

Funding acknowledgement:
201476 - Operation, Computing and Upgrades of the CMS Experiment (SNF)

Journal of Instrumentation

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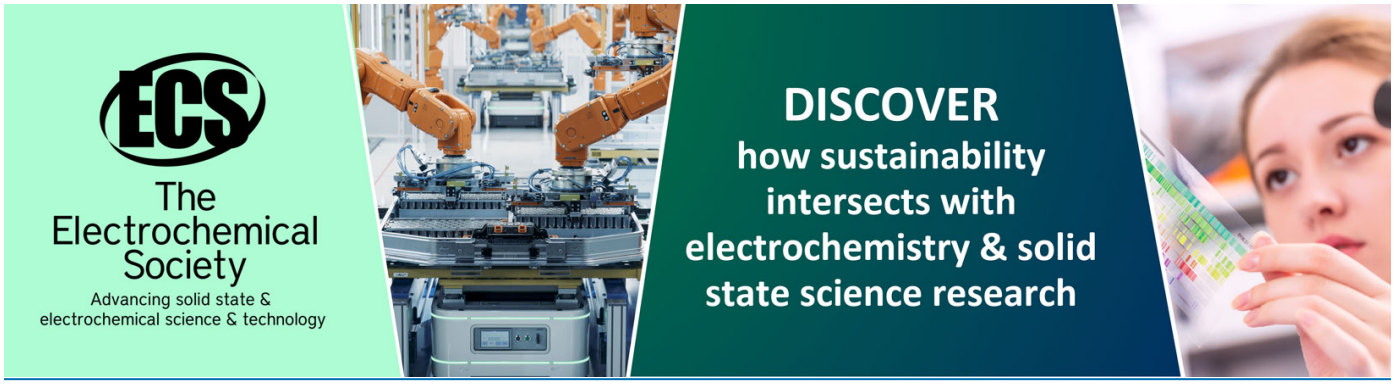

Published by IOP Publishing for Sissa Medialab

Received: *November 3, 2023*
Accepted: *February 3, 2024*
Published: *April 16, 2024*

Topical Workshop on Electronics for Particle Physics
Geremeas, Sardinia, Italy
1–6 October 2023

Universal test system for boards hosting bPOL12V DC-DC converters

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Abstract: The ECAL Barrel and MTD Barrel Timing Layer subdetectors of CMS are approaching series production of electronic boards, including voltage conditioning PCBs: LVRs and PCCs respectively. 2448 LVRs and 864 PCCs will be installed during LS3 of the LHC. These boards are hosting radiation-tolerant bPOL12V ASICs which convert a broad input voltage range into required voltage levels for microelectronics between 1.2–2.5 V. Each card must be tested multiple times at various production stages to ensure its conformity. This contribution describes a methodology of testing bPOL12V conversion quality including the detection of instability regions at certain load levels.

Keywords: Voltage distributions; Modular electronics; Radiation-hard electronics

*Corresponding author.

https://doi.org/10.1088/1748-0221/19/04/C04032

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1 Introduction

The ECAL Barrel (EB) [1] and MTD Barrel Timing Layer (BTL) [2] subdetectors of CMS [3] are currently progressing towards the mass production phase of their electronic boards, which include voltage conditioning PCBs known as LVR and PCC, respectively [4]. LVR stands for Low Voltage Regulator, while PCC stands for Power Conversion Card. A total of 2448 LVR and 864 PCC boards will be installed during the third long shutdown (LS3) of the Large Hadron Collider (LHC). These boards are equipped with radiation-tolerant bPOL12V ASICs [5, 6], designed to convert a wide input voltage range into the required voltage levels for microelectronics, ranging from 1.2 to 2.5 V. Each board undergoes multiple testing procedures at various stages of production to ensure its quality, such as:

- Factory acceptance test (FAT) — test performed at the manufacturer's facility before the application of shielding. Soldering the shielding significantly reduces the options for subsequent rework.
- Site Acceptance Test (SAT) — an essential test conducted upon the receipt of the card by the end user.
- On-demand tests — additional tests performed when specific requirements arise.

To guarantee the requested power quality, a dedicated test system was developed. Its architecture and the most compelling software components are presented in this contribution. Our objective is to share best practices derived from several years of experience with the utilization of the bPOL12V chip.

2 Test system architecture

The test system is composed of various laboratory measurement devices, controlled over a network with a dedicated piece of software. The test system architecture (figure 1) is flexible and may be easily adapted to test various PCBs equipped with bPOL12V converters. There is flexibility in choosing laboratory devices when replicating the setup. The specific setup employed for testing LVRs and PCCs consists of:

- Laboratory power supply (*R&S HMC8042*) — provides input voltage for the DUT (Device Under Test) and measures current consumption.
- Digital Multimeter (DMM) with relay board (*Keithley DAQ6510 + 7706*) — capable of measuring output voltages at rates of 1 MS/s and 200 kHz bandwidth. High acquisition rate is essential to keep track of the oscillations described in section 3.4.
- Electronic load (*Maynuo M9811*) — sufficient to fully load each channel
- Dual pole relay matrix (*Relay Pros ZADR85DPDTProXR*) — selects a channel connected to the electronic load
- A computer equipped with specialized GUI software

The test setup photo is shown in figure 2, implementations of two DUTs hosting bPOL12V DC-DC converters are presented as example in figure 3. This architectural framework can be effectively employed to evaluate any PCB based on the bPOL12V technology.

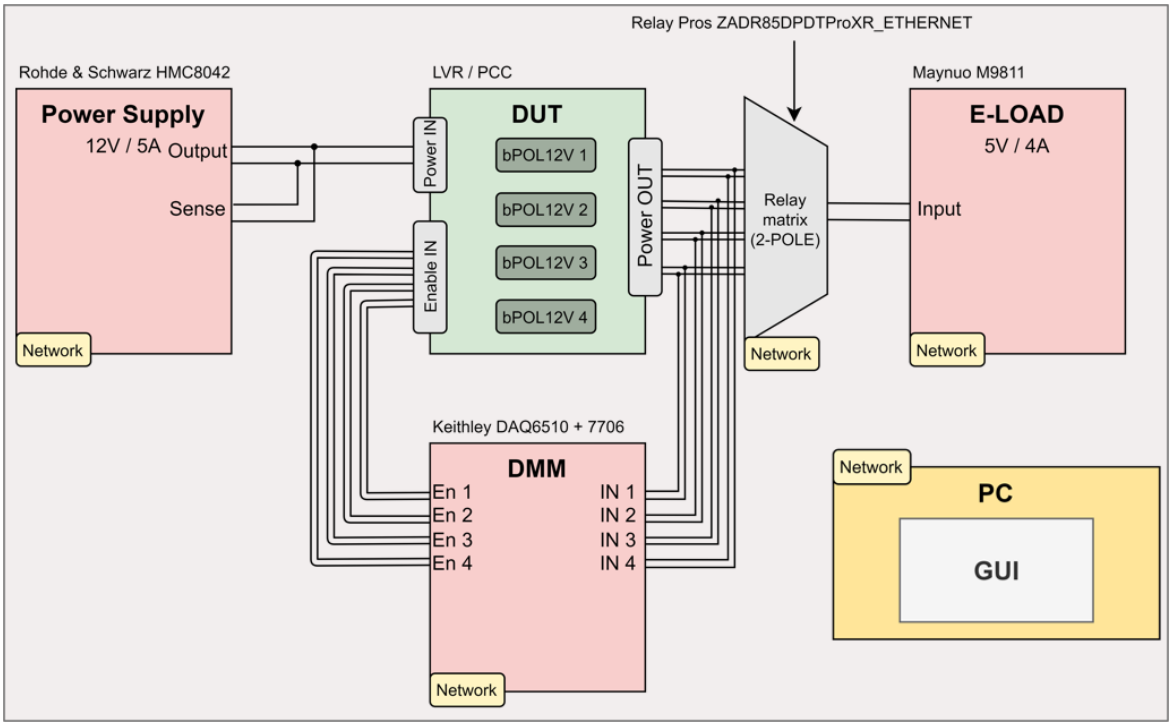

Figure 1. Architecture of the test system for PCBs hosting bPOL12V DC-DC converters.

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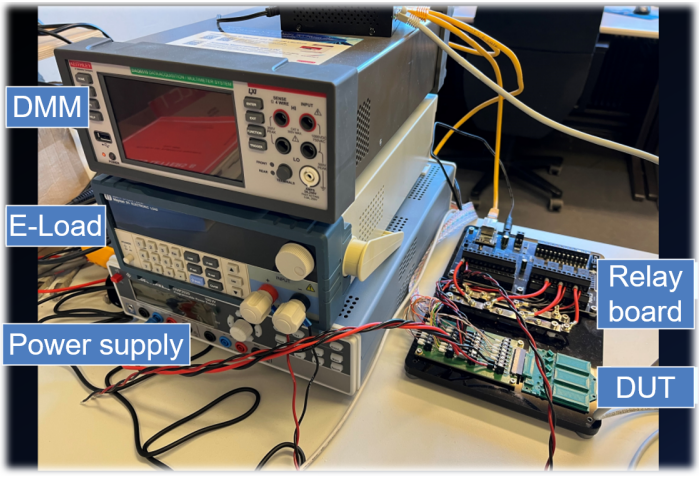

Figure 2. First version of the test system implementation used for PCCs-boards powering the MTD BTL detector. The main architecture components are labeled.

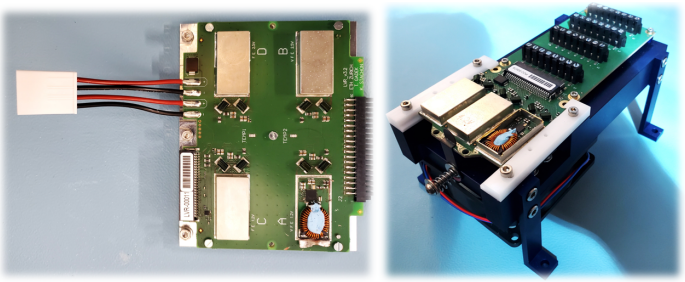

Figure 3. Example devices under test (DUT). LVR board on the left and PCC board on the right.

3 Test system software

3.1 Software components

The software was entirely made with Python 3, incorporating PyQT5 along with its capabilities in signaling and multi-threading. The test sequence is initiated in a new thread, which transmits results to a relational database in segments as soon as new data becomes available. This approach is taken to minimize the risk of data loss in scenarios like software crashes or power outages.

The state machine is designed to autonomously progress through all measurement steps as long as the safety conditions are satisfied. In the event of an error, further measurements are halted, and the setup is brought to a secure state. For example, if the input current draw exceeds the expected range, the software will deactivate the power supply. This precaution is vital for mitigating the risk of causing additional damage to a malfunctioning card, which could aid in identifying the root cause of the failure.

This software comprises a user-friendly graphical user interface (GUI), which can be employed by individuals with limited technical expertise to conduct a comprehensive examination of boards hosting DC-DC converters (as depicted in figure 4). The software supports pass/fail tests, based on a configurable validity range for each measured quantity. In the case of load-dependent efficiency curves, a template curve fitting process is employed to derive a value that is compared to the validity range. The latter concept is further elaborated upon in section 3.3.

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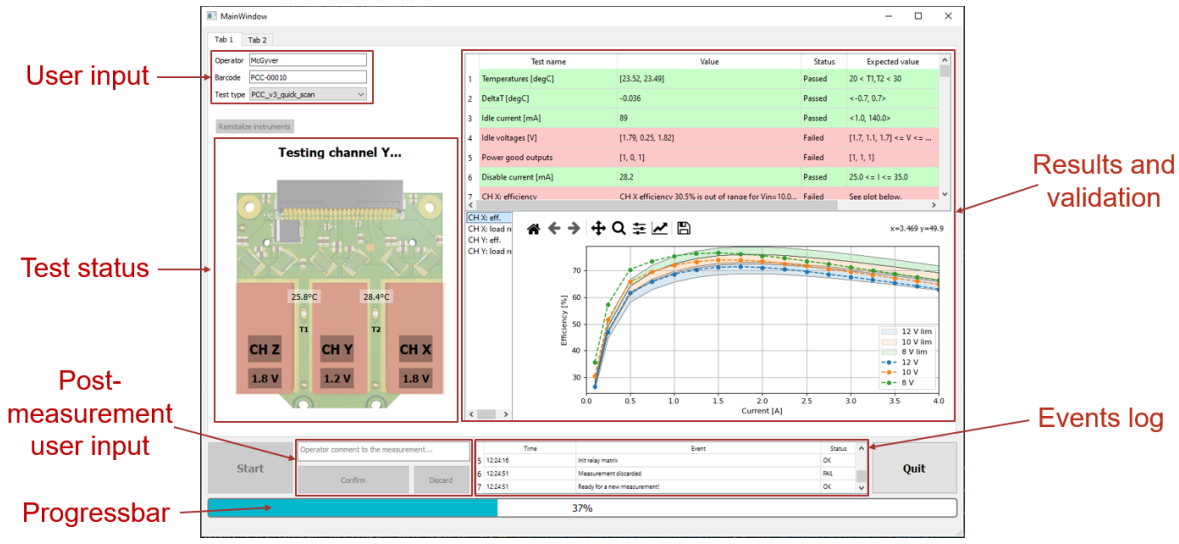

Figure 4. Main elements of a graphical user interface (GUI).

3.2 Test sequence

The test sequence consists of two main steps:

1. Quick test — This test, conducted without a load, provides a preliminary quality assessment of the PCB within a single second. The following properties are measured:
   - Idle output voltages (no load)
   - Idle input current
   - Disable input current (when all channels are disabled)
   - *Power good* outputs
   - Temperatures
2. Load test — This test involves loading each DC-DC channel, and it is usually more time-consuming, taking approximately 1 second per load point. Properties measured:
   - Output voltage
   - Input current
   - *Power good* status

3.3 Validation of efficiency curve

One of the resulting plots from the test is the efficiency versus load curve. This curve provides valuable insights as it can reveal additional power losses on the board, often stemming from production faults. To validate the curve, we have found the template fit method to be a reliable means of assessing the quality of the plot. For a sample population of 80 cards hosting 240 bPOL12V channels, we calculated a mean efficiency plot for each output voltage setting, which served as a template for

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subsequent fitting. From each curve, there is an amplitude value derived by minimizing a mean squared error (MSE) function given by formula (3.1)

$$\mathrm{MSE} = \frac{1}{n}\sum_{i=1}^{n}(y_i - \hat{y}_i)^2 \tag{3.1}$$

where n is number of points, y_i is measured value, $\hat{y}_i$ is expected value.

The amplitude parameter obtained through this optimization process is then compared to a predefined acceptance range to determine a pass/fail outcome. A family of efficiency curves for a sample of 79 converters, along with an example of a positive validation range, is shown in figure 5.

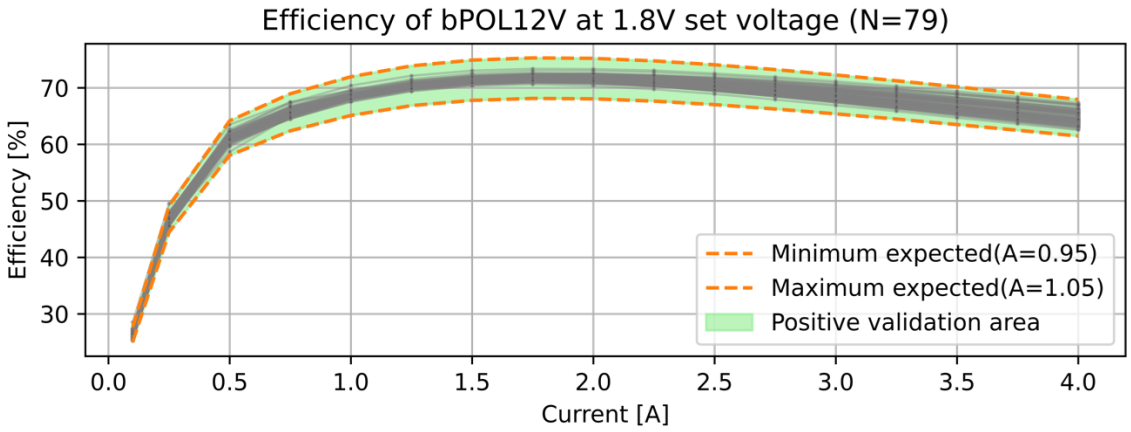

Figure 5. Efficiency plots for a sample of 79 converters (in grey). The green area is the positive validation area selected for bPOL12V working at 1.8 V output and 10 V input.

3.4 Instability region detection

We have observed that bPOL12V converters exhibit oscillating instabilities within narrow load ranges. This phenomenon impacts a sample of 22 out of the 35 channels that we examined, accounting for 62.9% of cases (see figure 6).

ID	CH A	CH B	CH C	CH D	CH E	CH F
1	OK (osc: 870-930 mA)	OK	OK	OK	OK (osc: 390-430 mA)	OK (osc: 810-890 mA)
2	OK	OK (osc: 570-630 mA)	OK	OK (osc: 380-460 mA)	OK	OK
3	OK (osc: 930-990 mA)	OK (osc: 390-450 mA)	OK (osc: 890-980 mA)	OK (osc: 380-450 mA)	OK (osc: 460-580 mA)	OK (osc: 860-920 mA)
4	OK (osc: 830-880 mA)	OK	OK (osc:960-1020 mA)	OK	OK (osc: 480-540 mA)	OK (osc: 890-970 mA)
5	OK (osc: 840-910 mA)	OK	Not working	OK	OK (osc: 540-590 mA)	OK
bPOL	OK (osc: 850-950 mA)	OK (osc: 120-370 mA)	OK	OK (osc: 0-320 mA)	OK (osc: 30-320 mA)	OK (osc: 910-990 mA)

Figure 6. Test summary of 6 PCBs hosting bPOL12V converters. Presence of instability regions is highlighted with yellow.

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These oscillations manifest as periodic sine-shaped signals, typically falling within the 10–20 kHz frequency range, with a peak-to-peak amplitude of up to 40 mV.

DMM with fast waveform acquisition is a key component to determine whether bPOL12V converter is within an unstable region. It acquires the output voltage data at a sampling rate of 100 kHz over a 20 ms period. By analyzing metrics such as the standard deviation or peak-to-peak (pk-pk) value of this waveform, we can identify the presence of oscillations at specific operational points. An illustrative comparison between stable and unstable operation is provided in figure 7.

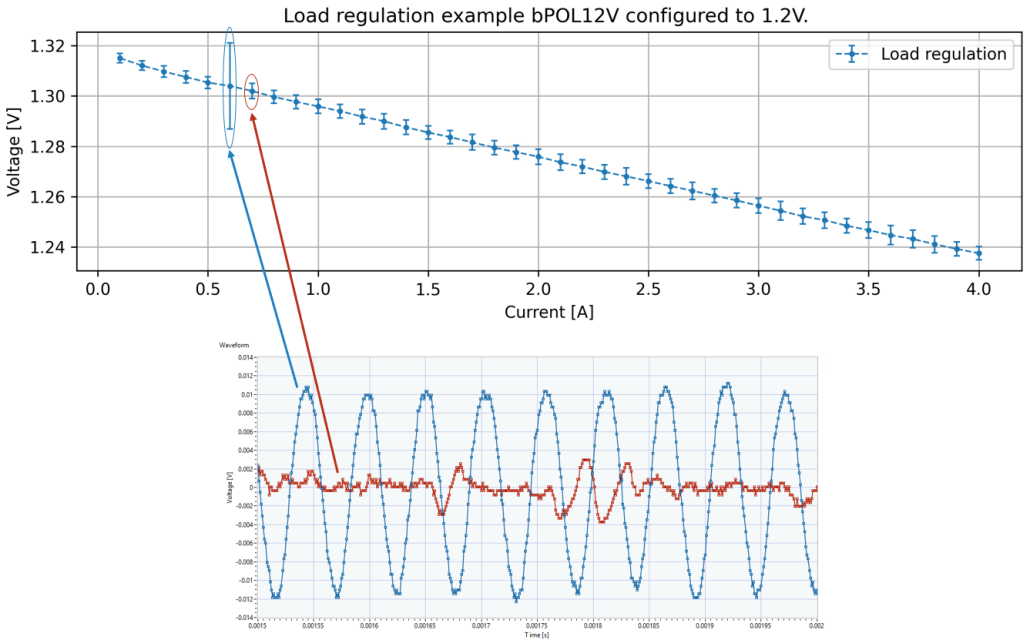

Figure 7. Load regulation plot with pk-pk error bars (top) and two waveforms corresponding to two measurement points where one of them suffers from instability.

4 Conclusions

Testing is one of the key components for providing a reliable system intended for long-term use. In our specific case, considerable efforts were dedicated to formulating test procedures and crafting sophisticated software that automates the testing process, which will serve to mitigate human errors and will preserve valuable test data about cards which will operate in particle physics machines. The test system architecture was used and validated with the final PCB prototypes: 80 PCC boards and 52 LVR boards hosting 448 conversion channels in total. This test setup will be put into operation at various stages of mass production testing, including the factory acceptance test at the PCB assembly location. The testing configuration is designed to guarantee adequate power quality, and the validation process should promptly detect any noteworthy discrepancies when compared to the reference prototypes that were tested. We strongly encourage other bPOL12V users to embark on a validation process to identify regions of instability within their power conversion systems, as this characteristic has the potential to undermine the ultimate performance of the system. Understanding the region where instabilities occur enables the avoidance of this range.

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Acknowledgments

We would like to express our deepest thanks to Michael Dröge and Christian Haller from ETH Zurich for excellent support in mechanical design, cabling of a test rack and components procurement.

Remark. This work was supported by the Swiss National Science Foundation with SNF FLARE 201476 grant.

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