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Optical absorption in silicon layers in the presence of charge inversion/accumulation or ion implantation

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We determine the optical losses in gate-induced charge accumulation/inversion layers at a Si/SiO_2 interface. Comparison between gate-induced charge layers and ion-implanted thin silicon films having an identical sheet resistance shows that optical losses can be significantly lower for gate-induced layers. For a given sheet resistance, holes produce higher optical loss than electrons. Measurements have been performed at $\lambda = 1550$ nm. [http://dx.doi.org/10.1063/1.4817255]

Small optical losses are essential for silicon photonics devices. However, for keeping *RC* time constants low and bandwidths high,[1] an increasing number of components, like high-speed electro-optic modulators[2,3] or photodetectors, require highly conductive electrodes, which in turn create high free-carrier absorption (FCA).

Even though there are several methods to increase the conductivity ($1/\rho$) of a semiconductor, so far only doping has been considered in silicon photonics. For thin conductive films, the sheet resistance $R_s = \rho/d$ is the relevant number when the film thickness d is given; the resistance of a sheet of length L and width w then is $R = R_s\, L/w$. However, while the optical loss via free-carrier absorption increases linearly with the doping level,[4] the conductivity grows less than linearly,[5] mainly because of electron-impurity scattering.[6] This confronts designers with a trade-off problem between device speed and insertion loss, properties which both are of primary technological importance.[2,7] A method for improving the conductivity of silicon structures without an undue increase of optical loss would therefore be highly desirable.

A possible solution for minimizing optical losses while maintaining a high electrical conductivity has recently been suggested.[8] In this publication the bandwidth of a silicon-based modulator has been dramatically increased by exploiting an electron accumulation layer induced by a gate voltage. The optical loss created by such an accumulation layer was very small. However, the optical loss caused by inversion/accumulation layers in silicon has not been measured systematically yet.

In this work we measure the optical absorption caused by electron and hole charge accumulation layers at a silicon/silicon dioxide interface. For equal charge carrier concentrations as a result from either impurity doping, or from free carriers, e.g., accumulated under the influence of an applied electric field, the optical losses are comparable in both cases. However, due to impurity scattering, the electrical conductivity is smaller for doped layers. Thus, for the same conductivities, the concentration of impurity-generated charges must be higher leading to a higher optical loss. By comparing our measurements with published data for doped layers, we show that the optical power attenuation coefficient for field-induced free carriers and given sheet resistance can be up to 3.5 times smaller.

The paper is organized as follows: First, we determine the optical loss in a rib waveguide when a gate voltage is applied. Second, we derive a model for describing such losses. Finally, we compare these losses to published data for ion implantation.

For determining the optical loss of conductive sheets as a function of gate fields, we record the optical transmission of rib waveguides structured on a silicon-on-insulator (SOI) wafer from Soitec, Fig. 1. We measure the transmission as a

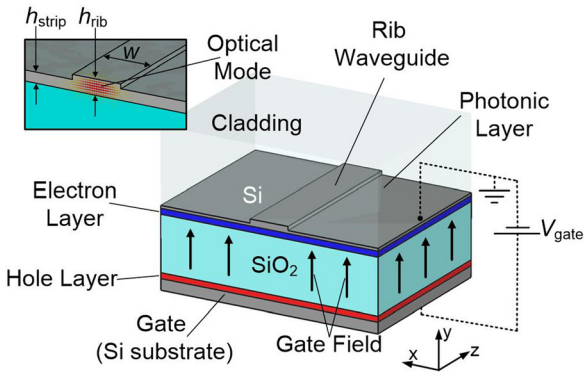

FIG. 1. Cross-section of the silicon chip used for optical loss vs. gate field measurements. The waveguide is located on top of a low-refractive index substrate (SiO_2). The optical quasi-TE_{00} mode is mainly confined in the upper lowly-doped (ideally intrinsic) silicon layer, and extends slightly into the silicon-dioxide substrate and into the 0.8 μm thick PMMA cladding. A gate voltage (V_{gate}) is applied between the silicon substrate and the grounded photonic layer. In the example shown in the picture, the gate voltage is positive, so that a hole charge layer (marked in red) is formed at the interface between gate and oxide, while an electron layer (marked in blue) is formed between the waveguide and the oxide. This electron layer reduces the sheet resistance in the photonic silicon layer, but also increases the optical losses. The rib height is $h_{rib} = 220$ nm, the strip height is $h_{strip} = 150$ nm, the rib width is $w = 700$ nm, and the silicon-oxide thickness is $d_{SiO_2} = 2\mu$m.

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function of the gate voltage V_{gate} applied to the silicon substrate (the photonic layer is electrically grounded). The fundamental quasi-TE_{00} mode of the waveguide is strongly confined to the photonic layer, Fig. 1. The mode couples to external fibers by standard gratings.[9] If the gate field across the silicon dioxide $E_{gate} = V_{gate}/d_{SiO2}$ is positive (negative), an electron (hole) layer is formed at the Si/SiO_2 boundary inside the photonic layer, Fig. 1. These charges then lower the sheet resistance of the photonic layer but will also increase the optical losses. Subsequently, we will measure and discuss these losses.

The optical transmission losses have been measured for different waveguide lengths (1, 3, and 10 mm) and the excess optical loss for free-carrier absorption have been extracted, black curve in Fig. 2. As expected, the optical loss increases for large positive or large negative gate fields. The minimum optical loss occurs at $E_{gate} = -0.018$ V/nm instead at $E_{gate} = 0$ or at a slightly positive gate field, as one would expect since silicon has a residual *p*-type doping.[9] This could be attributed to the presence of the PMMA cladding, but also residual impurities could play a role.[18]

We now compare the measured loss data in Fig. 2 as induced by applying a gate field with losses predicted due to free carrier absorption with doping. For this we follow Soref.[4,10] According to Soref the optical power attenuation coefficient at position $\vec{r}$ due to free carriers increases linearly with the concentration N_e and N_h of electrons and holes, respectively,

$$\alpha(\vec{r}) = C_e N_e(\vec{r}) + C_h N_h(\vec{r}). \tag{1}$$

In the case that the free carriers stem from impurity ionization only, the loss constants C_e and C_h in Eq. (1) have been empirically determined[4,10] at the wavelength $\lambda = 1550$ nm,

$$C_e^{(ion)} = 8.5 \times 10^{-22}\,\mathrm{m}^2, \tag{2}$$

$$C_h^{(ion)} = 6.0 \times 10^{-22}\,\mathrm{m}^2. \tag{3}$$

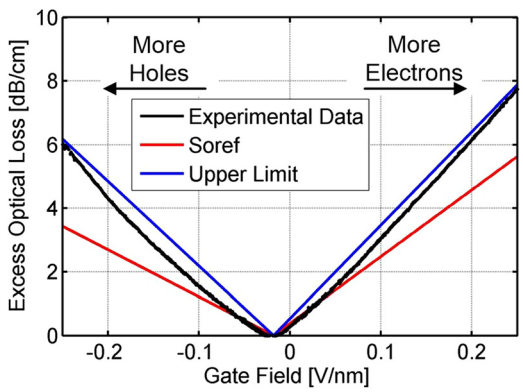

FIG. 2. Measured excess optical loss of a rib waveguide as a function of the applied gate field (black line). For large positive (negative) gate fields, an electron (hole) layer forms in the photonic layer, and the optical loss increases. The red curve shows the calculated losses according to Eqs. (1)–(3), which were empirically derived by Soref[4,10] from doping measurements. The blue curve represents our measurements in a linear worst-case approximation.

In contrast to Soref, here the free-carrier concentration in the lowly-doped (ideally intrinsic) photonic layer depends on the gate field. If charges are injected in intrinsic silicon by applying a field, different constants might apply. Because these injected carriers do not experience impurity scattering,[6] optical losses could be smaller. On the other hand, when charges are injected by a gate voltage, charge densities close to $10^{20}\,\mathrm{cm}^{-3}$ can appear in the vicinity of the Si/SiO_2 interface—a concentration regime where electron-electron scattering cannot be neglected.[6] Additionally, also the roughness of the Si/SiO_2 interface might play a role.[11] Therefore it is not clear *a priori* whether Soref's constants overestimate or underestimate the actual loss.

For calculating the waveguide attenuation coefficient α_{wg} of the quasi-TE_{00} mode using Eq. (1), we first define in a Cartesian coordinate (x, y, z)- system (Fig. 1) the electric field components in the corresponding directions denoted by $n = (1, 2, 3)$, and separate a dimensionless complex amplitude $A(z)$ from the modal field $\mathcal{E}_n(x,y)$. A monochromatic wave propagating along the z-direction with propagation constant k and an angular frequency ω is described by

$$E_n(x,y,z,t) = A(z)\mathcal{E}_n(x,y)e^{i(kz-\omega t)} + \mathrm{cc}, \tag{4}$$

$$H_n(x,y,z,t) = A(z)\mathcal{H}_n(x,y)e^{i(kz-\omega t)} + \mathrm{cc}. \tag{5}$$

In the slowly-varying amplitude approximation it can be shown[12] that the waveguide attenuation coefficient $\alpha_{wg} = -(1/|A(z)|^2)\partial|A(z)|^2/\partial z$ is given by (vacuum speed of light c, vacuum permittivity ϵ_0)

$$\alpha_{wg} = \frac{\epsilon_0 c}{\int \mathrm{d}x\mathrm{d}y(\mathcal{E}_1\mathcal{H}_2 - \mathcal{E}_2\mathcal{H}_1)} \int \mathrm{d}x\mathrm{d}y n(x,y)\alpha(x,y)(\mathcal{E}_1^2 + \mathcal{E}_2^2 - \mathcal{E}_3^2), \tag{6}$$

where $n(x,y)$ and $\alpha(x,y)$ are the local refractive index and the local attenuation coefficient Eq. (1), respectively. We notice that the last negative sign in Eq. (6) is due to the fact that if $\mathcal{E}_{1,2}(x,y)$ is chosen to be real, the quantity $\mathcal{E}_3(x,y)$ will be imaginary.

Next, we substitute Eq. (1) in Eq. (6). Since the charge distribution varies only along y, the local power attenuation coefficient $\alpha(x,y) = \alpha(y)$ does not depend on x (see coordinate system in Fig. 1). For the gate voltages considered in this work, our simulations[9] show that the electron and hole densities do not exceed $10^{20}\,\mathrm{cm}^{-3}$. This means that the variation of the silicon refractive index is less than 0.3%,[4] we therefore assume that the refractive index is constant, $n(x,y) = 3.48$. If we further assume that $\alpha(y)$ is large only in a thin silicon layer in the vicinity of the Si/SiO_2 interface at $y = 0$, the electric field $\mathcal{E}_n(x,y)$ can be considered constant with respect to y, and the integral in Eq. (6) becomes

$$\alpha_{wg} = C_{e(h)}\sigma_{e(h)}\tilde{\Gamma}, \tag{7}$$

where $C_{e(h)}$ represents the constant C_e for positive gate voltages or the constant C_h for negative voltages, and $\sigma_{e(h)} = \sigma_{e(h)}(V_{gate})$ is the corresponding two-dimensional voltage-dependent carrier density (unit m^{-2})

$$\sigma_{e(h)} = \int dy N_{e(h)}(y). \tag{8}$$

If the silicon is intrinsic and the charge layer thickness is much smaller than the oxide thickness (as in our case), the two-dimensional carrier densities for electrons and holes ($\sigma_e = \sigma$ for $V_{\text{gate}} > 0$, $\sigma_h = \sigma$ for $V_{\text{gate}} < 0$) can be approximated by

$$\sigma = \epsilon_0 \epsilon_{SiO_2} |V_{\text{gate}}| / (q d_{SiO_2}), \tag{9}$$

where $\epsilon_{SiO_2} = 3.8$ is the static relative permittivity of silicon dioxide, and q is the elementary charge.[13]

The so-called optical interaction factor $\tilde{\Gamma}$ of the waveguide (unit m^{-1}) is defined as

$$\tilde{\Gamma} = \epsilon_0 c n_{\text{Si}} \frac{\int dx (\mathcal{E}_1^2 + \mathcal{E}_2^2 - \mathcal{E}_3^2)|_{y=0^+}}{\int dx dy (\mathcal{E}_1 \mathcal{H}_2 - \mathcal{E}_2 \mathcal{H}_1)}. \tag{10}$$

For evaluating the interaction factor, we perform a numerical integration of the mode field. To this end, the optical mode is computed with commercially available software,[14] and we find $\tilde{\Gamma} = 2.63\,\mu m^{-1}$.

Using the constants $C_{e(h)}^{(\text{ion})}$ determined by Soref, Eqs. (2) and (3), we obtain the red curve in Fig. 2, which was shifted by the experimentally observed offset −0.018 V/nm as discussed before. The constants as used by Soref therefore underestimate the actual optical loss in the inversion/accumulation layer. If Soref's model should be applied nonetheless, its constants must be adjusted. In Fig. 2 the blue straight lines are a better approximation to the measurements and represent an upper loss limit. The corresponding loss constants are

$$C_e^{(\text{upper})} = 1.4\, C_e^{(\text{ion})}, \tag{11}$$

$$C_h^{(\text{upper})} = 1.8\, C_h^{(\text{ion})}. \tag{12}$$

We therefore conclude that optical loss due to an inversion/accumulation layer can be empirically described by Eq. (1) only if the coefficients $C_{e(h)}$ become field-dependent. For gate fields in the range from −0.25 V/nm to 0.25 V/nm, we find that the coefficients $C_{e(h)}$ lie between the values determined by Soref, Eqs. (2) and (3), and those given in Eqs. (11) and (12).

The assumption made in deriving Eqs. (7)–(9), namely, that the charge layer is infinitesimally thin, is true only approximately. However, numerical simulations based on industry's standard software ATLAS show that more than 50% of the total charge in intrinsic silicon is located within the first 5 nm from the interface(gate fields larger than 0.1 V/nm or smaller than −0.1 V/nm). If in this range of gate fields we replace the simulated charge distribution by a delta-shaped distribution as is assumed in Eq. (9), the calculated waveguide attenuation coefficient would differ by less than 5%, so we adopt the simpler approach Eqs. (7) to (9).

Now that we have measured the losses for a given gate field, we are also interested in the sheet conductance for a given gate field. Although several models exist for calculating the sheet resistance of accumulation/inversion layers in silicon,[11,15] we feel the need to measure this quantity for a sample belonging to the same SOI wafer as used for the optical loss measurements. To this end, a 2 mm × 2 mm square has been etched into a 220 nm thick photonic layer. The chip has been placed in a high-vacuum chamber for avoiding contamination of the surface, and to reduce the risk of electrical breakdown.[9] The resistance is measured by a standard four-point procedure,[16] the result of which is shown in Fig. 3. For the highest gate field, $E_{\text{gate}} = 0.25$ V/nm, we measure a sheet resistance of 2.91 kΩ/sq. This value corresponds, using Eq. (9), to an effective electron mobility $\mu_{e,\text{eff}} = 1 / (q\sigma R_s) = 394\ \text{cm}^2/\text{V/s}$, a factor 3.63 smaller than the intrinsic electron mobility $\mu_e = 1430\ \text{cm}^2/\text{V/s}$. For the gate field $E_{\text{gate}} = -0.25$ V/nm, we obtain a sheet resistance of 10.8 kΩ/sq. We observe that the sheet resistance in inversion/accumulation layers on thermally oxidized silicon (as in our SOI) is a sensitive function of surface roughness and Coulomb scattering with fixed oxide charges.[11] Effective mobilities larger than the one we found are possible,[11] leading to potentially higher sheet conductances and lower optical losses for the same gate fields.

Finally, we compare optical losses of gate induced sheet layers with losses of ion-implanted layers for a given sheet resistance by using published data on conductivity and optical loss in doped silicon.

In order to get rid of any influence from the waveguide geometry (see interaction factor in Eq. (6)), we investigate an optical mode propagating along a doped silicon slab having a thickness d in a lossless background material with the same (real) refractive index $n_{\text{Si}} = 3.48$ as silicon. The optical mode is assumed to have dimensions much larger than the slab thickness d, Fig. 4(a).

We start looking at the attenuation coefficient $\alpha_{e(h)}(d, R_s)$ in n-doped (p-doped) silicon slabs of thickness d with a sheet resistance $R_{s,e(h)}$. The sheet resistance $R_{s,e(h)} = (q\mu_{e(h)} N_{e(h)} d)^{-1}$ depends on the electron (hole) mobility $\mu_{e(h)}$, the electron (hole) density $N_{e(h)}$ and the slab

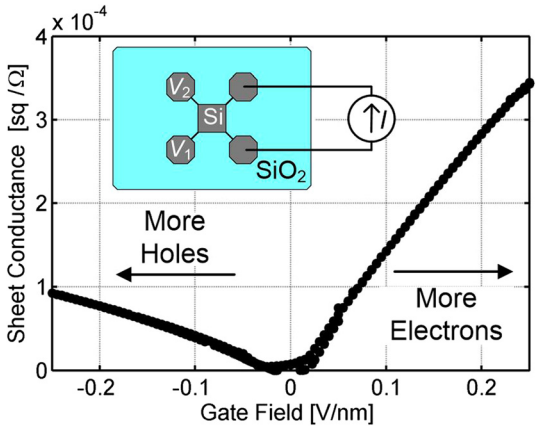

FIG. 3. Sheet conductance (inverse of sheet resistance) vs. gate field. The sample used consists of a 220 nm thick silicon belonging to an SOI wafer identical to the one used for the optical loss measurements. The measurements were performed in vacuum. The 2 mm × 2 mm silicon square as used for the four-point measurement is shown in the inset (the octagons are used for contacting the chip and connect the vertices of the square with 50 μm wide silicon strips). A current I is forced to flow across two adjacent vertices and the voltages V_1 and V_2 are measured on the other vertices. The sheet resistance is calculated as $R_s = 4.5324(V_2 - V_1)/I$.[16]

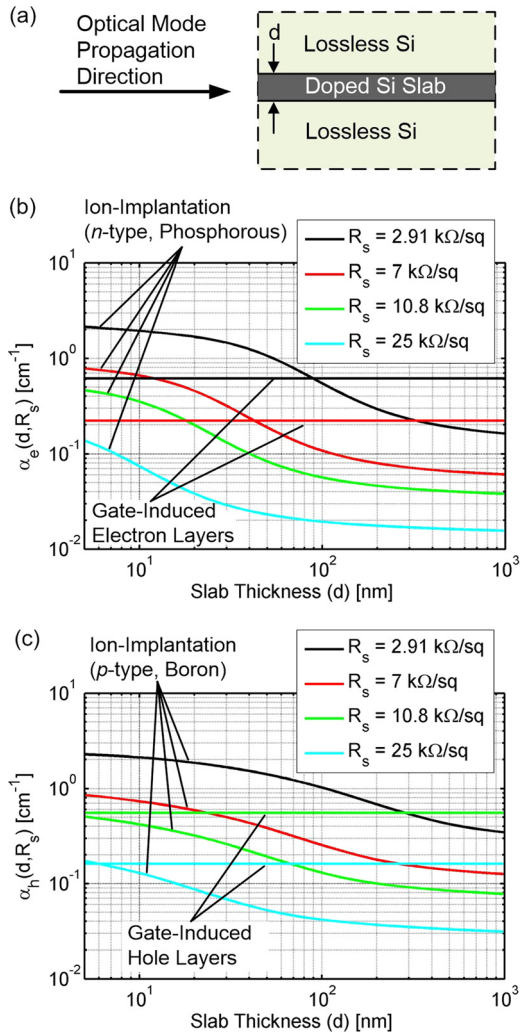

FIG. 4. Optical power attenuation coefficient of a mode (a) propagating along a silicon slab vs. slab thickness for a constant sheet resistance R_s, (b) for *n*-doping and an electron gate-induced layer and (c) for *p*-doping or gate-induced hole layers. The differently coloured lines represent different sheet resistances (legend) of the slab waveguide. If the carrier mobility in silicon would not depend on the doping levels, the curves for ion-implantation would be constant lines. The sheet resistance of gate-induced layers does not depend on the thickness of the silicon slab. For electrons, smaller optical losses can be obtained with gate-induced charge layers, especially for small thicknesses.

thickness d. From tabulated data[17] we extract the required ion concentration (for both n and p impurity types) for a given sheet resistance. We then assume that the ion concentration equals the free-carrier density $N_{e(h)}$ (100% impurity ionization, see supplementary material).[9,19,20] The attenuation coefficient $\alpha_{e(h)}(d, R_s)$ is then given by Eq. (7). Since the interaction factor $\tilde{\Gamma}$ depends from the particular optical mode, we set here arbitrarily $\tilde{\Gamma} = 1\,\mu\text{m}^{-1}$. It is found that the losses depend on the sheet thickness d, Figs. 4(b) and 4(c). This is because high impurity concentrations in silicon degrade the carrier mobility. For example, if the slab thickness is decreased, by a factor of ten, the ion concentration must be increased by more than a factor of ten for keeping the same sheet resistance R_s. And in fact, a sheet resistance of, e.g., 3 kΩ/sq can be obtained in a 1000 nm thick slab with an n-type ion concentration of $1.84 \times 10^{16}\,\text{cm}^{-3}$, as well as with a concentration of $6.03 \times 10^{17}\,\text{cm}^{-3}$ (32 times larger) in a 100 nm thick slab, or a concentration of $2.2 \times 10^{19}\,\text{cm}^{-3}$ (an additional factor 36 larger) in a 10 nm thick slab. For an ion concentration of $2.2 \times 10^{19}\,\text{cm}^{-3}$, the electron mobility has decreased by a factor 15 of its intrinsic value $\mu_e = 1430$ $\text{cm}^2/\text{V/s}$.

In the limit of large slab thickness, the attenuation coefficient $\alpha_{e(h)}(d, R_s)$ converges to a finite limit which depends on the electron (hole) intrinsic mobility ($\mu_e = 1430$ $\text{cm}^2/\text{V/s}$ and $\mu_h = 495$ $\text{cm}^2/\text{V/s}$) as well as on the loss constants Eqs. (2) and (3). We denote this limit with $\alpha_{e(h)}(\infty, R_s)$. The ratio $\alpha_h(\infty, R_s)/\alpha_e(\infty, R_s)$, equals

$$\alpha_h(\infty, R_s)/\alpha_e(\infty, R_s) = C_h^{(\text{ion})}/C_e^{(\text{ion})} \times \mu_e/\mu_h = 2.04. \quad (13)$$

Since this value is larger than one, we recover the well-known result that for moderate doping levels and a fixed sheet resistance holes produce more optical loss than electrons.

Next, we derive the attenuation coefficient $\alpha_{e(h)}(d, R_s)$ in the case of a gate-induced conductive sheet with a sheet resistance R_s. Since accumulation and inversion layers are a few nanometers thick only, the optical losses for layers thicker than, e.g., 5 nm must be independent of the slab thickness. For a given sheet resistance we derive the required gate voltage from the experimental data plotted in Fig. 3. The gate field in turn determines the optical losses according to the data in Fig. 1. The results are plotted in Figs. 4(b) and 4(c). We see that optical losses are independent of the slab thickness as stated above. Additionally, according to Fig. 4, holes produce more optical loss than electrons as is the case for ion implantation. But most importantly, one may observe that for thin slabs and for the same sheet resistance smaller optical loss can be obtained by injecting electrons with a gate voltage instead of using ion implantation.

In conclusion, we have measured the optical loss of inversion/accumulation layers in silicon, and loss coefficients have been determined. We find that the optical losses of thin sheet layers are smaller when the resistance is reduced by an inversion/accumulation layers rather than by doping silicon slabs.

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