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Optimal Design of the Modular Multilevel Converter for an Energy Storage System Based on Split Batteries

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Abstract

This paper presents the optimal design of a modular multilevel converter (MMC) for use in a stand-alone high power energy storage system based on split batteries (sBESS). The MMC allows for the sBESS to connect directly to the medium-voltage grid without the need for a line-transformer. A free parameter variation is performed to compare designs with different numbers of modules and different power semiconductors. Many commercially available IGBTs were found to be overdimensioned for the 5 MW, 20 kV target system, and better results were obtained with optimized assemblies. When the converter is designed with just a few more modules than absolutely necessary, the total size of the passive components can be reduced drastically, while the power losses increase only marginally. An attractive candidate system is given a closer look, for which a peak power-conversion efficiency of 99.3 % is predicted (not including power losses in the line-filter and in the dc-dc converters to interface the batteries).

1 Introduction

With the increasing share of electrical power from renewable sources, investments in a stronger national grid may become necessary to level out differences in local power-infeed across the country [1]. Battery energy storage systems can help to reduce this effort by buffering the energy in the region where the power fluctuations occur [2]. To allow for a high power output per deployed unit, these systems need to connect directly to the medium voltage distribution grid.

State-of-the-art solutions are based on conventional multilevel power converters that have a limited output voltage and therefore require bulky line-transformers to connect to the medium-voltage grid. Going to a higher number of voltage levels (and thus a higher output voltage) would come at the cost of a gradually increasing complexity.

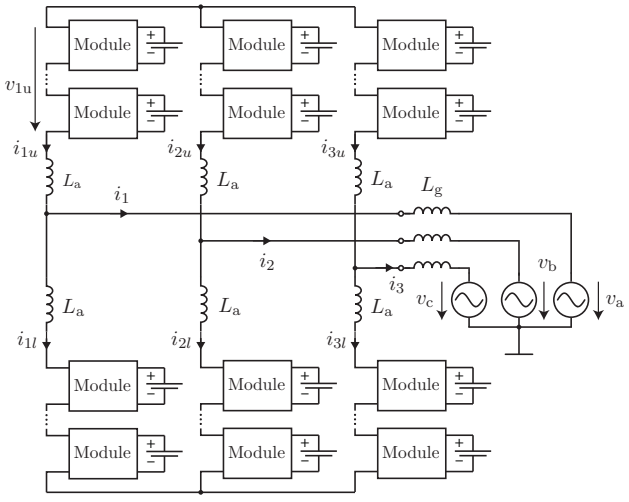

Fig. 1: Simplified circuit diagram of an energy storage system based on split batteries (sBESS). Each module has a battery attached to it.

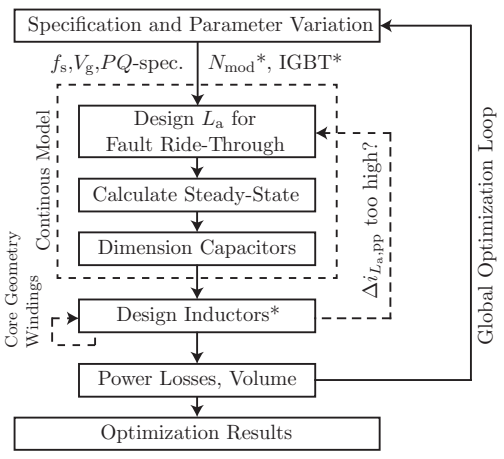

Fig. 2: Global optimization procedure: Parameters marked with an asterisk (*) are the *free* parameters of the optimization.

Parameter		Value
Nominal Grid Voltage	V_g	20 kV
Nominal Grid Power	P_out	5 MW
Reactive Power	Q_out	$\pm 5\% P_\mathrm{out}$
Battery Storage Capacity	W_tot	5 MWh

Tab. I: Specification of the presented sBESS.

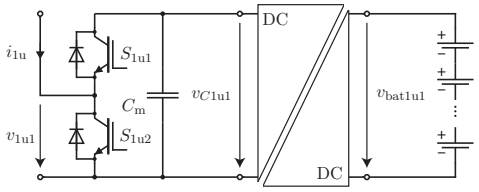

Fig. 3: Basic circuit diagram of a module.

In contrast to that, the modular multilevel converter [3] presents a new approach, which allows for the realization of a high number of output voltage levels by connecting multiple identical power electronic modules in series. Additional modules can easily be added to the design to provide redundancy, which increases the reliability of the entire system. The high number of output voltage levels makes for an excellent output current quality at minimal filtering effort and allows the converter to be deployed in the medium-voltage distribution grid without the need for a line transformer.

In [4], it is has been proposed to use the MMC converter for ultra-fast charging of electric vehicles and [5] describes an MMC converter based on H-bridge cells as a stand-alone high-power battery energy storage systems based on split batteries (sBESS). In [6] an MMC converter is proposed as a grid-tie inverter with integrated split battery storage capability, but no comprehensive design methodology has been given.

This paper presents an optimal design procedure for the MMC converter used in a high-power sBESS. In contrast to [4] and [5], the system can operate without a dc-link or a dc-link capacitor, which makes the control structure different to that of the classical MMC.

Section 2 gives a brief summary of the operating principles of the system and introduces common terminology. **Section 4** presents the derivation of the continuous model on which the design of the passive components in **Section 5** is based. An optimization procedure is proposed in **Section 3**, that leads to a pareto-optimal design of the MMC converter concerning size of the passive components and power conversion efficiency. The procedure is outlined in Fig. 2. In **Section 6**, this method is applied to the specification from Tab. I and the results are interpreted. Finally, a conclusion is drawn in **Section 7**, which discusses the performance of the presented approach in general.

2 Operating Principles

The main component of the battery energy storage system in question is a modular multilevel converter (MMC) [3]. Fig. 1 shows its basic circuit diagram. Due to the inherent symmetry of the system, all considerations in this paper are made for the first leg, the upper arm within the first leg or the first module within the upper arm of the first leg, wherever possible, to prevent the excessive use of index variables.

A bidirectional dc-dc converter in each module decouples the power flowing in and out of the module from the charging process of the batteries, to maximize their lifespan. When the dc-dc converters are isolated (as shown in Fig. 3), the housing of the batteries can be grounded at the cost of a high isolation effort in the high-frequency transformers. Otherwise, the split batteries are on the same floating potential as the modules themselves and have to be isolated as a whole.

Under typical operating conditions, great care is taken to ensure that the voltages of all submodules within an arm are approximately equal (i.e. $v_{C1u1} = v_{C1u2} = \ldots = v_{C1uN}$). This is achieved with the common sorting algorithm discussed in [7]. Consequently, the arm voltage can be expressed as a controlled voltage source with $N+1$ discrete output voltage levels. The *internal arm voltage* corresponds to the maximum voltage that an arm can output when all its modules are inserted:

$$v_{1\mathrm{u,int}} = \sum_{n=1}^{N} v_{C1un}. \tag{1}$$

By appropriately making use of pulse-width modulation, the short-term average of the arm voltage v_{1u} can in a first approximation be controlled accurately to an arbitrary value between 0 V and $v_{1\mathrm{u,int}}$. Thus, it is common to regard v_{1u} as continuous [8], which is adopted in the following investigations.

3 Global Optimization Procedure

For a given specification, differ designs of the modular multilevel converter are possible. The algorithm depicted in Fig. 2 combines the individual design steps into a global optimization procedure to visualize the trade-off between minimizing the volume of the passive components and minimizing the power losses. The global loop of the optimization procedure iterates through all semiconductors in question and all possible numbers of modules. The minimum number of modules N_{min} is dependent on the voltage handling capability of each semiconductor; the maximum number of modules has been limited to around $1.5N_{\mathrm{min}}$. Increasing the number of modules even further produces a marginal reduction in the volume of the passive components but entails high power losses.

In every iteration of the outer loop, a converter is designed by the procedure described below. In a final step the results are compared as discussed in section 6.

3.1 Design Steps

The design phase begins with the calculation of the arm inductance necessary to limit the current in case of fault. This is described in section 5.2. Together with the specification given in Tab. I, this allows for the calculation of the arm voltages and the arm currents as discussed in section 4. Based on that, the capacitors are dimensioned as shown in section 5.1, and the internal arm voltage fluctuation is determined. In a subsequent step, the so obtained results are used to generate the PWM-waveforms of each individual arm voltage through phase opposition disposition (POD) carrier-based pulse-width modulation. The current ripple on the output is then calculated by inserting the so obtained waveforms into (2) – (9) and solving the system of equations in the Fourier domain. Should the current ripple exceed the specified maximum, then the arm inductance is recalculated and the above procedure is repeated.

The arm currents at full load (together with the maximum current in the arms in case of fault) and the value of the arm inductances form the design specification for the arm inductances. As described in section 5.2, their design presents a multi-objective optimization itself, which is solved by an inner optimization loop.

Notice how the variation of the switching frequency is not part of the optimization loop in Fig. 2. Under the assumption of perfect balancing, the switching frequency does not have any influence on the size of the capacitors, which are by far the largest passive components in the system. The influence on the arm inductances is also negligible, as their size is already determined by the rate of rise of the fault current, as discussed in section 5.2.

At low switching frequencies however, the assumption that the PWM voltage is quasi-continuous is violated. While the sorting algorithm was found to successfully balance at lower switching frequencies, the differences between the individual module voltages become noticeable. Both phenomena introduce distortion to the actual arm voltages which cannot be mitigated with the classical linear control approaches and which were found to lead to low-frequency harmonics on the output currents and the circulating currents. Thus, the switching frequency per module has been set to 250 Hz, where time-domain simulation indicate that this effect is not severe.

4 Steady-State Model

The battery energy storage system is required to provide both positive and negative active and reactive power according to the specification given in Tab. I.

It is the goal of the steady-state model to calculate the currents and voltages relevant to the design of the individual components of the converter. This includes the a priori unknown control commands for the arm voltages $v_{1\mathrm{u}}$, $v_{1\mathrm{l}}$, $v_{2\mathrm{u}}$, $v_{2\mathrm{l}}$, $v_{3\mathrm{u}}$ and $v_{3\mathrm{l}}$.

For the sake of clarity, this is done from ground up with the help of the circuit shown in Fig. 1. Similar calculations are shown in e.g. [9], [8] and [10] for the case that a dc-link is present. At first, the control variables are decoupled and afterwards, the ideal control commands for the arm voltages are determined given the momentary complex power demand $\underline{S}$ at the converter terminals.

4.1 Decoupling of the Control Variables

By applying Kirchhoff's Current Law and Kirchhoff's Voltage Law, the relationship between the arm currents and the arm voltages is derived. The explicit dependence on the time t as in $v_{1\mathrm{u}}(t)$ is omitted for the sake of readability:

$$v_{1u} + L_a \frac{di_{1u}}{dt} + L_g \frac{di_1}{dt} + v_a - v_b - L_a \frac{di_{2u}}{dt} - v_{2u} - L_g \frac{di_2}{dt} = 0 \tag{2}$$

$$v_{1l} + L_a \frac{di_{1l}}{dt} - v_{2l} - L_a \frac{di_{2l}}{dt} + L_a \frac{di_2}{dt} + \frac{di_2}{dt} + v_b - v_a - L_g \frac{di_1}{dt} = 0 \tag{3}$$

$$v_{2u} + L_a \frac{di_{2u}}{dt} + L_g \frac{di_2}{dt} + v_b - v_c - L_g \frac{di_3}{dt} - L_a \frac{di_{3u}}{dt} - v_{3u} = 0 \tag{4}$$

$$v_{2l} + L_a \frac{di_{2l}}{dt} - v_{3l} - L_a \frac{di_{3u}}{dt} + L_g \frac{di_3}{dt} + v_c - v_b - L_g \frac{di_2}{dt} = 0 \tag{5}$$

$$v_a + v_b + v_c = 0 \tag{6}$$

$$i_{1l} + i_{2l} + i_{3l} = 0 \tag{7}$$

$$i_{1l} + i_{2l} + i_{3l} = 0 \tag{8}$$

$$i_1 + i_2 + i_3 = 0 \tag{9}$$

The currents of a single leg are commonly represented by a part i_1, which flows through the grid, and a superimposed part i_b, which only circulates through the arms [8].

$$i_1 = i_{1u} - i_{1l} \tag{10}$$

$$i_b = \frac{i_{1u} + i_{1l}}{2} \tag{11}$$

Each arm voltage is composed of a dc-offset $\frac{V_{dc}}{2}$, a part $v_{1,line}$ and a part $v_{1,circ}$:

$$v_{1u} = \frac{V_{dc}}{2} - v_{1,line} + \frac{v_{1,circ}}{2} \tag{12}$$

$$v_{1l} = \frac{V_{dc}}{2} + v_{1,line} + \frac{v_{1,circ}}{2} \tag{13}$$

After a lengthy derivation, it is revealed that $v_{1,line}$ only has an influence on the line currents, and that $v_{1,circ}$ only has an influence on the circulating currents:

$$\frac{di_1}{dt} = \frac{2}{3} \frac{v_{1,line} - v_a - \frac{v_{2,line} - v_b + v_{3,line} - v_c}{2}}{L_g + \frac{L_a}{2}} \tag{14}$$

$$\frac{di_{1b}}{dt} = -\frac{1}{3} \frac{v_{1,circ} - \frac{v_{2,circ} + v_{3,circ}}{2}}{L_a} \tag{15}$$

The circulating currents may be decoupled with the following transformation:

$$v_{\alpha,circ} = \frac{2}{3} \left(v_{1,circ} - \frac{v_{2,circ} + v_{3,circ}}{2} \right) \tag{16}$$

$$v_{\beta,circ} = \frac{2}{3} \left(v_{1,circ} - \frac{v_{2,circ} + v_{3,circ}}{2} \right) \tag{17}$$

$$0 = (v_{1,circ} + v_{2,circ} + v_{3,circ}) \tag{18}$$

This is convenient, as the controller can now directly influence the actual circulating currents, and only the inversion of (16) – (18) is required in the implementation.

$$\frac{di_{1b}}{dt} = -\frac{v_{\alpha,circ}}{2L_a} \tag{19}$$

$$\frac{di_{2b}}{dt} = -\frac{v_{\beta,circ}}{2L_a} \tag{20}$$

The same can be done for the line currents:

$$\frac{di_1}{dt} = \frac{v_{\alpha,line} - v_a}{L_g + \frac{L_a}{2}} \tag{21}$$

$$\frac{di_2}{dt} = \frac{v_{\beta,line} - v_b}{L_g + \frac{L_a}{2}} \tag{22}$$

Please note, that while this simplifies the derivation of the ideal control commands shown in the next section, it is more common to transform (14) and the respective equations for i_2 and i_3 into dq-coordinates, where the control-structure becomes similar to that of any other typical three phase voltage source converter.

4.2 Steady-State Arm Voltages

Once, the circulating currents and the line currents are decoupled, they can be controlled with the help of common linear control theory as shown for the classical MMC converter in e.g. [7]. In steady-state, the required ideal control command $\underline{V}_{\alpha,\text{line}}$ to drive the appropriate line current

$$I_1 = \left| \frac{\underline{S}}{3\underline{V}_\text{g}} \right| \tag{23}$$

can directly be calculated from (21) using phasor arithmetics (w.l.o.g., it is assumed that $\angle \underline{I}_1 = 0°$):

$$\underline{V}_{\alpha,\text{line}} = I_1 \cdot \left(\frac{\underline{Z}_\text{a}}{2} + \underline{Z}_\text{g} \right) + \underline{V}_\text{a} \tag{24}$$

In the presented sBESS system, the active power delivered to the grid is obtained solely from the modules themselves. Therefore, no circulating current is needed during normal operation and it follows from (19), that ideally

$$\underline{V}_{\alpha,\text{circ}} = 0. \tag{25}$$

The control-reserve needed to ensure that the circulating current stays zero is negligible compared to the magnitude of $\underline{V}_{\alpha,\text{line}}$, which is according to (24) nearly the same as the line-voltage. Consequently, the reference values for the arm voltages in steady-state are in a good approximation determined by

$$v_{1\text{u}}(t) = \frac{V_\text{dc}}{2} - \hat{V}_\alpha \cdot \cos(2\pi f t + \varphi_\alpha), \tag{26}$$

$$v_{1\text{l}}(t) = \frac{V_\text{dc}}{2} + \hat{V}_\alpha \cdot \cos(2\pi f t + \varphi_\alpha), \tag{27}$$

where f is the grid frequency and

$$\hat{V}_\alpha = \sqrt{2} \left| I_1 \cdot \left(\frac{\underline{Z}_\text{a}}{2} + \underline{Z}_\text{g} \right) + \underline{V}_\text{a} \right|, \tag{28}$$

$$\varphi_\alpha = \angle \left(I_1 \cdot \left(\frac{\underline{Z}_\text{a}}{2} + \underline{Z}_\text{g} \right) + \underline{V}_\text{a} \right). \tag{29}$$

As the arm voltage reference may not be negative, V_dc is chosen as

$$V_\text{dc} = 2\hat{V}_\alpha \cdot 1.15, \tag{30}$$

including a voltage reserve of 15 % for dynamic control.

5 Design of the Passive Components

Now that the currents and voltages are known, the passive components can be designed.

In the following, the module capacitances are designed to keep the internal arm voltage fluctuation within the limits of safe operation. Afterwards, the arm inductances are designed so that the output current ripple is limited to a maximum of 10 % of the rated output current and that the overcurrent in case of a grid-side fault is limited to 150 % of the rated current. A description of how the actual components are realized and how the power losses are calculated is given at the end of each following subsection.

5.1 Dimensioning of the Module Capacitances

The steady-state analysis reveals, that the total instantaneous power feed *into* an arm is not constant over time [11]. For the MMC converter without a dc-link, this can be written as

$$p_{1\text{u}}(t) = \frac{\sqrt{2} I_1}{2} \cos(2\pi f t) \left(\frac{V_\text{dc}}{2} - \hat{V}_\alpha \cos(2\pi f t + \varphi_\alpha) \right) + N P_\text{bat}. \tag{31}$$

When all batteries provide power at the same constant rate

$$P_\text{bat} = \frac{1}{N} \frac{\sqrt{2} I_1}{2} \frac{\hat{V}_\alpha}{2} \cos(\varphi_\alpha), \tag{32}$$

then the net energy transfer is zero after on line period for each arm. However, the arm capacitances still have to provide the difference in instantaneous power. The balancing algorithm ensures that the voltages of all capacitors stay within a tight margin. Consequently, every capacitor is on average subject to the same energy fluctuation, which is calculated by integrating the instantaneous arm power:

$$w_{C1u1}(t) = \int_0^t \frac{p_{1u(t')}}{N} \mathrm{d}t' = \sqrt{2} I_1 \frac{V_{dc} \sin(2\pi f t) - \frac{\hat{V}_\alpha}{2} \sin(4\pi f t + \varphi_\alpha)}{8\pi f N} + C_W \tag{33}$$

The peak-to-peak value

$$\Delta w_{C1u} = N \Delta w_{C1u1} = {}_{pp} \left\{ \int_0^t p_{1u(t')} \, \mathrm{d}t' \right\} \tag{34}$$

describes the difference between the minimum (W_0) and the the maximum energy ($W_0 + \Delta w_{C1u}$) stored in all N capacitors in one arm together during one mains period. Both values are directly related to the minimum and the maximum internal arm voltage [8]:

$$W_0 = \frac{1}{2} C_m \frac{(v_{1u,int,min})^2}{N} \tag{35}$$

$$W_0 + \Delta w_{C1u1} = \frac{1}{2} C_m \frac{(v_{1u,int,max})^2}{N} \tag{36}$$

For the converter to operate safely, two important criteria have to be met, which put an upper limit and a lower limit on this fluctuation: First, the maximum voltage v_{max} of a single capacitor may not exceed a critical value v_{crit}, which is typically limited by the employed power semiconductors. Assuming all module capacitors share virtually the same voltage, this translates to

$$v_{1u,int,max} \leq N \cdot v_{crit} \tag{37}$$

Second, the internal arm voltage may never fall below the reference value for the PWM. A sufficient condition for this to be fulfilled is to require the internal arm voltage to always be higher than the maximum allowed value of the arm voltage which according to (26) and (27) is V_{dc}:

$$v_{1u,int,min} \geq V_{dc} \tag{38}$$

It follows directly from (35) and (36) that the minimum required value for the capacitance is

$$C_m \geq \frac{2\Delta w_{C1u1}}{v_{crit}^2 - \left(\frac{V_{dc}}{N}\right)^2}. \tag{39}$$

According to (37), the minimum number of modules allowed is

$$N_{min} = \lceil n_{min} \rceil := \left\lceil \frac{V_{dc}}{v_{crit}} \right\rceil, \tag{40}$$

where $\lceil x \rceil$ denotes the ceiling operator applied to x. Since the energy fluctuation is dependent on the operating point, (39) can be evaluated in the whole operating area to find the determining "worst case" Δw_{C1u1}. The overall energy storage capability of all six arms is an excellent measure for the size of the module capacitors:

$$W_{C,tot} = 6 \frac{\Delta w_{C1u}}{(1 - \frac{1}{\lambda})^2} \tag{41}$$

The introduced overdimensioning factor λ describes the voltage fluctuation in the capacitors, independent of the actual number of modules or the actual semiconductor blocking voltage.

$$\lambda = \frac{v_{crit}}{V_{dc}/N} = \frac{N}{n_{min}} \tag{42}$$

When the maximum permissible module voltage is close to the minimum required module voltage, λ approaches one and the size of the capacitors tends to infinity. In other words: for a chosen semiconductor, the overall size of the module capacitors gets large when the number of modules in the system is close to its theoretical minimum of n_{min}. In this analysis, the critical module voltage has been set to 60 % of the breakdown voltage for all power semiconductors with blocking voltages above 1.7 kV, and 70 % of the breakdown voltage for the 1.7 kV switch.

When the internal arm voltage of a certain arm is allowed to fall below V_{dc} (at times where the output-voltage of that arm is low itsself), then arm capacitance can be reduced further [11]. In contrast to (38), this presents the *necessary* condition:

$$v_{1\mathrm{u,int}}(t) \geq v_{1\mathrm{u}}(t) \cdot 1.15 \quad \forall \quad t \in [0,T]. \tag{43}$$

A voltage reserve of 15 % has been included for dynamic control. The above can be evaluated numerically with the help of the steady-state model and has been the basis for the converter design. Still, the analytic relation (41) derived from the *sufficient* condition illustrates the general law of scaling in a more comprehensive way, and has thus been discussed in a detailed manner.

5.1.1 Realization and Power Losses

For this analysis, *Electronicon* film capacitors have been taken as the reference, because they offer high energy densities, excellent current handling capabilities and a presumably long lifetime. The energy density for the prismatic E56-type [12] is around

$$\rho_{\mathrm{C,el}} \approx 150 \, \frac{\mathrm{J}}{\mathrm{liter}} \tag{44}$$

in the desired voltage- and capacitance-class. The volume is assumed to scale linearly with the rated energy storage capacity.

The power losses in the module capacitances are calculated according to the procedure described in [13]. The loss tangent for the considered Electronicon E56 film capactors is $\tan\delta_0 = 2 \cdot 10^{-4}$ as given in the datasheet [12].

5.2 Dimensioning of the Arm Inductances

When deployed in the medium-voltage grid, the sBESS is assumed to be equipped with an LCL-type line filter of which

$$L_{\mathrm{f1}} = \frac{L_{\mathrm{a}}}{2} + L_{\mathrm{g}} \tag{45}$$

represents the converter-side inductance. A very common approach is to choose this inductance such that it limits the ripple of the output current to around 10 % of the rated current [14] and afterwards design the remaining elements of the filter. However, the optimal design of an LCL-filter is not a straight forward procedure and would have gone beyond the scope of this analysis.

Instead, only L_{f1} is designed. Because the realization of an inductor itself presents an optimization problem, this procedure is included in the overall system optimization and is outlined in the following.

5.2.1 Determining L_{f1}

The minimum value for L_{f1} that limits the current ripple on the output can be estimated with the help of the steady-state model by replacing the continuous arm voltages with their respective modulated waveforms. However, this may suggest a too low maximum current and a too low inductance.

For all the converter designs calculated in this analysis, the decisive factor has always been the limiting of the fault current. In case of a grid-side voltage-dip, the current will rise quickly until at least the precontroller of the converter output voltage reacts. The effective inductance L_{f1} is decisive, because it limits the rate of rise of the output current during that time [15].

In this analysis, a sudden voltage drop at the terminals from nominal voltage to zero is considered as the worst-case scenario. The total delay in the control loop has been estimated as

$$T_{\mathrm{d}} = 25\,\mu\mathrm{s}, \tag{46}$$

including a 5 µs delay until the IGBT turns off, a 10 µs delay introduced by the measurement of the grid-voltage, and another 10 µs delay for the failure-handling routine implemented directly on the control FPGA.

It is furthermore crucial to execute the modulation of the arm voltages as part of the failure handling routine, or to realize it directly in hardware on an FPGA in order allow the IGBTs to switch out-of-order when a fault in the grid occurs. These few additional switching operations are assumed to have a negligible influence on the thermal design of the converter.

The maximum tolerated current in case of fault has been set to 150 % of the rated current. Under these assumptions, the minimum value of L_{f1} is calculated as shown in [15]:

$$L_{\mathrm{f1}} > \frac{\sqrt{\frac{2}{3}}V_{\mathrm{G}}}{\frac{0.5\sqrt{2}I_{\mathrm{nom}}}{T_{\mathrm{d}}}} = \frac{\sqrt{\frac{2}{3}}20\,\mathrm{kV}}{\frac{51\,\mathrm{A}}{25\,\mu\mathrm{s}}} \approx 8.0\,\mathrm{mH} \tag{47}$$

5.2.2 Realization

Equation (45) suggests, that L_{f1} can be realized either by one inductance $L_{\mathrm{g}} = L_{\mathrm{f1}}$ per phase, by one inductance $L_{\mathrm{a}} = 2L_{\mathrm{f1}}$ per arm, or by a combination of both. Since the arm inductances also limit the circulating current ripple, it is desirable to make them as large as possible by setting L_{g} to zero[1].

The arm inductance is considered to be distributed among the different modules. This way, the module inductances only need to be isolated against the moderate module's floating output voltage and natural cooling becomes possible.

5.2.3 Design Procedure and Power Losses

The design procedure of the module inductors is a classical multi-objective optimization: The goal is to minimize the power losses while at the same time keeping the volume of the inductance as low as possible.

In order to achieve this, a free parameter variation of the geometric dimensions of the inductor's core and the number of windings has been performed.

The skin and proximity effect in the windings are considered according to [16]. The H-Field is calculated with a one-dimensional approach; the flux in the air-gap is assumed to be homogenous. The core losses are calculated with the improved generalized Steinmetz equation (IGSE) [17]. A similar procedure has been used in [18] to design a transformer. The core of the inductor is made of two C-cores. Stranded round wire is used for the windings because the high-frequency components are small thanks to the high number of output-voltage levels. Silicon steel with a tape-thickness of 0.1 mm (0.004″) has been taken as the core material because of its high saturation flux density and low cost. The rated current of each module inductance $i_{L_{\mathrm{a}},\mathrm{max}}$ is equal to the highest arm current in case of a grid-side fault, including a margin for emergency turn off.

5.3 Cooling System and Power Losses in the IGBTs

The conduction losses and the switching losses of the IGBTs and their anti-parallel diodes are calculated using datasheet parameters. As they contribute the major share of the overall power losses, they dictate the size of the cooling system. To remove the generated heat, each IGBT-module is equipped with a heatsink for forced air cooling. Its size is estimated using a cooling system performance index of

$$\mathrm{CSPI}_{\mathrm{sem}} = 10. \tag{48}$$

The CSPI describes the relation between the size of a heatsink and it's thermal resistance when used in combination with a certain fan [19].

The heatsink is designed for an elevated ambient temperature of $T_{\mathrm{A}} = 45\,^{\circ}\mathrm{C}$. The average temperature at the base-plate of the semiconductor modules is not allowed to exceed $T_{\mathrm{case,max}} = 80\,^{\circ}\mathrm{C}$, and the average junction temperature of the semiconductors is not allowed to exceed $T_{\mathrm{j,max}} = 125\,^{\circ}\mathrm{C}$.

6 Results

Different designs of a modular multilevel converter for use in a high power energy storage system based on split batteries (sBESS) have been compared with the presented optimization procedure. All realizations investigated vary in the number of modules, the choice of the IGBTs, and the volume and power losses of the passive components.

[1] The circulating current ripple is not of primary concern in this analysis, because the converter is not connected to a dc-bus. Nevertheless, time-domain simulations have revealed, that the circulating current ripple stays approximately within the same range as the output current ripple when dimensioning the arm inductances as described.

Name	V_{br}	I_{nom}	Semiconductor Dies
Infineon FZ400R17KE4	1.7 kV	400 A	
MITSUBISHI CM400DY-50H	2.5 kV	250 A	
ABB 5SNG 0250P330305	3.3 kV	250 A	
Infineon FZ400R33KL2C	3.3 kV	400 A	
ABB 2.5 kV	2.5 kV	100 A	3× 5SMX 12L2516 + 1× 5SLX 12L2515
ABB 3.3 kV	3.3 kV	100 A	3× 5SMX 12M3300 + 1× 5SLX 12M3301
ABB 4.5 kV	4.5 kV	100 A	3× 5SMY 12N4501 + 1× 5SLY 12N4500
ABB 6.5 kV	6.4 kV	100 A	4× 5SMY 12M6501 + 2× 5SLX 12M6521

Tab. II: Semiconductors considered in this analysis and their most important characteristics.

Different IGBTs with blocking voltages ranging from 1.7 kV to 6.5 kV have been considered. Their most important parameters are summarized in Tab. II. In Fig. 4, their performance is shown in a side-by-

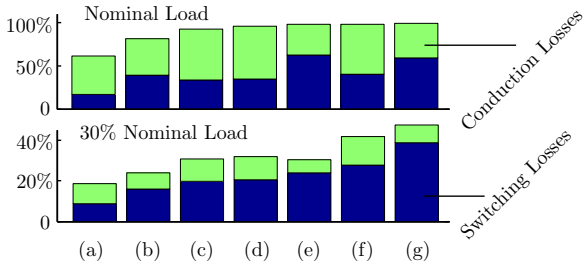

Fig. 4: Comparison of the power losses for designs with different IGBTs at nominal load and 30% nominal load. (a) Infineon FZ400R17KE4 1.7 kV, (b) ABB 4.5 kV, (c) ABB 2.5 kV, (d) ABB 3.3 kV, (e) ABB 6.5 kV, (f) MITSUBISHI CM400DY-50H 2.5 kV, (g) Infineon FZ400R33KL2C 3.3 kV

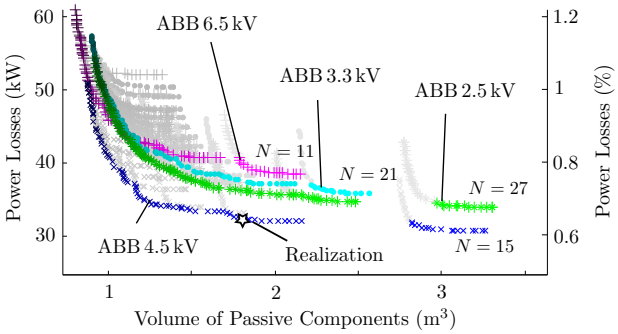

Fig. 5: Trade-off between the size of the passive components and the power losses for the different Semiconductors considered in the analysis. The gaps in between the results occur, as the number of modules is of course discrete.

side comparison averaged over the designs with different module counts for operation at full load. The *Mitsubishi CM400DY-50H* and the *Infineon FZ400R33KL2C* are available off-the-shelf. Despite their comparatively low current-ratings, they are still clearly overdimensioned for their task, resulting in poor low load performance.

Better results are obtained with the custom assemblies ABB 2.5 kV, ABB 3.3 kV, ABB 4.5 kV, ABB 6.5 kV, calculated with the datasheet parameters from commercially available IGBTs and diode dies. The die count in the assemblies has been optimized for low power losses, and only the combinations that yield the best performance are shown.

While the *FZ400R17KE4* 1.7 kV switch leads to designs with the lowest power losses, at least 34 modules are required per arm, which has been deemed uneconomical for a prospective realization. Hence, only the custom assemblies are given a closer look in the following in-depth analysis.

6.1 Size of components vs. Power conversion Efficiency

Fig. 5 shows the principal result of this study. For different IGBT modules, the colored markers approximate the theoretical trade-off between minimizing the size of the converter while at the same time keeping the power losses as low as possible. Notice how the curves are not steady, because the number of modules is discrete.

Among the considered IGBTs, the *ABB 6.5 kV* IGBT leads to solutions with the lowest module counts (starting at 11 modules) but also yields the highest power losses. With designs starting at 15 modules, the *ABB 4.5 kV* switch offers the best performance at full load and the second lowest module-count.

6.2 Sources of Power Losses vs. Largest Components

Fig. 6 shows a breakdown of the volume of the passive components and the power losses for designs with different numbers of modules. The switch used for the calculations is the *ABB 4.5 kV* custom assembly. It becomes evident, that adding just a few more modules to the design than absolutely necessary drastically reduces the size of the the module capacitors while increasing the power losses only marginally. The

total volume of the inductors has been held constant at around $200\,\mathrm{dm}^3$. The volume of the heatsinks required for forced air cooling is negligible.

The main sources of power losses are the switching losses and the conduction losses, which both rise when the number of modules is increased. The power losses in the inductors are comparatively low, and the power losses in the capacitors are negligibly small.

6.3 Realization

An attractive realization has been chosen which is marked by the black star in Fig. 5. The switches used are again the *ABB 4.5 kV* custom assemblies. With a total of 16 modules and a maximum power conversion efficiency of 99.3 % this presents an attractive choice. Fig. 7 shows a breakdown of the power losses and the volume required by the passive components for the chosen realization when operating at nominal load.

When assuming that a power conversion efficiency of around 98 % can be achieved for the dc-dc converters in the modules, the peak power conversion efficiency of the sBESS is predicted to be around 97 % (not including the roundtrip efficiency of the batteries and the power losses in a prospective mains filter).

With a total volume of $1.8\,\mathrm{m}^3$ for the passive components, the MMC converter is an ideal candidate to be employed in a high-power battery energy storage system based on split batteries. While this figure does neither include the overhead in volume for constructing a robust assembly and for meeting the isolation-requirements between the modules, nor the volume of the dc-dc converters to interface the batteries, the following comparison is tempting: An oil-filled 5 MVA medium-voltage transformer has a volume of around $14.2\,\mathrm{m}^3$ [20] and has yet to be paired with an appropriate low-voltage high-power converter.

An estimate of the volume occupied by the batteries can be calculated with commercially available rack-mountable packs, for which an energy-density of $40\,\frac{\mathrm{kWh}}{\mathrm{m}^3}$ is assumed [21]. This results in a total battery volume of around $130\,\mathrm{m}^3$. Lithium-titanate (LTO) cells are taken due to their high cycle life and high round-trip efficiency ($> 94\,\%$ expected for operation at nominal power).

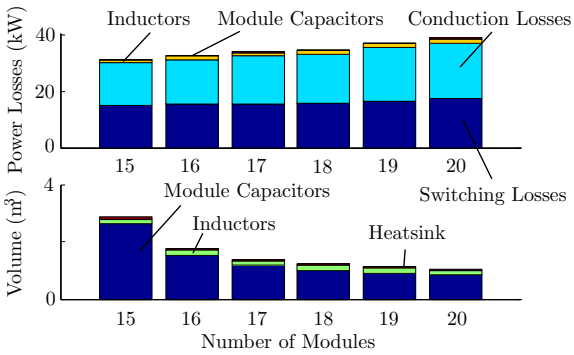

Fig. 6: Sources of power losses and size of the passive components for designs with different numbers of modules.

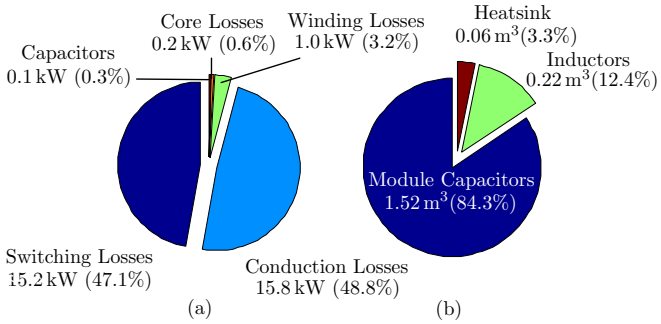

Fig. 7: (a) Shares of power losses at full load and (b) shares of the volume of the passive components.

7 Conclusion

This analysis has shown, that the choice of the correct power semiconductors is most crucial to the design of the MMC for use in an energy storage system based on split batteries. The conduction- and switching-losses present the major share of the overall power losses.

The module capacitors are by far the largest passive components. Their volume is dictated by the number of modules added to the design in addition to the technically possible minimum. Due to the high output voltage and the high number of voltage levels, the value of the arm inductances is not determined by the output current ripple but by the reaction time of the voltage precontrol in case of a grid-side fault. For a total delay between measurement and precontrol of the grid voltage of $T_\mathrm{d} = 25\,\mu\mathrm{s}$, the arm inductances are comparatively small. For implementations where this reaction time cannot be achieved, their value will scale proportionally with T_d.

A possible realization of the MMC converter has been presented in Section 6.3. The volume of the main passive components totals to $1.8\,\mathrm{m}^3$, and the peak power-conversion efficiency is predicted to be as high

as 99.3 % (not including the power losses in the dc-dc converters to interface the batteries, the batteries themselves and a prospective line-filter).

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