Diss. ETH No. 21525

Flexible oxide semiconductor electronics on plastic substrates

A dissertation submitted to

ETH Zürich

for the degree of

Doctor of Sciences

presented by

Niko Stephan Münzenrieder

Dipl.-Phys. TU München
born June 17, 1983
citizen of Germany

accepted on the recommendation of

Prof. Dr. Gerhard Tröster, ETH Zürich, examiner
Prof. Dr. Arokia Nathan, University of Cambridge, co-examiner

2013

Niko Münzenrieder
Flexible oxide semiconductor electronics on plastic substrates
Diss. ETH No. 21525

First edition 2013
Published by ETH Zürich, Switzerland

Printed by Reprozentrale ETH

Acknowledgments

First of all, I thank Prof. Dr. Gerhard Tröster for giving me the chance to perform this thesis at the Electronics Laboratory. I am very grateful for his support, the excellent infrastructure, and the nearly unlimited freedom I enjoyed during all phases of my thesis. I would also like to thank Prof. Dr. Arokia Nathan for co-examining my PhD thesis.

Additionally, I like to thank Kunigunde Cherenak for teaching me how to build a flexible transistor, and Giovanni Salvatore for the nice projects we realized together.

Especially, I would like to thank my former and current office mates Holger Harms, Thomas Kinkeldei, Christoph Zysset, Luisa Petti, Lars Büthe, and Christian Vogt for the great time, and all the interesting discussions. Thanks also to all other members of the Electronics Laboratory: Andreas, Alberto, Amir, Bernd, Bert, Conny, Clemens, Burçu, Christina, Daniel R., Daniel W., Franz, Johannes, Julia, Kilian, Long-Van, Marc, Martin W., Martin K., Mirco, Michael, Peter, Rolf, Sebastian, Silvan, Sinziana, Thomas H., Thomas S., Tobias, Ulf, Yuriy and Zack. In particular I like to mention Ruth Zähringer and Fredy Mettler for their help with administrative questions, and technical issues.

This work would not have been possible without the possibilities inside the ETH FIRST clean room. Among others, I have to thank Yargo Bonetti, Emilio Gini, Otte Homan, and Silke Schön for running this great institution. In addition, I am thankful for all the photolithography masks from Martin Lanz.

I had the chance to participate in a number of very interesting projects with other institutes and universities. In this context I like to thank Charles Perumal, Koichi Ishida, Reza Shabanpour, Bahman Boroujen, Corrado Carta, Frank Ellinger, Markus Tuomikoski, Nassim Nasseri, Randall Erb, Rafael Libanori, André Studart, and Joakim Reuteler for our enjoyable collaborations.

Furthermore, Zhang Chenming, Jonas Zürcher, Sergio Bottinelli, Deniz Görk, Ivo Strebel, and Pascal Voser delivered valuable inputs while performing their Semester and Master theses.

Finally, I also want to thank my family.

Zürich, October 2013 Niko Münzenrieder

Contents

Abstract

Since hundreds of years it is known that the world is not flat but spherical. Similarly, most of the objects in our daily life are not planar, but bendable and foldable like documents and textiles. The integration of electronic functionality into everyday objects can improve their benefit to the user, and also give rise to new applications such as flexible displays and smart textiles. The main obstacle which prevents the combination of electronics with deformable objects is the fact that electronic devices are fabricated on rigid substrates. The attachment of rigid electronics to flexible substrates restricts the bendability, is contrary to our aesthetic demands, and additionally causes problems with the localization of strain between flexible and stiff areas. One possibility to overcome these limitations is the fabrication of flexible electronic devices like thin-film transistors (TFTs) on plastic foils.

The thermal properties of plastic have to be considered during the fabrication. Therefore amorphous Indium-Gallium-Zinc-Oxide (IGZO) is a promising semiconductor since it provides a carrier mobility $>10\,cm^2V^{-1}s^{-1}$ when deposited at room temperature.

In this thesis, IGZO based TFTs were fabricated on free standing 50 µm thick polyimide substrates. Double gate structures and self-alignment was used to improve the electrical performance of the TFTs. Double gate TFTs exhibited an improved DC performance when compared to single bottom gate reference TFTs. In particular, a subthreshold swing as low as 69 mV/decade was demonstrated. On the other hand self-alignment enabled the fabrication of flexible IGZO TFTs with channel lengths of 0.5 µm. The short channel and the simultaneously reduced parasitic capacities resulted in a transit frequency of 135 MHz.

Bending of flexible electronics induces strain. This strain can not only cause changes in device performance, but also trigger the formation of cracks and lead to the failure of the electronics. Under tensile and compressive strain IGZO TFTs stayed functional down to a bending radius of ≈4 mm (strain ϵ ≈+0.6 %) and ≈1.1 mm (ϵ ≈-2.2 %) respectively. At these bending radii, tensile strain increased the effective mobility by ≈4 % while compressive strain decreased the effective mobility by ≈8 %. It was also found that illumination amplifies the influence of strain by a factor up to 5. In addition, the effects of up to 20 000 repeated bending and reflattening cycles were investigated.

To reduce the minimal possible bending radius of flexible IGZO TFTs the increase of the ductility of the TFT, and the reduction of the

strain induced by bending have been evaluated. Focused ion beam images showed that the use of ductile metals to fabricate the TFT gate contact is a practicable way to enable smaller bending radii. This finding led to TFTs with Cu gate contacts, which could be bent to a tensile radius of 1.7 mm. A reduction of the by bending induced strain was possible by the reduction of the substrate thickness. IGZO TFTs on a 1 μm thin parylene membrane could be placed on nearly any kind of surface, such as a 2 mm radius plastic rod.

For applications like the rectification of an AC signal diodes are beneficial. Room temperature deposited nickel oxide was evaluated as a potential oxidic p-type material for flexible electronics. Nickel oxide in combination with IGZO was used for the fabrication of flexible oxidic pn diodes. The resulting diodes exhibited a threshold voltage of 1.1 V, and could be operated while bend to a radius of 10 mm.

As a step towards the application of flexible electronics, digital and analog circuits were demonstrated. Prior to the fabrication of circuits, a set of design rules was compiled. These design rules guarantee the functionality of the circuits even when they are bent to a radius of 5 mm. Based on these rules logic gates, a 1-bit SRAM cell, as well as different amplifiers were fabricated. In particular, common source amplifiers exhibited a cutoff frequency of 1.2 MHz while bent, and thereby demonstrated operation in the megahertz regime.

Zusammenfassung

Seit Hunderten von Jahren ist es eine bekannte Tatsache, dass die Erde selbst die Form einer Kugel hat. Genau so sind die meisten Objekte, welchen wir in unserem täglichen Leben begegnen, nicht flach. Dokumente oder Textilien sind beispielsweise flexibel und können gefaltet werden. Gleichzeitig verspricht die Kombination von elektronischen Bauelementen mit Alltagsgegenständen einen grossen Nutzen für die Anwender und sogar neue Applikationen wie flexible Bildschirme oder elektronische Textilien. Die Integration von Elektronik mit derartigen Objekte scheitert meist daran, dass sich integrierte Schaltungen praktisch immer auf starren Halbleitersubstraten befinden. Werden starre elektronische Bauelemente auf flexible Substrate aufgebracht, ergeben sich dort versteifte Bereiche. Diese Bereiche reduzieren die Biegsamkeit des Substrates und stören das ästhetische Empfinden des Benutzers. Zudem können mechanische Spannungen am Übergang von starren zu flexiblen Bereichen zum Versagen der Elektronik führen. Die Lösung dieser Probleme liegt in der Herstellung von elektronischen Bauelementen auf flexiblen Substraten. Ein vielversprechender Ansatz für die Verwirklichung von flexibler Elektronik ist die Herstellung von Dünnschichttransistoren (TFTs) auf Plastikfolien.

Durch die limitierten thermischen Eigenschaften von Plastik muss die Herstellung von elektronischen Bauelementen auf Plastiksubstraten bei niedrigen Temperaturen erfolgen. Dies führt zur Verwendung von amorphem Indium-Gallium-Zink-Oxid (IGZO), welches bei Raumtemperatur abgeschieden werden kann, und dabei eine Ladungsträgerbeweglichkeit $>10\,\mathrm{cm^2V^{-1}s^{-1}}$ aufweist.

Die vorliegende Arbeit behandelt auf $50\,\mu\mathrm{m}$ dickem Polyimid hergestellte IGZO TFTs. Doppel-Gate Strukturen und selbstausgerichtete Kontakte wurden verwendet, um die elektrischen Eigenschaften der Transistoren zu verbessern. Doppel-Gate TFTs zeigten verbesserte DC Eigenschaften als vergleichbare TFTs mit unten liegendem Gate-Kontakt. Insbesondere war es möglich, den Subthreshold-Swing auf einen Wert von 69 mV/Dekade zu reduzieren. Gleichzeitig ermöglichte die Selbstausrichtung von Kontakten TFTs mit einer Kanallänge von $0.5\,\mu\mathrm{m}$ und verkleinerten parasitären Kapazitäten, was zu TFTs mit einer Transitfrequenz von 135 MHz führte.

Die Biegsamkeit von flexibler Elektronik stösst an ihre Grenzen, sobald mechanische Spannungen zur Bildung von Rissen in den Bauelementen führen. Aber auch kleinere Spannungen können

die Eigenschaften von flexiblen, elektronischen Bauelementen beeinflussen. Zugspannung zerstört einen IGZO TFT bei einem Biegeradius von ≈4 mm (Dehnung ϵ ≈+0.6 %) und führt zusätzlich zu einer Erhöhung der effektiven Ladungsträgerbeweglichkeit von bis zu ≈4 %. Druckspannung anderseits zerstört einen IGZO TFT erst bei einem Biegeradius von ≈1.1 mm (ϵ ≈-2.2 %) und verringert die effektive Ladungsträgerbeweglichkeit bei diesem Radius um ≈8 %. Darüber hinaus wurde festgestellt, dass die Beleuchtung der TFTs den Einfluss von mechanischer Spannung um einen Faktor 5 verstärken kann. Abschliessend wurden auch die Auswirkungen von bis zu 20 000 wiederholten Biege- und Entspannungsvorgängen auf die TFTs untersucht.

Zur Reduzierung des minimalen Biegeradius wurden zwei Ansätze verfolgt: die Erhöhung der Duktilität der TFTs, und eine Verringerung der durch Verformungen verursachten Spannungen. Untersuchungen der gebogenen TFTs zeigten, dass der Gate-Kontakt verantwortlich für die Entstehung von Rissen ist. Folglich kann die Biegsamkeit von IGZO Transistoren durch duktilere Gate-Metalle verbessert werden, was zu IGZO TFTs mit Cu Gate-Kontakten und einem minimalen Biegeradius von 1.7 mm (Zugspannung) führte. Durch die Reduzierung der Dicke des Substrates war es möglich, die durch Biegen verursachten Spannungen zu verringern. IGZO TFTs auf einer 1 μm dicken Parylene Membran konnten auf verschieden Objekten, wie hier einem Plastikstab mit 2 mm Radius, platziert werden.

Anwendungen, wie die Gleichrichtung von Wechselstrom, profitieren von der Verfügbarkeit von Dioden. Zur Realisierung von flexiblen pn-Dioden wird ein p-Typ Halbleiter benötigt, welcher sich analog zu IGZO bei niedrigen Temperaturen abscheiden lässt. Dazu wurde die Brauchbarkeit von Nickeloxid erforscht. Die Kombination von Nickeloxid und IGZO führte zu pn-Dioden mit einer Schwellspannung von 1.1 V. Diese pn-Dioden konnten ausserdem betrieben werden, während sie zu einem Radius von 10 mm gebogen waren.

Die Anwendung flexibler Elektronik wurde durch verschiedene digitale und analoge Schaltungen untersucht. Um die Biegsamkeit der auf IGZO TFTs basierenden integrierten Schaltungen zu maximieren, wurden Regeln bezüglich deren Design erarbeitet. Diese Regeln garantierten die Funktionsfähigkeit aller Schaltungen auch bei Biegeradien von 5 mm. Die hergestellten Schaltungen umfassen Logikgatter, eine 1-bit SRAM Zelle, sowie mehrere Verstärker. Insbesondere flexible Common-Source Verstärker zeigten eine Grenzfrequenz von 1.2 MHz und ermöglichen damit Betrieb im Megahertzbereich.

1

Introduction

1.1 Motivation

Since the first transistor was fabricated in 1947, semiconductor industry continuously improved the performance and the integration density of transistors, which led to the fact that in the meantime virtually every electronic gadget is equipped with integrated circuits [1]. Later, the rise of solar cells and flat panel displays pushed the development of large scale electronics. Nowadays, flexible electronics promises once again to change the daily life of billions of people in the world. Mechanically flexible and therefore bendable devices can be unobtrusively integrated into wearable devices, textiles, or healthcare equipment, and thereby lead to a higher functionally of everyday objects [2]. Furthermore, completely new applications like bendable displays or smart tags seem to be possible, and even the possible implantation of flexible medical devices into the human body is foreseen. Despite the unique mechanical properties of the devices itself, flexible electronics promise two additional advantages when compared to standard silicon technology. First, the fabrication can be done directly on plastic or paper substrates; therefore size and weight are not determined by the available single crystalline semiconductor wafers. Second, the bendability of the flexible large area substrates enables roll to roll fabrication methods. The system on panel approach which aims at the simultaneous integration of functional circuit blocks, sensors, and actuators on one flexible substrate, promises to reduce the integration efforts, and to enable large scale and light weight systems while keeping the fabrication costs low [3, 4].

At the same time it also has to be mentioned that the operation frequency and complexity of electronic circuits fabricated on flexible substrates will probably never be able to compete with circuits on semiconductor wafers. Hence, flexible electronics will enable new products, but not replace high performance devices based on materials like Si, GaAs, or SiC. This is because flexible plastic substrates are e.g. non-crystalline, mechanically instable, and have a limited thermal resistance. As a result, the fabrication of features smaller $\approx 1\,\mu m$, the use of crystalline semiconductors, and the choice of materials are general limited.

Electronics on flexible substrates are normally build using thin-film transistors (TFTs) [5] based on low temperature deposited semiconductors. The search for an appropriate semiconductor was and still is one of the most important tasks. Here, several classes of materials rang-

ing from amorphous silicon, organic molecules and solution processed carbon nanotubes to oxidic semiconductors are possible canidates. The first demonstration of a SnO_2 based oxide semiconductor TFT fabricated on glass was in 1964 [6]. Moreover, the high bandgap (typically >3 eV) of oxide semiconductors causes only little light absorption and hence allows the fabrication of transparent electronics.

Nevertheless, it took almost forty years until oxide semiconductor electronics clearly outperformed devices fabricated using other low temperature deposited semiconducting materials [7]. In particular amorphous Indium-Gallium-Zinc-Oxide (IGZO) can be deposited at room temperature and enables the fabrication of flexible TFTs with a field effect mobility around $15\,cm^2V^{-1}s^{-1}$, and on/off current ratios $>10^8$. Since oxide semiconductor TFTs also exhibit an electrically stability as least as good as the stability of a-Si:H TFTs, they can be used to fabricate circuits. The fact that solely for transparent displays [8] a revenue of more than 100 billion US$ is predicted for the year 2030 demonstrate the great potential of oxide semiconductors.

This thesis investigates and describes the mechanical and electrical performance of oxide semiconductors based electronics on bendable plastic substrates. Ways to achieve smaller bending radii, as well as higher transconductance values and transit frequencies are explored, and the application of digital and analog circuits is demonstrated.

1.2 State of the Art

This section summarizes the state of the art concerning flexible electronics, whereas the focus is on IGZO based TFTs. The first part describes fabrication techniques and materials suitable for the fabrication of flexible electronic devices. Second, the performance and the scaling behavior of flexible TFTs are reviewed. Finally an overview on the bendability and the influence of strain on flexible TFTs is given.

1.2.1 Flexible electronics

Mechanically flexible electronic devices are investigated since the 1960s [9], and a variety of approaches to fabricate flexible devices has been developed. Some of these approaches require manufacturing techniques and materials which are not used in standard silicon technologies.

Fabrication methods

Flexible electronic devices can be fabricated by several approaches; each of them has individual requirements regarding the process parameters and utilized materials:

- A silicon wafer thinned down to thicknesses below 50 μm becomes flexible [10]. The thinned die can then be attached to a flexible substrate [11, 12].
- The fabrication of silicon electronics on the free standing plastic foil is possible by the transfer of Si nanomembranes to a flexible substrate and subsequent continuation of the device fabrication. This technique requires a silicon oxide sacrificial layer, while the transfer itself can be done by direct flip transfer [13] or soft stamp methods [14].
- Post-processing of Si wafers, prior to the device fabrication, creating a porous layer underneath the fabricated devices [15], or engineering of the intrinsic stress [16] can be used to create thin chips without the need for a sacrificial layer or thinning process. These thin chips can also be placed on flexible substrates.
- Devices can be fabricated on polymers which are spin coated to a rigid substrate [17]. After fabrication the polymer is peeled off from the host substrate which results in flexible electronic devices. Here, it has to be ensured that no extensive strain is induced during the peel-off process.
- Inkjet [18] or transfer [19] printing methods can be used to fabricate electronic devices on a large scale. Here, the minimum feature size is limited by the available printing tools, and the employed materials have to be solution processable [20, 21].
- Direct fabrication of devices on free-standing, flexible substrates [22] can combine the advantages of standard semiconductor technologies and large area processing, but also suffers from the limited thermal and mechanical stability of flexible substrates [23, 9].

Materials

The fabrication of flexible electronic devices incorporates different classes of materials, these are: bendable substrates, conductors, insulators, and most important semiconductors. A schematic of a thin-film

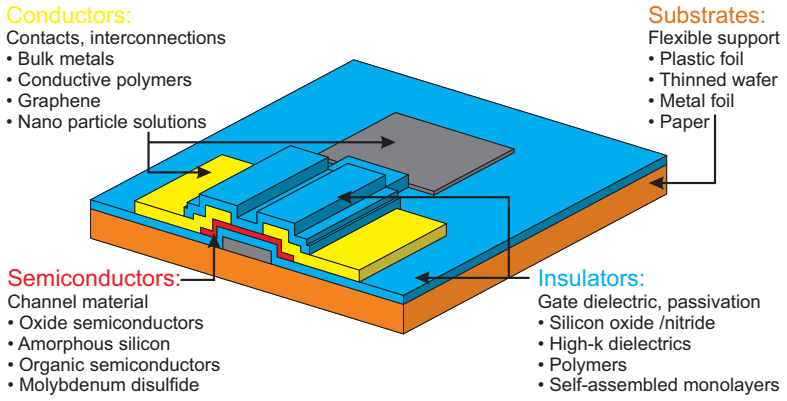

Figure 1.1: Schematic of a passivated, bottom gate thin-film transistor, and visualization of the materials most commonly used in flexible electronics.

transistor including numerous materials which are usable for the fabrication of flexible electronics is given in Fig. 1.1.

Flexible Substrates: The thickness, the surface roughness and the stability of the substrate influence the bendability, the fabrication, and the performance of the electronic devices fabricated on them [24, 25]. Concerning the potential commercialization, the costs of the substrate also has to be considered. A possible low cost material is paper [26], which is cheap, but also has a surface roughness between 0.4 µm and 20 µm [27]. Organic TFT have also been fabricated on conventional banknotes [28]. An alternative substrate is metal foil with a thickness around 100 µm. Metal foils can withstand high temperatures >650 °C [29], but have to be electrically insulated by an additional coating [30]. The most common substrates for flexible electronics are polymers. Numerous polymers like polyethylene naphthalate (PEN) or polyethylene terephthalate (PET) can be used for the fabrication of electronic devices [31]. Many polymers suffer from a low glass transition temperature around 100 °C [32]. An exception is polyimide which has a higher glass transition temperature around 300 °C [33]. Additionally, polyimide is not attacked by etchants and solvents needed during the fabrication process. Therefore electronic devices on polyimide in gen-

eral exhibit a better electrical performance than devices fabricated on other polymers. At the same time polyimide has limited light transmittance (absorbance $\approx$200 cm^{-1} at a wavelength of 405 nm [34]).

Conductive layers: Contacts and interconnection lines can either be done by metals which can be vacuum deposited from the bulk [35], or spin coated and printed using a solution of nano particles [36]. Alternative materials which exhibit higher resistivities than metals are conductive polymers like PEDOT:PSS [37], conductive oxides like ITO [38], or materials like solution processed graphene [20].

Isolators: The most common insulators for flexible electronics are low temperature PECVD deposited silicon oxide or silicon nitride [22]. The transconductance of TFTs can be increased by the use of high-k gate dielectrics like aluminum oxide or hafnium oxide, which exhibit dielectric constants ϵ_r up to 30 [39]. Additionally, polymers can be used to insulate the gate contact of a transistor, but these insulators provide lower capacitance values. This is due to the compared to inorganic materials reduced ϵ_r and in general increased layer thickness [40]. One promising approach to fabricate organic layers with a high specific capacitance could be the use of self-assembled monolayers [41], or a hybrid silicon dioxide /silicone polymer [42].

Semiconducting materials: The performance of flexible electronic devices, especially thin-film transistors, is to a large extent determined by the properties of the employed semiconductor. In particular a large carrier mobility is important for the DC and AC performance. At the same time, high carrier mobilities are normally correlated with a high semiconductor crystallinity [43], and hence deposition or annealing temperatures which are not compatible with flexible plastic substrates [44]. Beside the possibility of transferring single crystalline semiconductor membranes or thin chips to flexible foils [12], the deposition of the semiconductor has to be done at temperatures <300 °C [22].

Silicon is used to fabricate large scale electronics like display backplanes. Low temperature deposited silicon results in amorphous layers with a reduced carrier mobility around 1 $cm^2V^{-1}s^{-1}$ [45]. An advantage of amorphous silicon is that it can be doped to fabricate n- and p-type semiconducting layers [46].

Nanowires made from carbon or other semiconductors can be prepared at higher temperatures and afterwards solution processed [47]. The high mobility in single nanowires potentially enables flexible semiconductor layers with mobilities similar to the mobility of crystalline semiconductors, but the often random nanowire alignment can lead to a reduced mobility $<1\,cm^2V^{-1}s^{-1}$ [48].

P-type semiconducting polymers can be deposited at room temperature using by e.g. spin coating or evaporation processes. Due to the weak intermolecular interactions between the molecules, the mobilites in semiconducting polymers are normally $<1\,cm^2V^{-1}s^{-1}$ [49]. Higher hole mobilities up to $8\,cm^2V^{-1}s^{-1}$ have been demonstrated with small-molecules like C10-DNTT [50]. Furthermore, recent developments also enabled electron mobilities around $1\,cm^2V^{-1}s^{-1}$ in n-type organic semiconductors [51]. However, the instability of organic semiconductors under ambient conditions causes parameter changes (e.g. threshold voltage shifts >5 V), and has to be improved prior to a commercial application [52].

Since 2004 oxide semiconductors emerged as possible semiconductors for flexible electronics [7, 53]. N-type material like Zinc-Oxide [54], Zinc-Tin-Oxide [55], Cadmium-Indium-Antimony-Oxide [56], and in particular Indium-Gallium-Zinc-Oxide [7] can be deposited at room temperature and exhibit carrier mobilities above $10\,cm^2V^{-1}s^{-1}$. While grain boundaries in polycrystalline oxides like ZnO cause mobility variations on a substrate [57], amorphous materials like IGZO result in uniform layers. Similar to organic semiconductors, oxide semiconductors have the drawback that n- and p-type materials are not available with similar performance [58]. Nevertheless recent developments showed oxidic p-type materials like cuprous oxide (Cu_2O) with improved hole mobilities of $3.9\,cm^2V^{-1}s^{-1}$ [59]. Compared to amorphous silicon, amorphous oxide semiconductors also have a better electrically stability. This is due to the (compared with amorphous silicon) reduced tailing state and deep level state density [60].

An additional, more exotic way to deposit a semiconductor on a flexible substrate, which is not compatible with large scale processing, is the exfoliation of two-dimensional semiconductors. In contrast to graphene, transition-metal dichalcogenides like molybdenum disulfide MoS_2 exhibit a bandgap, and are therefore suited for the fabrication of transistors. While it is not yet clear what mobility values can be expected from MoS_2 TFTs [61, 62], mobilities up to $30\,cm^2V^{-1}s^{-1}$ have been demonstrated in MoS_2 TFTs on flexible substrates [63].

Overall, amorphous oxide semiconductors have the most beneficial properties for the fabrication of large scale electronics at low temperatures. Consequently, the commercial fabrication of IGZO backplanes for high resolution displays started in 2012 [64].

1.2.2 Flexible devices

Already before the first realization of a bipolar transistor, the field effect transistor concept was proposed in 1930 [65]. Field effect transistors can be fabricated by stacking material layer with nanometer scale thicknesses. Thin-film transistors have an increased mechanical flexibility and a smaller material consumption, when compared to transistors fabricated with bulk semiconductors. Therefore thin-film transistors are well suited for the fabrication of flexible large scale electronics. Hence, the first flexible TFT based on Tellurium and fabricated on paper was demonstrated already in 1968 [9]. Nowadays, oxide semiconductors provided the most favorable tradeoff between electrical performance, mechanical flexibility, as well as compatibility with large area and low temperature fabrication techniques of all semiconductors for flexible electronics. Therefore, the following two sections focus on oxide semiconductor based TFTs.

IGZO based TFTs

TFTs with IGZO as channel material can be fabricated directly on free standing plastic substrates [7]. IGZO can be deposited by e.g. sputtering [7], spin coating [66], or pulsed laser deposition [67], whereas room temperature RF magnetron sputtering is the most common deposition method. State-of-the art flexible n-type IGZO TFTs can be designed to operate at voltages $\leq$5 V with an average threshold voltage around 0.5 V, an effective carrier mobility around 10 $cm^2V^{-1}s^{-1}$, subthreshold swings below 100 mV/decade and on-off current ratios up to 10^{10} [68]. At the same time mobilities of 160 $cm^2V^{-1}s^{-1}$ have been demonstrated for IGZO TFTs with a calcium reduction layer fabricated on Si [69]. Other possibilities to improve the TFTs properties are the following:

The electrical performance and the stability of IGZO TFTs can be improved by a post-annealing step at a temperature around 300 °C [70].

The use of high-k dielectrics like hafnium oxide ($\epsilon_r \approx$30 [71]) can increase the gate capacitance [72] and, depending on the deposition

method, also improve the interface between IGZO and gate insulator leading to a reduced interface trap density [73]. A widely used gate insulator in flexible IGZO TFTs is ALD deposited Al_2O_3, because this material shows a low pinhole density, can be grown at temperatures below 150 °C, and has a dielectric constant close to 10 [74].

IGZO TFTs are affected by ambient conditions like the humidity [75]. The passivation and encapsulation of the IGZO layer in bottom gate TFTs (using materials like SiO_x, TiO_x or Al_2O_3) can prevent the penetration of water into the IGZO and hence improve the electrical stability under gate bias stress [76, 77]. Additionally, the passivation of the IGZO surface can also improve the device performance, in particular the subthreshold swing [78].

Typical IGZO TFTs with metallic source and drain contacts exhibit contact resistances in the order of $2 \times 10^5 \Omega\,\mu m^{-1}$. This value can be lowered by the use of an suitable source /drain contact metal, whereas Cu is an appropriate choice [79]. Furthermore the contact resistance has been reduced by plasma treatment [80], or doping of the IGZO in the source /drain contact region with Hydrogen [81]. This measures can decrease the resistivity of IGZO by 4 orders of magnitude, and thereby also reduce the contact resistances.

Besides the possibility of changing or modifying the material properties, improved TFT structures can be adopted to enable better device performances:

Self-alignment of the source and drain contacts has been used to realize flexible IGZO TFTs with a channel length of 4 μm, and overlap length down to 0.89 μm on glass [82]. Similar to standard silicon technology, self-alignment can be done by doping the semiconductor to fabricate source and drain contacts [83]. At the same time the transparency of IGZO also allows the use of backside illumination techniques [84].

Double gate structures either with two independent bottom and top gates, or one connected double gate contact have been used to increase the coupling between the gate and the IGZO channel [85]. Even an additional, floating gate contact can be used to tune the threshold voltage of IGZO TFTs [86]. Double gate geometries can also be used to improve the stability of IGZO TFTs by a better encapsulation of the IGZO layer [87].

Furthermore, IGZO TFTs can be entirely transparent if the metallic contacts are replaced by a transparent and conductive material like Indium-Tin-Oxide [88].

IGZO TFT based circuits

The operation frequency of n-type IGZO TFTs, and the yield of the fabrication process is often demonstrated by ring oscillators, here typical propagation delay values per inverter stage are ≈0.5 µs -1 µs [17, 30]. Ring oscillators fabricated with self-aligned IGZO TFTs at the same time exhibit propagation delay values down to 17 ns per stage [82]. Ring oscillators have only limited application possibilities; therefore the fabrication of digital and analog circuits is much more important. Since one of the targeted applications for IGZO TFTs, are display backplanes, driving circuits are an active field of research [89]. In contrast to other circuits like amplifiers, operation frequencies around 100 Hz are sufficiently high for display backplanes [90]. Due to this small operation frequencies, the fabrication of complete, IGZO TFT driven, active matrix displays was already demonstrated [91].

Digital circuits like inverters, NAND and NOR gates operated at frequencies up to 5 kHz have been presented [92]. Based on these elements, also more complex digital circuits such as a shift register [93] were realized on rigid substrates.

Due to the high requirements concerning device performance and stability, there are only few IGZO based analog circuits. A RFID chip based on more than 1000 IGZO TFTs [94], and a DC-DC converter operated at a clock frequency of 1 MHz were fabricated on glass substrate. The to our knowledge only analog IGZO circuit on a flexible substrate was demonstrated by our own group at the Electronics Laboratory. This circuit was a transimpedance amplifier with a cutoff frequency of ≈8 kHz and a current-to-voltage gain of 86.5 dB [95].

The problem of a missing complimentary oxide semiconductor in addition to n-type IGZO was tackled by the investigation of hybrid complimentary circuits based on IGZO in combination with organic p-type semiconductor. Vertically-stacked complementary inverters using n-type IGZO and p-type pentacene could be operated with a supply voltage of 5 V, and exhibited a voltage gain of 61 [96]. Besides complimentary circuits, IGZO TFT based circuits using 'pseudo' CMOS designs [97], and n-type dual gate TFTs [98], can achieve improved circuit performance. Nevertheless, recently developed materials and deposition techniques also enabled the fabrication of the first purely oxidic complimentary circuits using IGZO and e.g. p-type SnO, which resulted in CMOS inverters on paper (in this case also the gate insulator is paper) [99].

1.2.3 Bendability of flexible devices

The bendability of flexible electronic devices strongly depends on the thickness of the devices. This is the reason why the bendability of thinned Si wafers is normally limited to bending radii around 10 mm [100]. Additionally, the ductility of the employed materials influences the minimum bending radius. Hence, ductile organic TFTs are more flexible than TFTs based on brittle inorganic materials. The impact of mechanical strain on performance parameters like the effective mobility and the threshold voltage of TFTs depends on the particularly used semiconductor. Even within the class of oxide semiconductors large differences concerning the bendability can occur. Our group showed already in the past that, polycrystalline ZnO based TFT are strongly affected by bending, whereas amorphous IGZO TFTs show only small changes of the performance parameters [101] while bend. IGZO TFTs on flexible substrates can normally be bent to radii in the order of 4 mm [30]. Here, tensile mechanical strain of ≈1 % increases the effective mobility of IGZO TFTs by ≈5 %, and decreases the threshold voltage by up to 250 mV [102].

The influence of bending on the operation frequency is normally investigated using ring oscillators. The increased mobility of IGZO TFTs under tensile mechanical strain causes an enhancement of the oscillation frequency of IGZO ring oscillators by up to 9 % when bent to a radius of 4 mm [30]. The under strain changed effective mobility also changed the gain and the cutoff frequency of a flexible IGZO based transimpedance amplifier. A bending radius of 5 mm reduced the transimpedance gain by 1 dB Ω and increased the cutoff frequency from 8.38 kHz to 9.83 kHz [95]. Furthermore, also digital circuits under mechanical strain have been presented. Encapsulated organic inverters could be bent to a radius of 100 µm [103], Additionally, inverters, NAND and NOR gates based on nanocarbon and fabricated on a 300 µm thick substrate survived tensile strain of 50 % induced by bending to a radius of 8 mm [104]. At the same time inverters made from pentacene and IGZO could only be strained to a value of 1.25 % (radius: 5 mm) [102]. In addition, a-Si:H inverters were also three dimensionally deformed to a spherical dome with a 66° field of view [105].

A reduction of the minimal bending radius of flexible TFTs in general and IGZO TFTs in particular is possible by the use of materials with a higher ductilities or mechanical strength and by a reduction of the,

by bending induced, strain in the device. The following approaches were demonstrated:

- Encapsulation of the devices using a material layer with similar thickness and Young's modulus as the substrate shifts the neutral strain axis towards the devices and thereby enables smaller bending radii. This approach has been used to bent IGZO TFTs (demonstrated at the Electronics Laboratory, ETH Zurich) [106] as well as organic TFTs [103] to radii in the order of 100 μm.

- Since the substrate is nearly always the thickest material layer of a flexible TFT, it determines the strain which is induces by bending [107]. Hence a reduction of the substrate thickness results in a reduction of the mechanical strain and smaller bending radii. Polysilicon TFTs fabricated on a 8 μm thin polyimide foil could be bent to a radius of 1 mm [108]. Organic transistors have even been fabricated without substrate (here the gate insulator acts as mechanical support) and bent to a radius of 5 μm [109].

- A hybrid silicon dioxide /silicone polymer gate insulator with a high ductility is presented in [42]. Amorphous silicon TFTs based on this gate insulator could be bent to down to 0.5 mm radius in tension and down to 1 mm radius in compression. Additionally, TFTs made from a hybrid Indium-Zinc-Oxide /carbon nanotube composite stayed operational when bent to a radius of 0.7 mm [110]. This is because the carbon nanotubes reinforced the oxide semiconductor, and led to a higher mechanical strength.

- It has also been demonstrated that patterning of material layers can successfully prevent propagation of cracks and lead to more strain resistive layers [111]. This concept led to a reduction of the failure rate of bent (radius: 5 mm) ZnO TFTs by nearly 50 % [112].

- TFTs on flexible substrates can also be fabricated on ridges islands [113, 105] or locally protected by a stiff material layer [114]. These results have partially been reported by our group at the Electronics Laboratory. In this case the TFTs are not exposed to strain, but depending on the fill factor of the rigid areas, the overall bendability of the flexible electronic is reduced.

1.3 Objectives

This thesis discusses the fabrication and the properties of flexible electronics based on oxide semiconductors. The first objective focuses on the electrical properties of IGZO TFTs and how the device structure and the manufacturing process can be modified to increase the transconductance and transit frequency of flexible IGZO TFTs. Additionally, the use of p-type semiconducting NiO for oxide electronics is explored. The following two objectives deal with the influence of strain induced by bending: The second objective is on the measurement of electronic devices while bent, and discusses the strain induced parameter shift of flexible IGZO TFTs, as well as their minimum bending radius. The formation of cracks which is the dominant failure mechanisms under high mechanical strain is studied in the third objective. Here, approaches to reduce the minimum possible bending radius are also verified. In the last objective, the application of IGZO TFTs in integrated circuits is discussed, and the properties of these circuits are investigated.

1.3.1 Electrical performance of flexible oxide semiconductor based electronic devices

The fabrication and hence the electrical performance of electronics on free-standing plastic foils is affected by several substrate specific limitations like the mechanical instability or the low temperature resistance of plastic substrates. Simultaneously, flexible devices have to fulfill certain requirements e.g. a as high as possible drain current for the fabrication of display driving circuits, or an maximized transconductance and transit frequency for the fabrication of amplifiers..

In this thesis the following research questions concerning the electrical performance of flexible electronic devices based on oxide semiconductors are discussed:

- Which properties of flexible substrates limit the miniaturization and electrical performance of TFTs on free-standing plastic substrates?
- How can the gate capacitance and therefore the transconductance of flexible TFTs be increased?
- Can the channel length of TFTs fabricated on free-standing plastic foil be scaled into the submicron regime?

- How can the overlap capacities of a flexible TFT be reduced?
- What is a suitable p-type semiconductor for flexible oxide electronics?

1.3.2 Influence of mechanical strain

The full potential of flexible electronics can only be utilized if the devices are deformable or mounted on a curved surface. Bending of the devices at the same time induces mechanical strain which can influence the device performance, and ultimately lead to permanent device failure. Concerning the application of flexible electronics, it is important to understand the origin and the magnitude of the strain induced performance parameter shifts of flexible devices. Additionally, it has to be known up to which value the devices can be strained. Furthermore, roll to roll fabrication techniques can only be applied if the devices survive the strain induced during the fabrication process.

The following research questions are investigated within this thesis, aiming at the evaluation of the influence of mechanical strain on flexible electronic devices:

- How can the influence of strain on flexible electronics be measured?
- What is the effect of mechanical strain on the performance parameters of flexible IGZO TFTs?
- Is there a difference between tensile and compressive strain?
- What is the maximum strain at which flexible IGZO TFTs can be operated?
- How does repeated bending and reflattening affect flexible IGZO TFTs?

1.3.3 Maximum bendability of transistors

The robustness and the number of possible applications of flexible transistors increase with their bendability. TFTs based on oxide semiconductors exhibit a reduced flexibility when compared to organic TFTs. Applications like smart textiles require ways to enable smaller bending radii of IGZO TFTs. Since the bendability of IGZO TFTs is

limited by the strain induced formation of cracks in the TFT stack, either the ductility of the TFT has to be increased or the strain at a given bending radius has be decreased.

Answers to the following research questions will be given in this thesis, and TFTs with improved flexibility will be demonstrated:

- What are suitable approaches to reduce the mechanical strain in bent electronic devices?
- Which layer of the device stack is responsible for the formation of cracks under bending?
- Can the ductility of the IGZO TFT stack be improved, without degenerating the electrical device performance?
- Is the reduction of the substrate thickness a suitable way to increase the flexibility of IGZO TFTs?

1.3.4 Flexible circuits

Commercially available flexible electronics will not only incorporate single transistors but requires integrated circuits. Here, digital circuits e.g. to store data, and analog amplifiers for sensor readouts or signal transmission are requested. However, challenges related to the comparatively small transconductance and operation frequency (in contrast to standard semiconductor technologies), and the fact that no commercial design tools are available, have to be handled.

In this thesis, the following research questions concerning the application of flexible IGZO TFTs are addressed:

- How can the influence of strain on the performance of circuits be minimized?
- Is it possible to fabricate flexible integrated circuits using IGZO TFTs?
- Can flexible IGZO based circuits operate in the megahertz regime?

1.4 Thesis Outline

The thesis is structured into ten chapters. In chapter 2, a summary of the achievements, the limitations, a conclusion of the work as well as an outlook of possible future research directions can be found. In chapters 3 to 10, scientific publications according to the order in Table 1.1 are presented. Fig. 1.2 visualizes the structure of the thesis and indicates the relation of the single scientific publications to each other.

In chapter 3 flexible IGZO TFTs and ways to improve their DC performance are presented. Chapter 4 introduces a custom build bending tester able to characterize TFTs while bent. The influence of mechanical strain on IGZO TFTs is quantified and explained in Chapter 5. Chapters 6 and 7 describe two possible ways to prevent the formation of cracks in flexible IGZO TFTs and thereby enable smaller bending radii. Design rules for the fabrication of flexible circuits based on IGZO TFTs are given in Chapter 8. Applications of these design rules are given in the last two Chapters. Chapter 9 shows an integrated flexible 1-bit SRAM element, and Chapter 10 demonstrates bendable amplifier circuits.

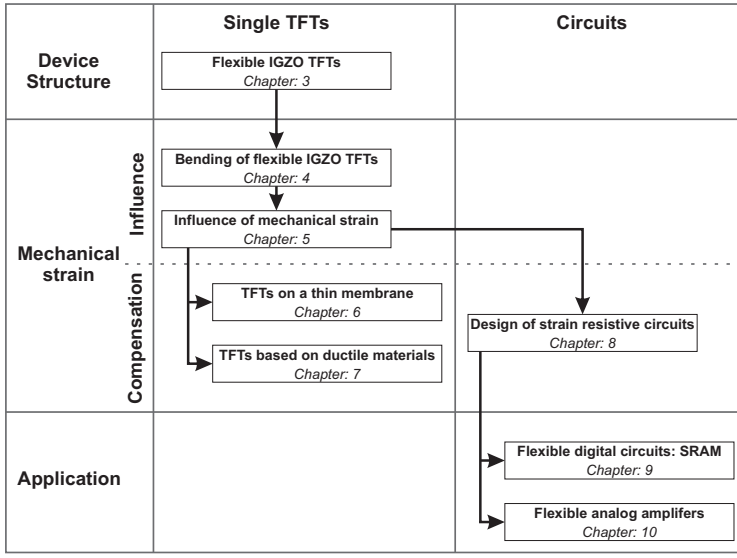

Figure 1.2: Outline of the thesis, structured into ten chapters.

Table 1.1: Publications and their corresponding sections in this thesis.

Chapter	Publication
3	Flexible double gate a-IGZO TFT fabricated on free standing polyimide foil N. Münzenrieder, C. Zysset, L. Petti, T. Kinkeldei, G.A. Salvatore, and G. Tröster Solid-State Electronics, 84, pp. 198–204, 2013.
4	Testing of flexible InGaZnO-based thin-film transistors under mechanical strain N. Münzenrieder, K. Cherenack, and G. Tröster The European Physical Journal Applied Physics, 55 (2), pp. 23904-p1–23904-p5, 2011.
5	The Effects of Mechanical Bending and Illumination on the Performance of Flexible IGZO TFTs N. Münzenrieder, K. Cherenack, and G. Tröster IEEE Transactions on Electron Devices, 58 (7), pp. 2041–2048, 2011.
6	InGaZnO TFTs on a Flexible Membrane Transferred to a Curved Surface with a Radius of 2 mm N. Münzenrieder, G.A. Salvatore, T. Kinkeldei, L. Petti, C. Zysset, L. Büthe, and G. Tröster 71st Device Research Conference, DRC, Notre Dame, USA, pp. 165–166, 2013.
7	Investigation of gate material ductility enables flexible a-IGZO TFTs bendable to a radius of 1.7 mm N. Münzenrieder, L. Petti, C. Zysset, D. Görk, L. Büthe, G.A. Salvatore, and G. Tröster 43rd European Solid-State Device Research Conference, ESSDERC13, Bucharest, Romania, pp. 362–365, 2013

8	Design rules for IGZO logic gates on plastic foil enabling operation at bending radii of 3.5 mm N. Münzenrieder, C. Zysset, T. Kinkeldei, and G. Tröster IEEE Transactions on Electron Devices, 59 (8), pp. 2153–2159, 2012.
9	A flexible InGaZnO based 1-bit SRAM under mechanical strain N. Münzenrieder, C. Zysset, T. Kinkeldei, K. Cherenack, and G. Tröster Semiconductor Conference Dresden, SCD, Dresden, Germany, pp. 1–4, 2011.
10	Flexible a-IGZO TFT amplifier fabricated on a free standing polyimide foil operating at 1.2 MHz while bent to a radius of 5 mm N. Münzenrieder, L. Petti, C. Zysset, G.A. Salvatore, T. Kinkeldei, C. Perumal, C. Carta, F. Ellinger, and G. Tröster IEEE International Electron Devices Meeting, IEDM, San-Francisco, USA, pp. 5.2.1 - 5.2.4, 2012

1.5 Additional Publications

The following publications have been written in addition to those presented in this thesis:

- K. Cherenack, N. Münzenrieder, and G. Tröster. Impact of Mechanical Bending on ZnO and IGZO Thin-Film Transistors. In *IEEE Electron Device Letters*, 31 (11), pages 1254–1256, 2010.
- K. Cherenack, C. Zysset, T. Kinkeldei, N. Münzenrieder, and G. Tröster. Wearable Electronics: Woven Electronic Fibers with Sensing and Display Functions for Smart Textiles. In *Advanced Materials*, 22 (45), page 5071, 2010.
- N. Münzenrieder, K. Cherenack, and G. Tröster. Testing of InGaZnO TFTs under applied compressive strain. *Plastic Electronics*, Dresden, Germany, 2010.

- N. Münzenrieder, K. Cherenack, and G. Tröster. Testing of flexible IGZO based TFTs under mechanical strain. *3rd International Symposium on Flexible Organic Electronics*, Halkidiki, Greece, 2010.
- C. Zysset, T. Kinkeldei, K. Cherenack, N. Münzenrieder, and G. Tröster. Verwebbare Elektronik. *MikroSytemTechnik Kongress*, 2011.
- T. Kinkeldei, N. Münzenrieder, C. Zysset, K. Cherenack, and G. Tröster. Encapsulation for Flexible Electronic Devices. In *Electron Device Letters*, 32 (12), pages 1743–1745, 2011.
- C. Zysset, N. Münzenrieder, T. Kinkeldei, K. Cherenack, and G. Tröster. Indium-gallium-zinc-oxide based mechanically flexible transimpedance amplifier. In *Electronics Letters*, 47 (12), pages 691–692, 2011.
- N. Münzenrieder, K. Cherenack, and G. Tröster. Flexible InGaZnO thin film transistors & The impact of tensile & compressive mechanical stress on a long time scale. *7th International Thin-Film Transistor Conference (ITC)*, Cambridge, United Kingdom, 2011.
- T. Kinkeldei, C. Zysset, N. Münzenrieder, and G. Tröster. Influence of Flexible Substrate Materials on the Performance of Polymer Composite Gas Sensors. In *International Meeting on Chemical Sensors*, Nürnberg, Germany, 2012.
- T. Kinkeldei, C. Zysset, N. Münzenrieder, L. Petti, and G. Tröster. In Tube Integrated Electronic Nose System on a Flexible Polymer Substrate. In *Sensors*, 12 (10), pages 13684–13693, 2012.
- C. Zysset, T. Kinkeldei, N. Münzenrieder, K. Cherenack, and G. Tröster. Integration Method for Electronics in Woven Textiles. In *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, 2 (7), pages 1107–1117, 2012.
- T. Kinkeldei, C. Zysset, N. Münzenrieder, and G. Tröster. An electronic nose on flexible substrates integrated into a smart textile. In *Sensors and Actuators B: Chemical*, 174, pages 81–86, 2012.
- C. Zysset, N. Münzenrieder, T. Kinkeldei, K. Cherenack, and G. Tröster. A Woven Active-Matrix Display. In *IEEE Transactions on Electron Devices*, 59 (3), pages 721–727, 2012.

- N. Münzenrieder, C. Zysset, T. Kinkeldei, L. Petti, G.A. Salvatore, and G. Tröster. Mechanically Flexible Double Gate a-IGZO TFTs. In *42nd European Solid-State Device Research Conference (ESSDERC12)*, Bordaux, France, pages 133–136, 2012.

- R. Erb, K. Cherenack, R. Stahel, R. Libanori, T. Kinkeldei, N. Münzenrieder, G. Tröster and A. Studart. Locally Reinforced Polymer-Based Composites for Elastic Electronics. In *ACS Applied Materials & Interfaces*, 4 (6), pages 2860–2864, 2012.

- T. Kinkeldei, C. Zysset, N. Münzenrieder, and G. Tröster. The influence of bending on the performance of flexible carbon black/polymer composite gas sensors. In *Journal of Polymer Science Part B: Polymer Physics*, 51 (5), pages 329–336, 2013.

- L. Petti, N. Münzenrieder, C. Zysset, T. Kinkeldei, G.A. Salvatore, and G. Tröster. Influence of Mechanical Strain on Flexible IGZO-Based Ferroelectric Memory TFTs. In *9th International Thin-Film Transistor Conference (ITC)*, Tokyo, Japan, 2013.

- C. Zysset, T. Kinkeldei, N. Münzenrieder, K. Cherenack, and G. Tröster. Fabrication technologies for the integration of thin-film electronics into smart textiles, in *Multidisciplinary know-how for smart-textiles developers*, ed. T. Kirstein, Cambridge: Woodhead Publishing, 2013.

- N. Münzenrieder, C. Zysset, L. Petti, T. Kinkeldei, G.A. Salvatore, and G. Tröster. Room temperature fabricated flexible NiO/IGZO pn diode under mechanical strain. In *Solid-State Electronics*, 87, pages 17–20, 2013.

- C. Zysset, N. Nasseri, L. Büthe, N. Münzenrieder, T. Kinkeldei, L. Petti, S. Kleiser, G. Salvatore, M. Wolf, and G. Tröster. Textile Integrated Sensors and Actuators for Near-Infrared Spectroscopy. In *Optics Express*, 21 (3), pages 3213–3224, 2013.

- R. Shabanpour, K. Ishida, C. Perumal, B.K. Boroujeni, T. Meister, C. Carta, F. Ellinger, L. Petti, N. Münzenrieder, G.A. Salvatore, and G. Tröster. A 2.62 MHz 762 μW Cascode Amplifier in Flexible a-IGZO Thin-Film Technology for Textile and Wearable-Electronics Applications. In *International Semiconductor Conference Dresden - Grenoble (ISCDG)*, Dresden, Germany, pages 1–4, 2013.

- C. Perumal, K. Ishida, R. Shabanpour, B.K. Boroujeni, L. Petti, N. Münzenrieder, G.A. Salvatore, C. Carta, G. Tröster, and F. Ellinger. A Compact a-IGZO TFT Model Based on MOSFET SPICE Level=3 Template for Analog/RF Circuit Designs. In *Electron Device Letters*, 34 (11), pages 1391–1393, 2013.

- G.A. Salvatore, N. Münzenrieder, C. Barraud, L. Petti, C. Zysset, L. Büthe, K. Ensslin, and G. Tröster. Fabrication and Transfer of Flexible Few-Layers MoS2 Thin Film Transistors to Any Arbitrary Substrate. In *ACS Nano*, 7 (10), pages 8809–8815, 2013.

- C. Zysset, N. Münzenrieder, L. Petti, L. Büthe, G.A. Salvatore, and G. Tröster. IGZO TFT-Based All-Enhancement Operational Amplifier Bent to a Radius of 5 mm. In *Electron Device Letters*, 34 (11), pages 1394–1396, 2013.

- T. Kinkeldei, C. Denier, C. Zysset, N. Münzenrieder, and G. Tröster. 2D Thin Film Temperature Sensors Fabricated onto 3D Nylon Yarn Surface for Smart Textile Applications. In *Research Journal of Textile and Apparel*, 17 (2), pages 16–20, 2013.

- C. Zysset, T. Kinkeldei, N. Münzenrieder, L. Petti, G.A. Salvatore, and G. Tröster. Combining electronics on flexible plastic strips with textiles. In *Textile Research Journal*, 83 (11), pages 1130–1142, 2013.

- N. Münzenrieder, C. Zysset, L. Petti, T. Kinkeldei, G.A. Salvatore, and G. Tröster. Flexible self-aligned amorphous InGaZnO thin-film transistors with sub-micrometer channel length and a transit frequency of 135 MHz. In *IEEE Transactions on Electron Devices*, 60 (9), pages 2815–2820, 2013.

Bibliography

[1] W.F. Brinkman, D.E. Haggan, and W.W. Troutman. A history of the invention of the transistor and where it will lead us. *Solid-State Circuits, IEEE Journal of*, 32(12):1858–1865, 1997.

[2] A. Nathan, A. Ahnood, Matthew T. Cole, Sungsik Lee, Y. Suzuki, P. Hiralal, F. Bonaccorso, T. Hasan, L. Garcia-Gancedo, A. Dyadyusha, S. Haque, P. Andrew, S. Hofmann, J. Moultrie, Daping Chu, A.J. Flewitt, A.C. Ferrari, M.J. Kelly, J. Robertson, G. Amaratunga, and William I. Milne. Flexible electronics: The next ubiquitous platform. *Proceedings of the IEEE*, 100(13):1486–1517, 2012.

[3] Z. Meng, M. Wang, and M. Wong. High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications. *Electron Devices, IEEE Transactions on*, 47(2):404–409, 2000.

[4] R.F. Service. Patterning electronics on the cheap. *Science*, 278:383–384, 1997.

[5] P.K. Weimer. The tft a new thin-film transistor. *Proceedings of the IRE*, 50(6):1462–1469, 1962.

[6] H.A. Klasens and H. Koelmans. A tin oxide field-effect transistor. *Solid-State Electronics*, 7(9):701–702, 1964.

[7] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, 432(7016):488–492, 2004.

[8] E. Fortunato, P. Barquinha, and R. Martins. Oxide semiconductor thin-film transistors: A review of recent advances. *Advanced Materials*, 24(22):2945–2986, 2012.

[9] W.S. Wong and A. Salleo. *Flexible electronics: materials and applications*, volume 11. Springer, 2009.

[10] H.L. Kao, A. Chin, B.F. Hung, J. M. Lai, C.F. Lee, M. F Li, G.S. Samudra, C. Zhu, Z.L. Xia, X.Y. Liu, and J.F. Kang. Strain-induced very low noise rf mosfets on flexible plastic substrate. In *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pages 160–161. IEEE, 2005.

[11] B. Holland, R. Mcpherson, T. Zhang, Z. Hou, R. Dean, R.W. Johnson, L. Del Castillo, and A. Moussessian. Ultra-thin, flexible electronics. In *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, pages 1110–1116. IEEE, 2008.

[12] T. Zhang, Z. Hou, R.W. Johnson, L. Del Castillo, A. Moussessian, R. Greenwell, and B.J. Blalock. Flexible electronics: Thin silicon die on flexible substrates. *Electronics Packaging Manufacturing, IEEE Transactions on*, 32(4):291–300, 2009.

[13] H.-C. Yuan and Z. Ma. Microwave thin-film transistors using si nanomembranes on flexible polymer substrate. *Applied physics letters*, 89(21):212105–212105, 2006.

[14] Z.-T. Zhu, E. Menard, K. Hurley, R.G. Nuzzo, and J.A. Rogers. Spin on dopants for high-performance single-crystal silicon transistors on flexible plastic substrates. *Applied Physics Letters*, 86(13):133507–133507, 2005.

[15] M. Zimmermann, J.N. Burghartz, W. Appel, N. Remmers, C. Burwick, R. Wurz, O. Tobail, M. Schubert, G. Palfinger, and J. Werner. A seamless ultra-thin chip fabrication and assembly process. In *Electron Devices Meeting, 2006. IEDM'06. International*, pages 1–3. IEEE, 2006.

[16] D. Shahrjerdi and S.W. Bedell. Extremely flexible nanoscale ultrathin body silicon integrated circuits on plastic. *Nano letters*, 13(1):315–320, 2012.

[17] M. Mativenga, M.H. Choi, J.W. Choi, and J. Jang. Transparent flexible circuits based on amorphous-indium-gallium-zinc-oxide thin-film transistors. *Electron Device Letters, IEEE*, 32(2):170–172, 2011.

[18] S.H. Ko, H. Pan, C.P. Grigoropoulos, C.K. Luscombe, J.M.J. Fréchet, and D. Poulikakos. All-inkjet-printed flexible electronics fabrication on a polymer substrate by low-temperature high-

resolution selective laser sintering of metal nanoparticles. *Nanotechnology*, 18(34):345202, 2007.

[19] D.R. Hines, V.W. Ballarotto, E.D. Williams, Y. Shao, and S.A. Solin. Transfer printing methods for the fabrication of flexible organic electronics. *Journal of applied physics*, 101(2):024503–024503, 2007.

[20] F. Torrisi, T. Hasan, W. Wu, Z. Sun, A. Lombardo, T.S. Kulmala, G.-W. Hsieh, S. Jung, F. Bonaccorso, P.J. Paul, C. Daping, and Andrea C. F. Inkjet-printed graphene electronics. *ACS nano*, 6(4):2992–3006, 2012.

[21] M. Singh, H.M. Haverinen, P. Dhagat, and G.E. Jabbour. Inkjet printing—process and its applications. *Advanced materials*, 22(6):673–685, 2010.

[22] K.H. Cherenack, A.Z. Kattamis, B. Hekmatshoar, J.C. Sturm, and S. Wagner. Amorphous-silicon thin-film transistors fabricated at 300 °C on a free-standing foil substrate of clear plastic. *Electron Device Letters, IEEE*, 28(11):1004–1006, 2007.

[23] K.H. Cherenack, B. Hekmatshoar, J.C. Sturm, and S. Wagner. Self-aligned amorphous silicon thin-film transistors fabricated on clear plastic at 300< formula formulatype=. *Electron Devices, IEEE Transactions on*, 57(10):2381–2389, 2010.

[24] H. Cheng, J. Wu, M. Li, D.-H. Kim, Y.-S. Kim, Y. Huang, Z. Kang, K.C. Hwang, and J.A. Rogers. An analytical model of strain isolation for stretchable and flexible electronics. *Applied Physics Letters*, 98(6):061902–061902, 2011.

[25] W. Xu, J.S. Yang, and T.J. Lu. Ductility of thin copper films on rough polymer substrates. *Materials & Design*, 32(1):154–161, 2011.

[26] Y. Chen, J. Au, P. Kazlas, A. Ritenour, H. Gates, and M. McCreary. Electronic paper: Flexible active-matrix electronic ink display. *Nature*, 423(6936):136–136, 2003.

[27] A.C. Siegel, S.T. Phillips, M.D. Dickey, N. Lu, Z. Suo, and G.M. Whitesides. Foldable printed circuit boards on paper substrates. *Advanced Functional Materials*, 20(1):28–35, 2010.

[28] U. Zschieschang, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, and H. Klauk. Organic electronics on banknotes. *Advanced Materials*, 23(5):654–658, 2011.

[29] M.N. Troccoli, A.J. Roudbari, T.-K. Chuang, and M.K. Hatalis. Polysilicon tft circuits on flexible stainless steel foils. *Solid-state electronics*, 50(6):1080–1087, 2006.

[30] S.A. Khan, P.-C. Kuo, A. Jamshidi-Roudbari, and M. Hatalis. Effect of uniaxial tensile strain on electrical performance of amorphous igzo tfts and circuits on flexible metal foils. In *Device Research Conference (DRC), 2010*, pages 119–120. IEEE, 2010.

[31] M. Ito, M. Kon, C. Miyazaki, N. Ikeda, M. Ishizaki, R. Matsubara, Y. Ugajin, and N. Sekine. Amorphous oxide TFT and their applications in electrophoretic displays. *Physica Status Solidi (A)*, 205(8):1885–1894, 2008.

[32] Y. Shi and S.A. Jabarin. Glass-transition and melting behavior of poly (ethylene terephthalate)/poly (ethylene 2, 6-naphthalate) blends. *Journal of applied polymer science*, 81(1):11–22, 2001.

[33] R. Yokota, S. Yamamoto, S. Yano, T. Sawaguchi, M. Hasegawa, H. Yamaguchi, H. Ozawa, and R. Sato. Molecular design of heat resistant polyimides having excellent processability and high glass transition temperature. *High Performance Polymers*, 13(2):S61–S72, 2001.

[34] R.H. French, J.M. Rodríguez-Parada, M.K. Yang, R.A. Derryberry, and N.T. Pfeiffenberger. Optical properties of polymeric materials for concentrator photovoltaic systems. *Solar Energy Materials and Solar Cells*, 95(8):2077–2086, 2011.

[35] S.P. Lacour, J. Jones, Z. Suo, and S. Wagner. Design and performance of thin metal film interconnects for skin-like electronic circuits. *Electron Device Letters, IEEE*, 25(4):179–181, 2004.

[36] D. Kim, S. Jeong, S. Lee, B.K. Park, and J. Moon. Organic thin film transistor using silver electrodes by the ink-jet printing technology. *Thin Solid Films*, 515(19):7692–7696, 2007.

[37] T. Kawase, H. Sirringhaus, R.H. Friend, and T. Shimoda. All-polymer thin film transistors fabricated by high-resolution ink-

jet printing. In *Electron Devices Meeting, 2000. IEDM'00. Technical Digest. International*, pages 623–626. IEEE, 2000.

[38] H.-K. Kim, J.-A. Jeong, K.-H. Choi, S.-W. Jeong, and J.-W. Kang. Characteristics of flexible ito electrodes grown by continuous facing target roll-to-roll sputtering for flexible organic solar cells. *Electrochemical and Solid-State Letters*, 12(5):H169–H172, 2009.

[39] J.H. Kim, B.D. Ahn, C.H. Lee, K.A. Jeon, H.S. Kang, and S.Y. Lee. Characteristics of transparent zno based thin film transistors with amorphous hfo< sub> 2</sub> gate insulators and ga doped zno electrodes. *Thin Solid Films*, 516(7):1529–1532, 2008.

[40] H.-W. Zan and T.-Y. Hsu. Stable encapsulated organic tft with a spin-coated poly (4-vinylphenol-co-methyl methacrylate) dielectric. *Electron Device Letters, IEEE*, 32(8):1131–1133, 2011.

[41] T. Schmaltz, A.Y. Amin, A. Khassanov, T. Meyer-Friedrichsen, H.-G. Steinrück, A. Magerl, J. J. Segura, K. Voitchovsky, F. Stellacci, and M. Halik. Low-voltage self-assembled monolayer field-effect transistors on flexible substrates. *Advanced Materials*, pages 1–4, 2013.

[42] L. Han, K. Song, P. Mandlik, and S. Wagner. Ultraflexible amorphous silicon transistors made with a resilient insulator. *Applied Physics Letters*, 96(4):042111–042111, 2010.

[43] C. Kittel and P. McEuen. *Introduction to solid state physics*, volume 7. Wiley New York, 1996.

[44] G. Liu and S.J. Fonash. Selective area crystallization of amorphous silicon films by low-temperature rapid thermal annealing. *Applied Physics Letters*, 55(7):660–662, 1989.

[45] J.C. Sturm, Y. Huang, L. Han, T. Liu, B. Hekmatshoar, K. Cherenack, E. Lausecker, and S. Wagner. Amorphous silicon: The other silicon. In *Ultimate Integration on Silicon (ULIS), 2011 12th International Conference on*, pages 1–4. IEEE, 2011.

[46] R.A. Street, J. Zesch, and M.J. Thompson. Effects of doping on transport and deep trapping in hydrogenated amorphous silicon. *Applied Physics Letters*, 43(7):672–674, 1983.

[47] X. Duan, C. Niu, V. Sahi, J. Chen, J.W. Parce, S. Empedocles, and J.L. Goldman. High-performance thin-film transistors using semiconductor nanowires and nanoribbons. *Nature*, 425(6955):274–278, 2003.

[48] T. Takenobu, T. Takahashi, T. Kanbara, K. Tsukagoshi, Y. Aoyagi, and Y. Iwasa. High-performance transparent flexible transistors using carbon nanotube films. *Applied physics letters*, 88(3):033511–033511, 2006.

[49] I. McCulloch, M. Heeney, C. Bailey, K. Genevicius, I. MacDonald, M. Shkunov, D. Sparrowe, S. Tierney, R. Wagner, W. Zhang, M.L. Chabinyc, R.J. Kline, M.D. McGehee, and Toney M. F. Liquid-crystalline semiconducting polymers with high charge-carrier mobility. *Nature materials*, 5(4):328–333, 2006.

[50] U. Zschieschang, R. Hofmockel, R. Rödel, U. Kraft, M.J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. Butschke, H. Richter, J.N. Burghartz, and H. Klauk. Megahertz operation of flexible low-voltage organic thin-film transistors. *Organic Electronics*, 2013.

[51] J.E. Anthony, A. Facchetti, M. Heeney, S.R. Marder, and X. Zhan. n-type organic semiconductors in organic electronics. *Advanced Materials*, 22(34):3876–3892, 2010.

[52] X. Guo, R.P. Ortiz, Y. Zheng, S. Kim, M.-G.and Zhang, Y. Hu, G. Lu, A. Facchetti, and T.J. Marks. Thieno [3, 4-c] pyrrole-4, 6-dione-based polymer semiconductors: toward high-performance, air-stable organic thin-film transistors. *Journal of the American Chemical Society*, 133(34):13685–13697, 2011.

[53] H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono. Amorphous oxide channel tfts. *Thin Solid Films*, 516(7):1516–1522, 2008.

[54] E. Fortunato, P. Barquinha, A.C.M.B.G. Pimentel, A.M.F. Gonçalves, A.J.S. Marques, R.F.P. Martins, and L. Pereira. Wide-bandgap high-mobility zno thin-film transistors produced at room temperature. *Applied Physics Letters*, 85(13):2541–2543, 2004.

[55] P. Görrn, M. Sander, J. Meyer, M. Kröger, E. Becker, H.-H. Johannes, W. Kowalsky, and T. Riedl. Towards see-through displays: Fully transparent thin-film transistors driving transparent

organic light-emitting diodes. *Advanced Materials*, 18(6):738–741, 2006.

[56] H. Tetsuka, Y. Jin Shan, K. Tezuka, and H. Imoto. Transparent amorphous conductive cd–in–sb–o thin films for flexible devices. *Vacuum*, 80(9):1038–1041, 2006.

[57] R.L. Hoffman. Zno-channel thin-film transistors: Channel mobility. *Journal of Applied Physics*, 95(10):5813–5819, 2004.

[58] H. Hosono. Ionic amorphous oxide semiconductors: Material design, carrier transport, and device application. *Journal of Non-Crystalline Solids*, 352:851–858, 2006.

[59] E. Fortunato, V. Figueiredo, P. Barquinha, E. Elamurugu, R. Barros, G. Gonçalves, S.-H.K. Park, C.-S. Hwang, and R. Martins. Thin-film transistors based on p-type cu2o thin films produced at room temperature. *Applied physics letters*, 96(19):192102–192102, 2010.

[60] J.K. Jeong. The status and perspectives of metal oxide thin-film transistors for active matrix flexible displays. *Semiconductor Science and Technology*, 26(3):034008, 2011.

[61] M.S. Fuhrer and J. Hone. Measurement of mobility in dual-gated mos2 transistors. *Nature nanotechnology*, 8(3):146–147, 2013.

[62] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis. Single-layer mos2 transistors. *Nature nanotechnology*, 6(3):147–150, 2011.

[63] H.-Y. Chang, S. Yang, J. Lee, L. Tao, W.-S. Hwang, D. Jena, N. Lu, and D. Akinwande. High-performance, highly bendable mos2 transistors with high-k dielectrics for flexible low-power systems. *ACS nano*, 2013.

[64] Sharp IGZO LCD Panels. `http://www.sharp-world.com/corporate/news/120413.html`. [Online; accessed 22nd of July 2013].

[65] J.E. Lilienfeld. Lilienfeld, 1930. US Patent 1 745 175.

[66] Y.-H. Yang, S.S. Yang, C.-Y. Kao, and K.-S. Chou. Chemical and electrical properties of low-temperature solution-processed

in–ga–zn-o thin-film transistors. *Electron Device Letters, IEEE*, 31(4):329–331, 2010.

[67] A. Suresh, P. Gollakota, P. Wellenius, A. Dhawan, and J.F. Muth. Transparent, high mobility ingazno thin films deposited by pld. *Thin Solid Films*, 516(7):1326–1329, 2008.

[68] L.-Y. Su, H.-Y. Lin, H.-K. Lin, S.-L. Wang, L.-H. Peng, and J.J. Huang. Characterizations of amorphous igzo thin-film transistors with low subthreshold swing. *Electron Device Letters, IEEE*, 32(9):1245–1247, 2011.

[69] H.-W. Zan, C.-C. Yeh, H.-F. Meng, C.-C. Tsai, and L.-H. Chen. Achieving high field-effect mobility in amorphous indium-gallium-zinc oxide by capping a strong reduction layer. *Advanced Materials*, 24(26):3509–3514, 2012.

[70] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, and H. Hosono. Trap densities in amorphous-ingazno4 thin-film transistors. *Applied Physics Letters*, 92(13):133512–133512, 2008.

[71] B.H. Lee, L. Kang, W.-J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J.C. Lee. Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application. In *Electron Devices Meeting, 1999. IEDM'99. Technical Digest. International*, pages 133–136. IEEE, 1999.

[72] Y.S. Chun, S. Chang, and S.Y. Lee. Effects of gate insulators on the performance of a-igzo tft fabricated at room-temperature. *Microelectronic Engineering*, 88(7):1590–1593, 2011.

[73] L. Lan and J. Peng. High-performance indium–gallium–zinc oxide thin-film transistors based on anodic aluminum oxide. *Electron Devices, IEEE Transactions on*, 58(5):1452–1455, 2011.

[74] C.H. Woo, C.H. Ahn, Y.H. Kwon, J.-H. Han, and H.K. Cho. Transparent and flexible oxide thin-film-transistors using an aluminum oxide gate insulator grown at low temperature by atomic layer deposition. *Metals and Materials International*, 18(6):1055–1060, 2012.

[75] J.K. Jeong, H. Won Yang, J.H. Jeong, Y.-G. Mo, and H.D. Kim. Origin of threshold voltage instability in indium-gallium-zinc

oxide thin film transistors. *Applied Physics Letters*, 93(12):123508–123508, 2008.

[76] S.-Y. Huang, T.-C. Chang, M.-C. Chen, S.-C. Chen, C.-T. Tsai, M.-C. Hung, C.-H. Tu, C.-H. Chen, J.-J. Chang, and W.-L. Liau. Effects of ambient atmosphere on electrical characteristics of al2o3 passivated ingazno thin film transistors during positive-bias-temperature-stress operation. *Electrochemical and Solid-State Letters*, 14(4):H177–H179, 2011.

[77] D.Y. Yoo, E. Chong, D.H. Kim, B.K. Ju, and S.Y. Lee. Effect of magnesium oxide passivation on the performance of amorphous indium–gallium–zinc-oxide thin film transistors. *Thin Solid Films*, 520(10):3783–3786, 2012.

[78] H.-S. Seo, J.-U. Bae, D.-H. Kim, Y. Park, C.-D. Kim, I.B. Kang, I.-J. Chung, J.-H. Choi, and J.-M. Myoung. Reliable bottom gate amorphous indium–gallium–zinc oxide thin-film transistors with tio x passivation layer. *Electrochemical and Solid-State Letters*, 12(9):H348–H351, 2009.

[79] W.-S. Kim, Y.-K. Moon, K.-T. Kim, J.-H. Lee, B.-D. Ahn, and J.-W. Park. An investigation of contact resistance between metal electrodes and amorphous gallium–indium–zinc oxide (a-gizo) thin-film transistors. *Thin Solid Films*, 518(22):6357–6360, 2010.

[80] J.-S. Park, J.K. Jeong, Y.-G. Mo, H.D. Kim, and S.-I. Kim. Improvements in the device characteristics of amorphous indium gallium zinc oxide thin-film transistors by ar plasma treatment. *Applied physics letters*, 90(26):262106–262106, 2007.

[81] A. Sato, R. Abe, K.and Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono. Amorphous in–ga–zn–o coplanar homojunction thin-film transistor. *Applied Physics Letters*, 94(13):133502–133502, 2009.

[82] D.H. Kang, I. Kang, S.H. Ryu, and J. Jang. Self-aligned coplanar a-igzo tfts and application to high-speed circuits. *Electron Device Letters, IEEE*, 32(10):1385–1387, 2011.

[83] S. Kim, J. Park, C. Kim, I. Song, S. Kim, S. Park, H. Yin, H.-I. Lee, E. Lee, and Y. Park. Source/drain formation of self-aligned top-gate amorphous gainzno thin-film transistors by< formula formulatype=. *Electron Device Letters, IEEE*, 30(4):374–376, 2009.

[84] S.-M. Park, K.-S. Lee, K.-C. Choi, H.-J. Lee, H.-S. Seo, C. Ha, B.-C. Kim, J.-W. Kim, and S-Y. Cha. Self-aligned bottom-gate amorphous igzo thin film transistor using the back side exposure technique. In *SID Symposium Digest of Technical Papers*, volume 44, pages 644–646. Wiley Online Library, 2013.

[85] K.-S. Son, J.-S. Jung, K.-H. Lee, T.-S. Kim, J.-S. Park, Y.-H. Choi, K.C. Park, J.-Y. Kwon, B. Koo, and S.-Y. Lee. Characteristics of double-gate ga–in–zn–o thin-film transistor. *Electron Device Letters, IEEE*, 31(3):219–221, 2010.

[86] H.W. Zan, W.T. Chen, C.C. Yeh, H.W. Hsueh, C.C. Tsai, and H.F. Meng. Dual gate indium-gallium-zinc-oxide thin film transistor with an unisolated floating metal gate for threshold voltage modulation and mobility enhancement. *Applied Physics Letters*, 98(15):153506–153506, 2011.

[87] K.-S. Son, J.-S. Jung, K.-H. Lee, T.-S. Kim, J.-S. Park, K.C. Park, J.-Y. Kwon, B. Koo, and S.-Y. Lee. Highly stable double-gate ga–in–zn–o thin-film transistor. *Electron Device Letters, IEEE*, 31(8):812–814, 2010.

[88] A. Suresh, P. Wellenius, V. Baliga, H. Luo, L.M. Lunardi, and J.F. Muth. Fast all-transparent integrated circuits based on indium gallium zinc oxide thin-film transistors. *Electron Device Letters, IEEE*, 31(4):317–319, 2010.

[89] B. Kim, H. N. Cho, W.S. Choi, S.-H. Kuk, Y.H. Jang, J.-S. Yoo, S.Y. Yoon, My. Jun, Y.-K. Hwang, and M.-K. Han. Highly reliable depletion-mode a-igzo tft gate driver circuits for high-frequency display applications under light illumination. *Electron Device Letters, IEEE*, 33(4):528–530, 2012.

[90] S. Sambandan and A. Nathan. Stable organic led displays using rms estimation of threshold voltage dispersion. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 53(9):941–945, 2006.

[91] J.-H. Lee, D.-H. Kim, D.-J. Yang, S.-Y. Hong, K.-S. Yoon, P.-S. Hong, C.-O. Jeong, H.-S. Park, S.Y. Kim, S.K. Lim, S.S. Kim, K.-S. Son, T.-S. Kim, J.-Y. Kwon, and S.-Y. Lee. World's largest (15-inch) xga amlcd panel using igzo oxide tft. In *SID Symposium Digest of Technical Papers*, volume 39, pages 625–628. Wiley Online Library, 2008.

[92] H. Luo, P. Wellenius, L. Lunardi, and J.F. Muth. Transparent igzo-based logic gates. *Electron Device Letters, IEEE*, 33(5):673–675, 2012.

[93] B. Kim, C.-I. Ryoo, S.-J. Kim, J.-U. Bae, H.-S. Seo, C.-D. Kim, and M.-K. Han. New depletion-mode igzo tft shift register. *Electron Device Letters, IEEE*, 32(2):158–160, 2011.

[94] H. Ozaki, T. Kawamura, H. Wakana, T. Yamazoe, and H. Uchiyama. 20-μw operation of an a-igzo tft-based rfid chip using purely nmos "active" load logic gates with ultra-low-consumption power. In *VLSI Circuits (VLSIC), 2011 Symposium on*, pages 54–55. IEEE, 2011.

[95] C. Zysset, N.S. Münzenrieder, T. Kinkeldei, K.H. Cherenack, and G. Tröster. Indium-gallium-zinc-oxide based mechanically flexible transimpedance amplifier. *Electronics letters*, 47(12):691–692, 2011.

[96] J.B. Kim, C. Fuentes-Hernandez, D.K. Hwang, W.J. Potscavage Jr, H. Cheun, and B. Kippelen. Vertically stacked hybrid organic–inorganic complementary inverters with low operating voltage on flexible substrates. *Organic Electronics*, 12(1):45–50, 2011.

[97] T.-C. Huang, K. Fukuda, C.-M. Lo, Y.-H. Yeh, T. Sekitani, T. Someya, and K.-T. Cheng. Pseudo-cmos: A design style for low-cost and robust flexible electronics. *Electron Devices, IEEE Transactions on*, 58(1):141–150, 2011.

[98] M.J. Seok, M.H. Choi, M. Mativenga, D. Geng, D.Y. Kim, and J. Jang. A full-swing a-igzo tft-based inverter with a top-gate-bias-induced depletion load. *Electron Device Letters, IEEE*, 32(8):1089–1091, 2011.

[99] R. Martins, A. Nathan, R. Barros, L. Pereira, P. Barquinha, N. Correia, R. Costa, A. Ahnood, I. Ferreira, and E. Fortunato. Complementary metal oxide semiconductor technology with and on paper. *Advanced Materials*, 23(39):4491–4496, 2011.

[100] H.Y. Li, L.H. Guo, W.Y. Loh, L.K. Bera, Q.X. Zhang, N. Hwang, E.B. Liao, K.W. Teoh, H.M. Chua, Z.X. Shen, C.K. Cheng, G.-Q. Lo, N. Balasubramanian, and D.-L Kwong. Bendability of single-crystal si mosfets investigated on flexible substrate. *Electron Device Letters, IEEE*, 27(7):538–541, 2006.

[101] K.H. Cherenack, N.S. Münzenrieder, and G. Tröster. Impact of mechanical bending on ZnO and IGZO thin-film transistors. *Electron Device Letters, IEEE*, 31(11):1254–1256, 2010.

[102] D.I. Kim, B.U. Hwang, J.S. Park, H.S. Jeon, B.S. Bae, H.J. Lee, and N.-E. Lee. Mechanical bending of flexible complementary inverters based on organic and oxide thin film transistors. *Organic electronics*, 13(11):2401–2405, 2012.

[103] T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya. Flexible organic transistors and circuits with extreme bending stability. *Nature materials*, 9(12):1015–1022, 2010.

[104] W.J. Yu, S.Y. Lee, S.H. Chae, D. Perello, G.H. Han, M. Yun, and Y.H. Lee. Small hysteresis nanocarbon-based integrated circuits on flexible and transparent plastic substrate. *Nano letters*, 11(3):1344–1350, 2011.

[105] P.I. Hsu, R. Bhattacharya, H. Gleskova, M. Huang, Z. Xi, Z. Suo, S. Wagner, and J.C. Sturm. Thin-film transistor circuits on large-area spherical surfaces. *Applied physics letters*, 81(9):1723–1725, 2002.

[106] T. Kinkeldei, N. Münzenrieder, C. Zysset, K. Cherenack, and G. Tröster. Encapsulation for flexible electronic devices. *Electron Device Letters, IEEE*, 32(12):1743–1745, 2011.

[107] S.D. Brotherton. Tfts on flexible substrates. In *Introduction to Thin Film Transistors*, pages 407–451. Springer, 2013.

[108] A. Pecora, L. Maiolo, F. Maita, and A. Minotti. Flexible pvdf-trfe pyroelectric sensor driven by polysilicon thin film transistor fabricated on ultra-thin polyimide substrate. *Sensors and Actuators A: Physical*, 2012.

[109] L. Zhang, H. Wang, Y. Zhao, Y. Guo, W. Hu, G. Yu, and Y. Liu. Substrate-free ultra-flexible organic field-effect transistors and five-stage ring oscillators. *Advanced Materials*, 2013.

[110] X. Liu, C. Wang, B. Cai, X. Xiao, S. Guo, Z. Fan, J. Li, X. Duan, and L. Liao. Rational design of amorphous indium zinc oxide/carbon nanotube hybrid film for unique performance transistors. *Nano letters*, 12(7):3596–3601, 2012.

[111] N.C. Woo, K. Cherenack, G. Tröster, and R. Spolenak. Designing micro-patterned ti films that survive up to 10% applied tensile strain. *Applied Physics A*, 100(1):281–285, 2010.

[112] K. Cherenack and G. Tröster. The path towards woven thin-film transistors. In *MRS Proceedings*, volume 1256. Cambridge Univ Press, 2010.

[113] R.M. Erb, K.H. Cherenack, R.E. Stahel, R. Libanori, T. Kinkeldei, N. Münzenrieder, G. Tröster, and A.R. Studart. Locally reinforced polymer-based composites for elastic electronics. *ACS Applied Materials & Interfaces*, 4(6):2860–2864, 2012.

[114] C. Zysset, N. Münzenrieder, T. Kinkeldei, K. Cherenack, and G. Tröster. Woven active-matrix display. *Electron Devices, IEEE Transactions on*, 59(3):721–728, 2012.

2

Thesis Summary

2.1 Contributions

2.1.1 Flexible IGZO TFTs

Thin-film transistors (TFTs) based on Indium-Gallium-Zinc-Oxide (IGZO) have been fabricated on free standing polyimide foil. Their device structure and electrical properties are described in the following section. Additionally, possibilities to improve the performance of these TFTs are presented.

a) Device structure

The inverted-staggered and passivated bottom-gate TFT geometry used to fabricate flexible IGZO transistors is shown in Fig.2.1. If not mentioned otherwise all TFTs presented in this thesis are fabricated by standard UV lithography using five photolithography masks, and are based on the following materials:

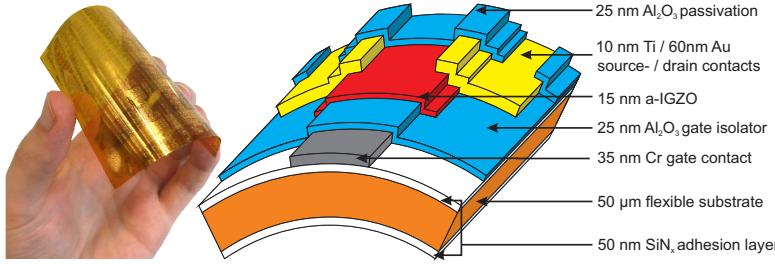

Figure 2.1: Photograph of a fully processed flexible substrate with IGZO TFTs, and schematic cross section of the passivated, inverted-staggered, bottom-gate IGZO TFTs.

As substrate a 50 µm thick polyimide foil (Kapton E from DuPont) was used.

50 nm thick PECVD deposited SiN_x layers on both sides of the substrate increased the adhesion between the substrate and all other material layers, and also reduced the outgassing of the substrate during the fabrication process.

Since Chromium provides a better adhesion than the most other metals, and can easily be structured by wet etching, evaporated Cr was used to fabricate the 35 nm thick bottom gate contact.

As gate insulator 25 nm ALD deposited Al_2O_3 was used. This material layer is conformal, provides a high dielectric constant (ϵ_r =9.5) and a low pinhole density. The ALD deposition temperature of 150 °C is the highest temperature during the TFT fabrication process.

Room temperature RF magnetron sputtered 15 nm thick amorphous IGZO served as semiconductor.

Source and drain contacts were made from evaporated 10 nm Ti and 60 nm Au. Here, Ti acts as adhesion layer and Au provides a high electrical conductivity.

Passivation of the device was done by additional 25 nm ALD deposited Al_2O_3.

The manufacturing process is described in section 5.2 (page 123), and was optimized concerning: device performance, low temperature fabrication, thicknesses of brittle material layers, and adhesion between different material layers aiming at electrical performance, long term reliability and bendability.

b) Electrical performance of flexible IGZO TFTs

IGZO TFTs have been electrically characterized according to their DC performance (e.g. **chapter five**, page 121), stability (**chapter three**, page 83), capacitance, and AC performance (both **chapter ten**, page 203).

IGZO TFT DC performance: Typical I_{DS}-V_{GS} transfer and I_{DS}-V_{DS} output characteristics of an IGZO TFT with a W/L ratio of 280 µm/10 µm, measured under ambient conditions, are shown in Fig. 2.2. Based on this measurements a linear field effect mobility μ_{lin} of 15 $cm^2V^{-1}s^{-1}$, a saturation field effect mobility μ_{sat} of 15 $cm^2V^{-1}s^{-1}$, a threshold voltage V_{th} of 1 V, an on/off current ratio $>9 \times 10^8$, a subthreshold swing (inverse of the subthreshold slope) SS of 120 mV/decade, and a transconductance g_m (at V_{GS} =5 V) of 650 µS was extrapolated using the Shichman–Hodges model of the TFT current.

The following two paragraphs describe the improvement of the IGZO TFT DC performance (higher transconductance, smaller subthreshold swing) by an increase of the transistor channel capacitance. The channel capacitance can be increased by the use of a gate insulator with a higher dielectric constant, or by a change of the geometrical properties (thinner insulator thickness, higher effective area). Since

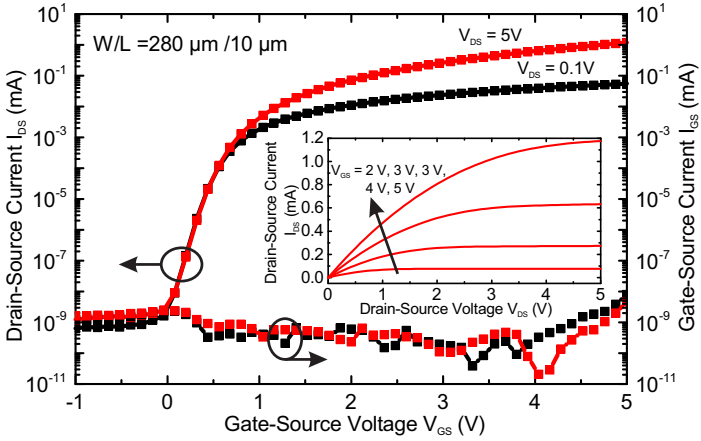

Figure 2.2: Typical IGZO TFT transfer characteristic measured at source–drain voltages of 0.1 V (linear regime) and 5 V (saturation regime). The inset shows the corresponding output characteristic.

Al_2O_3 already exhibits a ϵ_r of 9.5, and also forms a low trap density interface with IGZO [1], the geometry of the TFTs was changed.

Reduction of the gate insulator thickness: The high conformability, and low pinhole density of ALD deposited Al_2O_3 allows the fabrication of flexible IGZO TFTs with a gate insulator thickness of only 10 nm which is demonstrated in **chapter three** (page 83). Compared to TFTs with a 25 nm thick gate insulator (Fig. 10.4, page 208) TFTs with 10 nm Al_2O_3 exhibit a by a factor 2.7 increased gate capacitance (9.4 fFμm^{-2} instead of 3.4 fFμm^{-2}). The resulting reduction of the subthreshold swing to 84 mV/decade is shown in Fig. 2.3.

Flexible double gate TFTs: Since a further decrease of the gate insulator thickness (below 10 nm) is expected to increase the gate leakage current and decrease the yield, the double gate concept (described in **chapter three**, page 83) was applied to flexible IGZO TFTs. The bottom and the top gate were electrically connected to form an IGZO TFT controllable with a single gate voltage, and thereby ensures comparability with standard TFT designs. The inset of Fig. 2.4 shows the modified device structure. The increased gate area of the double gate TFTs results

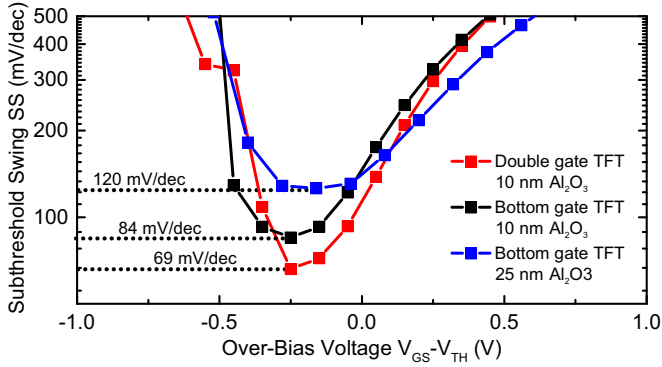

Figure 2.3: Extracted subthreshold swing $(\partial \log I_{DS}/\partial V_{GS})^{-1}$ of flexible IGZO TFTs with 25 nm and 10 nm thick Al_2O_3 gate insulator, as well as of double gate TFTs.

in a gate capacitance C_G of 17.1 fFμm^{-2} in the on regime. At the same time, the gate capacitance of the corresponding bottom gate reference TFT, with identical layer structure, is 9.4 fFμm^{-2}. This corresponds to an by ≈78 % increased C_G of the double gate TFT, as shown in Fig. 3.4 (page 90). This capacitance increase results in a subthreshold swing of 69 mV/decade (also shown in Fig. 2.3).

The transconductance values $g_m = \partial I_{DS}/\partial V_{GS}$ of a bottom gate TFT and a double gate TFT are shown in Fig. 2.4. The Figure also shows the transconductance ratio between the two TFTs. The increased gate capacitance due to the additional top gate, increases g_m from 364 μS to 700 μS. This corresponds to an increase of ≈92 %.

IGZO TFT AC performance: **Chapter ten** (page 203) describes that for numerous applications, such as flexible radios the speed of the utilized TFTs is a crucial parameter. One possibility to quantify the AC performance of a field-effect transistor is the transit frequency f_t which is defined as the unity gain frequency of the small-signal current gain h_{21} [2]:

$$f_t = \frac{g_m}{2 \cdot \pi \cdot C_G} \propto \frac{\mu_{FE}}{L \cdot (L + L_{OV})}$$

Here, g_m is the transconductance of the TFT, C_G the gate capacitance, μ_{FE} the effective mobility, L the channel length, and L_{OV} the

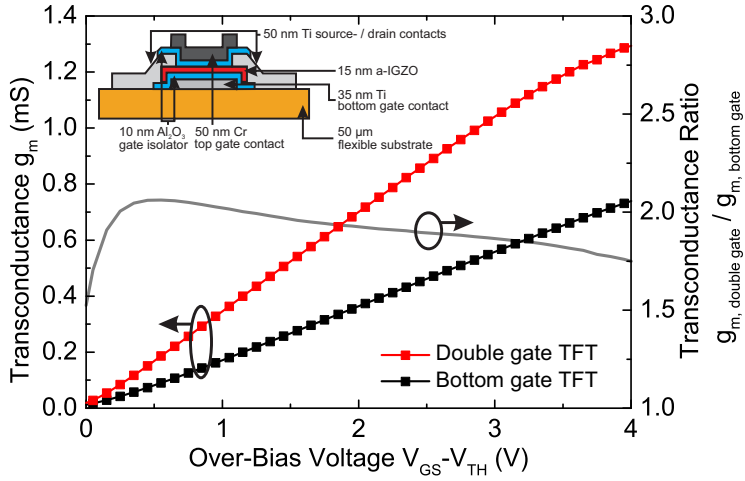

Figure 2.4: Transconductance of an IGZO double gate TFT, and a bottom gate TFT (with identical layer structure), and the ratio between the transconductance values of double and bottom gate TFT. The W/L ratio is 280 µm/10 µm. The inset shows the device structure.

gate to source /drain overlap length. L_{OV} is important since it determines the parasitic gate to source /drain overlap capacities and thereby contributes to the gate capacitance.

While the mobility is determined by the IGZO semiconductor, the structure sizes of the TFT have to account for the deformation of the free-standing plastic substrate during the fabrication process (a substrate expansion of ≈25 µm was observed on a 7.6 cm × 7.6 cm polyimide foil). These deformations require tolerances in the order of 10 µm on the photolithography masks, and thereby limit the minimum gate to source /drain overlap length to similar values.Additionally, the minimum feature size achievable by conventional photolithography (using glass photolithography masks and a mask aligner) on flexible substrates limits the channel length of flexible TFTs [3] to values >2 µm, leading to maximum f_t values of flexible IGZO TFTs in the order of 10 MHz [4].

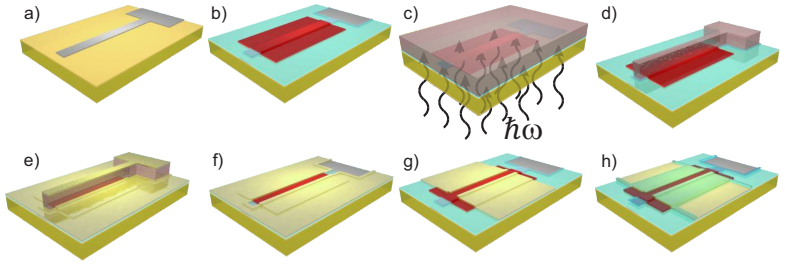

Figure 2.5: Manufacturing process flow of flexible, self-aligned IGZO TFTs. a) deposition and structuring of the Ti gate, b) deposition and structuring of the Al_2O_3 gate insulator and the IGZO semiconductor, c) backside illumination of photoresist, d) resist development, e) evaporation of the Cr /Au top metallization, f) channel structuring by lift-off, g) top metallization etching, h) Al_2O_3 passivation deposition and structuring.

TFTs with self-aligned source and drain contacts[1]**:** Self-alignment using backside illumination through the polyimide substrate is one possibility to perform a layer structuring without critical photolithography mask alignment steps. Thereby, self-alignment techniques overcome the problems related to the deformation of flexible substrates, and are able to reduce the channel length and the gate to source /drain overlaps in large area TFT fabrication on flexible foils [5, 6], resulting in higher TFT frequencies.

Self-aligned IGZO TFTs on flexible polyimide foil were manufactured as follows: First, a 50 nm thick SiN_x adhesion and a 35 nm thick Ti gate contact (Fig. 2.5a) were fabricated. Next, 25 nm of Al_2O_3 (ALD), and 15 nm of IGZO (RF magnetron sputtering) were deposited, and structured by conventional photolithography (Figure 2.5b). Here, a mask aligner was used to align the glass photolithography masks on the substrate. To structure the TFT channel by self-alignment positive photoresist was spin-coated and illuminated through the back of the semitransparent substrate. Here, the predefined, metallic gate contacts acted as photolithography mask (Fig. 2.5c). Because of the limited

[1]This section is based on: N. Münzenrieder, C. Zysset, L. Petti, T. Kinkeldei, G.A. Salvatore, and G. Tröster, Flexible self-aligned amorphous InGaZnO thin-film transistors with sub-micrometer channel length and a transit frequency of 135 MHz. In *IEEE Transactions on Electron Devices*, 60 (9), pages 2815–2820, 2013.

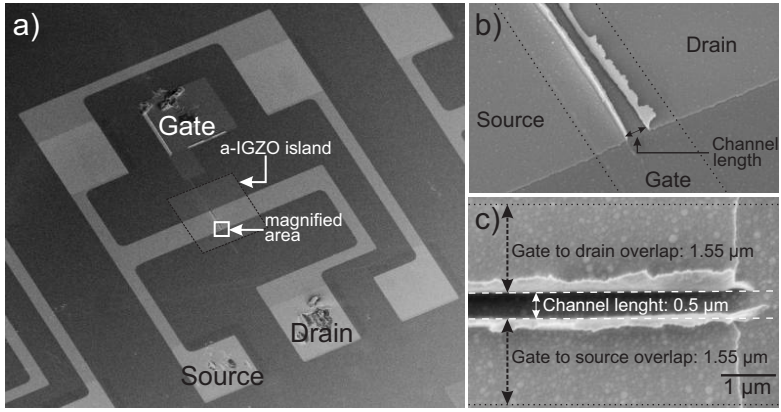

Figure 2.6: a) SEM micrograph of a complete flexible IGZO TFT illustrating the employed Ground-Signal-Ground layout of the contact pads. Damages of the contact pads originate from previous probe tip placement. b) Enlargement of the channel region showing the lift-off edges of the self-aligned source and drain contacts. (The sample was tilted by ≈35 °C inside the SEM), c) top view of the channel, used to determine the exact channel length and gate to source /drain overlaps.

transmittance of polyimide (absorbance ≈200 cm^{-1} at a wavelength of 405 nm [7]), the required illumination time, using the available UV lamp, was 5 min. After the resist development a strip of photoresist remained on top of the gate contact (Figure 2.5d). Since no glass photolithography mask alignment was necessary, no misalignment of the resist strip can occur. Following the self-aligned lithography, 10 nm Cr and 60 nm Au were deposited (e^--beam evaporation) on the substrate (Fig. 2.5e). A lift-off was performed to remove the self-aligned photoresist and the Cr /Au metallization on top of the TFT gate electrodes, and thereby define the TFT channel (Fig. 2.5f). The width of the TFTs and the contact pads were structured by conventional lithography (glass photolithography mask and mask aligner) and wet etching (Fig. 2.5g). The fabrication process was finalized by the deposition and structuring of a 25 nm thick Al_2O_3 passivation layer (Fig. 2.5h).

A SEM micrograph of a complete TFT illustrating the employed Ground-Signal-Ground (GSG) layout is shown in Fig. 2.6a. Magnifica-

tions of the channel region (Fig. 2.6b and 2.6c) show the dimensions of the TFT channel. The TFTs have a channel length of 0.5 µm (± ≈15 %) and a gate to source /drain overlap of 1.55 µm. The overlap is caused by the fact that the resist strip, structured by self-alignment, is narrower than the gate contact itself. This is a result of the light scattering in the resist, and the partially inhomogeneous light source used for backside exposure. The Cr /Au residuals besides the TFT channel are a result of the lift-off using the trapezoidal shaped self-aligned photoresist, but do not harm the TFT operation. The 0.5 µm long, self-aligned TFTs exhibits an effective mobility of 7.5 $cm^2V^{-1}s^{-1}$, a threshold voltage of 0 V, a subthreshold swing of 0.13 V/decade and an on-off current ratio $>10^9$. Compared to a 10 µm long TFT fabricated with conventional photolithography (page 39), the effective mobility and the threshold voltage are reduced. This is due to the following reasons: First, the smaller channel resistance of the 0.5 µm long self-aligned TFT increases the relative influence of the contact resistance and thereby reduces the effective mobility. Second, the drain-induced barrier lowering shifts the threshold voltage of the self-aligned short channel TFT to smaller gate voltages.

If self-aligned TFTs are compared to flexible IGZO transistors fabricated using conventional lithography a decrease of the gate to source /drain overlap length and therefore the total gate capacitance was observed. Fig. 2.7 compares the normalized gate capacitance of a self-aligned and a conventional flexible IGZO TFT. Since conventional TFTs with channel length <1 µm could not be fabricated on polyimide foil, both TFTs have a channel length of 1 µm. Self-alignment decreased the total gate to source /drain overlap from 8 µm to 3.1 µm, this corresponds to a reduction of the total gate length (channel length and gate to source /drain overlaps) by 54 %. The gate capacitance is reduced from 55 fF μm^{-1} to 41 fF μm^{-1} (-26 %). The difference between gate length reduction, and gate capacitance reduction can be explained by fringe effects, e.g. caused by the Cr /Au residuals besides the TFT channel.

The AC characteristic of the shortest fabricated self-aligned TFTs (channel length 0.5 µm) was characterized by S-parameter measurements. Fig. 2.8a shows a photograph of a tensile bent substrate (r =3.5 mm) connected to a network analyzer, including a micrograph of a bent TFT contacted with 2 GSG probe tips. The current-gain h_{21} of a TFT measured while flat and bent is plotted in Figure 2.8b. From this plot, the transit frequency of the self-aligned flexible IGZO TFTs

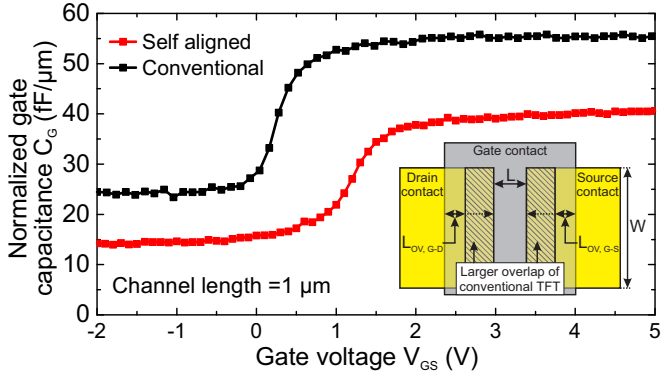

Figure 2.7: Gate capacitance of flexible TFTs (fabricated using self-alignment and conventional lithography). The reduced gate overlap (inset) of self-aligned TFTs leads to a decrease of the overlap capacities and therefore to a decrease of the total gate capacitance.

(unity gain frequency of $|h_{21}|$) was extracted to be 135 MHz in the flat case, and 138 MHz while bent to a radius of 3.5 mm ($\epsilon \approx 0.7$ %). The demonstrated frequency performance enables flexible electronic applications, in frequency domains hardly achievable with conventionally fabricated IGZO TFTs.

Self-aligned double gate TFTs: While a double gate structure can improve the DC performance of flexible IGZO TFTs, self-alignment of the source and drain contacts is a suitable way to decrease the parasitic overlap capacities and thereby enable higher transit frequencies. A combination of the self-alignment and double gate approaches promises to enable flexible IGZO TFTs with superior DC and AC behavior. Since the bottom and the top gate of a double gate TFT contribute to the gate capacitance in the same way, all lithography steps influencing the source /drain to (bottom and top) gate overlaps have to be done by self-alignment. In the case of flexible IGZO TFTs this calls for self-aligned source, drain and top gate contacts. Self-alignment of the top gate contact using negative photoresist and backside alignment requires transparent source and drain contacts (including transparent source /drain contact pads and interconnections), otherwise the top gate contact would form parasitic overlap capacities with the source

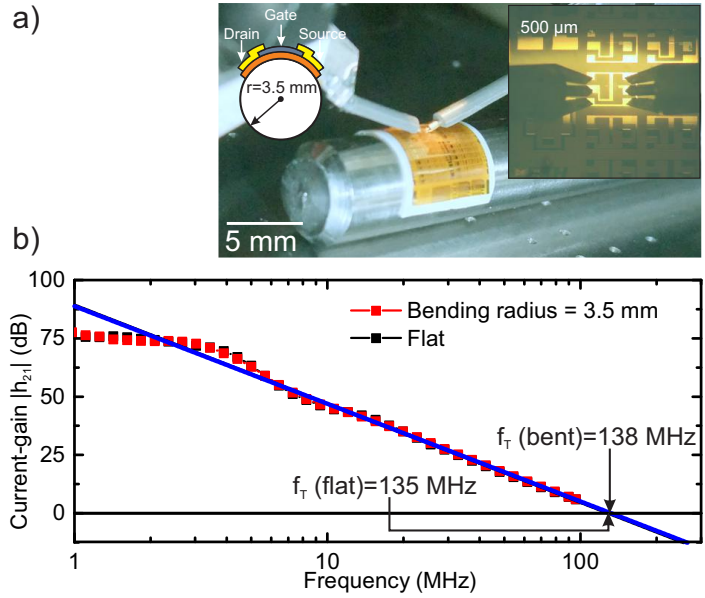

Figure 2.8: a) Photograph of a polyimide substrate bent to a tensile radius of 3.5 mm parallel to the TFT channel, and prepared for AC characterization. A single bent TFT contacted by 2 GSG probe tips is shown in the inset. b) Absolute value of h_{21} extracted from S-parameter measurements conducted on a flat TFT (channel length: 0.5 µm), and subsequently bent to a tensile radius of 3.5 mm ($\epsilon \approx 0.7\,\%$).

/drain metallization. Therefore, the metallic source /drain contacts have been replaced by transparent and conducting Indium-Tin-Oxide (ITO). ITO was deposited by room temperature RF magnetron sputtering. With the exception of the ITO source /drain contacts, the first part of the self-aligned double gate TFTs fabrication was identical to the self-aligned TFT fabrication described in the previous section (page 43), whereas the 25 nm thick Al_2O_3 device passivation was used as second gate insulator for the self-aligned 60 nm thick Cu top gate. The complete device structure is shown in Fig. 2.9a. Additionally, the ITO source and drain contact pads have been coated with 50 nm of Ti to improve the electrical contact during the TFT characterization.

Characteristics of a self-aligned double TFT, and a bottom gate

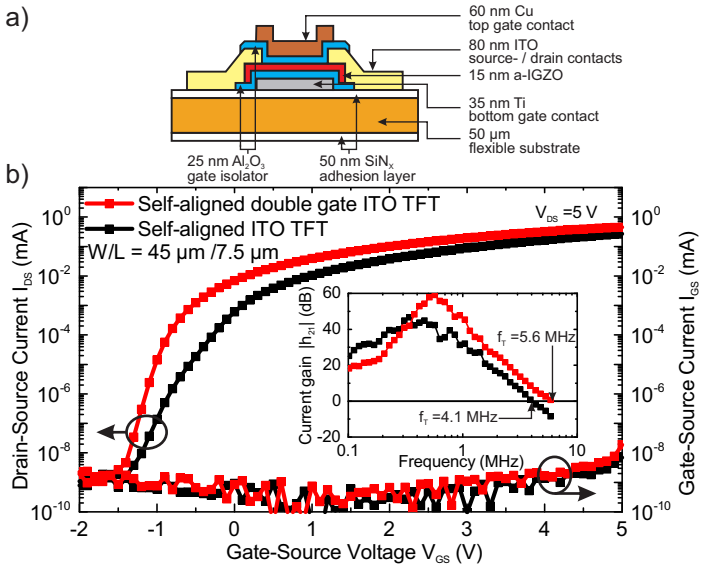

Figure 2.9: a) Schematic of a self-aligned double gate IGZO TFT with transparent ITO source /drain contacts. b) Transfer characteristics of a self-aligned double and bottom gate TFT, both fabricated on the same substrate using ITO source /drain contacts. The inset shows the corresponding current gain measurements.

TFT with similar device structure (W/L ratio =45 µm/7.5 µm), both fabricated on the same substrate are shown in Fig. 2.9b. The graph shows the transfer characteristics measured in the saturation regime and visualizes the improved device performance of the double gate TFT: Maximum transconductance is increased from 82 µS to 138 µS (+68 %), and subthreshold swing is decreased from 172 mV/decade to 109 mV/decade (-37 %).

The parasitic gate overlap capacitance is as low as 6.2 fF µm^{-1}, in contrast to 320 fF µm^{-1} for non-self-aligned double gate TFTs with 10 nm Al_2O_3 gate insulator (Fig. 3.4, page 90). Therefore self-aligned double gate TFTs are able to operate in the megahertz regime. This is demonstrated in the inset of Fig. 2.9b, were the self-aligned double gate TFT exhibits an transit frequency of 5.6 MHz (this value is nearly identical to a self-aligned bottom gate TFT with similar gate length,

see also page 49).

Additionally, the self-aligned double gate TFTs stay fully functional while bent, whereas the high brittleness of the ITO contacts limits the minimum bending radius to values around 6 mm (ϵ =0.4 %).

Scaling: An overview of the effect of channel length scaling on the transit frequency is given in Fig. 2.10. Here, self-aligned bottom and double gate TFTs are compared to conventionally fabricated bottom gate IGZO TFTs (page 205) with different gate to source /drain overlaps. A reduction of the gate to source /drain overlap and the channel length to 4 µm and 1 µm increases the transit frequency of conventional (non-self-aligned) IGZO TFTs to 48 MHz. Within this thesis conventional IGZO TFTs with channel length <1 µm were not fabricated on free standing plastic foil, and was to our knowledge also not reported in the past. Self-alignment could be used to fabricate TFTs with a channel length of 0.5 µm and a transit frequency of 135 MHz.

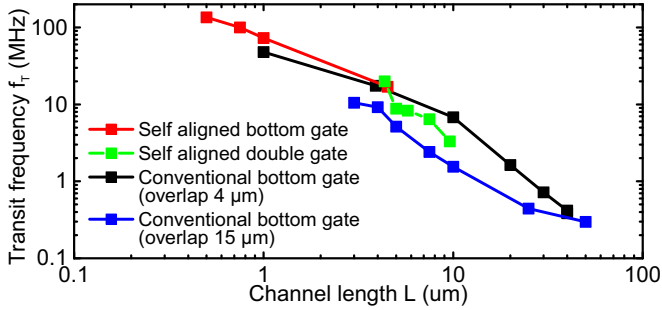

Figure 2.10: Influence of channel length scaling on the measured transit frequency of conventionally fabricated flexible IGZO TFTs with different source /drain overlaps, flexible self-aligned TFTs, and flexible self-aligned double gate TFTs with ITO source and drain contacts. Due to the different TFT characteristics, different bias points had to be used to maximize f_t, whereas all measurement where performed in the saturation region.

Measurements on flexible IGZO TFTs with different channel length also show two constrains:

- The measured f_t values in Fig. 2.10 do not follow a $1/L^2$ relation expected from an ideal transistor which exactly follows the Shichman–Hodges model and has no parasitic capacities. This is due to the overlap capacities, but also because of the source and drain contact resistances. The extracted contact resistance is $66\,k\Omega\,\mu m^{-1}$ (conventional TFTs), and $290\,k\Omega\,\mu m^{-1}$ (self-aligned bottom gate TFTs). This increase is due to the following reasons: First, the from $15\,\mu m$ /$4\,\mu m$ to $1.55\,\mu m$ decreased contact area (identical to the gate to source and drain overlaps) of self-aligned TFTs, and second a higher IGZO surface contamination under the source /drain metallization (in particular resist leftovers) caused by the self-aligned lithography. The contact resistance (which is independent from the channel length) leads to a reduction of the effective mobility in short channel TFTs and therefore to a less distinguished increase of f_t. The even higher contact resistance of self-aligned double gate TFTs with ITO contacts also limits their performance.
- Short channel effects decrease the output resistance g_{ds} of flexible IGZO TFTs with decreasing channel length (independent of the fabrication method). This leads to the fact that the g_m/g_{ds} ratio of self-aligned bottom gate TFTs is degraded from ≈40 (channel length $10\,\mu m$) to values around 2 for TFTs with channel length $<1\,\mu m$. A small g_m/g_{ds} ratio complicates the circuit design and limits the e.g. the gain of amplifiers.

2.1.2 Bendability of flexible IGZO TFTs

A method to characterize flexible TFTs under mechanical strain is presented. The influence of strain on the electrical performance and the mechanical stability of flexible IGZO TFTs are discussed. Finally methods to improve the flexibility and to enable smaller bending radii of flexible IGZO TFTs are investigated.

a) Measurement of IGZO TFTs under strain

To characterize TFTs on flexible plastic foils while bent to arbitrary tensile and compressive radii a custom build bending tester (Fig. 2.11) was used. This bending tester is described in **chapter four** (page 107).

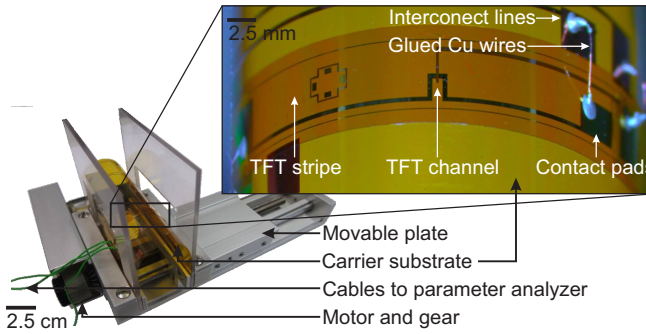

Figure 2.11: Custom-built bending tester with a loaded carrier substrate and close up of the attached flexible TFT bent to a radius of ≈8 mm. The TFT is loaded to apply tensile strain parallel to the length of the channel.

To simplify the mounting process of TFTs in the bending tester, and to exclude any influence of the contacts on the mechanical properties of the TFT channel, the TFTs for the bending tests were fabricated in a special stripe layout (Fig. 4.3, page 113): The TFT stripes (32 at the same time) were fabricated on a 7.6 cm × 7.6 cm polyimide foil. Each stripe had a size of (34.5 mm × 4.75 mm). The TFT channel is located in the center of the stripe, three contact pads for the source, drain, and gate contacts (size ≈3 mm × 3 mm) are fabricated at the edges of the stipe. Therefore the distance between contact pads and the TFT channel was ≈1 cm. To perform the measurement, a single TFT stripe was cut from the fabrication substrate and attached to a flexible carrier substrate (using double sided tape). An electrical contact between the pads of the TFT and interconnect lines on the carrier substrate was made with glued Cu wires. The interconnect lines on the carrier substrate itself were connected with a HP4156A parameter analyzer. The large distance between channel region and contact pads ensures that the mechanical properties of the TFT are not influenced by the measurement setup or the glued wires. Next, the carrier substrate is mounted between the two movable plates of the bending tester. The substrate has to be inserted with the TFT facing upwards to apply tensile strain and facing downwards to apply compressive one. A change of the plate distance enables bending radii from infinity (flat substrate) down to values <1 mm (this corresponds to mechanical strain >3.5 %

in the described TFTs). The actual bending radius was monitored with a CCD camera.

b) Influence of mechanical strain on flexible IGZO TFTs

The bending setup described in section 2.1.2a) (page 50) was used to evaluate the influence of mechanical strain on flexible IGZO TFTs. It was found that the influence of mechanical strain on IGZO TFTs depends on the direction of the applied strain, the illumination condition as well as the time scale.

Direction of applied strain: The geometrical alignment of the strain influences its impact on flexible IGZO TFTs. Here two cases have to be considered:

- Strain can be applied in tensile (positive strain under outward bending) or in compressive (negative strain under inward bending) direction.
- Strain can be applied parallel or perpendicular to the TFT channel and therefore parallel or perpendicular to the current flow (Bending in arbitrary directions relative to the channel is a superposition of parallel or perpendicular bending).

Tensile and compressive strain: The influence of bending parallel to the TFT channel on the normalized effective mobility μ_{FE} and the shift of the threshold voltage ΔV_{th} are illustrated in Fig. 2.12. A more detailed explanation can also be found in **Chapter five** (page 121). Under tensile strain the IGZO TFTs, described in section 2.1.1a) (page 38) stay functional down to a bending radius of ≈4mm (ϵ ≈+0.6 %). At this bending radius an increase of μ_{FE} by ≈4 % and a decrease of the threshold voltage by ≈80 mV was observed. At the same time the TFTs stay operational down to a radius of ≈1.1 mm (ϵ ≈-2.2 %) when exposed to compressive strain. Here a decrease of μ_{FE} by ≈-8 % and an increase of the threshold voltage by ≈90 mV was measured.

Since tensile /compressive strain modifies the distance between the atoms, the changes of effective mobility and threshold voltage can be explained by a decrease /increase of the energy level splitting ΔE of the binding and antibinding orbitals between the atoms in the semiconducting layer [8]. This changes the carrier density and causes a threshold voltage shift in the observed directions. The increase and

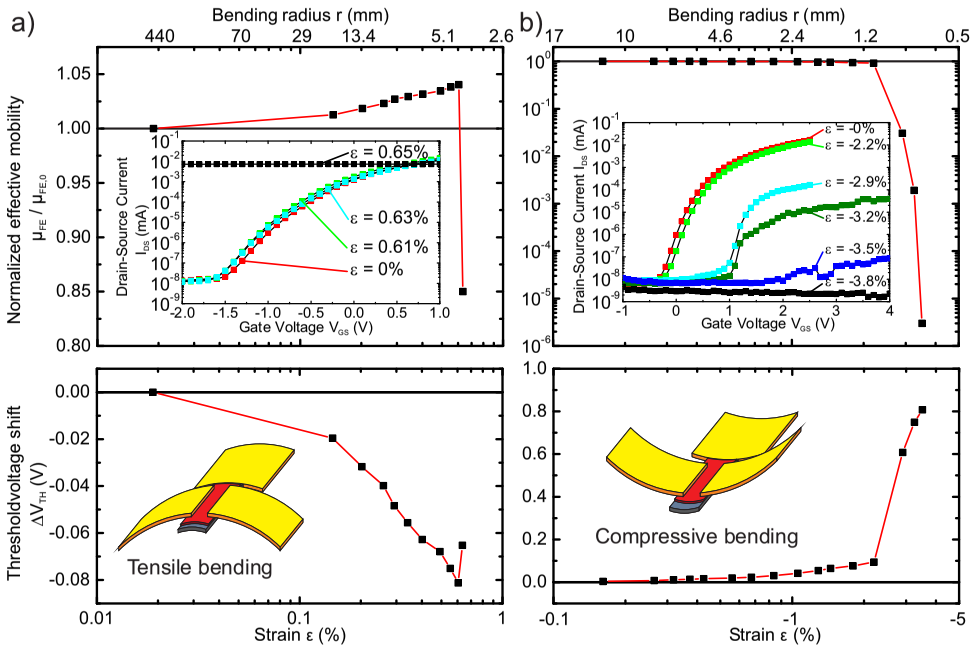

Figure 2.12: Influence of bending (parallel to the TFT channel) flexible IGZO TFTs in tensile (a) and compressive (b) direction on the effective mobility and the threshold voltage (W/L ratio =280 μm/115 μm and 280 μm/60 μm). The insets show the degeneration of the corresponding transfer characteristics at high strain values.

decrease of the effective mobility can be explained by a change of the electron-lattice interaction due to variations of the inter atomic distance, which results in a change of the effective mass m^* (k·p method [9]) and affects the mobility.

At smaller bending radii the formation of cracks perpendicular to the applied strain causes a degeneration of the TFT performance (see insets of Fig. 2.12) resulting in a drop of the effective mobility by several orders of magnitude and an increase of the threshold voltage. The direction of this crack induced shifts are independent of the direction of the strain (tensile /compressive).

Bending parallel and perpendicular to the TFT channel: Figure 2.13 shows a typical evolution of the TFT effective field-effect mobility versus mechanical strain induced by tensile bending of the substrate. Strain was applied parallel and perpendicular to the TFT channel (W/L = 280 µm/35 µm). Parallel bending increases the mobility until the TFT is destroyed above 0.72 % strain (ϵ). Perpendicular bending at the same time only slightly increases the mobility for small values of strain (≈0.3 %) but leads to a strong mobility degradation if the strain is increased above ≈0.3 %.

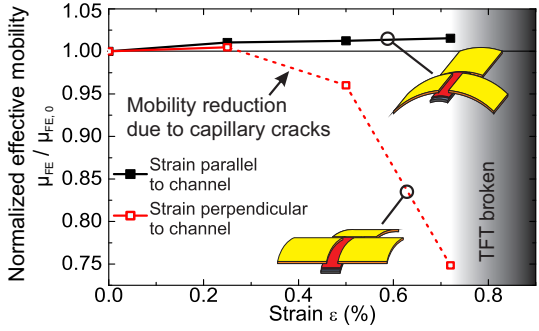

Figure 2.13: Typical effective mobility changes caused by tensile stain induced by bending. As indicated by the insets, strain was applied parallel and perpendicular to the IGZO TFT channel.

The performance degradation of TFTs exposed to perpendicular stains >0.3 % is caused by the formation of capillary cracks, perpendicular to the applied mechanical strain. The average width of the

cracks measured while the substrate was bent to a radius of 3.5 mm was ≈90 nm. The cracks propagate through the chromium (gate contact), IGZO (semiconductor), and Al_2O_3 (gate insulator, passivation) layers. Ductile gold contacts are only damaged in areas where they are covered with Al_2O_3. We measured an average distance between two neighboring capillary cracks of ≈100 µm, but in approximately 50 % of all cases, only one crack within one TFT channel was visible in the SEM. Therefore, and because the width of the TFT channels is larger than their length, capillary cracks in the tested glsglos:TFTs occurred only during bending perpendicular to the channel. Consequently, perpendicular bending disconnects a part of the gate, which explains the reduction of the effective mobility by the reduced effective W/L ratio. Reflattening reestablishes the electrical contact between the separated parts of the gate contact, and the original W/L ratio, as well as the original device performance is recovered. Independent from perpendicular or parallel bending, bending to radii smaller than 3.5 mm (ϵ >0.72 %) leads to extended cracks, causing short circuits between different material layers, and permanently destroys the TFTs.

Influence of light on the bending performance: The effect of bending IGZO TFTs with and without illumination (90 lx) on the effective field effect mobility and the threshold voltage is shown in Fig. 2.14, see also **chapter five** (page 121). In darkness the effective mobility changes by +3.1 % (-1.8 %) and V_{th} is modified by -15 mV (+19 mV) under tensile (compressive) bending down to a radius of 8 mm (ϵ ≈0.3 %). Since the TFTs are not damaged at a bending radius of 8 mm, the TFTs can be reflattened after bending. As seen in Fig. 2.14 reflattening leads to a recovery of the performance parameters to their initial values. Under illumination, the response of the IGZO TFTs to mechanical strain changes: Here μ_{FE} varies by +14.8 % (-3.7 %) and V_{th} is changed by -110 mV (+37 mV) under tensile (compressive) strain. This measurements represent an increase of the influence of strain up to a factor >5 (compared to the measurement in darkness). Additionally, the relaxation behavior of the effective mobility and the threshold voltage is modified: Under illumination μ_{FE} and V_{th} remain nearly constant at the values they reached at the maximum strain even when the strain is reduced to 0 % after bending. The performance values only gradually return to their original values over 5 h - 10 h in the darkness. The influence of light on the strain induced shift of the subthreshold swing is shown in Fig. 5.6d (page 129). The direction of the strain induced pa-

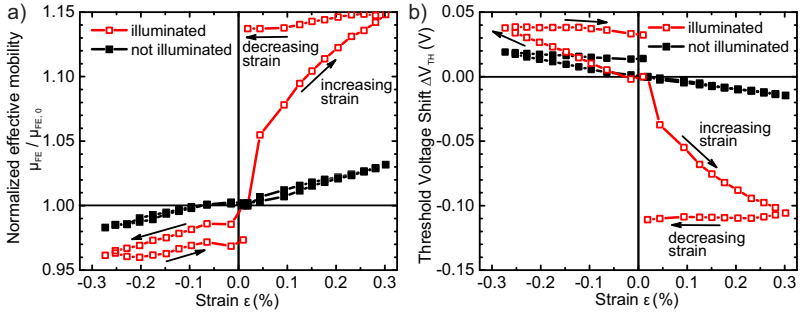

Figure 2.14: Normalized effective mobility (a), and threshold-voltage shift (b) for increasing and subsequently decreasing strain in darkness and illuminated with 90 lx. The time interval between two consecutive measurement points was always 5 min.

rameter shift under illumination is identical to the measurement without illumination. At the same time unstrained but illuminated TFTs do not show a comparable parameter shift. Hence, the measurements show the combined light /bending influence (and not a superposition of two independent effects).

This combined light /bending influence is explained by the fact that the by strain modified energy spacing between the bonding and antibonding orbitals of the semiconductor changes the light absorption of the IGZO. Therefore more (tensile strain) or less (compressive strain) photogenerated, positively charged holes h^+ are present in the n-type IGZO [10]. This h^+ can neutralize negatively charged oxygen inside the IGZO [11], [12] and/or negatively charged trapped electrons e^- near the Al_2O_3 /IGZO interface [13], [14]. The resulting change of the scattering center density influences the mean free path, and thus the mobility. At the same time, the increasing (tensile strain) or decreasing (compressive strain) number of photogenerated charge carriers changes the conductivity and therefore the threshold voltage. Additionally, the threshold voltage can also be affected by photogenerated holes near the dielectric/semiconductor interface or inside the gate insulator.

These results show that the parameter shift of flexible IGZO TFTs under tensile and compressive bending strongly depends on illumination of the device, which is especially important for bendable display applications.

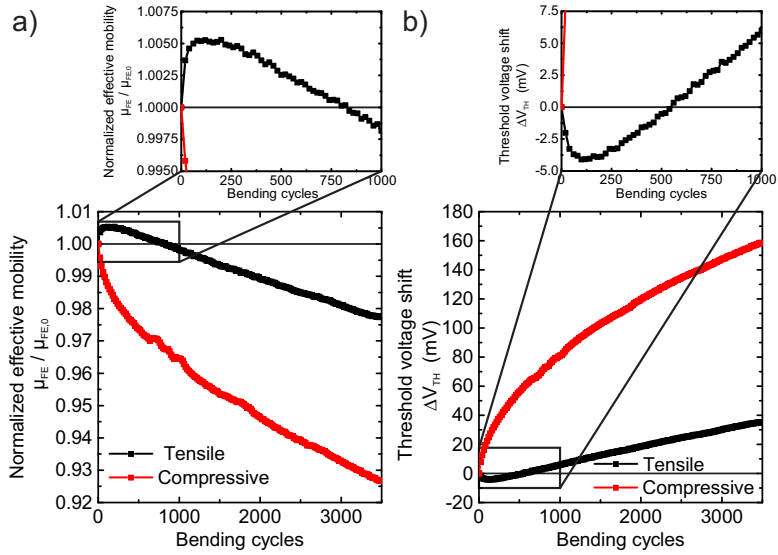

Figure 2.15: Effective mobility variation (a) and threshold voltage shift (b) of flexible IGZO TFTs after repeated bending and reflattening. Bending to a minimum radius of ≈5 mm was performed in tensile and compressive direction ($\epsilon \approx \pm 0.5\,\%$); total experiment time was ≈87.5 h. The measurements have been done while the TFTs were flat.

Influence of repeated bending and reflattening: Figure 2.15 shows the normalized effective mobility and the threshold voltage shift after different numbers of repeated cycles of bending and reflattening. Bending was performed in tensile and compressive direction, whereas a maximum strain of ≈ ±0.5 % was applied parallel to the TFT channel. The used bending tester (section 2.1.2a)) requires a timespan of ≈90 s to perform one bending cycle, resulting in a total cycling time t_{Str} of ≈87.5 h (3500 bending cycles). The graphs illustrates that the measured parameter shifts are different on long and short time scales.

Short term cycling: As shown in the detail diagrams of Fig. 2.15, 100 bending cycles (t_{Str} =2.5 h) increase μ_{FE} by ≈0.5 % for tensile and decrease μ_{FE} by ≈1 % for compressive bending while V_{th} is shifted by -5 mV (tensile) and +22 mV (compressive). The directions of the ob-

served shifts correspond to the results obtained from measurements performed while the TFTs are bent in tensile or compressive direction (Fig. 2.14). Therefore the influence of repeated bending can be explained by an incomplete recovery of the strain induced parameter shifts. The effects of up to 24 repetitions of bending and reflattening IGZO TFTs in darkness and under illumination are also shown in Fig. 5.8 (page 135).

Long term cycling: After longer cycling (up to 3500 bending cycles) a decrease of the effective mobility, and an increase of the threshold voltage was observed for tensile and compressive cycling. After 3500 bending cycles a decrease of μ_{FE} by -2.2 % (-7.3 %) and an increase of V_{th} by +35 mV (+158 mV) for tensile (compressive) cycling was measured. Additional long term cycling measurements are shown in Fig. 4.6 (page 117). The observed shifts can be explained by the electrical stress induced by multiple TFT transfer characteristic measurements during the cycling experiment, and by the formation of micro cracks. As described in section 3.3.2 (page 92) the electrical stress induced by multiple transfer characteristic measurements decrease the effective mobility and increase the threshold voltage. Therefore electrical stress has a similar influence as compressive strain. In the presented cycling experiment, the TFT transfer characteristic was measured 175 times (after every 20 bending cycles). In the case of tensile cycling, electrical and mechanical stress cause opposing effects. For a small number of bending cycles the mechanical stress is dominant and results the shifts described in the paragraph before. Over time the influence of the electrical stress gets more and more dominant and finally causes a negative shift of μ_{FE} and an positive shift of V_{th} for more than 820 (t_{Str} =20.5 h) and 540 (t_{Str} =13.5 h) bending cycles, respectively. In case of compressive cycling the influence of electrical and mechanical stress on the performance parameters add up and lead to the observed decreased of μ_{FE} and increase of V_{th}. In total it can be concluded that results obtained from long term cycling experiments (175 transfer characteristic measurements, experiment time >13.5 h) represent the electrical and not the mechanical stability of flexible IGZO TFTs.

c) Improvement of the bendability

The bendability of flexible TFTs can be improved by two different approaches: First by increasing the ductility of brittle material layers

in the device stack, which leads to TFTs able to withstand higher strain levels. The second approach is the reduction of the strain in the TFTs while bent.

Ductility of the gate metal: An investigation on the origin of cracks in flexible IGZO TFTs is described in **Chapter seven** (page 155). The most brittle material layer in the TFT stack was identified by cross sectional FIB images of cracks in bent TFTs, as shown in Fig 2.16a. The cross section shows that the crack has an average width of ≈30 nm, and gets wider close to the flexible polyimide substrate. Despite that the mechanical strain is higher in the upper layers of the TFT stack the Ti /Au top metallization is partially able to bridge the crack, while the lower Cr bottom gate is totally separated. This can be explained by the higher ductility of Au compared to Cr, but it also demonstrates that the limiting factor for the bendability is not the ceramic IGZO semiconductor or the Al_2O_3 gate insulator but the metallic and normally crystalline Cr [15]. To improve the TFT flexibility the Cr gate contact (rupture strain ϵ_R ≈0.5 % [16]), has been replaced by more ductile metals. These are Ti (ϵ_R ≈2 % [17]), Pt (ϵ_R ≈4 % [18]), and Cu (ϵ_R ≈4.5 % [19]). TFTs fabricated with these gate metals show comparable electrical performance (Tab. 7.1, page 160), but a significantly different strain resistance.

The influence of bending on TFTs with different gate metals is shown in Fig. 2.16b. Here, the evolution of the normalized effective mobility for different bending radii is plotted. The Cr gate TFT shows only a small variation of the mobility (≈4 %) as long as the strain is smaller than 0.7 % (r =3.8 mm), whereas at higher strain values a decrease of the mobility by several orders of magnitude is observed. This decrease is caused by the formation of cracks in the channel region. The strain value at which crack formation starts was defined as the threshold strain ϵ_{TH}. The threshold strain is a measure for the bendability of TFTs. Compared to the Cr gate TFT, the TFTs with more ductile gate metals exhibit higher ϵ_{TH} values. In particular the Cu gate TFT is operational up to a stain value of 1.55 % (corresponding to a bending radius r of 1.7 mm) (Fig. 7.7, page 165). The inset of Fig. 2.16b displays the minimal bending radii of TFTs with different gate metals (average value and standard deviation) obtained from multiple bending tests (up to 5 per gate material). The graph shows a clear correlation between the measured ϵ_{TH} and the reported ϵ_R of the gate metals, and that IGZO TFTs with Cu gates can be reliably bent to radii <2 mm.

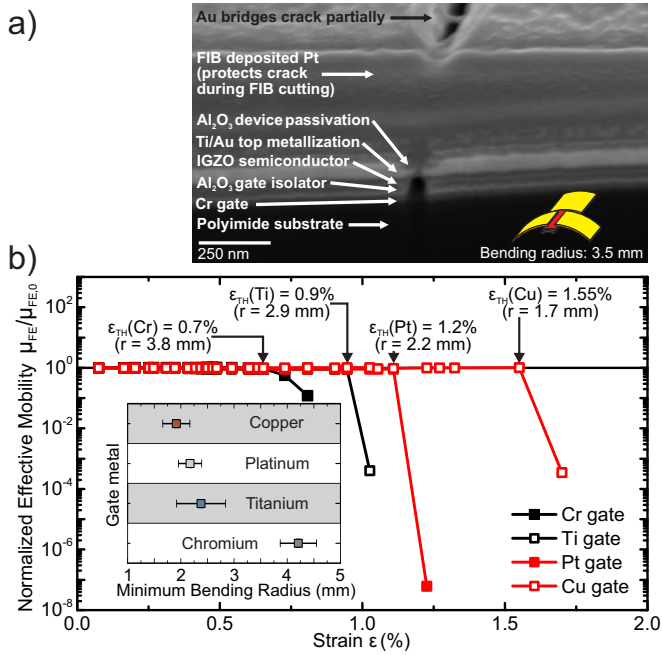

Figure 2.16: a) FIB image of a crack in a flexible IGZO TFT (Cr gate contact) bent to a radius of 3.5 mm. b) Evolution of the normalized effective mobility with increasing mechanical strain for flexible IGZO TFTs fabricated using gate metals with different ductilities, the inset shows the influence of the gate metal on the minimum bending radius (the data points and error bars give the mean values and the standard deviation).

These results in combination with the fact that Cu is a cheap material with a high electrical conductivity indicates that, among chromium, titanium, platinum and copper, Cu is the most suitable gate material for flexible IGZO TFTs.

TFTs on a 1 μm thin membrane: The advantage of a substrate thinner than 50 μm is illustrated by the following example: A flexible TFT on 50 μm thick polyimide substrate is exposed to a strain of ≈0.5 % when bent to radius of 5 mm. At the same time, an identical TFT bent to the

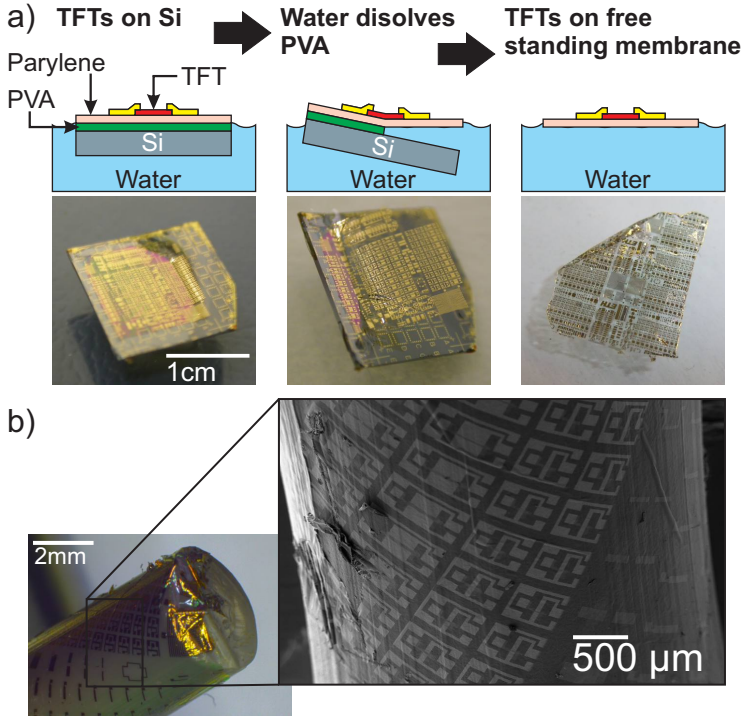

Figure 2.17: a) Releasing process: H_2O dissolves the PVA and release the 1 µm thick parylene membrane incl. the TFTs. b) Micrograph and SEM image of a parylene membrane (including TFTs) transferred to a plastic rod with a radius of 2 mm. Due to the thin membrane the strain is only 0.02 %.

same radius, but on top of an only 1 µm thick substrate is strained by only ≈0.01 %. Since such thin substrates are hard to handle during the fabrication a different approach concerning the manufacturing process is proposed in **chapter six** (page 145). In contrast to the fabrication on a free-standing polymer foil, TFTs are fabricated on top of a multi-layer polymer stack deposited on a Si carrier wafer. The polymer stack consist out of a spin coated 400 nm thick water soluble polyvinyl alcohol (PVA) layer and a thermally evaporated 1 µm thick parylene film. The chemical stability of parylene enables the fabrication of IGZO TFTs

using standard fabrication techniques. After the TFT fabrication the parylene membrane is released from the Si wafer by floating the chip in water, which dissolves the PVA. For a $2 \times 2\,cm^2$ chip the release takes ≈10 minutes after which the parylene membrane including the TFTs is floating on the water. This release is illustrated in Fig. 2.17a. The floating membrane can then be transferred to the final surface by dipping the desired substrate into the water, moving it towards the membrane, and lifting it. The membrane was successfully transferred to different substrates including polyimide, polypropylene, glass, plant leafs, and human skin; on these substrates the membrane sticks due to adhesion forces (the transfer to polyimide is demonstrated in Fig. 6.3, page 148). At the same time the adhesion is not sufficient to permanently place the membrane on rough materials like cotton textiles.

The transfer of TFTs to a curved surface is demonstrated in Fig. 2.17b. The parylene membrane with TFTs is attached to a plastic rod with a radius of 2 mm. The transferred TFTs are fully operational while bent to a radius of 2 mm, and exhibit an I_{on}/I_{off} of 2×10^8 (V_{DS} =V_{GS} =5 V), a threshold voltage of ≈2.1 V, a subthreshold swing of 230 mV/decade, and a field effect mobility of $\approx 21\,cm^2V^{-1}s^{-1}$. The corresponding TFT characteristics are shown in Fig. 6.6 (page 152). Additionally to the high flexibility of the thin parylene membrane, the transfer process has the advantage that the membrane, including the IGZO TFTs, can be placed on nearly any kind of flexible, elastic, or shaped surface. It thereby enables the functionalization of surfaces with electronics which are not compatible with semiconductor manufacturing technologies.

2.1.3 Flexible pn diode based on IGZO and NiO[2]

Besides thin-film transistors, thin-film diodes are important components for the realization of flexible electronic circuits. This section describes the fabrication of NiO/IGZO pn diodes on flexible polyimide substrate and their performance under mechanical strain [20].

[2]This section is based on: N. Münzenrieder, C. Zysset, L. Petti, T. Kinkeldei, G.A. Salvatore, and G. Tröster, Room temperature fabricated flexible NiO/IGZO pn diode under mechanical strain. In *Solid-State Electronics*, 87, pages 17–20, 2013. © 2013 Elsevier Ltd.

a) Device structure and fabrication

Due to the lack of an oxidic p-type semiconductor with a performance comparable to the one of IGZO, we fabricated and evaluated room temperature deposited nickel oxide (NiO) as material for the fabrication of pn diodes on flexible polyimide substrates. NiO was deposited by DC magnetron sputtering from a metallic Ni target [21]. Ni was oxidized during the sputter process in a 50 % Ar, 50 % O_2 atmosphere at a pressure of 6 mtorr (Ar flow =10 sccm, O_2 flow =10 sccm), while a DC power of 200 W was applied. Under the described conditions, a sputter rate of ≈6 nm min^{-1} was observed. To investigate the electrical properties of the sputtered NiO a 120 nm thick layer, was contacted by four evaporated Ti /Au contacts (Van der Pauw geometry) using a shadow mask process. The resulting sample was characterized by room temperature Hall measurements, which confirmed the p-type semiconducting behavior of the sputtered NiO. In particular a carrier density n_p of $+1.6 \times 10^{17} cm^{-3}$ and a Hall mobility μ_H of 0.45 $cm^2V^{-1}s^{-1}$ were measured. This parameters resulted in a specific resistivity of 85 Ω cm.

The corresponding n-type semiconductor of the pn diodes was IGZO. RF magnetron sputtering from a ceramic $InGaZnO_4$ target resulted in a carrier density n_e of -$2.2 \times 10^{19} cm^{-3}$, and a Hall mobility μ_H of 11.8 $cm^2V^{-1}s^{-1}$.

The device structure of the flexible diodes is shown in Fig. 2.18. An unstructured 50 nm thick evaporated Ti laver served as anode on top of a 50 µm thick polyimide foil. The pn junction was formed by 120 nm of NiO, and 40 nm of IGZO. These thicknesses account for the different carrier concentrations in NiO and IGZO, and prevented the formation of pinholes. NiO and IGZO were structured by a lift-off process. Cathode contacts on top of the semiconductor structures were formed by evaporated 10 nm Ti /60 nm Au layers, and structured in an additional lift-off process. The ohmic behavior of the two Ti /semiconductor junctions was confirmed by separate I–V measurements.

Figure 2.18: Schematic of the fabricated flexible pn diodes.

b) Electrical performance and influence of mechanical strain

I–V characteristics of a flexible NiO/IGZO diode with an area of 0.09 mm^2 while flat and bent are plotted in Fig. 2.19. The diode exhibited a rectifying characteristic with an effective threshold voltage $V_{th,eff}$ of 1.14 V, and an-off current ratio $>10^3$ (V = ±2.5 V). The reverse breakdown voltage was ≈-5 V. The capacitance of the diodes, measured at a DC voltage of 0 V was 428 nF/cm^2. This capacitance corresponds to a depletion region width W_D of ≈24 nm [10], calculated using an average dielectric constant ϵ_r of the IGZO/NiO stack of 11.8 [22, 23]. If voltages >1 V were applied the diode, the diode I–V characteristic showed a ohmic behavior with a differential resistance of ≈100 Ω. This ohmic behavior was due to a series resistance determined by the sheet resistance of the Ti anode (≈20 Ω/□). At voltages <≈0.7 V the rectifying property of the pn junction dominated the device performance. In this region an ideality factor of ≈3.2 was extracted (The ideality factor describes how closely the diode follows the Shockley ideal diode equation). This high ideality factor (a value of 1 corresponds to the ideal diode equation) can be attributed to structural imperfections and/or interface states of the NiO and IGZO layers [24, 25].

The flexibility of the fabricated NiO/IGZO pn diodes was investigated by attaching the diodes to a curved surface (using double sided tape); in the way that tensile or compressive strain was applied. The radius of the curvature was 10 mm, resulting in a mechanical strain ϵ of ≈ ±0.25 %. The I-V characteristic of a NiO/IGZO pn diode before bending, and while bent to a tensile radius of 10 mm, as well as a photograph of the bent and contacted substrate is shown in Fig. 2.19a. The flexible diodes remained operational while bent. At voltages >1 V, the applied tensile strain induced a reduction of the resistance by -6.3 %, and therefore an increase of the maximum diode current by 6.7 %. At voltages <0.4 V the current is increased by ≈45 % (average value between V =0.1 V and V =0.4 V). The same measurement for compressive strain applied to the diode is shown in Fig. 2.19b. Similar to the tensile case, the applied compressive strain induced a reduction of the resistance at voltages >1 V by -23 %, corresponding to an increase of the maximum diode current by 30 %. Simultaneously, compressive strain has a different influence in the diode dominated voltage region when compared to tensile strain. Compressive bending decreases the current by ≈-15 % (average value between V =0.1 V and V =0.4 V). The observed behavior can be explained by the fact that IGZO decreases /increases and metals

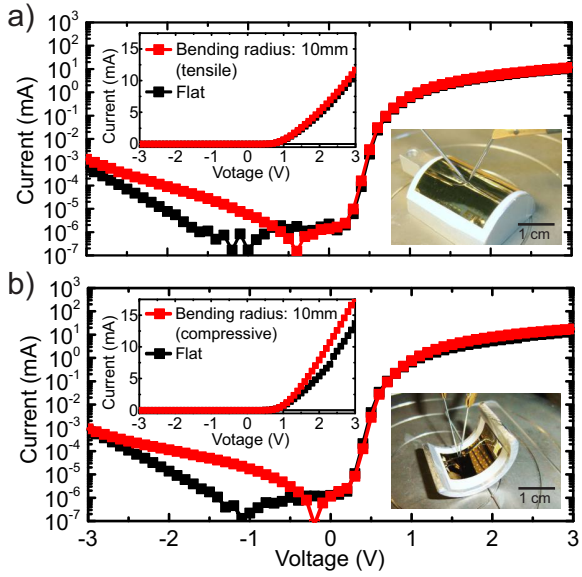

Figure 2.19: Diode I–V characteristic (diode area =0.09 mm^2) measured while flat, and while bent to a tensile (a) and compressive (b) radius of 10 mm (ϵ =0.25 %). The insets show the same data on a linear scale and photographs of the bent substrates.

increase /decrease their resistance under tensile /compressive strain (whereas compressive strain has a smaller influence on IGZO than tensile one) [26]. The measurements also suggest that NiO changes its resistance under strain in the same way as IGZO. The measurements of the bent diodes show an increased reverse leakage current (independent from tensile or compressive bending). At negative voltages the current is increased by up to 2 orders of magnitude, corresponding to an absolute increase <0.7 μA. Possible explanations for this increase are a higher temperature or stronger illumination during the measurements under strain.

2.1.4 Flexible circuits based on IGZO TFTs

The application of flexible IGZO TFTs calls for integrated flexible circuits. The fabrication and performance of digital and analog circuits, as well as a set of design rules to maximize the circuit bendability are described in this section.

a) Design of bendable circuits

Design rules for the layout of flexible integrated circuits were defined. These rules maximize the bendability of circuits compared to the bendability of the single TFTs. Section 2.1.2 (page 50) already described the different influence of mechanical strain parallel and perpendicular to the channel of flexible IGZO TFTs and the formation of cracks in the TFT gate contact. Based on these findings concerning the influence of the direction and strength of mechanical strain, design rules for digital NMOS IGZO circuits have been derived in **chapter eight** (page 169). The two most important one are the following:

1. All TFTs within a circuit should be aligned parallel to each other and also parallel to the applied mechanical strain
2. To avoid capillary cracks perpendicular to the channel, the gate length of TFTs strained parallel to the channel should be smaller than the expected minimal distance between two neighboring capillary cracks.

NAND gates (section 8.4.1, page 177) have been used to approve the correctness of these design rules under mechanical strain. The static n-type NAND gates were composed out of a load TFT (W/L = 140 μm/20 μm) and two driver TFTs (W/L = 1400 μm/20 μm) connected in series. The factor of 10 between the W/L ratios of the load and driver TFTs was a trade-off between the maximization of the output voltage swing and the area consumption of the circuits. The 20 μm long channels are shorter than the minimum distance between two capillary cracks of 31 μm (measured on single TFTs while the devices were bent to minimum possible bending radii of 3.5 mm). The circuits were fabricated with load TFTs oriented parallel and perpendicular to the driver TFTs. (Therefore, strain can be applied parallel to the driver TFTs and, at the same time, parallel and perpendicular to the load TFTs). The layout is shown in Fig. 2.20a.

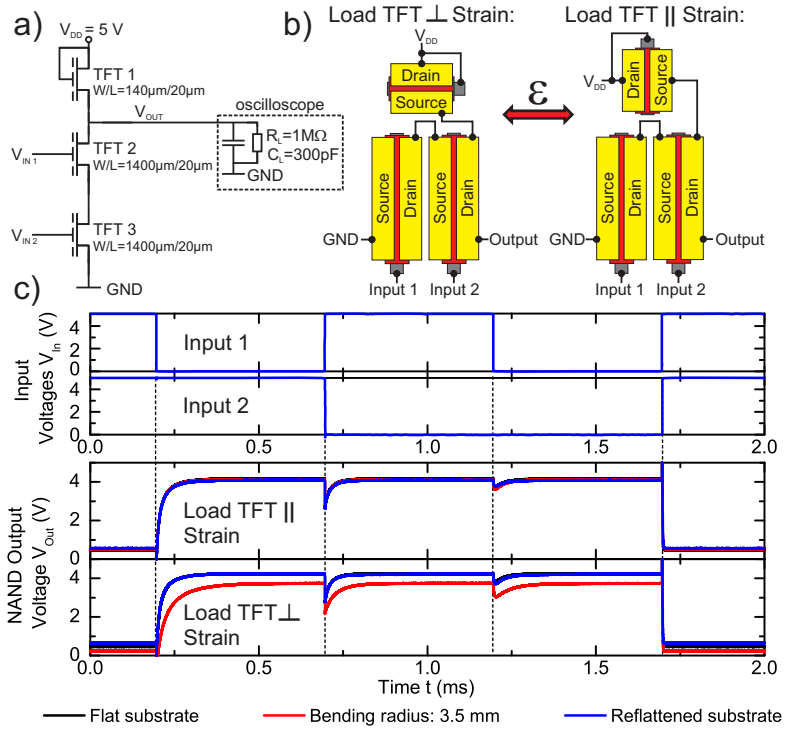

Figure 2.20: a) Layout of the fabricated flexible NAND gates. b) Input and output signals of two NAND gates before bending, with strain applied parallel to the driver TFTs and hence perpendicular and parallel to the load TFTs, and reflattened.

The circuits were characterized while flat, bent to a tensile radius of 3.5 mm ($\epsilon \approx 0.7\,\%$) parallel to the driver TFTs, and after reflattening. The corresponding input and output signals are plotted in Fig 2.20b. The NAND gate with perpendicular strained load TFT shows an increased load resistance, which is due to the smaller load TFT W/L ratio caused by capillary cracks. This results in decreased output voltage levels. Reflattening the circuit restores the original W/L ratio and, hence, the original output signals. At the same time, the NAND gate with all TFTs in parallel is insensitive to bending, and thereby confirmed validity of the presented design rules.

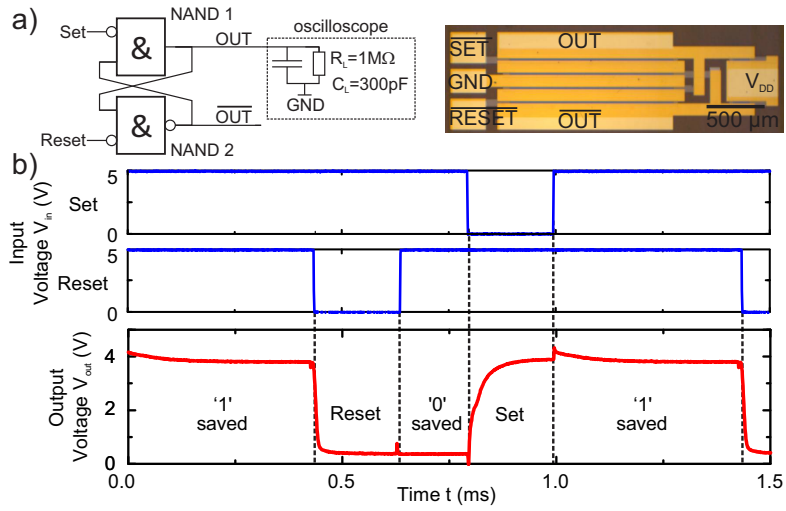

Figure 2.21: a) Circuit diagram and micrograph of the fabricated 1-bit SRAM. b) Input and output signals of the 1-bit SRAM while bent to tensile radius of 5 mm.

b) Flexible digital and analog circuits

To demonstrate the application of flexible IGZO TFTs, the following two paragraphs present digital and analog circuits designed according to the developed design rules.

Bendable SRAM cell: Digital circuit operation was demonstrated by a fully integrated 1-bit SRAM cell, composed of 6 IGZO TFTs and fabricated on flexible plastic foil. The layout and a micrograph of the device are shown in Fig. 2.21a. More details can be found in **chapter nine** (page 189). The circuit can be operated with a supply voltage of 5 V, and up to frequencies of 10 kHz. The 'set' (S) and 'reset' (R) signals are active low, therefore the condition S =R =0 V is not allowed. The input and output signals measured at an input signal frequency of 1 kHz and while the circuit is bent to a tensile radius of 5 mm ($\epsilon \approx 0.5\,\%$) are plotted in Fig. 2.21b.

The circuit shows the expected output signal: A low voltage pulse

(0 V) at the S input saves a digital '1' (output voltage ≈3.8 V). The output voltage is constant until a low voltage pulse is applied to the R contact, this changes the output voltage to ≈0.41 V (digital '0'). The rise and fall times t_r and t_f are ≈60 µs and ≈13 µs, respectively (Fig. 9.6, page 196). Additionally, the parallel alignment of all TFTs, and the uniform fabrication process ensures that bending affects all TFTs in the same way. Hence, the ratio between the conductivities of the load and driver TFTs stayed constant while the circuit was bent, therefore mechanical strain of ≈0.5 % has no significant influence on the performance of the flexible 1-bit SRAM cell.

Bendable amplifiers: Common source and cascode amplifiers are presented in **chapter ten** (page 203). The amplifiers have been fabricated on a free-standing plastic foil, using IGZO TFTs with a minimum channel length of 2.5 µm (Fig. 10.3, page 207). A circuit schematic and a micrograph of the flexible IGZO common source amplifier is shown in Fig. 2.22a.

The amplifier was designed to work at a supply voltage V_{DD} of 5 V. The AC characterization was performed with an input signal peak-to-peak amplitude v_{AC} of 100 mV, and a total output load of R_L=1 MΩ and C_L <2 pF. The common source amplifier was biased with an input voltage V_{DC} of 1.5 V. The amplifier exhibited a gain G of 6.8 dB, a cutoff frequency f_C of 1.2 MHz and a power consumption of 690 µW (Fig. 2.22b), which is in line with the expectations extracted from SPICE simulations [27].

The impact of mechanical strain on the flexible amplifiers was evaluated by bending the circuits to a tensile radius of 5 mm (ϵ ≈0.5 %) parallel to all TFT channels in the circuits. A micrograph of the bent circuit and the resulting Bode plots are also shown in Fig. 2.22b. Mainly because of the under strain nearly invariant transconductance ratio between the TFTs in the circuits, the measured variations of G and f_C (between flat and bent amplifiers) are less than 4 %, and 6 %. To emulate a realistic application scenario and to evaluate the influence of multiple bending, the flexible common source amplifier were characterized before and after 1000 cycles of repeated bending (5 mm radius) and re-flattening, corresponding to 25 h of continuous bending with the custom build bending tester. As shown in Fig. 10.11 (page 215), the common source amplifier stayed fully operational after 1000 bending cycles.

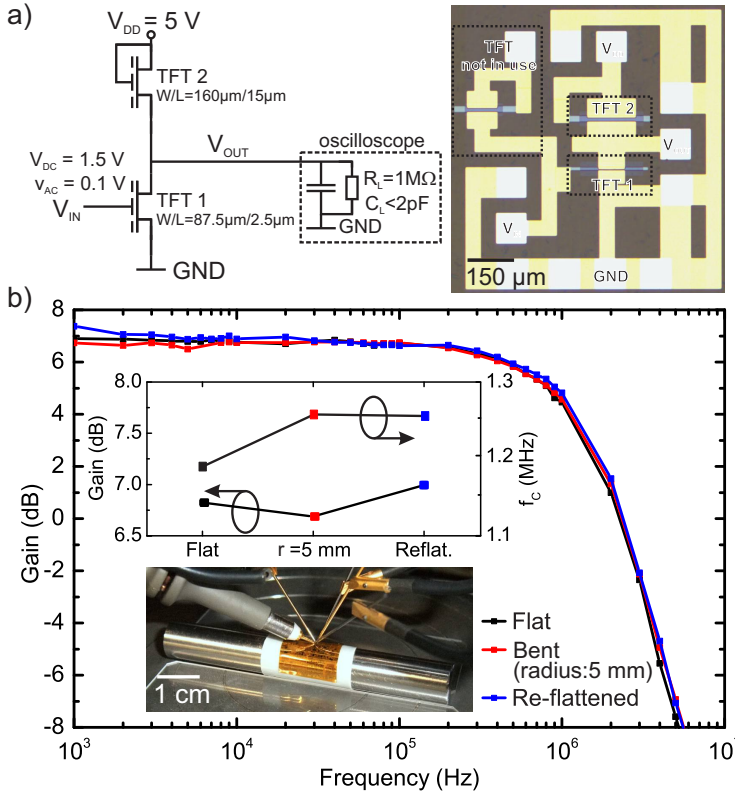

Figure 2.22: a) Circuit schematic and micrograph of the fabricated flexible common source amplifier. b) Bode plots of the flexible amplifier measured while the circuit was flat, bent around a rod of 5 mm radius, and re-flattened. The inset shows the evolution of gain and cutoff frequency, as well as an micrograph of the bent and contacted substrate.

This was the first demonstration of IGZO based amplifiers fabricated on a free-standing plastic foil which exhibited cutoff frequencies >1 MHz, and therefore showed the suitability of this technology for new electronic applications, like flexible AM-radios, or LF-RFID tags.

2.2 Conclusion

This thesis focuses on the development of flexible oxide semiconductor based electronics. Semiconducting IGZO has been used to fabricate transistors and diodes on free standing plastic substrates. Self-alignment techniques and double gate structures improved the DC and AC performance of IGZO TFTs, respectively. The effect of bending was extensively investigated, and methods to decrease the minimal possible bending radius, as well as to minimize the influence of strain on flexible circuits have been proposed. The performance and bendability of flexible circuits for digital and analog applications were presented. Based on the summary from section 2.1, the following conclusions can be drawn:

- Depending on the exact application of IGZO based electronics in future flexible devices, the electrical performance of IGZO TFTs on plastic foils has to be adopted. While e.g. rollable displays require TFTs with a high on-current and small subthreshold swing, flexible transceivers call for small parasitic capacities and therefore high frequencies.

  The increase of the channel capacitance was identified as a suitable way to increase the transconductance (and therefore the on-current) of flexible bottom gate IGZO TFTs, as well as to decrease their subthreshold swing. The high conformability and high dielectric constant (ϵ_r =9.5) of low temperature (<150 °C) ALD deposited aluminum oxide makes this material a appropriate gate insulator for flexible IGZO TFTs. Additionally, IGZO TFTs with Al_2O_3 gate insulator and backchannel passivation show high electrical stability and low interface trap density. It was dem onstrated that flexible IGZO TFTs with a 10 nm thin Al_2O_3 gate insulator benefit from the high oxide capacitance (8.4 mF/m^2), and exhibit a subthreshold swing of 84 mV/decade. A further increase of the gate capacitance was possible by the use of an additional top gate. The resulting double gate TFTs show an increase of the gate capacitance by 78 %, and a subthreshold swing of 69 mV/decade.

  If TFTs should be reliably fabricated on a 7.6 cm × 7.6 cm (3 × 3 inch) plastic substrate, the mechanical instability of plastic foils and the temperature induced expansion during the TFT fabrication process limit the minimal channel length and the gate

to source drain overlaps to values around 1 μm and 5 μm. This problem can be solved by self-alignment between the gate and source /drain contacts, which is the most critical alignment during the fabrication process of bottom gate TFTs. Self-alignment is done by backside illumination through the semitransparent plastic substrate. Due to the use of the developed self-alignment process it was possible to shift the minimum channel length of flexible IGZO TFTs into the submicron regime. Self-aligned TFTs exhibited channel length as small as 0.5 μm and gate to source /drain overlaps of 1.5 μm. This resulted in TFTs with a measured transit frequency of 135 MHz.

In addition, the use of transparent ITO source and drain contacts enabled a combination of the self-aligned and double gate approach. Due to this technology, flexible IGZO TFTs with a high gate capacitance, and low overlap capacities are possible at the same time. lengths >10 μm.

- Bending flexible IGZO TFTs showed that mechanical strain causes a reversible performance parameter shift at small strain values, and induces cracks at higher strain values. Additionally, the influence of mechanical strain depends on several factors:

  It was found that tensile strain causes a negative shift of the threshold voltage and an increase of the effective mobility, while compressive strain has the opposite effect. This shift is induced by a change of the effective mass and density of the electrons caused by a change of the interatomic distances in the IGZO. These parameter shifts recover nearly immediately when the TFTs are reflattend. Also the maximum bendability of IGZO TFTs is different for tensile and compressive bending. In tensile direction, minimum bending radii around 4 mm have been observed, while in compressive direction identical TFTs can be bent to a radius of 1.1 mm without the formation of any cracks harming the TFT functionality.

  The direction of the strain relative to the TFT channel also influenced the impact of strain. Bending parallel to the channel and therefore parallel to the current flow causes larger reversible parameter shifts. At the same time, the normally larger width of TFTs compared to their length increased the probability of crack formation under bending perpendicular to the TFT channel.

Since strain changes the interatomic distances in the IGZO and therefore the IGZO band structure the influence of strain interacts with the light absorption, leading to a combined strain – illumination effect. This interaction leds to an amplification of the influence of strain under illumination (90 lx) by a factor up to 5, when compared to measurements performed in darkness. Illumination also increased the recovery time of strain induced parameter shifts up to several hours.

The influence of repeated bending and reflattening is determined by the direction of the bending. The parameter shifts induced by repeated bending are comparable to the parameter shifts caused by electrical stress. This leads to the fact that on a long time scale flexible IGZO TFTs (with a voltage applied to the gate) always shift to higher threshold voltages and smaller effective mobilities (determined by electrical stress).

- A reduction of the minimal possible bending radius of flexible IGZO TFTs was achieved by the reduction of the induced strain (by decreasing the substrate thickness from 50 μm to 1 μm), and by the use of, compared to Cr, more ductile gate contact materials to fabricate the TFTs. TFTs on a thin parylene substrate and TFTs with Cu gate contacts could be bent to radii of 2 mm and 1.7 mm, respectively. The TFTs on the parylene substrate had the additional advantage that they could be placed on nearly any kind of shaped or flexible surface. Both approaches did not change the electronic properties of the TFTs.

- Nickel oxide was evaluated as a possible p-type semiconductor for flexible electronics. Room temperature sputtered NiO on polyimide foil exhibited a Hall mobility of $0.45\,cm^2V^{-1}s^{-1}$ and a positive carrier density of $+1.6 \times 10^{17} cm^{-3}$. NiO could be combined with IGZO to fabricate flexible oxide semiconductor based pn diodes. The characterization of these diodes under mechanical strain resulted in a strain modulated current-voltage characteristic. Here the results are in line with the results obtained from IGZO TFT bending experiments, with the exception that the 160 nm thick and brittle oxide layer (NiO+IGZO) limited the minimum bending radius in tensile and compressive direction to 10 mm.

- To minimize the influence of mechanical strain, and to guaranty an as small as possible minimal bending radius of integrated flexible circuits based on IGZO TFTs, design rules concerning the geometrical alignment of the single TFTs were proposed. According to these design rules all TFTs in a circuits should be aligned parallel to each other and parallel to the applied mechanical strain. In addition, the TFT channels should be shorter than the expected minimal distance between two strain induced cracks.

  These design rules, in combination with flexible IGZO TFTs exhibiting channel length as small as 2.5 μm, and channel width between 87.5 μm and 1400 μm led to different digital and analog circuits. The Circuits were operational while bent to a radius of 5 mm, and after ≥1000 cycles of repeated bending and reflattening. Flexible common source and cascode amplifiers exhibited voltage gains and cutoff frequencies up to 7.8 dB and 1.2 MHz. These results already enable applications, like flexible AM-radios, ultra-sound devices, and LF-RFID tags.

2.3 Limitations

- Although the carrier mobility of IGZO is higher than the one of amorphous Si or organic semiconductors, the achievable values around $15\,cm^2V^{-1}s^{-1}$ are at least one order of magnitude smaller than the carrier mobilities of crystalline semiconductors. This limits the gain and the operation frequency of oxide semiconductor based electronics.

- The compared to standard silicon technology high contact resistances on the order of $10\,k\Omega\,\mu m^{-1}$ or even $100\,k\Omega\,\mu m^{-1}$ limit the scalability of IGZO TFTs. This is an additional reason for the limited operation frequency.

- Until now, the class of oxide semiconductors does not provide a p-type semiconductor with a performance comparable to the one of IGZO. Therefore it is not possible to benefit from the increased functionality, performance, and power efficiency of CMOS circuits.

- The expansion of a flexible7.6 cm × 7.6 cm plastic substrate can reach values >10 μm during the fabrication process. This defor-

mation is caused by temperature changes and the absorption of water and solvents. Fluctuations of the substrate size during the fabrication have a negative impact on the accuracy possible during photolithography mask alignment, and therefore influence the device performance and integration density.

- An unobtrusive integration of flexible electronic devices calls for transparent substrates. Additionally, self-aligned backside illumination would profit from totally transparent substrates. While polyimide provides only a limited transparency and has a yellowish color, commercially available transparent plastic foils like PEN or PET exhibit a smaller thermal, chemical or mechanical stability.

- Tensile stain >1.5 % cause the formation of cracks in the IGZO semiconductor /Al_2O_3 gate insulator stack, and hence limit the bendability of IGZO TFTs. A further reduction of the minimal bending radius seems only possible by a reduction of the strain in the device which requires a more complicated fabrication process, or by the use of a more ductile semiconductor /gate insulator stack which may decrease the electrical performance.

2.4 Outlook

Flexible electronics in general, and oxide semiconductor based devices in particular promise to enable the integration of electronic functionality in a large number of objects, and thereby change the way people interact with electronic systems. Some additional research questions which could assist to achieve this goal are given in the following list:

- Oxide semiconductor based CMOS circuits would boost the performance and probably have a large effect on the commercialization of flexible electronics. Although the development of a low temperature processable oxidic p-type semiconductor with a carrier mobility >10 $cm^2V^{-1}s^{-1}$ is not impossible from the physical point of view, it is not clear whether and, if so, when the development will be successful. An alternative solution could be the use of hybrid CMOS circuits using an oxidic n-type and an organic p-type semiconductor. In this case compatible fabrication techniques and a suitable device encapsulation to guaranty

long term stability have to be established. Aside from the development of semiconductors, flexible oxide electronics could also benefit from the combination of other materials. The use of electrolytes or self-assembled monolayers (SAMs) as gate insulator is a possible way to increase the gate capacitance and the bendability at the same time. Additionally, source and drain contacts with an optimized work function would decrease the contact resistance of IGZO TFTs. Moreover, robust and transparent flexible substrates have the potential to simplify the self-aligned backside exposure lithography, or to increase the maximum possible fabrication temperature T_{MAX}. An interesting candidate for such an substrate is flexible glass [28].

- Alternative device structures inspired from standard semiconductor technology like vertical transistor or gate all around structures offer the possibility to improve the device performance without the need for new materials or more sophisticated fabrication techniques. Additionally unconventional structuring techniques could be able to reduce the minimum feature size of flexible TFTs. The use of electron beam lithography on nonconductive plastic foils is difficult because plastic foils are not as flat as a semiconductor wafer. Therefore the adjustment of the focus point has to be done close to the writing area which result in problems correlated with the unintended illumination of the resist. To avoid this problem, resist structuring by direct laser writing could be used. Here the sample is viewed and illuminated by two independent systems. Furthermore, a possibility to bring structured conductors like Carbon, Platinum or Tungsten directly onto the sample is the FIB induced chemical vapor deposition of these materials.

- The market success of flexible electronics will also strongly depend on the manufacturing costs. Especially since the integration density of devices on flexible substrates is low, fabrication has to be done on large scale substrates, or even in roll to roll processes. Display manufacturers already fabricate thin film electronics on square-meter sized glass panels, nevertheless not all fabrication techniques are compatible with large scale substrates. Solution based printing processes of oxides can allow the large scale fabrication of electronic devices without losing the beneficial electronic properties of materials like IGZO and Al_2O_3.

- The application of flexible oxide semiconductor based electronics to measure physiological signals, especially when the electronics are fabricated on a thin ($<\approx 1\,\mu m$) membrane, could be a promising approach. Thin flexible IGZO electronics can potentially be implanted into the body and enable more unobtrusive and more accurate measurements. To achieve this, the biocompatibility of all employed materials has to be proven. At the same time the electronics have to be able to communicate with the outside world. In the ideal case wireless transceivers based on oxide electronics will be available.

- Analog circuits for which the performance, in particular the gain, is determined by the ratio between different transistors, and with all TFTs aligned in parallel are not affected by bending. At the same time, if the performance of an analog circuit depends e.g. on the absolute resistance of a circuit element bending has an impact. This was demonstrated for a flexible transimpedance amplifier [29]. An active compensation which cancels the influence of bending could improve the stability of flexible oxide electronics based systems.

Bibliography

[1] L. Lan and J. Peng. High-performance indium–gallium–zinc oxide thin-film transistors based on anodic aluminum oxide. *Electron Devices, IEEE Transactions on*, 58(5):1452–1455, 2011.

[2] R. Gregorian and G.C. Temes. Analog mos integrated circuits for signal processing, 1986.

[3] S.A. Khan, P.-C. Kuo, A. Jamshidi-Roudbari, and M. Hatalis. Effect of uniaxial tensile strain on electrical performance of amorphous igzo tfts and circuits on flexible metal foils. In *Device Research Conference (DRC), 2010*, pages 119–120. IEEE, 2010.

[4] N. Münzenrieder, L. Petti, C. Zysset, G.A. Salvatore, T. Kinkeldei, C. Perumal, C. Carta, F. Ellinger, and G. Tröster. Flexible a-IGZO TFT amplifier fabricated on a free standing polyimide foil operating at 1.2 MHz while bent to a radius of 5 mm. In *Electron Devices Meeting (IEDM), 2012 IEEE International*, pages 5–2. IEEE, 2012.

[5] K.H. Cherenack, B. Hekmatshoar, J.C. Sturm, and S. Wagner. Self-aligned amorphous silicon thin-film transistors fabricated on clear plastic at 300< formula formulatype=. *Electron Devices, IEEE Transactions on*, 57(10):2381–2389, 2010.

[6] D.H. Kang, I. Kang, S.H. Ryu, and J. Jang. Self-aligned coplanar a-igzo tfts and application to high-speed circuits. *Electron Device Letters, IEEE*, 32(10):1385–1387, 2011.

[7] R.H. French, J.M. Rodríguez-Parada, M.K. Yang, R.A. Derryberry, and N.T. Pfeiffenberger. Optical properties of polymeric materials for concentrator photovoltaic systems. *Solar Energy Materials and Solar Cells*, 95(8):2077–2086, 2011.

[8] I.L. Spain and J. Paauwe. *High Pressure Technology: Equipment design, materials, and properties*. M. Dekker, Inc., M. Dekker, NY, USA, 1st edition, 1977.

[9] L.C.L.Y. Voon and M. Willatzen. *The kp Method: Electronic Properties of Semiconductors*. Springer, 2009.

[10] S.M. Sze and K.K. Ng. *Physics of Semiconductor Devices*. John Wiley and Sons, 2007.

[11] P.-T. Liu, Y.-T. Chou, and L.-F. Teng. Environment-dependent metastability of passivation-free indium zinc oxide thin film transistor after gate bias stress. *Applied Physics Letters*, 95(23):233504–233504, 2009.

[12] J.-H. Lee, H.-I. Kwon, H. Shin, B.-G. Park, and Y.J. Park. Electrical instabilities and low-frequency noise in ingazno thin film transistors. In *Physical and Failure Analysis of Integrated Circuits (IPFA), 2010 17th IEEE International Symposium on the*, pages 1–7. IEEE, 2010.

[13] H. Seo, Y.-J. Cho, J. Kim, K.-Y. Park, J. Lee, and D.-K. Choi. Permanent optical doping of amorphous metal oxide semiconductors by deep ultraviolet irradiation at room temperature. *Applied Physics Letters*, 96(22):222101–222101–3, 2010.

[14] A. Suresh, P. Wellenius, and J.F. Muth. High performance transparent thin film transistors based on indium gallium zinc oxide as the channel material. In *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pages 587–590. IEEE, 2007.

[15] J.E. Nestell, R.W. Christy, M.H. Cohen, and G.C. Ruben. Structure and optical properties of evaporated films of the cr-and v-group metals. *Journal of Applied Physics*, 51(1):655–660, 1980.

[16] M.J. Cordill, A. Taylor, J. Schalko, and G. Dehm. Fracture and delamination of chromium thin films on polymer substrates. *Metallurgical and Materials Transactions A*, 41(4):870–875, 2010.

[17] H. Ogawa, K. Suzuki, S. Kaneko, Y. Nakano, Y. Ishikawa, and T. Kitahara. Tensile testing of microfabricated thin films. *Microsystem technologies*, 3(3):117–121, 1997.

[18] K.N. Jonnalagadda, I. Chasiotis, S. Yagnamurthy, J. Lambros, J. Pulskamp, R. Polcawich, and M. Dubey. Experimental investigation of strain rate dependence of nanocrystalline pt films. *Experimental mechanics*, 50(1):25–35, 2010.

[19] N. Lu, Z. Suo, and J.J. Vlassak. The effect of film thickness on the failure strain of polymer-supported metal films. *Acta Materialia*, 58(5):1679–1687, 2010.

[20] N. Münzenrieder, C. Zysset, L. Petti, T. Kinkeldei, G.A. Salvatore, and G. Tröster. Room temperature fabricated flexible nio/igzo pn diode under mechanical strain. *Solid-State Electronics*, 87:17–20, 2013.

[21] K. Kobayashi, M. Yamaguchi, Y. Tomita, and Y. Maeda. Fabrication and characterization of in–ga–zn–o/nio structures. *Thin Solid Films*, 516(17):5903–5906, 2008.

[22] H.-J. Chung, J.H. Jeong, T.K. Ahn, H.J. Lee, M. Kim, K. Jun, J.-S. Park, J.K. Jeong, Y.-G. Mo, and H.D. Kim. Bulk-limited current conduction in amorphous ingazno thin films. *Electrochemical and Solid-State Letters*, 11(3):H51–H54, 2008.

[23] K.V. Rao and A. Smakula. Dielectric properties of cobalt oxide, nickel oxide, and their mixed crystals. *Journal of Applied Physics*, 36(6):2031–2038, 1965.

[24] Y. Zhao, W. Dong, X. Fang, Y. Zhou, G. Meng, R. Tao, Z. Deng, S. Zhou, and S. Dai. P-type Ca doped SrCu2O2 thin film: Synthesis, optical property and photovoltaic application. *Journal of Alloys and Compounds*, 513:50–54, 2012.

[25] A.N. Banerjee and K.K. Chattopadhyay. Recent developments in the emerging field of crystalline p-type transparent conducting oxide thin films. *Progress in crystal growth and characterization of materials*, 50(1):52–105, 2005.

[26] N. Münzenrieder, K.H. Cherenack, and G. Tröster. The effects of mechanical bending and illumination on the performance of flexible IGZO TFTs. *IEEE Transactions on Electron Devices*, (99):1–8, 2011.

[27] C. Perumal, K. Ishida, R. Shabanpour, B. Boroujeni, L. Petti, N. Münzenrieder, G.A. Salvatore, C. Carta, G. Tröster, and F. Ellinger. A Compact a-IGZO TFT Model Based on MOSFET SPICE Level=3 Template for Analog/RF Circuit Designs. *IEEE Electron Device Letters*, 2013.

[28] G. Mone. The future is flexible displays. *Communications of the ACM*, 56(6):16–17, 2013.

[29] C. Zysset, N.S. Münzenrieder, T. Kinkeldei, K.H. Cherenack, and G. Tröster. Indium-gallium-zinc-oxide based mechanically flexible transimpedance amplifier. *Electronics letters*, 47(12):691–692, 2011.

3

Flexible double gate IGZO TFTs

Niko Münzenrieder, Christoph Zysset, Luisa Petti, Thomas Kinkeldei, Giovanni A. Salvatore, Gerhard Tröster

Flexible double gate a-IGZO TFT fabricated on free standing polyimide foil

Solid-State Electronics, 84, pp. 198–204, 2013.
10.1016/j.sse.2013.02.025

Abstract

In this paper, the concept of double gate transistors is applied to mechanically flexible amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) thin film transistors (TFTs) fabricated on free standing plastic foil. Due to the temperature sensitivity of the plastic substrate, a-IGZO is a suitable semiconductor because it provides carrier mobilities around 10 $cm^2V^{-1}s^{-1}$ when deposited at room temperature. Double gate TFTs with connected bottom and top gate are compared to bottom gate reference TFTs fabricated on the same substrate. Double gate a-IGZO TFTs exhibit a by 78 % increased gate capacitance, a by 700 mV higher threshold voltage, and therefore an up to 92 % increased transconductance when characterized at the same gate voltage above threshold (over-bias voltage). The subthreshold swing and the on-off current ratios are improved as well, and reach excellent values of 69 mV/decade and 2×10^9, respectively. The mechanical flexibility of double gate TFTs compared to bottom gate TTFs is investigated, and device operation is shown while the double gate TFT is exposed to tensile strain of 0.55 %, induced by bending to a radius of 5 mm.

3.1 Introduction

Electronic devices, especially thin-film transistors (TFTs) fabricated directly on flexible plastic substrates are a key requirement for a number of new large-area applications such as rollable displays, electronic skins or woven electronics for smart textiles [1]. Additionally, the use of roll to roll techniques allows cost effective, large scale processing on flexible substrates [2]. While organic [3] and a-Si:H [4] based TFTs fabricated on flexible and temperature sensitive substrates in general suffer from low mobilities around 1 $cm^2V^{-1}s^{-1}$, amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) TFTs are nearly unaffected by the choice of the substrate (rigid or flexible), and offer mobilities around 10 $cm^2V^{-1}s^{-1}$ even when deposited at room temperature [5]. Besides the mobility, there are other important parameters to take into account for device performance, such as threshold voltage V_{th}, on-off current ratio I_{on}/I_{off}, and subthreshold swing SS. TFT performance parameters aim at a large I_{on}/I_{off}, a small SS, and a V_{th} which allows TFT operation between 0 V and 5 V. One important factor which influences the TFT performance is the capacitance of the gate insulator. In the past, several groups used different double gate structures [6], [7] to increase the coupling between the gate and the channel, and thereby improve the performance

of a-IGZO TFTs, fabricated on rigid glass or Si substrates. Additionally, other approaches to increase the gate capacitance, and therefore the gate-channel coupling, are the use of high-k materials [8], or thinner gate oxide layers.

In this work, the double gate concept was combined with a 10 nm thin gate oxide and applied to a-IGZO TFTs fabricated on free standing flexible plastic foils. The bottom and the top gate were electrically connected to form an a-IGZO TFT controllable with a single gate voltage, and ensure comparability with standard TFT designs. The resulting n-type a-IGZO TFTs showed improved performance, and remained fully operational while subjected to mechanically induced strain of 0.55 %. A-IGZO double gate TFTs while flat, as well as under mechanical strain, exhibit subthreshold slopes of 69 mV/decade and on-off current ratios $>10^9$. In addition, the transconductance g_m of double gate TFTs was increased by 92 % when compared to single bottom gate reference TFTs fabricated on the same substrate, and measured at the same gate voltage above threshold (over-bias voltage).

3.2 Fabrication

A micrograph of a fully processed flexible a-IGZO double gate TFT and the corresponding device cross section are shown in Figure 3.1. To ensure the successful fabrication of the presented a-IGZO double gate TFTs on flexible substrates, the following points had to be considered during the design:

- Atomic layer deposition (ALD) enables the deposition of thin (10 nm) and pinhole free aluminum oxide (Al_2O_3) insulation layers with good sidewall coverage. Additionally, ALD deposited Al_2O_3 provides a dielectric constant ϵ_r of 9.5.

- Evaporated Ti and Cr provide sufficient adhesion on polyimide and a-IGZO, suitable for the fabrication of flexible TFTs. Additionally, the work functions of these two materials are comparable (ϕ_{Ti} =4.33 eV, ϕ_{Cr} =4.44 eV) [9]. Therefore the work functions influence on the threshold voltage can be neglected if Ti and Cr gate contacts are compared.

- Ti, in contrast to other metals e.g. Au, Cu or Al, has a high resistance against all wet etchants used to structure Al_2O_3, a-IGZO, and Cr. Hence, Ti is a suitable material for the bottom

gate, which can be structured in a lift-off process, but should not be damaged by the chemicals used during further processing.

- Since wet etching is applicable to Cr, it is an appropriate material for the top gate contact.

To determine the influence of the double gate structure, flexible a-IGZO double gate TFTs, as well as standard single bottom gate reference devices were fabricated on the same free standing 50 µm thick Kapton®E polyimide foil from DuPont, using a maximum process temperature of 150 °C. The total substrate size was 7.6 cm × 7.6 cm. The manufacturing process for flexible a-IGZO TFTs on plastic substrates is described in the following paragraph:

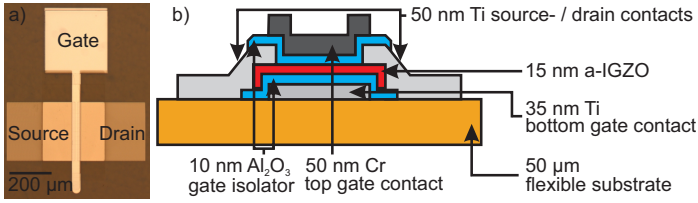

Figure 3.1: a) Micrograph of a fully processed flexible a-IGZO double gate TFT (W/L =280 µm/10 µm). b) Device cross section of double gate a-IGZO TFT including layer materials and thicknesses.

3.2.1 Single gate reference TFTs

Prior to fabrication, the substrate was cleaned by sonication in acetone and isopropanol for 5 minutes each, and was then pre-shrunk in a vacuum oven at 200°Cfor 24 h. To increase the adhesion of the successive material layers, the top surface was treated with ozone for 60 minutes, using a ultra violet ozone cleaning system. Next, negative MAN1420 photoresist and a Plassys MEB550SL e^--beam evaporation system were used to deposit 35 nm Ti and structure gate contacts in a lift-off process (photolithography mask 1). Resist leftovers were removed by an additional 60 min ozone treatment. A Picosun Sunale R-150B was used to deposit 10 nm Al_2O_3 as gate insulator by atomic layer deposition at 150 °C. Following, we deposited the 15 nm thick a-IGZO semiconducting layer using room temperature RF magnetron

sputtering in a pure Ar atmosphere and a ceramic $InGaZnO_4$. The semiconductor was patterned by standard photolithography (mask 2) and diluted hydrochloric acid [10] ($HCl : H_2O = 1 : 120$). The Al_2O_3 gate insulator was structured into islands 20 µm wider than the semiconductor islands by photolithography mask 3 and AL-11 aluminum etchant from Cyantek heated to 50 °C [11]. We deposited and structured (mask 4) source and drain contacts (50 nm Ti) similar to the gate with another e^--beam evaporation and lift-off step. A second layer of Al_2O_3 was deposited and structured identical to the gate insulation layer. This concludes the fabrication process of the standard bottom gate TFTs, which served as reference for the fabricated double gate TFTs. In this case the second Al_2O_3 layer worked as device passivation [12].

3.2.2 Double gate TFTs

Double gate TFTs with an additional top gate connected with the bottom gate were fabricated on the same substrate. Therefore, 50 % of the completed bottom gate TFTs were covered with 50 nm thick evaporated Cr. The Cr was then structured by standard photolithography and wet etching using again mask 1. The top Al_2O_3 layer served as second gate oxide in this case. Thereby the structuring of the Al_2O_3 into small islands ensured the electrical contact of the bottom and top gate on both sides of the channel region, whereas the 50 nm thick Cr is thick enough to establish a contact across the sidewalls of all previously structured layers (2×10 nm Al_2O_3 + 15 nm a-IGZO).

3.3 Results and Discussion

TFTs were characterized under ambient conditions using an Agilent technologies B1500A parameter analyzer with current-voltage, and capacitance-voltage measurement capabilities. Performance parameters were extrapolated from the transfer characteristics measured in the saturation regime using standard MOSFET equations to model the transistor current [9].

3.3.1 TFT characteristics

Figures 3.2a and 3.3a show transfer and corresponding output characteristics of a reference bottom gate a-IGZO TFT (W/L: 280 µm/10 µm),

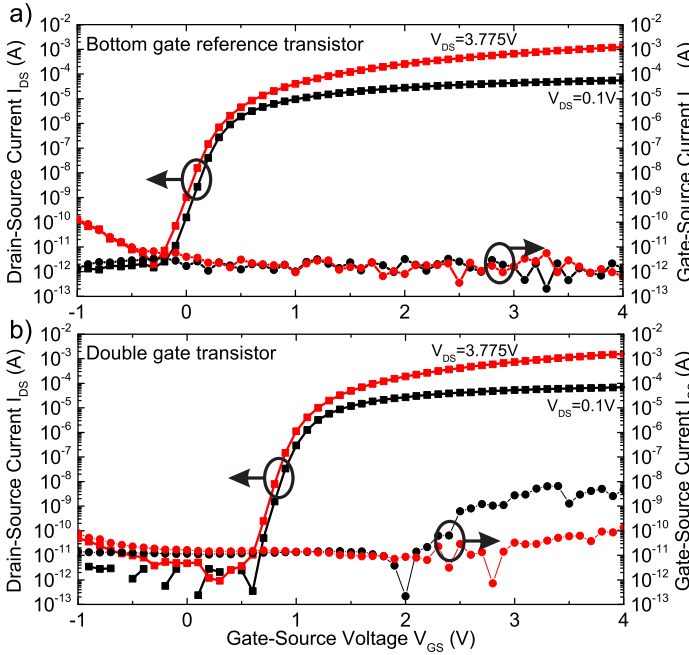

Figure 3.2: Typical a-IGZO TFT (W/L = 280 µm/10 µm) transfer characteristics measured in the linear and the saturation regime; a) bottom gate reference transistor, and b) double gate transistor manufactured on the same substrate.

and Figures 3.2b and 3.3b the equivalent measurements for an a-IGZO double gate TFT. The most obvious difference between the bottom gate and double gate TFTs is the change of the threshold voltage. The additional gate shifts V_{th} by +0.7 V from 0.25 V (bottom gate TFT) to 0.95 V (double gate TFT). This shift is caused by the changed geometry [13] and in good agreement with previously published double gate TFTs [14]. Additionally, the higher V_{th} value of 0.95 V ensures that the double gate TFT is totally turned off at V_{GS} =0 V, and therefore reduces the source-drain off-current by more than three orders of magnitude from 8.8 nA to 3.3 pA. For easier comparison the following graphs are normalized by the different threshold voltages and show all measurement results depending on the over-bias voltage $V_{OB} = V_{GS} - V_{th}$.

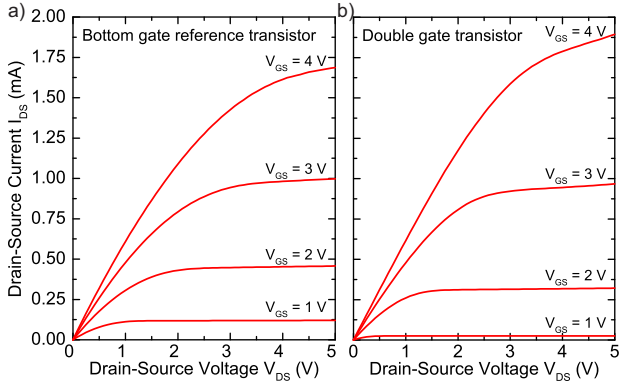

Figure 3.3: Typical a-IGZO TFT (W/L = 280 µm/10 µm) output characteristics; a) bottom gate reference transistor, and b) double gate transistor manufactured on the same substrate.

Figure 3.4 compares the total measured gate capacitance C_G of a bottom gate reference TFT and a double gate TFT (measured while source and drain are grounded). The W/L ratios are 280 µm/10 µm. The measurement shows the increased gate capacitance, and therefore stronger coupling between the gate contact and the TFT channel, of the double gate TFT (Figure 3.4). Due to the additional top gate, the area which defines the absolute capacitance is increased. The increased gate area of the double gate TFT results in a gate capacitance of 191 pF in the on regime (V_{OB} =2 V). In contrast, the gate capacitance of the corresponding bottom gate reference TFT is 107 pF under equal measurement conditions. This corresponds to an by ≈78 % increased C_G of the double gate TFT. The relative increase of the capacitance is nearly independent of the bias voltage, and also shown in Fig. 3.4. In particular the overlap capacitance between gate and the source / drain contacts (measured at negative bias voltages) as well as the total gate capacitance (overlap capacities + channel capacitance, measured at positive bias voltages) is increased in the same way.

The stronger coupling between the gate and the channel of the double gate TFT compared to the reference single bottom gate TFT has a direct influence on the drain-source current I_{DS}, which is increased from 338 µA to 702 µA (V_{OB} =2 V). This corresponds to an increase of ≈108 %.

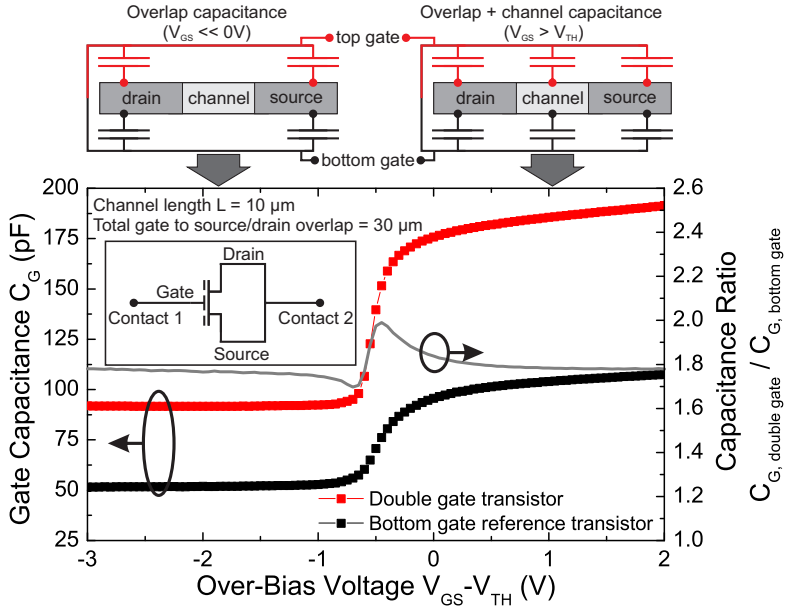

Figure 3.4: Measured absolute gate capacitance C_G, and ratio between C_G of a double gate TFT, and a corresponding bottom gate reference TFT. The measurement principle is shown in the inset. The W/L ratios are 280 µm/10 µm, the gate to drain and gate to source overlap length were 15 µm each.

Besides the increased capacitance of the gate contact, also the effective field effect mobility is increased from 8.3 $cm^2V^{-1}s^{-1}$ for the bottom gate reference TFT to 8.5 $cm^2V^{-1}s^{-1}$ for the double gate TFT (the calculation considers the measured gate capacitance increase of the double gate TFT). The small increase of 2.5 % is within the process variations of the presented flexible a-IGZO TFT. At the same time a small increase of the effective mobility in double gate transistors was also correlated with a reduced interface scattering, due to the reduced lateral electric field, in the past [14].

The transconductance $g_m = \partial I_{DS}/\partial V_{GS}$ for the reference single bottom gate TFT and the double gate TFT is shown in Figure 3.5. The Figure also shows the transconductance ratio between the two TFTs, and the square root of the drain current used to calculate g_m. Due to the

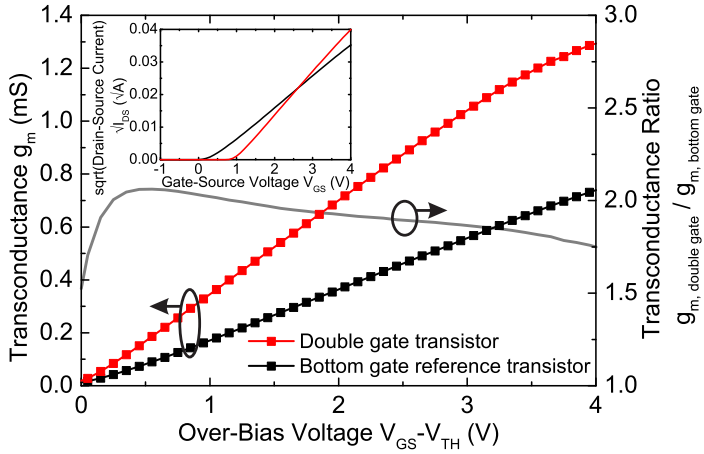

Figure 3.5: Calculated transconductance of an a-IGZO double gate TFT, and corresponding bottom gate reference TFT for different values of over bias (V_{GS} - V_{th}) at V_{DS} =3.775 V, and the ratio between the transconductance values of double and bottom gate TFT. The W/L ratio is 280 µm/10 µm. The inset shows the square root of I_{DS} used for the calculation.

higher gate capacitance, and slightly increased mobility of the double gate TFTs, g_m exhibits a steeper slope. The absolute value of g_m at V_{OB} = 2 V is increased from 364 µS to 700 µS due to the additional top gate. This corresponds to an increase of ≈92 %.

The on-off current ratio is mainly improved due to the increased gate capacitance and therefore maximum drain-source current while the off current is nearly unaffected by the additional top gate. The double gate TFT reaches a value of 2×10^9, which is a factor 2.2 higher than the on-off current ratio of the bottom gate reference TFT.

The subthreshold swings (inverse of subthreshold slope), for the double gate a-IGZO TFT and the reference single bottom gate TFT, are investigated in Figure 3.6. In Figure 3.6a the subthreshold region of the transfer characteristic from Figure 3.2 is magnified for both TFTs. It is visible that the double gate TFT exhibits a steeper slope. This is confirmed in Figure 3.6b were the subthreshold swing is calculated using $(\partial \log I_{DS}/\partial V_{GS})^{-1}$. Compared to [15] where bottom gate a-IGZO TFTs with a similar geometry, but 25 nm thick Al_2O_3 gate oxide exhibited

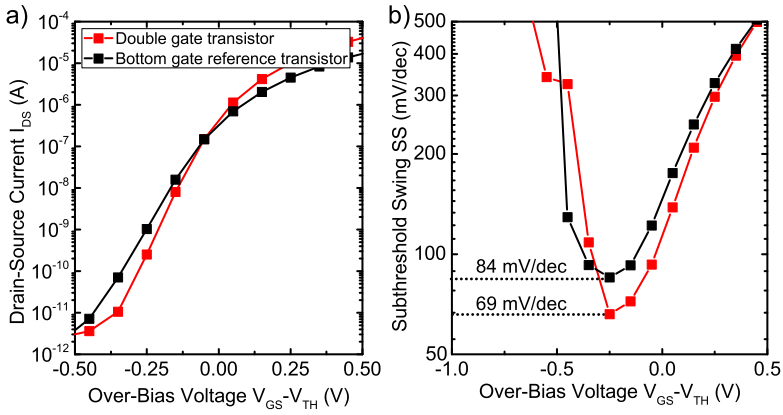

Figure 3.6: a) Enlargement of the subthreshold region of a double gate a-IGZO TFT and a corresponding bottom gate reference TFT. b) Extracted subthreshold swing $(\partial \log I_{DS}/\partial V_{GS})^{-1}$ of the measurement shown in (a) for different over-bias voltages.

a SS of 180 mV/decade, the reference bottom gate TFT in this paper showed a decreased SS of 84 mV/decade (this is due to the decreased oxide thickness and therefore increased capacitance). Furthermore, the additional top gate of the double gate a-IGZO TFT further improves the control of the channel potential [13] and reduces SS to 69 mV/decade.

The performance parameters of double gate TFTs and corresponding reference bottom gate TFTs are summarized in Table 3.1.

However, due to the thin gate oxide and the added top gate additional effects were observed. First, tunneling of carriers through the 10 nm thin gate oxide (single and double gate TFT) increases the gate leakage current I_{GS} in the "off" state (Figure 3.2). The tunnel current increases with increasing V_{DS}, but does not impair devices operated with a supply voltage of 5 V. Second, the larger interface area of the double gate TFT increases the gate leakage current I_{GS} (Figure 3.2b) by at least one order of magnitude.

3.3.2 Stability

The electrical stability of bottom gate reference- and double gate a-IGZO TFTs, was determined by standard gate bias stress measure-

Table 3.1: Performance parameters of a-IGZO double gate TFTs and bottom gate reference TFTs.

Parameter	Transistor		
	Bottom gate reference	Double gate	Relative change
Gate capacitance (V_{OB} =2 V)	107 pF	191 pF	+78 %
Field effect mobility	8.3 $cm^2V^{-1}s^{-1}$	8.5 $cm^2V^{-1}s^{-1}$	+2.5 %
Transconductance (V_{OB} =2 V)	364 µS	700 µS	+92 %
Threshold voltage	250 mV	950 mV	+700 mV
On-off ratio	9×10^8	2×10^9	×2.2
Subthreshold swing	84 mV/decade.	69 mV/decade.	-18 %

ments [16]. First, the TFT transfer characteristic was measured. Then, gate bias stress voltages between 0.1 V and 3 V were applied to the gate contact while source and drain contacts were grounded. In reference to the 10 nm thick gate insulator, this corresponds to a gate bias stress field (E_{Str}) between 1×10^7V m^{-1} and 3×10^8V m^{-1}. The gate bias stress field was always applied for a time period t_{GB-Str} of 300 s. Afterwards, a second measurement of the TFT transfer characteristic was used to determine the threshold voltage shift (ΔV_{th}). A new a-IGZO TFT was used for each measurement point. Figure 3.7 shows the observed results for bottom gate TFTs and double gate TFTs. The flexible bottom gate and double gate a-IGZO TFTs exhibit maximum threshold voltage shifts of ≈33 mV (single gate reference TFT) and ≈99 mV (double gate TFT). Thanks to the Al_2O_3 passivation layer [12], these values are small compared to unpassivated bottom gate a-IGZO TFTs [17]. Nevertheless the measurement also shows a significant difference between the gate bias stress stability of bottom gate reference- and double gate a-IGZO TFTs:

In contrast to the bottom gate reference TFTs, the double gate TFTs show a positive shift of the threshold voltage for all applied gate bias voltages. Additionally, the absolute value of ΔV_{th} is larger for double gate TFTs. This can be explained by the injection of electrons into the gate dielectric and the subsequent screening of the gate voltage [18]. Due to their larger gate area, this has a bigger effect on double gate TFTs. While the same effect also explains the positive threshold voltage shift of the bottom gate reference TFTs at high stress fields, the partially negative threshold voltage shift of the bottom gate reference TFTs at low stress fields can be explained by the interaction of the TFT with the environment.

It is known that oxide semiconductor based transistors with applied positive gate voltages are influenced by the absorption of oxygen (O_2) and desorption of water (H_2O) molecules [19], which act as acceptors in a-IGZO [20]. Since the bottom gate reference TFTs are passivated with a 10 nm thick aluminum oxide layer, the permeability of the Al_2O_3 has to be taken into account when the absorption of oxygen and water is discussed. According to the measurements performed in [21], an 8 nm thick aluminum oxide layer on PET foil has an oxygen transmission rate (WVTR) of $\approx 1.26 \times 10^{-4}$mol/m^2 per day, and a water vapor transmission rate (OTR) of $\approx 6.61 \times 10^{-2}$mol/m^2 per day. Therefore, the OTR is a factor ≈500 larger than the WVTR, and the absorption ($V_{GS}<0$) and desorption ($V_{GS}>0$) of water will dominate the interaction between

the TFT and the environment. Positive gate voltage stress causes the desorption of water at the backchannel of a-IGZO TFTs and thereby increases the electron concentration in the a-IGZO (the less important adsorption of oxygen under positive gate bias stress would decreases the electron concentration) [22]. The increased electron density then leads to a negative shift of the threshold voltage. This effect is less dominant for the double gate TFTs since the additional 50 nm thick Cr top gate should be a more effective barrier against water permeation compared to the only 10 nm thick Al_2O_3 passivation layer of the bottom gate reference TFT.

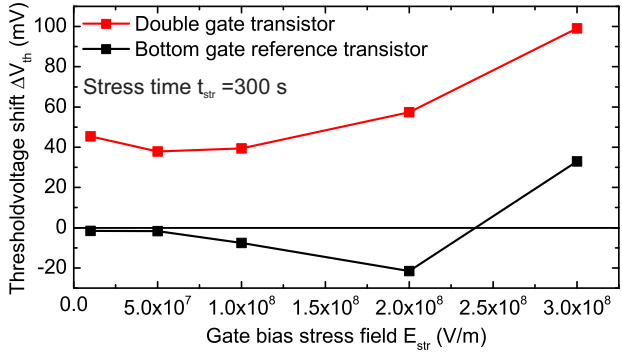

Figure 3.7: Threshold voltage shift of a-IGZO double gate TFTs and bottom gate reference TFTs induced by different gate bias stress fields. Source and drain contacts were grounded while stress voltage was applied to the gate contact. Stress was applied for a time period of 300 s.

The long term stability of the TFTs was evaluated by measuring their transfer characteristics before and after defined time intervals, whereas no voltage was applied to the TFTs in between [23]. Figure 3.8 shows the threshold voltage shift ΔV_{th} for an a-IGZO double gate TFT and a corresponding bottom gate reference TFT. The threshold voltage shifts are shown relative to the first measurement of the respective TFT performed at t_{LT} =0 s. The time interval between the measurements was continuously increasing from 30 s up to 80 h), whereas the accumulated time between the first and the last measurements was $t_{LT} = 6 \times 10^5$s (≅166 h). Both TFTs were measured in the saturation regime using the same maximum V_{GS} of 3 V. The bottom gate reference TFT shows

a continuous shift of the threshold voltage towards higher voltages (+90 mV after ≅166 h). This shift is due to the measurement itself: The measurement of the transfer characteristic takes approximately 20 s. During this time gate voltages up to 3 V which act as gate bias stress voltage are applied to the TFT. Similar to the gate bias stress experiment described above, this lead to the injection of electrons into the oxide, a screening of the gate potential and a positive shift of the threshold voltage. Additionally to this direct effect, the electrons trapped in the oxide have also an effect on the water absorption and desorption during the time intervals without external gate voltages. Since the trapped electrons behave like a negative gate voltage, the absorption of water decreases the electron concentration in the a-IGZO channel [22] and causes an additional positive shift of the threshold voltage.

The double gate TFT shows a different behavior which can be separated into two main effects: In region I ($t < \approx 10\,000$ s) the double gate TFT exhibits a continuously increasing threshold voltage, the shift is a factor 2 - 3 larger than the threshold voltage shift of the single gate TFT (+70 mV after 7200 s ≅2 h). In region II ($t > \approx 10\,000$ s) the threshold voltage nearly recovered to its original value, and a nearly time independent threshold voltage shift of ≈10 mV is observed. The described behavior was observed during several independent measurements. Similar to the bottom gate reference TFT, the threshold voltage shift of the double gate TFT in region I can be explained by the electrical gate bias stress induced by the measurement itself, causing charge injection into the gate oxide. Since the double gate TFTs are more sensitive to gate bias stress the measured threshold voltage shift is larger than for bottom gate reference TFTs. The observed threshold voltage shifts corresponds well with the shifts obtained from the gate bias stress measurements (compare Figure 3.7). As for the gate bias stress experiment the absorption of water is less important for double gate TFTs since they are better encapsulated by the additional top gate. In region II the time intervals between the single measurements are larger than in region I (ranging from 1.5 h to 80 h), therefore the time intervals are long enough for the double gate TFT threshold voltage to relax back to the initial value after the gate bias stress during each measurement [24]. At the same time the threshold voltage of the bottom gate reference TFT continues increasing, which can be explained by the additional effect of the absorbed water. Here, the measurement suggests that the positive threshold voltage shift induced by the absorbed water has a relaxation

time longer than the longest time intervals in this experiment (80 h). The long term stability measurement shows that the encapsulation of the double gate TFTs (additional 50 nm Cr top gate) reduces the interaction of the TFT with the environment, and leads to a better long term device stability when compared to the bottom gate reference TFT.

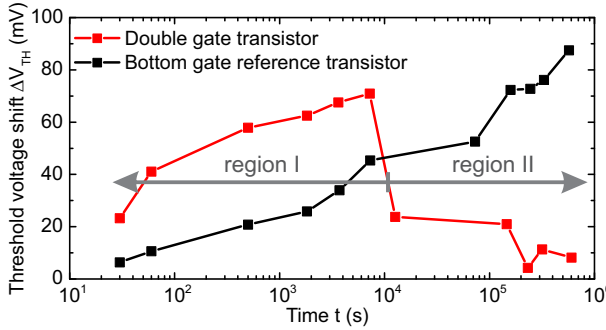

Figure 3.8: Threshold voltage shift of the same a-IGZO double gate TFT and bottom gate reference TFT measured after different time periods. No voltage was applied between the measurements.

3.3.3 Bendability

To investigate the flexibility of the fabricated a-IGZO double gate TFTs in comparison to the bottom gate reference TFTs, bending tests were performed as follows: Prior to any bending the transfer characteristic and the gate capacitance of the TFTs were measured. Next, TFTs were attached to double sided tape and wound around rods, in the way that tensile strain was applied parallel to the TFT channel. Afterwards, the bent transistors were contacted with probe needles as usual, and re-measured [25]. The radius of the employed rods was subsequently reduced to evaluate the minimum possible bending radius. Figure 3.9 shows a photograph of the bent and contacted double gate TFT. The transfer characteristic of an a-IGZO bottom gate reference TFT and a double gate TFT (W/L =280 µm/35 µm) before bending, and while bent to the minimum possible bending radius is shown in Figure 3.10. The measurement demonstrates that the transistors remained fully operational when bent, but also shows that the minimum bending radius

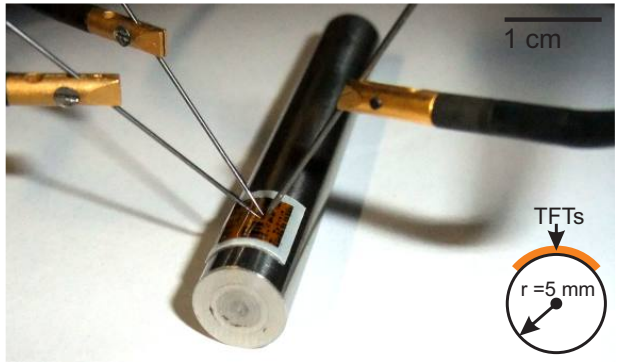

Figure 3.9: Photograph of a flexible substrate, including contacted double gate a-IGZO TFTs, bent to a tensile radius of 5 mm parallel to the TFT channel.

before the TFT is destroyed is different for bottom gate and double gate TFTs. While the flexible bottom gate reference TFTs can be bent to a radius of 3.5 mm, the double gate TFTs are destroyed at radii <5 mm. These bending radii correspond to tensile mechanical strain ϵ of 0.72 % and 0.55 % in the TFT channel. The values are calculated using the strain theory developed in [26] using the layer thicknesses and properties of the tested TFTs, and the initial bending of the free standing substrate (build in strain). Beside the different minimum bending radius, the influence of strain on the performance parameters of bottom gate reference TFTs and a double gate TFTs is also different. The bottom gate reference TFT (Figure 3.10a) shows an increase of the field effect mobility and a decrease of the threshold voltage by +2 % and -75 mV. These results are in line other bending experiments of flexible a-IGZO TFTs [27], and discussed in detail e.g. in [15]. At the same time, the applied tensile strain induced a positive threshold voltage shift of 25 mV and a reduction of the effective field effect mobility by 7 % of the double gate TFT (Figure 3.10b).

The gate capacitance of a bottom gate reference TFT and a double gate TFT both with a W/L ratio of 280 µm/35 µm measured while flat and bent are plotted in Figure 3.11. At an over-bias voltage of 0 V the gate capacitance slightly increases for the bottom gate reference TFT as well as for the double gate TFT by +0.7 % and +1.2 %, respectively.

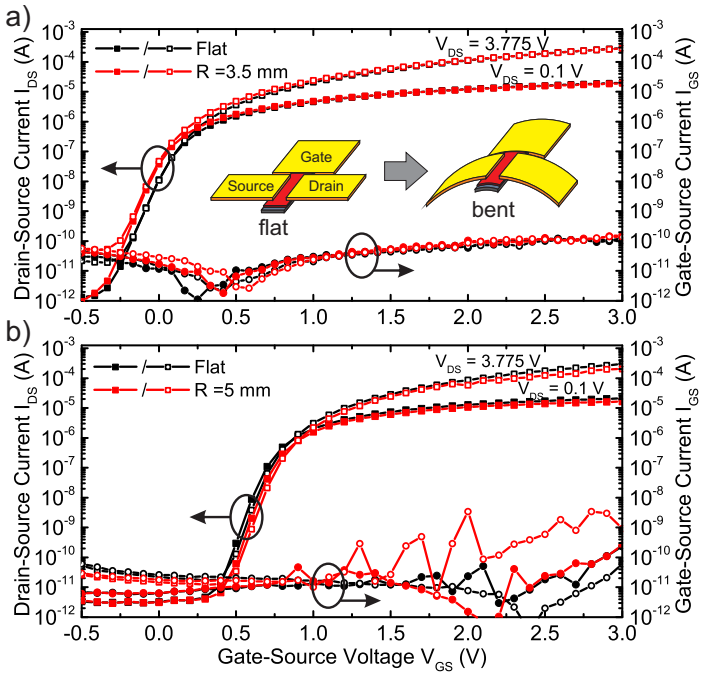

Figure 3.10: Transfer characteristic of the same a-IGZO TFTs (W/L =280 µm/35 µm) measured while flat and bent. a) bottom gate reference TFT bent to a tensile radius of 3.5 mm, b) double gate TFT bent to a tensile radius of 5 mm.

Although there is some noise visible in the measurements, the average increase of C_G due to bending is ≈1 % for bottom and double gate TFTs, and is also nearly independent of the bias voltage. This increase can be correlated to the by strain increased area of the TFT channel region and the, by the Poison effect, reduced thickness of the layer stack [28]. The measurement shows that the change of C_G and therefore the channel area is approximately the same for double gate and bottom gate TFTs, and that these change exhibits a value comparable to the value of the mechanically induced strain.

At the same time the different shift of the TFT field effect mobility and threshold voltage under strain for double gate and bottom gate TFTs, as well as their different minimum bending radii indicates a sig-

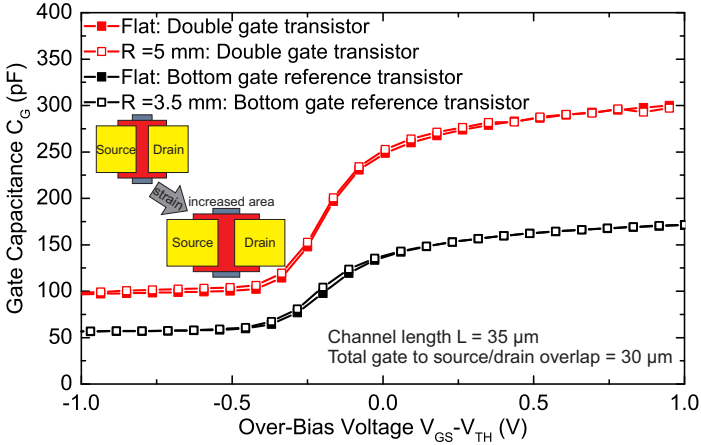

Figure 3.11: Gate capacitance of a bottom gate reference TFT and a double gate TFT (W/L =280 µm/35 µm) measured while flat, and bent to a tensile radius of 5 mm.

nificant change of the mechanical properties by the additional 50 nm thick Cr top gate contact. Figure 3.12a illustrates how the deposition of 50 nm thick evaporated Cr on bare polyimide foil introduces strain. Prior to the Cr deposition the polyimide foil was absolutely flat, after the Cr evaporation the substrate shows an inward curvature with a bending radius of ≈3.5 cm. Therefore the Cr on the polyimide foil is exposed to tensile strain while the surface of the flexible substrate is exposed to compressive strain when no external force is applied. Considering this build in strain and the fact that Cr is a quite brittle material [29] it is expectable that the double gate TFTs are less resistant to bending. Figure 3.12b shows a micrograph of a double gate a-IGZO TFT while bent to a radius of 3.5 mm (corresponds to a strain of 0.79 %, when the initial curvature of the substrate is taken into account). In contrast to the bottom gate reference TFT, the micrograph shows multiple cracks perpendicular to the applied strain and therefore parallel to the TFT channel. The cracks are formed only in areas covered with the Cr top gate, but e.g. not on the more ductile Au contacts. Furthermore no cracks have been observed when bottom gate reference TFTs were bent to a tensile radius of 3.5 mm. The formation of cracks explains the different behavior of the double gate TFT under strain compared to

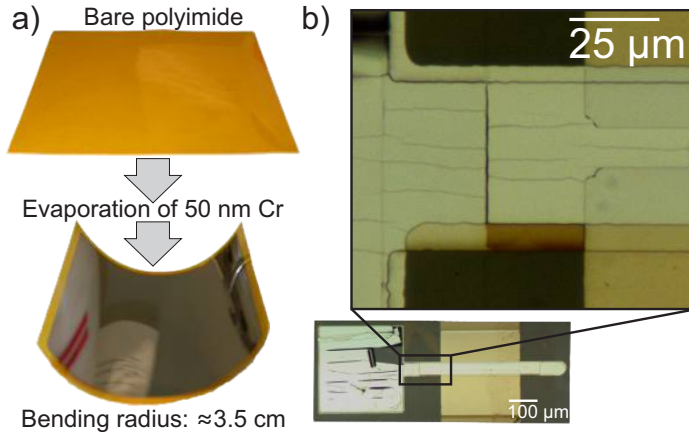

Figure 3.12: a) Photograph of a blank polyimide substrate, and a substrate coated with 50 nm of evaporated Cr. The curvature illustrates the build in strain. b) Optical micrograph of a double gate a-IGZO TFT bent to a tensile radius of 3.5 mm, cracks, parallel to the TFT channel are formed in the Cr top gate contact.

strained bottom gate reference TFTs. We believe that the use of more ductile metals like Cu as top gate contact would enable bending radii between 1 mm and 2 mm without the need of modifying the device structure, but at the cost of an even higher work function compared to Ti (ϕ_{Cu} =4.54 eV) [9].

3.4 Conclusion

A double gate structure was combined with 10 nm thick Al_2O_3 gate oxide layers to fabricate TFTs on free standing flexible plastic foils. Double gate a-IGZO TFTs yield improved performance parameters compared to single bottom gate reference TFTs fabricated on the same substrate. The by 74 % increased absolute gate capacitance increased the transconductance up to 92 % (V_{OB} =2 V). On-off current ratio increased by more than a factor of 2, while the subthreshold swing reached a value of 69 mV/decade. This is to our knowledge the smallest value ever reported on flexible a-IGZO TFTs. Although double gate TFTs are less resistant to mechanical strain than bottom gate reference TFTs, tensile

mechanical strain of 0.55 %, induced by bending the flexible a-IGZO double gate TFTs to a radius of 5 mm did not impair the device functionality significantly. In particular, the subthreshold swing remained unchanged while μ_{FE} decreased by 7 % and V_{th} increased by 25 mV.

Acknowledgment

This work has been partially supported by the European Commission through the FP7 Project: Flexible multifunctional bendable integrated light-weight ultra-thin systems (FLEXIBILITY), contract No: FP7-287568. This work has also been scientifically evaluated by the Swiss National Scientific Foundation (SNSF), and financed by the Swiss Confederation and Nano-Tera.ch.

Bibliography

[1] K. Cherenack, C. Zysset, T. Kinkeldei, N. Münzenrieder, and G. Tröster. Woven electronic fibers with sensing and display functions for smart textiles. *Advanced Materials*, 22(45):5178–5182, 2010.

[2] R.F. Service. Patterning electronics on the cheap. *Science*, 278:383–384, 1997.

[3] W. Li, H.E. Katz, A.J. Lovinger, and J.G. Laquindanum. Field-effect transistors based on thiophene hexamer analogues with diminished electron donor strength. *Chemistry of materials*, 11(2):458–465, 1999.

[4] K.H. Cherenack, A.Z. Kattamis, B. Hekmatshoar, J.C. Sturm, and S. Wagner. Amorphous-silicon thin-film transistors fabricated at 300 °C on a free-standing foil substrate of clear plastic. *Electron Device Letters, IEEE*, 28(11):1004–1006, 2007.

[5] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, 432(7016):488–492, 2004.

[6] H. Lim, H. Yin, J.S. Park, I. Song, C. Kim, J.C. Park, S.I. Kim, S.W. Kim, C.B. Lee, Y.C. Kim, Y.S. Park, and D. Kang. Double gate gainzno thin film transistors. *Applied Physics Letters*, 93(6):063505–063505, 2008.

[7] H.W. Zan, W.T. Chen, C.C. Yeh, H.W. Hsueh, C.C. Tsai, and H.F. Meng. Dual gate indium-gallium-zinc-oxide thin film transistor with an unisolated floating metal gate for threshold voltage modulation and mobility enhancement. *Applied Physics Letters*, 98(15):153506–153506, 2011.

[8] N.C. Su, S.J. Wang, and A. Chin. High-performance ingazno thin-film transistors using hflao gate dielectric. *Electron Device Letters, IEEE*, 30(12):1317–1319, 2009.

[9] S.M. Sze and K.K. Ng. *Physics of Semiconductor Devices*. John Wiley and Sons, 2007.

[10] J.B. Kim, C. Fuentes-Hernandez, W.J. Potscavage Jr, X.-H. Zhang, and B. Kippelen. Low-voltage ingazno thin-film transistors with alo gate insulator grown by atomic layer deposition. *Applied Physics Letters*, 94:142107, 2009.

[11] B. Zhou and W.F. Ramirez. Kinetics and modeling of wet etching of aluminum oxide by warm phosphoric acid. *Journal of The Electrochemical Society*, 143(2):619–623, 1996.

[12] I.T. Cho, J.M. Lee, J.H. Lee, and H.I. Kwon. Charge trapping and detrapping characteristics in amorphous ingazno tfts under static and dynamic stresses. *Semiconductor Science and Technology*, 24(1):015013, 2008.

[13] S. Zhang, R. Han, J.K.O. Sin, and M. Chan. A novel self-aligned double-gate tft technology. *Electron Device Letters, IEEE*, 22(11):530–532, 2001.

[14] K.-S. Son, J.-S. Jung, K.-H. Lee, T.-S. Kim, J.-S. Park, Y.-H. Choi, K.C. Park, J.-Y. Kwon, B. Koo, and S.-Y. Lee. Characteristics of double-gate ga–in–zn–o thin-film transistor. *Electron Device Letters, IEEE*, 31(3):219–221, 2010.

[15] N. Münzenrieder, K.H. Cherenack, and G. Tröster. The effects of mechanical bending and illumination on the performance of flexible IGZO TFTs. *IEEE Transactions on Electron Devices*, (99):1–8, 2011.

[16] K. Hoshino, D. Hong, H.Q. Chiang, and J.F. Wager. Constant-voltage-bias stress testing of a-igzo thin-film transistors. *Electron Devices, IEEE Transactions on*, 56(7):1365–1370, 2009.

[17] J.M. Lee, I.T. Cho, J.H. Lee, and H.I. Kwon. Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in ingazno thin film transistors. *Applied Physics Letters*, 93(9):093504–093504, 2008.

[18] A. Suresh and J.F. Muth. Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors. *Applied Physics Letters*, 92(3):033502–033502, 2008.

[19] P.-T. Liu, Y.-T. Chou, and L.-F. Teng. Environment-dependent metastability of passivation-free indium zinc oxide thin film tran-

sistor after gate bias stress. *Applied Physics Letters*, 95(23):233504–233504, 2009.

[20] J.-S. Park, J.K. Jeong, H.-J. Chung, Y.-G. Mo, and H.D. Kim. Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water. *Applied Physics Letters*, 92(7):072104–072104, 2008.

[21] B.M. Henry, A.G. Erlat, A. McGuigan, C.R.M. Grovenor, G.A.D. Briggs, Y. Tsukahara, T. Miyamoto, N. Noguchi, and T. Niijima. Characterization of transparent aluminium oxide and indium tin oxide layers on polymer substrates. *Thin Solid Films*, 382(1):194–201, 2001.

[22] J.K. Jeong, H. Won Yang, J.H. Jeong, Y.-G. Mo, and H.D. Kim. Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors. *Applied Physics Letters*, 93(12):123508–123508, 2008.

[23] W. Lim, S.H. Kim, Y.L. Wang, J.W. Lee, D.P. Norton, S.J. Pearton, F. Ren, and I.I. Kravchenko. Stable room temperature deposited amorphous ingazno4 thin film transistors. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 26(3):959–962, 2008.

[24] J.S. Jung, S.H. Rha, U.K. Kim, Y.J. Chung, Y.S. Jung, J.H. Choi, and C.S. Hwang. The charge trapping characteristics of si3n4 and al2o3 layers on amorphous-indium-gallium-zinc oxide thin films for memory application. *Applied Physics Letters*, 100:183503, 2012.

[25] N. Münzenrieder, C. Zysset, T. Kinkeldei, and G. Tröster. Design Rules for IGZO Logic Gates on Plastic Foil Enabling Operation at Bending Radii of 3.5 mm. *IEEE Transactions on Electron Devices*, 59(8):2153–2159, 2012.

[26] H. Gleskova, S. Wagner, and Z. Suo. a-si: H thin film transistors after very high strain. *Journal of Non-Crystalline Solids*, 266:1320–1324, 2000.

[27] D.I. Kim, B.U. Hwang, J.S. Park, H.S. Jeon, B.S. Bae, H.J. Lee, and N.-E. Lee. Mechanical bending of flexible complementary inverters based on organic and oxide thin film transistors. *Organic electronics*, 13(11):2401–2405, 2012.

[28] J.R. Rice. Foundations of solid mechanics. *Mechanics and materials: fundamentals and linkages*, pages 33–69, 1999.

[29] T.C. Reiley and W.D. Nix. The structure and mechanical properties of physically vapor deposited chromium. *Metallurgical Transactions A*, 7(11):1695–1701, 1976.

4

Bending of flexible IGZO TFTs

Niko Münzenrieder, Kunigunde Cherenack, Gerhard Tröster

Testing of flexible InGaZnO-based thin-film transistors under mechanical strain

The European Physical Journal Applied Physics, vol. 55, no. 2, pp. 23904-p1–23904-p5, 2011.
10.1051/epjap/2011100416

Abstract

Thin-film transistors (TFTs) fabricated on flexible plastic substrates are an integral part of future flexible large area electronic devices like displays, and smart textiles. Devices for such applications require stable electrical performance under electrical stress and also during applied mechanical stress induced by bending of the flexible substrate. Mechanical stress can be tensile or compressive strain depending on whether the TFT is located outside or inside of the bending plane. Especially the impact of compressive bending on TFT performance is hard to measure, because the device is covered with the substrate in this case. We present a method which allows us to continuously measure the electrical performance parameters of amorphous Indium-Gallium-Zinc Oxide (a-IGZO) based TFTs exposed to arbitrary compressive and tensile bending radii. To measure the influence of strain on a TFT it is attached and electrically connected to a flexible carrier foil, which afterwards is fastened to two plates in our bending tester. The bending radius can be adjusted by changing the distance between these plates. Thus it is possible to apply bending radii in the range between a totally flat substrate and ≈1 mm, corresponding to a strain of ≈3.5 %. The tested bottom-gate TFTs are especially designed for use with our bending tester and fabricated on 50 µm thick flexible Kapton®E polyimide substrates. To show the different application areas of our bending method we characterized our TFTs while they are bent to different tensile and compressive bending radii. These measurements show that the field effect mobilities and threshold voltages of the tested a-IGZO TFTs are nearly, but not absolutely, stable under applied strain, compared to the initial values the mobilities shift by ≈3.5 % in the tensile case and ≈-1.5 % in the compressive one, at a bending radius of 8 mm. We also measured the influence of repeated bending (2500 cycles over ≈70 h), where a shift of the performance parameters can be observed, too. The saturation mobility of the flat device decreases by 4.5 %, and the threshold voltage raises 0.1 V. These results show that it is possible to characterize the influence of different kinds of bending on flexible thin-film devices in a very reliable way with one experimental setup.

4.1 Introduction

Flexible electronic devices fabricated on plastic substrates, especially thin-film transistors (TFTs), are an important part of a large number of future applications such as flexible displays, smart textiles and

other large area electronics. One key point for such applications, because of the limited temperature resistance of plastic substrates, is device fabrication at low temperatures [1]. Therefore a attractive alternative as semiconductor material are oxide semiconductors like amorphous Indium-Gallium-Zinc Oxide (a-IGZO), since they have good electrical properties (e.g. mobilities $>10\,cm^2V^{-1}s^{-1}$) even when they are deposited at room temperature [2]. Another important point is the stability under electrical stress and, especially for devices used in flexible applications, mechanical strain induced by bending of the device. While the electrical stability under gate-bias stress of IGZO TFTs is well investigated, there is no easy way to characterize the influence of different bending radii on TFTs. To our knowledge bending experiments have been carried out by other groups over a limited number of tensile bending radii on oxide semiconductor TFTs [3] or on a-Si:H TFTs for compressive strain [4], always in such a way that TFTs were bent around rods or the inner side of hollow cylinders with fixed diameters. This method is not very flexible and it is difficult to place probe tips if the bending radii are getting to small. Here we present a way, including a custom build, labview controlled, bending machine, to measure the electrical parameters of our a-IGZO TFTs for tensile and compressive strain down to bending radii <1 mm, in an automated way without the need to connect probe needles with the sample. Therefore it is possible to make reliable measurements at different bending radii without any changes of the contact resistance, between the device and the parameter analyzer. The different possible bending options are demonstrated by three different bending experiments performed with our a-IGZO TFTs showing the influence of (I) tensile strain at various bending radii, (II) compressive strain at various bending radii, and (III) repeated increasing and decreasing tensile strain over 70 h corresponding to 2500 cycles of bending and reflattening.

4.2 Experimental

4.2.1 Bending machine

Our bending tester with a mounted carrier substrate (7.6 cm × 7.6 cm), including an attached TFT, is shown in Fig. 4.1. The dimensions of the machine are approximately 18.5 cm by 12 cm and 4.5 cm in height. Bending strain can be applied to the mounted flexible foil by changing the distance between the two points where the foil is fixed. The foil is

fixed by clamping it, using two 2 mm thick metal plates and 4 screws, on the left part of the machine and on the movable slide. The slide can be moved by the rotation of a shaft screwed through it, where one complete rotation of the shaft corresponds to a movement of 1 mm. We use a 012SR DC motor, with an IE2-512 pulse generator and an attached 20/1 planetary gear, all manufactured by Faulhaber, connected to the shaft via two cogwheels and a gearbelt for the rotation. The transmission ratio of the gear is 23:1, while the cogwheel / gearbelt system does not change the angular frequency. The movement is controlled by a labview based program; therefore a computer is connected with the motor via a Faulhaber RS-232 motion controller. With this control system it is possible to drive the slide to certain positions and also to cycle between 2 different positions at a maximum speed of 1 mm s^{-1}, adjustable in steps of 0.01 mm s^{-1}. Additionally a CCD camera can be mounted in front of the carrier substrate to monitor the actual bending of the foil. The exact measurement of the bending radius in the middle of the substrate, where the active channel of the TFT and the highest strain is located, is done by fitting circles into the pictures taken with the camera.

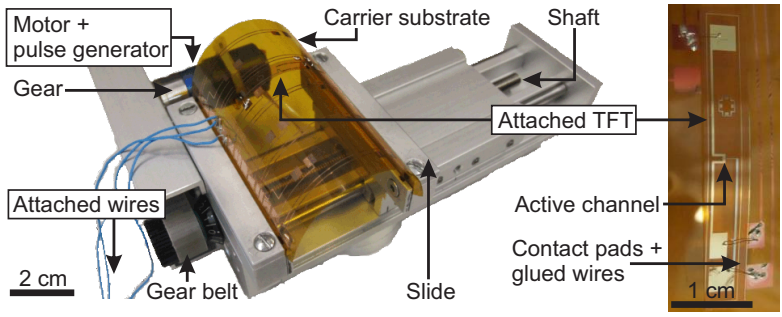

Figure 4.1: Photo of our custom built bending tester with a loaded carrier substrate and an attached flexible TFT bent to a radius of ≈19 mm. The TFT is loaded to apply tensile strain parallel to the length of the channel.

4.2.2 Bending properties

There are two major operating modes of our bending tester. (I) shown in Fig. 4.1, able to bent the transistors -starting from a flat substrate- down to radii of ≈8 mm, and (II) where spacers (glass plates) attached at the bending tester are used to decrease the minimum possible bending radius below 1 mm. The typical minimum bending radius of our TFTs is larger than 1 mm. These spacers clog the substrate to expand over the machine, and have to be not conductive to prevent shortcuts on the carrier foil.

The plate spacing versus the bending radius of the TFT loaded into the bending machine with and without glass spacers and the applied strain to our TFTs calculated using the strain theory developed in [5] can be seen in Fig. 4.2. Without spacers the maximum strain is limited to ≈0.4 %, but this value can be increased to >3.5 % with the glass plates.

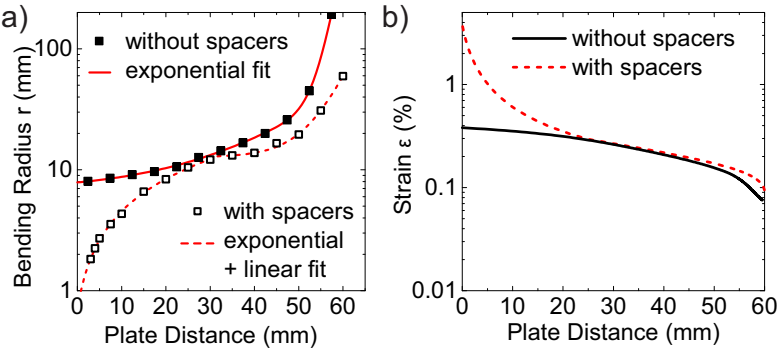

Figure 4.2: a) Measured bending radius of the TFT. Without spacers the behavior of the bending radius can be fitted by an exponential function, while the measurement with glass spacers is fitted by an exponential (distances >32.5 mm) and a linear function (distances <32.5 mm, here the carrier is in large-area contact with the spacers). b) Calculated strain vs. plate distance for tensile strain.

4.2.3 Mounting process

To attach one of our TFTs to the carrier substrate, to be mounted to the bending machine we perform the following steps: our TFTs are fabricated in a stripe design (34.5 mm × 4.75 mm) especially designed for bending experiments, therefore they have three very large contact pads (≈ 3 mm × 3 mm) connected to the active region located exactly in the middle of the stripe. A schematic drawing of a TFT stripe is shown in Fig. 4.3. These stripes are separated with a scissor along dicing streets surrounding them. Alignment marks on the carrier substrate indicating the place where the TFT stripe should be placed, to ensure that the active region is positioned exactly in the middle on the carrier substrate, because this is the place with the highest curvature. Before we attach the TFT stripe to the carrier substrate we solder three flexible wires onto the three large 600 nm thick Cu contact pads at the edge of the carrier substrate, these three large contact pads are connected with three smaller one near the TFT mounting region via 300 µm wide Cu lines. The free ends of the soldered wires can be connected with a HP4156A parameter analyzer. We have made the experience that the TFT often is not working anymore if it is attached before the soldering step, maybe because of the evaporating parts of the solder. Afterwards both ends of the TFT stripe are fixed, at the marked position, with a small (≈ 2 mm × 3 mm) piece of double sided tape. To establish an electrical contact between the TFT contact pads and the Cu pads beside the TFT on the carrier substrate, we use enameled copper wire with a diameter of 0.09 mm. The insulation layer is removed with a razorblade. Afterwards we use approximately 4 mm long pieces of wire to form small arches using a tweezers. Both ends of this wire arches are dipped into conductive epoxy EE129-4 from Epoxy Technology, and the wire is placed in a way that it connects one pad of the TFT and one pad on the carrier substrate. This procedure has to be repeated to connect all three (gate, source, and drain) contacts. After the gluing the epoxy has to be cured at room temperature for at least 24 h. The connections with the contact pads on the carrier substrate are shown in Fig. 4.3, too. Two additional Cu lines on the carrier substrate which can be used to align the carrier foil in the bending machine are used to ensure that the substrate is loaded in the same way every time, and that the TFT is located exactly in the middle between the 2 movable plates of the bending machine. After the mounting the carrier foil to the bending machine the soldered wires should always be located at the

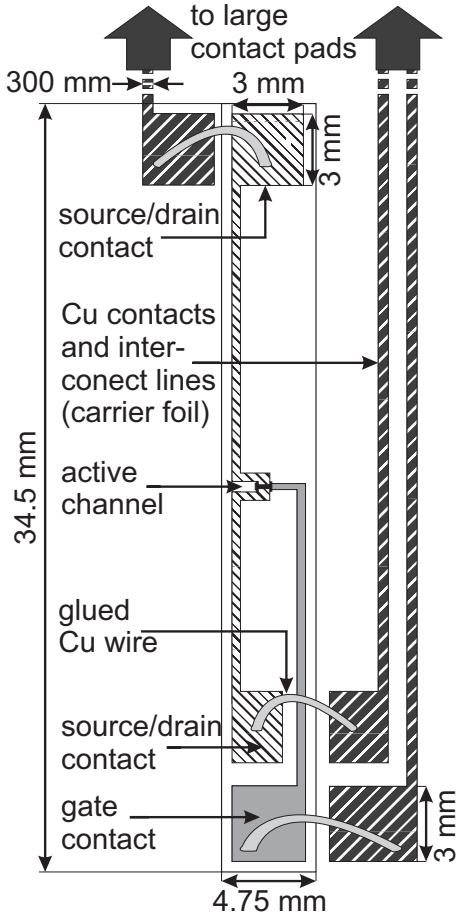

Figure 4.3: Schematic of a bending TFT stripe electrically connected to the pads on the carrier substrate.

fixed part of the machine (not at the slide), to avoid big forces due to the movement. The substrate has to insert with the TFT facing upwards to apply tensile strain, and facing downwards to apply compressive one. If spacers are needed, to bend the TFT to small radii, we add a 7.6 cm × 7.6 cm glass plate (for compressive tests) or two 2.54 cm × 7.6 cm microscope slides (for tensile test, otherwise the contact wires

can be pinched between the Kapton and the glass) on both mounting points by fixing them with the same clamps, and in the same step, as the carrier foil. This completes the TFT mounting process.

4.2.4 IGZO TFTs

We used a 50 µm thick Kapton®E substrate from DuPont that was cleaned by sonication in acetone and isopropanol, and was then pre-shrunk in a vacuum oven at 200 °C for 24 h to remove trapped residual solvents [6]. We deposited 50 nm of SiN_x on each side of the substrate using plasma enhanced chemical vapor deposition in an Oxford Instruments *PECVD80+*. Following substrate preparation, we deposited 35 nm Cr using a *Univex 500* e^--beam evaporator and patterned gates using standard photolithography. We then deposited 25 nm Al_2O_3 using atomic layer deposition in a *Picosun Sunale R-150B* at 150 °C, and 15 nm IGZO using RF sputtering at room temperature. Next, TFT islands were patterned and etched using HCl:DI water 1:120 [7]. Then, gate vias were etched using *AL-11* etchant from Cyantek heated to 50 °C [8], in the same step we also etch the Al_2O_3 and the underlying SiN_x (RIE process, Oxford Instruments Plasmalab 80+) to form dicing streets. We evaporated Ti /Au = 10 nm /60 nm contacts and structured them with a lift-off process. Finally, we deposited and patterned an additional 25 nm thick Al_2O_3 passivation layer.

4.3 Results and discussion

4.3.1 Experiment I+II: IGZO TFT bending

The standard test to characterize TFTs under bending is to measure the transfer curve while the TFT is bent to a specific radius or after it is reflattened [4]. We performed such tests on our a-IGZO TFTs for tensile (experiment I) and compressive (experiment II) bending, parallel to the channel length, and extracted the saturation field effect mobilities (μ_{sat}) and the threshold voltages (V_{th}) of the same TFT at different bending radii, using standard equations to model the TFT current [9]. We show the parameters normalized by their values measured while the TFT was not bent. The initial values of our a-IGZO TFTs are $\mu_{sat,0} \approx 10\,cm^2V^{-1}s^{-1}$ and $V_{th,0} \approx 0.8\,V$. Fig. 4.4 shows the change of the performance parameters for experiment I. The strain at the smallest measured radius was ≈0.302 %. The mobility and the threshold voltage

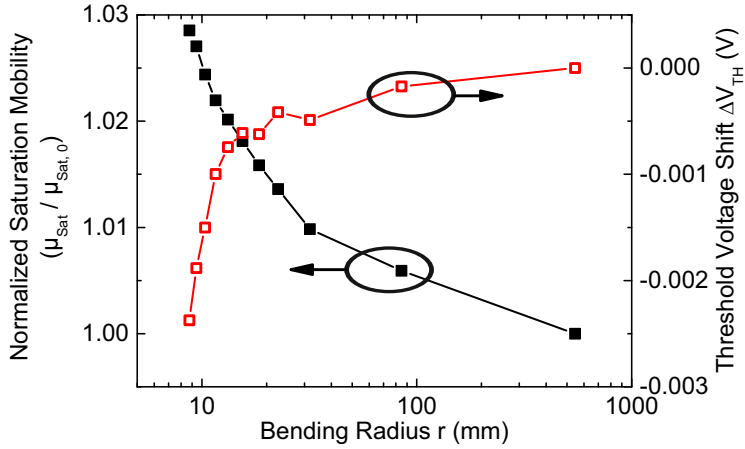

Figure 4.4: Experiment I: Influence of tensile bending on the saturation field effect mobility (μ_{sat}) and the threshold voltage (V_{th}) of our a-IGZO TFTs. Please note that a small bending radius corresponds to high strain.

are pretty stable [10]; μ_{sat} increases less than 3 %, while V_{th} is decreased by $\approx$ 0.0025 V. For experiment II the strain at the smallest measured radius was $\approx$ 0.273 % the differences compared to tensile comes from the build in strain of the deposited layers. The results are shown in Fig. 4.5, here the mobility is even more stable and is decreased by only 1.7 %, while V_{th} is increased by $\approx$0.019 V.

We think the reason for this behavior is that the conductivity inside the IGZO takes place mainly over large spherical s orbitals, with large overlaps, of the metal ions, mainly the indium [11], and therefore the electrical properties are pretty insensitive against mechanical deformation. At the same time the small observed changes can be explained by a change in the energy level splitting of the binding and antibinding orbitals between the atoms in the semiconducting layer and by an modification of the distance between the atoms induced by tensile/compressive strain [12]. This changes the carrier density and causes a shift in V_{th} in the directions we observed. The mobility changes can be explained by a change of the electron-lattice interaction due to variations in the inter atomic distance, which results in an change of the effective mass m^* (k·p method [13]) and affects the

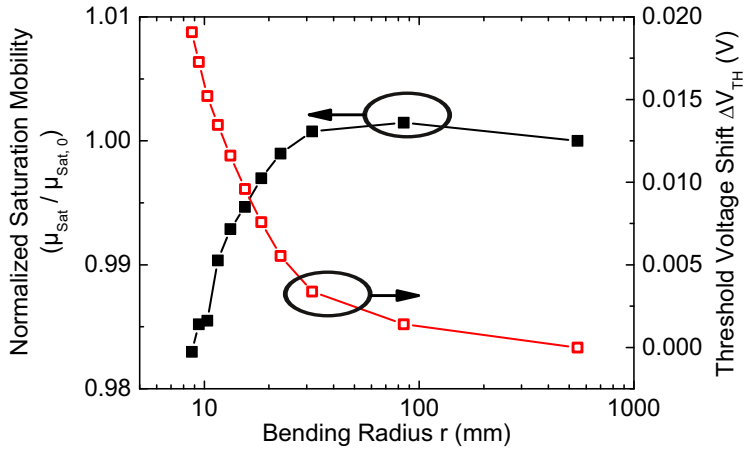

Figure 4.5: Experiment II: Influence of compressive bending on the saturation field effect mobility (μ_{sat}) and the threshold voltage (V_{th}) of our a-IGZO TFTs. Please note that a small bending radius corresponds to high strain.

mobility.

4.3.2 Experiment III: IGZO TFT cycling

We have cycled our a-IGZO TFTs from an infinite radius (flat substrate) down to a radius of ≈8 mm tensile 2500 times, the bending tester moved with 1 mm s^{-1}, and therefore the total experiment time was ≈70 h. To determine the TFT parameters we stopped the cycling for ≈10 s (at the moment when the TFT was flat) and measured the transfer characteristic. The evolution of the threshold voltage (V_{th}) and the saturation field effect mobility (μ_{sat}) can be seen in Fig. 4.6. Here μ_{sat} decreases by ≈4.5 % and V_{th} is increased by ≈ 0.11 V, both values show a saturation behavior if the number of cycles increased. We think the large number of bending cycles impacts the semiconductor, by the creation of additional scattering centers, maybe due to the formation of micro cracks, what reduces the conductivity.

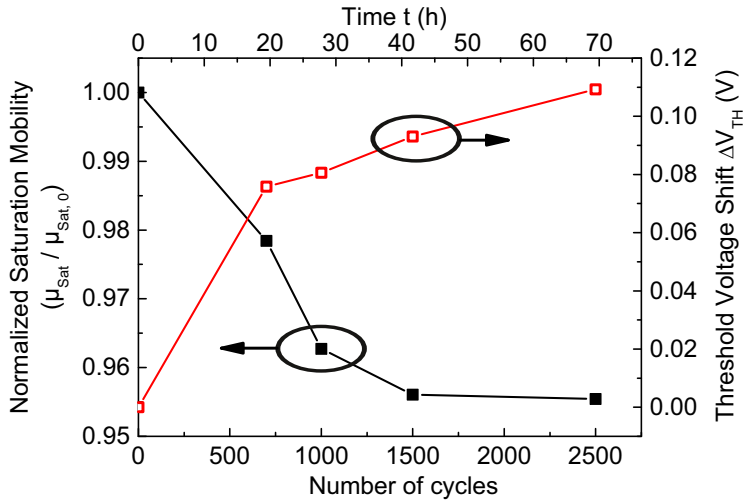

Figure 4.6: Experiment III: Influence of tensile cycling between a plate distance of 60 mm and 10 mm at a speed of 1 mm s^{-1} on the saturation field effect mobility (μ_{sat}) and the threshold voltage (V_{th}) of our a-IGZO TFTs.

4.4 Conclusion

The sensitivity of TFTs against applied mechanical stress induced by bending and the effect of long term cycling clearly shows the need to have the possibility to test these influences on transistors used in applications like future flexible and rollable displays. This possibility is given by the presented bending tester.

Bibliography

[1] K.H. Cherenack, A.Z. Kattamis, B. Hekmatshoar, J.C. Sturm, and S. Wagner. Amorphous-silicon thin-film transistors fabricated at 300 °C on a free-standing foil substrate of clear plastic. *Electron Device Letters, IEEE*, 28(11):1004–1006, 2007.

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, 432(7016):488–492, 2004.

[3] M. Ito, M. Kon, C. Miyazaki, N. Ikeda, M. Ishizaki, R. Matsubara, Y. Ugajin, and N. Sekine. Amorphous oxide TFT and their applications in electrophoretic displays. *Physica Status Solidi (A)*, 205(8):1885–1894, 2008.

[4] M.C. Wang, T.C. Chang, P.-T. Liu, S.W. Tsao, Y.P. Lin, and J.R. Chen. The instability of a-si: H tft under mechanical strain with high frequency ac bias stress. *Electrochemical and Solid-State Letters*, 10(10):J113–J116, 2007.

[5] H. Gleskova, S. Wagner, and Z. Suo. a-si: H thin film transistors after very high strain. *Journal of Non-Crystalline Solids*, 266:1320–1324, 2000.

[6] Kapton Polyimide Film. `http://www2.dupont.com/Kapton/en_US/`. [Online; accessed 20th of September 2010].

[7] J.B. Kim, C. Fuentes-Hernandez, W.J. Potscavage Jr, X.-H. Zhang, and B. Kippelen. Low-voltage ingazno thin-film transistors with alo gate insulator grown by atomic layer deposition. *Applied Physics Letters*, 94:142107, 2009.

[8] B. Zhou and W.F. Ramirez. Kinetics and modeling of wet etching of aluminum oxide by warm phosphoric acid. *Journal of The Electrochemical Society*, 143(2):619–623, 1996.

[9] D. Neamen. *Semiconductor Physics And Devices*. McGraw-Hill, Inc., New York, NY, USA, 3rd edition, 2003.

[10] K.H. Cherenack, N.S. Münzenrieder, and G. Tröster. Impact of mechanical bending on ZnO and IGZO thin-film transistors. *Electron Device Letters, IEEE*, 31(11):1254–1256, 2010.

[11] H. Hosono. Ionic amorphous oxide semiconductors: Material design, carrier transport, and device application. *Journal of Non-Crystalline Solids*, 352:851–858, 2006.

[12] I.L. Spain and J. Paauwe. *High Pressure Technology: Equipment design, materials, and properties*. M. Dekker, Inc., M. Dekker, NY, USA, 1st edition, 1977.

[13] L.C.L.Y. Voon and M. Willatzen. *The kp Method: Electronic Properties of Semiconductors*. Springer, 2009.

5

Influence of strain and light on IGZO TFTs

Niko Münzenrieder, Kunigunde H. Cherenack, Gerhard Tröster

The Effects of Mechanical Bending and Illumination on the Performance of Flexible IGZO TFTs

IEEE Transactions on Electron Devices, vol. 58, no. 7, pp. 2041–2048, 2011.
10.1109/TED.2011.2143416

Abstract

Amorphous indium–gallium–zinc–oxide (a-IGZO) is an interesting semiconducting material for use in flexible thin-film transistor (TFT) fabrication due to the high carrier mobility and low deposition temperatures. To use these TFTs in flexible applications, their behavior under applied mechanical strain and changing illumination, as well as the influence of bending on reflattened TFTs, needs to be understood. We have fabricated a-IGZO TFTs on flexible substrates and measured their behavior under tensile and compressive strains down to bending radii < 10 mm. Bending tests were applied in the dark, as well as under 90 lx illumination. Without illumination, the tensile and compressive strains caused a little change in the TFT performance, but the influence of the tensile strain combined with illumination causes changes in the TFT mobility of 15 % and changes in threshold voltage of -0.11 V. By comparison, the performance of illuminated TFTs under the applied compressive strain changes little compared with measurements in the dark. The impact of repeated tensile bending and reflattening shows a similar picture; bending tests carried out in the dark resulted in a nearly constant threshold voltage, but with illumination, we observed a shift of -0.1 V after 40 minutes of repeated bending.

5.1 Introduction

Electronic devices, including thin-film transistors (TFTs) fabricated on flexible plastic substrates, can be integrated into a large number of new applications such as flexible displays, smart textiles [1], and other large-area electronics. One key requirement for such applications is the ability to fabricate devices at low temperatures (<300 °C) [2] because of the limited temperature resistance of plastic substrates. At the same time, transistors need to be electrically stable under applied electrical and mechanical stresses. TFTs fabricated using oxide semiconductors such as amorphous indium–gallium–zinc–oxide (a-IGZO) are attractive for flexible electronics since they have good electrical properties even when a-IGZO is deposited at room temperature [3]. Much research has focused on studying the electrical instability induced by the gate bias stressing of a-IGZO TFTs [4]. Some groups also reported the impact of tensile [5] or compressive [6] bending over a limited range of radii and the impact of light on the electrical stability [7] of TFTs. However, to our knowledge, the influence of light combined with the mechanical stress has been not yet reported. Here, we show the results

of bending experiments to continuously monitor the electrical behavior of a-IGZO TFTs exposed to tensile and compressive strains (both in the dark and under illumination) down to the bending radii < 10 mm. We also compared the impact of the electrical and mechanical stresses for different illumination conditions over a longer time period and show that, under certain conditions, the influence of the mechanical stress can have the same order of magnitude effect on the TFT stability as the electrical stress.

5.2 Device fabrication and Evaluation

5.2.1 IGZO TFTs

We used a 50 μm thick Kapton E substrate from DuPont (surface area =7.6 cm × 7.6 cm), which was cleaned by sonication in acetone and isopropanol for 10 min and was then preshrunk in a vacuum oven at 200 °C for 24 h to remove trapped residual solvents [8]. We deposited 50 nm of SiN_x on each side of the substrate using plasma enhanced chemical vapor deposition (PECVD) in Oxford Instruments PECVD 80+. TFTs had a standard bottom gate back channel passivated geometry (see Fig. 5.1). Following the substrate preparation, we deposited 35 nm Cr using a Univex 500 e^--beam evaporator and patterned gates using standard photolithography (mask 1). We then deposited 25 nm Al_2O_3 using atomic layer deposition in Picosun Sunale R-150B at 150 °C. We used a PVD Products magnetron sputtering system to deposit 15 nm of IGZO at room temperature. This deposition was performed in a pure Ar atmosphere (pressure =2 mtorr) at a radiofrequency power of 75 W, using a ceramic $InGaZnO_4$ target. Next, TFT islands were patterned and etched using standard photolithography (mask 2) and HCl:DI water of 1:120 [9]. Then, gate vias were etched using standard photolithography (mask 3) and AL-11 etchant from Cyantek heated to 50 °C [10]. We spin coated and patterned MA-N1420 negative photoresist (mask 4) and structured the Ti /Au =10 nm /60 nm contacts with a liftoff process. Finally, we deposited and patterned an additional 25 nm passivation layer of Al_2O_3 [11] to improve the electrical stability, using again the semiconductor island mask. The TFTs discussed in this paper have a W/L ratio of 280 μm/115 μm or 280 μm/60 μm. TFT masks were designed so that the process substrate could be cut into stripes with one TFT per stripe (dimensions: 4.75 mm

× 34.5 mm). TFT electrodes were connected to interconnect lines leading to larger contact pads (3 mm × 3 mm) located on the same stripe.

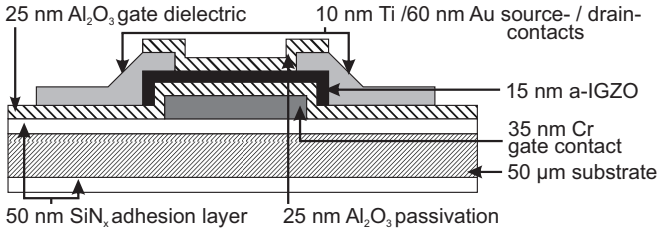

Figure 5.1: Schematic of the bottom gate back channel passivated a-IGZO TFT.

Fig. 5.2(a) shows a typical a-IGZO transfer characteristic measured with a HP4156A parameter analyzer. The performance parameters for the shown characteristic are linear field effect mobility μ_{lin} =9.5 $cm^2V^{-1}s^{-1}$, saturation field effect mobility μ_{sat} =8.4 $cm^2V^{-1}s^{-1}$, threshold voltage V_{th} =0.33 V, on/off ratio = 2.7×10^6, and subthreshold swing (inverse of the subthreshold slope)SS =0.18 V/decade, extrapolated using standard equations to model the TFT current [12]. The gate–source leakage current I_{GS} is always smaller than 10^{-7} mA. The family curve plot of the same a-IGZO TFT is shown in Fig. 5.2(b); for an applied gate–source voltage V_{GS} of 5 V, the drain–source current I_{DS} is saturated above a drain–source voltage V_{DS} of ≈4.5 V. The evolution of V_{th} with time, although without electrical or mechanical stress applied to the a-IGZO TFT, measured in the darkness and under illumination (90 lx), is shown in Fig. 5.3. The shift is increased by the light, although smaller than 5 mV, after 3000 s of illumination.

5.2.2 Bending measurements

TFTs were tested by attaching them to a reusable carrier substrate and loading them between two parallel plates in a custom built bending tester, as shown in Fig. 5.4(a). The plate can be adjusted from 14 mm (corresponding to a TFT bending radius of 8.7 mm) to a distance where the substrate is totally flat. The actual bending radius applied to TFTs was measured by fitting circles to images taken using a camera mounted to face the edge of the carrier substrate. TFTs are mounted as follows: 1) A flexible carrier substrate is coated with

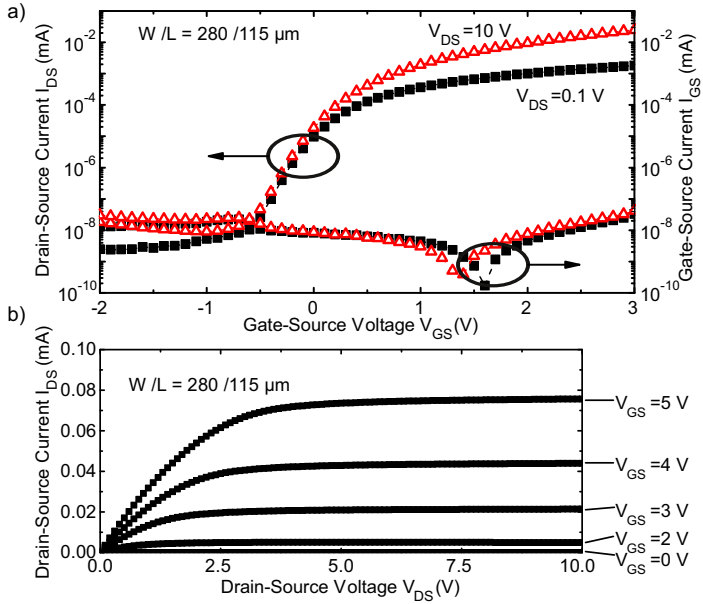

Figure 5.2: a) Typical a-IGZO TFT transfer characteristic measured at source–drain voltages of 0.1 V (linear regime) and 10 V (saturation regime). b) Typical a-IGZO TFT output characteristic with a maximum saturation current of about 72 µA.

600 nm of Cu. The copper layer is patterned to form three large contact pads connected to interconnect lines leading to the center of the substrate. 2) A TFT stripe is cut from the process substrate and is attached to the carrier substrate with double sided tape. 3) Electrical contact between pads on the TFT stripe and the interconnect lines on the carrier substrate is made using pieces of Cu wire (diameter of 0.09 mm) glued with conductive epoxy EE129-4 from Epoxy Technology. Fig. 5.4(b) shows a close up of a mounted TFT. 4) Three Cu cables are soldered to the large contact pads on the carrier substrate, and the free ends of these wires are attached the parameter analyzer to constantly monitor the electrical performance of the TFT. Afterward, the carrier substrate, with the attached TFT, is loaded into our bending tester (facing upward to apply tensile strain and downward for the compressive strain), and the bending radius was varied from infinity

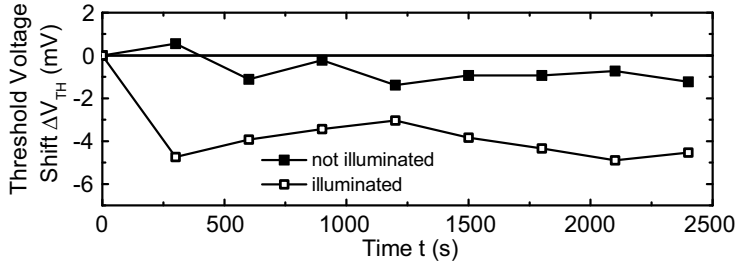

Figure 5.3: Impact of illumination without electrical or mechanical stress on the a-IGZO TFT threshold voltage.

(flat substrate) to ≈9 mm. TFTs are loaded to apply strain parallel to the channel length. The range of strains ϵ (where $\epsilon = \Delta L/L_0$, with initial channel length L_0) applied to the TFT channel region corresponds to 0 % - 0.3 % tensile and 0 % - 0.27 % compressive strains. This was calculated using the strain theory developed in [13] and taking into account the built in strain in the substrate following the fabrication. During the bending experiments, we measured the transfer characteristics of the TFTs by sweeping the gate–source voltage from 1.5 V to -1 V V, while setting the drain–source voltage at 0.1 V and 5 V; these two values are corresponding to the linear and saturation regimes of the a-IGZO TFTs (compare with Fig. 5.2).We choose this small V_{GS} range to ensure that the measurements obtained while applying the bending stress are not significantly influenced by the applied electrical stress field during measurement. To be sure that the applied electrical stress during measurement does not impact the mechanical strain measurement, we also waited for additional 5 min after measuring the characteristic before changing the radius to a new value and remeasuring the TFT characteristic. The initial bending radius was infinite (flat substrate) and was then stepwise decreased until the maximum strain value was reached. Then, the TFT was flattened again to monitor the TFT relaxation behavior. For compressive measurements under illumination, the complete bending setup was rotated so that the TFT faced the light source. This was to ensure that the TFT active region is exposed to the light. For the illumination itself, a conventional light bulb emitting a black body spectrum (color temperature of ≈2700 K) was used. This light source was chosen to simulate the use of our

TFTs under everyday illumination conditions. The illuminance was measured with a Gossen Mavolux lux meter.

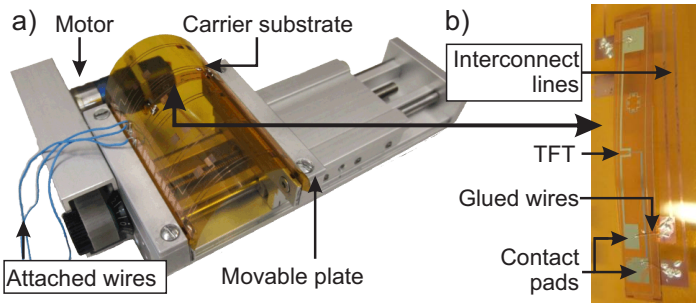

Figure 5.4: a) Photo of our custom built bending tester with a loaded carrier substrate and an attached flexible TFT bent to a radius of ≈19 mm. The TFT is loaded to apply the tensile strain. b) Close up of one TFT with attached contact wires.

5.3 Results and discussion

5.3.1 TFT bending

All TFTs were characterized at a specific bending radius by measuring the TFT transfer characteristics and extracting the linear mobility, the saturation mobility, the threshold voltage, and the subthreshold swing.

Fig. 5.5(a) shows the measured a-IGZO TFT saturation performance characteristic for a TFT that is initially flat and is then bent to a tensile bending radius of 9 mm and then to a compressive radius of 9 mm. All measurements were taken in the darkness. It is obvious that the transfer characteristic shifts in opposite directions for the tensile or compressive strain. It should be emphasized that, since the measurement of the characteristic under the compressive strain follows a tensile bending step, the observed shift caused by compressive bending is smaller than the shift that would be observed if we had omitted tensile bending. Fig. 5.5(b) shows the a-IGZO TFT saturation performance characteristic measured for a flat TFT and the same TFT bent to a 9 mm tensile radius (illuminated with 90 lx and also without illumination). This shows the strong impact that light has on the electrical properties of a-

IGZO TFTs under bending. Compared with the measurement without illumination, the influence of tensile bending is increased by a factor of ≈5 due to the illumination. The different shapes of the a-IGZO TFT characteristics shown in Fig. 5.5, as compared with Fig. 5.5, result from a different measuring range and particularly form a worse electrical connection of the device with the parameter analyzer caused by contacting the TFT via the carrier substrate for bending measurements. This modification of the absolute values is not critical because we only consider relative values in the next sections.

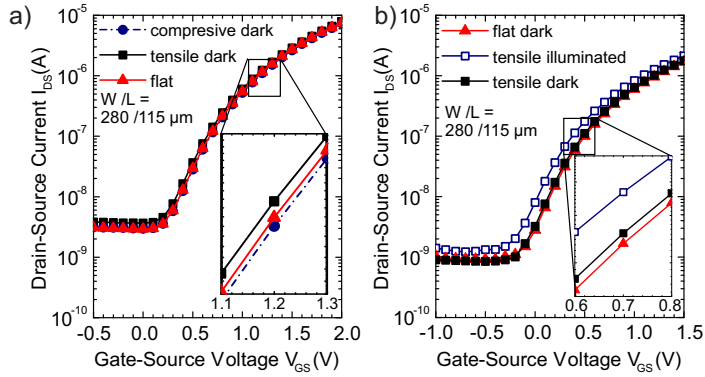

Figure 5.5: TFT transfer characteristics for (a) a TFT measured without illumination while it is flat and then while bent to ≈9 mm compressive and tensile radii and (b) a TFT that is initially flat (without illumination) and then bent to ≈9 mm tensile radius (in the darkness and while under illumination). All transfer characteristics are measured in the saturation regime (V_{DS} =5 V). (Insets) Enlarged section of the transfer characteristic (also using a logarithmic scale).

Typical measurement of normalized a-IGZO TFT linear and saturation mobilities versus applied strain (tensile and compressive) are plotted in Fig. 5.6(a) and (b), respectively. Fig. 5.6(c) shows the threshold voltage shift, and Fig. 5.6(d) shows the normalized subthreshold swing extracted from measurements obtained during the same experiment. We use the definition where the tensile strain corresponds to positive strain values and the compressive strain to negative strain values. The mobility and subthreshold swing values are normalized by their measurements at zero strain; the change in the threshold volt-

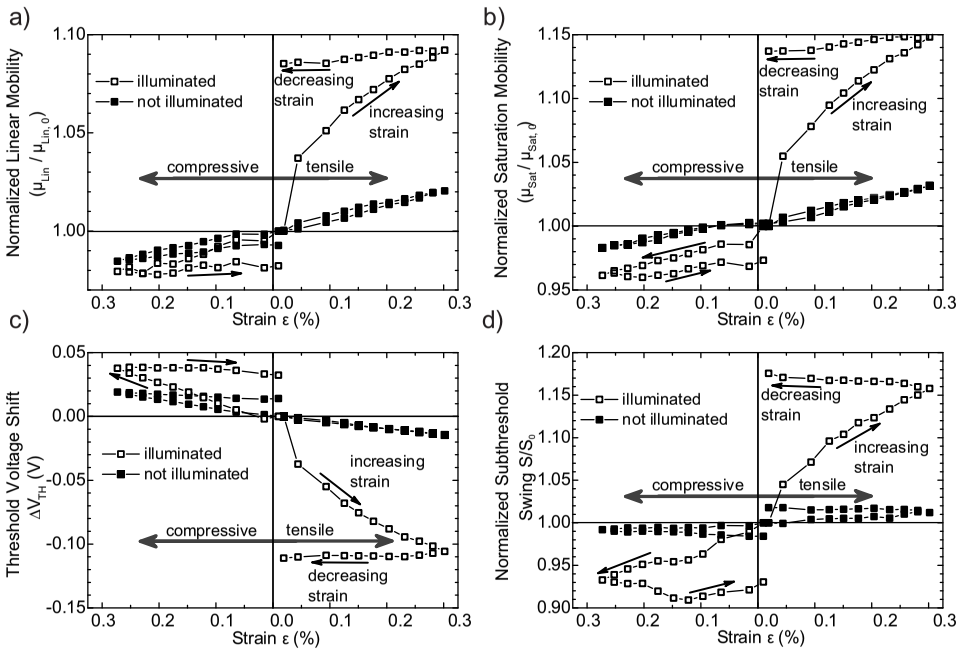

Figure 5.6: a) Normalized linear mobility, b) normalized saturation mobility, c) threshold voltage shift, and d) normalized subthreshold swing for increasing and subsequently decreasing strain in the darkness and illuminated with 90 lx. All values are extracted from the same experiment. The time interval between two consecutive measurement points is always 5 min.

age is shown as the difference to the value measured at zero strain. The measured threshold voltage shift is much larger than the shifts obtained without the mechanical stress (see Fig. 5.3). The increase or the decrease in the channel length L during bending is small (maximum of 0.3 %). It should be noted that the channel width W is constant during bending because the strain is applied parallel to the channel. Therefore, the influence of the W/L ratio change on the mobility/threshold voltage calculation is also small compared with the observed parameter variations, and we mainly observe a change in the semiconductor material properties.

a) Parameter shift induced by bending in the darkness

For bending strains up to the maximum applied value of ≈0.3 % (≈9 mm bending radius) in the absence of illumination, V_{th} shifts by up to -15 mV (tensile) and 19 mV (compressive). The linear and saturation field effect mobilities change by 1.5 % - 3 % with the applied strain. The mobility increases for the applied tensile strain and decreases for the compressive strain. The subthreshold swing increases for the tensile and decreases for the compressive bending by ≈1 % (transistor performance is worsened by a higher subthreshold swing). All observed parameters linearly change with the applied strain (therefore inversely proportional to the bending radius).We can extract the linear mobility, the saturation mobility, the threshold voltage, and the subthreshold swing to describe the response of the a-IGZO TFT performance parameters to the applied stain simply by fitting the parameter shift linearly against the applied strain. As an example, the result for the linear mobility is shown in Fig. 5.7. The slope of the four linear fits and, therefore, the response values of the four measured TFT parameters against the applied mechanical strain ϵ(%) are $(\mu_{lin}/\mu_{lin,0})/\epsilon$ =0.062 (see Fig. 5.7), $(\mu_{sat}/\mu_{sat,0})/\epsilon$ =0.081, $SS/S_0/\epsilon$ =0.035, and $\Delta V_{th}/\epsilon$ =-0.057 V.

All measured TFT parameters (see Fig. 5.6), except for the threshold voltage under the compressive strain and for the subthreshold swing, return to their initial values if the strain is decreased to zero (after reaching its maximum).

The observed behavior can be explained as follows:

Mechanical strain causes either an increase (in the case of the tensile strain) or a decrease (in the case of the compressive strain) of the distance between the atoms in the semiconductor layer and, of course, also in all other layers of the transistor. The direction of this change

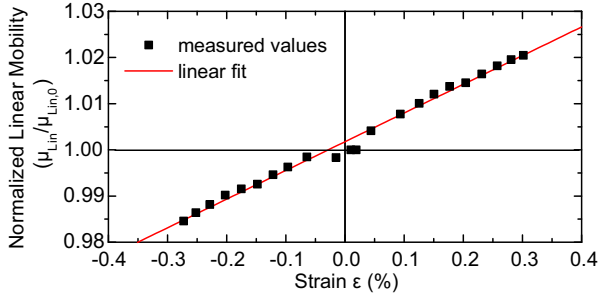

Figure 5.7: Normalized a-IGZO TFT linear mobility for different tensile and compressive strains. The measured values show a linear behavior. The linear fit gives the following relation between the linear mobility and the applied strain: $\mu_{lin} = (0.062\epsilon + 1.005)\mu_{lin,0}$.

of the interatomic distance is parallel to the applied strain. As we applied the strain parallel to the channel length ($\Delta L_{\parallel}$, corresponding to the length variation of the a-IGZO channel) of our a-IGZO TFTs, the change is also parallel to the current flow. The length variation perpendicular to the applied strain ($\Delta L_{\perp}$, corresponding to the width and thickness variations of the a-IGZO channel) induced by the Poisson effect is quantified by the Poisson ratio ν, where ν (of a cube with $L_{\perp} = L_{\parallel}$) $\approx -\Delta L_{\perp}/\Delta L_{\parallel}$. The Poisson ratio of IGZO is not known, but the theoretical value of the Poisson ratio has to be $-1 < \nu < 0.5$ in an isotropic material [14]. This means that, for example, an increase in the distances in parallel direction of 1 % leads to a maximum decrease of 0.5 % in the perpendicular directions or also to a maximum increase of 1 %. Therefore, the direction of the originally applied strain remains the dominant direction influencing interatomic spacing and, therefore, the TFT current. The most similar material to IGZO with a known Poisson ratio is ZnO, where $\nu_{ZnO} \approx 0.35$ [15].

The decrease in the threshold voltage for tensile bending can be now explained by an increase in the distance between the atoms that cause an effective decrease in the energy level splitting (ΔE) of the bonding and antibonding orbitals between the atoms in the semiconducting layer [16]. This changes the value of the Fermi function (more electrons are excited to the antibonding state for the material under tensile bending strain, as compared with the relaxed material, at the

same temperature). The additional electrons cause an increase in the channel conductivity and, therefore, a negative shift of V_{th}. For compressive bending, the same argument is valid, but here, the decrease in the interatomic distance leads to an increase in the energy spacing. Therefore, this results in a decrease in the channel conductivity and a positive shift of the threshold voltage.

The mobility increase for tensile bending can be correlated with a decrease in the electron–lattice interaction due to the decreased energy spacing in the direction parallel to the current flow. The k·p method tells us that this decreases the effective mass m^* of the charge carriers ($m^* \propto \Delta E$) [17] and affects their mobility ($\mu \propto m^{*-1}$). The mobility decrease for compressive bending is then caused by the increase in the energy spacing. Finally, the increase/decrease in the free carrier concentration under tensile/compressive bending increases/ decreases the capacitance of the semiconductor, resulting in an increase/decrease in the subthreshold swing [18].

This observed behavior indicates that a-IGZO has a positive pressure coefficient dE_G/dp, where E_G is the energy spacing and p is the pressure. Here, the pressure is proportional to strain ϵ expressed by $E_G = Y \times \epsilon$. Y is the Young modulus of the material.

b) Parameter shift induced by bending under illumination

Under illumination, the TFT behavior significantly changes; the influence of the tensile strain is increased by a factor > 5, as compared with the measurement without illumination, where V_{th} shifts by -110 mV, μ_{lin} and μ_{sat} are increased by 9.2 % and 14.8 %, respectively, andSS rises by 15.7 %. The relaxation behavior is modified as well. Even when the strain is reduced again to 0 % after bending, the TFT parameters remain nearly constant at the values they reached at the maximum strain. These values only gradually return to their original values over 5 h - 10 h in the darkness.

The fact that the values only change when the strain is increased shows that the observed parameter shift is not an effect of illumination or additional electrical stress (induced by the measurement itself) but is caused by a combination of mechanical stress and illumination. Therefore, this change in the TFT performance is a new instability mechanism induced by a combination of the mechanical stress and the illumination. For the compressive strain, the influence on the parameter shift is smaller but is still visible in the graphs (see Fig. 5.6). At

the minimal applied compressive bending radius, V_{th} shifts by 37 mV, μ_{lin} and μ_{sat} are decreased by 2.1 % and 3.8 %, respectively, andSS is reduced by 6.7 %, as compared with the values measured at the flat device. Therefore, the illumination increases the impact of compressive bending on the mobilities and the threshold voltage only by a factor of ≈2 and the impact on the subthreshold swing by a factor of ≈5. The relaxation behavior is also modified; all four performance parameters show the slow relaxation behavior already observed for tensile bending.

These measurements again confirm the combined light/ bending influence. The direction of the parameter shift is identical to the measurement without illumination and defined by the type of the applied mechanical strain. Illumination only modifies the strength of the effect; therefore, we do not measure only a superposition of two independent effects.

Our explanation for the influence of light on the TFT performance under bending is the following:

In the case of tensile bending, the smaller energy spacing between the bonding and antibonding orbitals of the semiconductor enables a-IGZO to absorb light with shorter wavelengths compared with the relaxed material. The band gap of IGZO has a size of ≈3 eV - 3.4 eV [3]; therefore, the minimum absorbable wavelength is ≈400 nm - 360 nm. This corresponds to the visible violet or ultraviolet light; the light in this spectral range is present in the natural sunlight or the black body radiation of the lamp used for these experiments. The higher absorption of the a-IGZO under tensile bending results in a higher electron/hole pair generation inside the active channel of the TFT; this can have two effects. The generated holes h^+ inside the n-type semiconductor [18] can neutralize negatively charged oxygen inside a-IGZO [19], [20] and/or negatively charged trapped electrons near the Al_2O_3/a-IGZO interface [21], [22]. The resulting smaller scattering center density, particularly at the interface, reduces electron scattering and increases the mean free path, resulting in higher mobilities. Under compressive bending, the absorption is weaker due to the increased energy spacing and fewer holes, as compared with the flat substrate that are generated. Therefore, the number of scattering centers increases with increasing strain, and the mobility drops. At the same time, the increasing (in the case of the tensile strain) or decreasing (in the case of the compressive strain) number of photogenerated electrons changes the conductivity and the capacitances and also affects the TFT performance parameters.

The increased conductivity under tensile bending and illumination reduces the threshold voltage and contributes to the mobility increase, whereas the increase in the subthreshold swing can be explained by the increased capacitance. Under illuminated compressive bending, the reduction of the conductivity and the capacitance with increasing strain, as compared with the relaxed layers, causes the observed opposite effect. The threshold voltage is maybe also modified by photogenerated holes near the dielectric–semiconductor interface or inside the gate insulator causing an increase (tensile strain) or decrease (compressive strain) in the effective electrical field in this region.

The observed effect is probably larger for tensile bending because the intensity of the black body radiation increases with increasing wavelength (the maximum of the radiation emission curve λ_{Max} is located at larger wavelengths in this case, i.e., $\lambda_{Max} \approx 1070\,\text{nm}$), and therefore, the absorption gain for a decreased energy spacing is larger than the decrease during the compressive phase where the absorption is reduced due to the increased energy spacing.

5.3.2 TFT cycling

The bending tests showed that bending can influence the a- IGZO TFT performance even after the device is reflattened. Therefore, we performed TFT cycling experiments using our bending machine to induce the mechanical stress by cycling the TFT bending radius between infinity and ≈9 mm. The time needed to reach the minimum bending radius starting from a flat substrate is 50 s; therefore, one complete cycle needs 100 s. To measure the TFT performance after a specific number of cycles, we stopped the cycling at a point when the device was totally flat, measured the transfer characteristic, and continued the cycling. We have measured the characteristic after every six bending cycles (corresponding to 10 min continuous mechanical stress in between) and extracted the common TFT performance parameters. Fig. 5.8 shows the behavior of the linear and saturation field effect mobilities and the subthreshold swing versus the duration of the mechanical stress induced by tensile cycling, with and without illumination. The observed parameter shifts are in the same order of magnitude as the values measured for the single bending cycle discussed in the previous section (see Fig. 5.6).

However, an increasing number of bending cycles also causes an increase in the parameter shift measured on the flat device. The behavior

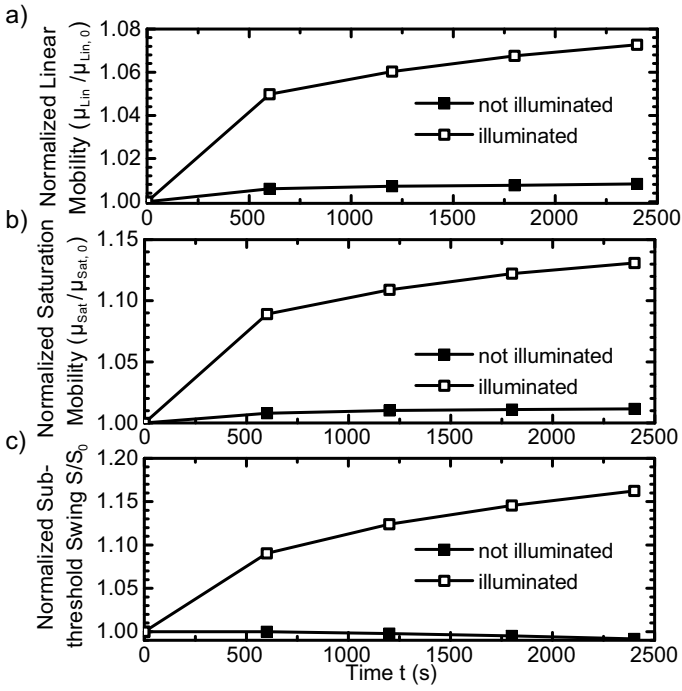

Figure 5.8: a) Linear field effect mobility μ_{lin}, b) saturation field effect mobility μ_{sat}, and c) subthreshold swingSS of the a-IGZO TFT for different tensile cycling times with and without illumination, where one bending cycle corresponds to 100 s.

of the performance parameters under compressive cycling is different. For the same number of bending cycles, the linear and saturation field effect mobilities are nearly constant. The change of μ_{lin} (with and without illumination) and μ_{sat} (not illuminated) is ≈0.2 %, whereas μ_{sat} (illuminated) is varied by ≈0.35 %. The shift of the subthreshold swing is shown in Fig. 5.9. For cycling under illumination, the increase in the free carrier concentration due to photogeneration, resulting in an increase in the subthreshold swing, seems to be the dominant factor. We see a decrease in the values for cycling without illumination, indicating a decrease in the free carrier concentration (comparable with the results shown in Fig. 5.6). The thresholdvoltage shift caused by repeated

bending is shown in Fig. 5.10. In the tensile case, the threshold voltage shifts by ≈ - 5 mV (no illumination) and≈ -100 mV (illuminated) after 2400 s of cycling; for compressive cycling, the maximum shift is ≈6 mV (no illumination) and ≈33 mV (illuminated). These values are comparable with the values measured at the reflattened TFT.

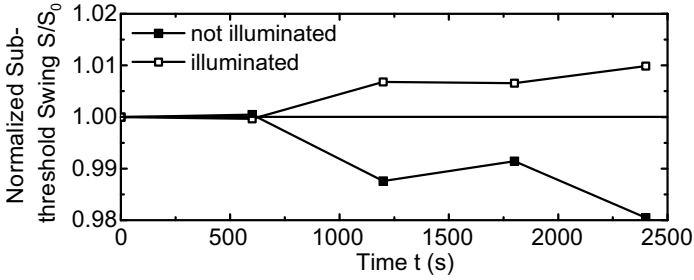

Figure 5.9: Normalized a-IGZO TFT subthreshold swingSS for different compressive cycling times with and without illumination, where one bending cycle corresponds to 100 s.

The evolution of the threshold voltage shift dependent on the time of the cycling can be described by an exponential function. Fig. 5.11 shows ΔV_{th} induced by tensile cycling and an exponential fit of the measured data. An exponential fit with the following equation is used to model the behavior:

$$\Delta V_{th} = A \times \exp(-\sigma_{TH} \times t_{Str}) + \Delta V_{th,\infty},$$

where $\Delta V_{th,\infty}$ is the maximum threshold voltage shift, σ_{TH} is a shift constant that determines the strength of the increase in the threshold voltage shift, and t_{Str} is the stress time (duration of the cycling). For $t_{Str} = 0$ s, the shift should be zero; therefore, the amplitude should be equal to $-\Delta V_{th,\infty}$. The maximum threshold voltage shift and the shift constant for the mechanical stress experiments are as follows:

1. Tensile, illuminated: $\Delta V_{th,\infty}$ =-98.6 mV and $\sigma_{TH} = 1.57 \times 10^{-3} s^{-1}$;
2. Tensile, darkness: $\Delta V_{th,\infty}$ =-4.8 mV and $\sigma_{TH} = 1.54 \times 10^{-3} s^{-1}$;
3. Compressive, illuminated: $\Delta V_{th,\infty}$ =58.3 mV and $\sigma_{TH} = 1.33 \times 10^{-3} s^{-1}$; and
4. Compressive, darkness: $\Delta V_{th,\infty}$ =13.4 mV and $\sigma_{TH} = 0.25 \times 10^{-3} s^{-1}$;

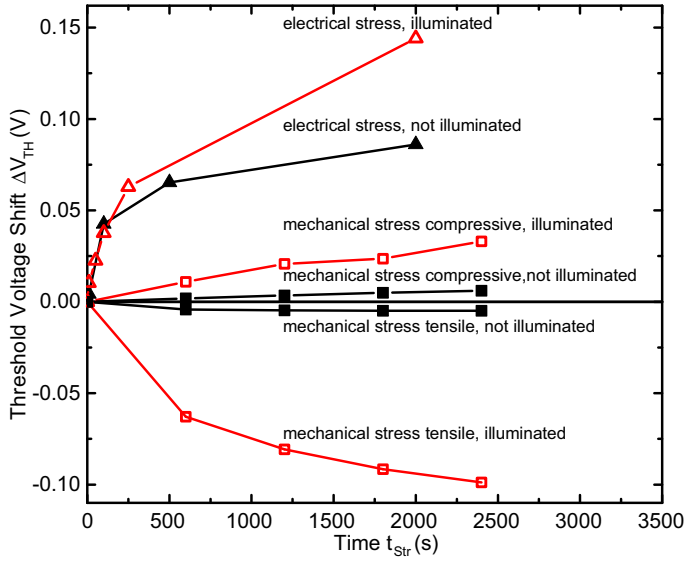

Figure 5.10: Threshold voltage shift of the a-IGZO TFT, which is induced by electrical (at a stress field of 1×10^8 V/m) and mechanical stresses induced by cycling (compressive and tensile). The data were measured with and without illumination.

To compare the influence of the mechanical stress with the electrical one, we also performed an electrical stress test with our TFTs, where we applied a gate bias stress field E_{Str} of 1×10^8 V/m and a voltage of 0 V at the source–drain contacts for different times and illumination conditions and monitored the resulting threshold voltage shift. The results of these experiments are also plotted in Fig. 5.10. The shift parameters are as follows:

5. Electrical stress, illuminated: $\Delta V_{th,\infty}$ =145 mV and σ_{TH} =$2.27 \times 10^{-3} s^{-1}$; and

6. Electrical stress, darkness: $\Delta V_{th,\infty}$ =86.4 mV and σ_{TH} =$2.87 \times 10^{-3} s^{-1}$.

In general, the influence of tensile cycling is larger than the influence of compressive cycling. This is consistent with the results measured for a single TFT bending cycle. This suggests that the TFT nearly

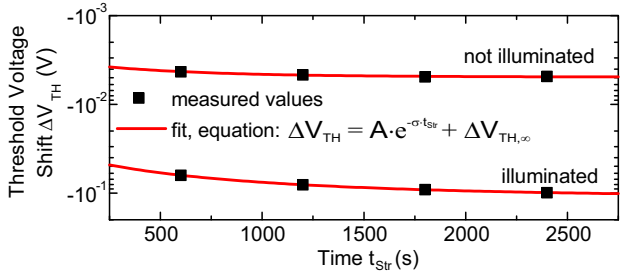

Figure 5.11: Threshold voltage shift of the a-IGZO TFT, which is induced by tensile cycling, with and without illumination. The equations of the fitting curves are the following: not illuminated, ΔV_{th} =4.83 mV exp(-0.003 54 $s^{-1} \times t_{Str}$) -4.83 mV; and illuminated, ΔV_{th} =98.2 mV exp(-0.001 58 $s^{-1} \times t_{Str}$) -98.6 mV.

completely relaxes in the 50 s time needed to reflatten the TFT following the compressive strain. In comparison, the tensile strain also has a strong effect on the TFT performance even after the TFT has been flattened again. It is also striking that, for compressive cycling, the parameters directly related to the carrier concentration (V_{th} andSS) are more strongly affected than the mobilities (influenced by the interaction of the electrons with the lattice). This indicates that some time is needed to restore the former carrier concentrations after the strain has been released (and the initial lattice configuration has been recovered).

5.4 Conclusion

The major results of this paper have been summarized in Fig. 5.12, where the influence of the mechanical strain on the saturation field effect mobility of a-IGZO TFTs is plotted. It has been shown that the applied mechanical strain induced by bending (tensile and compressive) has a considerable influence on the saturation mobility and all other performance parameters (μ_{lin}, V_{th}, and SS) of a-IGZO TFTs and that the strength and the relaxation behavior of this parameter shift are strongly affected by the illumination of the device. At the same time, the mechanical stress induced by cycling a-IGZO TFTs between two different bending radii also has a significant impact on the performance of reflattened TFTs. Flexible a-IGZO TFTs are nearly equally sensitive

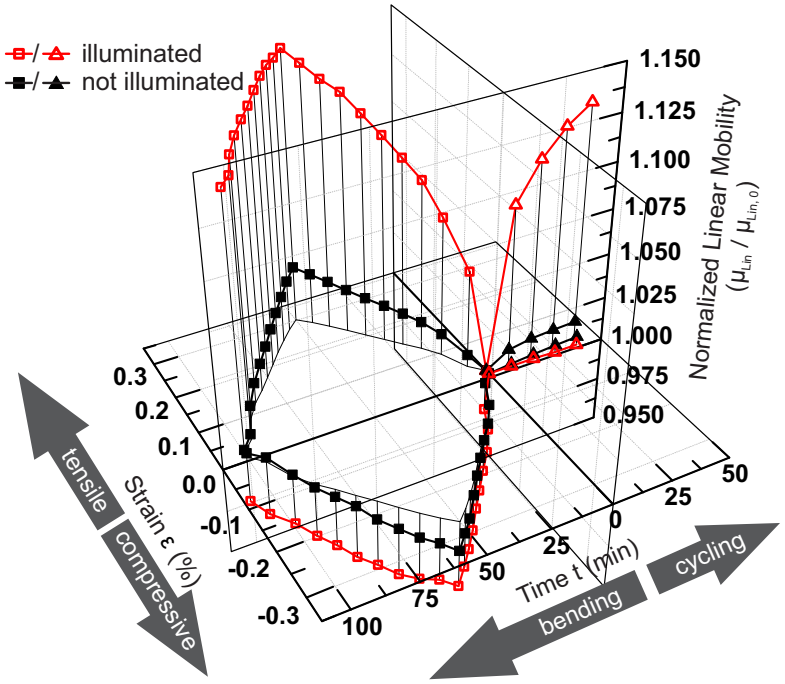

Figure 5.12: Shift of the normalized saturation mobility of a-IGZO TFTs induced by bending to specific radii and cycling between different radii for tensile and compressive strains measured with and without illumination.

to electrical and mechanical stresses induced by cycling, particularly under illumination. These facts need to be considered when designing future flexible display applications.

Acknowledgment

The authors would like to thank F. Mettler and Dr. Simone from DuPont for their support for this paper. This paper has been scientifically evaluated by the Swiss National Scientific Foundation.

Bibliography

[1] K. Cherenack, C. Zysset, T. Kinkeldei, N. Münzenrieder, and G. Tröster. Woven electronic fibers with sensing and display functions for smart textiles. *Advanced Materials*, 22(45):5178–5182, 2010.

[2] K.H. Cherenack, A.Z. Kattamis, B. Hekmatshoar, J.C. Sturm, and S. Wagner. Amorphous-silicon thin-film transistors fabricated at 300 °C on a free-standing foil substrate of clear plastic. *Electron Device Letters, IEEE*, 28(11):1004–1006, 2007.

[3] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, 432(7016):488–492, 2004.

[4] J.K. Jeong, H. Won Yang, J.H. Jeong, Y.-G. Mo, and H.D. Kim. Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors. *Applied Physics Letters*, 93(12):123508–123508, 2008.

[5] M. Ito, M. Kon, C. Miyazaki, N. Ikeda, M. Ishizaki, R. Matsubara, Y. Ugajin, and N. Sekine. Amorphous oxide TFT and their applications in electrophoretic displays. *Physica Status Solidi (A)*, 205(8):1885–1894, 2008.

[6] M.C. Wang, T.C. Chang, P.-T. Liu, S.W. Tsao, Y.P. Lin, and J.R. Chen. The instability of a-si: H tft under mechanical strain with high frequency ac bias stress. *Electrochemical and Solid-State Letters*, 10(10):J113–J116, 2007.

[7] J.-H. Shin, J.-S. Lee, C.-S. Hwang, S.-H.K. Park, W.-S. Cheong, M. Ryu, C.-W. Byun, J.-I. Lee, and H.Y. Chu. Light effects on the bias stability of transparent zno thin film transistors. *Etri Journal*, 31(1):62–64, 2009.

[8] Kapton Polyimide Film. `http://www2.dupont.com/Kapton/en_US/`. [Online; accessed 20th of September 2010].

[9] J.B. Kim, C. Fuentes-Hernandez, W.J. Potscavage Jr, X.-H. Zhang, and B. Kippelen. Low-voltage ingazno thin-film transistors with

alo gate insulator grown by atomic layer deposition. *Applied Physics Letters*, 94:142107, 2009.

[10] B. Zhou and W.F. Ramirez. Kinetics and modeling of wet etching of aluminum oxide by warm phosphoric acid. *Journal of The Electrochemical Society*, 143(2):619–623, 1996.

[11] I.-T. Cho, J.-M. Lee, J.-H. Lee, and H.-I. Kwon. Charge trapping and detrapping characteristics in amorphous ingazno tfts under static and dynamic stresses. *Semiconductor Science and Technology*, 24(1):015013, 2009.

[12] D. Neamen. *Semiconductor Physics And Devices*. McGraw-Hill, Inc., New York, NY, USA, 3rd edition, 2003.

[13] H. Gleskova, S. Wagner, and Z. Suo. a-si: H thin film transistors after very high strain. *Journal of Non-Crystalline Solids*, 266:1320–1324, 2000.

[14] Y.C. Fung. Foundations of solid mechanics. 1965. *Englewood Cliffs, NJ*, 436.

[15] H. Gercek. Poisson's ratio values for rocks. *International Journal of Rock Mechanics and Mining Sciences*, 44(1):1–13, 2007.

[16] A. Rockett. *The materials science of semiconductors*. Springer Publishing Company, Incorporated, 2007.

[17] L.C.L.Y. Voon and M. Willatzen. *The kp Method: Electronic Properties of Semiconductors*. Springer, 2009.

[18] S.M. Sze and K.K. Ng. *Physics of Semiconductor Devices*. John Wiley and Sons, 2007.

[19] P.-T. Liu, Y.-T. Chou, and L.-F. Teng. Environment-dependent metastability of passivation-free indium zinc oxide thin film transistor after gate bias stress. *Applied Physics Letters*, 95(23):233504–233504, 2009.

[20] J.-H. Lee, H.-I. Kwon, H. Shin, B.-G. Park, and Y.J. Park. Electrical instabilities and low-frequency noise in ingazno thin film transistors. In *Physical and Failure Analysis of Integrated Circuits (IPFA), 2010 17th IEEE International Symposium on the*, pages 1–7. IEEE, 2010.

[21] H. Seo, Y.-J. Cho, J. Kim, K.-Y. Park, J. Lee, and D.-K. Choi. Permanent optical doping of amorphous metal oxide semiconductors by deep ultraviolet irradiation at room temperature. *Applied Physics Letters*, 96(22):222101–222101–3, 2010.

[22] A. Suresh, P. Wellenius, and J.F. Muth. High performance transparent thin film transistors based on indium gallium zinc oxide as the channel material. In *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pages 587–590. IEEE, 2007.

6

Transferable TFTs on a Flexible Membrane

Niko Münzenrieder, Giovanni A. Salvatore, Thomas Kinkeldei, Luisa Petti, Christoph Zysset, Lars Büthe, Gerhard Tröster

InGaZnO TFTs on a Flexible Membrane Transferred to a Curved Surface with a Radius of 2 mm

71st Device Research Conference, pp. 165–166, 2013.
10.1109/DRC.2013.6633845

Abstract

Thin-film transistors have attracted a considerable amount of attention since they enable cost effective and large scale device fabrication. Fabricating TFTs directly on flexible plastic foils enables mechanically flexible transistors [1, 2, 3]. However, the mechanical instability of plastic substrates limits the accuracy of the photo mask alignment during the fabrication, and therefore the minimal feature size of the structures and their performance. An alternative way to produce flexible electronic devices is to peal-off a spin-coated polymer layer from a rigid substrate [4], or to spall the thin top layer from a crystalline silicon wafer after device fabrication [5]. These methods in general suffer from high strain applied during the separation process, or a limited flexibility of the final devices. Here, we propose a new approach based on the fabrication of transistors on top of a flexible 1 µm thin parylene membrane deposited on a Si carrier wafer, which can be transferred to nearly any kind of flexible or shaped surfaces. TFTs fabricated on Si and afterwards transferred to a flexible polyimide foil, exhibit transistor functionality even when the polyimide substrate is bent to a tensile radius of 5 mm. Additionally, TFTs are also transferred to a plastic rod with a radius of 2 mm.

6.1 Fabrication

The fabrication process starts with spin coating a 400 nm thick water soluble polyvinyl alcohol (PVA) layer, and the evaporation of a 1 µm thick parylene layer on a $2 \times 2\,cm^2$ silicon chip. Following the substrate preparation, bottom gate thin-film transistors consisting of a 15 nm thin sputtered amorphous Indium-Gallium-Zinc-Oxide (IGZO) semiconductor, and a 25 nm thick ALD deposited Al_2O_3 gate insulator are fabricated at a maximum process temperature of 150 °C, as described in [3]. The device structure and the fabrication process flow are illustrated in Fig. 6.1. Here, the fabrication on rigid Si, and chemically stable parylene make this technology compatible with standard semiconductor manufacturing techniques.

6.2 Results

The characterization of a typical device measured on the Si chip (black curve in Fig. 6.4) exhibits an I_{off} as low as $50\,fA\,\mu m^{-1}$ with an I_{on}/I_{off}

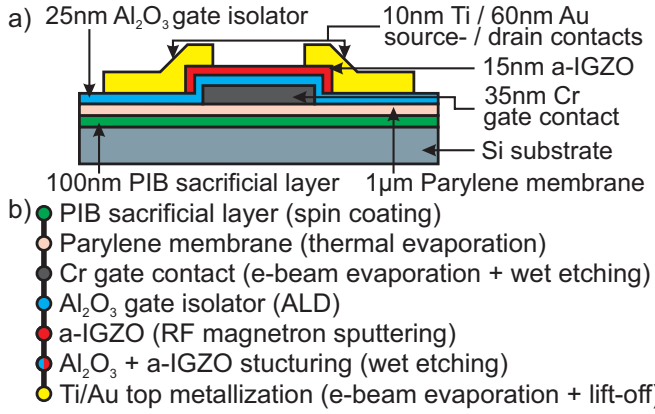

Figure 6.1: a) Cross section (a) and fabrication process flow (b) of bottom-gate, inverted staggered a-IGZO TFTs on a Si /polyvinyl alcohol (PVA) /parylene stack. Maximum process temperature is 150 °C.

$>10^7$ (V_{DS} = V_{GS} =5 V), a threshold voltage of ≈2.7 V, a subthreshold swing of 245 mV/decade, a transconductance of ≈0.735 mS µm^{-1}, a field effect mobility of ≈21 cm^{2}V^{-1}s^{-1}, and an output resistance of ≈625 kΩ (V_{DS} = V_{GS} =5 V). To releases and transfer the parylene membrane, the chip is floated in water, which dissolves the PVA (Fig. 6.2). For a 2×2 cm^2 chip the release takes ≈10 minutes after which the parylene membrane incorporating the devices is floating on the water. The floating membrane can then be transferred to the final substrate by dipping the desired substrate into the water, moving it towards the membrane, and lifting it.

The membrane then sticks on the final substrate due to adhesion forces. Subsequent heating to 60 °C for 10 minutes improves the adhesion and evaporates residual water. Here, we transferred the membrane to a 50 µm thick polyimide foil (Fig. 6.3).

The transferred device exhibits a transistor characteristic (red curve in Fig. 6.4), with changed performance parameters compared to the measurement prior to the transfer.

We noticed a decrease of the gate leakage current due to the insulating plastic substrate, an average decrease of the output resistance by a factor of ≈6, a shift of the threshold voltage by -0.3 V, and an increase of the mobility by ≈1 cm^{2}V^{-1}s^{-1} which is mirrored by the in-

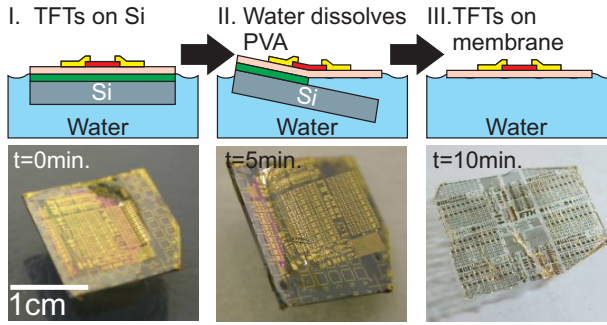

Figure 6.2: Releasing process: H_2O dissolves the PVA and release the 1 µm thick parylene membrane incl. the TFTs.

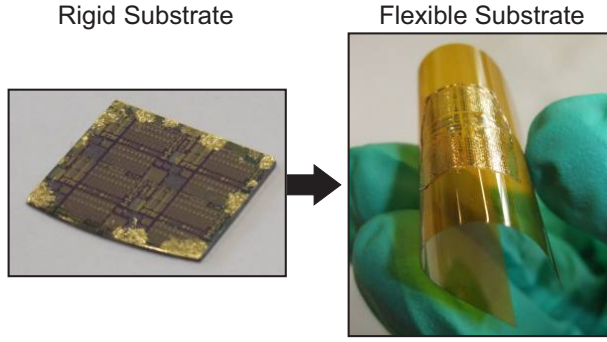

Figure 6.3: TFTs fabricated on a rigid Si substrate can e.g. be transferred to a flexible polyimide foil.

creased transconductance and I_{on}/I_{off} ratio (red curve in Fig. 6.4). The observed shift of the threshold voltage and the mobility are caused by the absorption of water during the transfer [6]. To demonstrate the flexibility of the TFTs on their new substrate, we bent the devices around a rod with a radius of 5 mm in a way that tensile strain (≈0.5 %, substrate thickness: 51 µm) parallel to the TFT channel was applied. The blue curve in Fig. 6.4 demonstrates that the TFTs stay fully functional and exhibit a slightly increased I_{on}, as expected from IGZO TFTs under tensile strain [5]. The performance parameters of the TFT at

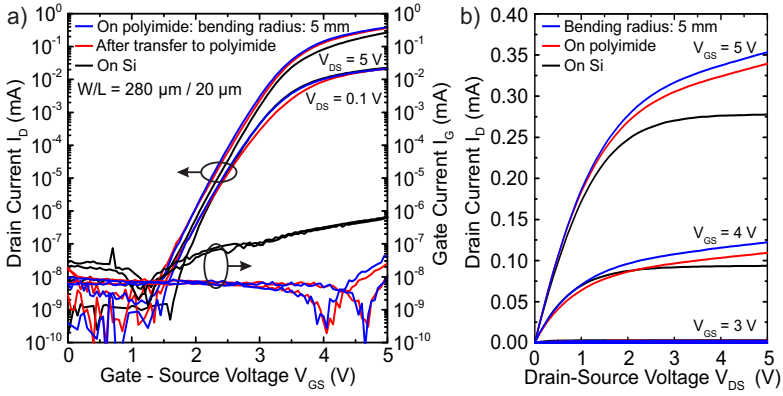

Figure 6.4: DC characteristic of an IGZO TFT measured on Si, transferred to a 50 µm thick polyimide foil, and bent to a tensile radius of 5 mm (strain ≈0.5 %) parallel to the TFT channel: a) Transfer-, b) Output characteristic.

the different fabrication steps (on Si, transferred to polyimide, bent on polyimide) are summarized in Tab. 6.1. Due to the formation of cracks in the TFT stack, device operation at bending radii smaller than 5 mm (strain >0.5 %) is not possible.

Since the mechanical strain in the TFT stack under bending strongly depends on the substrate thickness, smaller bending radii are possible by a direct transfer of the parylene membrane to a curved surface. In this case the substrate thickness is only 1 µm, and the strain in the TFTs stack reduces accordingly (e.g. a bending radius in of 0.1 mm corresponds to mechanical strain of only 0.4 % when calculated with a substrate thickness of 1 µm). The transfer of a TFT to a curved surface is demonstrated in Fig. 6.5. Here the parylene membrane with TFTs is attached to a plastic rod with a radius of 2 mm. The corresponding transfer and output characteristics of a transferred TFT are shown in Fig. 6.6. In contrast to TFTs on a 50 µm thick polyimide substrate, the transferred TFTs are fully operational while bent to a radius of 2 mm.

Table 6.1: Performance parameters of the same TFT measured on Si, after transfer to polyimide, and bent to a tensile radius of 5 mm. Performance improves after transfer to a non-conductive substrate.

Parameter (saturation region)	**Silicon** as fabricated	**Polyimide** transfered	**Bent Polyimide** radius =5 mm
field effect mobility ($cm^2V^{-1}s^{-1}$)	21.3	22.6	22.1
threshold voltage (V)	2.7	2.4	2.2
transconductance (V_{DS} = V_{GS} =5 V) (μS)	195	245	250
subthreshold swing mV/decade	245	220	211
I_{on}/I_{off} ratio (V_{DS} = V_{GS} =5 V)	6×10^7	2×10^8	3×10^8
gate current (V_{DS} = V_{GS} =5 V) (pA)	658	11	10

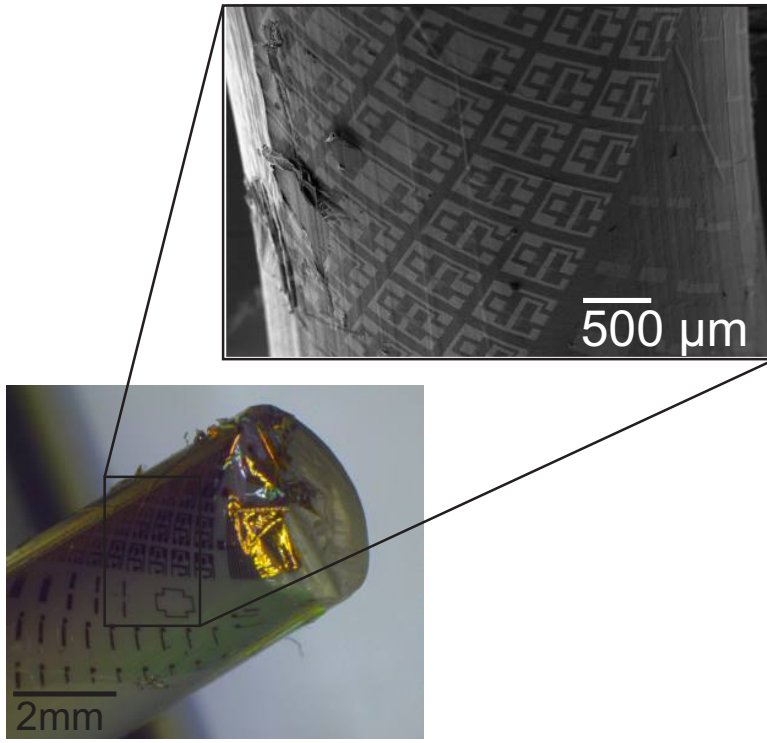

Figure 6.5: Micrograph and SEM image of a parylene membrane (incorporating TFTs) transferred to a plastic rod with a radius of 2 mm. Due to the thin membrane the strain is only SI0.02%.

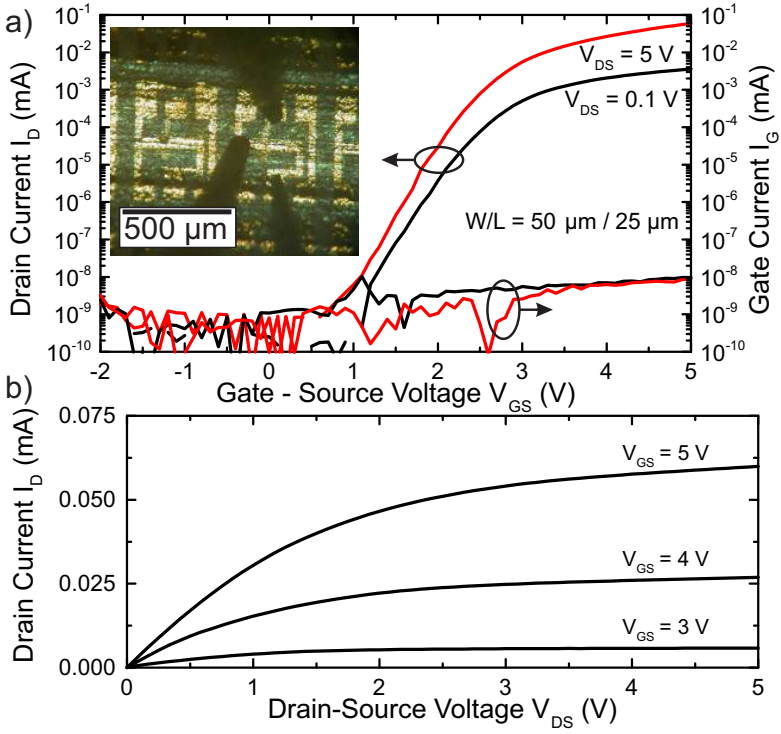

Figure 6.6: Transfer characteristic (a), and output characteristic (b) measured on a TFT transferred to a plastic rod with 2 mm radius. The inset shows the bent and contacted TFT.

Bibliography

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, 432(7016):488–492, 2004.

[2] H. Klauk, M. Halik, U. Zschieschang, F. Eder, G. Schmid, and C. Dehm. Pentacene organic transistors and ring oscillators on glass and on flexible polymeric substrates. *Applied physics letters*, 82(23):4175–4177, 2003.

[3] N. Münzenrieder, L. Petti, C. Zysset, G.A. Salvatore, T. Kinkeldei, C. Perumal, C. Carta, F. Ellinger, and G. Tröster. Flexible a-IGZO TFT amplifier fabricated on a free standing polyimide foil operating at 1.2 MHz while bent to a radius of 5 mm. In *Electron Devices Meeting (IEDM), 2012 IEEE International*, pages 5–2. IEEE, 2012.

[4] D. Tsamados, N.V. Cvetkovic, K. Sidler, J. Bhandari, V. Savu, J. Brugger, and A.M. Ionescu. Double-gate pentacene thin-film transistor with improved control in sub-threshold region. *Solid-State Electronics*, 54(9):1003–1009, 2010.

[5] D. Shahrjerdi and S.W. Bedell. Extremely flexible nanoscale ultrathin body silicon integrated circuits on plastic. *Nano Letters*, 13(1):315–320, 2013.

[6] J.-S. Park, J.K. Jeong, H.-J. Chung, Y.-G. Mo, and H.D. Kim. Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water. *Applied Physics Letters*, 92(7):072104–072104, 2008.

7

TFTs with ductile gate contacts

Niko Münzenrieder, Luisa Petti, Christoph Zysset, Deniz Görk, Lars Büthe, Giovanni A. Salvatore, Gerhard Tröster

Investigation of gate material ductility enables flexible a-IGZO TFTs bendable to a radius of 1.7 mm

43rd European Solid-State Device Research Conference (ESSDERC13), pp. 362–365, 2013.

Abstract

TFTs on flexible plastic foils have the potential to enable new applications like electronic skins or smart textiles. Due to the temperature sensitivity of plastic substrates, amorphous In-Ga-Zn-O (a-IGZO) is a promising semiconductor since it provides a carrier mobility >10 $cm^2V^{-1}s^{-1}$ when deposited at room temperature. Therefore, a-IGZO TFTs have significantly increased electrical performance compared to organic TFTs, but also suffer from a decreased bendability. Here, focused ion beam (FIB) images are used to identify the gate metal as the dominant factor for the formation of cracks in bent a-IGZO TFTs. Flexible a-IGZO TFTs using a high-k Al_2O_3 gate dielectric and different gate contact materials (Cr, Pt, Ti, or Cu) exhibit a similar effective mobility μ_{FE}, threshold voltage V_{th}, and on-off current ratio of: ≈15 $cm^2V^{-1}s^{-1}$, ≈1 V, and >10^9. Simultaneously, bending experiments confirmed that their bendability depends on the ductility of the gate material. These findings are used to identify Cu as suitable gate material, and to fabricate a-IGZO TFTs on free-standing plastic foil which can be operated at a bending radius of 1.7 mm (1.55 % strain), whereas bending shifts μ_{FE} and V_{th} only by +2 %, and -6 mV.

7.1 Introduction

Electronics on flexible substrates, especially thin-film transistors (TFTs) fabricated directly on free standing plastic foils promise to enable a number of new and cheap devices such as bendable displays, electronic skins and smart textiles [1]. The realization of such novel applications calls for TFTs on plastic substrates which are designed and fabricated according to three major constrains: First, the temperature sensitivity of plastic substrates generally limits the maximum fabrication process temperature to values smaller than ≈150 °C [2]. Second, the TFTs need to provide a sufficient electrical performance. The two most important parameters are the effective mobility μ_{FE} and the threshold voltage V_{th}, whereas μ_{FE} should be as high as possible and V_{th} should enable transistor operation at voltages <5 V. The third constrain of flexible TFTs is their bendability. Here smaller bending radii enable a larger number of potential applications and a more unobtrusive integration of electronics into everyday objects.

Although, transistors partially or completely made from organic materials offer a bendability to radii <1 mm [3, 4], TFTs based on amorphous Indium-Gallium-Zinc- Oxide (a-IGZO) [5], especially in combi-

nation with a high-k gate dielectric like Al_2O_3 have attracted much attention because they provide a significantly better electrical performance (e.g. mobilities >10 $cm^2V^{-1}s^{-1}$) when compared to organic TFTs [6]. To achieve a high bendability, the adhesion between the different material layers of flexible TFTs has to be optimized, which lead to the fact that until now one of the most common gate metals for the fabrication of flexible bottom gate TFTs (organic and inorganic) is Cr [7, 8, 9]. This is because Cr provides a good adhesion on plastic substrates. The measured influence of bending flexible a-IGZO TFTs with a Cr bottom gate is presented in Fig. 7.1. The graph shows a small increase of the effective mobility with decreasing bending radius, and also illustrates that no transistor operation can be observed at bending radii smaller ≈4 mm. The mobility shift as well as the minimal possible bending radius have been reported earlier and are typical for a-IGZO TFTs under tensile strain [10, 11]. At the same time, the exact reason for the limited bendability was not investigate in the past.

In this paper, the formation of cracks in the Cr gate metal is identified as the dominant failure mechanism of bent flexible a-IGZO bottom gate TFTs. This finding leads to the use of more ductile gate metals, whereas Cu enabled the fabrication of flexible a-IGZO TFTs on free standing plastic foil which can withstand bending radii smaller than 2 mm.

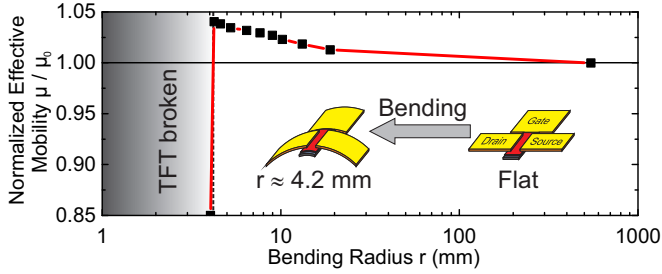

Figure 7.1: Influence of tensile bending on the effective mobility of a-IGZO TFTs with Cr bottom gates.

7.2 Origin of device failure under strain

Optical microscope and SEM images of a bent (r =3.5 mm) TFT with Cr bottom gate (cross section and martials shown in Fig. 7.2) show multiple cracks in the TFT channel region, which are aligned perpendicular to the applied mechanical stain (Fig. 7.3a+b), but neither optical nor SEM top view micrographs are able to show the origin of these cracks. Therefore, a focused ion beam (FIB) combined with a SEM has been used to take a cross sectional image (Fig. 7.3c) of a flexible a-IGZO TFT while bent to a radius of 3.5 mm (using a metal rod). The cross section shows that the crack has an average width of ≈30 nm, and gets wider close to the flexible polyimide substrate. Despite that the mechanical strain is higher in the upper layers of the TFT stack the Ti/Au top metallization is partially able to bridge the crack, while the lower Cr bottom gate is totally separated. This can be explained by the higher ductility of Au compared to Cr, but it also demonstrates that the limiting factor for the bendability is not the ceramic a-IGZO semiconductor or the Al_2O_3 gate insulator but the metallic and normally crystalline Cr [12]. Hence, the replacement of the Cr gate by a more ductile metal promises to improve the bendability of the TFTs, without a loss of the beneficial electrical properties of a-IGZO or Al_2O_3.

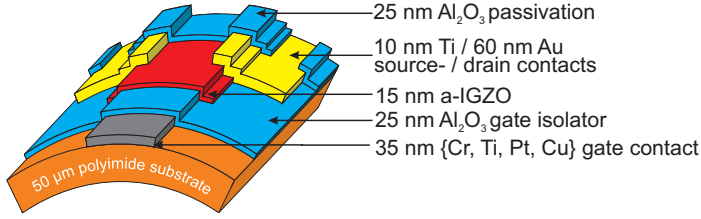

Figure 7.2: Schematic of the fabricated flexible bottom gate TFTs.

7.3 Flexible TFTs using various gate metals

Beside Cr (rupture strain ϵ_R ≈0.5 % [13]), materials with a higher ductility have been selected a gate metal. These are Ti (ϵ_R ≈2 % [14]), Pt (ϵ_R ≈4 % [15]), and Cu (ϵ_R ≈4.5 % [16]).

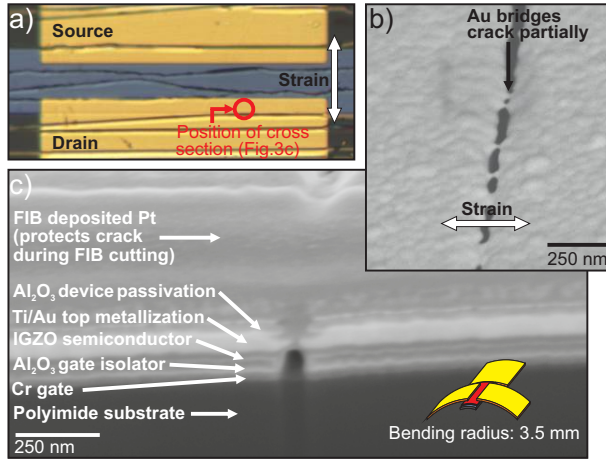

Figure 7.3: Optical (a) and SEM (b) top view, and cross sectional FIB (c) image of a crack in a flexible a-IGZO TFT (Cr gate contact) bent to a radius of 3.5 mm. The picture shows the gate/drain overlap region (marked in Fig. 7.3a), here all material layers are present.

7.3.1 Fabrication

A schematic of the flexible TFTs is shown in Fig. 7.2. A 50 µm thick polyimide foil served as substrate. Since not all metals provide an adhesion as good as the one of Cr, the adhesion of the polyimide was improved by a 60 min ozone treatment. Following the e^--beam evaporation and structuring (lift-off) of the 35 nm thick gate contact (Cr, Ti, Pt, or Cu), a 25 nm thick Al_2O_3 gate insulator (ϵ_r =9.5) was deposited in an ALD process, and a 15 nm thick a-IGZO semiconductor was deposited by room temperature RF magnetron stuttering. Next, Al_2O_3 and a-IGZO were structured by wet etching. A Ti/Au (10 nm/ 60 nm) top metallization was used to fabricate source and drain contacts in a lift-off process. The fabrication was concluded by an additional 25 nm thick Al_2O_3 layer as device passivation. The maximum process temperature during the fabrication was 150 °C. A more detailed description of the fabrication process can be found in [11].

Table 7.1: Electrical performance parameters (saturation region) of flexible a-IGZO TFTs, fabricated using different gate metals.

Parameter	Gate metal			
	Cr	**Ti**	**Pt**	**Cu**
Theshold voltage (V)	1.1	1.0	1.2	1.1
Subthreshold swing (mV/decade)	102	126	110	154
Transconductance (mS) (V_{DS} = V_{GS} =5 V)	0.18	0.19	0.17	0.20
On-off current ratio (V_{DS} =0 V, 5 V)	9×10^9	2×10^{10}	2×10^{10}	4×10^9
Effective mobility ($cm^2V^{-1}s^{-1}$)	15	15.3	14.7	16.1
Gate current (A) (V_{DS} = V_{GS} =5 V)	1.2×10^{-10}	3.6×10^{-10}	1.1×10^{-10}	1.7×10^{-10}

7.3.2 Performance

Performance parameters were extrapolated from transfer characteristics measured under ambient conditions in the saturation regime using standard MOSFET equations [17].

Fig. 7.4 shows typical transfer and corresponding output characteristics of the fabricated TFTs. The W/L ratio is always 560 µm/ 60 µm. The measurement demonstrates that the electrical performance is not significantly influenced by the use of different gate metals. This is also shown in Tab. 7.1, where the performance parameters of TFTs with Cr, Ti, Pt, and Cu gate are compared. It is worth mentioning that although the four metals have work functions ϕ which vary by up to ≈1.3 eV [17], the threshold voltage is nearly independent from the used gate metal. This can be explained by the fact that the fixed oxide charges [17] have a bigger influence on V_{th} than the work function difference.

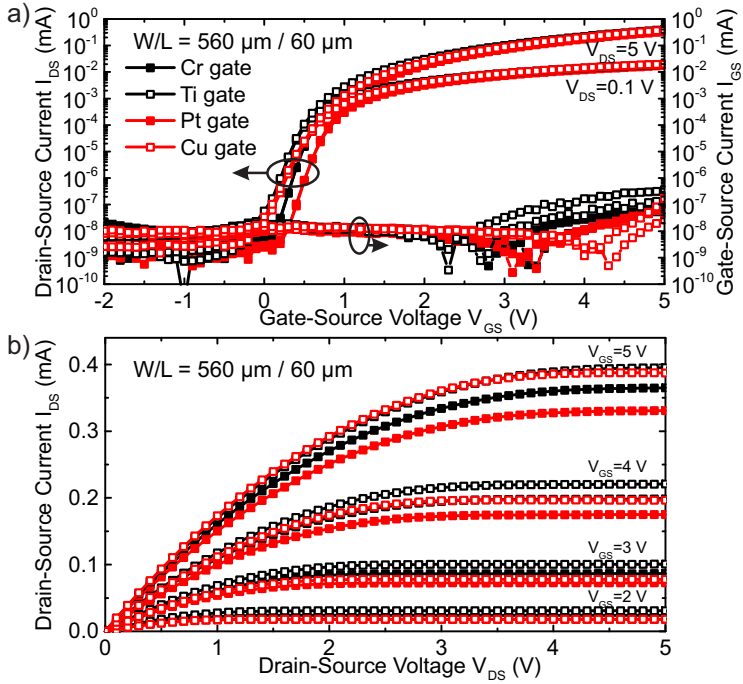

Figure 7.4: Transfer (a) and output (b) characteristics of typical a-IGZO TFTs fabricated using diffent gate metals.

7.4 Bending

7.4.1 Experimental

To measure the influence of bending on the fabricated TFTs in a reliable way, we used a TFT layout with contact pads ≈1 cm away from the channel, and a custom build bending tester [11] shown in Fig. 7.5. To perform the measurement, a single TFT was cut from the substrate and attached to a flexible carrier substrate. An electrical contact between the pads of the TFT and the interconnect lines on the carrier substrate was made with glued Cu wires. The interconnect lines on the carrier substrate itself were connected with a parameter analyzer. Thereby, the TFT can be measured at arbitrary bending radii without the need to place any probe tips. The large distance between channel region and

contact pads also ensures that the mechanical properties of the TFT are not influenced by the measurement setup. The carrier substrate is then mounted between two movable plates in a custom build bending tester. Here, a change of the plate distance changes the bending radius of the TFT, whereas the actual bending radius was monitored with a CCD camera.

TFTs were characterized at different bending radii starting from a flat substrate down to a minimum radius of 1.1 mm. This corresponds to tensile mechanical strain between 0.07 % and 2.3 %, calculated using the strain theory developed in [18] (the calculation also considers the build in strain of the flat substrate). Tensile strain was chosen because it is known that it has a bigger influence then compressive one [11]. TFTs were always bent parallel to the TFT channel and therefore also parallel to the current flow. To minimize the effect of electrical stress on the measurement, the gate voltage V_{GS} was only varied in a small interval (V_{GS} = -0.5 V...2.5 V).

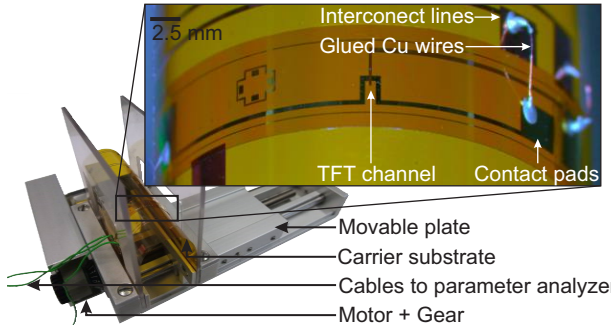

Figure 7.5: Custom-built bending tester with a loaded carrier substrate and close up of the attached flexible TFT bent to a radius of ≈8 mm.

7.4.2 Results

The influence of bending on TFTs with different gate metals is shown in Fig. 7.6. Here, the evolution of the effective mobility μ_{FE} for different bending radii is plotted. For easier comparison, the values are normalized by the value measured at the flat substrate. The graph shows that the gate metal has a significant influence on the bending performance. The Cr gate TFT shows only a small variation of the mobility

(≈4 %) as long as the strain in smaller than 0.7 % (r =3.8 mm), whereas at higher strain values a decrease of the mobility by several orders of magnitude is observed. The strain value at which the mobility drops significantly corresponds to the strain at which crack formation starts. We define this strain value as the threshold strain ϵ_{TH}, it is a measure for the bendability of the TFTs. The inset of Fig. 7.6 demonstrates the influence of cracks on the transfer characteristic, which mirrors the decrease of the mobility at $\epsilon > \epsilon_{TH}$. The cracks in the channel region reduce the TFT conductivity (causing the mobility decrease), and also reduce the controllability of the channel (causing the off-current increase). In contrast to the Cr TFT the TFTs with more ductile gate metals exhibit significantly higher ϵ_{TH} values. In particular the Cu gate TFT is fully operational up to a stain of 1.55 % (r =1.7 mm). To demonstrate the full functionality of the Cu gate TFT while bent to a radius <2 mm, Fig. 7.7 shows the transfer characteristic while flat and bent to a radius of 1.7 mm. Here, the threshold voltage is decreased by ≈6 mV and the mobility is increased by ≈2 %, which is in good agreement with previously published values [10, 11].

As long as the strain value in the channel region was never larger than ϵ_{TH}, the TFTs stay fully functional after they are reflattened subsequently to the bending experiment.

For a reliable and comparable quantification of the minimal possible bending radius, defined as the bending radius corresponding to ϵ_{TH}, multiple bending tests (up to 5 per gate material) were performed. The observed minimal bending radii (average value and standard deviation) are visualized in Fig. 7.8. The graph shows that a-IGZO TFTs with Cu gates can be reliably bent to radii <2 mm which is an improvement by a factor ≈2 compared to previously published a-IGZO TFTs fabricated on free standing plastic foil. The measured minimal bending radii for all gate materials and the rupture strain ϵ_R of the same materials (measured on thin-films) are summarized in Tab. 7.2. At the one hand side, the table shows a clear correlation between the measured ϵ_{TH} and the reported ϵ_R of the gate metals. At the other hand, although ϵ_R reaches values up to 4.5 % the flexibility of the TFTs saturates at strain value of ≈1.5 %. This shows that at strain levels around 1.5 % the brittleness of the a-IGZO and/or the Al_2O_3 is getting dominant, indicating that more strain resistive TFTs are only possible with a modification of the semiconductor and/or gate insulator layer which would also influence the electrical performance. Additionally, we observed that while an increase of the channel length L leads to

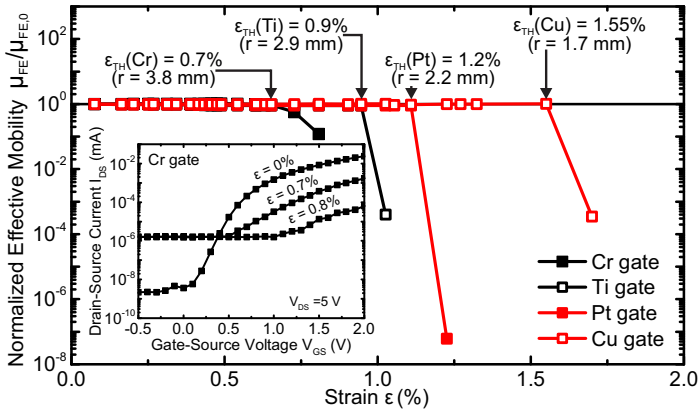

Figure 7.6: Typical evolution of the normalized effective mobility with increasing mechanical strain for flexible a-IGZO TFTs fabricated using gate metals with different ductilities. The inset shows the degradation of the transfer characteristic in the saturation regime (Cr gate TFT) which corresponds to the drastically reduced μ_{FE} at high strain values.

less strain resistive TFTs (for bending parallel to the channel), TFTs with shorter L do not exhibit a significantly improved bending performance (measured down to a channel length of 10 µm). Nevertheless, even smaller bending radii of a-IGZO TFTs are expected to be possible by a reduction of the strain in the devices by an encapsulation of the TFTs or the use of thinner substrates.

7.5 Conclusion

The formation of cracks in bent flexible a-IGZO TFTs has been investigated, and the ductility of the gate metal was identified as the limiting factor of their bendability. These findings have been used to optimize the cracking behavior of flexible TFTs by the use of more ductile materials without significantly influencing their electrical performance. TFTs fabricated on free standing polyimide foil, and based on Cu gate contacts exhibit full functionality when bent to a radius of 1.7 mm (ϵ =1.55 %), which is to our knowledge the smallest value ever reported on flexible a-IGZO TFTs. At this bending radius the Cu gate TFTs exhibit a by ≈6 mV decreased threshold voltage and a ≈2 % increased

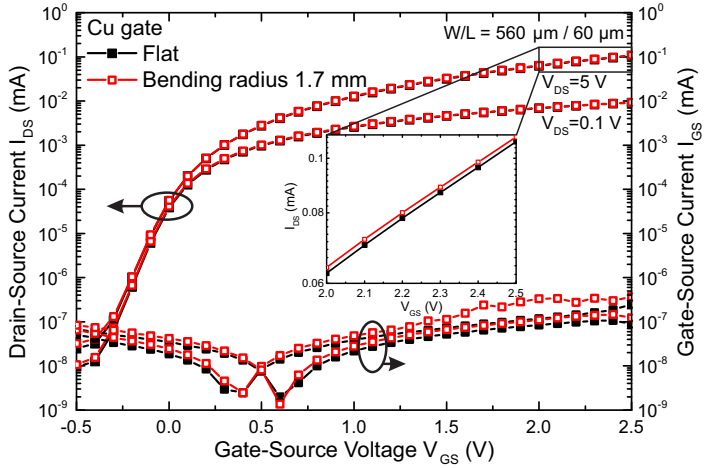

Figure 7.7: Transfer characteristics of a Cu gate a-IGZO TFT while flat and bent to a tensile radius of 1.7 mm (ϵ =1.55 %). The inset shows the under strain increased drain current. The slightly different shape of the characteristics compared to Fig. 7.5 results from a different measuring range, and especially from a worse electrical connection via the carrier substrate.

effective mobility. These results in combination with the fact that Cu is a cheap material with a high electrical conductivity suggest that Cu is the most suitable gate material for flexible a-IGZO TFTs.

Acknowledgment

Authors would like to thank Joakim Reuteler from the ETH Zurich Electron Microscopy Center for the FIB images.

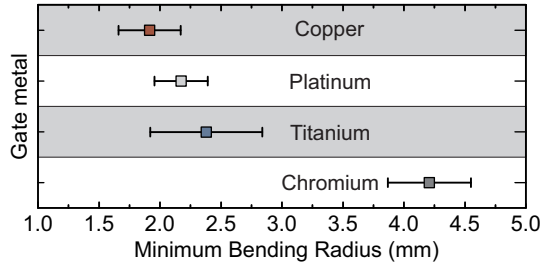

Figure 7.8: Influence of the gate metal on the minimum bending radius (the data points and error bars give the mean values and the standard deviation).

Table 7.2: Bending performance of flexible a-IGZO TFTs, fabricated using different gate metals, and previosly reported rupture strains of the same metals [13, 14, 15, 16].

Parameter		Gate metal Cr	Ti	Pt	Cu
Average value	Minimum bending radius (mm)	4.2	2.4	2.2	1.9
	Strain (ϵ_{TH})	0.67 %	1.12 %	1.21 %	1.39 %
Best measured value	Minimum bending radius (mm)	3.8	1.9	2	1.7
	Strain (ϵ_{TH})	0.73 %	1.39 %	1.33 %	1.55 %
Rupture strain of thin films (ϵ_R)		≈0.5 %	≈2 %	≈4 %	≈4.5 %

Bibliography

[1] R.F. Service. Patterning electronics on the cheap. *Science*, 278:383–384, 1997.

[2] A. Sazonov, D. Striakhilev, C.-H. Lee, and A. Nathan. Low-temperature materials and thin film transistors for flexible electronics. *Proceedings of the IEEE*, 93(8):1420–1428, 2005.

[3] T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya. Flexible organic transistors and circuits with extreme bending stability. *Nature materials*, 9(12):1015–1022, 2010.

[4] L. Han, K. Song, P. Mandlik, and S. Wagner. Ultraflexible amorphous silicon transistors made with a resilient insulator. *Applied Physics Letters*, 96(4):042111–042111, 2010.

[5] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, 432(7016):488–492, 2004.

[6] F. Ante, F. Letzkus, J. Butschke, U. Zschieschang, K. Kern, J.N. Burghartz, and H. Klauk. Submicron low-voltage organic transistors and circuits enabled by high-resolution silicon stencil masks. In *Electron Devices Meeting (IEDM), 2010 IEEE International*, pages 21–6. IEEE, 2010.

[7] J.S. Meena, M.-C. Chu, C.-S. Wu, J.-C. Liang, Y.-C. Chang, S. Ravipati, F.-C. Chang, and F.-H. Ko. Facile synthetic route to implement a fully bendable organic metal–insulator–semiconductor device on polyimide sheet. *Organic Electronics*, 13(5):721–732, 2012.

[8] D. Zhao, D.A. Mourey, and T.N. Jackson. Fast flexible plastic substrate zno circuits. *Electron Device Letters, IEEE*, 31(4):323–325, 2010.

[9] H. Kavak and H. Shanks. Stability of hydrogenated amorphous silicon thin film transistors on polyimide substrates. *Solid-state electronics*, 49(4):578–584, 2005.

[10] D.I. Kim, B.U. Hwang, J.S. Park, H.S. Jeon, B.S. Bae, H.J. Lee, and N.-E. Lee. Mechanical bending of flexible complementary inverters based on organic and oxide thin film transistors. *Organic electronics*, 13(11):2401–2405, 2012.

[11] N. Münzenrieder, K.H. Cherenack, and G. Tröster. The effects of mechanical bending and illumination on the performance of flexible IGZO TFTs. *IEEE Transactions on Electron Devices*, (99):1–8, 2011.

[12] J.E. Nestell, R.W. Christy, M.H. Cohen, and G.C. Ruben. Structure and optical properties of evaporated films of the cr-and v-group metals. *Journal of Applied Physics*, 51(1):655–660, 1980.

[13] M.J. Cordill, A. Taylor, J. Schalko, and G. Dehm. Fracture and delamination of chromium thin films on polymer substrates. *Metallurgical and Materials Transactions A*, 41(4):870–875, 2010.

[14] H. Ogawa, K. Suzuki, S. Kaneko, Y. Nakano, Y. Ishikawa, and T. Kitahara. Tensile testing of microfabricated thin films. *Microsystem technologies*, 3(3):117–121, 1997.

[15] K.N. Jonnalagadda, I. Chasiotis, S. Yagnamurthy, J. Lambros, J. Pulskamp, R. Polcawich, and M. Dubey. Experimental investigation of strain rate dependence of nanocrystalline pt films. *Experimental mechanics*, 50(1):25–35, 2010.

[16] N. Lu, Z. Suo, and J.J. Vlassak. The effect of film thickness on the failure strain of polymer-supported metal films. *Acta Materialia*, 58(5):1679–1687, 2010.

[17] S.M. Sze and K.K. Ng. *Physics of Semiconductor Devices*. John Wiley and Sons, 2007.

[18] H. Gleskova, S. Wagner, and Z. Suo. a-si: H thin film transistors after very high strain. *Journal of Non-Crystalline Solids*, 266:1320–1324, 2000.

8

Design of digital circuits based on flexible IGZO TFTs

Niko Münzenrieder, Christoph Zysset, Thomas Kinkeldei, Gerhard Tröster

Design rules for IGZO logic gates on plastic foil enabling operation at bending radii of 3.5 mm

IEEE Transactions on Electron Devices, vol. 59, no. 8, pp. 2153–2159, 2012.
10.1109/TED.2012.2198480

Abstract

Findings obtained from bending experiments with mechanically flexible InGaZnO-based thin-film transistors are used to derive design rules for flexible InGaZnO-based n-channel metal–oxide–semiconductor logic circuits. Based on the developed design rules, flexible NAND *gates, inverters, and five-stage ring oscillators are fabricated directly on free-standing plastic foils at temperatures ≤150 °C. Geometrically well-designed circuits operated at a supply voltage of 5 V are exposed to tensile mechanical strains, induced by bending, up to 0.72 % without performance degradation. This corresponds to a bending radius of 3.5 mm. At the same time, increases in the rise time by a factor of ca 2 and reductions in the high and low output voltage levels by ca 10 % and 50 % have been observed for circuits with disadvantageous geometrical design. Ring oscillators designed to be operated under strain show an increase in oscillation frequency from 22.9 kHz (flat substrate) to 23.32 kHz (bending radius: 3.5 mm). This demonstrates the field-effect mobility increase in a-IGZO-based circuits under tensile mechanical strain. Long-term reliability is evaluated with 20 000 cycles of repeated bending and reflattening without circuit failure.*

8.1 Introduction

Electronic circuits on flexible substrates promise to enable a number of new applications, such as rollable displays, electronic skins, or woven electronics [1]. In addition, the system-on-panel approach, which was demonstrated in [2], aims to integrate, e.g., sensors, actuators, and control electronics on flexible substrates, to reduce the fabrication costs. While organic and a-Si:H-based thin-film transistors (TFTs) fabricated on flexible substrates, in general, suffer from low mobilities at or below $1\,cm^2V^{-1}s^{-1}$ [3], [4], state-of-the-art single-crystalline silicon chips have to be thinned and transferred to foils [5]. At the same time, TFTs based on oxide semiconductors, such as amorphous indium–gallium–zinc-oxide (a-IGZO), fabricated at temperatures ≤150 °C, provide electron mobilities above $10\,cm^2V^{-1}s^{-1}$ [6]. Therefore, a-IGZO combines higher mobilities than other amorphous materials with the ability of low-temperature deposition directly on large-area temperaturesensitive plastic substrates.

While a-IGZO-based circuits, either fabricated on or transferred to plastic foil, have been presented [7, 8], the influence of bending these circuits is nearly not investigated, although this is a crucial point in

flexible electronics. The influence of strain, induced by bending the substrate, on the electrical performance of a-IGZO TFTs was already determined by our work [9] and other groups' work [10]. Fig. 8.1 shows a typical evolution of the TFT saturation field-effect mobility versus mechanical strain induced by tensile bending of the substrate. Strain was applied parallel and perpendicular to the TFT channel. Parallel bending increases the mobility until the TFT is destroyed above 0.72 % strain (ϵ). Perpendicular bending at the same time only slightly increases the mobility for small values of strain (≈0.3 %) but leads to capillary cracks and, therefore, a strong performance degradation if the strain is increased above ≈0.3 %. The formation and influence of capillary cracks will be discussed later in this paper. The different effects of parallel and perpendicular bending have to be taken into account when designing and fabricating flexible a-IGZO circuits, which should be operated under mechanical strain.

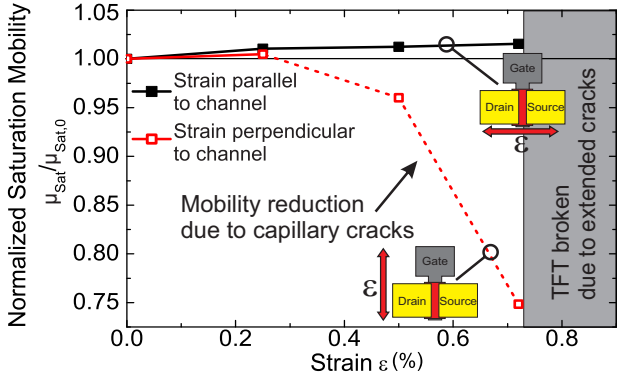

Figure 8.1: Typical mobility changes induced by mechanical tensile stain caused by bending. As indicated by the insets, strain was applied parallel and perpendicular to the a-IGZO TFT channel.

Here, we use findings from bending experiments with single a-IGZO TFTs on plastic foils to derive design rules for flexible NMOS a-IGZO logic circuits. The design rules are used to fabricate NAND gates, inverters, and five-stage ring oscillators, which can be bent to a radius of 3.5 mm. Additionally, the circuits are fully operational after 20 000 cycles of repeated bending and reflattening.

8.2 Fabrication Process

A free-standing 50 µm-thick polyimide foil served as substrate for the fabrication of n-type a-IGZO TFTs using a passivated bottom-gate inverted staggered TFT geometry, as described in [9]. The device geometry, including layer materials and thicknesses, is shown in Fig. 8.2. All metal layers were evaporated, whereas Al_2O_3 was fabricated by atomic layer deposition. The a-IGZO semiconducting layer was radiofrequency sputtered at room temperature. In addition to [9], the Cr gates were cleaned by an ozone plasma for 60 min after etching to increase the adhesion of the Al_2O_3 gate oxide. Circuit interconnect lines were integrated into the top metallization layer. The chosen materials and fabrication techniques are a tradeoff between performance, low-temperature fabrication, thickness reduction of brittle materials, and adhesion between different material layers, aiming at long-term reliability and bendability.

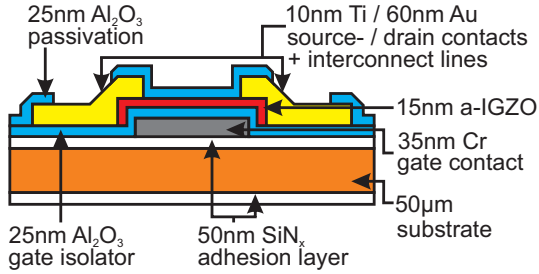

Figure 8.2: Cross section of our flexible a-IGZO TFTs.

A typical a-IGZO TFT (W/L = 280 µm/35 µm) transfer characteristic is shown in Fig. 8.3. The performance parameters, which are extrapolated using standard MOSFET equations [11], are threshold voltage V_{th} = 0.3 V, saturation field-effect mobility μ_{sat} = 13.5 $cm^2V^{-1}s^{-1}$, linear fieldeffect mobility μ_{lin} = 14.5 $cm^2V^{-1}s^{-1}$, transconductance g_m = 0.18 mS, on/off ratio I_{on}/I_{off} >10^7, and subthreshold swing (inverse of subthreshold slope) SS = 150 mV/decade.

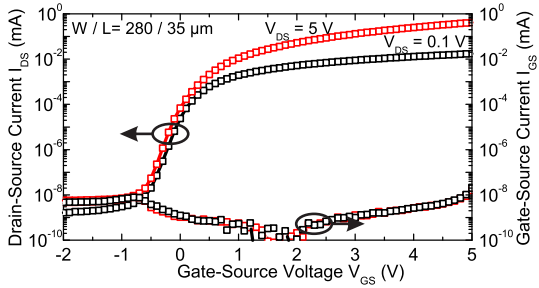

Figure 8.3: a-IGZO TFT transfer characteristic measured at source/drain voltages V_{DS} of 0.1 V (linear regime) and 5 V (saturation regime).

8.3 Influence of mechanical strain

Electrical measurements under tensile mechanical strain were performed by winding the flexible substrate around rods with 10-, 5-, and 3.5-mm radius and contacting them with probe tips. A bent substrate is shown in Fig. 8.4. The applied radii correspond to tensile mechanical strains in the channel of 0.25 %, 0.5 %, and 0.72 %, which are calculated using [12]. The effects of bending switching TFTs and load TFTs with connected gate and drain contacts were evaluated. Both elements are necessary to build logic gates. As described in the introduction, tensile strain changes the field-effect mobility (Fig. 8.1). Since the influence of compressive strain is smaller, compared with tensile strain [12], the qualitative behavior under compressive bending will be the same as under tensile bending with a negative mobility change in the elastic region (no formation of cracks), whereas compressive bending causes cracks at higher strain levels. The transfer characteristics of TFTs while flat and bent to a tensile radius of 3.5 mm are plotted in Fig. 8.5(a) and (b). The graphs show the different effects of stain (0.72 %), depending on the direction relative to the TFT channels. Parallel bending modifies the source drain current by less than 3 % [Fig. 8.5(b)], mainly due to a shift of the field-effect mobility. However, strain perpendicular to the channel strongly influences the TFT behavior. Fig. 8.5(a) shows, in particular, a reduction in the on-current (I_{on}) by ≈22 % and an increase in the off-current (I_{off}) by four orders of magnitude due to capillary cracks.

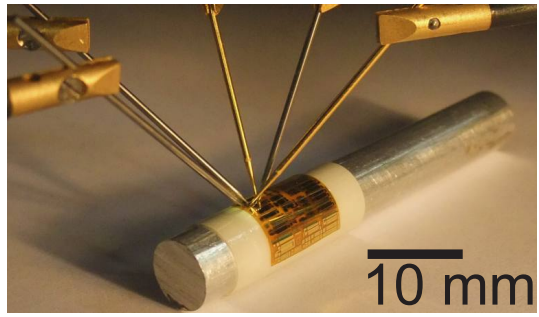

Figure 8.4: Photograph of the flexible substrate, bent to a tensile radius of 3.5 mm.

Comparable results are observed when bending load TFTs with connected gate and drain contacts [Fig. 8.5(c) and (d)]. Fig. 8.5(c) shows that strain perpendicular to the channel cause an increased resistance due to the reduced on-current. Strain parallel to the channel has no significant effect [Fig. 8.5(d)]. If the TFTs are reflattened after bending, their original characteristics are recovered.

The performance degradation of TFTs exposed to perpendicular stains >0.3 % is caused by the formation of capillary cracks, perpendicular to the applied mechanical strain. Fig. 8.6(a) shows one of these capillary cracks. The average width of the cracks while the substrate is bent to a radius of 3.5 mm was ≈90 nm. The cracks propagate through the chromium, a-IGZO, and Al_2O_3 layers. Ductile gold contacts are only damaged in areas where they are covered with Al_2O_3. This is because, aside from the ceramic a-IGZO and Al_2O_3 layers, chromium is, compared to other metals like gold, a brittle material [13]. We measured an average distance between two neighboring capillary cracks of ≈100 µm, but in approximately 50 % of all cases, only one crack within one TFT channel was visible. The two closest cracks we could find had a distance of 31 µm. Therefore, we observed capillary cracks only during bending perpendicular to the channel, because the width of the TFT channels is much larger than their length. Hence, all observed capillary cracks formed parallel to the channel. Consequently, perpendicular bending disconnects a part of the gate that remains floating. The floating and, hence, uncontrollable charges in the disconnected part of the gate result in an increased off-current similar to the drain

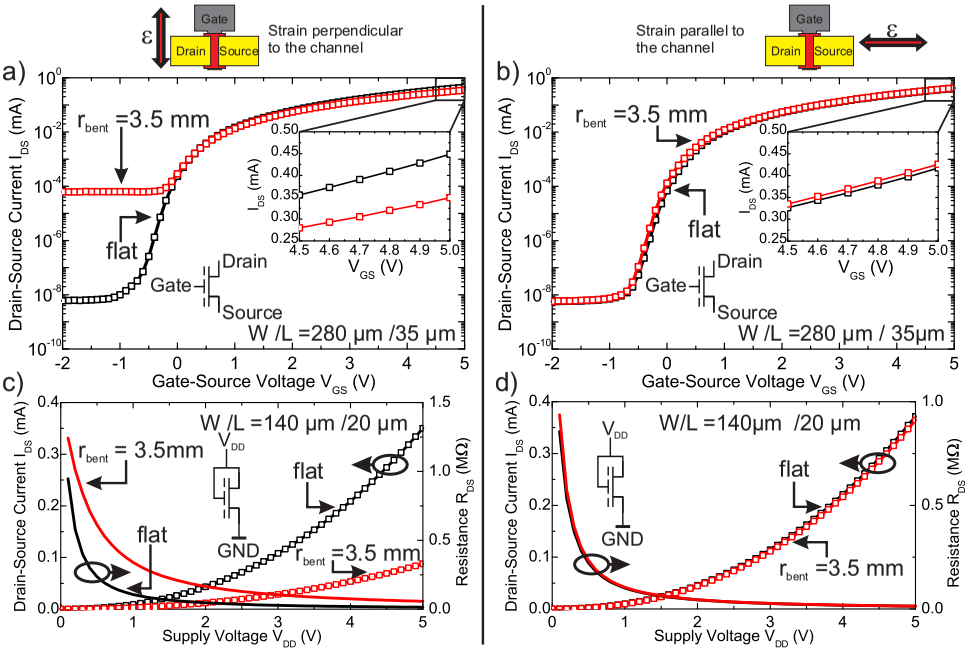

Figure 8.5: Single a-IGZO TFTs characterized while flat and with applied strain of 0.72 % (bending radius: 3.5 mm) a) perpendicular and b) parallel and to the channel (logarithmic Y axis). c) perpendicular and d) parallel strained load TFT with connected drain and gate contacts while flat and bent, including the static resistance (linear Y axis).

current at V_{GS} =0 V [Fig. 8.5(a)]. At the same time, the on-current is reduced due to the reduced effective W/L ratio. In total, this results in a reduced on/off-current ratio. Since the capillary cracks do not occur in specific locations but rather in a stochastic manner, the curves in Fig. 8.5(a) and (c) are exemplary and could also suffer from more or less distinct on/off-current ratio reductions. After reflattening the substrate, the observed capillary cracks are still visible, but their width is drastically reduced. The measured average width of capillary cracks at the surface of the reflattened substrate is 16 nm [Fig. 8.6(b)]. At the same time, both edges of the cracks have contact at several locations. Hence, reflattening reestablishes the electrical contact between the separated parts of the gate contact, and the original W/L ratio is recovered. The potentially higher electrical resistance of the closed crack is negligible because the electrical potential will still be uniform, due to the small gate current (I_{GS} <10 pA).

Bending to a radius smaller than 3.5 mm ($\epsilon > 0.72\,\%$) leads to extended cracks, causing short circuits between different material layers, and permanently destroys the TFTs. The orientation of these extended cracks depends on the direction of the applied strain. Destroyed TFTs, after strains $\epsilon > 0.8\,\%$, are shown in Fig. 8.6(c). In this case, reflattening does not recover the original TFT characteristic. These findings concerning the influence of the direction and strength of mechanical strain lead to the following design rules for digital NMOS a-IGZO circuits:

1. Driver TFTs should be strained only parallel to the channel to avoid capillary cracks and maintain switching performance as long as possible.

2. Load TFTs can be oriented in both directions relative to the driver TFTs without compromising the circuit operation, although a perpendicular alignment will increase the load resistance and modify the circuit performance if stained.

3. To avoid capillary cracks perpendicular to the channel, the gate length of TFTs strained parallel to the channel should be smaller than the expected minimal distance between two neighboring capillary cracks.

Additionally, two rules concerning the mechanical properties of our a-IGZO TFTs are derived.

4. Strain should, in general, not be increased above 0.72 %.

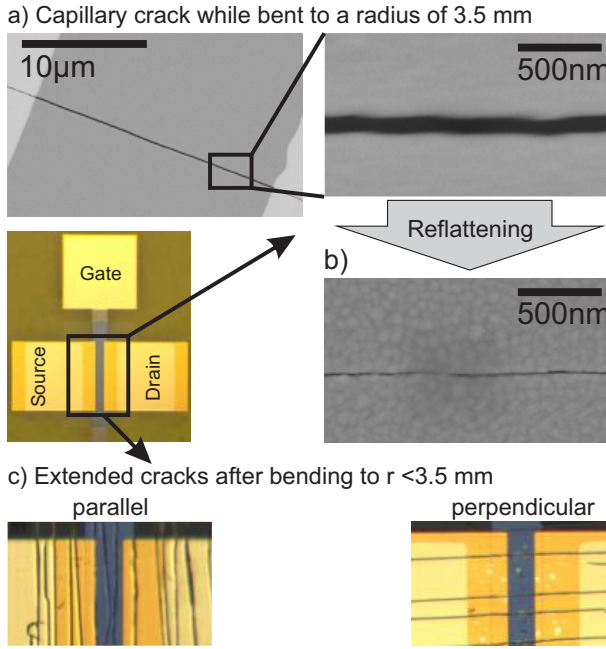

Figure 8.6: a) SEM images of a capillary crack parallel to the TFT channel induced by tensile bending (ϵ = 0.72 %) perpendicular to the channel. b) Capillary crack after reflattening the substrate. c) Extended cracks induced by tensile bending (ϵ > 0.72 %) parallel and perpendicular to the channel.

5. Temporarily applied mechanical strain should not influence the performance of the reflattened circuits.

8.4 Circuits

8.4.1 Circuit Design

To verify the design rules, we fabricated and tested digital NMOS circuits based on a-IGZO TFTs. All circuits are static n-type logic gates composed of load TFTs (W/L =140 µm/20 µm) and driver TFTs (W/L = 1400 µm/20 µm). The gate length is always smaller than the measured minimal crack distance of 31 µm (design rule 3). The fabrication of

circuits is identical to the fabrication of single TFTs, with the exception that the required interconnect lines are manufactured together with the gate and source–drain metallization layers; thereby, no additional process steps are required.

According to the design rules, all circuits were fabricated with load TFTs oriented parallel and perpendicular to the driver TFTs. (Therefore, strain can be applied parallel to the driver TFTs and, at the same time, parallel and perpendicular to the load TFTs). We fabricated inverters [Fig. 8.7(a)], NAND gates [Fig. 8.7(b)], and five-stage ring oscillators [Fig. 8.7(c)].

Fig. 8.7 also shows schematics of all circuits. Ring oscillators are designed with five inverters in a feedback loop plus an additional inverter as output buffer. In addition, Fig. 8.7 shows the direction of the applied strain for all circuits.

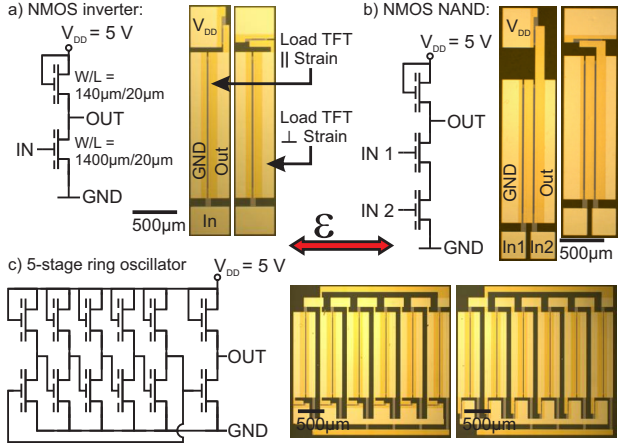

Figure 8.7: Circuit schematics and micrographs of the fabricated circuits with load TFTs aligned parallel and perpendicular to the driver TFTs: a) Inverter, b) NAND gate, 5-stage ring oscillator.

8.4.2 Circuit Characterization

As for single TFTs, circuits were bent around rods to characterize the influence of strain. In compliance with the constrains of the used a-IGZO TFTs, Fig. 8.4 shows a contacted NAND gate bent to a tensile

radius of 3.5 mm (ϵ = 0.72 %). According to design rule 1, driver TFTs are always strained parallel to the channel. The following measurement conditions were applied during electrical circuit characterization: supply voltage V_{DD} = 5 V, input voltage swing v_{in} = 5 V, and input signal frequency f_{in} = 1 kHz. All signals were monitored using a multichannel oscilloscope at a sampling rate of 50 MS s^{-1}. The total output load for the tested circuits was 1 MΩ and 300 pF. In everyday use, flexible devices will be repeatedly bent and reflattened. Therefore, we additionally tested the longterm stability of the flexible a-IGZO circuits by bending and reflattening them for multiple times. Cycling between a flat substrate and a tensile bending radius of 4.5 mm (ϵ = 0.56 %) was performed by using our custom-built automated bending tester [9]. Therefore, a unit cell of our substrate was mounted at the center of a larger (7.5 cm × 7.5 cm) carrier foil. The carrier foil itself was mounted in the bending tester, with one rim at the fixed part and the opposed one at the movable part of the bending tester. The bending tester moved the two opposed rims toward each other and therefore created a bending at the middle of the foil. The velocity of this movement was 1 mm s^{-1}. Ambient temperature and humidity during the long-term measurements were kept constant at 21 °C and 60 %RH. The circuits were illuminated using a standard light bulb, resulting in a constant illumination strength of 200 lx.

8.5 Results

The digital input and output signals of an exemplary a-IGZO inverter and NAND gates under mechanical strain are shown in Figs. 8.8(a) and 8.9, respectively. Both gates are measured before bending, while strained to 0.72 %, and after bending (reflattened). Additionally, Fig. 8(b) shows the analog characteristic of the inverter with the load TFT aligned perpendicular to the driver TFT while flat and strained by 0.72 %.

As expected from Fig. 8.5(b) and design rule 2, the digital circuits with all TFTs in parallel are insensitive to bending. On the one hand, tensile bending increases the field-effect mobility by ≈1.5 % (Fig. 8.1). At the same time, the output levels of NANDs and inverter gates are determined by the ratio between the conductivities of the load and driver TFTs. This ratio remains constant if all TFTs are stained by the same factor and in the same direction. We also do not see a change in the rise and fall times (t_r and t_f). A decrease in t_r and t_f

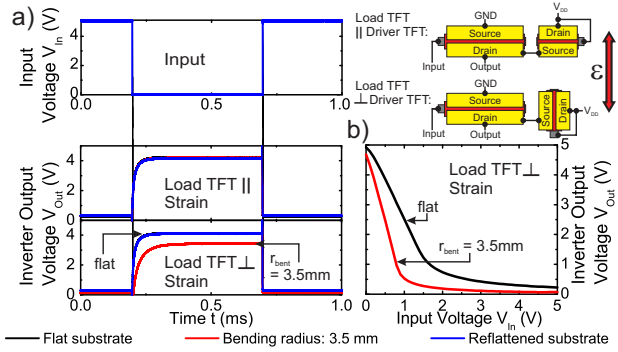

Figure 8.8: a) Input and output signals of fabricated inverter gates, before bending, with strain applied parallel to the driver TFTs and hence perpendicular and parallel to the load TFTs, and reflattened. b) DC characteristic measured with a parameter analyzer (different total output load) of the perpendicular aligned load TFTs while flat and strained.

due to the increasing mobility could not be measured, mainly because the external output load is constant during bending. Therefore, the changes in TFT conductivity are negligible for digital circuits with all TFTs in parallel.

Circuits with perpendicular strained load TFTs show an increase in the load resistance due to the smaller load TFT W/L ratio caused by capillary cracks. This results in a lowering of the output voltage levels and an increase in the rise time [14]. The output voltage swings in Figs. 8.8(a) and 8.9 are reduced by ≈0.3 V while strained (0.72 %). In particular, the high and low output voltages are reduced by ≈0.5 V and ≈0.2 V, and the rise times are increased by a factor > 2. The fall times remain unchanged since the characteristics of the driver TFTs stay unaffected (compare design rule 1). In addition, the increased maximum slope of the plotted analog inverter characteristic [Fig. 8.8(b)] shows that the voltage amplification of the inverter is increased while bent. Simultaneously, the average current consumptions of these inverter and NAND gates are reduced from 130 µA to 63 µA and from 67 µA to 25 µA while bent, due to the smaller W/L ratio of the load TFT, and also because the absolute reduction of the on-current of the driver TFTs is

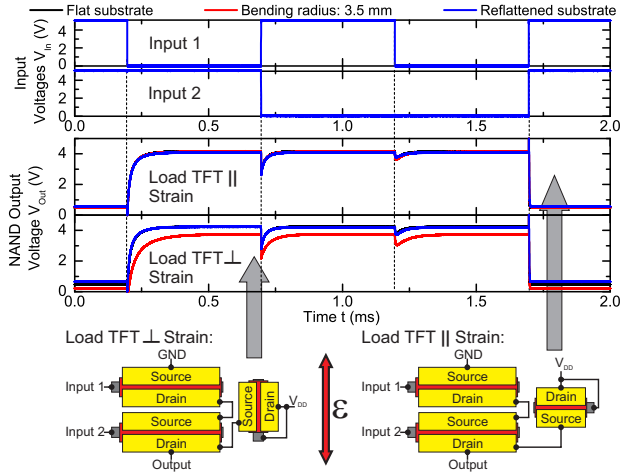

Figure 8.9: Input and output signals of exemplary NAND gates before bending, with strain applied parallel to the driver TFTs and hence perpendicular and parallel to the load TFTs, and reflattened.

larger than the increase in the off-current (Fig. 8.5). Reflattening the circuit restores the original W/L ratio and, hence, the original output signals. The evolution of the circuit high and low output voltage levels, as well as t_r and t_f with increasing strain and reflattened, is visualized in Fig. 8.10.

Aside from the digital inverter and NAND gates, we also measured the influence of bending on five-stage ring oscillators with parallel and perpendicular aligned load TFTs. Fig. 8.11 shows the output amplitude and frequency measured at different bending radii. Ring oscillator performances show a similar behavior as digital circuits, but additionally, the small mobility increase with increasing tensile strain has an influence. Due to the increasing mobility, the oscillator with parallel load TFTs shows an increase in the frequency from 22.9 kHz to 23.32 kHz (gate delay reduction from 4.4 µs to 4.3 µs) and a reduction in the amplitude from 2.04 V to 2 V while strained by 0.72 %. This observation is consistent with the results achieved by other groups [10] and Fig. 8.1. A more detailed analysis of the influence of strain on analog flexible circuits can be found, e.g., in [15].

The oscillator with perpendicular load TFTs changes the output

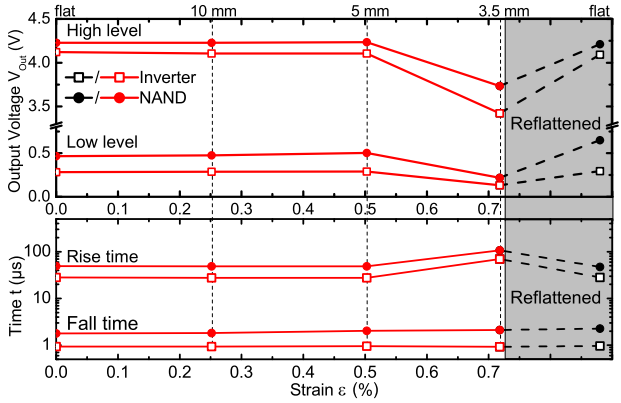

Figure 8.10: Output parameters of a NAND and an inverter gate before bending, with different strains applied parallel to the driver TFTs and perpendicular to the load TFTs, and reflattened.

amplitude, while strained to 0.72 %, from 2 V to 2.3 V and the frequency from 22.4 kHz to 16.4 kHz, corresponding to a gate delay of 4.5 µs and 6.1 µs, respectively. This is due to the increased amplification and, therefore, decreased bandwidth of the single inverters [compare Fig. 8.8(b)]. For smaller strain values (before the formation of capillary cracks), an increase in the frequency and a decrease in the amplitude, analog to the ring oscillator with parallel strained load TFTs, are visible.

To determine the influence of mechanical strain on a longer time scale and verify that bending does not influence the function of reflattened circuits, the substrate was bent and reflattened 20 000 times. This corresponds to more than two weeks of continuous bending by the used bending tester. The minimum bending radius was 4.5 mm. None of the tested inverters, NAND gates, or ring oscillators stopped working during this experiment. Fig. 8.12 shows the NAND parameters during this cycling experiment, which were measured at the flat substrate after different numbers of bending cycles. While the rise and fall times, as well as the low voltage levels of the output signal, are nearly constant, the high voltage level increased by ≈0.4 V, independently from the orientation of the load TFTs. Therefore, mainly the driver TFT off-current is modified. This is consistent with an obser-

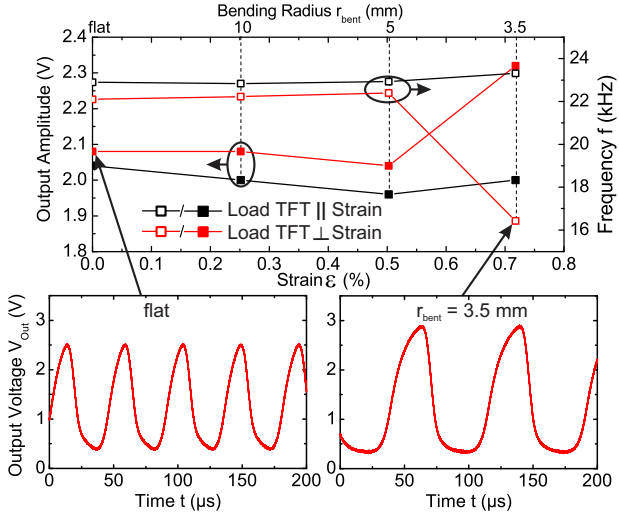

Figure 8.11: Amplitude and frequency of 5-stage ring oscillators before bending, and with strain applied parallel to the driver TFTs and hence perpendicular and parallel to the load TFTs.

vation we made in the past, i.e., that long-term cycling increases the threshold voltage by ≈100 mV [16]. Due to the small threshold voltage of the used a-IGZO TFTs, repeated bending mainly decreases the source drain current of our a-IGZO TFTs when V_{GS} ≈0 V (Fig. 8.3). As a result, the driver TFT conductivity is further decreased if the TFTs are turned off, and the high voltage output level increases.

8.6 Conclusion

Based on results obtained by bending single TFTs, we have derived three design rules for flexible NMOS a-IGZO logic gates. We have verified these design rules by fabricating and applying tensile strain to digital circuits and ring oscillators.

Our design rules enable the operation of the circuits up to applied strains of 0.72 %, corresponding to a minimal bending radius of 3.5 mm. Table 8.1 summarizes all results and shows that the achieved bending radius is, to our knowledge, significantly smaller than the bending

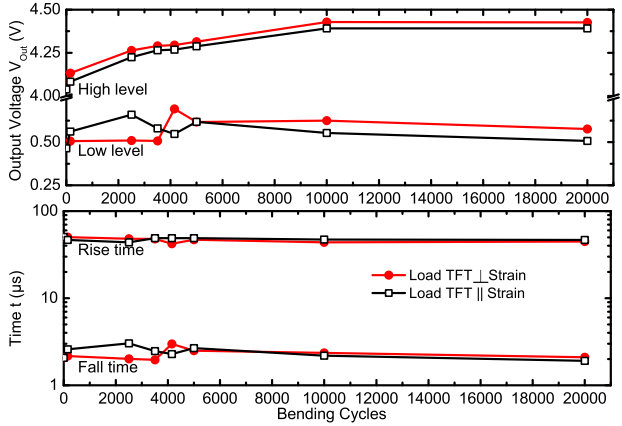

Figure 8.12: Output parameter of NAND gates with strain applied parallel to the driver TFTs and hence perpendicular and parallel to the load TFTs for different numbers of bending cycles.

radii achieved for inorganic circuits in other publications. To further decrease the influence of strain on circuits, one of the following would be necessary:

1. A reduction in the dimensions (especially the gate width and length) would reduce the probability for the formation of capillary cracks in the active region and therefore reduce the influence of strain.

2. The encapsulation of the substrate shifts the devices closer to the neutral stress plane, although it is difficult to place the TFTs exactly on the neural plane and avoid the problems of cracks completely [17].

3. In particular, the influence of the mobility change induced by strain in the elastic region, and not by capillary cracks, visible in circuits like the shown ring oscillators, and can be reduced by compensator circuits or a feedback [15]. This would require a more complicated electrical circuit design and potentially more transistors.

Furthermore, the circuits are still working after 20 000 repetitions of bending and reflattening. A flexible device with these specifications could be rolled up to a diameter of less than 1 cm 20 times a day and would still have an extrapolated lifetime of around three years.

Acknowledgment

This work has been scientifically evaluated by the Swiss National Scientific Foundation.

Table 8.1: Comparison of previously published flexible inorganic digital circuits. (*Calculated using the strain values given in [10])

	[5]	[7]	[8]	[10]	This Work
Channel material	Crystalline Si	Amorphous IGZO	Amorphous IGZO	Amorphous IGZO	Amorphous IGZO
Fabrication method	Thinned (20 µm) CMOS chip attached to Kapton foil	Fabricated on polyimide foil bonded to glass carrier (T_{MAX} =260 °C)	Fabricated on glass substrate (T_{MAX} =300 °C) and transferred to PET foil	Fabricated on stainless steel foil (T_{MAX} =300 °C)	Fabricated on free standing polyimide foil (T_{MAX} =150 °C)
Fabricated devices	Digital and mixed signal test circuits, 11-stage ring oscillator	Inverter, 5-stage ring oscillator	Two-clock shift register, 11-stage ring oscillator	7-stage ring oscillator	Inverters and NANDs with different geometrical alignments, 5-stage ring oscillators
V_{DD}	3.6 V	20 V	20 V	6 V - 26 V	5 V
Bending performance	Smallest bending radius: 20 mm	Smallest bending radius: 30 mm	No bending	Smallest bending radius: Single TFTs 4 mm Circuits: ≈10 mm*	Smallest bending radius: 3.5 mm Repeated bending cycles: 20000

Bibliography

[1] K. Cherenack, C. Zysset, T. Kinkeldei, N. Münzenrieder, and G. Tröster. Woven electronic fibers with sensing and display functions for smart textiles. *Advanced Materials*, 22(45):5178–5182, 2010.

[2] S.M. Venugopal and D.R. Allee. Integrated a-Si: H Source Drivers for 4" QVGA Electrophoretic Display on Flexible Stainless Steel Substrate. *Display Technology, Journal of*, 3(1):57–63, 2007.

[3] W. Li, H.E. Katz, A.J. Lovinger, and J.G. Laquindanum. Field-effect transistors based on thiophene hexamer analogues with diminished electron donor strength. *Chemistry of materials*, 11(2):458–465, 1999.

[4] K.H. Cherenack, A.Z. Kattamis, B. Hekmatshoar, J.C. Sturm, and S. Wagner. Amorphous-silicon thin-film transistors fabricated at 300 °C on a free-standing foil substrate of clear plastic. *Electron Device Letters, IEEE*, 28(11):1004–1006, 2007.

[5] H. Rempp, J. Burghartz, C. Harendt, N. Pricopi, M. Pritschow, C. Reuter, H. Richter, I. Schindler, and M. Zimmermann. Ultrathin chips on foil for flexible electronics. In *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pages 334–617. IEEE, 2008.

[6] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, 432(7016):488–492, 2004.

[7] H.-H. Hsieh, C.-H. Wu, C.-C. Wu, Y.-H. Yeh, H.-L. Tyan, and C.-M. Leu. Amorphous in2o3-ga2o3-zno thin film transistors and integrated circuits on flexible and colorless polyimide substrates. In *SID Symposium Digest of Technical Papers*, volume 39, pages 1207–1210. Wiley Online Library, 2008.

[8] M. Mativenga, M.H. Choi, J.W. Choi, and J. Jang. Transparent flexible circuits based on amorphous-indium-gallium-zinc-oxide thin-film transistors. *Electron Device Letters, IEEE*, 32(2):170–172, 2011.

[9] N. Münzenrieder, K.H. Cherenack, and G. Tröster. The effects of mechanical bending and illumination on the performance of flexible IGZO TFTs. *IEEE Transactions on Electron Devices*, (99):1–8, 2011.

[10] S.A. Khan, P.-C. Kuo, A. Jamshidi-Roudbari, and M. Hatalis. Effect of uniaxial tensile strain on electrical performance of amorphous igzo tfts and circuits on flexible metal foils. In *Device Research Conference (DRC), 2010*, pages 119–120. IEEE, 2010.

[11] S.M. Sze and K.K. Ng. *Physics of Semiconductor Devices*. John Wiley and Sons, 2007.

[12] H. Gleskova, S. Wagner, and Z. Suo. a-si: H thin film transistors after very high strain. *Journal of Non-Crystalline Solids*, 266:1320–1324, 2000.

[13] T.C. Reiley and W.D. Nix. The structure and mechanical properties of physically vapor deposited chromium. *Metallurgical Transactions A*, 7(11):1695–1701, 1976.

[14] R.C. Jaeger and T.N. Blalock. *Microelectronic circuit design*, volume 97. McGraw-Hill New York, 1997.

[15] C. Zysset, N.S. Münzenrieder, T. Kinkeldei, K.H. Cherenack, and G. Tröster. Indium-gallium-zinc-oxide based mechanically flexible transimpedance amplifier. *Electronics letters*, 47(12):691–692, 2011.

[16] N.S. Münzenrieder, K.H. Cherenack, and G. Tröster. Testing of flexible ingazno-based thin-film transistors under mechanical strain. *Eur. Phys. J. Appl. Phys*, 55(2):23, 2011.

[17] T. Kinkeldei, N. Münzenrieder, C. Zysset, K. Cherenack, and G. Tröster. Encapsulation for flexible electronic devices. *Electron Device Letters, IEEE*, 32(12):1743–1745, 2011.

9

Bendable digital circuits

Niko Münzenrieder, Christoph Zysset, Thomas Kinkeldei, Kunigunde Cherenack, Gerhard Tröster

A flexible InGaZnO based 1-bit SRAM under mechanical strain

Semiconductor Conference Dresden (SCD), pp. 1 - 4, 2011.
10.1109/SCD.2011.6068719

Abstract

Amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) is a promising material for the use in thin-film transistors (TFTs) and more complex electronic devices fabricated on flexible plastic substrates due to the low required deposition temperatures, and the high achievable electron mobilities. Here we show a mechanically flexible, fully integrated 1-bit SRAM composed of 6 a-IGZO TFTs fabricated on flexible polyimide foil that is operated with a supply voltage of 5 V, and for the first time electrically tested while bent to tensile radii of 10 mm and 5 mm. We observed circuit operation up to an input frequency of 10 kHz. The output signal of our 1-bit SRAM stays virtually unchanged even when the circuit is exposed to tensile mechanical strain of 0.52 %, induced by bending it to a radius of 5 mm.

9.1 Introduction

Mechanically flexible electronic devices fabricated on plastic foils, and not on rigid silicon wafers or glass plates, will enable a large number of new applications such as smart textiles [1] or flexible displays, manufactured with cheap roll-to-roll processes [2]. One key requirement for the production of such flexible structures is device fabrication at low temperatures (<300 °C) [3] because of the limited temperature resistance of the available plastic substrates. TFTs fabricated using oxide semiconductors such as amorphous indium-gallium-zinc-oxide (a-IGZO) as the channel material are attractive for flexible electronics because of their electron mobilities higher than $10\,cm^2V^{-1}s^{-1}$, which are achieved even when a-IGZO is deposited at room temperature [4]. One of the most important basic elements for all electronic circuits are thin-film transistors (TFTs). For digital applications it is necessary to perform logic operations and to store values in memory cells. Single flexible TFTs based on a-IGZO [4], ZnO [5], and other organic [6] and inorganic [3] materials have already been presented. At the same time there are only very few flexible, a-IGZO based, circuits. Inverters and ring oscillators fabricated on flexible substrates [7], and also a flexible shift register fabricated on a carrier substrate and transferred to a flexible plastic foil [8] have been published. The second technique has the disadvantage that it is not compatible with roll-to-roll fabrication methods. However while it has been shown that IGZO TFTs function under mechanical strain [5], the operation of a-IGZO circuits on a bent substrate have, to our knowledge, not yet been reported.

Here we present a fully integrated 1-bit SRAM composed of 6 a-IGZO TFTs fabricated on flexible plastic foil. We demonstrate the function of this device under mechanical strain induced by bending the circuit to a radius of 5 mm.

9.2 Device fabrication and evaluation

9.2.1 TFT fabrication

The device structure of our inverted staggered (bottom-gate, top-contact) thin-film transistors is show in Fig. 9.1. We used a flexible 50 μm-thick Kapton®E polyimide substrate from DuPont (surface area = 7.6 cm × 7.6 cm), that was cleaned by sonication in acetone and isopropanol for 5 minutes each, and was then pre-shrunk in a vacuum oven at 200 °C for 24 h to remove trapped residual solvents [9]. We deposited 50 nm of SiN_x on each side of the substrate using plasma enhanced chemical vapor deposition (PECVD) in an Oxford Instruments PECVD80+. We then deposited a 35 nm thick layer of Cr in a Plassys MEB550SL e^--beam evaporator, and structured it using standard photolithography (mask 1). Afterwards, the sample was treated in a UV ozone cleaning system for 60 min to clean the surface and prepare it for the following depositions. A Picosun Sunale R-150B was used to deposit 25 nm Al_2O_3, as a gate insulator, by atomic layer deposition (ALD) at 150 °C. Next, we deposited 15 nm of a-IGZO using room temperature RF magnetron sputtering in an Ar atmosphere and a ceramic $InGaZnO_4$ target. We patterned and etched the semiconductor by standard photolithography (mask 2) and diluted hydrochloric acid [10] ($HCl : H_2O = 1 : 120$). To remove the Al_2O_3 above the gate contact pads, we used photolithography mask 3 and AL-11 aluminium etchant from Cyantek heated to 50 °C [11]. Due to the limited resistivity of a-IGZO against chemical etchants we deposited the upper metal layer (source and drain contacts, interconnects) using a lift off process. Therefore we structured negative photoresist (mask 4) and evaporated 10 nm Ti and 60 nm Au with a second electron beam evaporation step. To increase the electrical stability of our devices, we finally deposited additional 25 nm of Al_2O_3 (ALD) [12], and opened contact holes (mask 5).

A typical transfer characteristic of one of our a-IGZO TFTs, measured with a HP4156A parameter analyzer, is shown in Fig. 9.2a. The width (W) and the length (L) of the active channel are 1400 μm, and

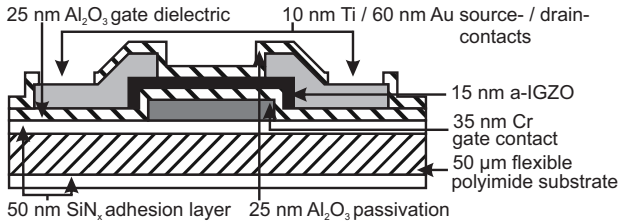

Figure 9.1: Schematic of our flexible bottom gate a-IGZO TFTs.

20 µm, respectively. The performance parameters for the shown characteristic are: saturation field effect mobility μ_{sat} =14.3 $cm^2V^{-1}s^{-1}$, linear field effect mobility μ_{lin} =14.4 $cm^2V^{-1}s^{-1}$, threshold voltage (V_{th}) =0.7 V, on/off ratio =3×10^8 and subthreshold swing (inverse of subthreshold slope) SS =0.15 V/decade, extrapolated using standard equations to model the transistor current [13]. The gate-source leakage current (I_{GS}) is always smaller than 10^{-7}mA. The output characteristic plot (Fig. 9.2b) shows a clear saturation behavior for high drain-source voltages (V_{DS}). For an applied gate-source voltage (V_{GS}) of 5 V the drain-source current (I_{DS}) is saturated above a drain source voltage of ≈5 V. The maximum measured I_{DS} value is ≈ 3.5 mA.

9.2.2 Circuit design

A schematic circuit diagram of the fabricated 1-bit SRAM is shown in Fig. 9.3. The 1-bit static memory cell consists of 6 n-channel enhancement TFTs forming two cross-coupled NAND gates. The circuit is designed to work with a supply voltage (V_{DD}) of 5 V. To simplify the whole structure we used TFTs with only two different W/L ratios: driver transistors (TFTs 3, 4, 5 and 6 in Fig. 9.3), and load TFTs, here both the drain and the gate contacts are connected with the power supply (TFTs 1 + 2 in Fig. 9.3). If a gate voltage is applied to the driver TFTs the voltage levels at the output pads should shift close to the ground level. Therefore the ratio between the conductivity of the driver and load TFT has to be lager then one. The W/L ratios have been chosen accordingly: W/L (driver): 1400 µm /20 µm, and W/L (load): 140 µm /20 µm. All active elements and interconnects are fully integrated on the same substrate.

The 'set' (S) and 'reset' (R) signals of this structure are active low.

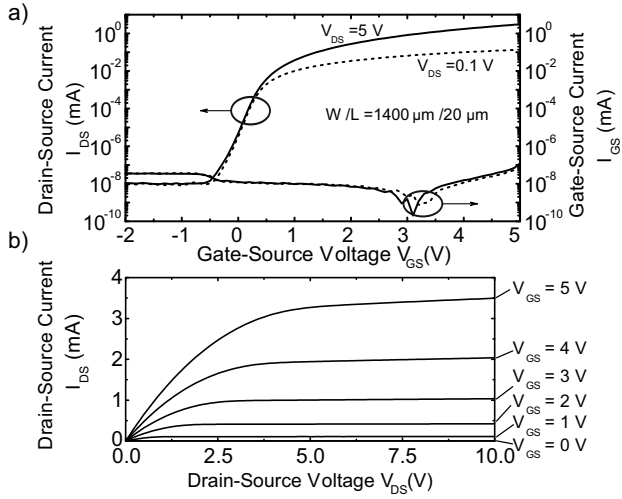

Figure 9.2: Transfer characteristic measured at source-drain voltages of 0.1 V (linear regime) and 5 V (saturation regime), and b) output characteristic of one of our a-IGZO TFTs.

Therefore the normal condition of these signals is 'on' (5 V). When a low signal pulse (0 V) is applied to the set contact a "1" (5 V) will be saved at the output pad. When a low signal pulse is applied to the reset contact this will set the output to a saved logic "0" (0 V). The undefined, and therefore forbidden input combination in this case is S = R = "0", while S = R = "1" does not change the stored value.

9.2.3 Measurement setup

To measure the performance of our flexible a-IGZO 1-bit SRAM we applied a supply voltage of 5 V to V_{DD}. Two HP 33120A waveform generators were used to create the input stimuli for our circuit. We applied a square wave input signal to S and R with a fill factor of 80 % at various frequencies that oscillated between 0 V and 5 V. A phase shift between these S and R signals ensured that the undefined input state S = R = "0" was not possible. To visualize the input and output signals of the tested circuit a multi channel digital Tektronix DPO 4034 phosphor oscilloscope was used to display all inputs and the produced output

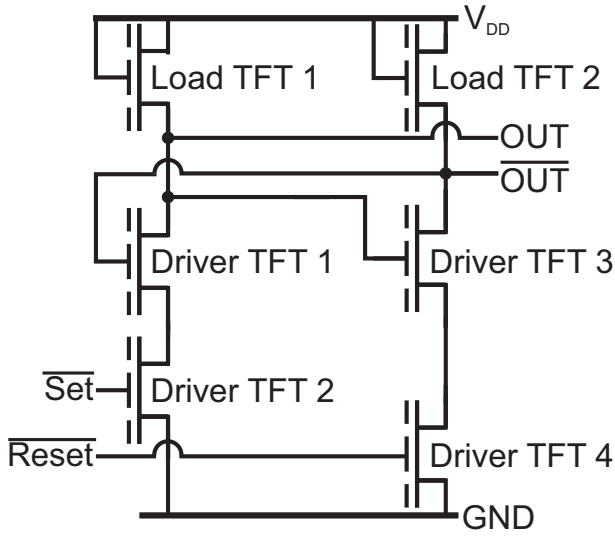

Figure 9.3: Circuit diagram of the fabricated 1-bit SRAM.

signal simultaneously. The complete schematic of the measurement setup is shown in Fig. 9.4a.

The characterization under mechanical strain was obtained by attaching circuits to double sided tape, and winding them around rods with different diameters. The electrical contacts to the bent circuit's contact pads where established using probe needles (as in the flat case). We always started with a flat circuit and decreased the bending radius stepwise. Fig. 9.4b shows a photograph of a curved substrate, with a contacted 1-bit SRAM bent to a tensile radius of 5 mm. We compared the performance of the flat device with that of the same device bent to a tensile radius of 10 mm, followed by bending to 5 mm.

9.3 Results

A micrograph of the fabricated flexible 1-bit SRAM is shown in Fig. 9.5. Output characteristics for operation frequencies between 100 Hz and 10 kHz are shown in Fig. 9.6. The circuit shows the expected output signal for a constant supply voltage of 5 V. A low voltage pulse at the S contact saves a digital '1' (3.8 V). When R is set to 0 V, the output signal

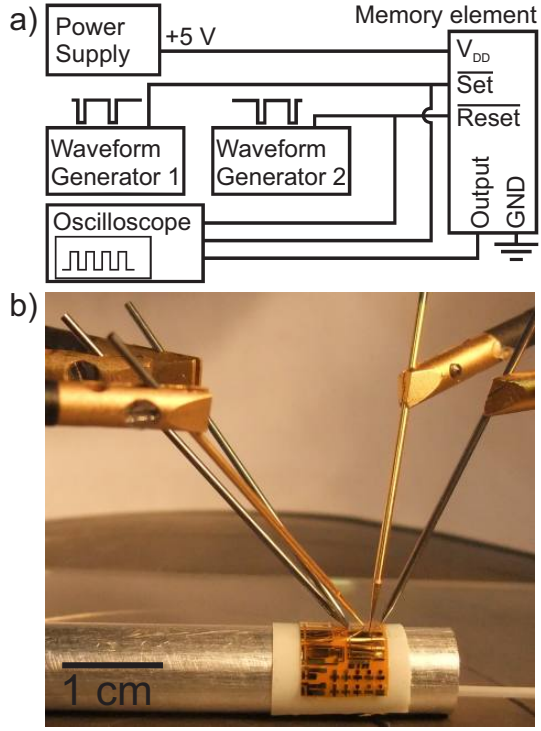

Figure 9.4: a) Schematic of the measurement setup. b) Picture of a contacted flexible 1-bit SRAM, bent around a rod with 5 mm radius.

Figure 9.5: Micrograph of the fabricated flexible 1-bit SRAM. The labeled brighter areas are the contact pads, where the Al_2O_3 passivation has been removed.

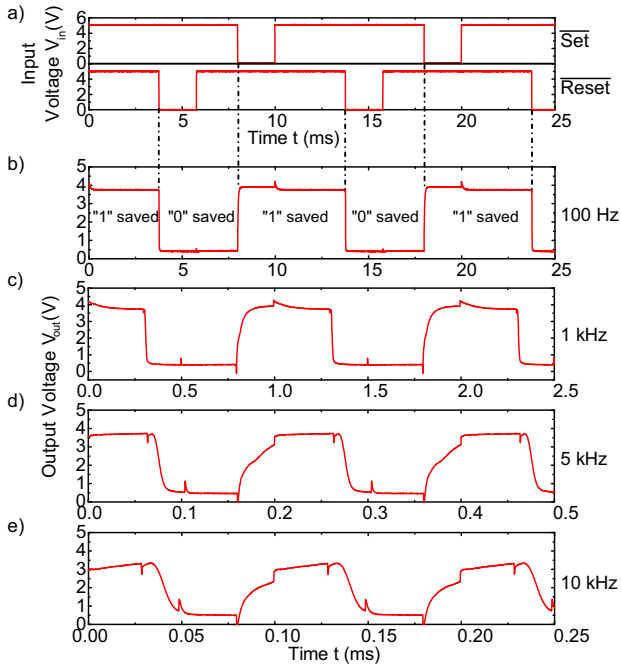

Figure 9.6: a) Input signals allpied to the set (S) and reset (R) contact, with a fill factor of 80 %, and a phase shift of ≈90°. b) - e) Output signals for different input signal frequencies of 0.1 kHz, 1 kHz, 5 kHz, and 10 kHz respectively.

changes to a save a value of 0.41 V (digital '0'). When a 'high' signal (5 V) is applied to R and S at the same time the actual output signal is saved. The output voltage levels differ from 0 V and 5 V because of transverse currents (Fig. 9.2a shows a source drain leakage current of ≈1 nA, for V_{GS} =0 V), induced by the exclusive use of n-type transistors. The average current consumption of the circuit is 192 µA (measured at an operation frequency of 1 kHz). The rise time t_r is 60 µs, while the fall time t_f is ≈13 µs. Here the rise time is defined as the time span required for the output signal amplitude to increase from 10 % of the maximum value to 90 % of the maximum value (exclusive of overshoot or undershoot). The fall time is the time needed to decrease the signal from 90 % to 10 %. The slopes of the rising and falling edges are independent

from the operation frequency. Therefore the maximum operation frequency is <16 kHz (at this frequency the output signal cannot reach the high voltage level anymore). The maximum frequency depends also on the phase shift between the input signals. Fig. 9.6e shows that the high voltage level of the output signal for an input signal frequency of 10 kHz is already decreased (compared to measurements at lower frequencies), due to the needed rise time.

9.3.1 Influence of bending

To evaluate the impact of mechanical strain on the performance of our flexible 1-bit SRAM, induced by bending, we also characterized circuit performance while bent to tensile radii of 5 mm and 10 mm. This corresponds to mechanical strain of 0 % (flat device), 0.27 % (10 mm bending radius), and 0.52 % (5 mm bending radius), calculated using the strain theory developed in [14], and using the layer thicknesses of the fabricated circuit. We always applied the strain parallel to the channel length, and therefore also parallel to the current flow through all TFTs. Fig. 9.7a shows the output signal of our 1-bit SRAM under mechanical strain. The circuits still works at the 5 mm bending radius. The input frequency for all shown measurements is 1 kHz. An enlargement of the rising edge is shown in Fig. 9.7b. While we measured that tensile bending to a radius of 5 mm decreases the threshold voltage of single a-IGZO TFTs by ≈0.125 V and increases the field effect mobilities by ≈10 %, bending of our flexible 1-bit SRAM has virtually no effect on the circuit performance. We think the reasons for the insensitivity of the 1-bit SRAM to mechanical strain are:

- The parallel alignment of all TFTs, and the uniform fabrication process ensures that bending affects all TFTs equally. Therefore the ratio between the conductivities of the load and driver TFTs is constant in a first order approximation, and the potential at the two output pads will not change.

- A more detailed consideration of the performance variation of a-IGZO TFTs under mechanical strain shows that the change of the source drain current is not independent of the gate voltage as a higher gate-source voltage induces a higher absolute current change. The effective gate-source voltages ($V_{GS,eff}$) of the TFTs 4 + 6 (Fig. 9.3) are 0 V or 5 V, while $V_{GS,eff}$ is smaller for TFT 3 + 5, and again smaller for TFT 1 + 2 (depending on the conductivity

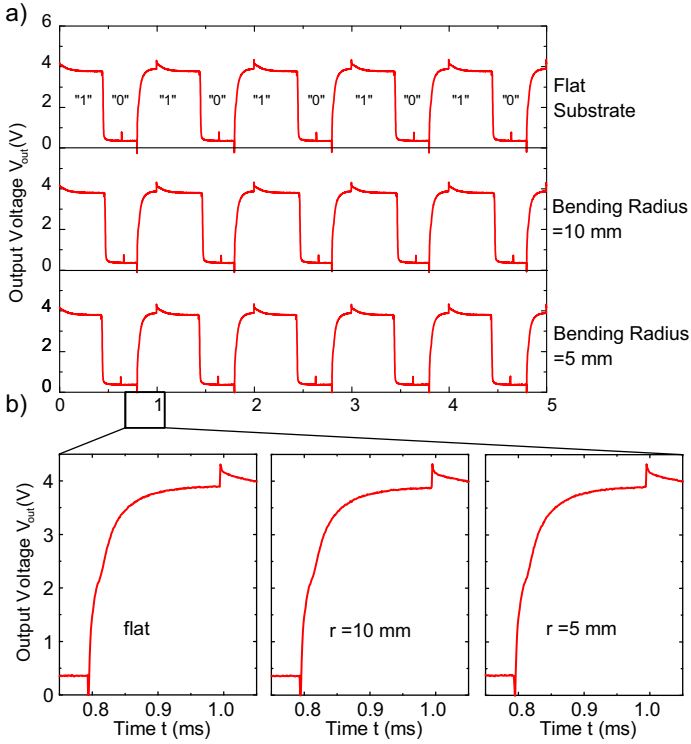

Figure 9.7: a) Output signal of the 1-bit SRAM while it is flatt, and bent to tensile radii of 10 mmm and 5 mm. The frequency of the input signals was 1 kHz. The small change in the duration of the "1" and "0" phases comes from a small variation of the phase-shift of the input signals during the measurment. b) Enlargement of the rising edges.

of the other transistors) [15]. This effect is compensated by the feedback loop, which decreases the gate voltage of the TFTs if V_{th} decreases and the mobility increase due to mechanical strain.

The 1-bit SRAM continues to work without any change in circuit performance when the substrate is reflattened after the bending test. On the other hand, if the device is bent to even smaller radii than 5 mm the circuit stops working even when the substrate is flattened again. This is because of the formation of micro cracks inside the brittle layers

of the device (Al_2O_3, SiN_x). These cracks also propagate though the metallic interconnect lines, and destroy the 1-bit SRAM.

9.4 Conclusion

A fully integrated 1-bit SRAM composed of 6 a-IGZO TFTs has been fabricated on a flexible polyimide substrate. This element is an essential basic module to build more complex logic circuits. The circuit continues working up to operation frequencies of 10 kHz. We also for the first time show the circuit performance of IGZO 1-bit SRAM bent to different tensile radii. The output signal of the complete circuit showed nearly no response to the applied mechanical strain even when bent to tensile strains of 0.52 %.

This is the first demonstration of a 1-bit SRAM under mechanical strain induced by bending. It represents an important step towards fully integrated flexible electronic circuits.

Bibliography

[1] K. Cherenack, C. Zysset, T. Kinkeldei, N. Münzenrieder, and G. Tröster. Woven electronic fibers with sensing and display functions for smart textiles. *Advanced Materials*, 22(45):5178–5182, 2010.

[2] R.F. Service. Patterning electronics on the cheap. *Science*, 278:383–384, 1997.

[3] K.H. Cherenack, A.Z. Kattamis, B. Hekmatshoar, J.C. Sturm, and S. Wagner. Amorphous-silicon thin-film transistors fabricated at 300 °C on a free-standing foil substrate of clear plastic. *Electron Device Letters, IEEE*, 28(11):1004–1006, 2007.

[4] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, 432(7016):488–492, 2004.

[5] K.H. Cherenack, N.S. Münzenrieder, and G. Tröster. Impact of mechanical bending on ZnO and IGZO thin-film transistors. *Electron Device Letters, IEEE*, 31(11):1254–1256, 2010.

[6] Q. Cao, Z.-T. Zhu, M.G. Lemaitre, M.-G. Xia, M. Shim, and J.A. Rogers. Transparent flexible organic thin-film transistors that use printed single-walled carbon nanotube electrodes. *Applied physics letters*, 88(11):113511–113511, 2006.

[7] T.C. Huang, K. Fukuda, C.M. Lo, Y.H. Yeh, T. Sekitani, T. Someya, and K.T. Cheng. Pseudo-CMOS: A novel design style for flexible electronics. In *Design, Automation & Test in Europe Conference & Exhibition, 2010*, pages 154–159. IEEE, 2010.

[8] M. Mativenga, M.H. Choi, J.W. Choi, and J. Jang. Transparent flexible circuits based on amorphous-indium-gallium-zinc-oxide thin-film transistors. *Electron Device Letters, IEEE*, 32(2):170–172, 2011.

[9] Kapton Polyimide Film. `http://www2.dupont.com/Kapton/en_US/`. [Online; accessed 20th of September 2010].

[10] J.B. Kim, C. Fuentes-Hernandez, W.J. Potscavage Jr, X.-H. Zhang, and B. Kippelen. Low-voltage ingazno thin-film transistors with alo gate insulator grown by atomic layer deposition. *Applied Physics Letters*, 94:142107, 2009.

[11] B. Zhou and W.F. Ramirez. Kinetics and modeling of wet etching of aluminum oxide by warm phosphoric acid. *Journal of The Electrochemical Society*, 143(2):619–623, 1996.

[12] I.-T. Cho, J.-M. Lee, J.-H. Lee, and H.-I. Kwon. Charge trapping and detrapping characteristics in amorphous ingazno tfts under static and dynamic stresses. *Semiconductor Science and Technology*, 24(1):015013, 2009.

[13] S.M. Sze and K.K. Ng. *Physics of Semiconductor Devices*. John Wiley and Sons, 2007.

[14] H. Gleskova, S. Wagner, and Z. Suo. a-si: H thin film transistors after very high strain. *Journal of Non-Crystalline Solids*, 266:1320–1324, 2000.

[15] S.A. Khan, P.-C. Kuo, A. Jamshidi-Roudbari, and M. Hatalis. Effect of uniaxial tensile strain on electrical performance of amorphous igzo tfts and circuits on flexible metal foils. In *Device Research Conference (DRC), 2010*, pages 119–120. IEEE, 2010.

10

Bendable analog circuits

Niko Münzenrieder, Luisa Petti, Christoph Zysset, Giovanni A. Salvatore, Thomas Kinkeldei, Charles Perumal, Corrado Carta, Frank Ellinger, Gerhard Tröster

Flexible a-IGZO TFT amplifier fabricated on a free standing polyimide foil operating at 1.2 MHz while bent to a radius of 5 mm

Electron Devices Meeting (IEDM), 2012 IEEE International , pp. 5.2.1–5.2.4, 2012.
10.1109/IEDM.2012.6478982

Abstract

We present flexible common source and cascode amplifiers fabricated on a free-standing plastic foil, using amorphous-Indium-Gallium-Zinc-Oxide (a-IGZO) TFTs with minimum channel lengths of 2.5 μm. Amplifiers are operated at a supply voltage V_{DD} of 5 V, and exhibit maximum cutoff frequencies f_C of 1.2 MHz. The circuits stay fully operational while bent to a tensile radius of 5 mm, and after 1000 cycles of repeated bending and re-flattening. To our knowledge, these are the fastest flexible oxide semiconductor based amplifiers.

10.1 Introduction

TFTs based on oxide semiconductors, especially amorphous-Indium-Gallium-Zinc-Oxide (a-IGZO) [1] are promising devices for electronics fabricated on flexible, but temperature sensitive plastic substrates, since they combine an electron mobility $>10\,cm^2V^{-1}s^{-1}$ and the possibility of low temperature deposition. This enables the fabrication of fast and bendable analog circuits, opening the way to new electronics applications, such as flexible radios and RFID tags. To date, the highest operation frequency of oxide semiconductor-based flexible (but unstrained) circuits is 2 MHz, which was demonstrated for a 15-stage ZnO ring oscillator fabricated on polyimide laminated to glass [2]. For flexible analog circuits, the best cutoff frequency f_C reported, to our knowledge, is 10 kHz, which was demonstrated for a strained transimpedance amplifier [3].

10.2 Fabrication

Flexible n-type a-IGZO TFTs have been fabricated on a free-standing 50 μm thick polyimide foil using a bottom-gate, passivated, inverted staggered TFT geometry. ALD deposited Al_2O_3 (thickness: 25 nm, dielectric constant: 9.5) served as gate oxide. Room temperature deposition of 15 nm thick a-IGZO was done in a RF magnetron sputtering process, using a pure Ar atmosphere and a ceramic $InGaZnO_4$ target. Fig. 10.1 shows the fabrication process flow and the device cross-section. The maximum process temperature was 150 °C. The manufacturing process was optimized concerning: device performance, low temperature fabrication, thicknesses of brittle materials, and adhesion

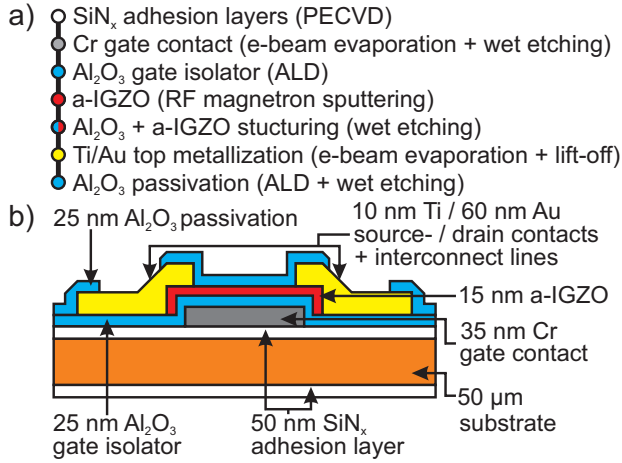

Figure 10.1: Fabrication process flow (a) and device cross-section (b) of flexible bottom-gate, passivated, inverted staggered a-IGZO based TFTs on free standing plastic foil.

between different material layers aiming at long term reliability and bendability.

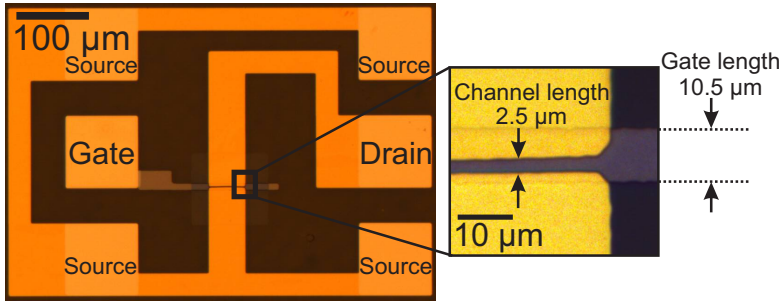

Figure 10.2: Micrograph of a flexible a-IGZO TFT with a channel length of 2.5 µm, a width of 50 µm, and a total gate overlap of 8 µm. The overlap is needed for reliable TFT operation across the whole 7.6 cm × 7.6 cm polyimide substrate.

The TFTs have been designed with Ground-Signal-Ground contact pads (pitch size: 150 μm), required for S-parameter measurements. For high operation frequency and transconductance, a channel length of 2.5 μm was chosen for all driver transistors presented in this paper. A total overlap of 8 μm between the gate and the source/drain contacts was selected to compensate for the temperature induced expansion of the flexible substrate during the fabrication process, and enable the alignment of different material layers using standard UV lithography. A micrograph of a fully processed flexible TFT is given in Fig. 10.2.

10.3 TFT characteristic

The I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics (Fig. 10.3) of a flexible a-IGZO TFT with a W/L ratio of 50 μm/2.5 μm (measured while the substrate was flat) exhibited a field effect mobility μ_{FE} of ≈14.5 $cm^2V^{-1}s^{-1}$, a threshold voltage V_{th} of 0.87 V, an on/off current ratio of 4×10^8, a subthreshold swing (inverse of subthreshold slope) SS of 170 mV/decade, and a transconductance g_m (at V_{GS} =3 V) of 208 μS. The gate capacitance C_G measurement of the same transistor (Fig. 10.4) shows a gate to source/drain overlap capacitance of ≈1.31 pF (negative bias voltage) and a total gate capacitance (V_{GS} =3 V) of 3.52 pF.

The bendability of the flexible a-IGZO TFTs was investigated by winding the substrate around a rod with 5 mm radius, which induced a tensile strain ϵ of ≈0.52 % [4] parallel to the TFT channel. The bent substrate was then contacted using standard probe tips. The resulting I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics for the same TFT as under flat conditions are also plotted in Fig. 10.3. Due to bending, a 70 mV higher V_{th} and a 0.2 $cm^2V^{-1}s^{-1}$ higher μ_{FE} were measured, causing a slightly reduced g_m (V_{GS} =3 V) of 204 μS. This is a result of the under tensile strain decreased resistivity of a-IGZO (increase of I_{DS} at V_{GS} <≈0.5 V) [5], and the under tensile strain increased resistance of the metallic interconnection lines (decrease of I_{DS} at V_{GS} >≈0.5 V), which becomes dominant for sufficiently small channel resistances at V_{GS} ≈0.5 V. The gate capacitance C_G of the flat and bent TFT is shown in Fig. 10.4. According to the under strain increased a-IGZO conductivity and the stretched gate area, bending increases C_G by ≈0.5 % to a value of ≈3.55 pF (V_{GS} =3 V).

The TFT AC behavior was characterized with a two-port network analyzer. Fig. 10.5 shows the measured S-parameters for a flexible a-IGZO TFT, while flat and bent to a tensile radius of 5 mm. S-parameters were used to calculate the current-gain h_{21} [6] of the flat and bent TFT

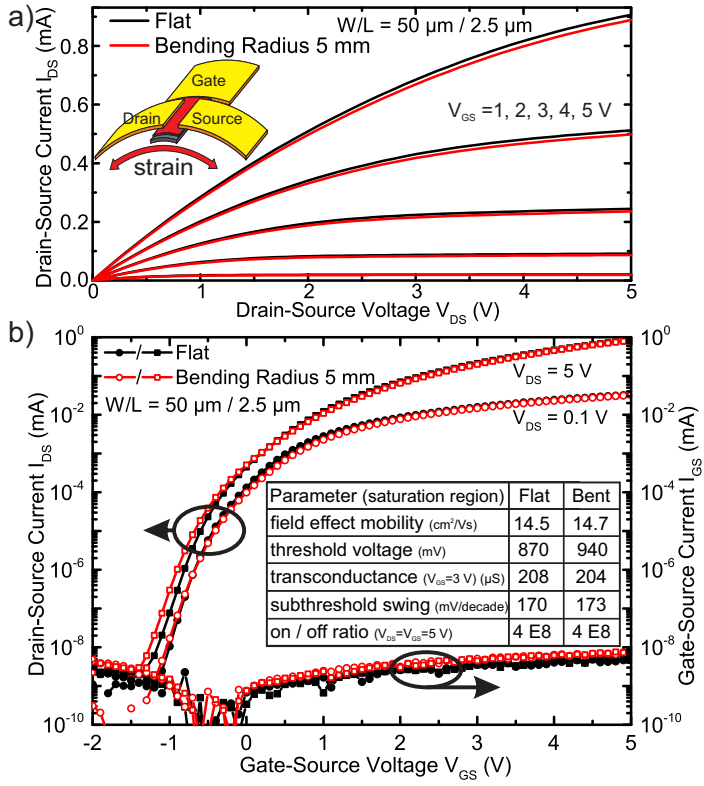

Figure 10.3: DC characteristic of a flexible a-IGZO TFT while flat, and bent to a tensile radius of 5 mm (strain ≈0.52 %) parallel to the TFT channel: a) Output characteristic, b) Transfer characteristic, and performance parameters (inset). Bending changes V_{th} by +70 mV, and μ_{FE} by +0.2 $cm^2V^{-1}s^{-1}$, leading to a 4 µS decreased g_m.

(Fig. 10.6). No significant variation in the AC behavior has been observed due to bending. For the flat and bent TFT, a transit frequency f_t of 10.7 MHz has been measured. This is in line with the value estimated from g_m and C_G; the expected strain induced decrease of f_t by ≈2 % is comprised within the observed measurement uncertainty.

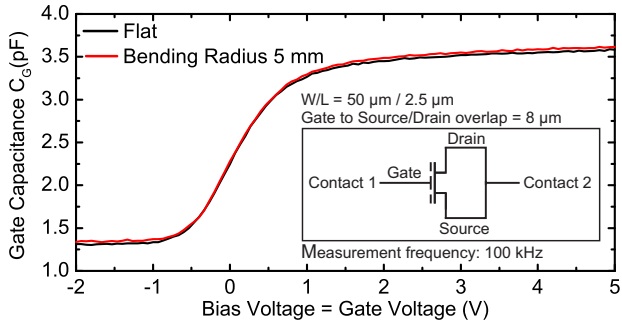

Figure 10.4: Gate capacitance C_G of a flexible a-IGZO TFT while flat, and bent to a tensile radius of 5 mm (source and drain connected). Bending increases C_G from ≈3.52 pF to ≈3.55 pF in the TFT on regime (V_{GS} =3 V), and from ≈1.31 pF to ≈1.34 pF in the TFT off regime. The measurement was performed at a frequency of 100 kHz.

10.4 Circuits

Simulations based on S-parameter measurements of single TFTs were used to design a common source and a cascode amplifier, both with an active TFT load. Schematic circuit diagrams and micrographs of the fabricated flexible a-IGZO amplifiers are shown in Fig. 10.7. Circuit interconnect lines were integrated into the top metallization layer. Both amplifiers are designed to work at a V_{DD} of 5 V. AC analysis was performed with an input signal peak-to-peak amplitude v_{AC} of 100 mV, and a total output load of R_L=1 MΩ and C_L <2 pF. The common source amplifier biased at an input voltage V_{DC} of 1.5 V, exhibited a gain G of 6.8 dB, and a f_C of 1.2 MHz (Fig. 10.8a), and a power consumption of 690 µW. In order to have a lower power consumption, the cascode amplifier was operated at V_{DC} =1.25 V, and at a cascode TFT bias voltage V_{BIAS} of 2.75 V. Here, a gain of 7.8 dB, an f_C of 840 kHz (Fig. 10.8b), and a power consumption of 395 µW were measured. Higher operating frequencies at the cost of higher power consumptions can be achieved by choosing different bias points.

Similar to single TFTs, the impact of mechanical strain on the flexible amplifiers was evaluated by bending the circuits to a tensile radius of 5 mm parallel to all TFT channels in the circuits; a bent and contacted circuit is shown in Fig. 10.9. The resulting Bode plots for the circuits

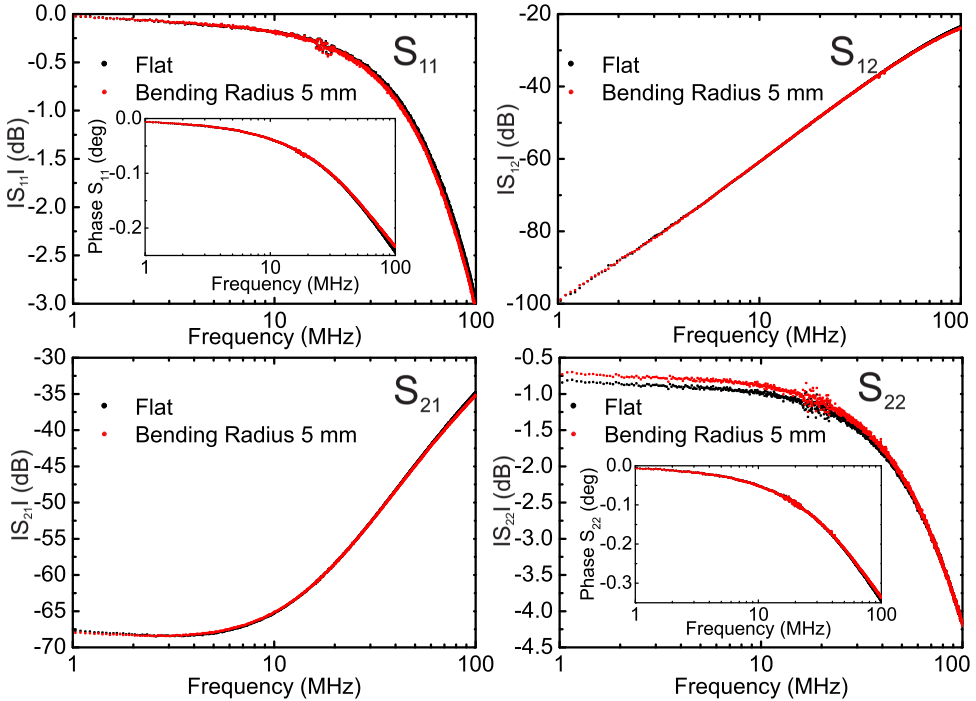

Figure 10.5: S-parameter measurement (after standard calibration procedure) of a flexible a-IGZO TFT (W/L =50 µm/2.5 µm) while flat, and bent to a tensile radius of 5 mm (v_{AC} = 100 mV, V_{DS} = 5 V, V_{GS} = 3 V). Port 1 and port 2 of the network analyzer were connected to the gate and drain contact, respectively (source contact is connected to ground). The measurement shows that the AC behavior is nearly unaffected by bending.

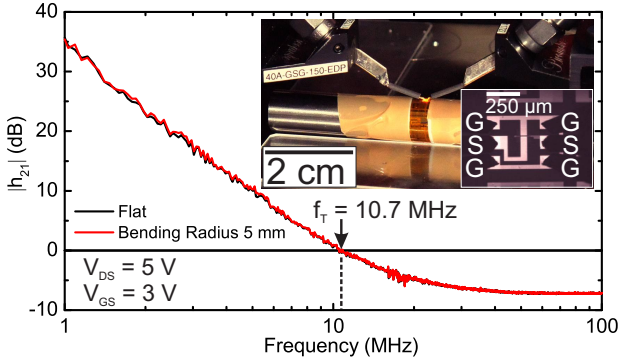

Figure 10.6: Absolute value of the current-gain h_{21} extracted from S-parameter measurements [6] of a flexible a-IGZO TFT (W/L =50 µm/2.5 µm) while flat, and bent to a tensile radius of 5 mm. The extrapolated f_t is 10.7 MHz for both measurements. The inset shows a flexible a-IGZO TFT contacted with two Ground-Signal-Ground (GSG) probe tips, and bent around a rod of 5 mm radius. The curved surface requires a vertical deformation of the GSG probe tips by ≈2.5 µm.

flat, bent, and re-flattened are shown in Fig. 10.10. Mainly because of the under strain nearly invariant transconductance ratio between the different TFTs in the circuits and the unaffected f_t, the measured variations for G and f_C (between flat and bent amplifiers) are less than 4 %, and 6 % for the common source and less than 7 % and 6 % for the cascode amplifier. Bending to radii <5 mm causes cracks in the TFT channel (Cr, Al_2O_3, a-IGZO layer stack) and permanently harms the amplifiers.

To emulate realistic application scenarios and to evaluate the influence of multiple bending, the flexible amplifiers were characterized before and after 1000 cycles of repeated bending (5 mm radius) and re-flattening, corresponding to 25 h of continuous bending with a custom build bending tester (inset of Fig. 10.11). After 1000 bending cycles, common source and cascode amplifiers stayed fully operational (Fig. 10.11).

Future TFTs with self-aligned source and drain contacts [7] will have channel lengths and gate overlaps ≤1 µm, thus enabling f_t >100 MHz, and further improving the circuit performance without

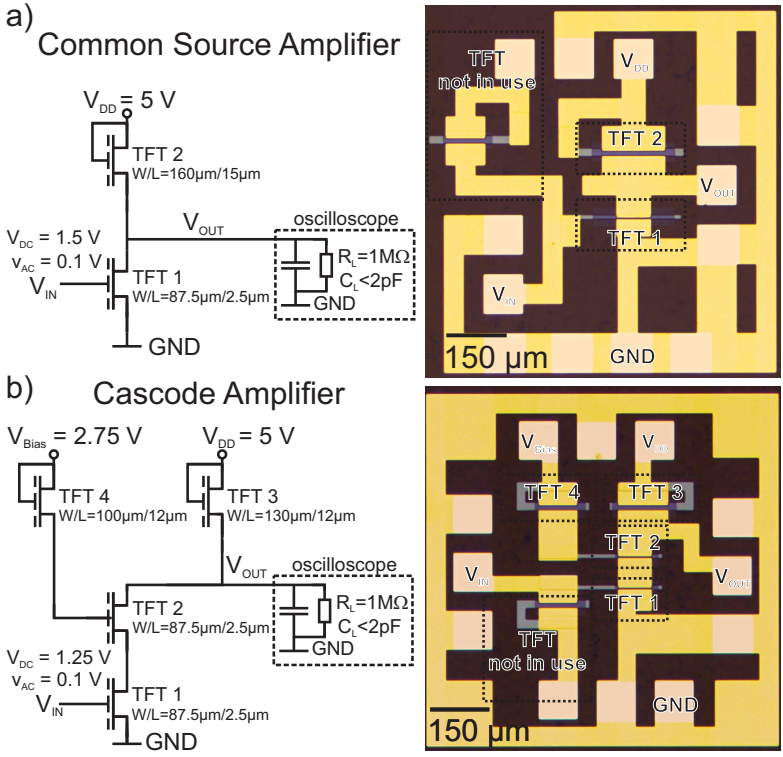

Figure 10.7: Circuit schematics and micrographs of the fabricated flexible amplifier circuits: a) Common source amplifier, b) Cascode amplifier. The additional TFTs to bias the inputs were not used. Each circuit occupies an area of ≈0.9 mm × 0.9 mm.

a loss of flexibility.

10.5 Conclusion

Mechanically flexible common source and cascode amplifier circuits based on a-IGZO TFTs were fabricated on a free-standing plastic foil using a-IGZO TFTs with minimal channel lengths of 2.5 µm. The circuits were supplied with V_{DD} =5 V. The amplifiers stayed fully operational while bent to a radius of 5 mm, and after 1000 cycles of repeated

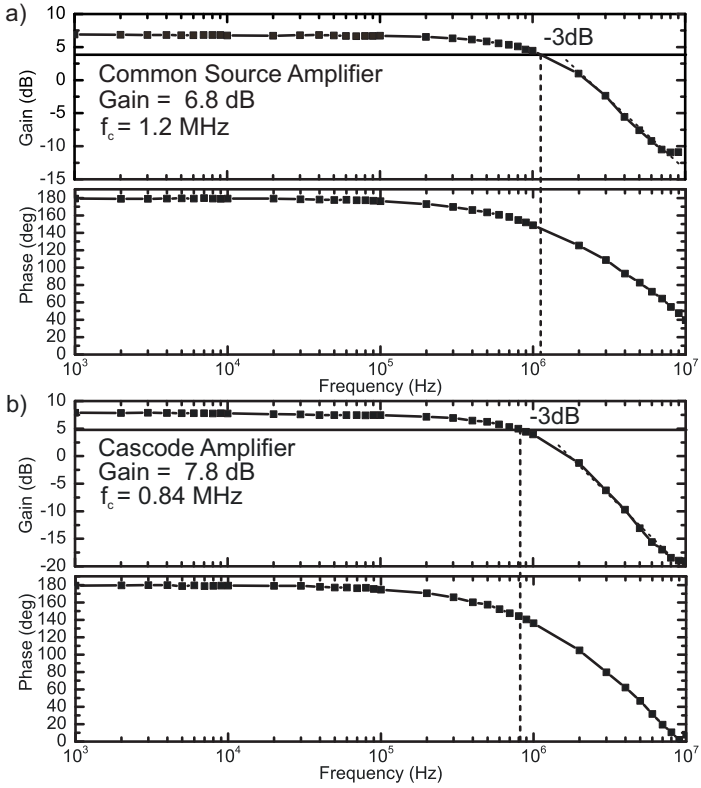

Figure 10.8: Bode plots of flexible amplifier circuits: a) Common source amplifier, b) Cascode amplifier. Measured GBWPs are 1.9 MHz (common source) and 1.5 MHz (cascode).

bending and re-flattening, showing cutoff frequencies of 1.2 MHz and gains of ≈7 dB. These results enable new electronic applications, like flexible AM-radios, ultra-sound devices, and LF-RFID tags.

Acknowledgment

This work has been partially supported by the European Commission through the FP7 Project: Flexible multifunctional bendable integrated light-weight ultra-thin systems (FLEXIBILITY), contract No:

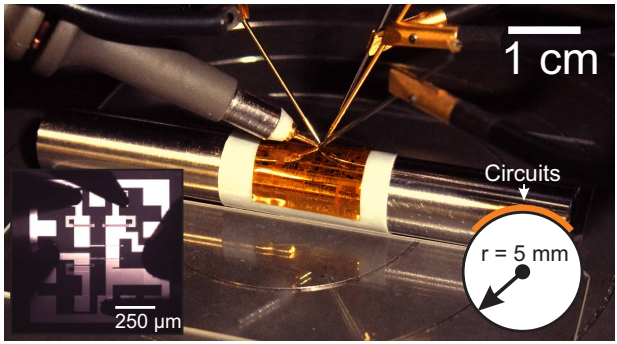

Figure 10.9: Photograph and micrograph (inset) of a contacted flexible cascode amplifier, bent around a rod of 5 mm radius.

FP7-287568. This work has also been scientifically evaluated by the Swiss National Scientific Foundation (SNSF), and financed by the Swiss Confederation and Nano-Tera.ch.

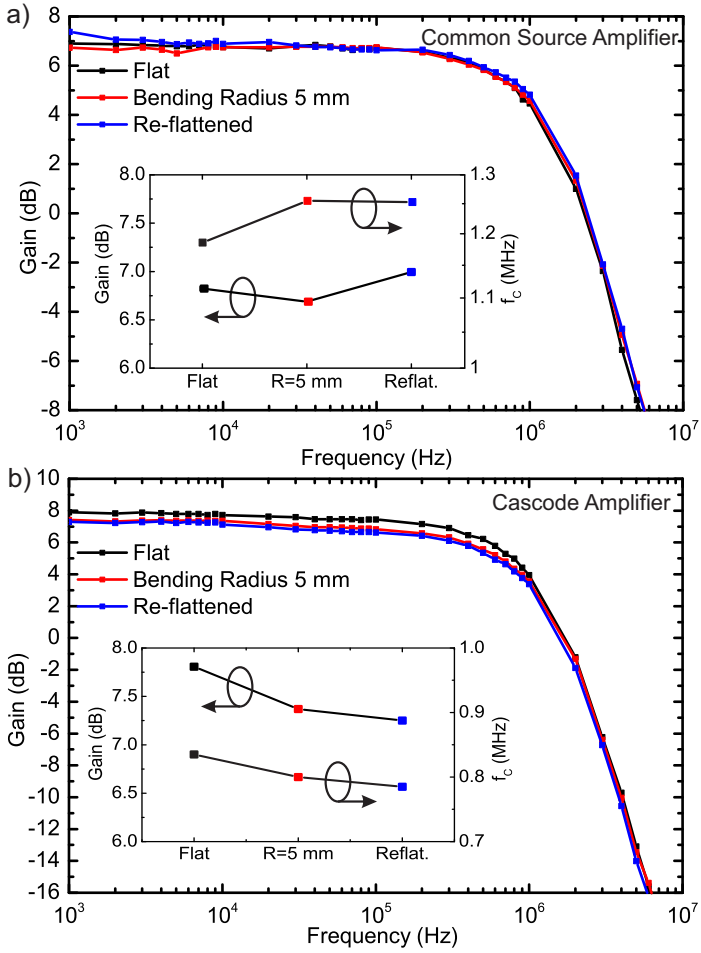

Figure 10.10: Bode plots of flexible amplifiers while the circuits are flat, bent around a rod of 5 mm radius, and re-flattened: a) Common source amplifier, b) Cascode amplifier. The insets show the evolution of gain and cutoff frequency. The amplifiers are fully operational when strained by 0.52 %.

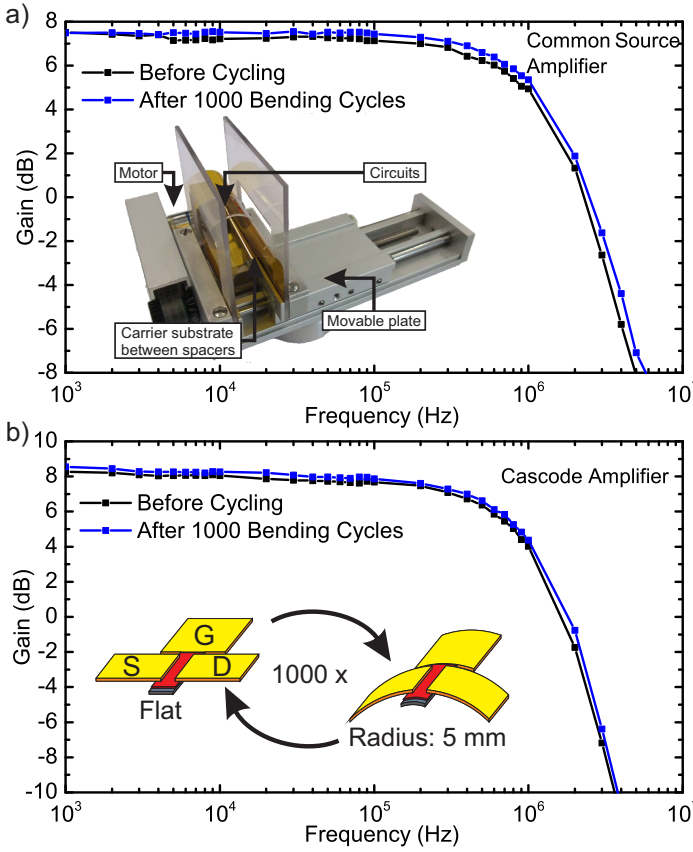

Figure 10.11: Bode plots of flexible amplifier circuits before cycling, and after 1000 cycles of repeated bending and re-flattening: a) Common source amplifier, b) Cascode amplifier. The inset in a) shows a photograph of the bending tester used for the cycling experiments. The amplifiers stayed fully operational after 1000 bending cycles (bending radius: 5 mm).

Bibliography

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, 432(7016):488–492, 2004.

[2] D. Zhao, D.A. Mourey, and T.N. Jackson. Fast flexible plastic substrate zno circuits. *Electron Device Letters, IEEE*, 31(4):323–325, 2010.

[3] C. Zysset, N.S. Münzenrieder, T. Kinkeldei, K.H. Cherenack, and G. Tröster. Indium-gallium-zinc-oxide based mechanically flexible transimpedance amplifier. *Electronics letters*, 47(12):691–692, 2011.

[4] H. Gleskova, S. Wagner, and Z. Suo. a-si: H thin film transistors after very high strain. *Journal of Non-Crystalline Solids*, 266:1320–1324, 2000.

[5] N. Münzenrieder, K.H. Cherenack, and G. Tröster. The effects of mechanical bending and illumination on the performance of flexible IGZO TFTs. *IEEE Transactions on Electron Devices*, (99):1–8, 2011.

[6] D. Lovelace, J. Costa, and N. Camilleri. Extracting small-signal model parameters of silicon mosfet transistors. In *Microwave Symposium Digest, 1994., IEEE MTT-S International*, pages 865–868. IEEE, 1994.

[7] D.H. Kang, I. Kang, S.H. Ryu, and J. Jang. Self-aligned coplanar a-igzo tfts and application to high-speed circuits. *Electron Device Letters, IEEE*, 32(10):1385–1387, 2011.

Glossary

Notation	Description	
ΔE	Energy Level Splitting	52, 131, 132
ΔL	Channel Length Variation	124
$\Delta L_{\parallel}$	Length Variation Parallel to Applied Strain	130
$\Delta L_{\perp}$	Length Variation Perpendicular to Applied Strain	130
$\Delta V_{th,\infty}$	Maximum Threshold Voltage Shift	136, 137
ΔV_{th}	Threshold Voltage Shift	52, 92, 94, 95, 130, 136
ϵ	Strain	ix, xi, 45, 46, 49, 52, 54, 55, 57, 64, 66, 68, 69, 124, 130, 132, 162–164, 170, 176, 178, 206
ϵ_R	Rupture Strain	59, 158, 163, 164
ϵ_{TH}	Threshold Strain (Strain value at which crack formation starts)	59, 162–164
ϵ_r	Dielectric Constant	6, 8, 38, 39, 64, 71, 85, 158
λ_{Max}	Maximum of the Radiation Emission Curve	134
μ	Carrier Mobility	132
μ_{FE}	Effective Field Effect Mobility. The effective field effect mobility is directly proportional to the drain-source current of a TFT. Therefore μ_{FE} also reflects changes of the contact resistance, the oxide capacitance, and the TFT channel geometry caused by strain or the formation of cracks	41, 52, 55, 57, 58, 101, 156, 162, 163, 206
μ_H	Hall Mobility	62, 63
$\mu_{lin,0}$	Initial Linear Electron Mobility	130

Notation	Description	
μ_{lin}	Linear Electron Mobility	39, 124, 130, 132, 134, 138, 172, 191
$\mu_{sat,0}$	Initial Saturation Electron Mobility	114, 130
μ_{sat}	Saturation Electron Mobility	39, 114, 116, 124, 130, 132, 134, 172, 191
ν	Poisson Ratio	130
ν_{ZnO}	Poisson Ratio of Zinc Oxide	130
ϕ	Work Function	160
ϕ_{Cr}	Work Function of Chromium	85
ϕ_{Cu}	Work Function of Copper	99
ϕ_{Ti}	Work Function of Titanium	85
σ_{TH}	Fiting Constant to Determine the Increase of the Threshold Voltage Shift during TFT Cycling	136, 137
A	Fitting Constant	136
a-Si:H	Amorphous Hydrogenated Silicon	3, 11, 84, 108, 170
AC	Alternating Current	x, 6, 39, 41, 45, 46, 69, 70, 206, 208
Al	Aluminium	85
Al_2O_3	Aluminum Oxide	8, 9, 38–40, 43, 46, 48, 54, 56, 59, 71, 75, 76, 85–87, 91, 92, 94, 101, 114, 123, 133, 146, 156–158, 163, 171, 174, 191, 194, 198, 204, 208
ALD	Atomic Layer Deposition	8, 38–40, 43, 71, 85, 146, 158, 191, 204
AM	Amplitude Modulation	69, 74, 211
Ar	Argon	62, 123, 191, 204
As	Arsenic	2
Au	Gold	39, 43–45, 59, 62, 63, 85, 99, 114, 123, 157, 158, 191
C	Carbon	2
C_G	TFT Gate Capacitance	40, 41, 88, 89, 98, 206

Notation	Description	
C_L	Load Capacitance	69, 208
C10-DNTT	2.9-Didecyldinaphtho[2.3-b:2.3-f]thieno[3.2-b]thiophene	7
CCD	Charge Coupled Device	50, 109, 160
CMOS	Complementary Metal–Oxide–Semiconductor	10, 74, 75, 185
Cr	Chromium	38, 43–45, 59, 73, 85–87, 94, 96, 99, 114, 123, 156–158, 160, 162–164, 171, 191, 208
Cu	Copper	ix, xii, 7, 9, 46, 50, 59, 73, 85, 99, 111, 124, 156–158, 160, 162–164
DC	Direct Current	ix, xi, 6, 10, 16, 39, 46, 62, 64, 70, 109, 147, 179, 206
DI	De-Ionized Water	114, 123
e^-	Electron	43, 56, 86, 114, 123, 158, 191
E_G	Energy Gap	132
E_{Str}	Gate-Bias Stress Field	92, 136
exp	Exponential Function	136
f_C	Cutoff Frequency	69, 204, 208
f_{in}	Input Frequency	178
f_t	Transit Frequency (unity gain frequency of the small-signal current gain h_{21})	41, 42, 49, 206, 208, 210
FIB	Focused Ion Beam	59, 76, 156–158, 165
G	Gain of Amplifer	69, 208
g_m	Transconductance (Transistor)	39, 41, 50, 85, 90, 172, 206
g_{ds}	Output Resistance (Transistor)	50

Notation	Description	
Ga	Gallium	2, 63, 86, 107, 123, 145, 156, 170, 191, 204
GBWP	Gain–Bandwidth Product	208
GSG	Ground-Signal-Ground	44–46, 206
h^+	Hole	56, 133
H_2O	Dihydrogen Monoxide	60, 86, 94, 147, 191
h_{21}	Current Gain	41, 45, 46, 206
HCl	Hydrochloride acide	86, 114, 123, 191
high-k	Material with High Dielectric Constant (Compared to SiO_2)	6, 8, 84, 156
I	Current	63, 64
I_{DS}	Drain-Source Current (Transistor)	39–41, 89–92, 124, 191, 206
I_{GS}	Gate-Source Current (Transistor)	92, 124, 174, 191
I_{off}	Off Current (Transistor)	62, 84, 146, 147, 149, 172
I_{on}	On Current (Transistor)	62, 84, 146, 147, 149, 172
IGZO	Indium-Gallium-Zinc-Oxide	ix–xii, 3, 7–12, 14–16, 38–47, 49, 50, 52, 54–60, 62–64, 66–76, 83–87, 89, 91, 92, 94, 95, 97–99, 101, 108, 114–116, 121–124, 127, 128, 130, 132–134, 136, 138, 146, 147, 155–158, 160, 163, 164, 169–174, 176–179, 182, 183, 185, 190–193, 197, 199, 203–206, 208, 211
In	Indium	63, 86, 107, 123, 145, 156, 170, 191, 204
ITO	Indium-Tin-Oxide	6, 46, 47, 49, 72

Notation	Description	
k·p	k·p Perturbation Theory	52, 115, 132
L	Transistor Channel Length	41, 49, 128, 163, 191
L_0	Initial Channel Length	124
$L_{\parallel}$	Length Parallel to Applied Strain	130
$L_{\perp}$	Length Perpendicular to Applied Strain	130
L_{OV}	Transistor Gate to Source/Drain Overlap Length	41
LF	Low-Frequency	69, 74, 211
m^*	Effective Mass of Charge Carriers	52, 115, 132
MoS_2	Molybdenum Disulfide	7
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor	87, 159, 172
n_e	Electron Concentration	63
n_p	Hole Concentration	62
Ni	Nickel	62
NiO	Nickeloxide	12, 62–64, 73
NMOS	n-channel MOSFET	66, 171, 176, 177, 183
O	Oxygen	7, 10, 63, 86, 107, 123, 145, 156, 170, 191, 204
O_2	Molecular Oxygen	62, 94
OTR	Oxygen Transmission Rate	94
p	Pressure	132
PECVD	Plasma-Enhanced Chemical Vapor Deposition	6, 38, 123, 191
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)	6
PEN	Polyethylene Naphthalate	5, 75
PET	Polyethylene Terephthalate	5, 75, 94, 185
pn	Positive Negative (Doping Profile	x, xii, 62–64, 73
Pt	Platinum	59, 156, 158, 160, 164

Notation	Description	
PVA	Polyvinyl Alcohol	60, 146, 147
R	Reset Signal	68, 192–194
r	Bending radius	45, 59, 157, 162
R_L	Load Resistance	69, 208
RF	Radio Frequency	8, 39, 43, 46, 63, 114, 158, 191
RFID	Radio-Frequency Identification	10, 69, 74, 204, 211
RH	Relative Humidity	178
RIE	Reactive Ion Etching	114
RS-232	Telecomunication Standard for Computer Serial Ports	109
S	Scattering parameters	45, 46, 205, 206, 208
S	Set Signal	68, 192–194
S_0	Initial Subthreshold Swing	130
SAM	Self-Assembled Monolayer	75
SEM	Scanning Electron Microscope	44, 54, 60, 149, 157, 158, 176
Si	Crystalline Silicon	2, 4, 8, 10, 60, 74, 146, 147, 149, 185
SiN_x	Silicon-Nitride	38, 43, 114, 123, 191, 198
SiO_x	Silicon-Oxide	9
Sn	Tin	10
SnO_2	Tin Dioxide	2
SRAM	Static Read Only Memory	x, xii, 16, 68, 189, 190, 192–194, 197–199
SS	Subthreshold Swing (Inverse of Subthreshold Slope)	39, 84, 91, 124, 130, 132, 134, 136–138, 172, 191, 206
t_f	Fall Time	68, 179, 180, 194
t_{GB-Str}	Gate-Bias Stress Time	92
t_{LT}	Long Term Stability Test Time	95
T_{MAX}	Maximum Process Temperature	75, 185
t_r	Rise Time	68, 179, 180, 194

Notation	Description	
t_{Str}	Stress Time (duration of the TFT cycling)	56–58, 136
TFT	Thin-Film Transistor	vi, ix, xi, xii, 2, 3, 5–16, 38–50, 52, 54–60, 62, 66–77, 83–92, 94–99, 101, 108–111, 114, 116, 121–124, 127, 128, 130, 132–134, 136–138, 145–147, 149, 155–158, 160, 162–164, 170–174, 176–185, 190–192, 197, 199, 203–208, 210, 211
Ti	Titanium	39, 43, 46, 59, 62–64, 85, 86, 99, 114, 123, 156–158, 160, 164, 191
TiO_x	Titanium-Oxide	9
UV	Ultraviolet	38, 43, 191, 205
V	Voltage	63, 64
v_{AC}	AC Voltage	69, 206, 208
V_{BIAS}	Bias Voltage	208
V_{DC}	DC Voltage	69, 208
V_{DD}	Supply Voltage	69, 178, 185, 192, 193, 204, 208, 211
V_{DS}	Drain-Source Voltage (Transistor)	39, 62, 91, 92, 124, 128, 146, 149, 160, 172, 191, 206
$V_{GS,eff}$	Effective Gate-Source Voltage (Transistor)	197
V_{GS}	Gate-Source Voltage (Transistor)	39–41, 62, 87, 90–92, 94, 95, 124, 146, 149, 160, 162, 174, 182, 191, 194, 206
v_{in}	AC Input Voltage Swing	178

Notation	Description	
V_{OB}	Over-Bias Voltage	87–90, 92, 101
$V_{th,0}$	Initial Threshold Voltage	114
$V_{th,eff}$	Effective Threshold Voltage	64
V_{th}	Threshold Voltage	39, 55, 57, 58, 84, 87, 91, 101, 114–116, 124, 130–132, 137, 138, 156, 160, 172, 191, 197, 206
W	Transistor Channel Width	191
W_D	Depletion Region Width	64
W/L	Width over Length Ratio (Transistor)	39, 41, 47, 52, 54, 66, 86–89, 91, 97–99, 123, 128, 160, 172, 174, 177, 180, 192, 206
WVTR	Water Vapor Transmission Rate	94
Y	Young's Modulus	132
Zn	Zinc	63, 86, 107, 123, 145, 156, 170, 191, 204
ZnO	Zinc-Oxide	7, 10, 12, 130, 190, 204

Curriculum Vitae

Personal information

Niko Stephan Münzenrieder

Born on June 17, 1983, in Neu-Ulm, Germany
Citizen of Germany

Education

2009 - 2013	PhD studies (Dr. sc. ETH) in Information Technology and Electrical Engineering, Swiss Federal Institute of Technology (ETH), Zürich, Switzerland.
2003 - 2008	Dipl.-Phys. Univ. in Physics, Technical University Munich (TUM), Germany.
1999 - 2002	Abitur, Technisches Gymnasium, Gewerbliche Schule Tübingen, Germany.

Work experience

2009 - 2013	Research assistant, Electronics Laboratory (IfE) ETH Zürich, Switzerland.
2007 - 2008	Student assistant, Walter Schottky Institute (WSI) Munich, Germany.