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Transient Fault Currents in HVDC VSC Networks During Pole-to-Ground Faults

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presented by

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Abstract

Multiterminal HVDC networks are a promising technology for future bulk power transmission. The protection of such a network, however, poses still a major challenge. In contrast to traditional point-to-point HVDC links, a real DC network requires HVDC circuit breakers at each end of a line to selectively isolate a fault and to keep other parts of the system operating. In order to specify the requirements of such HVDC circuit breakers, a full understanding of the transient fault currents and voltages is needed. This thesis provides a detailed analysis of the prospective transient fault currents and their influencing factors in a multiterminal HVDC grid. The effect of various network components on the transient fault current development is investigated, as well as the interaction between these components and the circuit breaker. The studies and analysis performed in the thesis have demonstrated that the fault currents are influenced by both, the network and circuit breaker parameters. The design of a circuit breaker, therefore, results in the trade-off between network and circuit breaker requirements.
Zusammenfassung

Acknowledgments

I would like to thank Prof. Christian Franck for the guidance of this thesis and the numerous valuable inputs. I would also like to express my thanks to my workmates, particularly to Michael, Martin, and Sedat, who shared the office with me.

And last but not least, I am very grateful to my girlfriend Gema. Without her incessant support, I would never have been able to complete this thesis.

The research project of this thesis was financially supported by ABB, Alstom Grid, Siemens, and the Swiss Federal Office of Energy (BfE).
List of Publications

Several journal and conference contributions emerged from the research in this thesis, partly in cooperation with Roger Wiget, Göran Andersson, Martin Pfeiffer, Michael M. Walter, and the study group of DKE.

Publication [1] is a summary of the pre-standardization work by the European HVDC Study Group founded on an initiative by the German Commission for Electrical, Electronic, and Information Technology (DKE). The results of this thesis contributed to the chapter on DC short-circuit faults.

The results of the master’s thesis written by Martin Pfeiffer in the framework of the thesis at hand are the basis for [6] and, partly for [9].

Publication [7] emerged from the research cooperation with the Power System Laboratory at ETH Zurich, where Roger Wiget and Göran Andersson contributed the part on steady-state load flow simulations.

The simulations in [9] were conducted by Martin Pfeiffer and the part on HVDC CBs was contributed by Michael M. Walter.


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List of Acronyms and Symbols

Acronyms

ANPC  Active Neutral Point Diode Clamped
A-RCB  Active Resonance Circuit Breaker
CB  Circuit Breaker
CCC  Capacitor-Commutated Converter
CSC  Current Source Converter
CZ  Current Zero Crossing
EMTDC  Electromagnetic Transients including DC
EMTP  Electromagnetic Transients Program
ER  Earth Return
FC  Flying Capacitor
FCL  Fault Current Limiter
GCT  Gate-Commutate Thyristor
GTO  Gate Turn-Off Thyristor
HCB  Hybrid Circuit Breaker
HLAC  High Impedance AC Side Grounding
HLGND  High Impedance Grounding
HRB  High Ohmic Busbar Grounding
HTS  High Temperature Superconductor
HVAC  High Voltage Alternating Current
HVDC  High Voltage Direct Current
IGBT  Insulated Gate Bipolar Transistor
LCC  Line Commutated Converter
LRGND  Low Impedance Grounding
MMC  Modular Multilevel Converter
MOA  Metal Oxide Arrester
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<td>MR</td>
<td>Metallic Return</td>
</tr>
<tr>
<td>MRTB</td>
<td>Metallic Return Transfer Breaker</td>
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<tr>
<td>MTDC</td>
<td>Multiterminal HVDC</td>
</tr>
<tr>
<td>MTMV</td>
<td>Multi-Terminal Multi-Vendor</td>
</tr>
<tr>
<td>MV</td>
<td>Medium Voltage</td>
</tr>
<tr>
<td>NGO</td>
<td>Non-Governmental Organization</td>
</tr>
<tr>
<td>NIS</td>
<td>Numerical Integration Substitution</td>
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<tr>
<td>NPC</td>
<td>Neutral Point Diode Clamped</td>
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<tr>
<td>ODE</td>
<td>Ordinary Differential Equation</td>
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<tr>
<td>OHL</td>
<td>Overhead Line</td>
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<tr>
<td>OPF</td>
<td>Optimal Power Flow</td>
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<tr>
<td>PCC</td>
<td>Point of Common Coupling</td>
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<td>PDE</td>
<td>Partial Differential Equation</td>
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<tr>
<td>P-RCB</td>
<td>Passive Resonance Circuit Breaker</td>
</tr>
<tr>
<td>PSCAD</td>
<td>Power Systems Computer Aided Design</td>
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<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
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<tr>
<td>RMS</td>
<td>Root Mean Square</td>
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<tr>
<td>SCB</td>
<td>Solid-State Circuit Breaker</td>
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<tr>
<td>SCFCL</td>
<td>Superconductive Fault Current Limiter</td>
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<tr>
<td>SCR</td>
<td>Short Circuit Power Ratio</td>
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<tr>
<td>TRV</td>
<td>Transient Recovery Voltage</td>
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<tr>
<td>UFS</td>
<td>Ultra Fast Switch</td>
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<tr>
<td>VSC</td>
<td>Voltage Source Converter</td>
</tr>
<tr>
<td>WF</td>
<td>Wind Farm</td>
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<tr>
<td>XLPE</td>
<td>Cross-Linked Polyethylene</td>
</tr>
<tr>
<td>ZIR</td>
<td>Zero Input Response</td>
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<td>ZSR</td>
<td>Zero State Response</td>
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Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
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<tbody>
<tr>
<td>(·)−</td>
<td>Backward Traveling Wave Quantity</td>
</tr>
<tr>
<td>(·)⁺</td>
<td>Forward Traveling Wave Quantity</td>
</tr>
<tr>
<td>(·)ᵣ</td>
<td>Receiving End Quantity</td>
</tr>
</tbody>
</table>
(·)ₚ Sending End Quantity
* Convolution Operator
α Inductive Damping Factor
β Capacitive Damping Factor
Δt Simulation Time Step
ΔTₜₐₜₑᶜᵗₜ Detection Delay
ΔTₙₒₙ𝑧ˡ e Nozzle Opening Delay
ΔTₜₒₜₜₑⁿｇ-opening CB Contact Separation Delay
δ(t) Dirac Impulse Function
Γ Reflection Coefficient
λ Eigenvalue
Λ Eigenvalue Matrix
ω Angular Frequency
φ Phase Angle
σ(t) Unit Step Function
τ Traveling Delay of Wave
τₐᵩₑ Arc Time Constant
a Arc Cooling Function Exponent
b Arc Time Constant Function Exponent
c Wave Propagation Speed
C₉ Cap DC Capacitor
Cₐ Cap Resonance Circuit Capacitor
Cₛ Snubber Capacitor
Eₐrc Arc Voltage Gradient
f Frequency
g Arc Conductance
iₐc AC Infeed Current
iₐrc Instantaneous Arc Current
iₖ DC Capacitor Current
iₖCB CB Current
i₇ Adjacent Feeder Current
k(ω) Wave Propagation Function/Constant
K Skin Effect Factor
l Line Length
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<tbody>
<tr>
<td>$l_{arc}$</td>
<td>Arc Length</td>
</tr>
<tr>
<td>$L_{ac}$</td>
<td>AC Inductance</td>
</tr>
<tr>
<td>$L_{dc}$</td>
<td>DC Side Inductance</td>
</tr>
<tr>
<td>$L_{pole}/L_{line}$</td>
<td>DC Pole/Line Reactor</td>
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<tr>
<td>$L_{res}$</td>
<td>Resonance Circuit Inductance</td>
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<tr>
<td>$L_{s}$</td>
<td>AC Phase Reactor</td>
</tr>
<tr>
<td>$L_t$</td>
<td>Transformer Reactance</td>
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<tr>
<td>$r_{arc}$</td>
<td>Arc Resistance</td>
</tr>
<tr>
<td>$R_{ac}$</td>
<td>AC Resistance</td>
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<tr>
<td>$R_{dc}$</td>
<td>DC Resistance</td>
</tr>
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<td>$R_f$</td>
<td>Fault Resistance</td>
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<tr>
<td>$R_{res}$</td>
<td>Resonance Circuit Resistance</td>
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<tr>
<td>$R_s$</td>
<td>Snubber Resistor</td>
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<tr>
<td>$T$</td>
<td>Transmission Coefficient</td>
</tr>
<tr>
<td>$u(t)$</td>
<td>Input Function</td>
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<tr>
<td>$V_{ac}$</td>
<td>AC Voltage</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>DC Voltage</td>
</tr>
<tr>
<td>$W$</td>
<td>Eigenvector Matrix</td>
</tr>
<tr>
<td>$Z_0(\omega)/R_0$</td>
<td>Characteristic Line Impedance</td>
</tr>
</tbody>
</table>
1 Introduction

Multiterminal High Voltage DC (HVDC) networks are widely recognized as a key component in the future power network, which will have to cope with an increasing electricity demand and high penetration of new renewable energy sources. Several initiatives from the academic community, industry consortia, and environmental NGOs \cite{vG10, JvL+11, Des09, Fri12, Atl12, Off11, Gre08} envision the creation of interconnected HVDC networks with the expected benefits of higher redundancy, increased flexibility for power trading, and reduced investment and operational costs. As the renewable energy sources are often far away from the load centers, the transmission distances become longer and cannot be realized in a technically and economically reasonable way based on HVAC technology \cite{NTA06}, particularly, in case of offshore connections with cables.

More than hundred point-to-point HVDC connections are in operation today, but only five multiterminal HVDC (MTDC) networks have been realized so far. There are three older Current Source Converter (CSC) based networks, such as the tapped ”Sardinia, Corsica, Italy (SACOI)-link” with three terminals \cite{BTAM89}, the four-terminal ”Nelson River” \cite{LRM+90} project, and the five-terminal ”Hydro-Québec/New England” system \cite{MMP+94}. Two new MTDC networks based on Voltage Source Converters (VSC) were commissioned in China recently, the three-terminal ”Nan’ao Island” network in 2013 \cite{ZRL+14} and the five-terminal ”Zhoushan Island” network in 2014 \cite{THP14}.

Some early publications on transients in CSC based MTDC networks from the 70s and 80s can be found. They are mainly based on operation experience with small DC grids like the ”Nelson River”
project [LRM\textsuperscript{+}90] and the tapped SACOI link [LRM\textsuperscript{+}90, BTAM89]. None of these systems is, however, a real DC grid. The Nelson River project consists of a double bipole HVDC link that can be paralleled and deparalleled with fixed power flow directions and two terminals at each end of the connection. The operation of the Sardinia-Italy link with a small tap in Corsica cannot be compared to the operation of a real MTDC neither. General aspects concerning transients due to faults in a 3-terminal DC network based on CSCs are discussed in [Dou70, SG86]. A newer study on fault clearing in a meshed four-terminal CSC-MTDC grid can be found in [Cig97].

The development towards new multiterminal HVDC systems will be modular, e.g. in steps. The system development has begun with point-to-point connections and continues through simple, radial, multiterminal systems. Such smaller systems will gradually be interconnected into larger radial and meshed HVDC systems comprising more DC terminals and HVDC links. Understanding, specification and standardization of design and operation principles of HVDC grids are seen as the first necessary steps towards such multi-terminal, multi-vendor (MTMV) systems [ACF\textsuperscript{+}14].

These new MTDC networks will be based on VSCs rather than on the older CSC technology due the VSC’s independent active and reactive power controllability, fast power reversal without mechanical switches, and the possibility to be connected to weak AC nodes [ALWM09]. Recent advances such as higher ratings of the semiconductor devices and the development of low-loss converter topologies make the multiterminal VSC-HVDC network a viable option. Its protection in case of a fault is, however, more demanding than in CSC-MTDC networks and still a major obstacle in the realization of a VSC-MTDC grid. While AC side circuit breakers (CBs) can adequately protect point-to-point HVDC connections, an interconnected HVDC network requires DC CBs to selectively isolate a faulty cable, which cannot be realized by AC side CBs due to the forced de-energization of the entire system [TO07, LRM\textsuperscript{+}85].

To specify the requirements of such DC CBs and possible fault
clearance support options, full understanding of the transient behavior of current and voltage and their influencing parameters is required. Nowadays, a lot of research is done in the area of VSC-MTDC networks and complex systems can be simulated with modern Electromagnetic Transients Program (EMTP) software. Most of the published work on transients-related issues in MTDC networks covers protection \cite{Twe12,DSR+11,CP11,VGC+11,TO07}, converter control during faults \cite{LO03,LJA04}, and transient stability \cite{CMCJ11,MMD10}.

The transient stability and control studies include simulations of transient fault currents, but on a large time scale of milliseconds to a few seconds and the simulations are usually based on simplified models for the DC lines with cascaded pi-sections. For the analysis of the fundamental fault current behavior, simulations in the range of microseconds to milliseconds have to be performed and more accurate line models are required to represent the exact waveform of the fault surges.

The publications by \cite{DSR+11,TO07} on protection strategies are based on more accurate simulations, but their main focus is on validating the protection algorithm rather than analyzing the fault currents fundamental influencing factors.

Detailed simulations of transient overvoltages during cable faults, loss of a converter, and converter AC faults are presented in \cite{GZH13}. This study lacks, however, parameter variations for the analysis of the influencing factors and their identification.

The DC fault analysis in \cite{YFO10} identifies three different time periods of a pole-to-pole fault development and presents the corresponding calculations for currents and voltages. The first period is the DC capacitor discharging phase, followed by a diode freewheeling phase, and a grid-side current feeding phase. During a pole-to-ground fault, a transient and a steady-state period are distinguished. Moreover, the influence of the fault resistance is discussed.

Publication \cite{RXM12} identifies four different stages during a pole-to-pole fault: a capacitor discharge, an AC feeding overcurrent, a
capacitor recharging, and an AC side isolation stage. Calculations are presented for the capacitor recharging stage and also pole-to-ground fault are analyzed.

Both of the aforementioned publications [YFO10, RXM12] are, however, limited to point-to-point links and the simulations and calculations are based on rudimentary line models. Moreover, both studies assume a grounding scheme that is not viable for a HVDC system connected to the AC transmission system.

The different fault current feeding sources are identified in [WB12, WJB13] and analytic expressions are derived for the individual contributions, but only the influence of the fault location is analyzed. Moreover, the mathematical description of the frequency-dependence of the line parameters and the skin-effect is missing and the proposed expressions can only be applied to radial networks without multiple feeders per busbar.

The literature review has shown the lack of deeper understanding of the fundamental development of transient overcurrents and overvoltages and their influencing factors in a MTDC network. Methods for the simulation of transients exist for the AC transmission, but only a few approaches could be found for a MTDC grid, which are mostly based on very simple models. The amplitude of overcurrents and overvoltages shall be quantified for different fault scenarios and the influence of each element of a MTDC network on the transient behavior investigated.

Therefore, this thesis presents the analysis based on the breakdown of the prospective fault current into its individual contributions from the different network components. The simulation models for the network components are presented in Chapter 4. The fault feeding sources are identified and analyzed in Chapter 5 using transient simulations. Calculations are derived in Chapter 6 to represent their contributions analytically.

Chapter 7 analyzes the influence of the network topology and Chapter 8 the effect of the grounding scheme.

Chapter 9 investigates the possible fault clearing options and
Chapter 10 presents the simulation study on HVDC CBs and their interaction with the other network components.

The conclusions of the thesis and the outlook are presented in Chapter 11.
2 Aim of This Work

The aim of this thesis is to contribute to a deeper understanding of transient fault currents and their influencing factors in multiterminal HVDC networks in order to derive requirement specifications for the network components, mainly the HVDC CB.

The influence of the components’ main parameters on the transient fault current development during pole-to-ground faults shall be investigated, as well as the interaction between these components and the CB, by means of simulations.

To achieve these goals, the following steps shall be taken:

- Derive and implement methods and models for all components in a MTDC network in order to simulate the transient voltage and current development during a pole-to-ground fault.
- Identify and analyze the fault current feeding sources.
- Identify and quantify the major fault current influencing factors, i.e. transmission technology, network topology, and network grounding schemes.
- Derive analytic expressions to calculate the rate-of-rise and amplitude of the component’s most demanding peaks in the transient fault current. This shall serve as a first proposal for pre-standardization efforts.
- Compare different HVDC CB technologies with respect to fault clearing capacity and interruption times, in particular with respect to network voltage stability.
As no CB technology is currently available to fully satisfy the needed specifications, analyze other options to clear the fault or to support the fault clearing.
3 Theory

3.1 HVDC Transmission

This section provides an overview of different HVDC technologies including converters and transmission configurations, which have been applied in traditional point-to-point connections. Future multiterminal HVDC networks will be based on one of these technologies or a combination of two or more technologies that might be existing in a multi-vendor HVDC system [ACF+14].

3.1.1 Converter Technologies

The key component in an HVDC system is the static power converter, which converts the electrical energy from AC to DC and vice-versa and provides fast power controllability [ALWM09]. The converter is either operated as rectifier for power conversion from the AC to the DC system or as inverter for the power flow from DC to AC.

There are two basic converter technologies, the Current-Source Converter (CSC), also referred to as Line-Commutated Converter (LCC), and the self-commutated Voltage Source Converter (VSC).

The first commercial CSC DC link between Gotland and the Swedish mainland was successfully commissioned in 1954 [ABB14]. At that time, mercury-arc valves were employed in the converters, which were gradually replaced by thyristor valves by the mid-1960s [ALWM09]. Capacitor-Commutated Converters (CCC) were introduced in the late 1990s [BJ07], which exhibit improved voltage stability due to converter reactive power compensation by the series capacitors. At the same time, the first VSC-based Pulse-Width
Modulation (PWM) controlled HVDC system using Insulated Gate Bipolar Transistors (IGBT) was commissioned [FAD09]. Since then, the VSC technology has been considerably improved and a fast growing number of VSC HVDC transmission systems have been installed.

**VSC vs. CSC**

Nowadays, the CSC is still applied in point-to-point high power and ultra high voltage HVDC transmission [Asp07] due to its cost-effectiveness, high reliability of the thyristors, and good short-circuit withstand capability. The VSC reveals, however, some major advantages over the CSC regarding the application in multiterminal HVDC networks [ALWM09, BJ07, FAD09]:

- Independent control of active and reactive power
- Faster dynamic response
- Avoidance of commutation failure
- No restriction on minimum AC network short-circuit capacity
- No reactive power demand
- Black-start capability
- Maximum active power exchange only limited by AC network impedance
- Fast power reversal possible without voltage polarity reversal and, consequently, without mechanical switching of poles

In the following studies, only half-bridge VSCs are considered in multiterminal HVDC network applications due to their increased flexibility and controllability as compared to the CSC.
**Two-Level Topology**

The conventional three-phase two-level topology as illustrated in Fig. 3.1 is the simplest possible converter topology with a relatively small footprint. Each converter arm consists of a series connection of many IGBTs in order to achieve the required blocking voltage capability of the converter. The valves in one arm are switched simultaneously using usually sinusoidal PWM composed by a sinusoidal reference and a triangular carrier signal as illustrated in the upper graph in Fig. 3.2. This converter topology allows to apply two different phase-to-phase voltage levels on the AC side, either the positive DC voltage $+V_{dc}$ or the negative DC voltage $-V_{dc}$ as shown in the lower graph in Fig. 3.2. Hence, extensive harmonic filtering on the AC and DC side is required to achieve the desired sinusoidal AC voltage shape (dashed curve in lower graph) and a smooth DC voltage $V_{dc}$ using a phase reactor $L_s$ and a DC capacitor $C_{cap}$. High switching frequency is required in two-level topologies, which increases the switching losses.

![Figure 3.1: Conventional two-level converter topology](image)

**Multilevel Topology**

To reduce the required harmonic filtering and switching losses in the valves, the converter has to be able to create more distinct output voltage levels as compared to the two-level topology. Numerous multilevel topologies have been developed so far, which can be categorized in two groups: the diode-clamped neutral-point (NPC)
converters and the flying capacitor (FC) converters [FAD09].

A three-level NPC converter topology as shown in Fig. 3.3 is able to connect the neutral point voltage to the output. The advantages of the NPC are lower switch blocking voltage and lower the harmonic filtering needs compared to the two-level topology. Moreover, the required switching frequency and resulting switching losses are lower in multilevel topologies [AXHC02]. Figure 3.4 depicts an example PWM pattern with three voltage levels and the desired sinusoidal output voltage.

**Figure 3.2:** Two-level PWM waveforms [FAD09]

**Figure 3.3:** Three-level NPC converter topology [FAD09]
The NPC topologies have, however, significant drawbacks due to the inherent difficulty in DC capacitor voltage balancing and uneven distribution of losses between the converter valves due to their different duties. The number of diodes and the complexity of the control increases significantly with the number of levels [AXHC02]. The active NPC (ANPC) illustrated in Fig. 3.5 overcomes the problem of uneven loss distribution.

The five-level FC converter topology shown in Fig. 3.6 offers an even better performance given the five possible output voltage levels as depicted in Fig. 3.7. The switch blocking voltage and the switching losses are lower than in three-level topologies. In contrast to the NPC option, the FC topology ensures the same duty cycles for all semiconductor switches.
The disadvantage of the FC converters is the large volume of the capacitors, which increases proportionally to the square of their nominal voltage, and the resulting large footprint [AXHC02].

![Diagram of NPC phase leg](image)

**Figure 3.6:** Five-level FC converter topology [FAD09]

![Waveforms of Five-level PWM FC converter](image)

**Figure 3.7:** Five-level PWM waveforms [FAD09]

The newest generation of converter topologies is based on the modular multilevel converter (MMC) concept [Mar10]. Each converter arm consists of $n$ identical submodules as illustrated in Fig. 3.8 and represents a controllable voltage source, which is able to control the AC and DC voltages via the switching states of the sub-modules. In contrast to the other converter topologies, no DC filter
3.1 HVDC Transmission

Capacitors are needed in the MMC topology, due to the dynamic controllability of the DC voltage. The AC side filtering needs decrease with increasing number of submodules.

Each submodule comprises a storage capacitor $C_{\text{storage}}$ and two IGBTs with anti-parallel freewheeling diodes. Through switching of the IGBTs, the submodule is either discharged, i.e. the voltage of $C_{\text{storage}}$ given to the output, bypassed, i.e. zero voltage given to the output, or the submodule is charged again after discharging.

Disadvantages of the MMC concept are the high number of switching devices and storage capacitors needed for a reasonable number of submodules. Moreover, the storage capacitors have to be relatively large given the low switching frequency of the IGBTs.

![Figure 3.8: MMC converter topology](image)

3.1.2 Configurations and Operation Modes

The branches of a multiterminal HVDC network can be operated in monopolar or bipolar configuration. It is also possible to have different configurations within the same network [Cig13]. The different options are explained in the following paragraphs.
3 Theory

Asymmetric Monopole

Monopolar systems are intended for moderate power transfers and are the least expensive systems [BJ07]. Only one converter is used for each terminal. The asymmetric monopole, as depicted in Fig. 3.9 with earth return, is the simplest configuration. It requires only one fully insulated high-voltage conductor, but at the expense of a constant DC current through the ground that can cause corrosion of buried metallic structures such as pipes and earthing equipment of substations, transfer of high potentials, and saturation of transformers [JS10]. The use of a dedicated low-voltage neutral conductor mitigates the aforementioned problem, but requires the installation of two cables/lines and reveals higher transmission losses and costs compared to systems with earth return [Cig13].

![Figure 3.9: Asymmetric monopole configuration with earth return [Cig13]](image)

Symmetric Monopole

The symmetric monopole shown in Fig. 3.10 is the most popular configuration for point-to-point VSC HVDC links [Cig13]. There are no ground currents during normal operation, but two fully insulated pole conductors have to be installed. In contrast to the bipolar configuration, the two poles in the symmetric monopole cannot be operated independently, although they carry potential of opposite polarity.
3.1 HVDC Transmission

Bipole

The bipolar configuration in Fig. 3.11 has a higher transmission capacity than the other systems and provides more flexibility and redundancy due to two independently controlled poles. After a ground fault or the loss of one converter, the bipole can still be operated as an asymmetric monopole at reduced capacity. A metallic return is used again for the monopolar operation, if DC ground currents are not permissible. This solution results in higher costs compared to the earth return scheme because of the additional neutral cable.

Combination

A combination of different configurations within the same network is also possible under certain conditions. An example network comprising all three configurations is presented in Fig. 3.12. The two
bipole and the asymmetric monopole terminals, however, can only be operated with a dedicated metallic return conductor. The symmetric monopole converter has to be connected between the positive and negative poles of the bipole and cannot adjust itself DC current imbalances during faults.

![Figure 3.12: Combination of all three configurations](image)

**Figure 3.12:** Combination of all three configurations [Cig13]

### 3.2 Transients in HVDC Networks

Potential sources of transients in an HVDC network include surges due to pole-to-ground faults, pole-to-pole faults, lighting strikes, the operation of switching devices, and the sudden loss of a terminal and the subsequent change in the DC voltage. The emphasis in this thesis is on pole-to-ground faults, since they are regarded as significantly more frequent than pole-to-pole faults [CP11], although the latter would lead to more severe conditions [YFO12].

The time development of a pole-to-ground fault is explained in the following paragraph using the example of a fault in a cable system.

#### 3.2.1 Pole-to-Ground Faults

In cable systems, aging of the cable’s main insulation or external damages due to digging or anchoring in case of sea cables [Wor09] may lead to a breakdown of the cable insulation and eventually to a pole-to-ground fault. After the breakdown of the cable insulation,
3.2 Transients in HVDC Networks

an arc burns between the pole and the sheath of the cable and a ground loop through the sheath and the next grounding point is established. The current through the arc increases rapidly, which likely leads to explosion and destruction of the cable at the ground fault location. Subsequently, the arc burns between the pole and the ground, and a low-ohmic path is established in between. After the ground fault occurs, the voltage at the fault location decreases within a few microseconds to a level given by the fault resistance. Its value depends on the magnitude of the fault current and the characteristics of the soil, e.g. the ionization and de-ionization time constants, and the soil resistivity, as described in [WLD05]. The voltage drop at the fault location occurs very quickly, but not instantaneously due to the voltage supporting, distributed cable capacitance and the inductance in the fault path. The severity of the pole-to-ground fault depends on the value of the fault resistance and thus on the characteristics of the discharge path. In general, the higher the fault resistance, the lower the voltage drop along the line. Right after the fault occurrence, negative voltage surges start to travel from the fault location into both directions towards the terminals. Along its way, the distributed cable capacitance is discharged gradually into the ground fault. Upon the arrival at the terminals after the traveling time $\tau$, the negative voltage surge is reflected back as a positive surge due to the capacitive termination of the cable given by the DC capacitors [Kim70], [Hin70]. DC capacitors include the VSC capacitors and possible tuned filter capacitors, which are usually installed at the DC side of a VSC in order to reduce the voltage ripple injected by the converter. The converter technology determines the size of the DC capacitor. In general, multi-level converter topologies require less filtering, but larger converter capacitors due to the lower valve switching frequency. A 3-level neutral point clamped VSC requires an about three times higher capacitor volume than a 2-level topology for the same target value of less than 5% voltage ripple on the DC line [AXHC02]. Other topologies such as the MMC [Mar10] with a sufficiently large
number of submodules do not need any filter capacitances and the blocked converter valves prevent a discharge of the storage capacitors during DC faults [ALWM09]. In bipolar HVDC schemes, the midpoint of the DC capacitors is usually grounded to provide a reference voltage to the pole voltages [BJ07], [AXHC02]. The midpoint is grounded either via a low-ohmic connection or through a reactor depending on the requirement, whether the bipole has to be able to be operated in monopolar mode or not. The grounded capacitor midpoint and the ground fault form a loop that provokes a discharge of the capacitors. This discharge current is superposed on the reflected, backward traveling surge, which can be approximated by the convolution of the incident wave form and the impulse response of the DC capacitor [MM01] (assuming a purely capacitive cable termination):

\[ v_{\text{reflected}}(t) = \left[ -\delta(t) + \frac{2}{R_c C} e^{-\frac{t}{R_c C_{\text{cap}}}} \sigma(t) \right] * v_{\text{incident}}(t), \]  

(3.1)

where \( R_c \) is the approximated, concentrated cable resistance, \( C_{\text{cap}} \) the DC capacitance, \( \delta(t) \) a Dirac pulse, and \( \sigma(t) \) a step function.

As the surge arrives again at the fault location, one part is reflected and the other part transmitted through the fault into the opposite section of the cable according to the reflection coefficient \( \Gamma \) and transmission coefficient \( T \) as depicted in Fig. 3.13. The forward and backward traveling waves result in multiple peaks in the current wave form. The reflection coefficient is given by:

\[ \Gamma = -\frac{1}{1 + 2 \frac{R_f}{Z_0}}, \]  

(3.2)

where \( R_f \) is the fault resistance and the surge impedance of the cable is
\[ Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}. \] (3.3)

Fig. 3.14 illustrates the dependence of the reflection coefficient on the magnitude of the fault resistance. The transmission coefficient is related to the reflection coefficient as follows:

\[ T = 1 + \Gamma. \] (3.4)

Figure 3.13: Reflection and transmission of surges at fault location

Figure 3.14: Reflection coefficient at fault location as a function of fault resistance
3.3 Simulation of Electromagnetic Transients

The objective of power system transient simulation is the prediction of overcurrents and overvoltages resulting from system disturbances [WA07] as described in Section 3.2. The simulation process must be able to reproduce both, lumped elements, such as electrical machines and capacitor banks, and distributed elements, including Overhead Lines (OHLs) or cables. Also non-linear elements, such as switching arcs, surge arresters, and magnetic saturation phenomena must be represented in the simulations.

In the following, computational techniques to the solution of electromagnetic transient problems are described.

3.3.1 Direct Equation Solution

Some problems can be simplified and the system under study can be reduced to a simple RLC circuit with lumped elements. These second order systems can be solved analytically by well documented mathematical methods. An example is given in [YFO10], where the time development of the transient fault current and voltage is calculated for a pole-to-ground fault in a HVDC link.

In contrast to digital simulation, the analytic solution is continuous and does not have the problems resulting from numerical integration as explained in the following paragraphs. Most of the transient problems, however, are of higher order and comprise also distributed elements that cannot be solved directly by analytic methods.

3.3.2 State Variable Analysis

Another time domain method, which mitigates the aforementioned problem, is the state variable analysis. It consists of the derivation of partial differential equations (PDEs) from the distributed line parameters and the conversion of these equations into a set of coupled ordinary differential equations (ODEs) by spatial discretization of
the line [MK00]. Thus, all states of the system are accessible and a high spatial resolution can be achieved.

These higher order systems can be represented as a set of coupled implicit differential equations, commonly expressed in the state-space representation, as outlined in the following equations:

\[
\begin{align*}
\dot{x} &= A \cdot x + B \cdot u \quad (3.5) \\
y &= C \cdot x + D \cdot u, \quad (3.6)
\end{align*}
\]

where \(x\) is a vector containing all state variables, \(u\) is the source vector, \(y\) is the output vector, and \(A, B, C, D\) are coefficient matrices. This system of differential equation expressed in implicit form can be solved using a predictor-corrector algorithm and no rearranging into explicit form is required [WA07].

![Figure 3.15: Example circuit for state variable analysis](image)

To illustrate the application of state variable analysis, the example circuit in Fig. 3.15 is represented in the state space by

\[
\begin{bmatrix}
\dot{v}_2 \\
\dot{i}_2 \\
\dot{i}_1
\end{bmatrix} = 
\begin{bmatrix}
0 & \frac{-1}{C} & 1 \\
\frac{1}{L_2} & -\frac{R_2+R_f}{L_2} & 0 \\
\frac{1}{L_1} & 0 & 0
\end{bmatrix}
\begin{bmatrix}
v_2 \\
i_2 \\
i_1
\end{bmatrix}
+ 
\begin{bmatrix}
0 \\
0 \\
\frac{1}{L_1}
\end{bmatrix}
\cdot 
\begin{bmatrix}
v_1
\end{bmatrix}
\cdot \dot{u}. \quad (3.7)
\]

In this example, the state variables are directly accessed and the
output vector is equal the state variable vector $y = x$, i.e. $C = 1$ and $D = 0$ in (3.6).

The solution in the time domain is defined by the system’s zero input response (ZIR) and zero state response (ZSR) as follows:

$$x(t) = e^{A(t-t_0)} \cdot x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)} \cdot B \cdot u(\tau) d\tau.$$  \hspace{1cm} (3.8)

A possible way to solve the exponential function is the eigenvalue decomposition of the coefficient matrix $A$ into $A = W \cdot \Lambda \cdot W^{-1}$ with the eigenvalues in the diagonal of matrix $\Lambda$ and the eigenvectors in matrix $W$. The final time domain solution can be computed by

$$x(t) = W e^{A(t-t_0)} W^{-1} \cdot x(t_0) + \int_{t_0}^{t} W e^{A(t-\tau)} W^{-1} \cdot B \cdot u(\tau) d\tau.$$  \hspace{1cm} (3.9)

For a sinusoidal voltage source $u(t) = V_1 \cdot \sin(\omega t)$, the integral of the ZSR in (3.9) can be solved as

$$ZSR = W \cdot \text{diag} \left[ \frac{1}{\omega^2 + \lambda_i^2} \cdot (e^{\lambda_i(t-\tau)} V_1 \sin(\omega \tau - \xi_i)) \right] \cdot W^{-1} \cdot B \bigg|_{\tau = t}^{\tau = t_0}.$$  \hspace{1cm} (3.10)

with

$$\xi_i = \arctan \left( \frac{\lambda_i}{\omega} \right)$$  \hspace{1cm} (3.11)

and the eigenvalues $\lambda_i$.

The advantages of the state variable approach are the simplicity and the lack of numerical oscillations resulting from numerical integration substitution techniques.
The state variable analysis is, however, computationally very expensive for larger systems with a high number of state variables. Moreover, there are difficulties to represent distributed parameters, e.g. transmission lines.

A possible application of the state space representation is shown in [YFO10], where the steady-state fault current during a pole-to-ground fault with the AC side current feeding is expressed in the state space. In [KA09], a state space model is proposed to represent the dynamics of a HVDC line for assessing the interactions of a multi-infeed HVDC system. The time domain solution is derived through eigenvalue and eigenvector decomposition as described in [Lyg]. Not only the series impedance line model as described in Section 3.4 can be tackled by this method, but also a Π-model or a T-model using one or more sections. The more sections are used, the higher is the system order and the required computational effort. If all conductors and the ground are modeled by lumped elements, the eigenvalue decomposition method is also able to deal with multiple modes. The proposed method, however, is not suitable for the correct simulation of traveling waves and is computationally intensive.

### 3.3.3 Electromagnetic Transients Program (EMTP)

A widely used time domain method for the simulation of transients in power systems is the Electromagnetic Transient Program (EMTP) [Dom69] based on the difference equations model. This method is also referred to as numerical integration substitution (NIS). It allows an accurate simulation of transients in networks modeled by distributed as well as lumped elements and permits the inclusion of the frequency dependence of the line parameters.

The EMTP method integrates the problems of derivation of the network differential equations, the connection of them to a solvable system, and the numerical solution of the equations. The simple, but reasonable accurate trapezoidal integrator is often used to solve the NIS. The trapezoidal rule is, however, prone to numerical oscillations due to truncation. An alternative to the NIS is the root-matching
method as explained in [WA07].

**Discretization of System Elements**

A basic characteristic of EMTP is the discretization of the system elements. The differential equations for the inductor and capacitor shown in Figures 3.16(a) and 3.17(a) are

\[
e_k(t) - e_m(t) = L \cdot \frac{d i_{k,m}(t)}{d t}
\]  
(3.12)

and

\[
i_{k,m}(t) = C \cdot \frac{d (e_k(t) - e_m(t))}{d t}.
\]  
(3.13)

The differential equations can be transformed into integral form as

\[
i_{k,m}(t) = i_{k,m}(t - \Delta t) + \frac{1}{L} \int_{t-\Delta t}^{t} (e_k(\tau) - e_m(\tau)) d\tau
\]  
(3.14)

and

\[
e_k(t) - e_m(t) = \frac{1}{C} \int_{t-\Delta t}^{t} i_{k,m}(\tau) d\tau + e_k(t - \Delta t) - e_m(t - \Delta t),
\]  
(3.15)

where the past state at \( t - \Delta t \) is the known and the new state at \( t \) is unknown and solved for.

In the next step, the integral of the inductor is solved using the trapezoidal rule

\[
i_{k,m}(t) = \frac{\Delta t}{2L} \cdot (e_k(t) - e_m(t)) + I_{k,m}(t - \Delta t)
\]  
(3.16)
with the current source $I_{k,m}$ known from the past history value:

$$I_{k,m}(t-\Delta t) = i_{k,m}(t-\Delta t) + \frac{\Delta t}{2L} \cdot (e_k(t - \Delta t) - e_m(t - \Delta t)) \quad (3.17)$$

The capacitor integral is solved analogously

$$i_{k,m}(t) = \frac{2C}{\Delta t} \cdot (e_k(t)-e_m(t)) + I_{k,m}(t-\Delta t) , \quad (3.18)$$

again including the past value for the current source $I_{k,m}$

$$I_{k,m}(t-\Delta t) = -i_{k,m}(t-\Delta t) - \frac{2C}{\Delta t} \cdot (e_k(t) - e_m(t - \Delta t)) \quad (3.19)$$

Equations (3.16) and (3.18) can be represented as Norton equivalents as illustrated in Figures 3.16(b) and 3.17(b), respectively. In both elements, the value of the equivalent current source is the value of the current from the previous simulation time step $I_{k,m}(t - \Delta t)$.

Figure 3.16: Norton equivalent of the inductor [Dom69]

The equation of a resistor is simply
3 Theory

The transmission line with characteristic impedance $Z_0$ and the time of the wave. Fig. 3.18 depicts an EMTP two-port model of the transmission line with characteristic impedance $Z_0$.

From Fig. 3.18 follow the equations for the sending end and receiving end currents using a simulation time step of $\Delta t$:

$$i_{k,m}(t) = \frac{1}{R} \cdot (e_k(t) - e_m(t))$$  \hspace{1cm} (3.20)

and no discretization is required.

The truncation error introduced by the discretization with the trapezoidal rule in (3.16) and (3.18) is of order $(\Delta t)^3$, which implies a sufficiently small time step $\Delta t$ in the simulations [Dom69].

**EMTP Transmission Line Model**

The EMTP model of a lossless transmission line is based on the decoupling of the sending and receiving end given by the traveling time of the wave. Fig. 3.18 depicts an EMTP two-port model of the transmission line with characteristic impedance $Z_0$.

From Fig. 3.18 follow the equations for the sending end and receiving end currents using a simulation time step of $\Delta t$:
\[ i_s(t) = \frac{1}{Z_0} v_s(t) - I_s(t - \Delta t) \]  
\[ i_r(t) = \frac{1}{Z_0} v_r(t) - I_r(t - \Delta t) , \]  
with the past values of the equivalent current sources

\[ I_s(t - \Delta t) = \frac{1}{Z_0} v_s(t - \Delta t) - i_s(t - \Delta t) \]
\[ I_r(t - \Delta t) = \frac{1}{Z_0} v_r(t - \Delta t) - i_r(t - \Delta t) . \]

**Nodal Equations**

The nodal equations for any arbitrary system can be established using the elements equivalent circuits, which results in a system of linear algebraic equation

\[ Yv(t) = i(t) - I(t - \Delta t) \]  

with nodal conductance matrix \( Y \), vector of node voltages \( v(t) \), vector of branch currents \( i(t) \), and vector \( I(t - \Delta t) \) containing past values of the equivalent current sources. The nodal conductance matrix \( Y \) is formed following the well-known admittance matrix.

**Figure 3.18:** EMTP transmission line model
formation rules in steady-state analysis. This matrix has to be set up once as long as the simulation time step $\Delta t$ remains unchanged, e.g. in simulations with fixed time step.

Part of the nodal voltages in (3.25) are known, while others are unknown and must be computed based on the known values. Therefore, the nodal equations in (3.25) are rearranged into a subset of unknown $v_1$ and a subset of known values $v_2$:

$$
\begin{bmatrix}
Y_{11} & Y_{12} \\
Y_{21} & Y_{22}
\end{bmatrix}
\begin{bmatrix}
v_1(t) \\
v_2(t)
\end{bmatrix}
=
\begin{bmatrix}
i_1(t) \\
i_2(t)
\end{bmatrix}
- \begin{bmatrix}
I_1(t - \Delta t) \\
I_2(t - \Delta t)
\end{bmatrix}.
$$

(3.26)

The unknown vector $v_2(t)$ is obtained by solving

$$
Y_{11} \cdot v_1(t) = i_1(t) - I_1(t - \Delta t) - Y_{12} \cdot v_2(t)
$$

(3.27)

using well-known numerical methods for matrix factorizations. Since $Y$ contains mainly zero elements, computation time can be saved, if only non-zero elements are stored, i.e. sparse matrix approach. After the computation of $v_1(t)$, the value of $I(t - \Delta t)$ has to be updated for the next time step.

Not only passive elements can be simulated using EMTP, but also switches and elements with nonlinear time-varying parameters, such as saturable transformers.

### 3.3.4 Evaluation

The disadvantage of the EMTP method is the discrete integration algorithm, which requires the past history of the network [MK00]. The choice of the discrete simulation time step is crucial in order to get accurate results. The traveling delay on a transmission line must not be smaller than the solution time step $\Delta t$. The solution time step also bounds the maximum possible frequency in the simulation output. Moreover, the EMTP method gives only the sending
and receiving end values for the line current and voltage. Intermediate points cannot be obtained unless the line is split appropriately, which would require a higher computational effort for a large number of intermediate values as compared to the state variable analysis [RGB05].

The evaluation of the simulation approaches showed that the EMTP approach is the best choice for models consisting of transmission lines with distributed, frequency-dependent parameters and in which only the sending end and receiving end quantities are of interest. The state-space approach performs better than the EMTP approach in case of single frequency line models with cascaded Pi-sections, where the voltage and current distribution along the line is of interest and its values have to be accessible. The EMTP based frequency-dependent line model has been selected for the studies due to the best performance, most accurate results, and the fact that only the receiving end and sending end currents are required.

### 3.3.5 Simulation Software

Various EMTP-type programs are available today. A selection of popular simulation tools are given in Table 3.1 (list is not complete). All simulations in this thesis have been performed using the PSCAD/EMTDC engine, which is one of the most popular and proven software in industry and academia.

#### PSCAD/EMTDC

The Power Systems Computer Aided Design (PSCAD) is a graphical user interface to the EMTDC [Man10] engine (EMTDC stands for Electromagnetic Transients including DC). EMTDC solves differential equations in the time domain based on a fixed time step. It allows to represent electromagnetic, electromechanical, and control systems and to simulate their time domain instantaneous responses. In contrast to phasor domain solution engines, such as load-flow and transient stability programs, EMTDC gives instantaneous values in
Table 3.1: EMTP-Type Software (list is not complete)

<table>
<thead>
<tr>
<th>Program</th>
<th>Organization</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATP Program</td>
<td><a href="http://www.emtp.org">www.emtp.org</a></td>
</tr>
<tr>
<td>PSCAD/EMTDC</td>
<td>Manitoba HVDC Research Centre</td>
</tr>
<tr>
<td>MicroTran</td>
<td>Microtran Power Systems Analysis Corporation</td>
</tr>
<tr>
<td>PSS NETOMAC</td>
<td>Siemens AG</td>
</tr>
<tr>
<td>EMTAP</td>
<td>EDSA Micro Corporation</td>
</tr>
<tr>
<td>PowerFactory</td>
<td>DlgSILENT</td>
</tr>
<tr>
<td>RSCAD</td>
<td>RTDS Technologies Inc.</td>
</tr>
</tbody>
</table>

time, which can also be converted in phasor magnitudes and angles. Moreover, all frequencies, bounded only by the solution time step, can be represented by EMTDC, whereas load-flow and stability programs yield only fundamental frequency information given the system’s representation by steady-state equations.

Some advantages of EMTDC over other EMTP-type programs are the mathematical collapsing of series and parallel electric elements, the increased LDU matrix decomposition speed using the Optimal Ordering algorithm, the interpolation algorithm, and the superior transmission line and cable models.

### 3.4 Line Models

Possible line models for transient simulations are listed in this section in the order of increasing level of detail.

#### 3.4.1 Frequency-Independent

These are single frequency models and do not take into account the frequency-dependency of the line parameters.
Series Impedance

The simplest cable model consists of a single series impedance and neglects all cable capacitances. This is only accurate for steady-state simulations, i.e. load flow calculations, and in medium voltage DC cables as used in [YFO10] and the IEC 61660 standard [IEC97] for DC auxiliary installations in power plants and substations. This model is not suitable for long HVDC cables.

Cascaded Lumped Pi-Sections

This model accounts for the cable capacitance using a certain number of cascaded Pi-sections with lumped, frequency independent impedances and admittances as illustrated in Fig 3.19. The number of sections depends on the frequency range of concern [RGB05]. The highest frequency that can be represented by the cascaded Pi-circuits is approximated by the following equation [TCW+99]

\[ f_{\text{max}} = \frac{N \cdot c}{\pi \cdot l}, \]  

(3.28)

where \( N \) represents the total number of Pi-sections, \( c \) the traveling speed of the wave, and \( l \) the length of the line. Lumped parameters are generally less accurate than distributed parameters except for the special case with a simulation time step larger than the line traveling time, when the lumped nominal Pi-circuits are the only viable solution [MMD93]. Moreover, the Pi-sections introduce an arti-
cial ringing in the wave form due to the reflections at the junctions between two neighboring Pi-sections [MMD93].

**Bergeron Model**

The Bergeron’s model [Ber61] takes into account the distributed nature of the line parameters except for the line resistance, which is implemented in lumped form at the line ends and in the middle of the line. This is still a single frequency model that is adequate whenever only the fundamental frequency is of interest and the lines are sufficiently long [Man10]. Reasonable results are achieved provided that \( R/4 \ll R_0 \), where \( R_0 = \sqrt{L/C} \) is the characteristic line impedance [WA07].

**Distributed Parameters**

Traveling wave theory has to be considered in case of lines with frequency independent, distributed elements. In contrast to Bergeron’s model, also the line resistance is represented in a distributed form. This frequency independent line model is again only accurate for systems with a dominant fundamental frequency.

The partial differential equations for an ideal lossless transmission line with \( R = 0 \) and \( G = 0 \) are

\[
\begin{align*}
-\frac{\partial v}{\partial x} &= L \cdot \frac{\partial i}{\partial t}, \\
-\frac{\partial i}{\partial x} &= C \cdot \frac{\partial v}{\partial t}
\end{align*}
\]

with constant line inductance \( L \) and line capacitance \( C \).

These equations can be transformed into decoupled equations
\[-\frac{\partial^2 v}{\partial x^2} - L \cdot C \cdot \frac{\partial^2 v}{\partial t^2} = 0, \tag{3.31}\]
\[-\frac{\partial^2 i}{\partial x^2} - L \cdot C \cdot \frac{\partial^2 i}{\partial t^2} = 0 \tag{3.32}\]

with the general solution in d’Alembert form with forward \((\cdot)^+\) and backward \((\cdot)^-\) traveling waves

\[v(x, t) = v^+ \left( t - \frac{x}{c} + \xi^+ \right) + v^- \left( t + \frac{x}{c} + \xi^- \right), \tag{3.33}\]
\[i(x, t) = i^+ \left( t - \frac{x}{c} + \xi^+ \right) + i^- \left( t + \frac{x}{c} + \xi^- \right), \tag{3.34}\]

where \(c = 1/\sqrt{L \cdot C}\) is the propagation speed. \(\xi^+\) and \(\xi^-\) are arbitrary constants for the forward and backward traveling wave, respectively.

The general solution of a lossy transmission line cannot be directly expressed in d’Alembert form in the time domain as for the ideal line due to the dispersion given by the losses [MM01]. The time domain partial differential equation are now

\[-\frac{\partial v}{\partial x} = L \cdot \frac{\partial i}{\partial t} + R \cdot i, \tag{3.35}\]
\[-\frac{\partial i}{\partial x} = C \cdot \frac{\partial v}{\partial t} + G \cdot v. \tag{3.36}\]

Decoupling and transformation of the equations into the Laplace domain yields
\[-\frac{d^2V}{dx^2} - k^2(s) \cdot V = 0, \quad (3.37)\]
\[-\frac{d^2I}{dx^2} - k^2(s) \cdot I = 0 \quad (3.38)\]

where \(k(s) = \sqrt{(R + sL)(G + sC)}\) is the propagation constant.

The general solutions in the Laplace domain of equations (3.37) and (3.38) have the form

\[V(x, s) = V^+(s)e^{-k(s)(x-x^+)} + V^-(s)e^{-k(s)(x-x^-)}, \quad (3.39)\]
\[I(x, s) = \frac{1}{Z_0(s)} \cdot \left[ V^+(s)e^{-k(s)(x-x^+)} - V^-(s)e^{-k(s)(x-x^-)} \right], \quad (3.40)\]

where \(V^+, V^-, x^+, \text{ and } x^-\) are again arbitrary functions and \(Z_0(s) = \sqrt{(R + sL)/(G + sC)}\) is the line’s characteristic impedance.

Equations (3.39) and (3.40) have no straightforward solution in the time domain. Reference [MM01] proposes an approach consisting of the convolution \(\ast\) of the timely and locally resolved impulse response \(q(x, t)\) of the line and the input voltage step \(v^+(t)\) and \(v^-(t)\), which yields the current and voltage values at every point in time and space:

\[v(x, t) = [q_v(x, t) \ast v^+(t)] + [q_v(l - x, t) \ast v^-(t)], \quad (3.41)\]
\[i(x, t) = [q_i(x, t) \ast i^+(t)] + [q_i(l - x, t) \ast i^-(t)], \quad (3.42)\]

where \(l\) is the line length.

The time domain voltage impulse response \(q_v(x, t)\) is given in [MM01]:
where $I_1(\cdot)$ is the modified first-order Bessel function \[AS64\], $u(t)$ the unit step function, and $\delta(t)$ the Dirac function. The coefficients $\mu = 0.5 \cdot (\alpha + \beta)$ and $\nu = 0.5 \cdot (\alpha - \beta)$ depend on the inductive $\alpha = R/L$ and capacitive $\beta = G/C$ damping factors.

The impulse response comprises two terms, a principal term that accounts for the attenuation introduced by the distributed losses of the line and a remainder term, which represents the distortion of the wave form due the line’s dispersion. The resulting convolution integral can easily be solved for the principal term, since it consists only of a delayed Dirac pulse, whereas the more complex remainder requires a lot of computational effort. The trapezoidal rule is applied to solve approximately the convolution integral \[MM01\]. In most cases, however, the remainder term can be neglected as stated in \[Rus69\].

The current impulse response $q_i(x,t)$ is missing in \[MM01\], but can be derived similarly:

$$ q_i(x,t) = \frac{\beta + 1}{R_0} e^{-\mu \frac{x}{c}} \delta \left( t - \frac{x}{c} \right) + e^{-\mu t} I_1 \left( \nu \sqrt{t^2 - \left( \frac{x}{c} \right)^2} \right) \sigma \left( t - \frac{x}{c} \right) \\
+ \frac{\beta - \mu R_0}{R_0} I_0 \left( \nu \sqrt{t^2 - \left( \frac{x}{c} \right)^2} \right) \sigma \left( t - \frac{x}{c} \right) $$

(3.44)

with $R_0 = \sqrt{L/C}$ and the modified zero-order Bessel function $I_0(\cdot)$ \[AS64\].
3.4.2 Frequency-Dependent Parameters

The most accurate line model considers multimodal wave propagation and frequency dependent, distributed parameters. Several models exist for AC transmission lines, but they can also be applied to DC transmission. Since a closed mathematical solution of the exact line equations in the time domain is practically impossible, numerical approximation techniques are required. The solution as a function of the frequency is highly oscillatory and makes ordinary numerical techniques very susceptible to instability and accuracy errors [Mar82]. One of the first frequency dependent models was proposed by [Bud70], which has low accuracy due to the oscillatory nature of the solution. An improvement was achieved by [MD74] that further developed the idea of weighting functions. In the time domain, these functions consist, however, of a train of peaks due to the successive reflections of the waves at both ends of the line and the corresponding convolution in the time domain is, therefore, difficult to evaluate.

In order to improve the weighting function method by [Bud70], [Sne72] introduced a change of variables and proposed forward travelling functions (single mode propagation)

\[
F_r(s) = V_r(s) + Z_0(s) \cdot I_r(s) \quad (3.45)
\]
\[
F_s(s) = V_s(s) + Z_0(s) \cdot I_s(s) \quad (3.46)
\]

and backward travelling functions

\[
B_r(s) = V_r(s) - Z_0(s) \cdot I_r(s) \quad (3.47)
\]
\[
B_s(s) = V_s(s) - Z_0(s) \cdot I_s(s) , \quad (3.48)
\]

where \( V_r \) and \( I_r \) are the receiving end values and \( V_s \) and \( I_s \) the sending end values. \( Z_0(s) = \sqrt{(R + sL)/(G + sC)} \) is the line’s characteristic impedance.
A comparison of equations (3.46) to (3.48 with the frequency domain propagation functions (3.39) and (3.40) shows that

\[ B_r(s) = A(s) \cdot F_s(s) \tag{3.49} \]

and

\[ B_s(s) = A(s) \cdot F_r(s) \tag{3.50} \]

where

\[ A(s) = e^{-k(s)l} \tag{3.51} \]

with the exponent \( k(s) = \sqrt{(R + sL)(G + sC)} \) of the propagation function \( e^{-k(s)l} \) and the line length \( l \).

\( A(s) \) is a weighting function that links the amplitude of the forward or backward traveling wave at one end of the line with the one at the other end of the line. The real part of the complex number \( A(s) \) is the attenuation constant and the imaginary part is the phase constant. In [MM01], the weighting function \( A(s) \) is denominated as ”global propagation operator” \( P(s) \) and corresponds to the frequency domain response of the physical system. The time domain solution of (3.49) is a convolution integral

\[ b_r(t) = \int_{\tau}^{\infty} f(t - u) \cdot a(u) \, du. \tag{3.52} \]

The lower limit of this integral is the traveling time \( \tau = l/c \) of the fastest frequency component of the traveling wave defined by the line length \( l \) and the propagation speed \( c \).

The direct evaluation of the convolution integral in (3.52) as originally proposed by [Bud70,MD74] is, however, a lengthy process and
prone to numerical instabilities due to the shape of the weighting function. An alternative to the direct evaluation is the synthesis of the weighting function $A(s)$ and the characteristic impedance $Z_0(s)$ by rational functions as proposed in [Mar82, MMD93]. They synthesize the characteristic impedance of the line in the frequency domain as

$$Z_0(s) = \frac{N(s)}{D(s)} = \frac{(s + z_1)(s + z_2)\cdots(s + z_n)}{(s + p_1)(s + p_2)\cdots(s + p_n)}. \quad (3.53)$$

The poles $p_n$ and the zeros $z_n$ are real, positive, and simple. The weighting function $A(s)$ can be expressed as

$$A(s) = A_0(s) \cdot e^{-s\tau}, \quad (3.54)$$

where $A_0(s)$ has the same shape as $A(s)$, but shifted by the traveling time $\tau$ of the fastest frequency component. Function $A_0(s)$ is approximated again by rational functions

$$A_0(s) = \frac{N(s)}{D(s)} = \frac{(s + z_1)(s + z_2)\cdots(s + z_n)}{(s + p_1)(s + p_2)\cdots(s + p_m)}. \quad (3.55)$$

with a higher number of poles than zeros and the poles lying in the left hand side of the complex plane.

A partial fraction expansion of the rational functions approximation (3.53) and (3.55) in the Laplace domain and subsequent transformation into the time domain results in a sum of exponential terms from which the past history integrals of the convolution can be evaluated recursively. The poles and zeros of the rational function are determined using curve fitting techniques. The number of poles and zeros is either pre-established or determined by the fitting routine, as proposed by [Mar82]. This routine is based on an adaptation of Bode’s simple asymptotic fitting concept, in which
the poles and zeros of the rational approximation are successively allocated running from zero to the highest frequency.

**Multiphase Systems**

In the previous section, only single phase system with one time delay \( \tau \) have been considered. Multiphase systems with multiple conductors such as cables may contain widely different time delays for the individual modes. In this case, the fitting of the function \( A_0(s) \) with rational functions in the phase domain may be very difficult [GS98]. Therefore, the phase domain quantities are transformed into the modal domain

\[
i = T_i i^m
\]
\[
v = T_v v^m.
\]

\( T_i \) and \( T_v \) are the transformation matrices and the superscript \( m \) denotes modal quantities.

The modal weighting function \( A^m(s) \) is related to the phase domain quantity by

\[
A = T_i A^m T_i^{-1}.
\]

References [Mar82, MMD93] assume the transformation matrices \( T_i \) and \( T_v \) to be constant and frequency-independent. In general, these matrices are, however, a function of frequency and have to be fitted as well. The method of optimal scaling was introduced by [GS98] to fit the transformation matrix, which allows to fit it column-by-column and saves substantially computational time. The same method is used to fit \( A(s) \) and \( Z_0(s) \). Unlike traditional methods [Mar82], the new rational function approximation is not limited to real poles and zeros. Moreover, [Mar82] considers only the magnitude function \( A_0(s) \) in the fitting process. The fitting by optimal
scaling, however, uses both the real and the imaginary part of $A^m$. Therefore, the time delay in (3.54) is removed before the fitting process, yielding a smooth function, which can be fitted by low order rational functions.

A comprehensive study of multiple mode propagation from a system point of view is given in [Kim70, Hin70], where two modes, namely a conductor mode (positive sequence) and a ground mode (zero sequence) is distinguished. The transformation of the time values into the modal domain is described for a monopolar line to ground fault in a bipolar scheme with 2 terminals. The ground fault on one pole induces a voltage step on the unfaulted pole due to capacitive coupling of the poles. This voltage surge propagates in both directions and is reflected at the terminals. Different terminations are considered and the corresponding reflection factors are defined for each mode. In case of capacitive termination, the highest overvoltage occurs at the location that corresponds to the fault location mirrored at the midpoint of the line.
4 Transient Simulation Models

4.1 Converter

The default converter model used in the simulations is a generic ±320 kV 900 MW bipolar half-bridge VSC converter with concentrated midpoint-grounded DC capacitors $C_{\text{cap}}$ at each terminal and possible pole reactors at each feeder as depicted in Fig. 4.1.

The capacitive coupling of the positive and negative pole, which may induce voltage surges on the healthy pole [Hin70], [Kim70], is neglected. In case of interconnections with screened cables, this is a justified simplification, whereas in OHL links, the distance between the poles has to be large enough to ensure that the induced voltage step is negligibly small. Applying this assumption, the bipole can be simplified to an asymmetrical monopole, which is equally valid to a bipole without coupling of the poles. After local detection of an overcurrent in the converter arm, the control protects the IGBT modules through blocking of the valves within a few $\mu$s making the half-bridge based VSC an uncontrolled rectifier [YFO10, CLP11] as depicted in Fig. 4.1. This simplification is valid for all half-bridge based converter topologies as presented in Section 3.1.1. Only the number of series connected free-wheeling diodes differs in each topology and, hence, the converter resistance during blocking. Also the transient converter inductance varies among the topology, e.g. the MMC topology requires additional arm reactors. The converter topology, i.e. its resistance and inductance during transient operation, has only a marginal influence on the total fault current in the system and, therefore, the same transient model as illustrated in Fig. 4.1 is used in all simulations. The converter topology is, how-
ever, decisive for the size of the DC capacitor $C_{\text{cap}}$, whose influence on the transient fault current is analyzed in detail in Chapter 5.

Additional pole or line reactors $L_{\text{pole}}$ may be required at each end of a line to limit the rate of rise of the fault current as discussed in Chapters 5, 9, and 10.

The primary windings of the converter transformers with reactance $L_t$ have star configuration with grounded neutral and delta configuration on the secondary side. The additional phase reactor $L_s$ between the converter bridge and the transformer serves for harmonic filtering of the AC currents. Other shunt filters for AC side filtering are neglected, since they have almost no influence on the transient fault current. The losses of the transient converter model during the AC infeed are determined by the on-state resistance $R_D$ of the freewheeling diodes. The value for $R_D$ is based on a series connection of 89 4500 kV/2000 A press-pack IGBTs [ERT+04]. The considered secondary winding voltage of each converter transformer is between 213 and 270 kV. The default parameter values are given in Section 4.3.

![Figure 4.1: Default converter model for transient simulations](image)

The PSCAD implementation of the converters consists of an additional DC voltage source for the initial steady-state operation and
a transient model comprising the freewheeling diodes only as illustrated in Fig. 4.2. No implementation of IGBTs or switching control is required in the transient studies and DC voltage sources are sufficient for the initialization of the steady-state line currents.

![Diagram of the converter model](image)

**Figure 4.2**: PSCAD implementation of the converter model

At the beginning of the simulation, the system is in steady-state operation and the switches ”BRK2” are open and ”BRK1” closed. The AC and DC voltage sources are ramped up steadily within 5 ms to prevent large initial transients in the system. The values of the DC voltage sources at each terminal are set in order to reach approximately the nominal line currents by applying the required voltage drop along the line. Therefore, the line resistance has to be known to calculate the needed voltage drop.

After the steady-state model has reached its steady-state, the ground fault circuit is closed. The overcurrent is detected independently at each terminal and after having exceeded the protection threshold value, the switches ”BRK2” are closed and ”BRK1”
opened to activate the transient converter model.

![Figure 4.3: Comparison of converter initialization methods - $i_{cb}$: Total line current, $i_c$: DC capacitor contribution, $i_{ac}$: AC network contribution](image)

To mitigate inrush currents from the previously no-loaded AC side, the voltage drop across "BRK2" has to be as small as possible. Therefore, the ground fault circuit is closed when one of the AC phase voltage is at its peak and the transformer ratio is chosen to ensure that the DC voltage is equal the AC phase voltage peak value. There is always a small voltage difference across the contacts of "BRK2" due to the travelling delay of the surge until it reaches the terminal. The error introduced by this initialization method is, however, negligibly small. Figure 4.3 illustrates the comparison of the proposed initialization through DC voltage sources in a single terminal system with an alternative method, which uses the diode rectifier to initialize the line current. For this comparison study,
the rectifier is connected to the line, which is terminated by a load resistance.

The advantages of the proposed initialization method over other methods are: the complex switching control of the converter valves can be neglected, the same converter model can be used at all terminals, and no distinction between converters in rectifying and inverting mode has to be made. Moreover, no loads in series to the converters in inverter mode have to be modelled and the nominal line currents can easily be initialized by the DC voltage sources in a DC network with a large number of terminals.

### 4.2 AC Network

The AC networks adjacent to the converters are modeled by their equivalent short-circuit impedance consisting of \( R_{ac} \) and \( L_{ac} \), and a voltage source \( V_{ac} \) as illustrated in Fig. 4.1. The values of the AC network parameters are determined based on the Short-Circuit Power Ratio (SCR) of the AC network at the Point of Common Coupling (PCC). The SCR is defined as the ratio of the short circuit capacity at the PCC and the rated power of the converter as follows:

\[
\text{SCR} = \frac{P_{sc}}{P_{PCC}} / \frac{P_{\text{rated converter}}}{.} \quad (4.1)
\]

The equivalent AC resistance is calculated by

\[
R_{ac} = \frac{V_{ac}^2}{\text{SCR} \cdot P_{\text{converter}}} \cdot \cos \left[ \arctan \left( \frac{X_{ac}}{R_{ac}} \right) \right] \quad (4.2)
\]

and the value for the AC inductance by

\[
L_{ac} = \frac{V_{ac}^2}{\text{SCR} \cdot P_{\text{converter}}} \cdot \sin \left[ \arctan \left( \frac{X_{ac}}{R_{ac}} \right) \right] \cdot \frac{1}{2 \cdot \pi \cdot f} \quad (4.3)
\]
The fraction $\frac{X_{ac}}{R_{ac}}$ is the ratio between AC system’s reactance and resistance and $f$ is the system frequency.

### 4.3 Default Parameter Values

The default values of the system parameters are summarized in Table 4.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Converter Power (Bipole)</td>
<td>900 MW</td>
</tr>
<tr>
<td>DC Voltage</td>
<td>$\pm 320$ kV</td>
</tr>
<tr>
<td>AC Voltage (L-L, RMS)</td>
<td>400 kV</td>
</tr>
<tr>
<td>AC System Frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>$X_{ac}/R_{ac}$ of AC Network</td>
<td>10</td>
</tr>
<tr>
<td>SCR at PCC</td>
<td>variable</td>
</tr>
<tr>
<td>Transformer Secondary Winding Voltage</td>
<td>variable</td>
</tr>
<tr>
<td>Transformer Leakage Reactance</td>
<td>0.1 p.u.</td>
</tr>
<tr>
<td>Converter Phase Reactor</td>
<td>0.05 p.u.</td>
</tr>
<tr>
<td>Total Resistance of Converter</td>
<td>0.3283 $\Omega$</td>
</tr>
<tr>
<td>DC Capacitor</td>
<td>variable</td>
</tr>
<tr>
<td>Line/Pole Reactor</td>
<td>variable</td>
</tr>
</tbody>
</table>

The parameters denoted as variable are changed throughout the chapters of this thesis. These parameters are subject to individual investigations of their influence on the system behaviour. A certain range of values for the parameter variations is given in each chapter and a new base case scenario is defined with a corresponding set of the aforementioned variable parameter values. Starting from the base case, these parameter values are then increased and decreased to demonstrate their influence. The base case scenario has to be adapted each time to the chosen range of parameter variations in order to amplify the effect of the maximum and minimum value of
the investigated variable parameter.

4.4 Lines

4.4.1 Cable Model

The same PSCAD cable model is used in the simulations throughout this thesis. The general design of the cable cross-section is derived from a real 150 kV cross-linked polyethylene (XLPE) VSC-HVDC submarine cable [RHPL07], [Wor09]. The cross-section was scaled up to a 320 kV cable respecting the diameter of the copper conductor [ABB06], while keeping the electric field stress (cold condition) similar. The material properties are based on values given in [MMD10]. Table 4.2 summarizes the material properties and Fig. 4.4 illustrates the cable cross-section dimensions of all cable layers. Thin semiconducting layers are extruded on the inner and outer surface of the main insulation of the cable to provide smooth surfaces without field enhancing protrusions. The PSCAD uses fixed built-in corrections for the permittivity of the semiconducting layers. The cable sheath is assumed to be grounded at each cable joint every approximately 900 m as in [DRA+10] to prevent overvoltages in the sheath during pole-to-sheath faults. Simulations have shown that the sheath impedance in the aforementioned grounding scheme contributes only a negligibly small portion to the conductor current damping and the sheath is, therefore, mathematically eliminated in the simulations, i.e. assumed to have ground potential over the whole cable length. The shunt conductance of the XLPE insulation is set to $10^{-12}$ S/km.

The chosen cable model makes use of the PSCAD built-in detailed frequency-dependent, distributed-parameter line model as described in Section 3.4.2. This is the most accurate model available that also accounts for the frequency dependence of the cable parameters.
### Table 4.2: Properties of the Assumed 320 kV XLPE Cable

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Outer Radius (mm)</th>
<th>Resistivity (Ωm)</th>
<th>Rel. permittivity</th>
<th>Rel. permeability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>Copper</td>
<td>21.4</td>
<td>1.72 \cdot 10^{-8}</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Insul.</td>
<td>XLPE</td>
<td>45.9(^1)</td>
<td>-</td>
<td>2.3</td>
<td>1</td>
</tr>
<tr>
<td>Sheath</td>
<td>Lead</td>
<td>49.4</td>
<td>2.2 \cdot 10^{-7}</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Insul.</td>
<td>XLPE</td>
<td>52.4</td>
<td>-</td>
<td>2.3</td>
<td>1</td>
</tr>
<tr>
<td>Armor</td>
<td>Steel</td>
<td>57.9</td>
<td>1.8 \cdot 10^{-7}</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>Insul.</td>
<td>PP</td>
<td>61.0</td>
<td>-</td>
<td>2.1</td>
<td>1</td>
</tr>
</tbody>
</table>

\(^1\) Including inner and outer semi-conductor layer of 1.2 and 1.3 mm thickness, respectively

#### 4.4.2 Overhead Line Model

The implemented OHL model is based on real data of a HVDC OHL connection. The parameters of the stranded 45/7 AL3/Steel conductors and steel shield wires are taken from the IEC technical report 61597 for OHLs [Int95]. The monopolar tower dimensions are based on data of the 500 kV Inga-Shaba HVDC link [Ele93]. A scheme indicating the height of the conductor and the ground wire is illustrated in Fig. 4.5. The OHL properties required as input parameters in PSCAD are summarized in Table 4.3. PSCAD simply decreases the effective conductor height by a factor of 2/3 of the sag to approximate the effect of the conductor sag [Man10]:

\[
y' = y - \frac{2}{3} \cdot d_{sag},
\]

where \(y'\) is the effective height, \(y\) the original conductor height from the data sheet, and \(d_{sag}\) the total sag. In this way, the sag is eliminated by assuming an uniform conductor height \(y'\).

The selected conductors of the OHL have a similar current carry-
ing capacity as compared with the XLPE cable, whereas the rated voltage is much higher. For better comparison of the simulation results of the two transmission media, the rated voltage of the OHL is reduced to the cable voltage of 320 kV and the same converter ratings as in the cable system are applied.
Table 4.3: Properties of the 500 kV OHL

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conductor Radius</td>
<td>16.2 mm</td>
</tr>
<tr>
<td>Strand Radius</td>
<td>4.5 mm</td>
</tr>
<tr>
<td>Total # of Strands</td>
<td>52</td>
</tr>
<tr>
<td># of Outer Strands</td>
<td>21</td>
</tr>
<tr>
<td>Conductor DC Resistance</td>
<td>57.8 mΩ/km</td>
</tr>
<tr>
<td>Sag</td>
<td>13.9 m</td>
</tr>
<tr>
<td>Height of Conductor</td>
<td>25.32 m</td>
</tr>
<tr>
<td>Ground Wire Radius</td>
<td>9.5 mm</td>
</tr>
<tr>
<td>Ground Wire Sag</td>
<td>13.25 m</td>
</tr>
<tr>
<td>Ground Wire DC Resistance</td>
<td>2.86 Ω/km</td>
</tr>
</tbody>
</table>

Figure 4.5: OHL scheme with conductor C1 and ground wire G1
5 Analysis of Transient Fault Currents

5.1 Contribution of Fault Current Sources

5.1.1 Introduction

This section aims to contribute to the better understanding of the transient development of the fault current through a DC CB during a pole-to-ground fault in an MTDC cable network. Therefore, the fault current is broken down into the individual contributions from the different network components, such as DC capacitors, cables, and the adjacent AC network. A breakdown of the fault current allows for a detailed analysis of the influence of the component parameters and fault condition on the total fault current in the DC CB. It enables the specification of DC CB requirements and fault detection mechanisms, as well as the identification of measures to reduce the transient overcurrent in the CB without additional Fault Current Limiters (FCLs). This section illustrates the sensitivities of the key parameters in different scenarios, which consider the converter technology including the required filters and the fault condition, i.e. the fault impedance.

To do so, this section analyzes pole-to-ground faults in a simple, radial, bipolar three-terminal HVDC cable system with two cable branches only. This is the simplest possible layout including all available components, which are able to contribute to the fault current in the CB. While cable faults occur less frequently than overhead line faults, but are typically permanent, it is still a condition that a future DC network has to cope with. The em-
phasis in this section is on pole-to-ground faults, since they are regarded as significantly more frequent compared to pole-to-pole faults [CP11], although the latter fault would lead to more severe conditions [YFO12].

5.1.2 Simulation Model

Cable Model

The default cable model and cable parameters as presented in Section 4.4.1 are applied in this study.

Converter and Network Model

The 3 terminal radial HVDC network shown in Fig. 5.1 is modeled in PSCAD using the EMTP approach. A pole-to-ground fault with a fault resistance $R_f$ is applied at 100 km away from terminal 1. This fault distance was arbitrarily chosen and represents not the worst case. The effect of the distance on the fault current will be shown in the following study by varying the fault resistance, which has a much higher impact than the smaller cable resistance of the faulted cable section. The highest fault current would occur during a busbar fault, which is, however, a very unlikely fault scenario.

The converters are modeled as a $\pm 320$ kV bipolar half-bridge based VSC topology with concentrated midpoint-grounded DC capacitors $C_{cap}$ at each terminal as presented in Section 4.1.

The equivalent model as described in Section 4.2 is used for the adjacent AC networks. Terminal 1 is operated in rectifier mode with a secondary winding voltage of the converter transformer of 237 kV and terminals 2 and 3 are operated as inverters with 213 kV at the AC side of the converter.

5.1.3 Results and Discussion

The simulations are performed in PSCAD using a time step of 10 $\mu$s. The following paragraphs describe and discuss the results of the sim-
5.1 Contribution of Fault Current Sources

Figure 5.1: Network layout with different fault feeding sources: (A) DC capacitor, (B) adjacent feeder cable, (C) AC infeed at terminal 3, (D) AC infeed at terminal 1

ulation. First, the base case is presented and then the key parameters are varied to explain their influence on the fault current in the CB.

Base Case

The base case assumes a constant fault resistance $R_f$ of 7 $\Omega$, which corresponds to the ground resistance of a sparking ground connection in wet loamy sand at the current peak of 19.35 kA [WLD05]. The dependence of the fault resistance on the fault current is neglected in all the simulations, as well as the sheath impedance, which might be present after the fault occurrence for a very short time. The base case value of the DC capacitor is 100 $\mu$F and the DC pole reactor is neglected in the base case. The SCR of the adjacent AC networks at the PCC is assumed to be 10 for each terminal.
The cables are initially at rest at 320 kV and no current is flowing. This simplification is justified by the negligible influence of the initial steady-state current on the transient peak current. Figures 5.2 and 5.3 illustrate the development of the fault current in the CB (solid line) and distinguish the different fault current contributors as labeled in Fig. 5.1: A) DC capacitor, B) adjacent feeder cable, C) AC infeed at terminal 3, and D) AC infeed at terminal 1. The contributions (A) and (D) are determined easily by measuring the corresponding currents in the capacitor and at the output of the converter bridge, respectively. To determine the contributions from the neighboring feeder capacitance (B) and the remote terminal (C), however, the measured current at the receiving end of the adjacent feeder has to be further broken down based on two sequent simulations: first with terminal 3 connected to the system and second without terminal 3 (only with the filter capacitor connected to the remote end). The direct measurement of the AC infeed at terminal 3 (D) with a single simulation run is not possible due to the time delay and distortion introduced by the line connecting terminal 3 and 1. The fault occurs at time $t = 0$ ms. As shown in Fig. 5.2, the fault appears at terminal 1 after a short delay (about 0.5 ms) given by the line length of 100 km between fault and terminal 1. The first peak corresponds to the discharge of the DC capacitor at the arrival of the negative voltage surge generated at the fault location. The subsequent peaks originate from the forward and backward traveling initial surge. After the second peak at around 2.5 ms, a sudden decrease of the CB current can be observed, which arises from a positive surge from terminal 2 transmitted through the fault.

The first 5 ms are dominated by the capacitive discharge current contributions as depicted in Fig. 5.3 (areas A) and B)), which gives an overview of the first 100 ms after fault occurrence. The surge propagates through the busbar into the neighboring feeder and its cable capacitance is discharged through the busbar into the faulted cable. Due to the distributed nature of the neighboring feeder capacitance, the cable is discharged gradually as the negative voltage
5.1 Contribution of Fault Current Sources

Figure 5.2: Breaker current contributions, zoomed - A): DC capacitor, B): adjacent feeder cable, C): AC infeed at terminal 3, D): AC infeed at terminal 1, solid line: total CB current

surge propagates through the cable towards terminal 3. Note that the adjacent feeder contribution (area B in Figures 5.2 and 5.3) includes the contribution of the concentrated DC capacitor at terminal 3. The DC capacitor and the adjacent feeder cable capacitance are discharged simultaneously. The lumped DC capacitance is the dominant contributor during the first few milliseconds, whereas the cable capacitance contribution is larger afterwards due to its distributed nature.

After 10 ms, the capacitive discharge contributions fade out and a steady-state period dominated by the AC infeed at terminals 1 and 3 begins (c.f. areas C) and D)). The AC infeed starts as soon as the DC voltage drops below the voltage of the AC side of the converter and the freewheeling diodes become conducting. Current from the AC side is injected into the DC network through one or two diodes (depending on the phase of the AC voltages and the magnitude of the DC voltage) in the upper half and a return path is
set up through the grounded filter midpoint and one or two diodes in the lower half of the 6-pulse bridge. This results in a phase-to-phase fault or two simultaneous phase-to-phase faults as seen from the AC side. The current contribution from the AC side rises slower compared to the capacitor discharge contributions as it is limited by the AC impedance.

All terminals connected to the busbar with the faulted feeder also contribute to the fault current in CB1. DC capacitor discharge and AC current feeding start once the voltage surge arrives at terminal 3. The reflected surge plus the discharge current and the AC current travel to terminal 1 and superpose the current in CB1 as depicted in Fig. 5.2 (area C). A higher delay for the AC infeed at terminal 3 as compared to terminal 1 can be observed due to the travel time of the initial negative voltage surge on the line between terminals 1 and 3 after having passed through the busbar, and the travel time back to terminal 1. Over the whole simulation period, the contribution from
5.1 Contribution of Fault Current Sources

Terminal 3 is smaller than the contribution from terminal 1, because of the long cable of 300 km and, consequently, higher attenuation.

After 30 ms, a 300 Hz ripple from the converter 6-pulse bridge is visible (c.f. Fig. 5.3). During this period, the cable and filter capacitances are periodically charged and discharged. The charging of the capacitances (negative currents) is truncated in Figures 5.2 and 5.3, since it does not contribute to the CB current.

Dependence of Fault Current on Fault Resistance

![Graph](image)

**Figure 5.4:** Contributions from fault current sources to the maximum CB current within 5 ms; ○: maximum CB current, □: DC capacitor, △: adjacent feeder, ◊: AC infeed at terminal 1

Fig. 5.4 illustrates the dependence of the maximum fault current in CB1 on the fault resistance. The maximum values within 5 ms of the CB current and its contributions from the individual components are given for certain values of the fault resistance. The other system parameters are kept equal to the base case. The short simulation period is chosen in order to account only for the initial discharge peaks with the highest $di/dt$. Depending on the SCR of
the AC network, the CB current may increase up to much higher values at a later point in time. As can be seen in Fig. 5.4, low values for the fault resistance result in high peak currents during the first 5 ms after fault occurrence. This is due to the larger voltage drop initiated at the fault location given the lower fault resistance. The DC capacitor has the highest contribution amongst all fault current contributors for the whole range of fault resistance as the capacitor discharging is the dominant process during the first few milliseconds. Note that the adjacent feeder contribution in Fig. 5.4 includes the AC infeed at terminal 3, which has a marginal share in this simulation. At very high values of fault resistance (> 50 Ω), the DC capacitor is the only contributor to the fault current in the CB (neglecting a minor contribution from the adjacent feeder) and the AC infeed contribution decreases to zero. To explain this fact, the time-to-peak-current has to be considered, i.e. which surge of
the forward and backward traveling wave leads to the maximum current. As the DC capacitor discharge current after the first surge decreases rather slowly given the high DC capacitance in this simulation, the subsequent discharge current is superposed on the first one and depending on the magnitude of the second negative voltage surge, i.e. the fault resistance, the second discharge current peak might be higher than the first one. The magnitude of the second surge at terminal 1 depends on the reflection coefficient at the fault location and thus, on the fault resistance. For zero fault resistance, the reflection coefficient is -1 (c.f. Equation (3.2) and Fig. 3.14) and, hence, the entire wave is reflected back to terminal 1, but with opposite sign. For very high fault resistances, the reflection coefficient tends to 0 and the surge is entirely transmitted through the fault towards terminal 2. Low fault impedances up to 50Ω result in a high reflection coefficient and, thus, the second surge is responsible for the maximum current in the CB as indicated in Fig. 5.4. At this time, the current from the AC side has already increased and contributes a small share to the total CB current. During high impedance fault conditions (> 50Ω), however, the first surge leads already to the maximum current in the CB. The AC infeed current has not increased yet due to the high AC inductance and the DC capacitor current is the only contributor to the CB current. Fig. 5.5 depicts the CB current waveforms for fault resistances of 0.5, 20, and 100Ω and illustrates the above stated.

**Influence of DC Capacitor on Fault Current**

The maximum fault current in the CB increases almost linearly with the value of the DC capacitance as depicted in Fig. 5.6. For very low filter capacitances, such as in MMC topologies, only the AC infeed and the adjacent feeder contribute to the initial fault current in the CB. Note that the adjacent feeder contribution in Fig. 5.6 includes the AC infeed at terminal 3. As indicated in Figures 5.6 and 5.7 (left), the time-to-peak-current is higher than in converter topologies with large DC capacitors and corresponds approximately
to the fourth surge at $t = 7\tau$, where $\tau$ corresponds to the travel time on the cable from the fault to terminal 1. For DC capacitances above $7 \mu F$, the first surge leads to the maximum current in the CB and, hence, the capacitor has the largest share on the total current as shown in Fig. 5.7 (center). During the first DC capacitor discharge peak, the adjacent AC network does not feed the fault yet, which results in zero AC side contribution for a certain range of DC capacitor sizes as indicated in Fig. 5.7.

For even higher values above $50 \mu F$, the second negative voltage surge at $t = 3\tau$ produces the maximum current and, consequently, the contribution from the AC infeed is higher compared to DC capacitors with $10 - 20 \mu F$. In general, the second negative voltage surge is responsible for the maximum current in case of high values of the DC capacitance, because the second capacitor discharge peak is superposed on the still high first discharge current given the increased capacitor time constant (c.f. Fig. 5.7, right).
5.1 Contribution of Fault Current Sources

Figure 5.7: Breaker current contributions for $C_{\text{cap}} = 0.5 \mu F$ (left), $C_{\text{cap}} = 20 \mu F$ (center), $C_{\text{cap}} = 100 \mu F$ (right) - A): DC capacitor, B): adjacent feeder cable, C): AC infeed at terminal 3, D): AC infeed at terminal 1

Influence of AC Short Circuit Capacity

As shown in Fig. 5.8, a variation of the SCR at the PCC has no influence on the first peaks within 5 ms, as they are exclusively originated in the discharge of the DC capacitor and cable capacitance. A higher SCR, however, results in a higher steady-state fault current of up to 12 p.u. in case of a strong AC network with a SCR of 20.

Influence of Neighboring Feeder Length

The length of the neighboring feeder at the busbar of terminal 1 determines the delay of the contribution of terminal 3 to the CB current. It also has an impact on the duration of the cable capacitance discharge. The longer the cable is, the later the contribution from terminal 3 appears and the longer the cable capacitance discharge into the fault lasts, which depends on the travel time of the surge. The cable discharge starts as the forward traveling negative
Figure 5.8: Influence of the SCR at the PCC on the development of the fault current in the DC CB

Voltage surge penetrates into the feeder via busbar and ceases after twice the travel time on the cable between terminals 1 and 3, when the positive backward traveling voltage surge arrives again at terminal 1.

**Influence of DC Pole Reactor**

DC pole reactors serve multiple purposes such as DC current filter or FCL in series with the CB. The latter is needed to limit the rate of rise of the fault current in hybrid HVDC CBs, such that the current does not exceed the CB's maximum breaking current capability within the breaking time. For a maximum rise of the fault current of $3.5 \text{kA}/\text{ms}$ in a 320 kV MTDC with 10\% overvoltage, a 100 mH DC pole reactor is required [CBHJ12]. Fig. 5.9 illustrates the influence of the pole reactor $L_r$ on the CB current development within the first 10 ms after fault occurrence for various reactor sizes. A higher inductance reduces considerably the rate of rise of the current during the capacitive discharge dominated period. The peak of the
prospective CB current within the considered time frame is reduced and delayed. A larger DC reactor also reduces the steady-state fault current level, increases, however, the systems time constant and deteriorates the performance of the converter control.

$$L_r = 0 \text{ mH}$$
$$L_r = 10 \text{ mH}$$
$$L_r = 100 \text{ mH}$$
$$L_r = 200 \text{ mH}$$
$$L_r = 300 \text{ mH}$$

Figure 5.9: Influence of the DC pole reactor $L_r$ on the development of the fault current in the DC CB

5.1.4 Conclusions

This section has illustrated the contribution from each network component to the fault current in a DC CB and has explained their dependencies on the network parameters. Simulations have been performed in a simple, radial HVDC network using PSCAD. The results have shown that filter and cable capacitance discharges are dominant during the first 10 ms, whereas the AC infeed contributions from terminal 1 and 3 are dominantly present after about 10 ms. Measures to reduce the first peaks from capacitive discharges are: the reduction of the DC capacitors’ size (including filter capacitors), i.e. change of the converter topology, the limitation of the number of
feeders per busbar to reduce the cable contributions to the CB fault current, and the increase of the pole reactor size to limit the rate of rise of the discharge current. In order to reduce the maximum CB current during the later AC infeed dominated period, the converter topology has to be changed to a full-bridge configuration that allows the control of the AC infeed, but does not isolate the faulty cable branch in a MTDC network. Alternatively, the phase reactor between the converter and the transformer has to be increased to reduce the rate of rise of the AC infeed and the number of DC feeders per busbar has to be limited to reduce the contributions from the AC side at remote terminals.

Converter topologies with low DC capacitor requirements are favorably in terms of maximum CB current and time-to-peak within 5 ms, but still have the disadvantage of high contributions from the AC infeed after several tens of milliseconds and, thus, high CB currents that have to be interrupted. The rate of rise of the CB current is comparable to converter topologies with large DC capacitors due to the similar behavior of the distributed cable capacitance. This capacitance of neighboring feeder cables is crucial. The higher the number of feeders at the same bus, the higher the capacitance discharge contribution during the first period.

Foreseeable DC CBs will require additional fault clearance support, such as FCLs, e.g. inductance in series with the CB.

To estimate the minimum CB requirements \( (di/dt \text{ and peak current}) \), zero DC capacitance has to be assumed and the initial discharge current from adjacent feeders has to be calculated.

## 5.2 Comparison of Cables and OHLs

### 5.2.1 Introduction

The breakdown of the fault current into individual contributions as presented in Section 5.1 allows for a detailed analysis of the influence of the component parameters and fault condition on the total
fault current in the DC CB. It enables the specification of DC CB requirements and fault detection mechanisms, as well as the identification of measures to reduce the transient overcurrent. In addition to the previous section, this section compares the results of the cable system with those of an OHL system. It illustrates the sensitivities of the key parameters in different scenarios, which consider the transmission technology, i.e. OHL or cable, the converter technology including the required DC filters, and the fault condition. The influence of the key parameters, such as fault impedance and fault location, is described rather qualitative than quantitative. Moreover, the resulting maximum CB currents are compared for various CB technologies and corresponding current interruption times.

To do so, simulations in PSCAD-EMTDC of pole-to-ground faults in a simple, bipolar, radial three-terminal HVDC system are performed and analyzed. This is the simplest possible layout including all available components, which are able to contribute to the fault current in the CB. The emphasis in this section is again on pole-to-ground faults.

### 5.2.2 Simulation Setup

**Converter and Network Model**

The same 3 terminal radial HVDC grid with either cable or OHL interconnections as presented in the previous section (Fig. 5.1) is modeled in PSCAD using the EMTP approach. A pole-to-ground fault with a fault resistance $R_f$ is applied again 100km away from terminal 1. The converters are modeled as default ±320 kV 900 MW bipolar half-bridge based VSC converters with concentrated midpoint-grounded DC capacitors at each terminal as described in Section 4.1. In case of OHL connections, the distance between the positive and negative pole is assumed to be large and the capacitive coupling of the poles, which may induce voltage surges on the healthy pole [Hin70], [Kim70], is neglected.

The PSCAD implementation of the converters used in this study
consists of a constant voltage source for the initial steady-state operation and a transient model comprising the freewheeling diodes only as presented in Section 4.1. The threshold of the fault detection is set to a small value of $1.5 \cdot 10^{-6} \text{kA/\mu s}$, at which the converter model is switched from the steady-state model to the transient model. The adjacent AC networks are modeled by their equivalent circuit as presented in Section 4.2. Terminal 1 is operated in rectifier mode and terminals 2 and 3 are operated as inverters with a secondary winding voltage of each converter transformer of 213 kV.

**Cable and OHL Models**

This study is based on the default cable and OHL models as presented in Sections 4.4.1 and 4.4.2, respectively.

**5.2.3 Results and Discussion**

Simulations have been performed using a time step of $10 \mu s$. The DC capacitor size, the fault resistance, and the SCR at the PCC are varied using both transmission technologies. A comparison of the parameter sensitivities of OHL and cables is presented in the following paragraphs.

**Comparison of Line Parameters**

Table 5.1 compares the line parameters of the cable and OHL at 0.001 Hz, which have been extracted using the PSCAD Line Constants Program. The longitudinal losses $R$, the transversal losses $G$, and the capacitance $C$ of the two transmission technologies reveal the largest differences. The conductor in the cable has a larger cross section and is made of copper instead of aluminium/steel, which results in lower longitudinal losses compared with the OHL. The capacitance and the transversal losses of the cable, however, are two orders of magnitude larger than in the OHL due to the cable design with XLPE insulation and screen. The resulting propagation velo-
### Table 5.1: Comparison of OHL vs. Cable Parameters at 1 mHz

<table>
<thead>
<tr>
<th>Parameter</th>
<th>OHL</th>
<th>Cable</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R$ [$\Omega$/km]</td>
<td>0.0578</td>
<td>0.0123</td>
</tr>
<tr>
<td>$X$ [$\Omega$/km]</td>
<td>$2.03 \cdot 10^{-5}$</td>
<td>$2.17 \cdot 10^{-5}$</td>
</tr>
<tr>
<td>$G$ [$S$/km]</td>
<td>$1.0 \cdot 10^{-8}$</td>
<td>$1.0 \cdot 10^{-6}$</td>
</tr>
<tr>
<td>$B$ [$S$/km]</td>
<td>$5.29 \cdot 10^{-11}$</td>
<td>$1.18 \cdot 10^{-9}$</td>
</tr>
<tr>
<td>$v_0$ [km/s]</td>
<td>$3.0 \cdot 10^3$</td>
<td>$1.98 \cdot 10^5$</td>
</tr>
<tr>
<td>$\tau_{100km}$ [ms]</td>
<td>0.33</td>
<td>0.5</td>
</tr>
<tr>
<td>$\mu$</td>
<td>9.56</td>
<td>4.44</td>
</tr>
<tr>
<td>$\nu$</td>
<td>8.37</td>
<td>-0.87</td>
</tr>
</tbody>
</table>

The velocity of the quasi TEM-mode $v_0$ is about 100% of the speed of light in the OHL and around 66% in the cable. The traveling delays for 100 km are indicated by $\tau_{100km}$ for both transmission media. The indicator $\mu = 0.5 \cdot (\alpha + \beta)$ is a measure for the damping of the amplitude of a traveling wave introduced by the losses and $\nu = 0.5 \cdot (\alpha - \beta)$ is an indicator for the distortion of the wave shape. $\alpha = R/L$ is the inductive and $\beta = G/C$ the capacitive damping factor as defined in [MM01]. The OHL exhibits a higher damping, but less distortion of the wave shape, i.e. the wave fronts are not flattened as much as in the cable. For a distortionless transmission line, the Heaviside condition $\nu = 0$ has to be fulfilled [MM01].

### Base Case

The base case assumes a constant fault resistance of 5 $\Omega$, DC capacitors of 50 $\mu$F at each terminal, and an SCR of the AC system at each PCC of 20.

Fig. 5.10 illustrates the simulation results of the base case for a cable system (upper graph) and OHL system (lower graph). The plots show the superposition of the individual fault current contributions of the DC capacitor (A), the adjacent feeder capacitance and the filter capacitor at terminal 3 (B), the AC infeed at the remote terminal.
The pole-to-ground fault occurs at 0 ms. Discharge of concentrated DC capacitors and distributed feeder capacitance is dominant during the first 10 ms. Thereafter, the capacitive discharges fade out and the main fault current contributors are the infeed from the AC side at terminals 3 and 1. The DC capacitors are periodically charged by the AC infeed and discharged into the fault. Note that the negative current (capacitor charging) is truncated in Fig. 5.10, since it does not contribute to the CB current. During the second period after 10 ms, a 300 Hz ripple is visible that is injected from the converters acting as 6-pulse rectifiers. The main differences between cables and OHL are found in the maximum steady-state fault current in the CB after 100 ms, which is about 14 kA in the cable and about 11 kA in the OHL system for this base case. The maximum steady-state fault current is determined by the series line impedance and, therefore, the OHL connections, which have a higher impedance than the cables, yield lower fault current values. Moreover, the capacitive discharge dominated first period exhibits a distinct behavior in the two transmission technologies: the cable is dominated by large discharge peaks with high di/dts from the DC filters, whereas the OHL connections lead to much smaller filter discharge peaks using the same filter size as in the cable system. Although the distortion of the negative voltage surges is lower in OHLs as compared to cables (c.f. Table 5.1) and one would expect higher dv/dts leading to larger capacitor discharge currents, the OHL yields lower capacitor current contributions than cables due to the larger damping in the system. The frequency of the subsequent discharges, however, is higher in the OHL given the higher surge propagation $v_0$ speed as compared to the cable (c.f. Table 5.1). Also the fault current contribution of the adjacent feeder at the bus at terminal 1 is much lower in the OHL system due to its relatively low capacitance.
5.2 Comparison of Cables and OHLs

Influence of DC Capacitor

The size of the DC capacitor has been varied between 0.1 $\mu$F and 100 $\mu$F. The fault resistance is kept constant at 5 $\Omega$. Fig. 5.12 shows the fault current contributions during the first 10 ms after the ground fault has occurred for the lowest (upper row) and highest capacitor size (lower row) and the two transmission technologies: cable (left column) and OHL (right column). Generally, a change in the DC capacitor size has no impact on the steady-state fault current, but only on the first, capacitive discharge dominated period. In both, cables and OHLs, very small DC capacitors yield a negligibly small contribution to the overall fault current in the CB. In the case of
cables, the first peak is dominated by the discharge of the distributed capacitance of the adjacent feeder cable to terminal 1. In OHLs, only the AC infeed at terminal 1 contributes to the CB current, which increases rather slowly due to the limiting AC impedance.

If large capacitors are installed, the cable exhibits the characteristic discharge pattern with a first peak from the initial negative voltage surge at 0.5 ms, a second peak at 1.5 ms from the second negative voltage surge, which corresponds to the reflected surge (reflected at the fault location), and a subsequent decrease in the capacitor current at 2.2 ms due to an incident positive voltage surge. This positive surge originated at terminal 2 from the incident initial negative surge and was then transmitted through the ground fault

**Figure 5.11:** Fault current contributions: (A) DC capacitor, (B) adjacent feeder cable, (C) AC infeed at terminal 3, (D) AC infeed at terminal 1
location to terminal 1. The following gradually decreasing peaks correspond to the subsequent arrivals of the surges at the terminal.

The OHL leads to a series of superposing small capacitor discharges. The maximum of the DC capacitor contribution occurs later at around 3 ms and is smaller than in the cable. Generally, a change in the capacitor size has less influence on the CB current development in the OHL than in the cable.

![Figure 5.12: Fault current contributions: (A) DC capacitor, (B) adjacent feeder cable, (C) AC infeed at terminal 3, (D) AC infeed at terminal 1](image)

As shown in Fig. 5.10, the fault current in the CB increases over time due to the increasing contribution of the AC networks at terminals 1 and 3 given the SCR of 20 at both PCCs. This results in higher breaking currents for slower CBs. The size of the DC capacitor, however, has only an impact during the first few milliseconds and, therefore, the maximum values of the prospective fault current
in the CB within 2 ms for various capacitor sizes between 0.1 and 100 µF are investigated and depicted in Fig. 5.13. The height of the bars represents the maximum breaking currents, which a fast hybrid DC CB [HJ11] would have to cope with. In the OHL system (dashed bars), the maximum CB current saturates beyond 50 µF at around 4 kA and the DC capacitor is the only fault current contributor. As the size of the DC capacitor decreases, the contribution of the AC infeed at the closest terminal (terminal 1) increases. For the lowest value of the capacitor, the AC infeed is the sole CB fault current contributor. The maximum CB currents always occur 2 ms after fault occurrence, which is the upper limit of the considered time frame in this case.

A distinct pattern can be seen in the cable system (solid bars). Its resulting maximum CB currents within 2 ms are higher and, in contrast to the OHL system, the adjacent feeder has a considerable share on the total fault current, particularly for the smallest capacitor size and sizes above 60 µF. Unlike in the OHL system, the maximum values of the CB current in a cable system occur earlier than 2 ms, except for the maximum in case of the smallest capacitor size. For capacitors with less than 60 µF, the maximum occurs at 0.5 ms when the first negative surge arrives and the DC capacitor is the main fault current contributor. For larger values of more than 60 µF, the second surge leads to the maximum CB current at 1.5 ms and a large contribution of the adjacent feeder, as well as a small contribution of the slowly increasing AC infeed is visible.

**Influence of Fault Resistance**

To investigate the influence of the fault resistance, its value is varied as done with the DC capacitance in the previous paragraph. The DC capacitor is kept constant at 50 µF. Fig. 5.14 illustrates the CB current development during the first 10 ms for a very small impedance (upper row) and a high-impedance fault (lower row). The level of the CB current decreases in both transmission media for increasing fault resistance. In case of a low fault resistance, the cable exhibits
5.2 Comparison of Cables and OHLs

Figure 5.13: Maximum CB current within 2ms in cable (solid bars) and OHL (dashed bars) for various capacitor sizes - black: DC capacitor contribution, red: adjacent feeder contribution, green: AC infeed at terminal 1

a considerably higher CB current than the OHL, whereas the results of the two transmission technologies do not differ significantly during a high-impedance fault. A small fault resistance results in a high reflection coefficient and yields, therefore, a higher peak of the second capacitor discharge as compared with the high-impedance fault. This effect is particularly visible in the cable system in Fig. 5.14 (left column). As the reflection coefficient decreases with increasing fault resistance, the transmission coefficient increases accordingly and, consequently, the sudden decrease due to the positive voltage surge at 2.2ms becomes more accentuated (c.f. Fig. 5.14 lower left graph).

The maximum CB currents within 2ms are given in Fig. 5.15 with solid bars for the cable system and dashed bars for the OHL system for various values of the fault resistance between 0.1 and
100 Ω. For both transmission technologies, the total CB current decreases with increasing fault resistance. The DC capacitor is the only contributor in the cable system for fault resistances above 20 Ω and throughout the variation range in case of OHL lines. The reason for that are again the decreased reflection coefficient for higher fault resistances and, therefore, a lower second capacitor discharge peak, which, in contrast to the first peak, could also comprise other current contributions than from the filter itself. The maximum values of the CB current in cables and OHLs converge to the same value for a very high fault resistance as it becomes dominant over the line resistance. The sensitivity of the maximum value on the fault resistance is again smaller in OHL than in cable systems.

Figure 5.14: Fault current contributions: (A) DC capacitor, (B) adjacent feeder cable, (C) AC infeed at terminal 3, (D) AC infeed at terminal 1
5.2 Comparison of Cables and OHLs

Figure 5.15: Maximum CB current within 2 ms in cable (solid bars) and OHL (dashed bars) for various fault resistances - black: DC capacitor contribution, red: adjacent feeder contribution, green: AC infeed at terminal 1

Influence of AC SCR

A variation of the SCR of the AC system at the PCCs has no impact on the first, capacitive discharge dominated period up to 5 ms as depicted in Fig. 5.16. It has, however, a considerable influence on the level of the steady-state short-circuit current in the CB, when the AC infeed is the main contributor. An increase of the SCR affects OHL and cable systems similarly. The additional increase of the fault current due to an increase in the SCR becomes lower towards higher values of the SCR.

5.2.4 Conclusions

In this section, the fault current through a DC CB has been broken down into the individual contributions of the fault current feeding
components and the dependencies of each contributor on key parameters. The results have shown that the filter and line capacitance discharges are the dominant contributors in the first 10 ms, during which the cable and OHL show distinct discharge patterns. The cables exhibit larger DC capacitor and cable capacitance contributions compared with the OHL due to lower damping (lower $R$) and higher cable capacitance, respectively. Smaller capacitor discharge peaks are seen in OHL connections, but with a higher frequency given the higher propagation speed. After 10 ms, the AC infeeds at terminals 1 and 3 are exclusively present and the OHL system yields a slightly lower fault current level due to the higher resistivity compared with the cable.

The CB fault current in a cable system has demonstrated high
sensitivity to a change of the DC capacitor size and the fault resistance, whereas the influence of these parameters is negligible in OHL systems. An increase in the SCR of the adjacent AC networks at the PCC affects only the steady-state fault current and shows a similar impact on both transmission technologies.
6 Analytic Approximation of Fault Currents

6.1 Contributions from Capacitive Sources

6.1.1 Introduction

The results in the previous chapter are based on simulations performed with the PSCAD simulation software using fully detailed, frequency-dependent models for the cables and OHLs. Standardized calculations of the maximum and minimum values of current and voltage, rather than fully detailed simulations are required to ease the specification of the network components, e.g. the CBs. Standard calculation procedures exist for short-circuit currents in HVAC systems, but not yet for HVDC networks. A summary of technical guidelines and pre-standardization studies for such HVDC grids has been published in [ACF14]. Recently, the IEC 61660 standard for medium voltage DC systems [IEC97] has been used for short-circuit current calculations in HVDC systems [WJB13]. This standard provides calculation rules of the short-circuit currents in small low and medium voltage auxiliary networks. It simplifies, however, the lines of the network to lumped frequency-independent series impedances, which is a valid assumption for medium voltage networks with short interconnections and small line capacitances. In an HVDC network, however, the capacitance cannot be neglected. The wave shape of the propagating surges is distorted, particularly, in systems with long cable interconnections. Hence, the lines have to be represented by distributed, frequency-dependent parameters and the skin effect has to be taken into account. The IEC 61660 standard yields only
good results for HVDC networks under the following conditions: the lines are relatively short and the DC capacitor, as well as the pole reactor are large, so that the lumped elements (capacitor and reactor) become dominant over the frequency-dependent, distributed line parameters. This effect is illustrated in Fig. 6.1 for different sets of line length and DC capacitor size.

![Image of DC Capacitor Currents](image)

**Figure 6.1:** IEC results (blue) compared with simulations (red) - top: \( l = 10 \text{ km}, C_{\text{cap}} = 100 \mu \text{F}; \) middle: \( l = 100 \text{ km}, C_{\text{cap}} = 100 \mu \text{F}; \) bottom: \( l = 10 \text{ km}, C_{\text{cap}} = 1 \mu \text{F} \)

This section proposes new expressions for the approximation of overcurrents in HVDC cable networks based on individual surges and the planar skin effect. The derived approximations, however, can also be applied to OHL based systems. Results are only shown for the cable system due to its higher fault current levels [BF13a].
6.1 Contributions from Capacitive Sources

Approximations are given for the individual contributions from DC capacitors at the DC side of the converters and neighboring feeders at the same busbar as the faulted cable. The contribution from the AC side, which is present in a half-bridge based converter, is neglected in this study, since the main focus is on the initial transient period during the first few milliseconds after fault occurrence. During this period, the capacitive contributors are dominant and result in the highest rates of rise of the fault current [BF13b].

6.1.2 Setup for Benchmark Simulations

A description of the PSCAD models used in the benchmark simulations for the validation of the approximative calculations of the prospective short-circuit current in the CB is presented in this paragraph.

Network Model

The network used in the simulations is illustrated in Fig. 6.2. A solid pole-to-ground fault occurs at a certain distance to the CB under study. The faulted cable is connected to a DC busbar together with an additional feeder representing a meshed DC grid. A DC capacitor comprising the converter capacitors and possible tuned filter capacitors is installed between the converter and the DC busbar. The converters can be omitted in the transients simulations, since they are assumed to have full-bridge configuration and are blocked immediately after detection of the fault yielding the equivalent circuit diagram shown in Fig. 6.3. The contributions to the CB current $i_{cb}$ are the DC capacitor current $i_c$ and the adjacent feeder current $i_f$. The cables are represented by their characteristic impedance $Z_0(\omega)$. 
6 Analytic Approximation of Fault Currents

The default cable model and parameters presented in Section 4.4.1 are used in this study.

6.1.3 Derivation of Analytic Expressions

The basics for the derivation of analytic expressions of fault surges is the well-known traveling wave theory, which implies the following partial differential equations for the voltage $v$ and current $i$ at the point $x$ on the cable:

\[
Z_0(\omega) i_f + i_{cb} Z_0(\omega) = 0
\]

\[
v_c = \frac{1}{C_{cap}} \int i_c dx
\]
\[ -\frac{\partial v}{\partial x} = L \frac{\partial i}{\partial t} + Ri \] (6.1)
\[ -\frac{\partial i}{\partial x} = C \frac{\partial v}{\partial t} + Gv \] (6.2)

with the cable resistance \( R \), inductance \( L \), capacitance \( C \), and shunt conductance \( G \). The transformation into the Laplace domain yields

\[ \frac{dV}{dx} = -Z(s)I \] (6.3)
\[ \frac{dI}{dx} = -Y(s)V \] (6.4)
\[ Z(s) = R + sL \] (6.5)
\[ Y(s) = G + sC \] (6.6)

where \( Z(s) \) is the cable impedance and \( Y(s) \) the cable admittance. Rearrangement of these equations results in independent expressions for the voltage and the current

\[ \frac{d^2V}{dx^2} - k^2(s)V = 0 \] (6.7)
\[ \frac{d^2I}{dx^2} - k^2(s)I = 0 \] (6.8)

with the propagation constant \( k(s) \) defined as

\[ k(s) = \sqrt{Z(s) \cdot Y(s)} \] (6.9)

The solutions of the second order differential equations (6.7) and (6.8) are

\[ V(x,s) = V^+(s)e^{-k(s)x} + V^-(s)e^{k(s)x} \] (6.10)
\[ I(x,s) = \frac{1}{Z_0(s)} \left[ V^+(s)e^{-k(s)x} - V^-(s)e^{k(s)x} \right] \] (6.11)

which is the superposition of the forward and backward traveling
waves with the initial amplitudes $V^+(s)$ and $V^-(s)$, respectively, and the characteristic surge impedance $Z_0(s)$ defined as

$$Z_0(s) = \sqrt{\frac{Z(s)}{Y(s)}}.$$  \hfill (6.12)

The closed-form solution of the back-transformation into the time domain for constant, frequency-independent cable parameters can be found in [MM01]. In the following, the back-transformations for frequency-dependent cable parameters considering the skin effect are derived.

**Frequency-Dependence of Parameters**

![Graph showing frequency-dependent cable resistance and inductance](image)

**Figure 6.4:** Frequency-dependent cable resistance (blue, dotted line) and inductance (red, solid line)
The frequency dependence of the cable parameters are investigated in the frequency range from 1 mHz to 1 MHz using the PSCAD Line Constants Program. The shunt parameters of the capacitance $C$ and the conductance $G$ are practically frequency-independent. The resistance $R(f)$ reveals the highest dependence on the frequency over the whole frequency range of this study as illustrated in Fig. 6.4 (dotted line). This is due to the skin effect, i.e. the displacement of the current to the surface of the inner conductor at high frequencies and corresponding small penetration depths causing an increase of the effective resistance. Fig. 6.4 depicts also the cable inductance $L(f)$ (solid line), which is zero at $f = 0$ Hz (not visible in Fig. 6.4) and reveals a peak in the low frequency range below 1 Hz. For frequencies above 1 Hz, the inductance is almost constant and decreases only slightly with increasing frequency.

**Short-Circuited, Infinitely Long Cable**

In the first step of the derivation of an analytic expression for the distortion of the wave shape, an infinitely long cable that is short-circuited at one end as depicted in Fig. 6.5 is analyzed. A closed-form expression for the timely development of the current $i_x(x,t)$ and the voltage $v_x(x,t)$ at any point $x$ on the cable shall be derived.

\[ Z_0 \]

\[ i_x \]

\[ v_x \]

\[ \text{Faulted Feeder} \]

\[ \text{Ground Fault} \]

**Figure 6.5: Discharge of infinite long line**
As described in Section 6.1.3, only the cable resistance exhibits a strong frequency dependence, whereas the other parameters remain almost constant over the frequency range of interest. The ground fault initiates a negative voltage surge with a very steep wave front, which results in high frequencies. Even if the wave fronts are flattened out during the propagation through the cable, as well as after the reflection at the DC capacitor, the dominant frequency content is still above the frequency range, where the cable inductance shows a high dependence (c.f. Fig. 6.4). Therefore, only the resistance is modeled as a frequency dependent parameter. Due to the high frequency content of the traveling waves, the penetration depth is much smaller than the diameter of the conductor and it is assumed that the current flows through an indefinitely thin layer at the surface of the conductor. This so-called planar skin effect impedance is proportional to the square root of the frequency [WN57]. In general, XLPE cables exhibit a very low DC resistance of the inner conductor and negligible dielectric losses as indicated in Section 6.1.3 and, therefore, the DC resistance and the shunt conductance can be neglected. Hence, the cable impedance and admittance can be described in the Laplace domain as

\[
Z(s) = L \cdot s + K \cdot \sqrt{s}, \quad (6.13)
\]

\[
Y(s) = C \cdot s, \quad (6.14)
\]

where \(K\) represents the skin effect factor. Expanding the square root of the propagation constant \(k(s)\) and the characteristic impedance \(Z_0(s)\) by binomial expansion and truncation after the second term, one obtains the approximations [WN57]:

\[
k(s) = \sqrt{(L \cdot s + K \cdot \sqrt{s}) \cdot C \cdot s} \approx \frac{s}{c} \left(1 + \frac{K}{2L} \cdot s^{-1/2}\right) \quad (6.15)
\]

\[
Z_0(s) = \sqrt{\frac{L \cdot s + K \cdot \sqrt{s}}{C \cdot s}} \approx R_0 \left(1 + \frac{K}{2L} \cdot s^{-1/2}\right) \quad (6.16)
\]
with the characteristic cable impedance at high frequency $R_0 = \sqrt{L_{HF}/C_{HF}}$ and the propagation speed $c = 1/\sqrt{L_{HF}C_{HF}}$. The equations for the voltage and current surges in the Laplace domain are computed using (6.10) and (6.11), while considering only the forward traveling wave $V^+(s)$ and assuming an initial voltage step of magnitude $V_0$ at the fault location

$$V^+(s) = \frac{V_0}{s}$$

$$V^-(s) = 0$$

$$V(x, s) = \frac{V_0}{s} \cdot \exp \left( -\frac{x}{c} \cdot s - \frac{x}{c} \alpha s^{1/2} \right)$$

$$I(x, s) = \frac{V_0}{R_0 s (1 + \alpha s^{-1/2})} \cdot \exp \left( -\frac{x}{c} \cdot s - \frac{x}{c} \alpha s^{1/2} \right). \quad (6.17)$$

The time domain solutions are derived in [WN57] and [Mag68], respectively:

$$v_x(x, t) = V_0 \cdot \text{erfc} \left( \frac{\alpha}{2\sqrt{t-\tau}} \cdot \tau \right) \cdot \sigma(t-\tau) \quad (6.19)$$

$$i_x(x, t) = \frac{V_0}{R_0} \cdot e^{\alpha^2 t} \cdot \text{erfc} \left( \frac{\alpha}{2\sqrt{t-\tau}} + \frac{\alpha}{2\sqrt{t-\tau}} \cdot \tau \right) \cdot \sigma(t-\tau), \quad (6.20)$$

where $\alpha = \frac{K}{2L}$ is the distortion factor, $\tau = \frac{x}{c}$ the traveling wave delay, $\sigma(t)$ the unit step function, and erfc the complementary error function [AS64].

The proposed equations provide a good approximation to the high frequency behavior of a coaxial cable, where the planar skin effect is predominant [Nah62]. Other skin effect models for lower frequencies are the cylindrical skin effect [HN72] and the $f^m$-law with $0 < m < 1$ as described in [Nah62]. The general case including dielectric losses is discussed in [XZZB05] and [Nah62], and a model considering a non-zero DC resistance of the inner conductor is pre-
sented in [NH72]. However, the aforementioned models cannot be represented by closed form analytic expressions.

**DC Capacitor Contribution**

The voltage across the DC capacitor $v_c$ is equal to the sum of the forward and reflected, backward traveling wave. The corresponding expression in the Laplace domain for a ground fault at distance $l$ from the CB is:

$$V_c(s) = \left[ V^+(l, s) + V^-(l, s) \right] = \left[ V^+(l, s) + V^+(l, s) \cdot \Gamma(s) \right]$$

(6.21)

with the reflection coefficient

$$\Gamma(s) = \frac{Z_{cap}(s)}{Z_{cap}(s)} \left| \frac{R_0 - R_0}{R_0 + R_0} \right| = -\frac{s}{s + \frac{2}{CR_0}}$$

(6.22)

which depends on the characteristic impedance $R_0$ and the impedance $Z_{cap}(s) = \frac{1}{sC}$ of the capacitor with value $C$.

- Exact Transformation

The exact back-transformation into the time domain can be found using the transformation pairs in [Chu72] and the displacement law:
\[ v_c(t) = V_0 \cdot \text{erfc} \left( \frac{\alpha \tau}{2\sqrt{t - \tau}} \right) - \\
V_0 \frac{1}{2} e^{-\frac{2}{CR_0} (t-\tau)} \cdot \left[ e^{-i\alpha \tau \sqrt{\frac{2}{CR_0}}} \cdot \text{erfc} \left( \frac{\alpha \tau}{2\sqrt{t - \tau}} - i \sqrt{\frac{2}{CR_0}} (t - \tau) \right) + \\
\cdot \left[ e^{i\alpha \tau \sqrt{\frac{2}{CR_0}}} \cdot \text{erfc} \left( \frac{\alpha \tau}{2\sqrt{t - \tau}} + i \sqrt{\frac{2}{CR_0}} (t - \tau) \right) \right] \cdot \sigma(t - \tau). \]

\[ (6.23) \]

Note that the error function in (6.23) has a complex argument and requires the computation of the Faddeeva-Function denoted as \( w(z) \) in [AS64].

Hence, the capacitor current contribution \( i_c \) can be derived by

\[ i_c(t) = -C_{\text{cap}} \cdot \frac{dv_c}{dt}. \]  

\[ (6.24) \]

The minus sign in (6.24) arises from the definition of the voltage polarity of \( v_c \) as illustrated in Fig. 6.3.

- Approximation

Instead of using the lengthy equation of the exact time domain solution (6.24), an approximation based on the modification of the argument of the exponential function in the Laplace domain for the reflected voltage wave in (6.21) is proposed. To do so, the frequency \( s \) is shifted by \( \frac{2}{CR_0} \) in the nominator of
\[ V^+(l,s) \cdot \Gamma(s) = -\frac{V_0}{R_0} \cdot \exp\left(-\tau s - \tau \alpha s^{1/2}\right) \cdot \frac{1}{s + \frac{2}{CR_0}} \]
\[ \approx -V_0 \cdot e^{-\tau (s + \frac{2}{CR_0})} \cdot e^{\frac{2}{CR_0}} \cdot \frac{e^{-\tau \alpha \sqrt{s + \frac{2}{CR_0}}}}{s + \frac{2}{CR_0}}. \]

(6.25)

The error introduced by this frequency shift is compensated by the factor $e^{\frac{2}{CR_0}}$ for the first term in the exponential function, but is not corrected for the second term due to the square root of the frequency. This approximation is only valid for large $s$ compared to $\frac{2}{\tau C}$, where $\tau C = CR_0$ is the time constant of the DC capacitor. The modified equation in the Laplace domain (6.25) allows for the application of the displacement law when transforming the equation back into the time domain:

\[ v_c(t) = V_0 \cdot \text{erfc}\left(\frac{\alpha \tau}{2\sqrt{t-\tau}}\right) \cdot \left(e^{-\frac{2}{CR_0} (t-\tau)} - 1\right) \cdot \sigma(t-\tau). \]

(6.26)

One obtains the capacitor current contribution using again the time derivative of the voltage:

\[ i_c(t) = -C \cdot \frac{dv_c}{dt} = -V_0 \cdot \left[\exp\left(-\frac{\alpha^2 \tau^2}{4(t-\tau)}\right) \cdot (t-\tau)^{-\frac{3}{2}} \cdot \left(e^{-\frac{2}{CR_0} (t-\tau)} - 1\right) - \frac{2}{CR_0} e^{-\frac{2}{CR_0} (t-\tau)} \cdot \text{erfc}\left(\frac{\alpha \tau}{2\sqrt{t-\tau}}\right)\right] \cdot \sigma(t-\tau). \]

(6.27)

**Adjacent Feeder Contribution**

The contribution of the adjacent feeder cable $i_f$ at the same busbar as the faulted cable (c.f. Figures 6.2 and 6.3) can be derived in a similar way as the capacitor contribution described in the pre-
vious paragraph. The incident negative voltage surge initiated at the ground fault location is transmitted partly through the busbar into the neighboring feeder, which is consequently discharged and contributes to the total fault current in the CB. Hence, the adjacent feeder current is determined in the Laplace domain for a ground fault at distance $l$ from the CB by

$$I_f(s) = T(s) \cdot I^+(l, s) = [1 + \Gamma(s)] \cdot I^+(l, s),$$

(6.28)

where $I^+(l, s)$ is the incident current surge and $T(s)$ the transmission coefficient. The adjacent feeder is assumed to be infinitely long and, therefore, unlike in the equation for the capacitor voltage (6.21), there is no backward traveling wave that has to be considered.

- Exact Transformation

The exact transformation into the time domain is computed by partial fraction decomposition of the denominator of (6.28):

$$I_f(s) = I^+(l, s) - \frac{V(l, s)}{(1 + \alpha s^{-1/2})(s + \frac{2}{CR_0})}$$

$$= I^+(l, s) - \frac{V(l, s)}{\alpha^2 + \frac{2}{CR_0}} \left( \frac{\frac{2}{CR_0}}{\frac{2}{CR_0} + s} + \frac{\alpha s^{1/2}}{\frac{2}{CR_0} + s} - \frac{\alpha}{\alpha + s^{1/2}} \right).$$

(6.29)

The first and last term in (6.29) can be directly transformed into the time domain using the transformation pairs in [Chu72] and [CJ59], whereas the nominator and denominator of the second term have to be multiplied first by $s^{1/2}$ to be transformed, which implies the derivative of the resulting time domain solution:
\[
\frac{\alpha s}{2 CR_0 s^{1/2} + s^{3/2}} = \frac{d}{dt} \mathcal{L}^{-1} \left\{ \frac{\alpha}{2 CR_0 s^{1/2} + s^{3/2}} \right\}.
\] (6.30)

The equation in the time domain is shown in Fig. 6.6.

\[
i_f = \frac{1}{R_{01}} V_{01} (e^{a_1 t} \text{Erfc}[a_1 \sqrt{t - T_1}] + \frac{a_1 T_1}{2 \sqrt{t - T_1}} + 1/(a_1^2 - b_1) \frac{a_1 e^{-a_1^2 T_1^2}}{\sqrt{\pi} \sqrt{t - T_1}} \\
+ 0.5a_1 \left[ \frac{1}{b_1} e^{b_1(t - T_1)} \left( -\frac{2e^{-a_1 b_1(t - T_1)} + \frac{a_1 T_1}{2 \sqrt{b_1(t - T_1)}}}{\sqrt{\pi}} \right) - a_1^2 e^{a_1 t} \text{Erfc}[a_1 \sqrt{t - T_1}] \right]
\]

\[
+ \frac{a_1 T_1}{2 \sqrt{t - T_1}} + 1/\sqrt{b_1} 0.5a_1 e^{b_1(t - T_1)} (e^{-a_1 \sqrt{b_1(t - T_1)}} \text{Erfc}[-\sqrt{b_1(t - T_1)}] + 2 \frac{a_1 T_1}{2 \sqrt{b_1(t - T_1)}} \\
- e^{a_1 \sqrt{b_1(t - T_1)}} \text{Erfc}[\sqrt{b_1(t - T_1)} + \frac{a_1 T_1}{2 \sqrt{t - T_1}}] + 0.5b_1 e^{b_1(t - T_1)} (e^{-a_1 \sqrt{b_1(t - T_1)}} \text{Erfc}[-\sqrt{b_1(t - T_1)}] \\
+ \frac{a_1 T_1}{2 \sqrt{t - T_1}} + e^{a_1 \sqrt{b_1(t - T_1)}} \text{Erfc}[\sqrt{b_1(t - T_1)} + \frac{a_1 T_1}{2 \sqrt{t - T_1}}]) \text{HeavisideTheta}[t - T_1]
\]

\[
R_{01} = \frac{L_{HF}}{C_{HF}} \\
a_1 = \frac{K}{2 L_{HF}} \\
b_1 = \frac{2}{C_{DC} R_{01}} \\
T_1 = \frac{x}{c} \\
c = \frac{1}{\sqrt{LC}}
\]

**Figure 6.6:** Exact back-transformation of adjacent feeder contribution in Mathematica

- **Approximation**

  A simpler, approximative solution can be obtained again by
applying a frequency shift to $I^*(l, s + \frac{2}{CR_0})$ and corresponding correction factors, except for the square root terms, to make use of the displacement law. The resulting time domain equation is

$$i_f(t) = \frac{V_0}{R_0} \cdot e^{\alpha^2 t} \cdot \text{erfc} \left( \alpha \sqrt{t - \tau} + \frac{\alpha \tau}{2 \sqrt{t - \tau}} \right) \cdot \left( 1 - e^{-\frac{2}{CR_0}(t-\tau)} \right) \cdot \sigma(t - \tau).$$ \hspace{1cm} (6.31)

This approximation is again valid for $s \gg \frac{2}{CR_0}$.

**Total CB Current**

The total fault current during the first surge is obtained by the superposition of the individual fault current contributions from the DC capacitor and the neighboring feeder as:

$$i_{cb}(t) = i_f(t) + i_c(t).$$ \hspace{1cm} (6.32)

To consider also the subsequent surges, which have been reflected at the fault location, the travel delay in the equations for the DC capacitor current $i_c$ and the adjacent feeder current $i_f$ have to be incremented by $2 \cdot \tau$ for each new surge. The CB current including $N$ subsequent surges is then

$$i_{cb}(t) = \sum_{m=0}^{N-1} \left[ i_f(t - 2 \cdot \tau \cdot m) + i_c(t - 2 \cdot \tau \cdot m) \right].$$ \hspace{1cm} (6.33)

Note that no backward traveling surges on the adjacent feeder cable are considered here due to the assumption of an infinitely long and, therefore, reflectionless adjacent feeder.

**6.1.4 Comparison and Discussion**

In this section, the results of the analytic calculations and the benchmark simulations are compared and validated. First, the results of
a single current surge on a short-circuited, infinitely long cable are compared and later, the total CB current is evaluated for different distances to the ground fault and DC capacitor sizes.

Parameters

The required input parameters for the analytical calculations are derived from the cable model described in Section 4.4.1 evaluated at 1 MHz using the PSCAD Line Constants Program. The resulting values are: \( R = 2.886 \, \Omega/\text{km}, \) \( L = 1.531 \cdot 10^{-4} \, \text{H/km}, \) and \( C = 1.882 \cdot 10^{-7} \, \text{F/km}. \) The skin effect factor \( K \) is then computed as [Mag68]:

\[
K = \frac{R(1 \, \text{MHz})}{\sqrt{\pi} \cdot 1 \, \text{MHz}} = 1.628 \cdot 10^{-3} \, \Omega/\text{km}.
\]  

(6.34)

Single Surge

Figures 6.7 and 6.8 show the comparison of the results of the benchmark model (solid curves) and the analytic calculations (dashed curves) for a single voltage (6.19) and current surge (6.20) at various distances from the fault location. The wavefronts of the analytic expressions exhibit a very good agreement with the simulations, whereas an increasing discrepancy can be seen for increasing time. This is due to the assumptions of constant inductance and planar skin effect, which are valid at high frequencies. The wave tails, however, contain also lower frequencies and the value of the inductance becomes slightly higher, which damps the current amplitudes as seen in Fig. 6.8. At low frequencies, the skin depth increases and the square root law of the planar skin effect is not valid anymore. In general, the error of the analytic calculation is negligible during the first few milliseconds for short distances to the fault, whereas it increases with increasing distance and time.
6.1 Contributions from Capacitive Sources

Figure 6.7: Voltage at various locations on the infinitely long cable - solid curve: PSCAD simulations, dashed curve: analytic calculations

Total CB Current

To validate the analytic expression for the CB current derived in this section, a variation of the DC capacitor size $C$ and distance to fault $l$ is presented here and plots are shown for the first surge.

- Variation of DC Capacitor Size

  For a low DC capacitor size of 1 $\mu$F, the superposition of the exact back-transformations of the capacitor and feeder contributions (dotted curve) shows a very good agreement with benchmark simulations (solid curve) as depicted in Fig. 6.9. The approximative transformation (dashed curve), however, overestimates the CB current peak due to the frequency shift
introduced in the Laplace domain (6.25). To improve the approximate solution, a simple scaling factor for the capacitor contribution (6.27), which is dominant in this case, is proposed and the result for a visually estimated scaling factor of 0.88 (dashed-dotted line) is illustrated in the same plot. The adjacent feeder contribution (6.31) remains unscaled.

Fig. 6.10 illustrates the results for a large DC capacitor size of 100 µF. On the one hand, the exact transformation exhibits again a good accuracy for the wavefront, but a somehow larger discrepancy afterwards due to the smoothing of the surge by the capacitor and, consequently, a downwards frequency shift. On the other hand, the approximative solution
6.1 Contributions from Capacitive Sources

Figure 6.9: CB current for $l = 100 \text{km}$ and $C = 1 \mu\text{F}$ - Solid line: PSCAD, dotted line: exact solution, dashed line: approximative solution, dashed-dotted line: scaled approximative solution

reveals a high correlation with the temporal development of the solution of the benchmark simulations, but with a certain offset and slightly exaggerated slope of the wavefront. The same scale factor for the capacitor contribution as in the previous case is applied and the results plotted (dashed-dotted curve) in the same figure. The scaled approximation shows the best agreement for the large DC capacitor.

The relative error of the peak CB current $i_{cb}^{\text{max}}$ during the first surge of the analytic expressions (exact and approximative) is analyzed and summarized in the first and second column of Table 6.1 for the two capacitor sizes. A clear trend of increas-
Figure 6.10: CB current for \( l = 100 \text{ km} \) and \( C = 100 \mu \text{F} \) - Solid line: PSCAD, dotted line: exact solution, dashed line: approximative solution, dashed-dotted line: scaled approximative solution

ing relative error of the exact solution for increasing capacitor size is visible, whereas the approximative solution shows the opposite trend. A larger capacitor shifts the waves’ dominant frequency downwards and, hence, deteriorates the accuracy of the exact solution based on the planar skin effect, which is only valid at high frequencies as explained in Section 6.1.4. The performance of the approximative solution, however, is improved by a larger capacitor, because its time constant \( \tau_C \) is higher and so \( 1/\tau_C \) smaller compared to the frequency \( s \) reducing the error introduced in (6.27) and (6.31) (c.f. Sections 6.1.3 and 6.1.3). The exact and approximative expres-
6.1 Contributions from Capacitive Sources

Emissions yield a higher average \((di/dt)^{avg}\) of the wavefront up to the peak than the PSCAD benchmark results as indicated in Table 6.2 and reveals an increasing error towards larger DC capacitors, particularly, for the approximative solution. In general, the approximative solution matches better the wave tails and the exact solution better the high frequency wave fronts. However, its analytic expression is not as compact as the approximative solution and has a very long form for the adjacent feeder contribution. The performance of the approximative solution can be considerably improved by a scaling factor, but this is rather a model fitting factor.

<table>
<thead>
<tr>
<th></th>
<th>100 km/1 (\mu)F</th>
<th>100 km/100 (\mu)F</th>
<th>10 km/100 (\mu)F</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exact</td>
<td>1.03</td>
<td>6.56</td>
<td>2.83</td>
</tr>
<tr>
<td>Approximative</td>
<td>20.35</td>
<td>13.61</td>
<td>4.33</td>
</tr>
<tr>
<td>Approx. scaled</td>
<td>8.96</td>
<td>0.47</td>
<td>1.6</td>
</tr>
</tbody>
</table>

Table 6.2: Relative Error of \((di/dt)^{avg}\) in %

<table>
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<tr>
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<th>100 km/1 (\mu)F</th>
<th>100 km/100 (\mu)F</th>
<th>10 km/100 (\mu)F</th>
</tr>
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<td>1.62</td>
</tr>
<tr>
<td>Approximative</td>
<td>11.26</td>
<td>29.8</td>
<td>6.51</td>
</tr>
<tr>
<td>Approx. scaled</td>
<td>5.39</td>
<td>14.31</td>
<td>2.25</td>
</tr>
</tbody>
</table>

- Variation of Distance to Fault

A variation of the distance to the fault has only little influence on the results as shown in Fig. 6.11, where the distance to fault \(l\) is reduced to 10 km. The overall fault current level is higher as compared to the 100 km cable between fault and CB in Fig. 6.10 given the lower damping. In the benchmark results in Fig.
6.11 (solid line), the current increases again at 0.16 ms due to the arrival of the second surge of the forward and backward traveling wave on the short 10 km cable. The relative error of the analytic calculations (exact and approximative) is smaller compared to the case with a 100 km cable and 100 $\mu$F capacitor as indicated in the third columns of Tables 6.1 and 6.2.

![Figure 6.11: CB current for $l = 10$ km and $C = 100 \mu$F - Solid line: PSCAD, dotted line: exact solution, dashed line: approximative solution, dashed-dotted line: scaled approximative solution](image)

**Figure 6.11:** CB current for $l = 10$ km and $C = 100 \mu$F - Solid line: PSCAD, dotted line: exact solution, dashed line: approximative solution, dashed-dotted line: scaled approximative solution

### 6.1.5 Conclusions

New analytic time domain expressions for the calculation of fault currents through the CB in HVDC grids during pole-to-ground faults have been proposed. These take into account the planar skin effect
and an adjacent feeder in case of meshed HVDC networks. In general, good accuracy is achieved with the expressions based on the exact back-transformation from the Laplace domain. The peak values and the average $\frac{d}{dt}$ of the wavefronts stay in good agreement with the benchmark simulations. The formulas of the exact transformations have performed better for small DC capacitors and the scaled approximative solutions better for high values of the capacitor. The proposed equations allow a simple CB specification and a highly accurate representation of the temporal development of transient CB currents without detailed simulations, even for very complex current curves with multiple surges. To provide also analytic equations for the time-to-peak and the corresponding average $\frac{d}{dt}$, differentiable functions for the individual contributions have to be found. The improved equations may then serve as a basis for future HVDC fault current calculation standards.

6.2 Contribution from AC Network

6.2.1 Introduction

In Chapter 5, it has been shown that during the first few milliseconds after fault occurrence, the fault current through the CB is dominated by capacitive contributions, whereas the infeed from the AC side becomes the main contributor during the following period. In steady-state, the short-circuit current in an MTDC network is solely fed by the AC networks through the converters.

For the capacitive contributions dominated period, analytic expressions considering individual surges and the planar skin effect have been presented in the previous Section 6.1.

This study is continued in this section and analytic expressions are also proposed for the requirement specification of the CB during the AC infeed dominated second period. Analytic and numeric calculations are presented for the steady-state short-circuit current $I_{avg}^0$ in point-to-point HVDC connections and MTDC systems, as
well as the transient peak value $I_{\text{max}}$ of the AC infeed.

Calculation rules for transient and steady-state short-circuit currents from the adjacent AC network through the freewheeling diodes of the blocked half-bridge converter in DC traction systems can be found in [PNC08, Poz98, BAM91]. These publications consider, however, only single terminal systems and the proposed formulas cannot be applied to meshed MTDC networks.

The IEC 61660 standard for medium voltage DC systems [IEC97] provides formulas for the calculation of the fault current contribution from the adjacent AC network in small radial medium voltage DC networks, which cannot be used for meshed MTDC systems with more than one feeder per busbar.

This section derives novel expressions for the AC network contributions in meshed MTDC networks with arbitrary topology and presents formulas for the peak value as well as the steady-state fault current through the CB.

The approximations are derived for the AC infeed during pole-to-ground faults in HVDC cable systems and compared with simulations in PSCAD for validation. The approximations could also be applied to OHL networks and pole-to-pole faults, but results are only presented for cable systems, since they yield higher fault current levels than OHL schemes as explained in Section 5.2.

Fig. 6.12 illustrates the typical temporal development of the fault current through the CB in the faulted cable of a simplified single terminal arrangement as depicted in Fig. 6.13. The total CB current (solid curve) is the sum of the AC network (dashed curve) and DC capacitor contribution (dotted curve) to the ground fault.

After the ground fault occurs, the voltage at the fault location decreases rapidly and negative voltage surges start to travel from the fault location into both directions towards the terminals.

In the following, only solidly earthed HVDC schemes are considered, since they yield the highest fault currents among all possible grounding schemes as described in Chapter 8. The grounded capacitor midpoint and the ground fault form a loop that provokes
Figure 6.12: Breakdown of the total CB current (solid curve) into contributions from AC side (dashed curve) and DC capacitor (dotted curve)

**Figure 6.13:** Single line diagram of single terminal AC infeed

a discharge of the capacitors upon the arrival of the surge at the terminal and yields the first peak $I_{p1}$ at around 1 ms as seen in Fig. 6.12.

The surges are reflected and travel forward and backward between
the terminal and the fault location [Kim70] that leads to multiple peaks in the current pattern (three peaks visible between 1 and 8 ms in Fig. 6.12). During this first 8 ms, the pattern is determined by the traveling surges and consecutive DC capacitor discharges as explained and calculated in the previous Section 6.1.

The AC side feeds the fault through the free-wheeling diodes (dashed curve in Fig. 6.12) as soon as the DC capacitors are discharged and the voltage at the terminal drops below the converter’s AC side voltage [YFO10]. In contrast to the half-bridge topologies, converters with full-bridge schemes are able to block the AC infeed and, consequently, the fault current comprises only contributions from capacitive sources (see Section 5.1).

In the following, the AC contribution increases and the DC capacitor is charged again by the AC infeed with the peak at 10 ms and discharged into the ground fault that leads to the peak $I_{\text{max}}$ in the CB current at around 13 ms. The maximum of the CB current is determined by various factors: the DC capacitor, the possible pole reactor in series to the CB, the distance to the fault, the short-circuit capacity of the adjacent AC network, and the fault resistance. During the period between 10 and 40 ms, the AC side and the DC capacitor contribution interact and influence each other, which results in a damped oscillation of the CB current.

The DC capacitor contribution gradually decreases until the steady-state is reached at around 40 ms. In the steady-state, the DC capacitor is still charged and discharged, but has no net contribution to the fault current, i.e. its mean value is zero, and has, therefore, no influence on the total fault current through the CB. The steady-state CB current exhibits a 300 Hz ripple given by the blocked converter acting as a 6-pulse diode rectifier.

The aim of this section is, thus, to present an analytic approximation of the time development of the total CB current. It is, however, not possible to analytically represent the exact waveform as shown in Fig. 6.12 (solid curve), but some characteristic points are calculated instead. These are the amplitude of the peak of the transient
period $I_{\text{max}}$ and the average steady-state short-circuit current $I_{0}^{\text{avg}}$.

### 6.2.2 Setup for Benchmark Simulations

The default cable model as described in Section 4.4.1 is used for the benchmark simulations.

The converters are modeled as default $\pm 320$ kV bipolar half-bridge VSC topology with concentrated midpoint-grounded dc capacitors $C_{\text{cap}}$ at each terminal as described in Section 4.1. This model is valid for all half-bridge based topologies with anti-parallel freewheeling diodes, independently of whether it is a two-level, three-level or a modular multilevel converter (MMC). The MMC topology has additional arm reactors $L_{\text{arm}}$ as indicated in Fig. 6.14. An additional phase reactor $L_{s}$ is installed between converter bridge and transformer for harmonic filtering of the ac currents. The MMC topology does not require filtering and $L_{s}$ is usually neglected. The pole reactors, which are usually installed on the dc side, are neglected in this study, because it considers the worst case without additional damping [BF13b].

![Electrical equivalent scheme of the half-bridge based converter model with blocked IGBTs](image)

**Figure 6.14:** Electrical equivalent scheme of the half-bridge based converter model with blocked IGBTs ($V_{ac}$: AC voltage, $R_{ac}$: AC resistance, $L_{ac}$: AC inductance, $L_{t}$: Transformer reactance, $L_{s}$: phase reactor, $L_{arm}$: arm reactor (MMC), $C_{\text{cap}}$: DC capacitor)
6.2.3 Derivation of Analytic Expressions

In the following, analytic approximations are derived for the value of the steady-state, as well as for the overshoot of the transient response of the CB current.

**Steady-State Short-Circuit Current**

The formula for the steady-state short-circuit current during a pole-to-ground fault can be derived by dividing the voltage by the impedance as in [IEC97]:

\[
I_{0}^{\text{avg}} = \frac{3}{\pi} \cdot \frac{\sqrt{\frac{2}{3}} \cdot N \cdot V_{\text{ac}}}{\sqrt{X^2 + R^2}}
\]

\[
X = (\omega L_{\text{ac}} + \omega L_{t}) N^2 + \omega L_{s} + \frac{1}{2} \omega L_{\text{arm}}
\]

\[
R = N^2 \cdot R_{\text{ac}} + \frac{2}{3} R_{f} + \frac{2}{3} R_{\text{dc}}
\]

with the AC network impedance \(R_{\text{ac}} + j \cdot \omega L_{\text{ac}}\), the phase-to-phase RMS source voltage \(V_{\text{ac}}\), the transformer reactance \(L_{t}\), the transformer turns ratio \(N\), the phase reactor \(L_{s}\), the resistance of the faulted cable section \(R_{\text{dc}}\), and the possible additional fault resistance \(R_{f}\). The factor \(3/\pi\) in (6.35) comes from the integration of the DC voltage over one sixth of a period to get the average DC voltage of the unloaded 6-pulse diode converter. Equation (6.35) assumes the diode rectifier with three diodes conducting at the same time and, therefore, the DC side resistances are multiplied by a factor of \(2/3\). The DC side inductances have no influence on the steady-state current and are omitted in the calculations.

- **Point-to-point connection**

  The steady-state fault current through the CB \(I_{\text{dc1}}\) in a point-to-point HVDC connection as illustrated in Fig. 6.15 is not
provided by [IEC97], but can be calculated similarly. To do so, Kirchhoff’s Voltage Law (KVL) is applied to the circuit sections to both sides of the ground fault and Kirchhoff’s Current Law (KCL) to the node of the ground fault. The resulting system of three equations is then solved for current $I_{dc1}^{avg}$:

$$I_{dc1}^{avg} = \frac{3}{\pi} \sqrt{\frac{2}{3}} N_1 V_{ac1} \cdot (Z_2 + \frac{2}{3} R_f)$$
$$\cdot \frac{Z_1 Z_2 + \frac{2}{3} R_f Z_1 + \frac{2}{3} R_f Z_2}{Z_1 Z_2 + \frac{2}{3} R_f Z_1 + \frac{2}{3} R_f Z_2} - \frac{3}{\pi} \sqrt{\frac{2}{3}} N_2 V_{ac2} \cdot \frac{2}{3} R_f$$
$$\cdot \frac{Z_1 Z_2 + \frac{2}{3} R_f Z_1 + \frac{2}{3} R_f Z_2}{Z_1 Z_2 + \frac{2}{3} R_f Z_1 + \frac{2}{3} R_f Z_2} \quad (6.38)$$

$$Z_i = j \omega \left( L_{ac,i} N_i^2 + L_{t,i} N_i^2 + L_{s,i} + \frac{1}{2} L_{arm,i} \right)$$
$$+ R_{ac,i} N_i^2 + \frac{2}{3} R_{dc,i} , \quad i = 1, 2. \quad (6.39)$$

In the general case with non-zero fault resistance $R_f$, the fault currents in both sections depend on each other, whereas with zero fault resistance, (6.38) reduces to (6.35).
• Multiterminal network

The steady-state short-circuit current in the faulted branch of a multiterminal network as depicted in Fig. 6.16 can be expressed as a system of linear equations. Each terminal is treated as a node with AC and DC branches connected to it. An additional node is added for the ground fault, which is earthed through the fault resistance \( R_f \). Hence, an n-terminal HVDC network results in a system of \( n + 1 \) linear equations. The general equation for an n-terminal network is

\[
\left[ Y_{dc} + \frac{2}{3} \cdot Y_{ac} \right] \cdot \begin{bmatrix} v_{dc,1} \\ v_{dc,2} \\ \vdots \\ v_{dc,n} \\ v_f \end{bmatrix} = \frac{3}{\pi} \cdot Y_{ac} \cdot \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \\ v_0 \end{bmatrix}
\]

(6.40)

with the DC network admittance matrix \( Y_{dc} \) including the fault node, but neglecting the AC admittances. It has the dimensions \((n + 1) \times (n + 1)\), where \( n \) is the number of DC nodes as labeled in Fig. 6.16. \( Y_{ac} \) is the \((n + 1) \times (n + 1)\) AC system admittance matrix with the AC admittances in the diagonal plus a zero element for the fault node. The elements
of $Y_{dc}$ are obtained by:

$$Y_{dc,ij} = \begin{cases} y_{dc,ii} + \sum_{i\neq j} y_{dc,ij} & \text{if } i = j, \\ -y_{dc,ij} & \text{if } i \neq j \end{cases} \quad (6.41)$$

with the DC line conductances $y_{dc,ij} = 1/R_{dc,ij}$ and the DC bus shunt conductances $y_{dc,ii} = 1/R_{dc,ii}$, i.e. fault conductance $1/R_f$.

The elements in the diagonal of $Y_{ac}$ are

$$Y_{ac,ii} = \left[ N_i^2(j\omega L_{ac,i} + j\omega L_{t,i} + R_{ac,i}) + j\omega(L_{s,i} + \frac{1}{2}L_{arm,i}) \right]^{-1}. \quad (6.42)$$

The input voltages $v_{0i}$ are calculated as

$$v_{0i} = \sqrt{\frac{2}{3}} \cdot N_i \cdot V_{ac,i}, \quad (6.43)$$

where $N_i$ is the turns ratio of the converter transformer and $V_{ac,i}$ the RMS phase-to-phase voltage of the corresponding adjacent AC system.

To calculate the average steady-state fault current through the CB indicated in Fig. 6.16 considering the AC side contributions from all terminals, the matrix of the left hand side of (6.40) has to be inverted numerically to solve (6.40) for the DC terminal voltages $v_{dc,1}, \ldots, v_{dc,n}$, and $v_f$. The CB current can be finally calculated by

$$i_0^{\text{avg}} = (v_{dc,1} - v_f) \cdot y_{1f}. \quad (6.44)$$
Note that the DC currents and voltages contain a certain ripple and only averaged values are considered. Therefore, the AC source voltages $v_{0x}$ are multiplied by $\frac{3}{\pi}$ and $N_x$ in (6.40) to get the average DC voltage of the unloaded converter.

The resulting matrices representing the example network in Fig. 6.16 are

$$Y_{dc} =
\begin{bmatrix}
y_{1f} + y_{13} & 0 & -y_{13} & 0 & -y_{1f} \\
0 & y_{2f} + y_{23} & -y_{23} & -y_{24} & -y_{2f} \\
& +y_{24} & & & \\
-y_{13} & -y_{23} & y_{13} + y_{23} & -y_{34} & 0 \\
& +y_{34} & & & \\
0 & -y_{24} & -y_{34} & y_{24} + y_{34} & 0 \\
-y_{1f} & -y_{2f} & 0 & 0 & y_{1f} + y_{2f} \\
& & & + \frac{1}{R_f} & 
\end{bmatrix} 
(6.45)$$

and

$$Y_{ac} =
\begin{bmatrix}
y_{ac1} & 0 & 0 & 0 & 0 \\
0 & y_{ac2} & 0 & 0 & 0 \\
0 & 0 & y_{ac3} & 0 & 0 \\
0 & 0 & 0 & y_{ac4} & 0 \\
0 & 0 & 0 & 0 & 0
\end{bmatrix} . 
(6.46)$$

**Transient Short-Circuit Current**

The exact time development of the transient contributions from all adjacent AC networks through the CB in the example network in Fig. 6.16 cannot be represented analytically. Formulas are derived for the peak value of the fault current $I_{max}$ instead (c.f. Fig. 6.12).
Along with the peak value of the capacitive contributions as calculated in Section 6.1 at 2 ms in Fig. 6.12, the peak of the AC infeed at 13 ms is a dimensioning criterion for the CB.

To do so, the transient behavior of the higher order system as shown in Fig. 6.16 is approximated by the well-known solution of an underdamped, oscillating second order system:

\[
i_{cb}(t) = \frac{\pi}{3} \cdot I_{0}^{\text{avg}} \cdot \left\{ 1 - e^{-\zeta_{MT} \cdot \omega_{T1} \cdot (t - T)} \cdot \left[ \cos(\omega_{MT} \cdot (t - T)) + \frac{\zeta_{MT}}{\sqrt{1 - \zeta_{MT}^2}} \cdot \sin(\omega_{MT} (t - T)) \right] \right\} \cdot u(t - T), \tag{6.47}
\]

where \(I_{0}^{\text{avg}}\) is the steady-state short-circuit current as calculated in (6.44), \(u(t)\) is a unit step function, and \(T\) is the traveling delay of the initial surge:

\[
T = \frac{l}{c} \tag{6.48}
\]

based on the line length \(l\) and the propagation speed of the surge \(c = 1/\sqrt{L \cdot C}\).

The damping ratio \(\zeta_{MT}\) expresses the level of damping in the system relative to critical damping. It indicates, whether the system is underdamped \((0 < \zeta_{MT} < 1)\), critically damped \((\zeta_{MT} = 1)\) or overdamped \((\zeta_{MT} > 1)\). In an overdamped system, the trigonometric functions in (6.47) turn into hyperbolic functions based on \(\sinh(x) = -j \cdot \sin(jx)\) and \(\cosh(x) = \cos(jx)\).

To obtain the unknown system damping ratio \(\zeta_{MT}\), the method proposed in [PNC08] is used. In [PNC08], the unknown damping ratio of a single terminal system with a converter connected to a faulted line is calculated through the multiplication of the known damping ratio of the converter itself by the ratio of the DC side and
AC side inductances. This method is applied to the MTDC system in Fig. 6.16 with assumed known damping ratio $\zeta_{T1}$ of the subsystem consisting of terminal 1 connect to the ground fault through the cable section 1-$\xi$F only. The known damping $\zeta_{T1}$ is then multiplied by the ratio of the decay rates of terminal 1 $\alpha_{T1}$ and the entire MTDC system $\alpha_{MT}$ as follows:

$$\zeta_{MT} = \zeta_{T1} \cdot \frac{\alpha_{T1} + \alpha_{MT}}{\alpha_{T1}}$$

(6.49)

using

$$\alpha_{T1} = \frac{R \cdot \omega}{X}$$

(6.50)

with $R$ and $X$ calculated by (6.37) and (6.36), respectively.

The decay rate of the MTDC network $\alpha_{MT}$ required in (6.49) is calculated as

$$\alpha_{MT} = \frac{R_{eq}}{L_{eq}}$$

(6.51)

using the equivalent MTDC network resistance $R_{eq}$ and inductance $L_{eq}$ as seen from terminal 1. For the example network in Fig. 6.16, these two parameters are computed as follows:

$$R_{eq} = \left[ \frac{1}{R_{1f}} + \frac{1}{R_{13}} + \left( \frac{1}{R_{23}} + \frac{1}{R_{34}} + \frac{1}{R_{24}} \right)^{-1} + R_{2f} \right]^{-1} + R_{f}$$

(6.52)

and
6.2 Contribution from AC Network

\[ L_{eq} = \left[ \frac{1}{L_{1f}} + \frac{1}{L_{13}} + \left( \frac{1}{L_{23}} + \frac{1}{L_{34}} + \frac{1}{L_{24}} \right)^{-1} + L_{2f} \right]^{-1}, \tag{6.53} \]

respectively.

The damping ratio of terminal 1 \( \zeta_{T1} \) used in (6.49) is derived from the peak value \( I_{T1}^{\text{max}} \) and the steady-state short-circuit current \( I_{0}^{T1,\text{avg}} \) of the single terminal system

\[ \zeta_{T1} = \sqrt{1 - \left( \frac{\pi^2}{\pi^2 + \left( \ln \left( \frac{I_{T1}^{\text{max}} - I_{0}^{T1,\text{avg}}}{I_{0}^{T1,\text{avg}}} \right) \right)^2} \right)} \tag{6.54} \]

The corresponding frequency \( \omega_{T1} \) of the single terminal system can be evaluated using

\[ \omega_{T1} = \frac{\pi}{2 \cdot \phi_{T1} \sqrt{1 - \zeta_{T1}^2} \omega} \tag{6.55} \]

and the phase angle

\[ \phi_{T1} = \arctan \left( \frac{X}{R} \right) \tag{6.56} \]

where \( R \) and \( X \) are the single terminal system parameters determined in (6.37) and (6.36), respectively.

The frequency of the transient oscillation in the MTDC system \( \omega_{MT} \) in (6.47) is calculated by

\[ \omega_{MT} = \omega_{T1} \cdot \sqrt{1 - \zeta_{MT}^2} \tag{6.57} \]
based on the damping ratio $\zeta_{MT}$ of the MTDC system and the frequency of the single terminal system $\omega_{T1}$.

Finally, the peak value of the transient fault current through the CB $I_{\text{max}}$ and the corresponding time to peak $t_{\text{max}}$ is derived from (6.47). The resulting formulas are

$$I_{\text{max}} = \frac{\pi}{3} I_{\text{avg}} \cdot \left( 1 + e^{-\frac{-\zeta_{MT} \cdot \pi}{\sqrt{1 - \zeta_{MT}^2}}} \right)$$

(6.58)

and

$$t_{\text{max}} = \frac{\pi}{\omega_{MT}} + T.$$  

(6.59)

### 6.2.4 Comparison and Discussion

The results of the derived formulas for the fault current through the CB as indicated in Fig. 6.16 are verified by comparison to PSCAD simulations as presented in this section. The comparison includes dc system, as well as ac system parameter variations to validate the analytic approximations. The considered dc parameters are the dc capacitor size, the fault resistance, and the network topology of the four-terminal system. The ac system parameter variations include the short-circuit power of the adjacent ac networks and the size of the converter’s commutation inductance, i.e. the arm reactor in an MMC. Results are shown for the steady-state and the peak value of the transient CB current in the MTDC network.

### Parameters

The default system parameters for the comparison are summarized in Table 6.3.

Three different MTDC network scenarios are considered and their values are summarized in Table 6.4. Grid topology A and B cor-
Table 6.3: Default System Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Converter Power</td>
<td>450 MW</td>
</tr>
<tr>
<td>DC Voltage</td>
<td>±320 kV</td>
</tr>
<tr>
<td>AC Voltage (L-L, RMS)</td>
<td>400 kV</td>
</tr>
<tr>
<td>AC Frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>SCR of AC Networks</td>
<td>20</td>
</tr>
<tr>
<td>X/R of AC Networks</td>
<td>10</td>
</tr>
<tr>
<td>Transformer Leakage Reactance</td>
<td>0.1 p.u.</td>
</tr>
<tr>
<td>Transformer Turns Ratio</td>
<td>270/400</td>
</tr>
<tr>
<td>Converter Phase Reactor</td>
<td>0.05 p.u.</td>
</tr>
</tbody>
</table>

respond to the topology presented in Fig. 6.16, but with different line lengths $l$. Grid topology C has a connection between terminal 1 and 4 ($l_{14}$) instead of 2 and 3 ($l_{23}$) as in layouts A and B. The fault resistance $R_f$ is varied between 0 and 4Ω and the DC capacitors $C_{cap}$ at all four terminals between 0 and 200 µF to consider systems with new converter technologies that require no or very low DC side filtering, as well as the worst case with very large DC capacitors.

The required input parameters for the analytic calculations are also presented in Table 6.4. The per unit length DC line resistance $R'_{dc}$ and inductance $L'_{dc}$ are obtained through the PSCAD Line Constant Program. The peak $I_{max}$ and the steady-state value $I_0$ of the short-circuit current of terminal 1 are derived from simulations of the single terminal system comprising terminal 1 only. The two values $I_{max}$ and $I_0$ depend only on the parameters of the AC network adjacent to terminal 1 and on the line length $l_{1f}$.

**Variation of Fault Resistance**

Table 6.5 summarizes the relative error of the analytic calculations of the peak and steady-state value of the CB current in the MTDC network with topology A as depicted in Fig. 6.16. The DC capaci-
### Table 6.4: Parameters of Four-Terminal HVDC Grid

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Topology A</th>
<th>Topology B</th>
<th>Topology C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$l_{1f}$</td>
<td>100 km</td>
<td>50 km</td>
<td>50 km</td>
<td>-</td>
</tr>
<tr>
<td>$l_{2f}$</td>
<td>70 km</td>
<td>70 km</td>
<td>70 km</td>
<td>-</td>
</tr>
<tr>
<td>$l_{13}$</td>
<td>180 km</td>
<td>80 km</td>
<td>180 km</td>
<td>-</td>
</tr>
<tr>
<td>$l_{23}$</td>
<td>80 km</td>
<td>180 km</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$l_{14}$</td>
<td>-</td>
<td>-</td>
<td>80 km</td>
<td>-</td>
</tr>
<tr>
<td>$l_{24}$</td>
<td>20 km</td>
<td>120 km</td>
<td>120 km</td>
<td>-</td>
</tr>
<tr>
<td>$l_{34}$</td>
<td>90 km</td>
<td>90 km</td>
<td>90 km</td>
<td>-</td>
</tr>
<tr>
<td>$R'_{dc}$</td>
<td></td>
<td>0.0123 Ω/km</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$L'_{dc}$</td>
<td></td>
<td>3.45 mH/km</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$R_{eq}$</td>
<td>2.26 Ω</td>
<td>1.23 Ω</td>
<td>1.27 Ω</td>
<td>-</td>
</tr>
<tr>
<td>$L_{eq}$</td>
<td>14.7 mH</td>
<td>8 mH</td>
<td>8.3 mH</td>
<td>-</td>
</tr>
<tr>
<td>$I_{max}$</td>
<td>10.35 kA</td>
<td>11.5 kA</td>
<td>11.5 kA</td>
<td>-</td>
</tr>
<tr>
<td>(Terminal 1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_0$</td>
<td>7.39 kA</td>
<td>7.42 kA</td>
<td>7.42 kA</td>
<td>-</td>
</tr>
<tr>
<td>(Terminal 1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{cap}$</td>
<td></td>
<td>0 – 200 µF</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$R_f$</td>
<td></td>
<td>0 – 4 Ω</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
tors $C_{\text{cap}}$ are neglected and the values are given for fault resistances $R_f$ between 0 and 4 Ω.

The peak value of the CB current $I_{\text{max}}$ can be estimated accurately using (6.58) with a relative error below 3% for all values of the fault resistance. The small deviations are mainly due to estimation errors of the single terminal peak and steady-state fault current values $I_{\text{T1}}^{\text{max}}$ and $I_0^{\text{T1,avg}}$, respectively. Equation (6.54) is sensitive to these values and errors in their estimation may deteriorate the accuracy of the calculate peak magnitude $I_{\text{max}}$ in the MTDC network. An alternative determination of the damping ratio $\zeta_{\text{MT}}$ in the MTDC system without relying on the single terminal damping ratio $\zeta_{\text{T1}}$ would mitigate this problem.

![Figure 6.17: Comparison of peak value results from analytic calculations ○ and PSCAD simulations □ for various fault resistances](image)

The analytic function (6.47) is plotted by the dashed curve in
Fig. 6.17 for zero fault resistance and the results of (6.58) and (6.59) are indicated by circles. The time to peak $t_{\text{max}}$ based on (6.59) exhibits rather large deviations from the actual values of the PSCAD simulation outcomes as indicated by squares in Fig. 6.17. The time to peak of the AC infeed is very difficult to estimate in an MTDC system due to the superposition of the contributions from all terminals, whose peaks occur at different instances in time due to the different distances to the fault, i.e. different phase angles. To specify the CB requirements, the exact time to peak of the AC infeed and the corresponding $di/dt$, however, are not as important as the $di/dt$ of the initial surge $I_{p1}$ as shown in Fig. 6.12. The $di/dt$ of the AC network contributions are much lower due to the current limiting AC side inductances.

The differences between simulated and approximated results for the average steady-state short-circuit currents are within a few tens of amps and the relative error is below 1% for all fault resistances as summarized in the second column of Table 6.5. The small differences are due the simplified calculation of the average steady-state current based on the sixth harmonic only and no other harmonics are considered, which are present in the simulations.

<table>
<thead>
<tr>
<th>$R_f[\Omega]$</th>
<th>Rel. Error Peak Value [%]</th>
<th>Rel. Error Steady-State Value [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.61</td>
<td>0.11</td>
</tr>
<tr>
<td>1</td>
<td>1.70</td>
<td>0.05</td>
</tr>
<tr>
<td>2</td>
<td>1.66</td>
<td>0.19</td>
</tr>
<tr>
<td>3</td>
<td>2.13</td>
<td>0.31</td>
</tr>
<tr>
<td>4</td>
<td>2.27</td>
<td>0.41</td>
</tr>
</tbody>
</table>
Variation of DC Capacitor Size

The relative error of the analytic calculation of the peak magnitude is presented in Table 6.6 for DC capacitor sizes between 0 and 200 µF. Although formula (6.58) does not take into account the DC capacitor size, the relative errors of the calculated peak magnitude remain below 8% for the considered capacitor sizes up to 200 µF. The deviations from the simulation results are again due to estimation errors in the single terminal damping ratio $\zeta_{T1}$ as explained in Section 6.2.4.

The calculations of the steady-state fault current through the CB, not shown in Table 6.6, yield the same relative error of 0.05% for all DC capacitor sizes, since the capacitors have no influence on the average steady-state fault current.

A graphic presentation of the PSCAD results (squares) and the analytic result (circle) is shown in Fig. 6.18. As can be seen, the DC capacitor size influences considerably the instance of time of the AC infeed peak. An exact estimation of this instance is beyond the scope of this paper. Moreover, Fig. 6.18 reveals that the DC capacitor size has more influence on the initial capacitor discharge peak $I_{p1}$ than on the AC infeed peak magnitude $I_{max}$.

Table 6.6: Variation of DC Capacitor - Topology A, $R_f = 1 \Omega$

<table>
<thead>
<tr>
<th>$C_{cap} [\mu F]$</th>
<th>Rel. Error Peak Value [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3.55</td>
</tr>
<tr>
<td>10</td>
<td>2.44</td>
</tr>
<tr>
<td>50</td>
<td>7.72</td>
</tr>
<tr>
<td>100</td>
<td>1.25</td>
</tr>
<tr>
<td>200</td>
<td>7.50</td>
</tr>
</tbody>
</table>
Variation of Network Topology

The variation of the network topology yields relative errors of the calculated peak magnitude between 1.7% in topology A to 3.77% in topology C as presented in Table 6.7. The relative error of the calculated average steady-state CB current remains again below 1%.

Variation of SCR

To validate the derived formulas, also the SCR of the adjacent ac networks is varied. The variation considers values of the SCR between 5 (weak ac system) and 40 (strong ac system). Table 6.8 shows that the proposed equations provide accurate results with relative errors below 0.06% for the steady-state value and below 1.7% for
6.2 Contribution from AC Network

Table 6.7: Variation of Network Topology - $R_f = 1 \Omega$, $C_{cap} = 0 \mu F$

<table>
<thead>
<tr>
<th>Topology</th>
<th>Rel. Error Peak Value [%]</th>
<th>Rel. Error Steady-State Value [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.70</td>
<td>0.05</td>
</tr>
<tr>
<td>B</td>
<td>3.30</td>
<td>0.29</td>
</tr>
<tr>
<td>C</td>
<td>3.77</td>
<td>0.47</td>
</tr>
</tbody>
</table>

Table 6.8: Variation of SCR - Topology A, $R_f = 1 \Omega$, $C_{cap} = 0 \mu F$

<table>
<thead>
<tr>
<th>SCR</th>
<th>Rel. Error Peak Value [%]</th>
<th>Rel. Error Steady-State Value [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0.01</td>
<td>0.06</td>
</tr>
<tr>
<td>10</td>
<td>0.65</td>
<td>0.03</td>
</tr>
<tr>
<td>20</td>
<td>1.7</td>
<td>0.05</td>
</tr>
<tr>
<td>30</td>
<td>1.02</td>
<td>0.01</td>
</tr>
<tr>
<td>40</td>
<td>0.67</td>
<td>0.04</td>
</tr>
</tbody>
</table>

the peak value of the transient ac infeed.

**Variation of Arm Reactor Size**

An MMC topology comprises an additional arm reactor $L_{arm}$ as shown in Fig. 6.14, which increases the converter’s total commutation reactance. As an additional proof for the validity of the proposed equations, the size of $L_{arm}$ is varied between 10 and 20% of the base impedance. Since the MMC does not require ac side filtering, the phase reactor $L_s$ is neglected and the transformer leakage reactance $L_t$ is kept fixed. Table 6.9 shows an increasing relative error for both the peak and the steady-state value of the CB current with $L_{arm}$ larger than 0.16 p.u. This is due to the fact that the derived formulas assume three simultaneously conducting diodes, whereas a larger commutation inductance, i.e. longer diode conduction periods, results in four simultaneously conducting diodes. The operation mode of the rectifier is not only influenced by the ac side
Table 6.9: Variation of Arm Reactor - Topology A, $R_f = 1\,\Omega$, $C_{cap} = 0\,\mu F$

<table>
<thead>
<tr>
<th>$L_{arm}[\text{p.u.}]$</th>
<th>Rel. Error Peak Value [%]</th>
<th>Rel. Error Steady-State Value [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>1.7</td>
<td>0.05</td>
</tr>
<tr>
<td>0.12</td>
<td>1.0</td>
<td>0.04</td>
</tr>
<tr>
<td>0.14</td>
<td>3.45</td>
<td>0.06</td>
</tr>
<tr>
<td>0.16</td>
<td>5.85</td>
<td>0.03</td>
</tr>
<tr>
<td>0.18</td>
<td>8.08</td>
<td>1.18</td>
</tr>
<tr>
<td>0.2</td>
<td>10.18</td>
<td>5.05</td>
</tr>
</tbody>
</table>

commutation inductance, but also by the load, i.e. the dc network and the fault resistance. For larger fault resistances, the operation point of the rectifier moves to the three-diode mode and the proposed formulas become more accurate. The study of all rectifier operation modes is beyond the scope of this paper and is subject to future extensions.

### 6.2.5 Conclusions

This paper presents novel analytic formulas for the calculation of the fault current contribution from the AC network through the DC CB during a pole-to-ground fault in a meshed MTDC system. Analytic expressions are derived for the steady-state short-circuit current through the CB, as well as for the peak value of the transient current in an MTDC network with arbitrary topology. In contrast to the existing IEC 61660 standard for small medium voltage DC networks, the expressions proposed in this paper can be applied to meshed MTDC systems with multiple feeders per bus-bar. The proposed expressions are validated by the comparison to detailed simulations in PSCAD using parameter variations of the DC capacitor size, fault resistance, and network topology.

Highly accurate results with relative errors below 1% are achieved with the formula for the steady-state CB current in MTDC net-
works. Also the amplitude of the transient peak of the AC infeed can be accurately calculated with relative errors below 8% for the whole range of DC capacitor size, fault resistance, and network topologies considered in this study. The accuracy could be improved with an alternative estimation of the MTDC system damping ratio, which serves as basis for the AC infeed peak magnitude calculations.

The proposed equations show an acceptable accuracy for arm reactors up to 0.16 p.u. in the base case with a small fault resistance. For larger reactors, the four-diode operation mode of the rectifier is prevailing and the derived formulas become less accurate. For a larger range of commutation inductance sizes, the derived approximations have to be improved and other rectifier operation modes have to be considered.

For a future short-circuit calculation standard, characteristic values connected piecewise by enveloping functions will be required to approximate the entire development of the prospective CB current over time as used in most existing standards. The expressions for peak and steady-state values of the CB current during the AC infeed dominated period as presented in this paper, together with the values of the initial surges as proposed in Section 6.1, could serve as characteristic values for such a standard.
7 Effect of DC Network Topology

7.1 Transient Fault Currents and Voltages

7.1.1 Introduction

Another key factor is the DC grid topology. This aspect has not received much attention in the literature yet and is the focus of this section. Using the example of a twelve-terminal North Sea grid connecting six northern European countries and three offshore clusters, this section investigates key dependencies between the DC grid topology and transient fault currents through HVDC CBs for different fault locations and grid structures.

Results are obtained through EMTP simulations in PSCAD based on equivalent models of onshore and offshore coupling points, converter stations, and frequency-dependent distributed-parameter cable representations.

7.1.2 Simulation Models

Converter and Onshore Coupling Points

Each VSC-HVDC converter station in the DC grid is assumed to be a bipolar half-bridge based converter with a nominal rating of 900 MW as described in Section 4.1. A small DC capacitor of $1 \mu F$ assumed for all simulations.

The default AC network model as in Section 4.2 is used for the adjacent onshore AC networks.
Cable Model

The default cable model as described in Section 4.4.1 is applied.

Offshore Coupling Points

Because most offshore wind farms will be based on variable speed turbines that are connected to the grid through fullpower frequency converters [Pfe12], a distinct representation of offshore coupling points is employed. There is a relatively broad consensus in the scientific literature regarding the nature and magnitude of the short circuit current contribution from full converter wind turbines. In [Md07, WGE11, NM11], it is stated that their fault current contribution is limited to the turbine’s nominal current or a value slightly above it. It is also generally agreed that the short circuit current contribution depends primarily on the characteristics of the converter rather than the physical properties of the generator.

The offshore nodes were thus modeled in a slightly different manner than the regular onshore AC nodes. The implementation leans on the approach in [BP08], in which the initial symmetrical short circuit current contribution of full converter wind turbines is modeled as:

\[ I_{SC} = k \cdot I_{rG} , \]  

(7.1)

where \( k \) is the factor by which the short circuit current exceeds the nominal current of the wind turbine. This approach was modified to account for initial transients reported in [WGE11] and [NM11]. The resulting model is implemented in the form of a voltage source with a variable short circuit power. Based on the information provided in [WGE11], \( k \) is chosen to decrease from 3 to 1.5 over the duration of two cycles (i.e. 40 ms) after the fault initiation and subsequently remains constant. For lack of more detailed information, a linear transition between the two values was chosen [Pfe12].
7.1.3 Grid Parameters and Scenarios

Coupling Point Characteristics

A detailed twelve-terminal VSC HVDC grid model, consisting of 9 onshore and 3 offshore nodes, was built around the geography of the North Sea as illustrated in Fig. 7.1. The location of onshore coupling points was derived from existing plans for offshore grids in the North Sea [Gre08, Off11], while also considering the location of existing high voltage substations as given on the ENTSO-E Grid Map [ENT11]. The locations of the three offshore nodes are roughly based on the location of approved zones in which licenses for large scale offshore wind farms have been granted. Tables 7.1 and 7.2 summarize key parameters of the nodes. The PCC voltage values correspond to the highest AC voltage level in each of the connected countries. The short circuit values, SSC, lean on assumptions made in [MS03] regarding the maximum short circuit current in the Spanish high voltage grid. The assumptions of the reactance to resistance ratio, X/R, lean on values given for high voltage networks in [Kun94].

<table>
<thead>
<tr>
<th>Node #</th>
<th>Country</th>
<th>PCC Voltage [kV]</th>
<th>$S_{SC}$ [MVA]</th>
<th>$X/R$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NO</td>
<td>300</td>
<td>23400</td>
<td>8.5</td>
</tr>
<tr>
<td>2</td>
<td>DK</td>
<td>380</td>
<td>26300</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>DE</td>
<td>380</td>
<td>26300</td>
<td>10</td>
</tr>
<tr>
<td>4</td>
<td>NL</td>
<td>380</td>
<td>26300</td>
<td>10</td>
</tr>
<tr>
<td>5</td>
<td>NL</td>
<td>380</td>
<td>26300</td>
<td>10</td>
</tr>
<tr>
<td>6</td>
<td>BE</td>
<td>380</td>
<td>26300</td>
<td>10</td>
</tr>
<tr>
<td>7</td>
<td>UK</td>
<td>400</td>
<td>27700</td>
<td>10</td>
</tr>
<tr>
<td>8</td>
<td>UK</td>
<td>400</td>
<td>27700</td>
<td>10</td>
</tr>
<tr>
<td>9</td>
<td>UK</td>
<td>400</td>
<td>27700</td>
<td>10</td>
</tr>
</tbody>
</table>
Grid Topologies

The four grid topologies under investigation are shown in Fig. 7.2. Connection distances are given in Table 7.3. The rationale behind each topology is briefly described in the following paragraphs:

(a) **Radial Grid:** This topology consists of a series connection of all three offshore nodes and radial connections from the offshore nodes to the onshore nodes in their zone. In principal, all individual countries can trade with each other.

(b) **Lightly Meshed Grid:** This topology extends the linear connection between the three offshore nodes with another offshore connection between nodes 10 and 11. This creates an N-1 level of redundancy in terms of power transfer between the three zones. Furthermore, the flexibility with regard to power trading is enhanced. For example, Norway could export power to Belgium, while at the same time Denmark imports power...
Table 7.2: Parameters of Offshore Nodes

<table>
<thead>
<tr>
<th>Node #</th>
<th>Concession Area</th>
<th>Nameplate Capacity [MW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>BARD Area</td>
<td>4000</td>
</tr>
<tr>
<td>11</td>
<td>Norfolk Bank</td>
<td>3600</td>
</tr>
<tr>
<td>12</td>
<td>Dogger Bank</td>
<td>4500</td>
</tr>
</tbody>
</table>

from the UK (this is not feasible in the radial grid).

(c) **Ring Shaped Grid:** In this topology, the three areas are connected with each other at their periphery. The full capacity of each inter-area connection can be scheduled independently of wind power evacuation requirements.

(d) **Densely Meshed Grid:** This topology consists of the largest number of connections and represents the highest level of redundancy and flexibility among the four topologies. Furthermore, because the average transmission distance between any two given points in this system is shortest, this scenario would also be expected to lead to the lowest system losses [BWAF14]. It is of course also associated with the highest investment costs.

**Fault Scenarios**

Faults f1 and f2 (c.f. Fig. 7.2) are applied to connections between offshore node 10 and onshore nodes 1 and 3, respectively. Fault f1 is 100 km away from node 1 and f2 is 85 km away from node 3. The primary difference between the two fault locations is that f2 is directly next to a peripheral node in all four scenarios, while f1 is only next to a peripheral node in grids (a) and (b). The location f3 is an example of a terminal fault. It is applied at node 10 on the feeder to node 1. All faults are considered to be positive pole-to-ground faults with a purely resistive constant fault impedance of 7 Ω. This value is based on findings in [WLD05].
7.1.4 Results and Discussion

Fault 1

The upper part of Fig. 7.3 shows the global maximum current through all DC CBs in each of the four grids as a function of time af-
Table 7.3: Connection Distances in Twelve Terminal Offshore Grid Topologies

<table>
<thead>
<tr>
<th>From</th>
<th>To</th>
<th>Distance [km]</th>
<th>From</th>
<th>To</th>
<th>Distance [km]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>9</td>
<td>595</td>
<td>6</td>
<td>7</td>
<td>145</td>
</tr>
<tr>
<td>1</td>
<td>10</td>
<td>405</td>
<td>6</td>
<td>11</td>
<td>145</td>
</tr>
<tr>
<td>1</td>
<td>12</td>
<td>465</td>
<td>7</td>
<td>8</td>
<td>240</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>240</td>
<td>7</td>
<td>11</td>
<td>100</td>
</tr>
<tr>
<td>2</td>
<td>9</td>
<td>610</td>
<td>8</td>
<td>12</td>
<td>180</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>155</td>
<td>9</td>
<td>12</td>
<td>210</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td>185</td>
<td>10</td>
<td>11</td>
<td>320</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>135</td>
<td>10</td>
<td>12</td>
<td>290</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>280</td>
<td>11</td>
<td>12</td>
<td>295</td>
</tr>
<tr>
<td>5</td>
<td>11</td>
<td>95</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

After the occurrence of \( f_1 \). As the fault currents approach steady-state (after approximately 300 ms), the maximum CB current in scenarios (c) and (d) is notably lower compared to those in topologies (a) and (b). The primary reason for this is that in topologies (c) and (d), the active short circuit current contributions feed the fault from two sides, reducing the maximum burden placed on individual feeders (and DC CBs).

The lower part of Fig. 7.3 is a magnified view of the first 6 ms of the same quantities as those shown in the upper part. In contrast to the steady-state case, in this initial transient period the maximum short circuit current is highest in topologies (c) and (d). This is because of discharge currents from cables that connect node 1 to nodes 9 and 12, which only exist in scenarios (c) and (d). Since the fault is closest to node 1, the maximum fault DC CB current initially occurs in the feeder from node 1 to \( f_1 \) in all four topologies. In topologies (a) and (b), the CB current from node 10 to \( f_1 \), i.e. \( i_{10-f_1} \), starts exceeding \( i_{1-f_1} \) shortly after the fault surge reaches node 10 (c.f. arrow on lower part of Fig. 7.3). The location of the maximum CB current then briefly alternates between \( i_{1-f_1} \) and \( i_{10-f_1} \), before
remaining at $i_{10-f1}$ until steady-state. In topology (c), $i_{1-f1}$ remains the maximum system current until approximately 20 ms after the fault, after which $i_{10-f1}$ slightly exceeds it. Finally, in grid (d), $i_{1-f1}$ remains the maximum CB current during the entire simulation.

A snapshot of the system fault currents and DC node voltages after 5 ms (equivalent to the break time of current hybrid DC CBs [CBHJ12]), is shown in Fig. 7.4. It further illustrates how at that particular point in time, the fault currents $i_{1-f1}$ and $i_{10-f1}$ in (a) and (b) are nearly identical, whereas in (c) and (d) $i_{1-f1}$ is clearly highest. Additionally, Fig. 7.4 gives the corresponding node voltages,
showing that after 5 ms, in grids (a) and (c) the voltage at the remote node 6 is not yet affected by the fault, whereas in (b) and (d) it is. This difference can be attributed to the absence of the link between nodes 10 and 11 in grids (a) and (c).

Figure 7.4: System snapshot comparison of the four different grid topologies 5 ms after the occurrence of fault 1

Fault 2

In Fig. 7.5, the global maximum DC CB current is shown for the four different topologies. In all four scenarios, the entire grid’s short circuit current is fed to f2 through the connection from node 10 (with the exception of the contribution from the peripheral node 3). Current $i_{10-f2}$ is thus clearly the maximum global DC CB current
in all four scenarios (c.f. Fig. 7.6). Its magnitude can therefore be fully attributed to the effect of the different DC grid topologies.

![Graph showing the global maximum DC CB current after a fault at location f2.](image)

**Figure 7.5:** Global maximum DC CB current after a fault at location f2

As the system approaches a steady-state, the fault current contribution from the four topologies in the order of weakest to strongest is: (c) ring, (a) radial, (b) lightly meshed, (d) densely meshed. This reflects differences in the average impedance between f2 and the active fault current sources, i.e. the AC coupling points.

Another feature that stands out in Fig. 7.5 is the fact that the maximum CB current in grid (d) is somewhat higher than in the other three grid scenarios during the first 10 ms (c.f. lower part of
7.1 Transient Fault Currents and Voltages

Fig. 7.5). This is because the initial response is dominated by the discharge of cable capacitances, of which there are more in grid (d) than in the other scenarios. Figure 7.6 shows that the maximum CB current after 5 ms ranges between 9.92 kA in topology (c) and 12.7 kA in topology (d). It can also be seen that the dense mesh of topology (d) leads to voltages in Area 1 that are around 10% higher than those in the other three topologies (after 5 ms).

Figure 7.6: System snapshot comparison of the four different grid topologies 5 ms after the occurrence of fault 2

Fault 3

Fault 3 constitutes one of the worst case scenarios: a fault directly at the terminal at one of the central nodes of the network. The fault is on the same cable as f1, but directly at the bus bar of node 10.
Fig. 7.7 shows the global maximum CB current for the four different scenarios. It can clearly be seen that the initial rates of rise and steady-state values of the fault current are more severe compared to those in the other two fault scenarios (c.f. Fig. 7.3 and Fig. 7.5). For example, the worst case CB current after 300 ms is more than 50% higher than that for f1 and more than 17% higher than for f2.

![Graph showing global maximum DC CB current](image)

**Figure 7.7:** Global maximum DC CB current after a fault at location f3.

The fast rate of rise is primarily due to the near instantaneous start of discharge currents from non-faulty feeder cables connected to node 10. The higher steady-state currents are primarily due to higher AC contributions caused by the proximity to node 10 as well
as to several onshore nodes.

The lower part of Fig. 7.7 shows that the fault current during approximately the first 1.5 ms is solely determined by the number of feeder cables connected to node 10, with the lowest fault currents for grid (c) (4 feeder cables at node 10) and the highest for grids (b) and (d) (6 feeder cables at node 10).

The differences between the four grid scenarios with regard to the steady-state fault current can be explained by the differences in the fault current distribution in the grid and differences in the impedance between other coupling points and the fault. The discontinuity in the maximum CB current after 1.5 ms (a slight increase for topology (d) and a decrease for the other three topologies) corresponds to the time when the reflection of the negative voltage wave from node 4 arrives at node 10 with a positive polarity. This leads to a sudden reduction of the contribution from this particular cable. Subsequent ripples between 1.5 ms and around 2.2 ms can similarly be attributed to the arrival of the reflected fault waves from nodes (2) and (3) (particularly notable for topology (a)). The shape of the CB current in topology (d) looks different during this phase due to different reflection coefficients at nodes 2 and 4 (due to a different number of feeders attached at these bus bars). The CB currents start to increase again at around 2.5 ms due to fault current contributions from AC nodes.

Figure 7.8 shows a snapshot of the system’s fault currents and DC voltages after 5 ms. It is important to note that in this figure, the global maximum system current (i.e. $i_{10-f3}$) is not represented. It illustrates the location and magnitude of the second highest line currents and gives an impression of the fault current distribution in each topology.

**Direct Comparison**

Table 7.4 provides a direct comparison of the total fault current (i.e. fault-to-ground current) and the maximum CB current in the grid for the three fault locations and four grid topologies. Values are
Effect of DC Network Topology

Figure 7.8: System snapshot comparison of the four different grid topologies 5 ms after the occurrence of fault 3.

given at a time of 5 ms (equivalent to typical hybrid DC CB break time) and 50 ms (equivalent to typical mechanical resonance breaker break time).

Considering all grid topologies and fault locations, the maximum prospective CB current after 50 ms is on average 40% higher compared to that after 5 ms. Furthermore, on average, there is a 21% difference in the maximum CB current between the grid with the lowest average CB current (grid (c)) and that with the highest average CB current (grid (d)).

Another general observation that can be made is that the closer a fault is to a terminal, the higher is the ratio of the maximum CB current to the total fault current.
Table 7.4: Total fault current and maximum DC CB current after 5 and 50 ms for different topologies and fault locations

<table>
<thead>
<tr>
<th></th>
<th>5 ms</th>
<th>(a)</th>
<th>(b)</th>
<th>(c)</th>
<th>(d)</th>
</tr>
</thead>
<tbody>
<tr>
<td>f1</td>
<td>total fault current [kA]</td>
<td>12.38</td>
<td>12.65</td>
<td>13.07</td>
<td>14.87</td>
</tr>
<tr>
<td>f1</td>
<td>max CB current [kA]</td>
<td><strong>5.86</strong></td>
<td><strong>5.85</strong></td>
<td><strong>7.07</strong></td>
<td><strong>8.41</strong></td>
</tr>
<tr>
<td>f2</td>
<td>total fault current [kA]</td>
<td>15.65</td>
<td>16.73</td>
<td>15.15</td>
<td>17.93</td>
</tr>
<tr>
<td>f2</td>
<td>max CB current [kA]</td>
<td><strong>10.51</strong></td>
<td><strong>11.61</strong></td>
<td><strong>9.92</strong></td>
<td><strong>12.74</strong></td>
</tr>
<tr>
<td>f3</td>
<td>total fault current [kA]</td>
<td>21.11</td>
<td>23.08</td>
<td>20.30</td>
<td>24.76</td>
</tr>
<tr>
<td>f3</td>
<td>max CB current [kA]</td>
<td><strong>19.97</strong></td>
<td><strong>22.00</strong></td>
<td><strong>17.99</strong></td>
<td><strong>22.40</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>50 ms</th>
<th>(a)</th>
<th>(b)</th>
<th>(c)</th>
<th>(d)</th>
</tr>
</thead>
<tbody>
<tr>
<td>f1</td>
<td>total fault current [kA]</td>
<td>17.53</td>
<td>17.97</td>
<td>19.55</td>
<td>21.51</td>
</tr>
<tr>
<td>f1</td>
<td>max CB current [kA]</td>
<td><strong>11.33</strong></td>
<td><strong>11.77</strong></td>
<td><strong>10.01</strong></td>
<td><strong>11.87</strong></td>
</tr>
<tr>
<td>f2</td>
<td>total fault current [kA]</td>
<td>22.98</td>
<td>23.97</td>
<td>22.33</td>
<td>24.15</td>
</tr>
<tr>
<td>f2</td>
<td>max CB current [kA]</td>
<td><strong>17.29</strong></td>
<td><strong>18.46</strong></td>
<td><strong>16.54</strong></td>
<td><strong>18.73</strong></td>
</tr>
<tr>
<td>f3</td>
<td>total fault current [kA]</td>
<td>27.61</td>
<td>29.62</td>
<td>26.42</td>
<td>30.02</td>
</tr>
<tr>
<td>f3</td>
<td>max CB current [kA]</td>
<td><strong>24.49</strong></td>
<td><strong>26.78</strong></td>
<td><strong>22.07</strong></td>
<td><strong>27.00</strong></td>
</tr>
</tbody>
</table>

7.1.5 Conclusions

While the choice of network topologies for future DC offshore grids will be strongly influenced by their economic merits under normal operation, the impact of the topology on the performance requirements of DC CBs cannot be neglected since the availability of technically and economically viable DC CBs is crucial for the feasibility of DC grids. Different grid topologies do not only lead to different fault current levels but, depending on the resulting distribution of fault currents in the network, also impact the maximum burden placed on individual CBs. Generally, it can be concluded that topologies that are advantageous for system redundancy and flexible trading, i.e. meshed networks, tend to be disadvantageous from a maximum fault current point of view.

For the three considered fault locations, the average maximum
CB current is highest in the densely meshed grid (d), followed by the lightly meshed grid (b), the radial grid (a) and the ring shaped grid (c).

The ring shaped grid shows a favorable performance in terms of maximum CB currents because its structure leads to a favorable distribution of the fault currents for the majority of possible fault locations. Furthermore, the high impedance between different areas leads to lower average steady-state fault current levels. For the particular topologies that have been considered, the ring shaped grid offers the same level of redundancy as the lightly meshed grid (b) with respect to power transfer between areas 1, 2, and 3. A disadvantage of this topology is that, depending on the exact trading patterns, it is likely to lead to higher power losses for inter-area trading.

In general, the maximum breaking current ability of a DC CB needs to be designed primarily with regard to its own interruption time and its location in the grid. A fast interruption time is generally favorable. Shortly after the fault, fault currents are more predictable because they primarily depend on passive elements such as cable capacitances, i.e. they are independent of operating conditions of AC coupling points. Furthermore, fault currents are likely to increase over time (of course, depending on the number, strength, and distribution of AC coupling points). In the case of terminal faults, DC CBs located at busbars that connect to multiple energized cables are subject to particularly high fault currents and rates of rise. Thus, the characteristics of CBs need to be chosen according to their location in the grid. Different CB technologies and specifications may co-exist in the same network. The main parameters that need to be considered for a holistic assessment are interruption speed, maximum breaking current, investment costs, and on-state losses.

In the future, the assessment of different topologies with regard to their fault protection requirements could be improved by considering additional fault locations and incorporating a weighting method
that depends on the likelihood of occurrence and impact of particular faults. Converters that are sufficiently far away from the fault may continue operating normally and their control behavior may affect the network’s overall fault response. The results presented in this study for fault currents shortly after the fault (i.e. first 5 ms) should not be influenced by this assumption. The validity of results for longer time frames may have to be verified with more detailed converter models with clear blocking criteria and realistic control characteristics.

7.2 Steady-State and Transient Behavior

7.2.1 Introduction

A DC network topology cannot be specified considering only the maximum transient fault currents as discussed in Section 7.1, but also the behavior under normal operation and after fault clearance have to be taken into account. Important network designing aspect regarding normal operation are the total losses of the network and the flexibility for the dispatching. Post-fault contingencies may reduce the reliability and security of the network and alternative, parallel lines for the re-routing of the power flows have to be available.

In contrast to Section 7.1, this section does not focus only on the influence of the DC network topology on the transient behavior, but discusses its influence on the overall system including the steady-state system losses in the combined AC-DC network and possible contingencies after the fault clearance.

Therefore, simulations are performed in a North Sea MTDC cable network with 12 terminals based on the proposed North Sea Supergrid described in [Eur09]. This DC network is coupled to three fictitious, simplified, asynchronous AC network areas in the UK, continental Europe, and Scandinavia, allowing for power trading between the AC areas. Three of the MTDC network terminals
are placed offshore and connected to large wind farms, whose power infeed varies. Four different DC network layouts are considered: radial, ring shaped, lightly meshed, and densely meshed. For each topology, three successive simulation steps are performed, one for the steady-state losses, one for transient overcurrents for three different ground fault scenarios, and one for the post-fault contingencies after fault clearance.

To evaluate the steady-state losses and to find possible post-fault contingencies, the steady-state Optimum Power Flow (OPF) in the combined AC-DC system, which minimizes the system losses, is calculated as will be explained in the next section. The OPF is an important power system planning tool, which has been used for decades in case of AC systems, but has not been adapted to combined AC-DC system until recently. A sequential AC-DC power flow algorithm with fixed infeeds is described in [BCB10] and an adaptation with variable power can be found in [WA12].

### 7.2.2 Methodology

For each simulation, an OPF calculation is performed first, whose resulting voltages and currents are used as initial values for the subsequent transient simulations of a pole-to-ground fault. The methodology of the two simulation steps is explained in the following paragraphs.

**Steady-State Simulation**

The method used to calculate the states and power flows in the whole grid is described in detail in [WA12]. The combined AC and HVDC OPF is based on models for the AC grid, the converters, and the DC grid, which are calculated simultaneously using an overall optimization routine. No master or local control of the converter set points is required in this steady-state optimization study and converter dynamics are neglected.
7.2 Steady-State and Transient Behavior

The AC grid flows are calculated according to the full flow equations and summed up at each node:

\[ P_{km} = U_k^2 G_{km} - U_k U_m G_{km} \cos(\theta_k - \theta_m) \]
\[ - U_k U_m B_{km} \sin(\theta_k - \theta_m) \] (7.2)

\[ Q_{km} = -U_k^2 (B_{km} + B_{km}^{sh}) + U_k U_m B_{km} \cos(\theta_k - \theta_m) \]
\[ - U_k U_m G_{km} \sin(\theta_k - \theta_m) \] (7.3)

Fig. 7.9 shows the model used for the VSC converters. An AC node (AC,c) with a short AC line is added to the AC node k, where the converter is placed. This line represents the transformer located between the node and the terminal. The new grid variables \( U_c \) and \( \theta_c \) can be used to determine the active and reactive power flow through the terminal.

\[ P_{loss} = P_{AC} + P_{loss} + P_{DC} = 0 \]

**Figure 7.9: VSC HVDC converter model [WA12]**

Since the steady-state condition is investigated in these simulations, the DC grid is modeled by resistive lines only. The DC cable resistance is derived from the cable model as used in the transient simulations described in the following paragraph.

The three parts briefly described above are merged into a single, nonlinear optimization problem. To minimize the losses in the grid, the objective function is chosen in order to minimize the active power
production.

The physical limits of the grid are represented by the constraints. The sum of the active and reactive power in each node has to be zero. The power on both sides of a converter and the losses in the converter itself also has to add up to zero. Inequality constraints ensure that the AC and DC voltage levels, the line loadings, and the active and reactive power production of the generators remain within fixed limits.

**Transient Simulation**

Identical converter and cable models as described in Sections 4.1 and 4.4.1, respectively, are used for the transient simulations. No fault current flows through AC lines parallel to DC lines are considered. The equivalent short-circuit impedance is calculated based on the short-circuit capacity of the AC network adjacent to the PCC. The pre-fault power flow conditions resulting from the steady-state simulation are established through constant voltage sources during the pre-fault setup period. After the fault has occurred and the current at the terminal exceeds 2 p.u., the converters are switched to uncontrolled rectifiers as it would happen in real half-bridge based systems, when the overcurrent protection blocks the IGBTs for safety purposes [YFO10]. The DC voltage filtering need is assumed to be low and, hence, small filter capacitors of only 1 µF are required at the DC side of each converter. This mitigates the domination of the large initial discharge currents of the concentrated filter capacitors over the distributed cable capacitances [BF13b] and allows, consequently, for a better comparison of the different DC network topologies.

### 7.2.3 Network Topologies and Fault Scenarios

This section describes the four proposed DC network topologies for a North Sea offshore grid and the models of the adjacent AC networks, as well as the three fault scenarios. The North Sea and its
surrounding countries have been selected for this study due to the already extensive employment of offshore wind power and expansion plans in this region [Lin11].

**AC Network**

The offshore DC grid is connected to a simplified model of an European AC grid as depicted in Fig. 7.10. The lines, loads, and generators are patterned on a reduced European grid map. The AC network consists of three separate, asynchronous network areas: a smaller network located in the UK, a large continental network, and a Scandinavian network, which is simplified to a single node. The grid voltage level was chosen to be 380 kV to reflect the highest level of the transmission grid, to which the DC grid will most probably be connected. Each node in the AC network represents a sub-area and has, therefore, rather high values of concentrated generation and load as listed in Table 7.9 in the Appendix. The AC line parameters are chosen from [Kun94].

The smaller UK grid in the North West has 14 nodes and 19 lines. Its lines are between 55 km and 285 km long. The 4 generators cannot provide enough energy to supply the whole load in this scenario, hence, the 3 converter stations connected to the DC grid have to import power. Each UK node provides around 11.7 GW of short circuit power.

The larger continental AC grid comprises 23 nodes and 52 lines. On average, these lines are a little longer compared to the UK network. They have lengths between 65 km and 435 km. There is an excess in generation capacity in this area and the grid has the possibility to export power via the 5 connected converter stations into the DC grid. The continental network is stronger than the UK grid with about 43 GW of short circuit power at each node.

Node 1 has a fixed generation and represents the Scandinavian grid, which is assumed to have excess power to export.

The average distance the power has to flow from the generation to the load is rather long, therefore, the overall losses of the AC grid
are high.

Figure 7.10: AC networks (red) combined with offshore DC grid (green)

**DC Network**

Four different DC grid topologies are investigated: radial, ring, lightly meshed, and densely meshed. As illustrated in Fig. 7.11, all DC topologies comprise the same AC coupling points connected through 9 converter stations. Three wind parks (node numbers 43, 44, and 45) with fixed infeed are located in the DC network. The
DC cable resistivity used in the OPF is 0.012304 Ω/km.

- **Radial Grid**
  Due to its simplicity and low investment cost, the radial topology will most likely be applied to a first offshore grid. It is designed like a star with the three wind parks in the center. This option (Fig. 7.11 A) comprises only 11 DC cables, the least number among all considered topologies, with a total length of 2270 km. In this topology, the converters are connected to only one DC cable and no DC bus bars are needed. The reliability is lower than in the other investigated topologies and it is likely to lose a complete converter station in case of a DC side fault. The radial network is assumed to be the base configuration for this study.

- **Ring Shaped Grid**
  The ring topology (Fig. 7.11 B) connects all converter stations and wind parks in a serial circuit resulting in two DC cables per converter station. This sums up to 12 DC lines, which have a total length of 2660 km. The advantage of this topology is the simplicity for construction and operation. Obviously, the ring topology has low reliability and high losses due to the long transmission distances.

- **Lightly Meshed Grid**
  To slightly increase the reliability compared to the radial topology, a lightly meshed grid is investigated as well, as shown in Fig. 7.11 C). The additional line compared to the radial topology increases the total line length to 2590 km. The security is only marginally increased compared with the radial network.

- **Densely Meshed Grid**
  The last topology is a densely meshed grid as illustrated in Fig. 7.11 D). Additional cables are added to the grid and the
total number of cables increases to 19 with a total length of 5185 km. The drawback of this topology is the higher cost for the long cables compared with the other topologies. The densely meshed grid increases the reliability, provides more flexibility for power exchange between the AC areas, and reduces the shortest connection distance between two points in the grid.

Figure 7.11: DC network topologies: A) radial, B) ring, C) lightly meshed, D) densely meshed

Fault Scenarios

Three different ground fault locations marked by red arcs in Fig. 7.11 are considered: a ground fault (F1) 1 km away from the offshore terminal 43 on the cable connecting 43 and 4, a fault (F2) close to the strong AC coupling point 4 on the same cable, and a fault
(F3) on the cable connecting nodes 44 and 8 close to a weak AC coupling point 8. Faults F2 and F3 are located 30 km and 50 km away from terminal 4 and 8, respectively. In all fault scenarios, a constant fault resistance $R_f$ of 7$\Omega$ is assumed, which corresponds to the ground resistance of a sparking ground connection in wet, loamy sand at the current peak of 19.35 kA [WLD05]. The dependence of the fault resistance on the fault current is neglected in all the simulations. The prospective fault currents are measured at the feeder CB locations at cable $43 \rightarrow 4$ in case of F1 and F2 and at cable $44 \rightarrow 8$ during F3.

### 7.2.4 Simulation Results

Pre-fault steady-state, transient, and post-fault steady-state simulations have been performed for all scenarios and topologies, whose results are presented in the following.

#### Pre-Fault OPF

For the four topologies, all generators in the UK grid are nearby or at their capacity limits. The additional load of about 22.4\% of the UK power is imported over the DC grid. Therefore, converters 7, 8 and 9 are mainly importing as shown in Fig. 7.12 in per unit with a base power of $S_b = 1$ GW. In continental Europe, converter station 2 imports power from the DC grid and all other converters export power into the DC grid. The wind park nodes have the same power infeeds for all topologies. The resulting active power losses are indicated in Table 7.5, which reveals that the overall system losses are dominated by the converter and the AC line losses in all topologies.

- **Radial Network**

  None of the DC cables reaches its capacity limit of 0.9 p.u., but the capacity margins of cables 9 to 44 and 7 to 45 are small. Similar to the highest line loading, the converter at node 7 has
the highest loading of all terminals as given in Table 7.6. The active power losses of the system are summarized in Table 7.5.

- Ring Network

The ring topology results in a completely different OPF. It is the only case, where node 1 is not at the maximum DC voltage level, but node 3 instead. On the other side of the DC grid, the lowest voltage level is at node 9, which is also the most loaded node with an import of over 1 p.u.. The DC grid reaches its limitation as the cable from node 45 to 7 is at its capacity limit. The power flows in the other lines are far below their limits. The overall losses are the highest among all topologies: the increase in the losses is about 4% in the DC network and about 7% in the continental grid compared with the base case. The power flows through the converters are significantly distinct from all other topologies.
7.2 Steady-State and Transient Behavior

- Lightly Meshed Network

The lightly meshed topology gives almost the same results as the radial network. This is not surprising due to the similar layout. The individual power losses and flows are almost equal to the radial network and the overall losses are reduced by only 0.26%. A larger difference can be found in the DC line loadings, which could be reduced by 2.88%. There is a slight change in the infeed from converters 5 and 6.

- Densely Meshed Network

The densely meshed topology has the lowest overall losses that are about 3.7% lower than in the radial topology. The most significant difference is in the DC grid power losses, which are reduced by more than 50% due to the shorter transmission distances. This results in the smallest DC voltage differences between the nodes. In this case, it is even possible to transfer more power from the wind parks through the DC grid to the UK than actually required and allows for the reduction of the loading of one of the UK’s generators.

<table>
<thead>
<tr>
<th>Table 7.5: Pre-Fault Active Power Losses in the Grid [p.u.]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Grid</td>
</tr>
<tr>
<td>Converters</td>
</tr>
<tr>
<td>Radial</td>
</tr>
<tr>
<td>Ring</td>
</tr>
<tr>
<td>Lightly Meshed</td>
</tr>
<tr>
<td>Densely Meshed</td>
</tr>
</tbody>
</table>
### Table 7.6: Line Loadings [p.u.]

<table>
<thead>
<tr>
<th>Topology</th>
<th>Highest loaded DC line</th>
<th>Power transfer</th>
<th>Highest loaded AC line</th>
<th>Power transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radial</td>
<td>44 to 9</td>
<td>0.84835</td>
<td>12 to 11</td>
<td>0.76390</td>
</tr>
<tr>
<td>Ring</td>
<td>45 to 7</td>
<td>0.89497</td>
<td>12 to 11</td>
<td>0.74683</td>
</tr>
<tr>
<td>Lightly Meshed</td>
<td>99 to 9</td>
<td>0.84568</td>
<td>12 to 11</td>
<td>0.76703</td>
</tr>
<tr>
<td>Densely Meshed</td>
<td>45 to 7</td>
<td>0.56504</td>
<td>12 to 11</td>
<td>0.71120</td>
</tr>
</tbody>
</table>

### Transient Simulations

The development of the prospective fault current in the CB at cable 43 → 4 next to terminal 43 during fault 1 is depicted in Fig. 7.13 for the 4 topologies. Right after the fault occurrence at 0 ms, a very steep peak can be observed due to the discharge of the concentrated filter capacitor of the converter at terminal 43 and the distributed cable capacitances of the neighboring feeders at the same bus. The forward and backward traveling surges result in subsequent smaller peaks. After the capacitor has been discharged, the current decreases, followed by a gradual increase due to the AC infeeds through the converters. To estimate the amplitude of the short circuit current that a CB needs to interrupt, two grey lines are plotted in Fig. 7.13. Full solid state or fast hybrid CBs would break the current within about 2 ms (indicated by the thick grey line "S"), but these CB types typically have high on-state losses. Metal contact CBs, such as active or passive resonance CBs have almost no on-state losses, but the break time is about 50 – 60 ms as indicated by "R" [BWPF12]. Fig. 7.14 illustrates the maximum fault currents at the fault location and their individual shares that flow through the DC CBs at both ends of the faulty cable. The maximum currents are indicated for each fault scenario and DC network topology, as well as for the two different DC CB technologies. The
maximum fault currents correspond to the sum of the current flows at both ends of the cable. In Fig. 7.14, the bars corresponding to the maximum currents in the CB closest to the fault are opaque and the values of the remote CB are shown with stacked, transparent bars. The topologies are distinguished by the following bar colors: blue (radial), cyan (ring), yellow (lightly meshed), and red (densely meshed).

![Graph showing current vs time for different topologies](image)

**Figure 7.13:** CB current at terminal 43 during fault 1 - S: solid state CB, R: resonance CB

- **Fault 1**

  This fault is the most severe amongst the three scenarios and results in the highest fault currents, as can be seen in Fig. 7.14 (left). The ring topology has the lowest fault current level and the densely meshed configuration the highest fault current contributions. The radial and lightly meshed layouts result in slightly lower fault current levels as compared to the densely meshed configuration.
Figure 7.14: Maximum fault current and individual CB currents for solid state CB (S) and resonance CB (R) - opaque bars: CB closest to fault; stacked, transparent bars: remote CB

meshed topology. The CB at terminal 43 (opaque bars) has to withstand almost the entire fault current given the location very close to the fault. The breaking currents at both ends of the cable are increased moderately for longer breaking times except in the ring topology, where a larger breaking time leads to a lower maximum at terminal 43.

- Fault 2

A ground fault close to a strong AC coupling point results in lower total fault currents than in fault 1. The same tendencies as in fault scenarios 1 can be observed in Fig. 7.14 (center) in terms of current increase with an increase in the breaking time. The densely meshed topology yields the highest values of total fault current, whereas the ring shaped network results in the lowest contributions. In contrast to the previous fault 1, the ring network (cyan) has a relatively high total fault current
level in comparison to the other topologies. The radial (blue) and the lightly meshed (yellow) topologies lead to no increase in the maximum breaker current at terminal 4 (opaque bars) with an increase in the interruption time, whereas a considerable increase can be observed in the other two topologies. The opposite is true for the remote CB at terminal 43 (transparent bars).

- **Fault 3** The ground fault close to a weak AC coupling point (cf. Fig. 7.14 (right)) yields a similar result of the maximum fault currents as compared to fault 2, whereas the overall fault current levels are reduced as expected. In contrast to the previous two scenario, the lightly meshed topology (yellow) performs slightly better than the radial grid (blue). The ring shaped network (cyan) remains the topology of choice and the same fault current distribution among the CBs at both ends of the faulty cable as during fault 2 is observed.

**Post-Fault OPF**

It is assumed that the fault is cleared by opening the DC CB at both ends of the faulted cable. Since the fault is permanent, it is not possible to re-close the CBs and a re-dispatch of the power flows is required. The connected VSC converter is still in operation to provide reactive power to the AC network, even if there is no more a DC line connected to.

- **Fault 1 and 2**

After fault 1 and 2, the cable between node 43 and 4 has been disconnected and the same post-fault OPFs are achieved for both fault scenarios. In the radial topology, as indicated in Table 7.7, the power flows and losses remain almost the same before the fault and after fault clearance due to the negligible pre-fault power flow through converter 4 as seen in Fig.
7.12. The lightly meshed topology is similar to the radial layout. The small input to the DC grid at converter 4 is mainly shifted to converter 3. The overall system losses are marginally increased.

More significant changes occur in the ring topology. The highest DC voltage is shifted from node 3 to 43, since this wind park is now only connected through a single line. The infeeds at all continental terminals are increased except for node 3, where it has decreased. Node 2 has almost doubled its export to the DC grid. This leads to different infeeds into the UK grid: the power flow through converter 7 and 9 has decreased and in node 8 increased. The post-fault system losses are 2% smaller due to the lower losses in the continental AC grid, which have declined by 5.4% given the higher flexibility in the open ring topology. In addition, the DC lines have 7.5% lower losses, whereas the converter losses remain equal and the losses in the UK AC grid increase slightly.

The densely meshed topology can compensate for the loss of the faulted cable without major disturbance in the system, therefore, the flows and overall losses in the grid are similar for the pre- and post-fault OPF.

- Fault 3

After fault 3, the connection between node 44 and 8 is opened. The radial and lightly meshed topology cannot provide the required imports to the UK grid anymore due to the power limitation of the remaining DC cables. Major disturbances including load-shedding and power outages are likely. The wind park at node 44 provides the required imports in the ring topology. As after fault 1 and 2, the open ring is more flexible than the closed one and, hence, the losses are slightly smaller. The power flows in the densely meshed topology can be rerouted through many alternative lines. This results again in an almost equal flow and loss situation as before the fault.
Table 7.7: Changes in Active Power Losses after the Fault [%]

<table>
<thead>
<tr>
<th>Fault</th>
<th>DC Grid Converters</th>
<th>DC Grid Lines</th>
<th>AC Lines UK</th>
<th>AC Lines Continental</th>
<th>Total Losses</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 and 2</td>
<td>Radial</td>
<td>-0.020</td>
<td>0.007</td>
<td>0.023</td>
<td>0.028</td>
</tr>
<tr>
<td></td>
<td>Ring</td>
<td>-0.070</td>
<td>-7.547</td>
<td>1.119</td>
<td>-5.419</td>
</tr>
<tr>
<td></td>
<td>Lightly Meshed</td>
<td>0.032</td>
<td>-0.842</td>
<td>0.002</td>
<td>0.260</td>
</tr>
<tr>
<td></td>
<td>Densely Meshed</td>
<td>-0.180</td>
<td>10.145</td>
<td>0.548</td>
<td>0.074</td>
</tr>
<tr>
<td>3</td>
<td>Ring</td>
<td>1.277</td>
<td>-5.971</td>
<td>-0.743</td>
<td>-4.928</td>
</tr>
<tr>
<td></td>
<td>Densely Meshed</td>
<td>0.562</td>
<td>12.680</td>
<td>-0.369</td>
<td>-0.274</td>
</tr>
</tbody>
</table>

7.2.5 Comparison and Discussion

The results achieved in this study are summarized in Table 7.8. The different topologies are ranked according to their performance from the best result (1) to the worst (4). The results for steady-state and transient performance are not congruent as discussed in the following paragraphs. There is no optimal network topology, which minimizes steady-state losses and transient overcurrents at once, and each topology has its drawbacks.

Table 7.8: Comparison of Performance

<table>
<thead>
<tr>
<th></th>
<th>Pre-Fault OPF</th>
<th>F1</th>
<th>F2</th>
<th>F3</th>
<th>Post-Fault OPF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radial</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>Ring</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Lightly Meshed</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Densely Meshed</td>
<td>1</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>1</td>
</tr>
</tbody>
</table>
**Steady-state operation**

The preferred scheme for the optimal power flow and overall losses is the densely meshed grid. After the fault, only minor changes occur in this topology. This is a clear operational advantage over all other topologies. A major drawback is the increased total cable length, which leads to much higher costs compared with other topologies. The radial and lightly meshed grid yield similar power flow results given their almost equal structure. The additional line in the lightly meshed network provides marginally better results. The comparison of pre- and post-fault results in the ring topology exhibits an interesting aspect: before the fault occurs, the ring is inflexible due to the fixed voltage distribution. It results in the highest losses amongst the considered topologies. After one line is disconnected, however, the degree of freedom is increased and a better solution can be found.

The radial topology will most likely be applied to a first offshore grid connecting large wind parks. This grid will be mainly used to transfer the offshore produced power to the onshore grids. To increase the capacity for the power exchange between the grids, particularly during no-wind conditions, and enhance the reliability and flexibility, the grid has to be transformed in a lightly meshed network in a next step. Later on, it has to be investigated, which level of meshing is reasonable for a further increase of capacity and reliability and expands the network towards a densely meshed grid.

**Transient overcurrents**

As shown in Fig. 7.14, the total fault current, i.e. the total height of the bars, increases with decreasing distance to the fault and increasing short circuit capacity of the AC network at the PCC of the onshore terminals (cf. node numbers 1-9 in Fig. 7.10). Therefore, fault 1 has the highest values (1 km between CB and fault) and fault 3 the lowest values (weak AC node and 50 km between CB and fault).
In all fault scenarios and topologies, a faster solid state CB would have to break a lower fault current than a slower resonance CB. The reason for that is the low initial discharge peak given the small DC filter capacitor size in this setup and the slow increase of the AC infeed currents limited by the AC impedances. As depicted in Fig. 7.13, the fault current still increases after 50 ms. The steady-state fault current is reached after 200 – 300 ms and thus, a slower CB would have to break an even higher current than the resonance CB.

In terms of total fault current level, the ring topology performs best among all topologies considered in this study. The reason for the good performance of the ring network is the low and evenly distributed number of feeders per busbar at the terminals. Fewer feeders at the busbars reduce the total distributed cable capacitance that may be discharged through the busbar and CB into the ground fault, as well as the lower short circuit power at the specific node given the reduced number of connections to the onshore AC nodes. Moreover, the ring reduces considerably the maximum current in the closest CB at terminal 43 during fault 1 at the cost of an increased maximum value in the remote CB at terminal 4. This is due to the equal number of feeders and similar short circuit power at the two terminals of the faulted cable.

The densely meshed topology, in contrast to the ring network, exhibits the highest fault current values due to the increased number of feeders per busbar and shorter transmission distances to the AC nodes.

The ring and densely meshed grid are unfavorable for the CBs close to fault 2 and 3 at terminals 4 and 8, respectively, whereas the radial and lightly meshed network support them, particularly in case of long breaking times. The additional connections at the network’s periphery in the ring and densely meshed networks lead to a re-distribution of the fault current at both terminals of the faulted cable and yield higher breaking currents in the closest CBs on one hand and lower currents in the remote CB on the other hand.
7.2.6 Conclusions

This section has discussed aspects of steady-state OPF and transient simulations in a large, combined AC/DC network. The simulations have been performed for four different DC network topologies and three different ground fault locations. All scenarios have been evaluated and compared in terms of overall system losses, transient fault currents, and post-fault contingencies. It has been demonstrated that an evaluation of grid topologies has to be done taking into account all of the aforementioned aspects. On the one hand, a ring shaped topology performs best in terms of transient overcurrents due to the low and equally distributed number of feeders per busbar, but has large overall system losses in the steady-state operation given the long transmission distances and the low number of cables. After clearing the fault and disconnecting the faulted cable, contingencies are very likely. On the other hand, a densely meshed grid provides low system losses, but high transient overcurrents, because of the increased number of feeders per busbar and short transmission distances to strong AC nodes. In terms of reliability and flexibility for power exchange, it is the best choice, whereas the investment costs are highly elevated due to the large number of cables and high converter ratings. Moreover, the short circuit power at the onshore AC nodes has to be considered in order to reduce fault current levels. No DC topology can optimally satisfy all aspects at the same time and individual calculations have to be done for every network and power flow scenario. The impact of a change in the overall setup including AC networks and power flow scenarios, e.g. a DC overlay grid with several parallel AC lines, has to be investigated in future studies.

7.2.7 Appendix

See Table 7.9 for the bus data of the pre-fault system. The assumed base power is $S_b = 1 \text{ GW}$. 
### Table 7.9: Bus Data [p.u.]

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<th>Reactive Power Generation</th>
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Table 7.9 – continued from previous page
8 Effect of Grounding Scheme

8.1 Introduction

All studies presented in the precedent Chapters 5 to 7 assume a low-ohmic grounding of the MTDC network. This chapter presents additional MTDC grounding strategies for monopolar and bipolar MTDC cable configurations and compares them in terms of transient CB current and overvoltage at the healthy pole during single pole-to-ground faults based on simulations in PSCAD. Moreover, advantages and disadvantages of each grounding scheme regarding operation and costs are explained. The emphasis in this chapter is again on pole-to-ground faults, since they are regarded as significantly more frequent compared to pole-to-pole faults [CP11].

8.2 HVDC Configurations

In general, monopolar and bipolar system configurations are distinguished. Monopolar systems are intended for moderate power transfers and are the least expensive systems [BJ07]. Only one converter is used for each terminal. The asymmetric monopole as depicted in Fig. 8.1 with earth return is the simplest configuration. It requires only one fully insulated high-voltage conductor, but at the expense of a constant DC current through the ground that can cause corrosion of buried metallic structures such as pipes and earthing equipment of substations, transfer of high potentials, and saturation of transformers [JS10]. The use of a dedicated low-voltage neutral conductor (cf. Fig. 8.1, dashed line) mitigates the aforementioned problem, but requires the installation of two cables/lines and reveals
higher transmission losses and costs compared to systems with earth return [Cig13].

The symmetric monopole shown in Fig. 8.2 is the most popular configuration for point-to-point HVDC links. There are no ground currents during normal operation, but two fully insulated pole conductors have to be installed.

The bipolar configuration in Fig. 8.3 has a higher transmission capacity than the other systems and provides more flexibility and redundancy due to two independently controlled poles. After a ground fault or the loss of one converter, the bipole can still be operated as a monopole at reduced capacity. A metallic return (cf. Fig. 8.3, dashed line) is used again for the monopolar operation, if DC ground currents are not permissible. This solution results in higher costs compared to the earth return scheme because of the additional neutral cable.

**Figure 8.1:** Asymmetric Monopole Configuration - A): solid grounding (LRGND), B): high-impedance grounding (HLGND), dashed line: metallic return (MR) conductor
8.3 Grounding Practices

Analogous to AC networks, HVDC systems are grounded either through a low-ohmic connection or via a high impedance. The low-ohmic grounding has the advantage of reduced overvoltages at the healthy pole during a pole-to-ground fault, but suffers high overcurrents. In contrast, high-impedance grounding reduces the maximum currents, but results in high overvoltages up to twice the nominal voltage at the healthy pole. Due to the floating potential of the DC network given the delta configuration of the transformer secondary windings, the converters require an additional voltage reference [BJ07], [AXHC02]. This can be provided by the following practices [Cig13] as illustrated in Figures 8.1-8.3:

**Figure 8.2:** Symmetric Monopole Configuration - A): solid grounding (LRGND), B): high-impedance grounding (HLGND), C): high-ohmic grounding busbars (HRB), D): high-impedance grounding AC side (HLAC)
Figure 8.3: Bipole Configuration - A): solid grounding (LRGND), B): high-impedance grounding (HLGND), C): high-ohmic grounding busbars (HRB), dashed line: metallic return (MR) conductor

A) Solid earthing of DC capacitor neutral (LRGND)

B) Earthing of DC capacitor neutral via reactor (HLGND)

C) Connection of high resistances from both DC buses to earth (HRB)

D) Connection of high-impedance star point reactors on the AC side of the converters (HLAC)

8.3.1 Asymmetric Monopole

The MTDC network based on asymmetric monopoles can be grounded either low-ohmic at all terminals (Fig. 8.1 option A) or via a high-impedance reactor together with a dedicated metallic return (MR)
conductor as illustrated in Fig. 8.1 (option B). Using the latter option, the MTDC network can either be grounded at all terminals or at one terminal only, which serves then as voltage reference. Metal oxide surge arresters (MOA) are usually connected in parallel to the grounding reactors to avoid overvoltages [SHC00]. In metallic return operation, the non-grounded terminals are protected by MOAs and metallic return circuit breakers (MRTB) to clear faults on the neutral conductor [JS10], [HHH+01]. The grounding MOAs and MRTBs are not shown in Figures 8.1-8.3.

8.3.2 Symmetric Monopole

For the symmetric monopole network in Fig. 8.2, the DC capacitor midpoint can be earthed solidly (option A) or via a reactor (option B), the DC busbars can be connected to earth through a high-ohmic resistance (option C) or the converter side of the transformer can be grounded via a star point reactor (option D) as proposed in [CLP11], [DNSM13]. For all options, the network can be grounded at all terminals or at only one. MOAs are used again to avoid excessive voltages across the grounding reactors and at non-grounded capacitor midpoints.

8.3.3 Bipole

The proposed bipole options are: solid grounding of the capacitor midpoint (option A in Fig. 8.3), grounding through a reactor (option B), and high resistance DC busbar earthing (option C). If the bipole has to be capable of monopolar operation after a fault at one pole or the loss of one converter, the system has to be either solidly grounded at all terminals or in case of high-impedance grounding, a metallic return is required with grounding at one terminal. The DC capacitor midpoints at the other terminals are protected again by MOAs and MRTBs.
8.4 Simulation Setup

A description of the PSCAD models of the network and cables for the simulation study are presented in this section.

8.4.1 Converter and Network Model

The 3 terminal radial HVDC networks shown in Figures 8.1-8.3 are modeled in PSCAD. In all configurations, the cable connecting terminal 1 and 2 is 270 km long and the cable between terminal 1 and 3 has a length of 350 km. A pole-to-ground fault occurs 100 km away from terminal 1 assuming the worst case with zero fault resistance. In the following, the current through the CB at terminal 1, which is the closest to the fault, will be analyzed. The converters are modeled as default VSC topology described in Section 4.1 with concentrated DC capacitors of 10 $\mu$F and 10 mH pole reactors $L_p$. For a better comparison of the results, the monopolar configurations are assumed to have the same rating of 900 MW as the bipole.

The AC network impedance is calculated assuming a short-circuit ratio (SCR) of the AC grid of 20.

In all configurations as illustrated in Figures 8.1-8.3, the DC busbars are protected against overvoltages by MOAs. The V-I characteristics of the MOA for DC applications are taken from [ABB09]. The voltage is scaled up and the DC reference voltage of the MOA at 1 mA is set to the nominal DC system voltage of 320 kV. The resulting V-I curve is depicted in Fig. 8.4 with a logarithmic scale for the arrester current and the arrester voltage normalized to the nominal DC system voltage.

The DC busbar earthing (option C in Fig. 8.2) is provided by a 1 M$\Omega$ resistor in order to maintain the DC currents at a reasonable low level during normal operation. For the DC side high-impedance grounding scheme (option B in Figures 8.1-8.3), a 100 mH reactor is used. The AC side earthing (option D in Fig. 8.2) uses a star point reactor with 5000 H, which is grounded through a 5 k$\Omega$ resistor as proposed in [DNSM13].
Terminal 1 is operated in rectifier mode with a secondary winding voltage of the converter transformer of 237 kV and terminals 2 and 3 are operated as inverters with 213 kV at the AC side of the converter.

![Figure 8.4: V-I characteristics of the MOA](image)

**8.4.2 Cable Model**

The default cable model and cable parameters as presented in Section 4.4.1 are applied in this study.

**8.5 Results and Discussion**

In this section, the results of the CB fault current simulations with the different earthing schemes are compared and discussed. The results are presented for the symmetric monopole and the bipole configuration. During pole-to-ground faults without capacitive coupling
of the poles, asymmetric monopoles show the identical behavior as bipole systems and are not presented here.

8.5.1 Symmetric Monopole Configuration

Figure 8.5 illustrates the fault current through the CB in the symmetric monopole system during the first 30 ms after fault occurrence for the different grounding options. The symmetric monopole inhibits the contribution from the AC side through the converter’s freewheeling diodes and has, therefore, zero steady-state fault current. There are, however, the capacitive contributions from the DC capacitors and the adjacent feeder capacitance [BF13b] that lead to a steeply increasing CB current. Even in grounding configurations without DC capacitor midpoint earthing (HRB and HLAC in Fig. 8.5), the capacitors are discharged. If no capacitor midpoint ground is provided, the ground loop is closed through the earthed sheath of the healthy pole cables. The cable capacitances and the DC capacitors form a series circuit and are discharged into the ground fault. As expected, the LRGND scheme leads to the highest CB current and the HRB and HLAC options to the lowest fault current levels. The HRB (cyan curve) and the HLAC (black curve) schemes are identical. Both options have a very high ohmic path for the ground current. For the chosen DC capacitor size of 10 µF, the earthing scheme has only a marginal influence on the CB current peak (blue, green, cyan, and black curve), since the cable discharge contribution from the negative, healthy poles is dominant. Large DC capacitors of 100 µF, however, yield much higher discharge peaks in LRGND configuration (red curve) and the advantage of lower fault currents in the non-solidly earthed HRB scheme (magenta curve) becomes more accentuated. Whether the symmetric monopole network is grounded at all terminals or only at one does not affect the capacitive discharge dominated period due to the delay of the contributions from the remote terminal 3 [BF13b].

A ground fault in a symmetric monopole leads only to moderate overvoltages at the healthy pole for all earthing schemes. The
maximum steady-state overvoltage of about 19% occurs in the HRB earthing scheme.

\[\text{Figure 8.5: CB current in symmetric monopole configuration - LRGND: Low R midpoint grounding, HLGND: High L midpoint grounding, HRB: High R busbar grounding, HLAC: High L AC side grounding}\]

### 8.5.2 Bipole Configuration

During the first 5 ms after fault occurrence, the results of the bipole system depicted in Fig. 8.6 are identical to those in the symmetric monopole as shown in Fig. 8.5. Afterwards, the bipole reveals much higher fault current levels due to the additional infeed from the AC side. The lowest steady-state fault current through the CB is seen in the HRB option (magenta curve), because of the largest impedance in the ground current path compared to the other grounding prac-
tices. The DC capacitor midpoint earthing options LRGND (blue curve) and HLGND (green curve) exhibit an almost equal steady-state fault current, but it increases slower in the HLGND due to the grounding reactor. Slightly lower steady-state CB currents can be observed with metallic return (red and cyan curve) than with earth return (blue and green curve) due to the single grounding point and the additional neutral cable impedance in the ground current path, which reduces the AC side contributions from terminal 3 and decreases the $\frac{di}{dt}$ of the resulting CB current.

**Figure 8.6:** CB current in bipole configuration - LRGND: Low R midpoint grounding, HLGND: High L midpoint grounding, HRB: High R busbar grounding, ER: Earth return, MR: Metallic return

Figure 8.7 shows the voltage at the healthy pole in the bipole configuration for the different earthing schemes. No overvoltages are observed with LRGND at all terminals using the earth return
(blue curve) and the highest permanent overvoltages in HRB configuration (magenta curve) due to the high-ohmic grounding point in the DC grid. The LRGND option (blue and red curve) has better transient performance than the system with HLGND (green and cyan curve) due to the temporary voltage shift of the capacitor midpoints and resulting higher voltages at the healthy pole. Moreover, it suffers higher permanent overvoltages in case of a metallic return with single grounding point at terminal 1 (red and cyan curve) due to the permanent midpoint voltage shift at the non-grounded terminals, which affects also the voltage at the healthy pole of the grounded terminal 1.

![Figure 8.7: Voltage at healthy pole in bipole configuration - LRGND: Low R midpoint grounding, HLGND: High L midpoint grounding, HRB: High R busbar grounding, ER: Earth return, MR: Metallic return](image-url)
8.6 Conclusions

The results have demonstrated the expected effect of high fault currents and low overvoltages in systems with solid earthing on the DC side and the opposite effect in high-impedance grounding schemes. The earth reference option through high resistors at the DC busbars exhibits the lowest fault currents, but the highest overvoltage stresses at the healthy pole. In general, only a marginal influence of the earthing practice can be observed during the first 5 ms, when the capacitive discharge dominates and the DC capacitor size is much more decisive. Bipole and symmetric monopole configurations yield the same results during this period. Afterwards, the CB current increases gradually in a bipole due to the increasing AC infeed and it decreases to zero in the AC infeed blocking symmetric monopole configuration. Moreover, the healthy pole in a symmetric monopole suffers less overvoltages than in a bipole. In terms of overvoltages, the grounding at a single terminal performs worse than grounding at all terminals due to the DC capacitor midpoint shift at non-grounded terminals.
9 Fault Clearing Options

9.1 Introduction

DC CBs are needed to selectively isolate a faulty cable by quickly and reliably breaking DC fault currents. As will be discussed in this chapter, the promising DC CB technologies still have significant drawbacks in terms of on-state losses or speed. The application of the well-known AC fault clearance concept to DC networks, in which CBs are placed at the ends of each line, is questionable. Other concepts to address fault clearance have to be chosen as long as no fully satisfying DC CB concept is developed. Options for fault clearance are the choice of converter technology and filter size, the choice of the grounding scheme, the layout of the network, or the support of the CBs by FCLs.

The goal of this chapter is not to analyze all of these options in detail, but to start the thinking off the beaten track and to contribute to promote the discussion for options other than the classical concept of relying only on CBs.

While submarine cable faults are less frequent than overhead line faults, but typically permanent, it is still a condition that a future DC network needs to be prepared for. The emphasis in this chapter is on pole-to-ground faults, since they are regarded as significantly more frequent compared to pole-to-pole faults [CP11], although the latter fault would lead to more severe conditions [YFO10].
9.2 Short-Circuit Development in Offshore Networks

9.2.1 Test System

Short circuit current developments and fault current reduction options will be discussed using the example of a four-terminal VSC-HVDC grid as illustrated in Fig. 9.1. The system represents a radial connection of an offshore wind farm node to three onshore nodes and is loosely based on a possible connection grid of the Kriegers Flak wind farm in the Baltic Sea [APAK07].

The cable and converter models used in the simulations correspond to the default models as presented in Chapter 4. The cable layer dimensions and parameters are summarized in Table 4.2.

The example DC network is connected to four AC nodes, one offshore wind farm (WF) and three countries connected radially to WF. Node ”N” is located 55 km north, ”W” 75 km west, and ”S” 130 km south of the wind farm. All AC nodes are assumed identical for simplicity and their short circuit behavior is modeled as that of a voltage source behind an inductance. In reality, their behavior might vary considerably. In particular, the representation of the short circuit current contribution of wind farms deserves further and more detailed attention. The connection to the converters is made via transformers with grounded Y-windings on the grid side and Delta-connection on the converter side. The chosen fault resistance of \( R_f = 7 \Omega \) is based on the impulse behavior of concentrated grounds at high currents [WLD05] and corresponds to the resistance at the peak current of a sparking connection in wet loamy sand. The parameters of the test system in its base case configuration are summarized in Table 9.1.

9.2.2 Short Circuit Current Development in Base Case

In this section, the short-circuit current resulting from a pole-to-ground fault on the positive pole on the line connecting WF and
### Table 9.1: System Parameters

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</table>

**Figure 9.1:** Four-terminal VSC-HVDC test system
S is modeled to show the principle behavior of the transient fault current development. In this scenario, the current $i_4$ in the positive pole from WF to S corresponds to the highest fault current that a potential DC circuit breaker would be subjected to. This current is the sum of the fault current contributions from all lines and the converters at WF, N, and W, indicated as $i_1$, $i_2$ and $i_3$, respectively. The fault occurs at $t = 0$ ms. All four currents are shown in Fig. 9.2

The upper part of Fig. 9.2 shows that in the absence of any clearance action, the development of the fault currents can be divided into a transient period (approximately the first 50 ms) and a steady-state period. The transient period is characterized by the discharge of passive circuit elements (primarily filter and cable capacitances), whereas the steady-state currents are directly linked to fault currents fed into the DC system from the AC side. The latter phenomenon is a characteristic of a pole-to-ground fault in a bipolar system, in which the fault creates a ground loop through the neutral of the filter capacitors. As soon as the DC voltage in the positive pole drops below the instantaneous converter AC bus voltage of one of the phases, the converter, in which the IGBTs are assumed to be instantaneously blocked for self-protection, becomes an uncontrolled diode rectifier [FAD09], allows the AC system to feed the DC fault. Even though the distance of the three feeding terminals varies between 0 and 75 km, the mean steady-state values of $i_1$, $i_2$ and $i_3$ deviate approximately 2% from each other, reflecting the low impedance of the DC cables.

The lower part of Fig. 9.2 shows a magnified view of the same quantities for the first 8 ms. The short time delay between the fault occurrence and the time at which the currents start rising corresponds to the travel time of the negative voltage wave from the fault location to WP. In the next 1 ms, $i_4$ is characterized by a series of peaks originating from discharges of the filter capacitances at WP caused by successive arrivals of reflections of the initial voltage wave. The transient contributions from the W and N feeder, $i_1$ and $i_2$, are characterized by a much slower rate of rise, representing a
9.2 Short-Circuit Development in Offshore Networks

Into the DC system from the AC side. The latter phenomenon is a characteristic of a pole-to-ground fault in a bipolar system, in which the fault creates a ground loop through the neutral of the filter capacitors. As soon as the DC voltage in the positive pole drops below the instantaneous converter AC bus voltage of one of the phases, the converter, in which the IGBTs are assumed to be instantaneously blocked for self-protection, becomes an uncontrolled diode rectifier [20], allows the AC system to feed the DC fault. Even though the distance of the three feeding terminals varies between 0 and 75 km, the mean steady-state values of $i_1$, $i_2$ and $i_3$ deviate approximately 2% from each other, reflecting the low impedance of the DC cables.

Figure 9.2: Short-circuit currents during pole-to-ground fault in four-terminal test system using base case parameters

Table III. compares promising technologies with respect to their total interruption time, on state losses, and state of development.

A. Full Solid State CB

Topologies for full solid state breakers are typically based on a certain number of GCTs, GTOs or IGBTs connected in series [21], [22]. The reaction times are extremely fast, which makes them ideal DC circuit breakers. Drawbacks are mainly the substantial on state losses (especially for IGBTs) and the high component costs. This inhibits full solid state breakers to be utilized in large numbers. So far, only applications in MV DC- and AC-networks have been proposed [21], [23]. HVDC multi-terminal network applications, where speed is a crucial factor should be considered instead. Advances in semiconductor device technology such as higher blocking voltages, lower forward losses or even new materials may be a key promoter for the full solid state CBs.

B. Hybrid Solid State CB with Mechanical Disconnector

Hybrid solid state CBs comprise a current interruption and a current conduction path. One proposed solution consists of a fast, but small solid state switch in series with a fast metal contact disconnector in the main path [25]. The actual breaker is located in a parallel path and consists of a number of series connected solid state switches. The small IGBT in the main path needs only to create a sufficiently high voltage for the commutation of the current to the parallel full IGBT breaker. The main path requires, therefore, fewer modules in series and, thus, features a smaller forward voltage and lower on state losses compared to the full IGBT breaker. The disadvantage of this arrangement is the increased interruption time due to the required opening time of the mechanical disconnector. The concept is very attractive, but the costs of the IGBT modules remain the same.

C. Hybrid Mechanical and Solid State CB

Hybrid mechanical solid state breakers combine the low forward losses of a pure (fast) mechanical breaker and the fast performance of a solid state breaker in the parallel path [21]. They are faster than common mechanical breakers, as the arc chamber must only create sufficient voltage for commutation, but no artificial current zero crossing. They are beneficial over hybrid solid state breakers, only if the contact separation speed and, thus, the buildup of arc voltage for...
9 Fault Clearing Options

9.3 Technologies for HVDC Circuit Breakers

The extremely high short-circuit current gradients in the modeled test system clearly identified the time of current interruption (the time until fault current limitation takes effect) as the most relevant parameter for the choice of breaker technology. Fig. 9.3 compares promising technologies with respect to their total interruption time, on state losses, and state of development.

9.3.1 Full Solid State CB

Topologies for full solid state breakers are typically based on a certain number of Gate-Commutated Thyristors (GCTs), Gate Turn-Off Thyristors (GTOs) or IGBTs connected in series [MSD04], [TO02]. The reaction times are extremely fast, which makes them...
ideal DC circuit breakers. Drawbacks are mainly the substantial on state losses (especially for IGBTs) and the high component costs. This inhibits full solid state breakers to be utilized in large numbers. So far, only applications in Medium Voltage (MV) DC- and AC-networks have been proposed [MSD04], [BM07]. HVDC multi-terminal network applications, where speed is a crucial factor should be considered instead. Advances in semiconductor device technology such as higher blocking voltages, lower forward losses or even new materials may be a key promoter for the full solid state CBs.

9.3.2 Hybrid Solid State CB with Mechanical Disconnector

Hybrid solid state CBs comprise a current interruption and a current conduction path. One proposed solution consists of a fast, but small solid state switch in series with a fast metal contact disconnector in the main path [HJ11]. The actual breaker is located in a parallel path and consists of a number of series connected solid state switches. The small IGBT in the main path needs only to create a sufficiently high voltage for the commutation of the current to the parallel full IGBT breaker. The main path requires, therefore, fewer modules in series and, thus, features a smaller forward voltage and lower on state losses compared to the full IGBT breaker. The disadvantage of this arrangement is the increased interruption time due to the required opening time of the mechanical disconnector. The concept is very attractive, but the costs of the IGBT modules remain the same.

9.3.3 Hybrid Mechanical and Solid State CB

Hybrid mechanical solid state breakers combine the low forward losses of a pure (fast) mechanical breaker and the fast performance of a solid state breaker in the parallel path [MSD04]. They are faster than common mechanical breakers, as the arc chamber must only create sufficient voltage for commutation, but no artificial current
zero crossing. They are beneficial over hybrid solid state breakers, only if the contact separation speed and, thus, the buildup of arc voltage for commutation can be significantly increased or if measures in the grid allow interruption times $> 20\, \text{ms}$. So far, ultrafast switches have been designed and tested only for MV levels [SFHK03], [HF02].

### 9.3.4 Mechanical Passive or Active Resonance CB

Mechanical passive or active resonance breakers have been developed for CSC HVDC systems and are based on AC gas circuit breakers. An additional LC-commutation circuit is placed in parallel to the CB. This enables a current oscillation between the two parallel paths and may create an artificial current zero crossing in the main path at which the CB can interrupt [PMR$^+$88], [Fra11]. The oscillation can be achieved by an active current injection from a pre-charged capacitor or excited passively by the arc. Yet, no technical solution has been found to overcome the maximal interruptible current for passive resonance breakers, which is a consequence of the positive UI-arc characteristics at high currents. Active resonance breakers create the current zero with pre-charged capacitors and are, therefore, not bound to this limit. However, considerable capacitor size (especially at high voltage levels) results and no open-close-open switching operations are possible. The low costs and low on state losses of mechanical breakers would allow them to be installed in large numbers. Due to their long interruption times, they are only effective in combination with fault limiting devices or in combination with faster breakers at critical locations. They should certainly be considered as DC load break switches.

### 9.4 Options in HVDC Offshore Networks

The two previous sections demonstrated that high levels and rates of rise of fault currents can occur in DC grids and that they exceed...
the capabilities of the interruption technology that is available today. Ways of easing the requirements of CBs through measures that affect the rate of rise, peak overshoot, or steady state of the fault current should therefore be investigated.

The presented options can be grouped into two general categories: options that do not affect the mean steady state fault current (Options 1 and 2), and those that do (the remaining five options).

**Option 1: Reducing Size of DC Capacitor**

Concentrated DC filter capacitors contribute significantly to the initial transient current peaks. Due to their proximity to potential feeder CBs, they lead to very high rates of rise. DC grid designs that rely on smaller capacitors or employ converter topologies, in which the DC capacitors cannot be discharged into a DC fault, such as in the MMC concept [Mar10], can thus be advantageous. Curve B in Fig. 9.4 shows $i_4$ for a case with filter capacitances of 10 µF compared to 100 µF in the base case (curve A). It can be seen that the magnitude of the initial current peak is reduced. However, during subsequent transients ($5 < t < 20$ ms), there are periods, during which the current is actually higher than in the base case. A faster voltage drop and, thus, an earlier initiation of the AC feeding phase might contribute to these transients.

**Option 2: Adding Pole Reactor**

The initial rate of rise can be significantly lowered through additional inductors. Curve C shows $i_4$ for a scenario, in which a 200 mH inductor is placed at the end of each feeder. While this can ease the $di/dt$ requirements and allow a fast breaker to interrupt at a lower current, the addition of inductors needs to be carefully balanced with the control performance of the system, which relies on current changes for power flow control.
Fault Clearing Options

Converter topologies, in which the DC capacitors cannot be discharged into a DC fault, such as in the Modular Multilevel Converter (MMC) concept [32], can thus be advantageous. Curve B in Figure 3 shows $i_4$ for a case with filter capacitances of 10 µF compared to 100 µF in the base case (curve A). It can be seen that the magnitude of the initial current peak is reduced. However, during subsequent transients ($5 < t < 20$ ms), there are periods, during which the current is actually higher than in the base case. A faster voltage drop and, thus, an earlier initiation of the AC feeding phase might contribute to these transients.

2) Adding Concentrated DC-Feeder Inductors: The initial rate of rise can be significantly lowered through additional inductors. Curve C shows $i_4$ for a scenario, in which a 200 mH inductor is placed at the end of each feeder. The occurrence of the peak current is shifted by around 35 ms.

While this can ease the $\frac{di}{dt}$ requirements and allow a fast breaker to interrupt at a lower current, the addition of inductors needs to be carefully balanced with the control performance of the system, which relies on current changes for power flow control.

3) Reducing Short Circuit Power of AC Nodes: Reducing the short circuit power of the AC nodes reduces the steady state fault currents, but does not influence the initial transients. This is represented by curve D, for which a short circuit power of 2250 MVA (instead of 4500 MVA) was assumed.

The network protection scheme has to take into account the short circuit capability of the individual AC nodes, particularly in schemes, which allow the implementation of slow DC CBs (i.e. with interruption times of > 20 ms) The current that needs to be interrupted in this case would directly depend on the combined strength of the AC nodes that are feeding the fault through that location. Short circuit limiting options include additional AC side reactors, thyristor controlled series inductors, or AC side superconducting fault current limitters (SCFCL) [34].

4) Using DC side SCFCLs: The idea of using resistive DC side SCFCLs for DC grid protection has been proposed by [35]. SCFCLs are characterized by a very rapid transition from zero resistance to their nominal conducting resistance once a critical current density is reached. SCFCLs would most likely be based on High Temperature Superconductors (HTS), which can be cooled with liquid nitrogen.

A very simple FCL model was implemented in series to the circuit breaker under consideration with a critical current of 2.1 kA (1.5 pu) and a nominal conducting resistance of $100 \ \Omega$. Curve E in Figure 3 demonstrates that the SCFCL limits the magnitude of the initial peak to less than half of the peak in the base case and reduces the fault current to below 3 kA within the first few ms and to around 3.8 kA in the steady-state period.

The simplified model of the SCFCL used in the simulation yields only indicative results and a more detailed model is necessary to fully assess the potential of SCFCLs in DC grids. The dissipation of heat is the main limiting factor. In this particular example, the energy converted into heat due to $I^2R$-losses amounts to around 7 MJ in the first 10 ms.

5) Full Bridge Converter Topologies: Full bridge converters [32], [33] inhibit the fault current contribution of the AC side through blocking of the reverse biased IGBTs. The initial fault current in a network employing full bridge converters exhibits a similar development as compared to the base case, whereas the current decreases to zero within approximately 15 ms (not shown in Figure 3) in a full bridge scheme.

Full bridge converters might be able to eliminate the need for separate CBs, if they are combined with fast acting disconnectors to isolate the faulty feeders [4]. The significant drawbacks, however, are the increased steady state losses, which are estimated to be 30 to 50% higher than in half-bridge converter designs [4], and the higher costs due the increased number of IGBTs. In addition, the network would need to be de-energized completely, though only for a short time, to clear a fault [22].

Figure 9.4: Fault current $i_4$ for different current reduction options described in the text.
Option 3: Reducing Short-Circuit Power of AC Nodes

Reducing the short circuit power of the AC nodes reduces the steady state fault currents, but does not influence the initial transients. This is represented by curve D, for which a short circuit power of 2250 MVA (instead of 4500 MVA) was assumed. The network protection scheme has to take into account the short circuit capability of the individual AC nodes, particularly in schemes, which allow the implementation of slow DC CBs (i.e. with interruption times of $> 20$ ms) The current that needs to be interrupted in this case would directly depend on the combined strength of the AC nodes that are feeding the fault through that location. Short circuit limiting options include additional AC side reactors, thyristor controlled series inductors, or AC side Superconducting Fault Current Limiters (SCFCL) [GAH09].

Option 4: Using DC Side SCFCLs

The idea of using resistive DC side SCFCLs for DC grid protection has been proposed by [MA12]. SCFCLs are characterized by a very rapid transition from zero resistance to their nominal conducting resistance once a critical current density is reached. SCFCLs would most likely be based on High Temperature Superconductors (HTS), which can be cooled with liquid nitrogen. A very simple FCL model with a threshold triggered switch and a parallel resistor was implemented in series to the circuit breaker under consideration. A threshold current of 2.1 kA (1.5 pu) and a resistor of $100 \Omega$ was chosen. Curve E in Fig. 9.4 demonstrates that the SCFCL limits the magnitude of the initial peak to around 8 kA and reduces the steady state fault current to below 3 kA.

The simplified model of the SCFCL used in the simulation yields only indicative results and a more detailed model is necessary to fully assess the potential of SCFCLs in DC grids. The dissipation of heat is the main limiting factor. In this particular example, the energy converted into heat due to $I^2R$-losses amounts to around
7 MJ in the first 10 ms.

**Option 5: Full Bridge Converter Topologies**

Full bridge converters [Mar10], [MBT11] inhibit the fault current contribution of the AC side through blocking of the reverse biased IGBTs. The initial fault current in a network employing full bridge converters exhibits a similar development as compared to the base case, whereas the current decreases to zero within approximately 15 ms (not shown in Fig. 9.4) in a full bridge scheme. Full bridge converters might be able to eliminate the need for separate CBs, if they are combined with fast acting disconnectors to isolate the faulty feeders [Fri12]. The significant drawbacks, however, are the increased steady state losses, which are estimated to be 30 to 50% higher than in half-bridge converter designs [Fri12], and the higher costs due the increased number of IGBTs. In addition, the network would need to be de-energized completely, though only for a short time, to clear a fault [TO02].

**Option 6: Isolated DC Circuits**

A symmetrical monopolar VSC HVDC configuration isolates the DC side from the AC side in case of a pole-to-ground fault. The resulting short circuit current behavior is similar to that described in 9.4, where only passive elements contribute to the fault current (this option is also not shown in Fig. 9.4). Drawbacks of the symmetrical monopolar scheme are the overvoltages on the healthy pole due to the charging of the corresponding filter capacitor and the reduced redundancy compared to bipolar systems. In order to achieve redundancy, two parallel symmetrical monopolar systems are required (with a total of 4 (high voltage) cables).
Figure 9.5: Modified network layout for investigation of selective placing of CBs
6) Isolated DC Circuits [4]: A symmetrical monopolar VSC HVDC configuration isolates the DC side from the AC side in case of a pole-to-ground fault. The resulting short circuit current behavior is similar to that described in 5), where only passive elements contribute to the fault current (this option is also not shown in Figure 3).

Drawbacks of the symmetrical monopolar scheme are the overvoltages on the healthy pole due to the charging of the corresponding filter capacitor and the reduced redundancy compared to bipolar systems. In order to achieve redundancy, two parallel symmetrical monopolar systems are required (with a total of 4 (high voltage) cables).

7) Selective Placing of High Performance CBs at Strategic Grid Locations:
The last fault current reduction option that is presented in this paper refers to the possibility of employing fast-acting CBs or FCLs (or a combination of the two) on grid connections that have a large impact on potential fault currents in other parts of the network. The system that was considered so far (Figure 1) is not suitable for investigations of this type, since all three cable connections can be considered to be of equal importance in terms of their fault current contribution. Therefore, a modified system was created, in which the original system was copied and mirrored (Figure 4). Both individual networks are connected with an additional 400 km submarine cable link between the original WF node and the mirrored WF node (denoted as WF').

Figure 5. Fault current contribution from mirrored subsystem, $i_{\text{link}}$, to the fault current $i_4$ with and without a fast CB at location of $i_{\text{link}}$. The fault type and location is identical to the previous investigations. The current $i_4$ through the breaker on the faulted line is now the algebraic sum of $i_1$, $i_2$, $i_3$ and $i_{\text{link}}$.

Figure 5 illustrates that in absence of a breaking device in the interlink, the fault current contribution from the mirrored system is significant. While the rise $i_{\text{link}}$ is relatively gradual, its contribution to current $i_4$ after 25 ms is nearly 50%.

In order to demonstrate the principle of this approach, a hypothetical fast CB is placed at the location of $i_{\text{link}}$. It is capable of interrupting the fault current as soon as it reaches 2.1 kA (1.5 p.u.) (cf. Figure 5). The effect of such a hypothetical device in the interlink is twofold: on the one hand, the subsystem without fault can continue to operate, though with a distorted power flow by the amount that was previously flowing through the interconnecting line. On the other hand, the stationary short-circuit current $i_4$ (after ~25 ms) through the breaker of line WF-S is almost halved (12 kA instead of 25 kA) and a breaker of lower rating may be chosen.

The emphasis in this very simple example is not on the numeric values of these currents, but rather on the qualitative observation that results from network splitting.
Option 7: Selective Placing of High Performance CBs

The last fault current reduction option that is presented in this study refers to the possibility of employing fast acting CBs or FCLs (or a combination of the two) on grid connections that have a large impact on potential fault currents in other parts of the network. The system that was considered so far (Fig. 9.1) is not suitable for investigations of this type, since all three cable connections can be considered to be of equal importance in terms of their fault current contribution. Therefore, a modified system was created, in which the original system was copied and mirrored (Fig. 9.5). Both individual networks are connected with an additional 400 km submarine cable link between the original WF node and the mirrored WF node (denoted as WF').

The fault type and location is identical to the previous investigations. The current \( i_4 \) through the breaker on the faulted line is now the algebraic sum of \( i_1, i_2, i_3 \) and \( i_{\text{link}} \). Figure 9.6 illustrates that in absence of a breaking device in the interlink, the fault current contribution from the mirrored system is significant. While the rise \( i_{\text{link}} \) is relatively gradual, its contribution to current \( i_4 \) after 25 ms is nearly 50%. In order to demonstrate the principle of this approach, a hypothetical fast CB is placed at the location of \( i_{\text{link}} \). It is capable of interrupting the fault current as soon as it reaches 2.1 kA (1.5 p.u.) (cf. Fig. 9.6). The effect of such a hypothetical device in the interlink is twofold: on the one hand, the subsystem without fault can continue to operate, though with a distorted power flow by the amount that was previously flowing through the interconnecting line. On the other hand, the stationary short-circuit current \( i_4 \) (after 50 ms) through the breaker of line WF-S is reduced by nearly one third (13 kA instead of 19 kA) and a breaker of lower rating may be chosen.

The emphasis in this very simple example is not on the numeric values of these currents, but rather on the qualitative observation that results from network splitting into sub-networks. By selecting a network topology that is only weakly meshed at some locations
and contains sub-networks, fast interruption or limiting devices at connecting locations can prevent that short circuit contributions from one subsystem feed into another. This may significantly reduce the requirements of other protection devices. Whether slower devices with an interruption time of only 25 ms (to interrupt the stationary currents) are acceptable in the first place remains a crucial point. Maybe the fault can now be cleared by de-energizing the sub-network completely [TO02], either by control of the converter terminals or in support with AC side CBs. A discussion of this issue is beyond the scope of this work.

9.5 Discussion and Conclusions

It is evident that the rate of rise and the amplitude of the transient and stationary part of the fault current through a breaker are extremely demanding due to the low resistance of the network. None of the existing breaker technologies is optimum with respect to fault clearing time, maximum interruption capability, losses during normal operation, and costs. Also the concept that is used today in point-to-point connections, opening the AC side breakers to de-energize the system, is not foreseeable for larger DC networks. We have thus reported on some other options that have an influence on the amplitude or the rate of rise of the short-circuit current to reduce the requirements on DC-CBs. Some of them address the problem inherently, others by adding components.

A reduction of the DC side filter capacitors would result in an inherent reduction of the amplitude of the first peak of the transient short-circuit current. However, accepting a larger ripple on the DC network or choosing another converter technology cannot be based on fault clearance considerations alone. Similarly for the grounding scheme of the network: besides the influence on mainly the stationary fault current, arguments with respect to converter terminal operation and insulation coordination have to be considered. As was explained in Section 9.3, the choice of CB technology is today
mainly a trade-off between speed and on-state losses. No single one solution is optimum for the entire network, but from knowing the possible prospective short-circuit currents, it may be possible to select a different technology at different locations in the network. One might accept the high losses at certain strategic locations where fast breaker action is inevitable.

As was mentioned before, de-energizing the complete network in the case of a fault will not be acceptable. However, one may be forced to accept a partial network outage as long as no suitable CBs are available. One may choose the network topology in a way that it can be split into sub-networks. Such a network is not as densely meshed as desired, but the losses from a few fast CBs at the connecting links may be accepted and the faulty sub-network can then be shut down to clear the fault.

In summary, the discussion on choosing an acceptable fault clearing option is not only driven by the CB technology, but may even involve the selection of converter terminal technology or the network topology.

The simulations in the present contribution concentrated only on the fault current through the breaker, but of course also the current through the freewheeling diodes and other sensitive components should be looked at in future studies. Moreover, in this study we modeled all nodes identically; even the offshore connection. The studies should be repeated with more detailed converter models as soon as a concrete location for the first network is known.
10 HVDC Circuit Breakers

10.1 Introduction

The availability of HVDC CBs will be critical for the reliability of MTDC networks. Point-to-point HVDC connections can be adequately protected by conventional CBs on the AC side of the converter, even if this results in the de-energization of the entire DC system \cite{TO07, LRM+85}. A real MTDC grid, however, requires DC CBs at each end of a line section to selectively isolate a fault by quickly and reliably breaking the fault current.

The interruption of an HVDC circuit requires generally the following \cite{Puc68}: a current zero has to be produced, the magnetic energy that is stored in the inductance has to be dissipated, and sufficient dielectric strength has to be established to withstand the transient recovery voltage (TRV). The first and second requirement are fulfilled rather easily in AC systems given the natural current zero crossing. In DC systems, however, the CB has to produce the current zero itself. This can be done either by insertion of a counteracting voltage or by injection of a current with opposite polarity. For practical purposes, the interruption process has to be completed within a certain time and the resulting switching surge has to be within the insulation’s withstand capability.

An HVDC CB has to be able to create a current zero, to dissipate the energy stored in the circuit, and to establish the dielectric strength. While DC CBs are widely available for low and medium voltage applications, only transfer and load current switches are in use in HVDC systems \cite{Fra11}. Numerous concepts for such an HVDC CB have been presented up to now in patents and articles,
which all show a similar arrangement with a switching element in the nominal path to build the dielectric strength, a commutation path to create the current zero, and an absorber path to dissipate the stored energy. The main switching element can either be an arc between the contacts of a mechanical CB, a solid-state based semiconducting device or the combination of both. Each of the proposed CB concept has advantages and drawbacks either in on-state losses or speed as described in Chapter 9.

The design of the HVDC CB has to be chosen according to the expected maximum fault current in a MTDC network, which depends on various factors. These prospective fault current influencing factors include among others: the DC capacitor size and fault resistance (Section 5.1), the transmission line technology (Section 5.2), the grounding scheme (Chapter 8), and the layout of the MTDC network (Chapter 7).

It has been shown that the expected fault current exceeds the breaking capability of most of the available HVDC CB concepts or their construction costs are too high. Therefore, the MTDC network design has to be adapted to the CBs capability and additional fault clearing support options have to be chosen as addressed in Chapter 9.

This chapter continues the discussion about the trade-off between CB and network design and analyzes their interaction into detail based on simulations in EMTDC-PSCAD. The modeling of five different HVDC CB concepts in PSCAD are presented and their performance is studied in a meshed four-terminal MTDC cable network during the current interruption process of a pole-to-ground fault. The influence of the CB itself, the network components, and the protection system properties on the maximum fault currents, as well as maximum and minimum voltages in the system are shown.

The considered CB concepts include the passive and active resonance CB, two solid-state based CB concepts, as well as a hybrid CB concept. Results are presented for pole-to-ground faults in cable systems.
10.2 Modeling of MTDC

The performance of the different HVDC CBs is tested in a meshed four-terminal MTDC network as shown in Fig. 10.1 using PSCAD simulations. The pole-to-ground fault occurs at a distance of 50 km to terminal 1 and 150 km to terminal 2. CBs are installed at all cable ends, but only CB1 and CB2 are tripped assuming differential relaying [Twe12]. The chosen network layout and cable lengths result in higher fault currents in CB1 than in CB2 in order to demonstrate their different behavior.

**Figure 10.1:** MTDC network layout (CBs and inductors only shown for line 12)

10.2.1 Cable Model

The default cable model as described in Section 4.4.1 is applied.
10.2.2 Converter Model

Each VSC-HVDC converter station in the DC grid is assumed to be a bipolar half-bridge based converter with a nominal rating of 900 MW as described in Section 4.1. Concentrated midpoint-grounded DC capacitors $C_{\text{cap}}$ at each terminal and line reactors $L_{\text{line}}$ at each cable end in series to the CBs are installed as illustrated in Fig. 10.2. In this chapter, these reactors are named ”line reactor” rather than ”pole reactor”, because each feeder at the busbar comprises a reactor and not only the poles of the converter. During the initialization period of each simulation run, DC voltage sources are connected to the terminals to establish the power flow during normal operation. During this period, ”S1” is open and ”S2” closed. The DC source values are chose as indicated in Fig. 10.1. The converter’s local overcurrent protection blocks the IGBT modules above a threshold value of about twice the nominal current [BM07] to protect them from overcurrents making the half-bridge based VSC an uncontrolled rectifier [YFO10]. Therefore, the converter model to be implemented for the transient period can be simplified to the diode rectifier shown in Fig. 10.2 by opening ”S2” and closing ”S1”. No post-fault control strategy for the converters is implemented in the model and the tripped converters remain blocked throughout the simulation time. In a modular multilevel converter (MMC), the phase reactor $L_s$ represents the arm reactors.

The AC network is modeled according to Section 4.2.

10.3 HVDC CB Concepts and Modeling

Five different HVDC CB concepts and their modeling in PSCAD will be presented in the following: the passive (P-RCB) and active resonance CB (A-RCB), the hybrid CB (HCB), and two full solid-state CB concepts (SCB1 and SCB2). Even if the concepts differ substantially in their construction, three different paths for the current as illustrated in Fig. 10.3 can be found in all con-
cepts [BMR+85]. A nominal path with the main switching element, either a classical mechanical CB, a semiconductor device or the combination of both, which carries the nominal current during normal operation and provides the required dielectric insulation in open position. After detection of the fault and tripping of the CB, the main switching element opens and the current commutates into the commutation path, which consists of the passive (P-RCB) or active (A-RCB) resonance circuit for current injection, the main breaker (HCB) or the snubber circuit (SCB). Meanwhile, the main switching element in the nominal path establishes the required dielectric strength/galvanic separation. The voltage across the CB increases and the current commutates into the absorber path, where the energy stored in the system inductance is dissipated in a MOA with non-linear VI-characteristics. The MOA dissipates the stored energy and limits the TRV across the CB.

A simple fault detection mechanism is implemented at CB1 and CB2 (cf. Fig. 10.1) with a level comparator to simulate differential
protection [Twe12] and selective opening of the CBs at the faulted line ends. All other CBs remain closed. A very optimistic detection delay $\Delta T_{\text{detect}}$ of 1 ms [Twe12] is chosen for all CB concepts. The detection delay is defined as the time from occurrence of the fault to sending the trip signal to the CB and accounts for all signal processing and communication delays due to the sending and receiving of values from the opposite line end as required in differential protection schemes [Twe12]. The decisive contribution to the detection delay is from the communication delay. Even with ultra fast signal processing, the communication delay cannot be reduced further. It depends on the size of the network and the inherent signal propagation speed of about 200 km/ms. For larger networks, the total detection delay becomes substantially larger than 1 ms.

**Figure 10.3:** General model for HVDC CB

### 10.3.1 P-RCB and A-RCB

The passive and active resonance CB as illustrated in Fig. 10.4 have a mechanical breaker in the nominal path, which is usually an AC air-blast CB [BMR+85] or an SF6 puffer CB [NNH+01] for the P-RCB and a vacuum CB [TKT+14] for the A-RCB. In the passive scheme, the components in the red boxes in Fig. 10.4 do not exist, whereas in the A-RCB, the capacitor $C_{\text{res}}$ is pre-charged by closing ”$S_b$” and the active current injection is initiated through closing of
The temporal development of the current and voltage during the interruption process in the P-RCB [BKM+70, BMR+85, NNH+01] is illustrated in Fig. 10.5 with example curves for the current in the nominal path (red), in the commutation path (green), in the absorber path (cyan), the sum of all currents (blue), and the CB voltage (magenta). Note that the CB parameters in Fig. 10.5 are different from the ones presented in Section 10.4.2 to improve the visibility.

After the current has exceeded the CB threshold at 0.6 ms and the differential protection system has given the trip signal selectively to the CB at 1.6 ms, the CB is tripped and the drive starts to move the contacts. An optimistic estimate of $\Delta T_{\text{opening}} = 4$ ms is assumed for the delay between the trip signal and contact separation. An arc is established between the contacts and the arc voltage forces the current to commutate into the commutation path, which consists of a resonance circuit with an inductance $L_{\text{res}}$, a capacitor $C_{\text{res}}$, and a parasitic resistance $R_{\text{res}}$ as indicated in Fig. 10.4. After another $\Delta T_{\text{nozzle}} = 5$ ms, the moving contact cleared the nozzle and the CB is able to clear the arc. Also the chosen nozzle clearing time is a an optimistic lower estimate for fast gas CBs. Once the nozzle is cleared, the arc has a negative V-I characteristic and together with
a sufficiently small parasitic resistance, the oscillations of the current in the commutation path start to grow at 10.6 ms (green curve in Fig. 10.5). This oscillating current is superimposed on the current through the nominal path (red), which results in a current zero crossing at around 29 ms and extinction of the arc. The current in the nominal path (red) is then zero, but the total current (blue) is still high due to the stored energy in the system inductance and resonance inductor. After the arc extinction, the capacitor $C_{\text{res}}$ is charged by the commutated current, until the threshold voltage of the MOA is exceeded. Then, the current commutates into the absorber path (cyan) and the voltage across the CB (magenta curve) rises rapidly. The fault current (blue) starts to decrease when the voltage across the CB is larger than the system voltage after about 30 ms. The stored energy is dissipated in the MOA resulting in a peak in the absorber current (cyan), which decays and brings the total current (blue) to zero at around 43 ms. At this point in time, the actual fault current interruption is completed and the residual current disconnector ”RD” as shown in Fig. 10.4 is opened to interrupt the residual current in the MOA and to provide additional galvanic separation of the circuit.

The current interruption process in the active scheme (A-RCB) [TKT+14], [EBH14] is shown in Fig. 10.6. A CB opening delay of 4 ms is again assumed, but can possibly be reduced, if a vacuum CB with special electromagnetic drive was used [HSKY06]. The resonance capacitor $C_{\text{res}}$ in Fig. 10.4 is pre-charged and through closing of ”$S_a$” after contact separation, a negative current (green curve in Fig. 10.6) is injected into the nominal path (red), which forces the arc current to zero and considerably reduces the time to the first current zero crossing as compared to the passive scheme. It requires, however, an additional charging unit with a DC source. It is assumed that the CB’s required voltage withstand capability is reached within the rise time of the resonance capacitor voltage of 2 ms.
The crucial part of the P-RCB modeling with mechanical switch is the arc model. In contrast to the A-RCB with active current injection, the passive concept requires a negative V-I characteristic of the arc conductance to achieve an unstable, growing oscillation in the resonance circuit. Therefore, an accurate modeling of the arc burning and extinction process is needed.

Black-box arc models are widely used to simulate the dynamic arc behavior due to their computational efficiency. Their accuracy, however, depends on the exact description of the arc parameter functions. The determination of these functions is difficult and they are usually only valid under specific conditions [Wal13]. Nevertheless, the dynamic arc behavior in P-RCB can successfully be predicted as presented in [NNH+01, Wal13].

The entire process of arc elongation during contact opening, dy-
namic behavior during cooling, and arc behavior near current zero is very complex and cannot be described by a single black-box arc model. Therefore, an approximation of two submodels is chosen for the study at hand. One model for the arc elongation until nozzle opening assuming clogged gas flow and one model for the dynamic behavior under forced cooling in the high-current and low-current range near current zero.

**Arc elongation:** It is assumed that the gas flow is low during contact opening until the nozzle is fully open. During this arc elongation period, the arc resistance $r_{\text{arc}}$ exhibits a positive V-I characteristic:

$$r_{\text{arc}}(t) = \frac{E_{\text{arc}} \cdot l_{\text{arc}}}{\Delta T_{\text{nozzle}}} \cdot \frac{l_{\text{arc}}}{t_{\text{arc}}} \cdot t,$$

(10.1)
where \( l_{arc} \) is the arc length at nozzle opening, \( E_{arc} \) the arc voltage gradient, \( i_{arc} \) the instantaneous arc current, and \( \Delta T_{nozzle} \) the required time for nozzle opening. The PSCAD implementation is illustrated in Fig. 10.7 with \( r_0 \) as arc resistance \( r_{arc} \) during the elongation process.

**Figure 10.7: PSCAD implementation of arc elongation**

**Arc dynamics:** After opening of the nozzle, the gas flow increases and the arc characteristic is dominated by the heating and cooling dynamics modeled as black-box model.

The majority of the available black-box models are modifications of Mayr’s [May43] and Cassie’s equation [Cas39] that are based on the energy balance equation:

\[
\frac{dQ}{dt} = P_{heat} - P_{cool},
\]  

(10.2)

which describes the change in the arc column’s energy content \( Q \) resulting from the imbalance between ohmic heating \( P_{heat} \) and cooling \( P_{cool} \).

Mayr’s equation originally assumed constant arc cooling power \( P \) and arc time constant \( \tau_{arc} \). A modification of it can be found
in [Sch72]:

\[ \dot{g} = \frac{g}{\tau_{arc}(g)} \left( \frac{u \cdot i}{P(g)} - 1 \right) \]  

(10.3)

with the arc parameters \( P(g) \) and \( \tau_{arc}(g) \) depending on the arc conductance \( g \). These two arc parameters are described by power functions

\[ P(g) = P_0 \cdot g^a \]  

(10.4)

\[ \tau_{arc}(g) = \tau_0 \cdot g^b \]  

(10.5)

The constant cooling power factor \( P_0 \) depends linearly on the blow pressure \( p \) resulting in \( P(g) = p \cdot P_0 \cdot g^a \) [BKM+70, Wal13].

To implement the dynamic arc model into PSCAD, equation (10.3) has to be transformed into

\[ g = \int_0^t \frac{1}{\tau_{arc}(g)} \left( \frac{i^2}{P(g)} - g \right) dt' \]  

(10.6)

The PSCAD implementation is realized as illustrated in Fig. 10.8. Time delay blocks are used to save the present values of current, voltage, and arc conductance for the next time step.

### 10.3.2 HCB

There are numerous different hybrid HVDC CB arrangements [AS98], [MKD05]. The description and modeling of all of them is beyond the scope of this study and one representative concept similar to [HJ11] as illustrated in Fig. 10.9 is chosen.

The nominal path consists of a few IGBTs and a fast mechanical disconnector in series. Series connected IGBTs with full voltage withstand capability are installed in the commutation path and a
10.3 HVDC CB Concepts and Modeling

MOA in the absorber path. For zero voltage switching and loss reduction, all IGBTs are protected by RCD snubber circuits consisting of a snubber capacitor $C_s$, a resistor $R_s$, and a diode. Note that Fig. 10.9 shows only the IGBTs for the positive current direction. For reverse blocking ability of the HCB, the same number of IGBTs with opposite polarity has to be installed in series.

To reduce the losses during normal operation, only one IGBT for each current direction is installed in the nominal path. This IGBT is able to commutate the fault current into the commutation path, but has not full TRV withstand capability. After tripping of the CB and blocking of the IGBT in the nominal path, the disconnector ”D” is opened. The current commutates into the snubber circuit and into the commutation path (green curve) about 10 $\mu$s after receiving the trip signal from the protection at around 1.6 ms as illustrated in Fig. 10.10. The current in the nominal path (red curve) is reduced to zero immediately. After full opening of the mechanical disconnector, the IGBTs in the commutation path are blocked at around 4.6 ms and the current commutates in their snubber circuits. In contrast to the SCB, the HCB cannot interrupt the current immediately after commutation, but has to wait until the disconnector has fully

**Figure 10.8:** PSCAD implementation of dynamic arc model
established its dielectric strength to be able to withstand the TRV. This delay is named commutation delay and is assumed to be 3 ms. Afterwards, the TRV rises rapidly and the current commutates into the absorber path (cyan curve), where the remaining energy is dissipated. Again, the fault current starts to decrease as soon as the voltage across the CB (magenta curve) exceeds the system voltage (yellow curve). The residual current disconnector "RD" is opened at the end to interrupt the MOA’s residual current.

### 10.3.3 SCB

Two different SCB concepts are considered in this study: one with the energy absorber path parallel to the nominal path (SCB1) [MKD05] as illustrated in Fig. 10.11 and one with the energy dissipation in a freewheeling path (SCB2) [ST12] as depicted in Fig. 10.12. The latter has the advantage of a reduced TRV across the CB [ST12],
**Figure 10.10:** Fault Current Interruption in HCB

[WM13].

SCB1 has RCD snubber circuits parallel to each IGBT as explained in Section 10.3.2 and the MOA parallel to the nominal path.
The second concept SCB2 contains only snubber capacitors $C_s$ and large resistors $R_d$ parallel to the IGBTs and freewheeling diodes to maintain the voltage balance of the series connected devices [ST12]. Both concepts exhibit a similar current interruption process as illustrated in Fig. 10.13. At around 1.5 ms, the IGBTs are blocked and the current commutates into the snubber circuits (green curve). Meanwhile, the voltage across the CB (magenta dashed curve) rises and the current commutates finally into the absorber path (cyan curve) at around 2.5 ms.

### 10.3.4 MOA Model

The PSCAD built-in MOA is used for the energy dissipation in the absorber path. The non-linear V-I characteristic curve for DC applications as depicted in Fig. 10.14 is taken from [ABB09]. The
reference voltage is chosen in order to have a leakage current of 1 mA under continuous operation voltage. The MOA characteristic curve in the non-linear and high-current area is equal under AC and DC voltage, but the low-current or continuous operating voltage area is distinct under DC voltage due to the missing capacitive leakage current that is present in AC applications.

10.4 Parameters

10.4.1 Base Case System Parameters

The default system parameters for the interaction study are summarized in Table 10.1. In the base case, a line reactor of 100 mH is installed between cable end and CB (cf. Fig. 10.2) to limit the $\frac{di}{dt}$ of the fault current [CBHJ12]. Moreover, a 50 $\mu$F DC capacitor is
assumed in the base case. Advanced converter topologies, such as the MMC, would not need any DC capacitors. This study considers, however, the general case with DC capacitors present.

### 10.4.2 Base Case CB Parameters

The parameters for all CB types are given in Table 10.2. The CB opening delay $\Delta T_{\text{opening}}$ is the delay from the trip signal to the contact separation in mechanical CBs. In case of the A-RCB, the counter-current is injected right after contact separation assuming that the TRV peak is reached only after full recovery of the CBs dielectric strength, i.e., after the CB has completely opened.

The P-RCB features an additional nozzle opening time $\Delta T_{\text{nozzle}}$, during which the arc exhibits a positive V-I characteristic as explained in Section 10.3.1.

A snubber capacitor of $85 \, \mu\text{F}$ per IGBT is chosen to limit the rate of rise of the voltage to $300 \, \text{V} / \mu\text{s}$ [CBHJ12].
Table 10.1: Base Case System Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Converter Power (per pole)</td>
<td>450 MW</td>
</tr>
<tr>
<td>DC Voltage</td>
<td>±320 kV</td>
</tr>
<tr>
<td>AC Voltage (L-L, RMS)</td>
<td>400 kV</td>
</tr>
<tr>
<td>AC Frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>SCR of AC Network</td>
<td>20</td>
</tr>
<tr>
<td>X/R of AC Network</td>
<td>10</td>
</tr>
<tr>
<td>Transformer Leakage Reactance</td>
<td>0.1 p.u.</td>
</tr>
<tr>
<td>Transformer Turns Ratio</td>
<td>216/400</td>
</tr>
<tr>
<td>Converter Phase Reactor</td>
<td>0.05 p.u.</td>
</tr>
<tr>
<td>DC Capacitor</td>
<td>50 μF</td>
</tr>
<tr>
<td>Line Reactor</td>
<td>100 mH</td>
</tr>
<tr>
<td>Fault Resistance</td>
<td>2 Ω</td>
</tr>
<tr>
<td>Converter Overcurrent Threshold</td>
<td>2.8 kA</td>
</tr>
<tr>
<td>CB Trip Threshold</td>
<td>2 kA</td>
</tr>
<tr>
<td>$\Delta T_{\text{detect}}$</td>
<td>1 ms</td>
</tr>
</tbody>
</table>
### Table 10.2: CB Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A/P-RCB:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Main CB:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta T_{\text{opening}}$</td>
<td>4 ms</td>
<td>[Kap11]</td>
</tr>
<tr>
<td>$\Delta T_{\text{nozzle (P-RCB)}}$</td>
<td>5 ms</td>
<td>[Kap11]</td>
</tr>
<tr>
<td>Arc Model (P-RCB):</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Arc Voltage Gradient, $E_{\text{arc}}$</td>
<td>1.4 kV/m</td>
<td>[TK01]</td>
</tr>
<tr>
<td>Arc Length, $l_{\text{arc}}$</td>
<td>5 cm</td>
<td></td>
</tr>
<tr>
<td>$P_0$</td>
<td>393 kW</td>
<td>[Wal13]</td>
</tr>
<tr>
<td>$a$</td>
<td>0.25</td>
<td>[Wal13]</td>
</tr>
<tr>
<td>$\tau_0$</td>
<td>15 $\mu$s</td>
<td>[Wal13]</td>
</tr>
<tr>
<td>$b$</td>
<td>0.5</td>
<td>[Wal13]</td>
</tr>
<tr>
<td>Blow Pressure</td>
<td>70 bar</td>
<td></td>
</tr>
<tr>
<td>Commutation Path:</td>
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<td></td>
</tr>
<tr>
<td>$C_{\text{res}}$</td>
<td>50 $\mu$F</td>
<td></td>
</tr>
<tr>
<td>$L_{\text{res}}$</td>
<td>500 $\mu$H</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{res}}$</td>
<td>0 $\Omega$</td>
<td></td>
</tr>
<tr>
<td>Pre-charge voltage (A-RCB)</td>
<td>40 kV</td>
<td></td>
</tr>
<tr>
<td><strong>HCB:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Commutation Delay</td>
<td>3 ms</td>
<td>[HJ11]</td>
</tr>
<tr>
<td>IGBT On-State Resistance</td>
<td>1.5 m$\Omega$</td>
<td>[ABB13]</td>
</tr>
<tr>
<td># of IGBTs in Commutation Path</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td>$R_s$</td>
<td>70 $\Omega$</td>
<td></td>
</tr>
<tr>
<td>$C_s$</td>
<td>85 $\mu$F</td>
<td>[CBHJ12]</td>
</tr>
<tr>
<td><strong>SCB:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IGBT On-State Resistance</td>
<td>1.5 m$\Omega$</td>
<td>[ABB13]</td>
</tr>
<tr>
<td># of IGBTs in Nominal Path</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td>$R_s$</td>
<td>70 $\Omega$</td>
<td></td>
</tr>
<tr>
<td>$C_s$</td>
<td>85 $\mu$F</td>
<td>[CBHJ12]</td>
</tr>
</tbody>
</table>
10.5 Results and Discussion

The simulations are performed in PSCAD using a time step of 1 µs. Results for the CB concept comparison in the base case and parameter variations are presented and discussed in the following paragraphs.

10.5.1 Comparison of CB Concepts in Base Case

The different HVDC CB concepts presented in Section 10.3 are compared in terms of interruption time, maximum CB fault current, and maximum and minimum voltages at the terminals during the fault current interruption process.

The interruption time is defined as the time from fault detection at the CB to current zero (CZ) in the faulted line, i.e., when the CB’s total current $i_{\text{total}}$ as indicated in Fig. 10.3 becomes zero. In contrast to the breaking time that considers only the time until current zero in the nominal path, the interruption time takes also the energy dissipation process into account. Another performance indicator is the time, when the $\frac{di}{dt}$ of the total current becomes negative for the first time. Table 10.3 presents the comparison of the different CB concepts in terms of time to CZ and time to negative $\frac{di}{dt}$ in the base case. Figure 10.15 shows the corresponding maximum fault currents through CB1 and CB2 at the ends of the faulted cable for the different CB concepts. As expected, the SCB has the lowest interruption time below 5 ms and, therefore, also the lowest maximum CB current of about 5 kA, whereas the P-RCB concept reveals the highest interruption time of up to 94 ms and 27 kA maximum current in CB1. The P-RCB concept exhibits also the highest difference in interruption time and maximum fault current between CB1 and CB2. It takes more than three times longer to interrupt the current in CB1 than in CB2. Fast CBs with interruption times below 10 ms act within the capacitor dominated period of the transient fault current [BF13b] and the loading of the CBs is almost equal given the same DC capacitor size at both terminals. Slow
Table 10.3: Interruption Time for Base Case in Milliseconds

<table>
<thead>
<tr>
<th>CB Type</th>
<th>Time to CZ</th>
<th>Time to di/dt &lt; 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CB1</td>
<td>CB2</td>
</tr>
<tr>
<td>SCB</td>
<td>3.3</td>
<td>4.0</td>
</tr>
<tr>
<td>HCB</td>
<td>9.2</td>
<td>9.0</td>
</tr>
<tr>
<td>A-RCB</td>
<td>12.2</td>
<td>13.6</td>
</tr>
<tr>
<td>P-RCB</td>
<td>94.2</td>
<td>27.9</td>
</tr>
</tbody>
</table>

acting-CBs, such as the P-RCB, however, interrupt the current in the later AC infeed dominated period, during which the fault location is decisive. CB1 is located closer to the fault as compared to CB2 and has more feeders at the adjacent busbar, through which the terminals 3 and 4 feed the ground fault (cf. Fig. 10.1).

Figure 10.15: Maximum CB Current for the Base Case
The fact that CB2 opens earlier than CB1 even worsens CB1’s situation due to re-routing of the fault currents in the network as depicted in Fig. 10.16 for a system with P-RCBs. After CB2 has interrupted the fault current at around 28 ms (green curve), line currents $i_{32}$ (cyan curve) and $i_{43}$ (yellow curve) change their direction and all four terminals feed the fault current in CB1. This results in a higher current load in CB1 (blue solid curve) as compared to the case if CB2 would not open at all (blue dashed curve) and the interruption time increased by about 142%.

![Figure 10.16: Line currents in MTDC network with slow P-RCB](image)

The corresponding terminal voltages of all four terminals are illustrated in Fig. 10.17 for the P-RCB and in Fig. 10.18 for the SCB. After fault inception at 0 ms, the voltages at all four terminals drop to about 0.4 p.u. within 10 ms in the network with P-RCBs as shown in Fig. 10.17. In contrast, the terminal voltages decrease only to
about 0.7 p.u. using SCBs as depicted in Fig. 10.18. The voltage at terminal 4 (cyan curve) remains unaffected, since the converter protection has not detected any overcurrent given the fast fault clearing of line 12.

The SCB reveals better performance in terms of minimum terminal voltages, because the fault is cleared before the terminal voltages reach their lowest possible level as in the slow-acting P-RCB. The lower limit of the terminal voltage depends on the line reactor and DC capacitor size as will be explained in Sections 10.5.2 and 10.5.3. It also depends on the fault resistance and the distance to the fault as described in [BF13b].

The P-RCB exhibits not only lower minimum voltages, but also higher overvoltages after fault clearing compared to the SCB as can be seen in Fig. 10.17. After the current is interrupted in CB2
at 28 ms, the voltage at terminal 2 (green curve) rises to about 1.3 p.u. and the voltage at terminal 1 decreases even further to about 0.1 p.u.. The voltage at terminal 1 later increases to 1.5 p.u. after fault clearance in CB1. The higher overvoltages using P-RCBs are due to the higher currents in the MOAs and, consequently, increased TRV and terminal voltages as compared to the SCB case.

A comparison of maximum and minimum terminal voltages for all CB concepts is illustrated in Fig. 10.19. A trend towards lower minimum voltages at all terminals can be seen for an increasing interruption time, whereas the maximum overvoltages do not show a clear trend. Due to the high time difference between current interruption at CB1 and CB2 in the P-RCB, the maximum overvoltages differ considerably among the terminals, e.g. 1.1 p.u. at terminal 3 and 1.5 p.u. at terminal 1. In general, the remote terminals 3 and
4 are less affected than the terminals 1 and 2 closest to the ground fault.

Figure 10.19: Maximum and Minimum Terminal Voltages for the Base Case

10.5.2 Influence of Line Reactor

Figure 10.20 shows the influence of the line reactor size on the maximum CB current and the maximum terminal and CB voltages in a network with SCBs. A 10 μF DC capacitor, smaller than the default capacitor size, is applied in all the variations to amplify the effect of the line reactor on the CB performance. A larger line reactor reduces the maximum current in CB1 (blue curve) and CB2 (red curve) as expected. A 200 mH reactor results in a maximum current of around 4 kA, whereas CB1 has to interrupt a fault current of 15 kA in case of a small 1 mH reactor in series. A larger line reac-
tor is beneficial in terms of maximum fault current, but it increases substantially the maximum terminal voltage (magenta curve) from 1.1 p.u. at 1 mH to 1.7 p.u. at 150 mH. The voltage across the CBs (cyan curve), however, is only marginally influenced by the reactor size and remains within 1.7 and 1.8 p.u.. The reactor size has no impact on the minimum terminal voltage, which stays at around 0.3 p.u. (not shown in Fig. 10.20).

![Figure 10.20: Influence of the line reactor size on the SCB performance (\(C_{\text{cap}} = 10 \mu\text{F}\))](image)

In general, large line reactors should be avoided, because they deteriorate the control performance due to the increased system time constant. Also the footprint of the converter station increases with increasing reactor size.
10.5.3 Influence of DC Capacitor

In contrast to the line reactor, an increasing DC capacitor size results in an increasing maximum CB current as illustrated in Fig. 10.21. The line reactor is kept constant at 10 mH for all capacitor values. Again, a smaller value than the base case value is chose to amplify the effect of the capacitor.

A large DC capacitor might seem a disadvantage at first glance, since the maximum current in CB1 (blue curve) increases from 10 kA in case of a small DC capacitor of 1 µF to about 15 kA with a large 200 µF capacitor. The voltage stability is, however, considerably improved with a larger DC capacitor due to its voltage supporting function. The minimum terminal voltage (green curve) is increased from 0 to 0.8 p.u. and the overvoltage at terminal 1 (magenta curve) is completely suppressed with capacitors larger than 100 µF. The CB voltage (cyan curve) is again only marginal affected by the DC capacitor size and remains between 1.8 and 1.9 p.u..

A further disadvantage of large dc capacitors is the increased the system inertia and converter station footprint.

10.5.4 Influence of Commutation Delay

In contrast to the SCB, most HCB concepts allow for proactive switching [Twe12,HJ11,WM13], i.e. after local detection of an overcurrent, the current can be commutated temporarily into the commutation path without interruption, while the selective protection is deciding, which CBs have to interrupt. With proactive control, the performance of the HCB can be improved and the time delay of the mechanical disconnector can be partly compensated. Fig. 10.22 compares the required time to CZ and the time to $\frac{di}{dt} < 0$ in a SCB and a HCB for different protection delays between 1 and 6 ms. The base case parameters as summarized in Section 10.4.2 are used in these simulations. For protection delays below 4 ms, the HCB (blue line) requires 9.2 ms independently of the protection delay, while the interruption time in the SCB (red line) increases with
increasing protection delay. The HCB achieves the same interruption times as the SCB only for long protection delays of more than 4 ms, but the gap between the two concepts is significantly reduced even for short protection delays. For a protection delay of 1 ms, the interruption in the HCB is about 2.8 times the interruption time in the SCB, whereas for a delay of 3 ms, the HCB is only about 50% slower than the SCB with respect to time to CZ. The time to negative di/dt shows an even smaller gap of 28%. The HCB exhibits, however, much lower steady-state losses than the SCB and does not require constant cooling of the IGBTs. The losses in a SCB amount to about 350 kW using 120 IGBTs [ABB13].
The highest insulation demands are not at the DC busbars, but at the CBs. Figure 10.23 shows the voltage across CB1 (blue curve) in case of the SCB type 1. Overvoltages of up to 1.7 p.u. are reached after current interruption depending on the V-I characteristics of the MOA. The insulation demands for the IGBTs can be drastically reduced, if SCB type 2 (red curve) is installed with the MOAs in a freewheeling path instead of arrester stacks parallel to the IGBTs as in type 1.
10.6 Conclusions

This chapter describes the modeling of five different HVDC CB concepts and their current interruption strategy. A comparison of the CB’s performance with respect to interruption time, maximum CB current, maximum and minimum terminal voltages, and maximum voltage across the CB is performed. Moreover, the influence of the network component, such as line inductor and DC capacitor, are analyzed.

Due to the high rate of rise of the fault current in a MTDC network, the fault has to be cleared by the CBs as fast as possible. As expected, the fast CB concepts, such as SCB and HCB, perform better than the slower P-RCB and A-RCB. They yield lower interruption times below 10 ms and, consequently, lower maximum CB
currents and voltages. Also the terminals experience less overvoltages and higher minimum terminal voltages.

The performance of the CB depends not only on the CB concept, but also on the network parameters, such as the line inductor, DC capacitor, and protection scheme. A larger inductor results in lower CB currents, but much higher maximum terminal voltages. Contrary to this, a larger DC capacitor improves DC voltage stability, i.e. mitigates overvoltages at the terminals and decreases considerably the voltage drops, but increases slightly the maximum CB current. The detection delay of the network protection impacts mainly the fast CB concepts with short interruption times. In general, the HCB performs worse than SCB, but the gap between the two concepts becomes smaller with increasing detection delay due to proactive switching control in the HCB.

The CB suffers the highest overvoltages up to 1.9 p.u. in a P-RCB and 1.75 p.u. in a SCB right after current interruption. These overvoltages can be suppressed, if the energy absorber is installed in a freewheeling path instead of parallel to the switch.

The analysis in this chapter demonstrates the complex interaction between CB and network components and reveals the trade-off between CB requirement specification and network parameters.
11 Conclusions and Outlook

This thesis supports the derivation of requirement specifications of components in a MTDC network by means of simulations and calculations. It contributes to a deeper understanding of the transient behavior of the MTDC grid during a pole-to-ground fault and analyzes the influencing parameters.

The modeling and implementation of the network components in a MTDC network for the simulation of transient voltages and currents were described first, as well as the required methods for the transient simulations.

In the next step, the fault current’s influencing parameters and components were analyzed in detail. Their influence was identified and quantified through a breakdown of the fault current into its individual contributions from the different fault current feeding sources.

As a first proposal for pre-standardization work, analytic expressions were derived to calculate the rate-of-rise and the maximum amplitude of the individual contributions.

After the network parameter considerations, also the protection of such a MTDC grid was analyzed. Fault clearing support options were identified and their influence on the fault current development investigated.

Finally, different HVDC CB technologies were compared with respect to fault clearing capacity and interruption times, as well as voltage stability.

The analysis in this thesis revealed the differences in the transient behavior between AC and HVDC networks. In DC networks, fault situations affect the entire system to a much larger extent than in
AC systems. Faults propagate faster and the rates-of-rise of the fault currents and voltages are significantly higher than in AC networks.

Due to the global characteristics of transients in HVDC networks, all network components have to be considered, which makes their requirement specification more challenging.

Particularly, the HVDC CB stays in a complex interaction with the network components and its specification ends in a trade-off between CB and network parameters.

This thesis demonstrated how the gap between network and CB requirements can be reduced and showed further improvement potential of the CB technology.

It can be concluded that CB requirements cannot be specified in a straightforward way. The entire system has to be analyzed instead and additional fault clearing support by current and voltage limiting components may be required.

Future research opportunities can be found in the field of system protection, particularly, in the implementation of a detailed fault detection scheme and its coupling with the switchgear. Also converters with full-bridge topology and AC infeed blocking capability shall be considered. Special attention will have to be given to full-bridge MMC converters. They are not only able to block the AC contribution through the converter arms, but also reduce the initial discharge currents from the DC capacitor as they do not need DC side filtering.

Not only transients during fault current interruption have to be investigated, but also during other switching processes, such as load and busbar switching.

More research effort is also needed in the analysis of the influence of DC side faults on the AC network, e.g. on the AC voltage stability.

Standards for the calculation of maximum fault currents will be required in the future to simplify the CB requirement specifications among all vendors. The work in this thesis on the analytic representation of the fault currents has to be continued and improved.
formulas have to be derived and validated. An analytic derivative of the proposed formulas has to be found in order to provide a closed form expression of the rate-of-rise of the fault current and its time to peak.
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