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Design of Bypass Switches for HV/MV Hybrid Transformer Auxiliary Converters

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***Index Terms*—Hybrid Transformer, Smart Grids, Distributed Generation, Power Control, Voltage Control.**

***Abstract*—The design of bypass switches is essential to protect the auxiliary converter connected to the HV/MV power transformer. In this paper critical fault cases are used to determine overcurrents in the HT auxiliary converter. The overcurrents are determined with a power transformer model that includes a core saturation model and parasitic capacitances between the transformer windings. Based on the determined overcurrent levels two bypass switches are designed to protect the HT auxiliary converter against critical faults.**

I. Introduction

The increasing share of renewable energy generation requires a more flexible and smarter grid [1], [2], for controlling voltage and power fluctuations [3], [4]. To address this, various concepts as for example FACTS, grid expansions, and distribution transformers with controllable tap changer have been investigated in the past [5], [6]. An alternative interesting concept for controllable transformers are the so-called hybrid transformers (HT). HT combine a line-frequency power transformer (LFT), which typically transfers the major power share ($\geq 90\%$), with an auxiliary AC/AC power electronics converter [7] for controlling the secondary voltage and the power flow. The AC/AC auxiliary converter is typically connected to an auxiliary winding of the LFT as shown in the single-phase representation of a HT in Fig.1. The auxiliary converter system power rating is typically designed only for a relatively small fraction ($\leq 10\%$) of the total LFT power rating [7], [8]. In general, such power electronics converters as the HT auxiliary converter are relatively sensitive to overcurrents/-voltages, which could occur in the medium voltage (MV) grid for example in case of a fault/lightning strike. Consequently protection systems are required for the HT [9], [7].

In the past, various concepts and topologies for HT [8], [10] as well as for the protection against grid faults at the medium voltage (MV) to low voltage (LV) grid interface [7] have been investigated. A summary and discussion of the most interesting HT and protection concepts can be found in [7], [8], [10]–[14], [16], [17]. The focus in these publications is on HT at the MV/LV grid interface. However, there are significant differences between a protection system for HT at the MV/LV grid interface and a protection system for HT at the high voltage (HV)/MV grid interface. The turns ratio of the transformer at the MV/LV (20kV/400V) grid interface is significantly higher than the turns ratio of the transformer at the HV/MV (110kV/20kV) grid interface. Due to the lower turns ratio transient overvoltages as for example switching impulses (SI) in the HV grid lead to significantly higher overcurrents in the HT auxiliary converter connected the HV/MV transformer. Furthermore, no transient overvoltages are investigated on the LV side for designing the protection system for the auxiliary converter of a HT at the MV/LV grid interface [13]. However, transient overvoltages need to be investigated in the MV grid where the auxiliary converter of the HV/MV HT is connected [15]. At the MV/LV grid interface a single bypass switch is used to protect the HT auxiliary converter [13], [16], [17]. A third difference is that, varistors at the auxiliary winding and a DC-link clamping circuit are sufficient to protect the HT auxiliary converter against transient overvoltages on the primary winding terminals of the MV/LV transformer as discussed in [13]. However, the protection schemes presented in [13], [16], [17] are not sufficient to protect a HT auxiliary converter of a HT at the HV/MV grid interface against overcurrents caused by critical fault cases as for example a SI in the HV grid and three phase (3Φ) short circuits in the MV grid. Such SI in the MV grid, single line-to-ground faults in solidly grounded MV grids, and line-to-line short circuits in the MV grid are identified as critical faults for the HT auxiliary converter at the HV/MV grid interface [15]. For protecting the HT auxiliary converter at the MV/LV grid interface a single bypass switch (Sec Bypass in Fig. 1) is sufficient. However, two bypass switches shown in Fig. 1 must be installed to protect a HT auxiliary converter at the HV/MV grid interface against critical faults. A critical HT auxiliary converter current is reached within microseconds in case of a SI in the HV grid. A mechanical switch MS with a turn on time in the milliseconds range [18] is too slow to bypass the HT auxiliary converter in case of a critical fault. As a consequence, a bypass switch with solid state switches, as for example thyristors, is required to bypass the HT auxiliary converter within a few microseconds. A bypass switch with anti-parallel thyristors that provides a fast bypass path for fault currents is designed for a LV three-phase HT auxiliary converter in [13], and in [17] for a LV single-phase HT auxiliary converter. However, the overcurrents caused by the transient overvoltages due to a SI reach a current level that requires a hybrid bypass switch consisting of thyristors and MS in parallel, in order to keep the number of paralleled thyristors in the bypass switch low. Such a bypass switch with MS and thyristors is designed in [16], for a 5 MVA HT based on an assumed maximum system fault current value for the bypass thyristors. However, transient overvoltages in combination with a transformer model need to be included in the design for the bypass switches for a HT auxiliary converter at the HV/MV grid interface.

A comprehensive bypass switch design for the HT auxiliary converter at the HV/MV grid interface that combines detailed models of the transformer and the converter is missing so far and is presented in this paper. The transformer model used for the bypass switch design includes the transformer parasitic capacitances and the transformer core saturation. Based on the transformer model transient overcurrents excited by transient overvoltages and transferred through the transformer are determined accurately. Determining the overcurrents accurately is important for designing the bypass switch rating. As HT auxiliary converter a three-phase bidirectional AC/AC back-to-back converter is selected. With the transformer model and the converter model the specifications for two bypass switches are derived. The bypass switch specifications are deduced with the overcurrent levels caused by SI in the HV grid or 3Φ-short circuits in the MV grid. HV SI or 3Φ-short circuits lead to the higher overcurrents in the HT auxiliary converter than MV SI, single line-to-ground faults in solidly grounded MV grids, and line-to-line short circuits in MV grids. The bypass switches are designed for AC currents as either solid state or hybrid switches. The solid state bypass switch consists of anti-parallel thyristors, which can conduct the bypass currents for an arbitrary length of time. In the hybrid bypass switch mechanical switches are connected in parallel to the bypass thyristors to take over the bypass currents from the thyristors after a certain time.

In a first step, the functionalities and design of the bypass switches are presented in **section 2**. Next a simulation model of the HT to design the bypass switches for the considered fault cases is given in **section 3**. Then, the specifications for the thyristors in the bypass switches are derived in **section 4**. The design procedure for the bypass switch components is explained in **section 5**. Results and a discussion are provided in **section 6**.

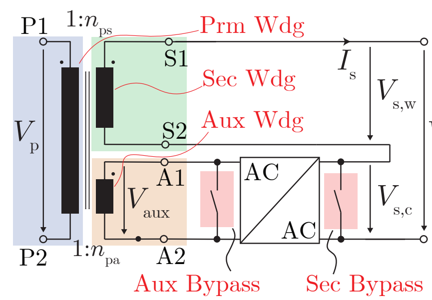

Fig. 1. Single phase representation of HT with bypass switches.

II. Design and Functionalities for the Bypass Switches

Without bypass switches the HT auxiliary converter needs to be designed for current ratings significantly higher than the nominal current rating of the MV grid. Further during the SI in the HV grid, saturation occurs in the core of the considered transformer in case the HT auxiliary converter is not bypassed. For the HT auxiliary converter considered in this paper, two bypass switches are needed as shown in Fig. 1. In Fig. 1 a bypass switch is connected to the auxiliary winding to bypass overcurrents induced by the transformer auxiliary winding. The auxiliary winding bypass switch is denoted as Aux Bypass. The Aux Bypass is designed as a hybrid bypass switch with n_p parallel thyristors and a mechanical switch (MS) in parallel as shown in Fig. 3. Without MS in the Aux Bypass a significant larger number $n_\mathrm{p} > 10$ of parallel thyristors is needed for bypassing the overcurrent in case of a HV SI. The number n_p of thyristors in the Aux Bypass is chosen such that the thermal limit of the thyristors is not exceeded. The thermal limit of the thyristors and the number n_p of parallel thyristors also depends on the turn on time t_on of the MS. The Aux Bypass operates as follows. In case an overcurrent is detected in currents i_c or i_r (Fig. 5) at the detection time t_d the anti-parallel thyristors and the MS of the Aux Bypass are turned on by the switching signals S_MS and S_thy in Fig 2. Note the delay between the fault time t_flt and the detection time t_d. At time $t_\mathrm{d} + t_\mathrm{dt}$ the thyristors start to conduct the bypass current i_bp. Time t_dt is the turn on delay of the thyristors. At time $t = t_\mathrm{d} + t_\mathrm{on}$ the switching contacts of the MS are assumed to be closed and the MS takes over the bypass current i_bp as shown in Fig. 2. Hence, the thyristors conduct the current only for $t_\mathrm{d}+t_\mathrm{dt} \leq t \leq t_\mathrm{d}+t_\mathrm{on}$. As the MS takes over, the number n_p of parallel thyristors in the Aux Bypass can be kept low. The MS conducts the bypass current i_bp until the fault is cleared by the protection system of the HV and/or MV grid. Note that the current levels of currents i_thy and i_MS in Fig. 2 only represent at what time instant the thyristors and the MS in the Aux Bypass conduct the current i_bp. The current levels of currents i_thy and i_MS in Fig. 2 do not represent the actual current levels that are reached in case the Aux Bypass is turned on. The specifications for the Aux Bypass are determined with the worst case fault of a HV SI at the transformers primary winding.

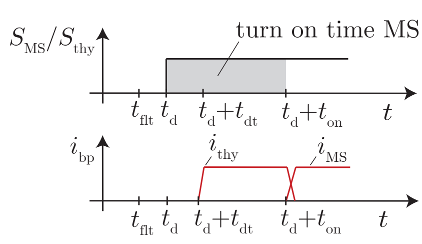

Fig. 2. Switching signals S_MS and S_thy and current waveforms of the thyristors and the MS in the Aux Bypass

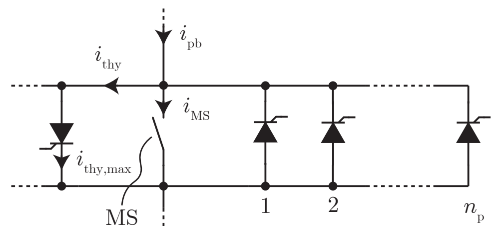

Fig. 3. Single phase representation of a bypass switch with $2n_\mathrm{p}$ thyristors and mechanical switch

The bypass switch in series to the secondary winding in Fig. 1 is denoted as Sec Bypass. The highest bypass current i_bp in the Sec Bypass in case of a 3Φ-short circuit, allows to design the Sec Bypass as a solid state switch with two anti-parallel thyristors per phase. Other than for the Aux Bypass the thyristors in the Sec Bypass are thermally designed to conduct the bypass current i_bp for an arbitrary length of time. In case a fault is detected at time t_d the Sec Bypass is turned on. Then the thyristors in the Sec Bypass conduct the current until the fault is cleared by the protection system of the HV and/or MV grid. The worst case fault to deduce the specifications for the Sec Bypass is the 3Φ short circuit in the MV grid. Both bypass switches the Aux Bypass and the Sec Bypass are turned on in case of SI in the HV and MV grid, during line-to-line short circuits or 3Φ short circuits in the MV grid.

III. Simulation Model for Transient Overvoltages and Three Phase Short Circuits

The specifications for the Aux Bypass and Sec Bypass switches are derived for SI and 3Φ short circuits based on a simulation model. To model the HV/MV HT accurately, a three phase model is chosen. In a three phase model the steady state fault currents are higher than in an equivalent single phase model of the transformer. Additionally modeling the grounding point [19] in Fig. 5 is more complex in a single phase model than in a three phase model. The three phase transformer with core saturation modeled in PLECS is illustrated in Fig. 5 including the nonlinear magnetic core elements for core saturation. The transformer primary winding is connected to the HV grid in delta connection shown in Fig. 4a. The transformer secondary winding is connected to the MV grid with line to ground capacitances C_lg and the load R_L as shown in Fig. 5. The HT auxiliary converter is an AC/AC back-to-back converter, where a three phase converter Ⓢ connected in series to the transformer secondary winding is assumed to operate as inverter. A LC-filter connects the secondary winding and

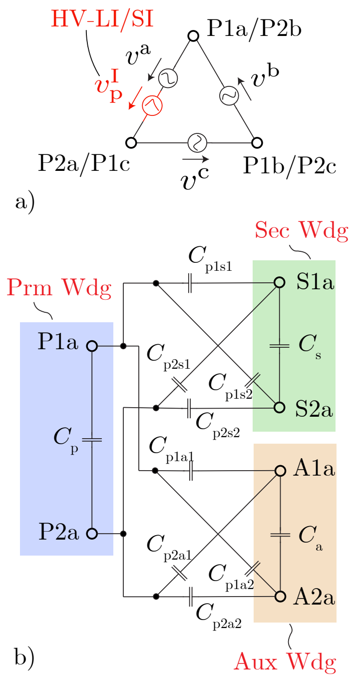

Fig. 4. a) Transformer primary winding connected in delta to the HV grid. b) Parasitic capacitances between the transformer primary, secondary and auxiliary windings in phase 'a'.

converter Ⓢ to filter currents i_c. A grounding inductor L_{co} connects the star point of the filter capacitances C_f to ground. According to [19], the filter capacitances C_f are the preferred grounding point. The three phase converter Ⓐ of the HT auxiliary converter connected to the transformers auxiliary winding is assumed to operate as active rectifier. Again a LC-filter to filter currents i_r connects converter Ⓐ and the auxiliary winding. The remaining terminals of the auxiliary winding are connected in star connection. The Aux Bypass is directly connected to the auxiliary winding terminals, while the Sec Bypass is connected to the secondary winding terminals. The bypass switches are assumed as ideal switches in order to determine the bypass switch currents $i^a_{bp,a}$,..,$i^c_{bp,a}$ and $i^a_{bp,s}$,..,$i^c_{bp,s}$. To limit the maximum current slopes $\frac{di_{bp,a}(t)}{dt}$ and $\frac{di_{bp,s}(t)}{dt}$ for the thyristors in both bypass switches, inductances $L_{pb,a}$ and $L_{pb,s}$ are inserted. Inductances $L_{pb,a}$ and $L_{pb,s}$ limit the current that flows from the filter capacitances C_f of the LC-filters at the time instant $t_d + t_{dt}$ when the bypass switches are closed.

A. *Transformer Parasitic Capacitance Model*

In addition to the SI in the HV grid and 3Φ short circuits in the MV grid, LI are investigated with the simulation model in Fig. 5. According to [15], LI are not critical for the HT auxiliary converter at the HV/MV grid interface. Therefore, the maximum overcurrent i_{max} excited by a LI is the maximum short time overcurrent the HT auxiliary converter is designed for. In other words, the HT auxiliary converter is designed to ride through LI without the bypass being closed. The maximum current i_{max} during LI plus a margin i_{extr} yields the tripping current $i_{trip} = i_{max} + i_{extr}$ up to which the Aux Bypass and Sec Bypass switches are not closed. This means the converter stays connected to the power transformer during a LI. Due to the fast transient LI the parasitic capacitances shown in Fig. 4b) are included into the simulation model since the parasitic capacitances are important to determine the tripping current i_{trip}. On the other hand the parasitic capacitances are not included in the simulation model for the thermal design of the bypass switches with SI in the HV grid or the 3Φ short circuit in the MV grid. The differences in the current i_{bp} flowing through the bypass switch in case of HV SI or 3Φ short circuit with and without the parasitic capacitances are small compared to the current values of currents i_{bp} during bypass operation. Therefore, the parasitic capacitances are only considered in simulations, where the HT auxiliary converter is not bypassed. The basic calculation of the parasitic capacitances is explained in [15].

B. *Fault Cases for Bypass Switch Specifications*

To determine the maximum currents $i^a_{bp,a}$,..,$i^c_{bp,a}$ and $i^a_{bp,s}$,..,$i^c_{bp,s}$ two fault cases where the HT auxiliary converter is bypassed are simulated. First, a SI is simulated in phase 'a' of the HV grid represented by voltage v^I_p in Fig. 4b). Second, the secondary winding is short circuited by the 3Φ short circuit illustrated in Fig. 5. Both faults lead to an overcurrent significantly higher than the tripping current i_{trip} of the bypass switches. In case the bypass switches are tripped by a fault, the converter switches are turned off at the same time.

C. *Control and Modulation Scheme*

The converter Ⓢ is controlled with a single voltage control loop to control voltages $v^a_{C,f}$-$v^c_{C,f}$ in Fig. 5 as described in [15]. The converter Ⓐ is controlled with a conventional two loop control approach. The inner control loop controls currents i^a_{aux},..., i^c_{aux}, while the outer control loop controls the DC-link voltage v_{dc} in Fig. 5 [20]. Each control loop is implemented as PI controller with the inner control loop and the voltage control loop in the dq-domain. The switching signals for converters Ⓐ and Ⓢ are controlled with space vector modulation.

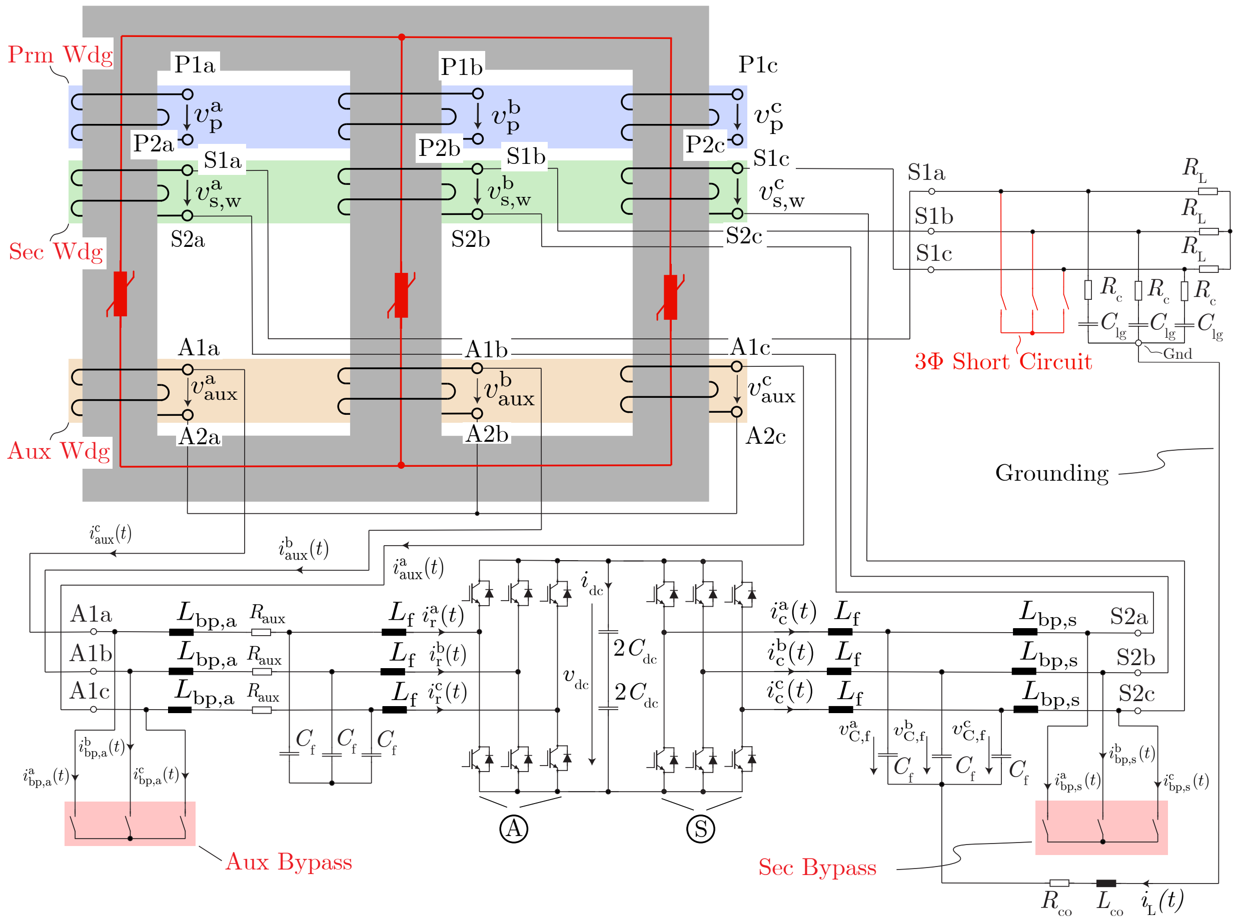

Fig. 5. Three-phase power transformer with core saturation model connected to the HT auxiliary converter.

IV. Specifications of the Bypass Switches

The specifications for the current rating i_{thy} of the thyristors in the Aux Bypass and the Sec Bypass are determined with the bypass currents i_{bp} flowing during the bypass operation. The minimum blocking voltage V_{DRM} of the bypass thyristors is calculated with voltage $v_{\mathrm{C,f}}$ plus the safety margin defined for two level voltage source inverters in [21]. The thyristors for the Aux Bypass and the Sec Bypass are selected based on the thyristor blocking voltage V_{DRM}. For the selected thyristors the maximum on state current slope $\frac{\mathrm{d}i_{\mathrm{bp}}}{\mathrm{d}t}$ is given in the thyristors data sheet. With V_{DRM} and the allowed $\frac{\mathrm{d}i_{\mathrm{bp}}}{\mathrm{d}t}$, the inductances $L_{\mathrm{bp,a}}$ and $L_{\mathrm{bp,s}}$ for limiting the current slopes are determined with (1).

$$L_{\mathrm{bp}} > \frac{V_{\mathrm{DRM}}}{\frac{\mathrm{d}i_{\mathrm{bp}}}{\mathrm{d}t}} \tag{1}$$

Various thyristor types including bi-directionally controlled thyristors, asymmetric bypass thyristors, pulse power thyristors, and phase controlled thyristors are commercially available. Bi-directional controlled thyristors conduct current in both directions through a single disc [22]. Therefore, the thyristor's junction temperature reaches higher levels for the same current level compared to two anti-parallel thyristor discs. There is a significant difference in the forward and reverse blocking voltage of asymmetric bypass thyristors [23] which is not desired for the Aux Bypass and the Sec Bypass. The allowed mean on state current and surge on state current is significantly lower for pulse power thyristors than for phase controlled thyristors [24] and therefore phase controlled thyristors are chosen for the Aux Bypass and the Sec Bypass. Due to the MV level and the current rating of the Aux Bypass the turn on time t_{on} for the MS is assumed as turn on time of a MV vacuum circuit breaker [18]. The turn on time t_{on} of the MS is one important design criterion for the number n_{p} of parallel thyristors needed in the Aux Bypass. The number n_{p} in the Aux Bypass is determined with a thermal model implemented in PLECS. When thyristors are connected in parallel the equal sharing of the bypass current i_{bp}

is essential. A symmetric layout is key to connect the paralleled thyristors with equal parasitic inductances to achieve equal current sharing. A symmetric layout can be achieved with two disc shaped buses in order to split the bypass current i_{bp} equally among the n_{p} thyristors [25]. The disc shaped bus allows to arrange the thyristors in a circle between the two disc buses as presented in [25] for $n_{\mathrm{p}} = 8$ thyristors and for pulse shaped currents in the kA range. Therefore, disc shaped buses with circular arrangement of the paralleled thyristors could be considered for a future prototype design of the Aux Bypass. Further, the positive temperature coefficient of the selected thyristors forward voltage V_{F} contributes to insure equal current sharing.

V. Thermal Design for the Bypass Thyristors

Thyristors from different manufacturers are selected for a thermal design of the Aux Bypass and Sec Bypass.

A. Aux Bypass

The thermal design of the Aux Bypass is based on a thermal model extracted from the data sheets of the selected thyristors and implemented in PLECS. Due to the short turn on time t_{on} of the Aux Bypass thyristors a thermal model to determine the transient behavior of the junction temperature T_{j} is needed. The thermal model provided by the thyristors data sheet allows to determine the junction to case thermal resistances $R_{\mathrm{th,j,c,1}}...R_{\mathrm{th,j,c,i}}$ and thermal capacitances $C_{\mathrm{th,j,c,1}}...C_{\mathrm{th,j,c,i}}$ shown in Fig. 6. PLECS converts the thermal model extracted from the data sheet internally into a Cauer model [26]. As a consequence, the thermal model in Fig. 6 is represented by a Cauer model. The variation in the case temperature of the thyristors is assumed to be negligible due to the short turn on time t_{on}. Therefore, the Cauer model in Fig. 6 is directly connected to the ambient temperature T_{amb}. Connecting the Cauer model of the Aux Bypass thyristors directly to ambient leads to an accurate estimation of the thyristors junction temperature T_{j} with the thermal model extracted from the thyristors data sheet [26]. The minimum number n_{p} of thyristors in parallel for the Aux Bypass is given by the number n_{p} of thyristors required to keep the junction temperature T_{j} below the maximum allowed junction temperature $T_{\mathrm{j,max}}$ given in the thyristors data sheet. In order to determine the number n_{p} of thyristors in parallel, the highest bypass current $i^{\mathrm{a}}_{\mathrm{bp,a}},..,i^{\mathrm{c}}_{\mathrm{bp,a}}$ flowing through the Aux Bypass is considered. The highest bypass current $i^{\mathrm{a}}_{\mathrm{bp,a}},..,i^{\mathrm{c}}_{\mathrm{bp,a}}$ is caused by the SI in the HV grid.

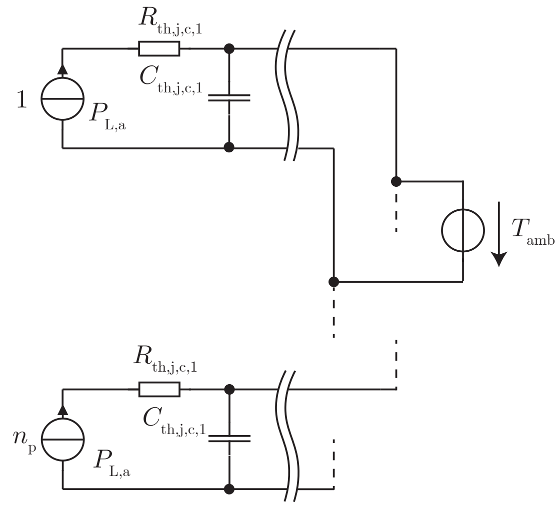

Fig. 6. Thermal model for the Aux Bypass

B. Sec Bypass

The Sec Bypass thyristors are turned on for an arbitrary length of time. The bypass currents $i^{\mathrm{a}}_{\mathrm{bp,s}},..,i^{\mathrm{c}}_{\mathrm{bp,s}}$ considered for the thermal design of the thyristors lead to losses $P_{\mathrm{L,s}}$ in the thyristors. The thermal network for the thermal steady state analysis consists of the source $P_{\mathrm{L,s}}$ representing the conduction losses of the thyristor, the thermal junction to case resistance $R_{\mathrm{th,j,c}}$, the thermal case to heat sink resistance $R_{\mathrm{th,c,hs}}$ and the thermal heat sink resistance $R_{\mathrm{th,hs}}$ connected to ambient T_{amb}. The thermal resistances $R_{\mathrm{th,j,c}}$, $R_{\mathrm{th,c,hs}}$, and $R_{\mathrm{th,hs}}$ are the thermal resistances of the Foster model determined from the data sheets of the thyristors and the heat sink. The estimation of the thyristors junction temperature T_{j} in a steady state thermal analysis with the thermal resistances $R_{\mathrm{th,j,c}}$, $R_{\mathrm{th,c,hs}}$, and $R_{\mathrm{th,hs}}$ and the step wise power loss $P_{\mathrm{L,s}}$ is in good agreement with thermal models validated through measurements [27]. The considered HT auxiliary converter is assumed to be water cooled as for example back-to-back converters in wind power applications with a similar power rating [28], [29]. With the water cooled HT auxiliary converter, water cooling is also chosen for the Sec Bypass. Therefore, thyristors with a water cooled heat sink with double sided cooling are assumed for the Sec Bypass. The junction temperature T_{j} of the Sec Bypass thyristors needs to stay below the maximum allowed junction temperature $T_{\mathrm{j,max}}$ given in the thyristors data sheet. In order to determine the junction temperature in steady state the losses $P_{\mathrm{L,s}}$ of the thyristors during bypass are determined. The losses $P_{\mathrm{L,s}}$ are calculated with the highest bypass currents $i^{\mathrm{a}}_{\mathrm{bp,s}},..,i^{\mathrm{c}}_{\mathrm{bp,s}}$ through the Sec Bypass during a 3Φ-short circuit in the MV grid.

VI. Results and Discussion

The results for the bypass switch design are based on a case study HV/MV HT. Only the most important case study parameters are listed in table I, while important parameters for the DC-link capacitance C_{dc}, the filter capacitances C_{f}, the filter inductances L_{f}, the switching frequency f_{sw}, the grounding inductance L_{co}, and the line to ground capacitances $C_{\mathrm{l,g}}$ are identical to the parameters presented in [19]. The HT auxiliary converter's DC-link voltage v_{dc} is regulated by the voltage controller to $v_{\mathrm{dc}} = 4\mathrm{kV}$. The HT auxiliary converter's power rating is $P_{\mathrm{c}} = 5.6\mathrm{MW}$. The standard SI and LI for the HV and MV gird are defined in [30] and [31].

TABLE I
General design parameters for the case study HT.

P_{n}	V_{p}	$V_{\mathrm{s,w}}$	V_{aux}	I_{s}
45MW	110kV	20kV	3kV	1.3kA

TABLE II
Parameters for HV/MV power transformer.

N_{prm}	N_{sec}	N_{aux}	A_{Fe}	B_{sat}	μ_{r}
1518	276	41	$0.2875\mathrm{m}^2$	1.8T	1500

The most important parameters for the HV/MV power transformer are listed in table II. The transformer geometry is derived from a HV/MV power transformer in [32] and more detailed geometry parameters are given in [15]. The saturation flux density B_{sat} and the relative permeability μ_{r} for power transformers are given in [33].

For the bypass switch design, the HT auxiliary converter is operated at nominal power P_{c} such that the nominal current $I_{\mathrm{c}} = I_{\mathrm{s}}$ flows through converter Ⓢ. Then the six fault cases the HV LI, MV LI, HV SI, MV SI, line-to-line short circuit and 3Φ short circuit are investigated. Only the results for the HV LI, HV SI and the 3Φ short circuit are shown in the following. The other faults result in lower bypass currents than during HV-SI and 3Φ short circuits. All faults are assumed to occur after $t_{\mathrm{flt}} = 3\mathrm{s}$.

A. Results

The HV LI leads to the highest overcurrent i_{trip} where the HT auxiliary converter is not bypassed. Results for currents i_{r} in converter Ⓐ during a HV LI are shown in Fig. 7. The maximum current reached is $i_{\mathrm{r,max}} = 2.45\mathrm{kA}$. The tripping current i_{trip} is then set to $i_{\mathrm{trip}} = 2.6\mathrm{kA}$ to avoid the bypass switches tripping during a HV LI. The current waveforms in Fig. 7 show that the currents i_{r} in converter Ⓐ reach their pre-fault waveforms after the fault within a few time periods T_{g} in the grid.

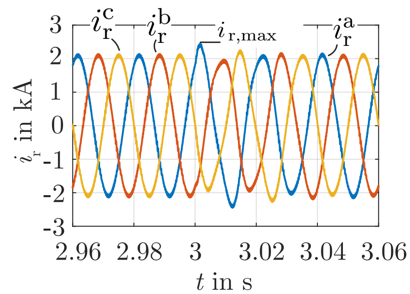

Fig. 7. Currents i_{r} of converter Ⓐ during LI at the transformer primary winding.

Next the two remaining fault cases namely the HV SI and the 3Φ short circuit are investigated. The HV SI fault case leads to the highest overcurrent in the HT auxiliary converter. To highlight the importance of the Aux Bypass and the Sec Bypass the HV SI is first investigated without the HT auxiliary converter being bypassed. The HV SI leads to a maximum overcurrent in converter Ⓐ of $i_{\mathrm{r,max}} \approx 10\mathrm{kA}$ as shown in Fig. 8. Assuming a HT auxiliary converter design to sustain a HV SI, switches with more than four times the current rating are required. Therefore, a bypass scheme is needed for the HV SI and also for MV SI, single line to ground short circuits in solidly grounded grids, line-to-line short circuits, and 3Φ short circuit fault cases.

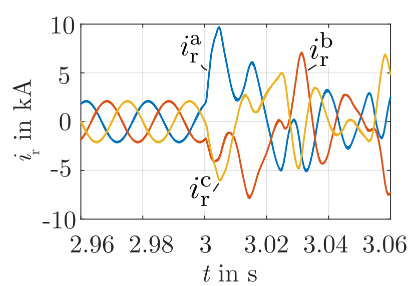

Fig. 8. Currents i_{r} of converter Ⓐ during the HV SI at the transformer primary winding without bypass.

The saturation of the power transformer core is an important result during the HV SI fault without bypass. The magnetic flux density B_{a} in phase 'a' of the transformer core reaches values $|B_{\mathrm{sat}}| < |B_{\mathrm{a}}|$ where the core becomes saturated as shown in Fig. 9. The saturation of the transformer core could lead to undesired distortion, unbalances, and DC-offsets in currents i_r and i_c in the HT auxiliary converter and consequently also in the MV grid.

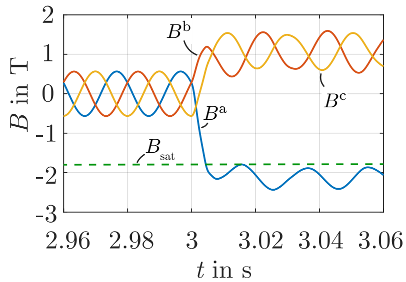

Fig. 9. Transformer core magnetic flux density B_abc during the HV SI at the transformer primary winding without bypass.

The Aux Bypass currents $i^\mathrm{a}_\mathrm{bp,a}$,..,$i^\mathrm{c}_\mathrm{bp,a}$ during bypassing in event of a HV SI fault are shown in Fig. 10. The Aux Bypass needs to be designed for a maximum current of $i_\mathrm{bp,a} \approx$ 90kA with high DC-offset. Therefore, a significant number n_p of thyristors in parallel is needed for the Aux Bypass. Further due to the high current reached during the HV SI the bypass currents are taken over from the thyristors by a MS in parallel. Note, that no saturation is reached in the transformer core with the converter bypassed by the Aux Bypass during the HV-SI.

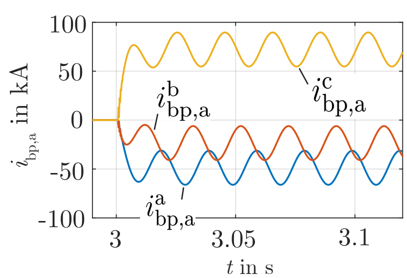

Fig. 10. Auxiliary winding bypass switch currents $i^\mathrm{a}_\mathrm{bp,a}$,..,$i^\mathrm{c}_\mathrm{bp,a}$ during HV SI at the transformer primary winding and bypass.

The design case for the Sec Bypass currents $i^\mathrm{a}_\mathrm{bp,s}$,..,$i^\mathrm{c}_\mathrm{bp,s}$ during a 3Φ short circuit is shown in Fig 11. The Sec Bypass currents $i^\mathrm{a}_\mathrm{bp,s}$,..,$i^\mathrm{c}_\mathrm{bp,s}$ are interfered by oscillations with the resonance frequency of inductances $L_\mathrm{bp,s}$ and the filter capacitances C_f. The maximum current through the Sec Bypass is $i_\mathrm{bp,s} \approx$ 7.3kA. The thyristors in the Sec Bypass are designed to conduct currents $i^\mathrm{a}_\mathrm{bp,s}$,..,$i^\mathrm{c}_\mathrm{bp,s}$ in Fig 11. for an arbitrary length of time.

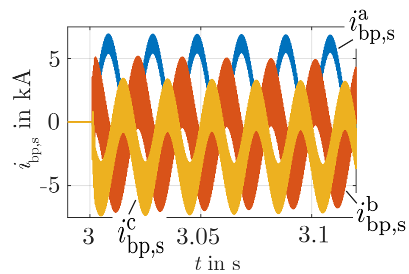

Fig. 11. Secondary winding bypass switch currents $i^\mathrm{a}_\mathrm{bp,s}$,..,$i^\mathrm{c}_\mathrm{bp,s}$ during 3Φ short circuit in the MV grid and bypass.

Two phase controlled thyristor discs from Dynex and ABB/Hitachi are considered in order to design the Aux Bypass and Sec Bypass. For all thyristors double side cooling is assumed. Results for the Aux Bypass and the Sec Bypass design with the Dynex DCR6650H42 thyristor [34] and the ABB/Hitachi 5STP 38Q4200 thyristor [35] are presented in the following.

First the Aux Bypass is designed with bypass currents $i^\mathrm{a}_\mathrm{bp,a}$,..,$i^\mathrm{c}_\mathrm{bp,a}$ during SI in the HV grid. In the hybrid Aux Bypass the bypass currents $i^\mathrm{a}_\mathrm{bp,a}$,..,$i^\mathrm{c}_\mathrm{bp,a}$ are taken over by a MS after an assumed closing time of t_on = 140ms. The closing time t_on includes a safety margin so that the number n_p of thyristors in parallel is sufficient in case closing the contacts of the MS takes longer than the closing time for a vacuum circuit breaker determined in [18]. Therefore, the closing time is set to t_on = 140ms, which is twice the closing time for a vacuum circuit breaker in [18]. For keeping the junction temperature T_j below the maximum junction temperature $T_\mathrm{j,max}$ a minimum of n_p = 6 thyristors in parallel from ABB and n_p = 4 thyristors in parallel from Dynex are required. The junction temperature T_j of the ABB thyristors and the Dynex thyristors during bypass operation of the Aux Bypass is shown in Fig. 12, where the junction temperatures T_j stay below $T_\mathrm{j,max}$. The maximum current $t_\mathrm{thy,max}$ per thyristor is $i_\mathrm{thy,max}$ = 14.9kA for the 6 parallel thyristors from ABB and $i_\mathrm{thy,max}$ = 22.4kA for the 4 parallel thyristors from Dynex. To limit the current slope $\frac{\mathrm{d}i_\mathrm{bp,max}}{\mathrm{d}t}$ in the Aux Bypass inductance $L_\mathrm{bp,a} = 40\mu$H is determined.

For the design of the Sec Bypass, the same phase controlled thyristors from Dynex and ABB/Hitachi are considered. The thyristors in the Sec Bypass are designed to conduct the bypass currents $i^\mathrm{a}_\mathrm{bp,s}$,..,$i^\mathrm{c}_\mathrm{bp,s}$ during a 3Φ short circuit in the MV grid for an arbitrary length of time. Therefore, a water cooled heat sink from DAU

[36] is chosen for the thyristors in the Sec Bypass. With the water cooled heat sink, no thyristors in parallel are required for the Sec Bypass to keep the junction temperature T_j below the maximum junction temperature $T_\mathrm{j,max}$. The junction temperature T_j of the Dynex thyristors in the Sec Bypass reaches $T_\mathrm{j} = 55C^\circ$ and the junction temperature T_j of the ABB thyristors in the Sec Bypass reaches $T_\mathrm{j} = 75C^\circ$ in steady state. Note that the losses $P_\mathrm{L,s}$ in the Sec Bypass are lower with thyristors from Dynex than with thyristors from ABB. Therefore, thyristors from Dynex are selected for the Sec Bypass. The maximum current $i_\mathrm{thy,max}$ for the thyristors in the Sec Bypass is $i_\mathrm{thy,max} = 7.3\mathrm{kA}$. To limit the current slope $\frac{\mathrm{d}i_\mathrm{bp,max}}{\mathrm{d}t}$ in the Sec Bypass inductance $L_\mathrm{bp,s} = 20\mu\mathrm{H}$ is determined.

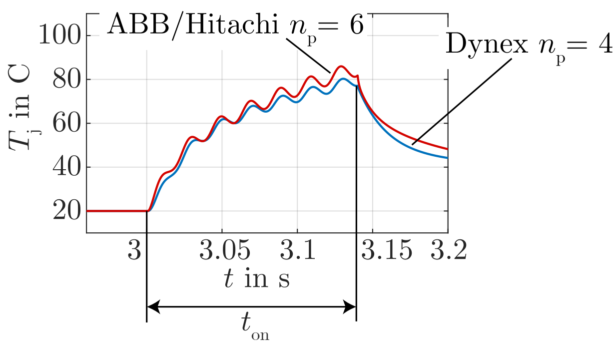

Fig. 12. Junction temperature T_j of the thyristors in the Aux Bypass during bypass

B. Discussion

The results for the Aux Bypass show that a low number of 4 parallel thyristors is achieved with the Dynex thyristor disc. Therefore, the Dynex thyristors are selected for the Aux Bypass. The bypass currents need to be taken over by the vacuum MS in order to keep the number n_p of parallel thyristors in the Aux Bypass low. Due to the MS and the short turn on time of the thyristors, cooling through natural convection is assumed. For the Sec Bypass no thyristor in parallel is needed to conduct the bypass currents for an arbitrary length of time. A water cooled heat sink keeps the junction temperature below the maximum junction temperature. Dynex thyristors lead to lower conduction losses and are preferred over the ABB thyristors for the Sec Bypass. The inductances $L_\mathrm{bp,a}$ and $L_\mathrm{bp,s}$ lead to a current slope within the limits defined in the data sheets. The most important design parameters for the Aux Bypass and the Sec Bypass are summarized in table III.

TABLE III
DESIGN PARAMETERS FOR BYPASS SWITCHES.

	$i_\mathrm{thy,max}$	n_p	$L_\mathrm{bp,a}/L_\mathrm{bp,s}$	$\frac{\mathrm{d}i_\mathrm{bp,max}}{\mathrm{d}t}$	V_DRM
Aux Bypass	22.4kA	4	40μH	173.65$\frac{\mathrm{A}}{\mathrm{s}}$	4.2kV
Sec Bypass	7.3kA	1	20μH	144$\frac{\mathrm{A}}{\mathrm{s}}$	4.2kV

VII. Conclusion

Two bypass switches are designed to bypass the HV/MV HT auxiliary converter in event of critical faults. The tripping current for the bypass switches is defined and current limiting inductors are designed. The number of thyristors in parallel for both bypass switches are determined based on the highest expected bypass currents. For the bypass switch connected to the transformer auxiliary winding of the considered case study HT a hybrid bypass switch is chosen with 4 parallel thyristors and a maximum current of $i_\mathrm{thy,max} = 22.4\mathrm{kA}$ per thyristor. No thyristors in parallel are required for the Sec Bypass with a maximum thyristor current of $i_\mathrm{thy,max} = 7.5\mathrm{kA}$ per thyristor. For the Aux Bypass natural convection is sufficient as cooling method while for the Sec Bypass a water cooled heat sink is assumed.

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