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Influence of Process Variations on the Electrical Performance of SiC Power MOSFETs

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***Abstract*— The SiC power MOSFET is a promising solution for power electronics applications demanding high power densities and efficiencies. High current applications typically use several transistors in parallel, which have to operate synchronously. Commercial SiC power MOSFETs, however, show a significant performance spread in electrical behavior and lifetime due to immature processing technology. Based on a TCAD simulation model calibrated to a 1.2 kV SiC MOSFET the critical processing steps are detected. It can be shown that controlling the epitaxial doping concentration as well as the interface trap density is most important for a reliable device fabrication.**

***Index Terms*— Power MOSFET, Process Variation, Sensitivity, SiC, TCAD Simulation.**

I. Introduction

To further increase the power density and the efficiency of power electronics systems, new materials such as wide bandgap semiconductors are explored. Due to its promising characteristics silicon carbide (SiC) has been intensively investigated over the last years [?], [?], [?], [?]. Power MOSFETs based on SiC are one of the most desired devices as they combine fast switching, high blocking capability and high junction temperature operation. However, their maturity level is yet not comparable to silicon based devices [?]. On the one hand, commercial SiC MOSFETs show a significant variation of the static electrical behavior within one device line, which is problematic especially for high current applications using parallel connections [?], [?]. On the other hand, the lifetime expectancy under stress varies significantly as well as the mechanism leading to an irreversible device failure [?]. These performance variations can be explained by unreliable fabrication processes which are sensitive to ambient conditions leading e.g. to different doping concentrations or mobilities [?], [?]. Hence, it is necessary to improve the processing technology for SiC to achieve better reliability, performance and thus yield of SiC power devices [?].

In order to purposefully improve the processing technology for SiC, it is important to detect the critical steps, which highly influence the device performance. A number of studies have been addressed to process variations in CMOS technology, [?], [?], [?], focusing on channel length and oxide thickness variation. SiC JFETs used in parallel connections have been investigated with respect to their dependence on variations of the p$^+$-gate doping profile [?]. For SiC power MOSFETs, however, no study exists.

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While physical Spice models, [?], could be used for the investigation of process variations, numerical simulation models including the MOSFET cell structure provide a higher degree of accuracy [?]. Therefore, the aim of this work is to investigate typical process variations and their influence on the device performance at room and elevated temperature with (Sentaurus) TCAD simulations. Based on process simulations resulting in the device structure shown in Fig. 1, the simulation model is calibrated to the measured characteristics of Wolfspeed's 1.2 kV SiC power MOSFET (C2M0080120D) [?]. For this purpose, eight MOSFETs are measured at room temperature, while three of them are additionally measured at elevated temperature. The simulation is fitted to the worst device. The reproduced transfer and output characteristics which show the key information, i.e. the threshold voltage and the on-state resistance, are shown in Fig. 2 and Fig. 3. As the simulations are done in a stationary mode, no self-heating takes places and thus the current is slightly overestimated compared to the measurement. The breakdown voltage is another key parameter which is also included in the model. Measurements reveal breakdown voltages ranging from 1610 V to 1675 V, while the simulation model exhibits a breakdown voltage of 1665 V. In the following, the most important components of the device design, namely the epitaxial layer, the surface, the gate-oxide, the interface traps and the inversion layer will be discussed (Fig. 1). Their sensitivity to exemplarily reported process variations will be investigated. Finally, two MOSFETs from the measured device line are analyzed regarding their structural differences using scanning electron microscopy (SEM).

II. Process Variations

A. Epitaxial Layer

The first step of the fabrication process after growing the substrate is the creation of the active layer of drift layer. This is typically done by epitaxial growth using chemical vapor deposition, where its thickness and doping concentration are the main design parameters.

Variations of the growth rate can influence the thickness of the drift layer [?]. Based on exemplary product specifications of n-type epitaxial layers with $d_{\mathrm{epi}} = 10\ \mu\mathrm{m}$, a variation in thickness of $\pm 10\ \%$ is assumed for the simulation [?]. The simulated structure consists of a main epitaxial layer, which is 10 μm thick, and a top epitaxial layer, which is 0.6 μm

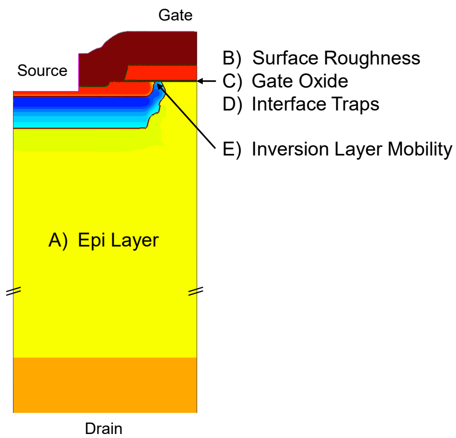

Fig. 1. Structure of simulated MOSFET (C2M0080120D from Wolfspeed) obtained by process simulations, where SEM images have been used as reference. Regions exposed to variations are indicated.

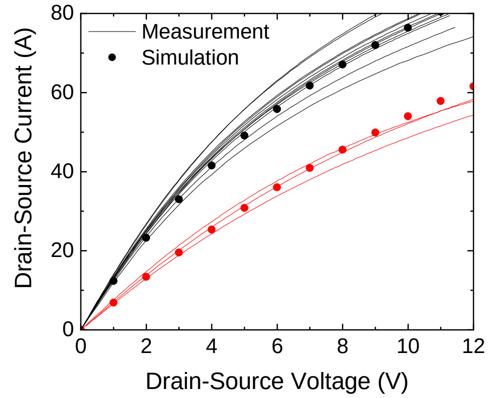

Fig. 3. Output characteristics for $V_{\mathrm{GS}} = 20\ \mathrm{V}$ at $T = 25\ °\mathrm{C}$ (black) and $T = 150\ °\mathrm{C}$ (red). Different devices from the same device line are measured, while the simulation represents a specific device.

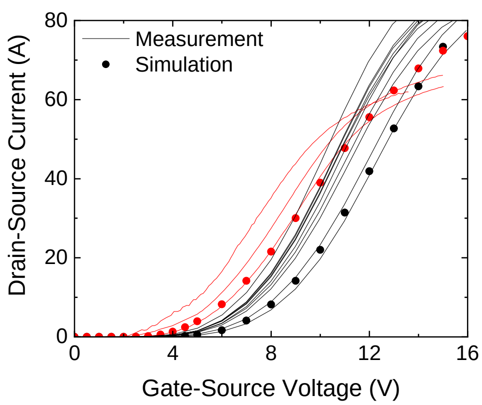

Fig. 2. Transfer characteristics for $V_{\mathrm{DS}} = 20\ \mathrm{V}$ at $T = 25\ °\mathrm{C}$ (black) and $T = 150\ °\mathrm{C}$ (red). Different devices from the same device line are measured, while the simulation represents a specific device.

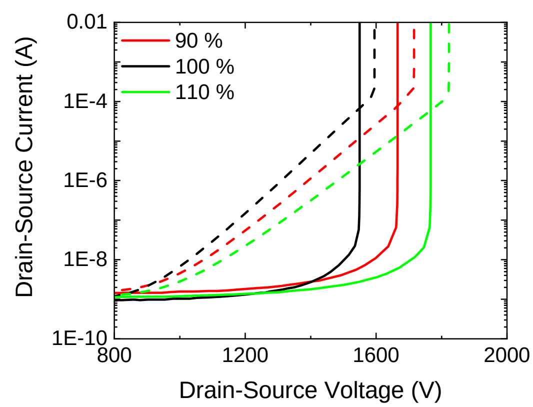

Fig. 4. Influence of epi thickness on breakdown characteristics for $V_{\mathrm{GS}} = 0\ \mathrm{V}$ at $T = 25\ °\mathrm{C}$ (solid) and $T = 150\ °\mathrm{C}$ (dash). $100\ \%$ equals a main epitaxial layer thickness of $10\ \mu\mathrm{m}$. The top layer has a constant thickness of $0.6\ \mu\mathrm{m}$.

thick. Here, only the main epitaxial layer thickness is varied, which affects the drift resistance and the breakdown withstand capability. The resulting influence on the on-state resistance is rather negligible ($\pm 2\ \%$), whereas the breakdown behavior is highly sensitive to the variation. Fig. 4 shows, that a decrease of $10\ \%$ in thickness results in a $7\ \%$ reduced breakdown voltage. At elevated temperature, the relation between drift layer thickness and breakdown voltage is similar. Additionally, a channel leakage current can be observed due to a higher intrinsic carrier concentration and a lowered threshold voltage.

Another property of the epitaxial layer is its doping concentration. For n-channel MOSFETs, typically nitrogen is used as drift layer dopant [**?**]. During the epitaxial growth the doping concentration is influenced by the precursor flow rate and the growth temperature [**?**]. This can lead to a variation in drift layer doping of $\pm 25\ \%$ [**?**]. A higher concentration lowers, on the one hand, the drift resistance, and, on the other hand, the threshold voltage, as the net p-body concentration is reduced. The corresponding influence on the output characteristics of the modeled power MOSFET, where both epitaxial layer concentrations are varied, is shown in Fig. 5. An increase of $25\ \%$ in concentration leads to a reduction in on-state resistance of around $11\ \%$ at $I = 20\ \mathrm{A}$ and $V_{\mathrm{GS}} = 20\ \mathrm{V}$ for $T = 25\ °\mathrm{C}$. At elevated temperature the same increase in concentration leads to a $15\ \%$ lower on-resistance. This indicates that the drift resistance is more dominant at higher temperatures. The influence on the transfer characteristics, i.e. the threshold voltage, can be seen in Fig. 6. A $25\ \%$ higher drift concentration lowers the threshold voltage by $0.25\ \mathrm{V}$, where the interception of tangent and x-axis is considered as V_{th}. At elevated temperature, the same shift occurs with increased concentration.

B. Surface Roughness

Due to the processes of epitaxial growth, post implantation annealing and etching, the surface of the epitaxial layer is not ideally plane. These processes highly depend on ambient conditions such as pressure, temperature and gas flow. Also the usage of a carbon cap during post implantation annealing can affect the surface properties. Resulting surface roughnesses with correlation lengths in the $10\ \mathrm{nm}$ and $100\ \mathrm{nm}$ range are

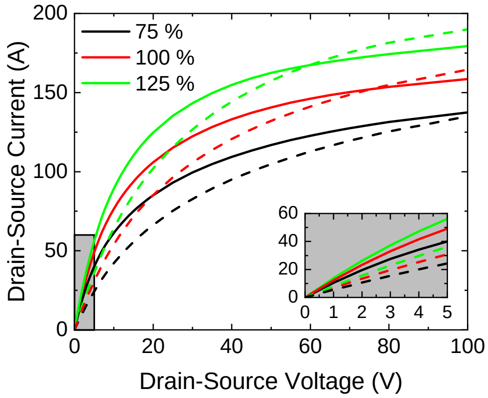

Fig. 5. Influence of drift doping concentration on output characteristics for $\boldsymbol{V_{\mathrm{GS}} = 20\ \mathrm{V}}$ at $\boldsymbol{T = 25\ ^\circ\mathrm{C}}$ (solid) and $\boldsymbol{T = 150\ ^\circ\mathrm{C}}$ (dash). $\boldsymbol{N_{\mathrm{D,main,100\%}} = 8 \times 10^{15}\ \mathrm{cm^{-3}}}$ and $\boldsymbol{N_{\mathrm{D,top,100\%}} = 2.8 \times 10^{16}\ \mathrm{cm^{-3}}}$.

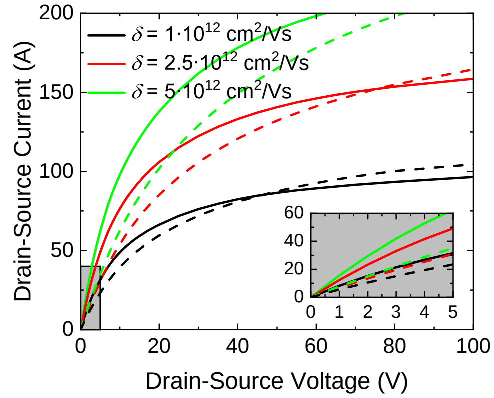

Fig. 7. Influence of surface roughness on output characteristics for $\boldsymbol{V_{\mathrm{GS}} = 20\ \mathrm{V}}$ at $\boldsymbol{T = 25\ ^\circ\mathrm{C}}$ (solid) and $\boldsymbol{T = 150\ ^\circ\mathrm{C}}$ (dash). The initial value is $\boldsymbol{\delta = 2.5 \cdot 10^{12}\ \mathrm{V/s}}$.

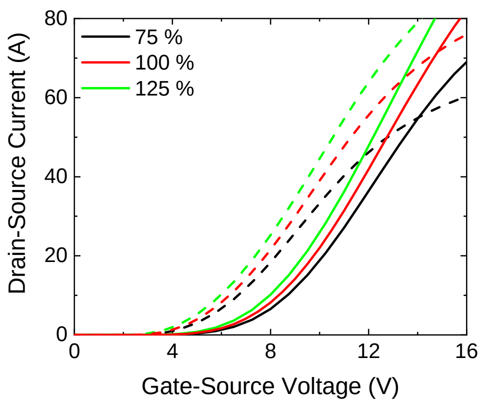

Fig. 6. Influence of drift doping concentration on transfer characteristics for $\boldsymbol{V_{\mathrm{DS}} = 20\ \mathrm{V}}$ at $\boldsymbol{T = 25\ ^\circ\mathrm{C}}$ (solid) and $\boldsymbol{T = 150\ ^\circ\mathrm{C}}$ (dash). $\boldsymbol{N_{\mathrm{D,main,100\%}} = 8 \times 10^{15}\ \mathrm{cm^{-3}}}$ and $\boldsymbol{N_{\mathrm{D,top,100\%}} = 2.8 \times 10^{16}\ \mathrm{cm^{-3}}}$.

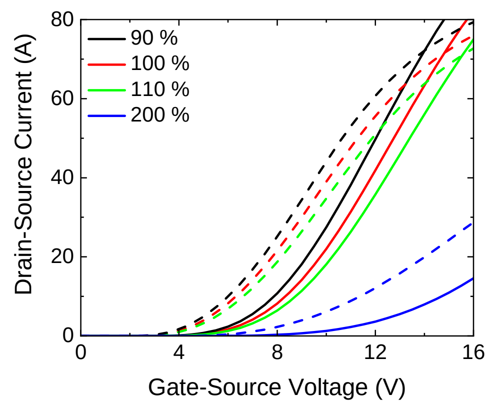

Fig. 8. Influence of gate-oxide thickness on transfer characteristics for $\boldsymbol{V_{\mathrm{DS}} = 20\ \mathrm{V}}$ at $\boldsymbol{T = 25\ ^\circ\mathrm{C}}$ (solid) and $\boldsymbol{T = 150\ ^\circ\mathrm{C}}$ (dash). 100 % equals 40 nm.

reported [**?**], [**?**]. Within numerical device simulations, the effect of surface roughness is included in a mobility model where a fitting parameter δ is used to reproduce the correct mobility degradation mechanism [**?**], [**?**]. A very rough surface leads to locally highly varying electric field, that impacts the trajectory of the carrier flow. The resulting influence on the output characteristics is shown in Fig. 7. As the fitting parameter becomes smaller, which corresponds to a rougher surface, the on-state resistance increases. For low values of δ the performance of the power MOSFET is significantly reduced. Changing the fitting parameter from $\delta = 2.5 \cdot 10^{12}\ \mathrm{V/s}$ to $\delta = 1.0 \cdot 10^{12}\ \mathrm{V/s}$ leads to an increase in on-state resistance of around 54 % at $T = 25\ ^\circ\mathrm{C}$. At elevated temperature, the reduction in on-resistance due to a higher fitting parameter is less significant as the channel resistance contributes less to the total on-resistance.

C. Gate Oxide

One of the next steps during the fabrication process of a SiC power MOSFET is the creation of the gate oxide. The typical gate oxide, the native oxide of SiC, $\mathrm{SiO_2}$, can be grown by thermal oxidation. The thickness of the thermal oxide is mainly controlled by temperature and time. The growth rate is further influenced by the surface composition. An implanted region, for example, contains weak Si-C bonds which can be oxidized faster [**?**]. A statistical deviation of $\pm 10\ \%$ as well as a deviation of +100 % due to anisotropic growth on stepped surfaces, [**?**], are assumed for the simulation. The gate oxide thickness, which is part of the MOS-capacitor, influences the threshold voltage of the power MOSFET. Its effect on the transfer characteristics of the exemplary device, which has an initial oxide thickness of 40 nm, is shown in Fig. 8. A thicker gate oxide leads to a reduced oxide capacitance and thus to an increased threshold voltage. According to the simulation, an increase of 10 % in thickness results in a shift of $\Delta V_{\mathrm{th}} = 0.5\ \mathrm{V}$ for room and elevated temperature. A 100 % thicker oxide leads to a threshold voltage shift of $\Delta V_{\mathrm{th}} = 5.5\ \mathrm{V}$. If a stripe design is used for the MOSFET, the locally increased oxide affects the entire stripe, since a continuous inversion layer has to be formed. This increase in threshold voltage is intolerably high and has to be avoided by all means in order

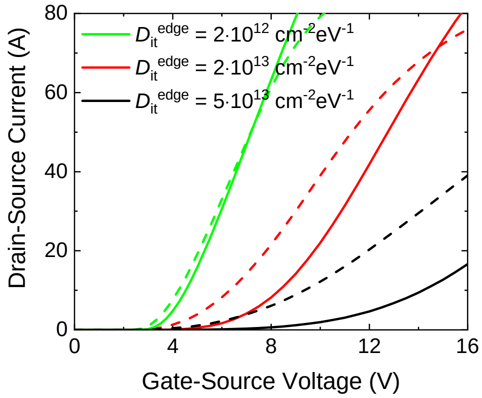

Fig. 9. Influence of gate-oxide thickness on transfer characteristics for $V_{\mathrm{DS}} = 20$ V at $T = 25$ °C (solid) and $T = 150$ °C (dash). 100 % equals 40 nm.

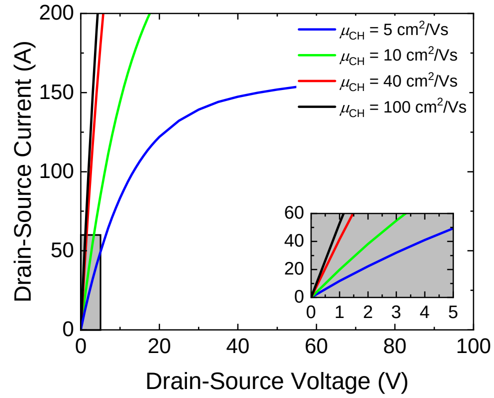

Fig. 10. Influence of channel mobility on output characteristics for $V_{\mathrm{GS}} = 20$ V at $T = 25$ °C.

to have an efficient and reliable device.

D. Interface Traps

The surface morphology, the thermal oxidation and the post-oxidation annealing, which depend on process conditions such as temperature, pressure and gas composition, are responsible for the density of interface traps [?], [?], [?]. The traps located in the channel region affect the threshold voltage by creating a negative charge, in case of acceptor traps. Enhanced Coulomb scattering at the interface additionally reduces the mobility and thus the overall on-resistance.

Within the simulation model, the interface trap density is described by an exponential distribution across the bandgap. To match the measured data of the investigated MOSFET, an acceptor trap distribution with an edge concentration of $2 \cdot 10^{13}$ cm^{-2}eV^{-2} and an exponential decay of 110 meV is used. Varying the edge concentration of the trap distribution significantly shifts the threshold voltage as can be seen in Fig. 9. Reducing the edge concentration by one magnitude, i.e. from $2 \cdot 10^{13}$ cm^{-2}eV^{-2} to $2 \cdot 10^{12}$ cm^{-2}eV^{-2}, results in a 3.75 V lower threshold voltage at $T = 25$ °C. The on-resistance is reduced by 24 % as Coulomb scattering at the interface is less pronounced. At elevated temperature, the amount of occupied traps is reduced due to the change in Fermi level, leading to a smaller threshold voltage shift (1.75 V). Also, the effect on the on-resistance is reduced. The model with reduced trap concentration exhibits an 11 % lower resistance. This shows, that the interface trap density has a significant influence on the electrical behavior especially at low temperatures.

E. Inversion Layer

The surface roughness, the oxide thickness and the interface trap density generate a specific SiC/SiO_2 interface characteristic, which defines the inversion layer mobility or channel mobility of the power MOSFET. As the channel resistance dominates the total on-resistance at medium voltage ranges ($\sim$1500 V), the inversion layer mobility plays a significant role for the power MOSFET under investigation [?]. At common operating conditions ($V_{\mathrm{GS}} = 20$ V, $I_{\mathrm{D}} = 20$ A, $T = 25 - 150$ °C), this mobility is mainly reduced by surface roughness and Coulomb scattering due to interface states.

The inversion layer mobility of the exemplary SiC power MOSFET is around 5 cm^2/Vs at $T = 25$ °C and around $\mu = 10$ cm^2/Vs at $T = 150$ °C. The effect of an improved mobility on the output characteristics at room temperature is shown in Fig. 10. Compared to the original mobility, a mobility of $\mu = 40$ cm^2/Vs reduces the on-state resistance by 73 %. An increase from $\mu = 40$ cm^2/Vs to $\mu = 100$ cm^2/Vs results in a 21 % lower resistance, i.e. the improvement by channel mobility is saturating at some point. The same holds true at elevated temperature, see Fig. **??**. Here, an increase from $\mu = 10$ cm^2/Vs to $\mu = 40$ cm^2/Vs leads to a 53 % lower resistance, a further increase in mobility to $\mu = 100$ cm^2/Vs results in a resistance that is 19 % lower. The beginning of saturation is for both, room and elevated temperature around 50 cm^2/Vs as can be seen in Fig. 11. This result shows that for channel mobilities greater than 50 cm^2/Vs the channel is no longer the dominating contributor to the total on-state resistance of the given 1.2 kV MOSFET, i.e. it is not necessary to achieve bulk mobility in the channel.

The influence on the threshold voltage is not as significant as on the on-resistance, see Fig. 12. Increasing the channel mobility from 5 cm^2/Vs to 100 cm^2/Vs results in a threshold voltage, that is 1.5 V lower, considering the interception of tangent and x-axis.

III. Structural Investigation of Devices

Two of the measured MOSFETs shown in Fig. 2 and Fig. 3, which have a different on-state resistance and threshold voltage ((a): $R_{\mathrm{DS,on}} = 77$ mΩ, $V_{\mathrm{th}} = 7.0$ V; (b): $R_{\mathrm{DS,on}} = 83$ mΩ, $V_{\mathrm{th}} = 7.5$ V) are investigated in more detail by SEM. For this purpose, the TO-247 packaged MOSFETs are cut and prepared by cross section polishing with argon using an ion milling system from Hitachi (IM 4000). An FEI SEM (Magellan 400) is used for imaging with a through-the-lens detector for the potential contrast of the p-body region.

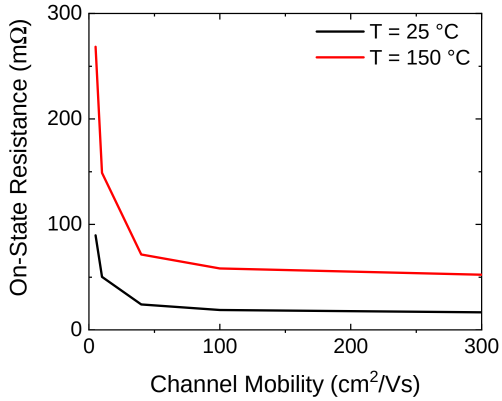

Fig. 11. On-resistance over channel mobility for the calibrated MOSFET model at room and elevated temperatures. The improvement of the on-resistance with increasing mobility saturates above $\mathbf{50\ cm^2/Vs}$.

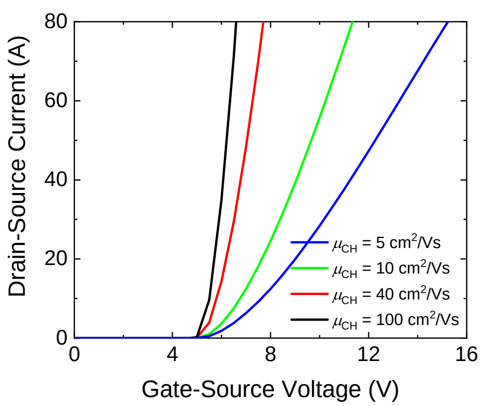

Fig. 12. Influence of channel mobility on transfer characteristics for $\boldsymbol{V_{\mathrm{DS}} = 20\ \mathrm{V}}$ at $\boldsymbol{T = 25\ ^\circ\mathrm{C}}$.

Fig. 14 shows the resulting cross sections of the device cells. While the oxide thicknesses of both cells seem to be identical, the p-bodies appear different. Although, the SEM is not able to measure the doping concentration, it shows a contrast between differently doped areas. The p-body of device (b) appears brighter compared to (a) suggesting a higher doping concentration, which would correspond to the higher threshold voltage. However, only SIMS measurements could give a definite proof.

No other structural differences can be observed between the two cells, i.e. the variation in electrical behavior is due to doping or interface (roughness, traps) variations.

IV. Conclusion

Based on a calibrated simulation model for a 1.2 kV SiC power MOSFET, the influence of processing variations on the device characteristics has been investigated at room and elevated temperature. It has been shown that variations in drift layer thickness mainly affect the breakdown voltage, while its doping concentration significantly influences the on-resistance, especially at higher temperatures, and the threshold voltage. Growing a uniformly thick gate oxide on the epitaxial layer is

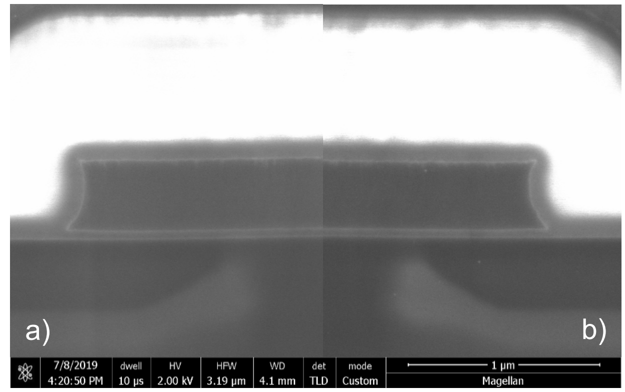

Fig. 13. Cross section SEM of two commercial MOSFETs. Device (a) has an on-state resistance of $\mathbf{77\ m\Omega}$ ($\boldsymbol{I_{\mathrm{D}} = 20\ \mathrm{A}}$) and a threshold voltage of 7.0 V (tangent at maximum slope). Device (b) has an on-state resistance of $\mathbf{83\ m\Omega}$ ($\boldsymbol{I_{\mathrm{D}} = 20\ \mathrm{A}}$) and a threshold voltage of 7.5 V (tangent at maximum slope).

highly affected by stepped surfaces leading to locally increased threshold voltages. The roughness and the trap density of the SiC/SiO_2 interface, which are included in the inversion layer mobility, highly influence the channel resistance and thus the on-resistance of the studied power MOSFET. The threshold voltage is in particular affected by the interface state density as they provide a negative charge, in case of acceptor traps. Simulations, however, have shown that the improvement in on-resistance due to an increasing inversion layer mobility saturates. Once the channel mobility reaches $50\ \mathrm{cm^2/Vs}$, the channel resistance becomes small and other mechanisms, such as the drift doping concentration dominate the output characteristics of the device. This effect is even more pronounced at elevated temperature.

Cross section SEM of two commercial MOSFETs has indicated that a variation in drift layer doping and interface properties are most possible the reason for their deviating behavior.

All in all, it can be stated, that the epitaxial layer should be the focus of processing improving measures, since its doping concentration and surface morphology have a significant impact on the channel mobility, the oxidation process and thus on the overall device performance.

Acknowledgment

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