4H-SiC Power VDMOSFET Manufacturing Utilizing POCl3 Post Oxidation Annealing

4H-SiC Power VDMOSFET Manufacturing Utilizing $POCl_3$ Post Oxidation Annealing

Yanrui Ju[1,a*], Didier Bouvet[2,b], Roger Stark[1,c], Judith Woerle[1,d] and Ulrike Grossner[1,e]

[1]Advanced Power Semiconductor Laboratory, ETH Zurich, Physikstrasse 3, 8092 Zurich, Switzerland

[2]CMI-GE, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland

[a]ju@aps.ee.ethz.ch, [b]didier.bouvet@epfl.ch, [c]stark@aps.ee.ethz.ch, [d]woerle@aps.ee.ethz.ch, [e]ulrike.grossner@ethz.ch

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Abstract. A novel $POCl_3$ post-oxidation annealing recipe was developed. The interface trap density (D_{it}) is extracted by the C-Ψ_S method close to conduction band edge. The performance of the $POCl_3$-treated oxide has been analyzed based on current density-electric field (J-E) measurements. A comprehensive and practical 4H-SiC power VDMOSFET manufacturing traveler has been designed. The power MOSFET fabricated based on this traveler exhibits less than half of the on-resistance and shows improved interface characteristics compared to a similarly designed commercial power MOSFET.

Introduction

The existence of interface traps at the SiC/SiO_2 interface is well investigated. Trapped charge at the interface, which is a function of the trap density and band bending, reduces the mobility due to Coulomb scattering, increasing channel resistance and restricting fast switching. Nitride-based post-oxidation annealing with N_2O or NO is a conventional method widely used in industrial production [1]. As an emerging approach, post-oxidation annealing in $POCl_3$ was demonstrated resulting in much higher peak mobilities than with nitridation [2-4]. Since the requirements on the precursor gas and furnace are also compatible with a conventional Si device manufacturing line, it has the potential to become a promising alternative for mass production. The purpose of this work is to explore the possibilities of adapting $POCl_3$ annealing for the fabrication of 4H-SiC power VDMOSFETs.

$POCl_3$ Annealing Process and MOS Capacitor Characterization

To the best of the authors' knowledge, $POCl_3$ experiments published with detailed process conditions had the $POCl_3$ bubbler temperature controlled at 15 °C during the process [2-4]. The annealing in this work is carried out with the bubbler temperature at 20 °C. The annealing atmosphere was a gas mixture with the ratio equal to N_2 carrier gas:O_2:main N_2 of 0.6:1:2.5. Based on the flow, the $POCl_3$ to total N_2 ratio is 0.007531. The sample used in this work was an n-type 4H-SiC substrate with an 11 µm thick, n-type epitaxial layer ($N_D = 8 \times 10^{15}$ $cm^{-3)}$ on top. Multiple cleaning solutions including a sulfuric peroxide mixture (SPM), RCA clean, and aqua regia were applied prior to gate oxidization. Starting from here, two types of devices have been fabricated: the first type, called 'full $POCl_3$', is the usual approach where the entire thermally grown gate oxide is doped with $POCl_3$. The second kind, here referred to as 'partial $POCl_3$', was processed with an alternative method described below. The first type of MOS capacitors were oxidized at 1250 °C, yielding an oxide thickness of around 25 nm. The second type received a rapid oxidation at the same temperature, aiming for 6 nm oxide thickness. Then, the samples were annealed in a $POCl_3$ tube at 1000 °C for 10 min. Another 20 nm oxide using TEOS was deposited by LPCVD on the "partial $POCl_3$" samples, followed by a densification annealing in N_2. The final oxide thickness of around 49 nm was identical for both MOS capacitors. Finally, the gate and anode electrodes were formed by a low stress W sputtering. All the post $POCl_3$ annealing, including densification and gate sintering, were performed at temperatures below 900 °C to avoid the redistribution of phosphorus. The MOS capacitors manufactured using the developed $POCl_3$ post-oxidation annealing recipe were then characterized electrically.

Capacitance-Voltage Analysis

All CV measurements show negligible frequency dispersion for both MOS capacitors as shown in Fig. 1. The comparatively high capacitance of the partial $POCl_3$ sample in the depletion region suggests a higher interface trap density at its interface.

An improved interface quality of the "partial-$POCl_3$" sample is further indicated by a lower D_{it} values, which were extracted by the C-Ψ_S method [5] (Fig. 2). If a significantly high-interface-trap density remained at the interface, a small derivation of the surface potential ($\Delta\varphi_s$) causes a large the amount of interface traps charged or discharged (ΔQ_{it}). The equivalent interface state capacitance $C_{it} = \Delta Q_{it}/\Delta\varphi_s$ will therefore increase. The total bulk capacitance in the semiconductor, which is equal to C_{it} connecting in parallel with the depletion capacitance (C_{dep}), $C_{s,tot} = C_{it} + C_{dep}$, will rise accordingly. Therefore, the measured capacitance in the range below flatband voltage of the partial $POCl_3$ MOS capacitor is larger than the value of full $POCl_3$ MOS capacitor. As $C_{s,tot}$ is connected in series with the gate dielectric capacitance (C_{ox}), the total capacitance (C_{tot}) is $\frac{1}{C_{tot}} = \frac{1}{C_{s,tot}} + \frac{1}{C_{ox}}$. Approximating the real part of the dielectric constants of partial and full $POCl_3$ oxide are identical, namely, the equivalent oxide thickness (EOT) is the same. As seen from the CV analysis (Fig. 1), C_{ox} starts to play a dominant role in deciding total capacitance at the more negative voltage in partial $POCl_3$ MOS capacitors compared to the one in full $POCl_3$ samples. Therefore, the flatband voltage of partial $POCl_3$ is more negative than for the full $POCl_3$ MOS capacitor. Accordingly, the negative shift of the flatband voltage is assumed being caused rather by traps than the positive charge induced by phosphorus. [6] The dispersion of capacitance under quasi-static and high frequency measurement of full $POCl_3$ MOS capacitor may result from more traps induced by $POCl_3$ annealing in oxide as it probably responses with quasi-static bias but cannot follow the high frequency.

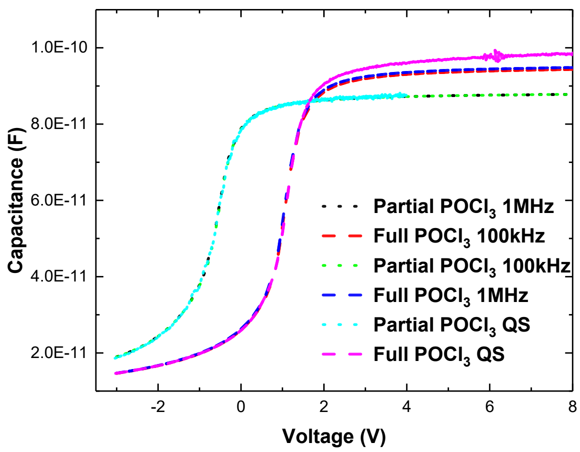

Figure 1. C-V curves of the partial $POCl_3$ and Full $POCl_3$ MOS capacitors at 100 kHz, 1MHz and in a quasi-static configuration.

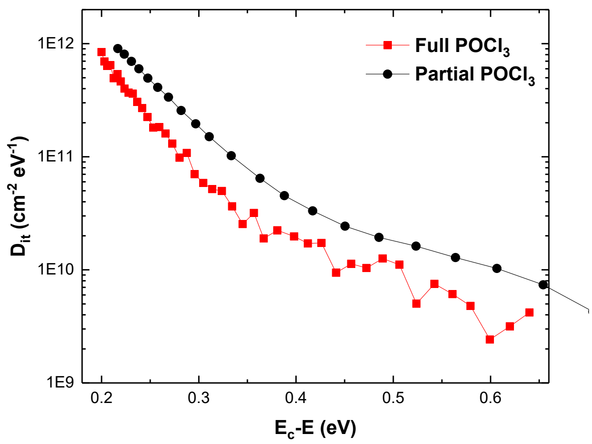

Figure 2. D_{it} extracted using the C-Ψ_S method.

Current-Voltage Analysis

To capture the permanent breakdown of the oxide, two kinds of capacitors with the same diameter of 600 µm were stressed under current density-electric field (J-E) measurements. The partial $POCl_3$ MOS capacitor had an almost two orders of magnitude lower leakage current at medium electric field than the full $POCl_3$ sample. Comparing to the leakage current of the partial $POCl_3$ capacitor due to the Fowler–Nordheim tunneling, the higher leakage current of the full $POCl_3$ capacitor may originate from more electron trapping in the gate oxide, which is also verified by bias temperature stress (BTS) measurement [3]. The leakage current for both samples was lower than 9 µA/cm^2 until an abrupt breakdown at around 9.34 MV/cm occurred.

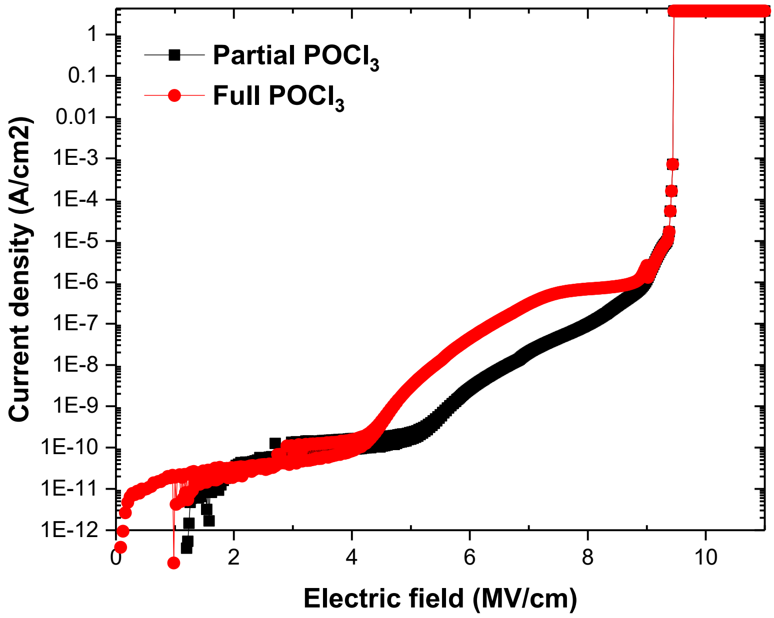

Figure 3. Current density- electric field measurement of the partial $POCl_3$ and full $POCl_3$ MOS capacitor.

Power VDMOSFET Frontend Manufacturing Process

In order to see the effect of $POCl_3$ annealing on the electron mobility, power VDMOSFETs with test structures were fabricated. The ion implantation sequence was p+, Junction Termination Extension (JTE), guard ring, p well, and n+ source. The implantation profile of the p well was a retrograded profile with the junction depth at around 1.1 µm as simulated by an in-house program based on Pearson IV [7]. The total p well implantation dose was 2.4e14 cm^{-2}. The sample was annealed at 1650 °C with the surface covered by a carbon cap. Another sacrificial thermal oxidation at 1100 °C for 1 hr was applied after carbon cap stripping in order to improve the cleanliness of the surface and to reduce defects in the SiC bulk.

Subsequently, the field oxide was patterned. The samples were loaded into an oxidation furnace immediately after the pre-oxidation clean to prevent the formation of the native oxide. The oxidation temperature was 1250 °C. The annealing in $POCl_3$ was then performed according to the previously described “partial $POCl_3$” process. The equivalent oxide thickness (EOT) is controlled to reach around 43 nm. The final oxide thickness was determined by ellipsometry measurements. Tungsten was chosen as the gate electrode in this work since it is a refractory metal and frequently used as the gate material in the high-k process. Finally, a 200 nm thick low-stress tungsten was sputtered as the gate electrode and patterned by the lithography and an RIE etch with high W/SiO_2 selectivity.

Power VDMOSFET Backend Manufacturing Process

The inter-layer dielectric (ILD) was deposited by ALD (SiO_x) and PECVD (TEOS). ALD SiO_x is required since it provides better conformal shape and prevents the formation of voids. The oxide was then etched for the contact slot opening by using a high selectivity SiO_x/SiC RIE process. Ni was evaporated on both sides of the native-oxide-free face of the chip. The source/drain metal silicide was formed simultaneously by annealing at 950 °C for 1.5 min. The unreacted Ni was then removed using heated Ni etchant. The final source and drain metallization was sputtered by PVD. The source metal on the front side was Al, while the drain metal on the backside was Ni/Ag. The source Al metal and metallic oxide were etched by ICP. For the final passivation layer, SiO_x was used.

Power MOSFET Characterization

For the mobility extraction, lateral NMOSFETs, fabricated on the same die as the power VDMOSFET, were used and a peak effective mobility of 70 $cm^2V^{-1}s^{-1}$ was measured as shown in Fig. 4. The channel length of the analyzed device was 10 µm and the width was 200 µm.

Fig. 5 presents I_d-V_g curves of the power VD-NMOSFETs. The active area is approximated to 5.4 mm^2. The threshold voltage is 2.5 V, extrapolated from the subthreshold exponential region. Lower V_T could be tailored by decreasing the $POCl_3$ annealing temperature. As outlined above in the post-oxidation annealing section, lower annealing temperatures, for instance, 950 °C, lead to higher phosphorus concentration and lower D_{it} at the interface. In addition, phosphorus also plays an important role as fixed positive charge at the interface. Therefore, the flat-band voltage also will be reduced. However, the mobility may be reduced as well in lower temperature annealing conditions. The specific on-resistance, extracted from Fig. 6, is 195 mΩ at V_{gs} = 10 V, I_d = 25 A, T_J = 25 °C (junction temperature), which, under the same bias, is about half of the value of the commercial MOSFETs [7].

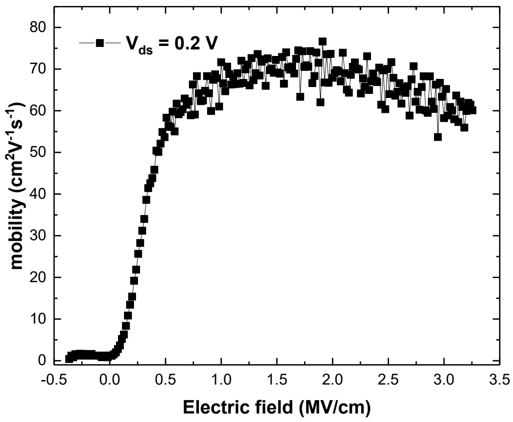

Figure 4. Mobility extraction from the transfer characterization of the test low voltage lateral MOSFET with L = 10 µm and W = 200 µm.

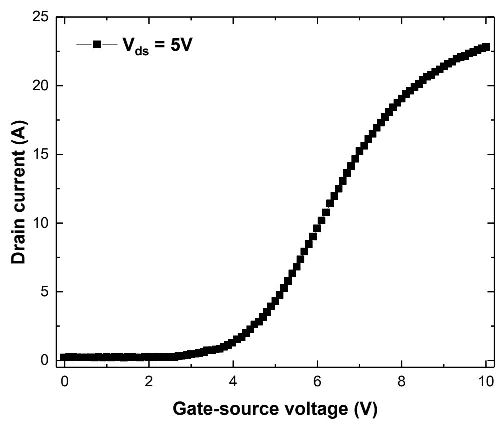

Figure 5. Transfer I_d-V_g characterization of the power MOSFET.

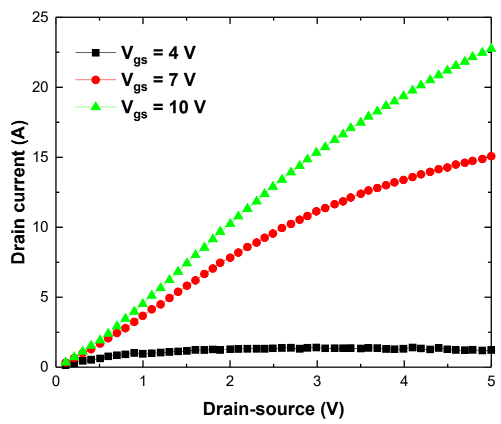

Figure 6. Output I_d-V_d characterization of the power MOSFET, extracted from a pulsed measurement.

The source Al metal layer of the measured power MOSFET is only about 800 nm thick. Such thin metal layer is unfavorable for the current spreading. Moreover, during the I_d-V_d large current measurement, the probing needles were badly connected to the source metal. Therefore, the Al source layer was burnt out after several measurements due to the current crowding. However, the MOSFET was still functioning with reduced output current after a local Al melting as shown in Fig. 7.

The C-V curves of the power VD-NMOSFETs, which are plotted in Fig. 8, are similar to the commercial device [8]. In comparison, the peak-like shape in C_{rss} and C_{oss} at low V_{ds} observed in Ref. [8], is not present here. One explanation of this could be that the near surface JFET region is modified with higher n-type doping in [8] such that the equivalent dopant concentration varies with the depletion depth developing below the gate overlay at the JFET area. Excess doping reduces the parasitic JFET resistance and lowers the quasi saturation effect during on-state. No JFET implantation step was performed for the devices shown here.

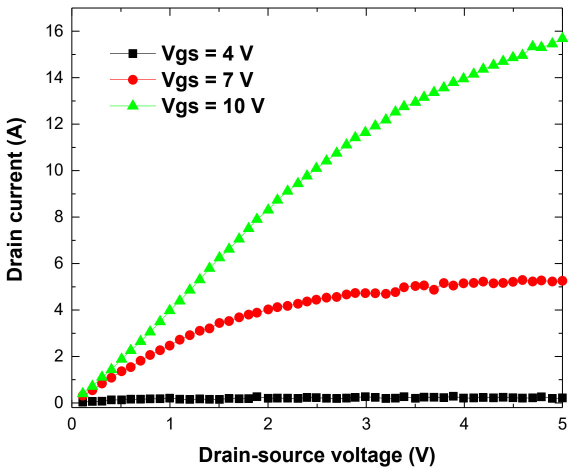

Figure 7. Output I_d-V_d characterization of the power MOSFET after the Al source metal was molten.

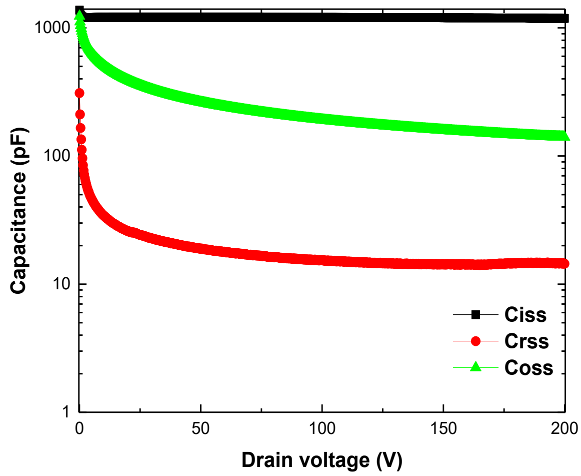

Figure 8. Capacitance voltage (C-V) characterization of the power MOSFET. The junction temperature is 25 °C, the V_{AC} is 30 mV, the frequency is 1 MHz.

Summary

In this work, a full 4H-SiC power MOSFET process based on a novel $POCl_3$ post oxidation annealing recipe has been developed. The interface trap density was effectively decreased by annealing. The oxide formed with this method shows good reliability and could therefore be used as gate oxide in power VDMOSFET manufacturing. The characterization of the fabricated power VDMOSFET proves the significant drop of the specific on-resistance and comparable CV properties as measured for a similar commercial power VDMOSFET.

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